

# **QML Process Optimizations**

Texas Instruments is certified and listed by the Defense Supply Center Columbus (DSCC) as a manufacturer of QML Class B and Class V microcircuits (integrated circuits) in accordance with MIL-PRF-38535 (General Specification for Manufacturing Integrated Circuits). The Quality System utilized by Texas Instruments in the manufacture of these microcircuits is fully compliant to the requirements of MIL-PRF-38535 and ISO9001. All processing, screening, and Quality Conformance Inspection (QCI) is performed in compliance with the test methods of MIL-STD-883, Microcircuits Test Method Standard, with exceptions as allowed by Paragraph 1.1 of MIL-PRF-38535. Under MIL-PRF-38535, a QML certified manufacturer is permitted to modify, substitute, or delete tests that do not improve the quality and/or reliability of the finished device as defined by the applicable device specification. All TI QML Class V flows are approved by DLA, NASA, and the Aerospace Corporation.

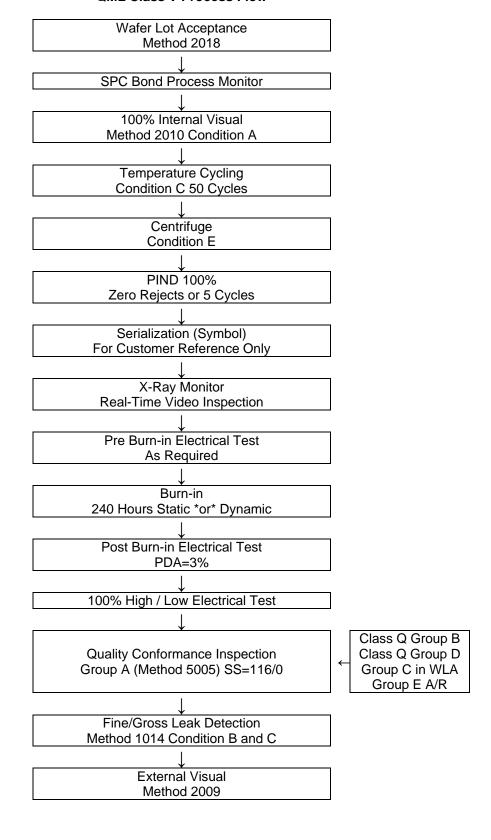
The elimination of screens and test is reflected on the Texas Instruments Processing Conformance Report attached to the Certificate of Conformance provided with each QML ceramic device lot. Approvals for these optimizations are granted by the QML manufacturer's Technology Review Board. Please note that under the QML program, only changes to Form, Fit, or Function are detailed in the DLA Standard Microcircuit Drawing (SMD). As a courtesy to our customers, Texas Instruments provides notification of optimizations via the Government Industry Data Exchange Program (GIDEP) Process Change Notification system.

### QML Class V Processing Baseline

The production baseline processing flow for TI QML Class V products is shown below. MIL-STD-883 Test Method 5004 specifies the processing requirements for Class Level S devices. The requirements are also listed along with any exceptions. Please note that these exceptions are considered non value-added (NVA) as qualification performed in accordance with MIL-PRF-38535 has determined that form, fit, function, or reliability is not affected.

Of particular note is the absence of read-and-record data collection and delta calculation. Texas Instruments warrants products to meet the DSCC SMD or JAN Slash Sheet as specified with respect to delta limits. Full characterization studies including drift analysis are performed at product release and after any major changes to assure shipped product meets these requirements.

# Texas Instruments **QML Class V Process Flow**



MIL-STD-883 TM-5004 100% Processing For Level S Devices				
Level S Requirement	TI Class V DSCC Approved Flow NVA Exception			
Wafer lot acceptance				
Nondestructive bond pull by device	Replaced with destructive bond pull monitor			
Internal visual				
Temperature cycling				
Constant acceleration				
Visual inspection				
Particle impact noise detection (PIND)				
Serialization	For customer reference only – not			
	used during test or shipment			
Pre burn-in electrical parameters	No read and record data			
Burn-in test				
Interim (post burn-in)				
Reverse bias burn-in	One burn-in only either static or dynamic			
Interim (post burn-in)	·			
Percent defective				
Final electrical test				
Delta Calculations per device spec	Not performed – devices warranted to meet SMD delta limits			
Seal				
Radiographic Inspection 100%	Replaced with real-time x-ray monitor			
QCI sample selection	See below			
External visual				
Radiation latch-up	Per detail device specification			

#### QML Class V QCI Baseline

The Quality Conformance Inspection (QCI) baseline for TI QML Class V products is shown below. MIL-STD-883 Test Method 5005 specifies QCI for Class Level S devices. The requirements are listed along with any exceptions. Again note that these exceptions are considered non value-added (NVA) as historical data and qualification performed in accordance with MIL-PRF-38535 has determined that form, fit, function, or reliability is not affected.

The most apparent change is the elimination of the by-lot Level S Group B. In place of this, TI has implemented a life test (Group C) as part of Wafer Lot Acceptance (WLA) and added die shear to the Level B Group B. Level B Group D is performed as shown.

Group B is performed generically for each week of seal using representative samples from each package family. Group D is also performed generically every 26 weeks using representative samples from each package family. The shipping coverage window for Group D is 36 weeks. Note that D8 (lid torque) has been eliminated based on process controls and historical data.

	Texas Instruments Class Level V Quality Conformance Inspection (QCI)				
Test /		MIL-STD-883			
Sub- Group	TEST	METHOD	CONDITION	SAMPLE / ACCEPT	COMMENTS
Group B					Frequency - once each week of seal for each package family and lead finish
B1	a. Resistance to Solvents	2015		3/0	
B2	a. Bond Strength	2011	C or D	22 / 0	3 devices minimum / 22 wires total
	b. Die shear	2019or /2027		3/0	
В3	a. Solderability	2003	245C +/- 5%	15 / 0	4 devices minimum / 15 wires total

	Texas Instruments Class Level V Quality Conformance Inspection (QCI)				
Test / MIL-STD-883					
Sub- Group	TEST	METHOD	CONDITION	SAMPLE / ACCEPT	COMMENTS
Group C C1	a. Steady-state life test b. End-point electrical test	1005	1000 hrs/125C or equivalent Use QA final test program/ temperatures	45 / 0	Frequency – each wafer lot

Texas Instruments Class Level V Quality Conformance Inspection (QCI)					
Test/	MIL-STD-883				
Sub- Group	TEST	METHOD	CONDITION	SAMPLE / ACCEPT	COMMENTS
Group D					Frequency - once every 26 weeks for each package family with a 36 week shipping window
D1	a. Physical Dimensions	2016		15 / 0	
D2	a. Lead Integrity	2004	Condition B2	45 /0	3 devices minimum / 45
	b. Seal (Fine and Gross)	1014	As applicable		icado total
D3	a. Thermal Shock b. Temperature Cycle c. Moisture Resistance d. Visual	1011 1010 1004 1004 and	Condition B, 15 cycles Condition C, 100 cycles	15 / 0	
	Examination e. Seal (Fine and Gross) f. End-point electrical test	1010 1014	As applicable Use QA final test program/ temperatures		
D4	<ul><li>a. Mechanical Shock</li><li>b. Vibration, Variable</li></ul>	2002 2007	Condition B Condition A	15 / 0	
	Frequency c. Constant acceleration d. Seal (Fine and Gross) e. Visual Examination f. End-point	2001 1014 1010 or 1011	Condition E Y1 axis only As applicable Use QA final test		
	electrical test		program/ temperatures		
D5	<ul><li>a. Salt Atmosphere</li><li>b. Visual Inspection</li><li>c. Seal (Fine and Gross)</li></ul>	1009 1009 1014	Condition A As applicable As applicable	15 / 0	
D6	a. Internal water vapor	1018	5000 PPM @ 100C	3 / 0 or 5 /1	Third party lab
D7	a. Adhesion of lead finish	2025		15 / 0 leads	Not for LCCC
D8	a. Lid torque	2024		None	Not performed for TI
Note: Any deviations to test methods or conditions, such as centrifuge, will be specified in the device traveler.					

MIL-STD-883 TM-5005 Group B (By Lot) QCI For Level S				
Level S Requirement	TI Class V DSCC Approved Flow NVA Exception			
Subgroup 1 a. Physical dimensions b. Internal water-vapor	Performed as part of Generic Group D QCI by package family with 36 week window			
Subgroup 2 a. Resistance to solvents b. Internal visual and mechanical c. Bond strength d. Die shear/substrate attach strength test	Subgroups a, c, and d are performed as part of Generic Group B QCI by package family by week of seal. Subgroup b is covered by 100% pre-cap inspection.			
Subgroup 3 a. Solderability	Performed as part of Generic Group B QCI by package family by week of seal.			
Subgroup 4 a. Lead integrity b. Seal c. Lid torque, lead fatigue	Performed as part of Generic Group D QCI by package family with 36 week window. Lid Torque testing eliminated for all package families.			
Subgroup 5 a. End-point electrical parameters b. Steady state life c. End-point electrical parameter	Performed as part of Wafer Lot Acceptance by wafer lot.			
Subgroup 6 a. End-point electrical parameters b. Temperature cycling c. Constant acceleration d. Seal e. End-point electrical parameters	Performed as part of Generic Group D QCI by package family with 36 week window			

MIL-STD-883 TM-5005 Group D QCI Levels B and S			
Level S Requirement	TI Class V DSCC Approved Flow NVA Exception		
Group D per MIL-STD-883	D8 Lid Torque testing eliminated for all package families - Class Q and Class V		

## TI QML Class Q Process Flow with Example Optimizations

## Class M and Class B **Example TI Class Q Optimization** Wafer Fabrication Wafer Level Reliability Monitors Wafer Preparation Die Mount & Cure Wire Bond Bond Pull and Die Shear (Sampled) Method 2011 & Method 2019 Internal Visual - Not Performed Method 2010 Condition B 100X Internal Visual ← Performed with 100X criteria Method 2010 Condition B 40X Internal Visual Lot Acceptance Seal Temperature Cycle ← Not Performed (10 Cycles -65°C/+150°C) Constant Acceleration ← Not Performed (30KG Y1 Plane) Topside Symbol Ambient Pre-Burn-In Electrical Test (Optional) Burn-In – 160 Hours / 125°C ← Not Performed or Duration Reduced (Method 1015 Condition A or D - Manufacturer's Option) Ambient Post-Burn-In Electrical Test Percent Defect Allowable (PDA) Calculation ← Not Performed If Burn-in Eliminated High Temperature Post-Burn-In Electrical Test Low Temperature Post-Burn-In Electrical Test ← Not Performed Group A Lot Accept (116/0) ← Not Performed At Low Temperature Fine & Gross Leak Detection (Method 1014 Condition B and C) External Visual (Method 2009) Pack & Ship QCI Group B (Generic by Package Family) QCI Group C (Generic by Microcircuit Group)

QCI Group D (Generic by Package Family) For QML Class Q devices Texas Instruments has qualified the modification and/or elimination of several screens and tests as approved by the Texas Instruments Technology Review Board (TRB). These include, but are not limited, to:

- Elimination of -55°C testing on multiple logic products including the TTL, LS, S, HC, AHC, AHCT, ALS, AS, F, ABT, AC, ACT, and BCT families.
- Elimination of -55°C testing on specific mixed signal products including the majority of CMOS technology based product families.
- Elimination of burn-in or replacing 100% burn-in with lot acceptance on multiple product technologies.
- Elimination of Group A lot acceptance testing on specific DSP and logic product families.
- Elimination of 100% temperature cycle and centrifuge for all low pin count ceramic devices (28 pin and below).
- Replace 100X pre-cap inspection with 40X pre-cap inspection using the 100X criteria for all product families.

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