Altera Stratix IV FPGA Interface for LTM9011 ADC with LVDS Outputs

Gary Yu

Summary

This document shows how to interface a Linear Technology LTM®9011 8-channel, simultaneous sampling 14-bit analog-to-digital converter (ADC) with high speed serial low voltage differential signaling (LVDS) to Altera Stratix IV FPGAs utilizing the dedicated I/O functions of the FPGA family.

Introduction

This document details the interface of an Altera Stratix IV FPGA to a high speed LTM9011 ADC from Linear Technology. Implementation is demonstrated via the LTM9011 demo board DC1884A and a Stratix IV GX FPGA development board contained in the Stratix IV GX FPGA development kits.

To learn more detailed information regarding the Stratix IV GX FPGA development kits and Linear Technology DC1884A, refer to:

- www.altera.com/products/devkits/altera/kit-siv-gx.html
- http://www.linear.com/demo/DC1884A

The FPGA design, implementation and simulation are described here.

ADC LVDS Interface

The LTM9011 is a high speed, octal ADC with a serial LVDS interface. Each channel output can be configured in 2-bit (2-lane) mode or 1-bit (1-lane) mode. This document only demonstrates 2-lane mode and 16-bit format (14 bits of data with two dummy bits per frame) supporting the maximum sampling rate up to 125Msps per channel.

The LTM9011 integrates two quad channel 14-bit ADCs similar to the LTC2175, as shown in the block diagram in Figure 1. The sample clock, ENC±, launches the A/D conversion and the output sample data are carried on two serial data streams. Each 14-bit sample is formatted as 16 bits while the LSBs always contain zeroes. Data bits are synchronized with the bit clock, DCO±, and the sample boundaries are indicated by the frame signal FR±. For more about LTM9011, see the data sheet at http://www.linear.com/product/LTM9011

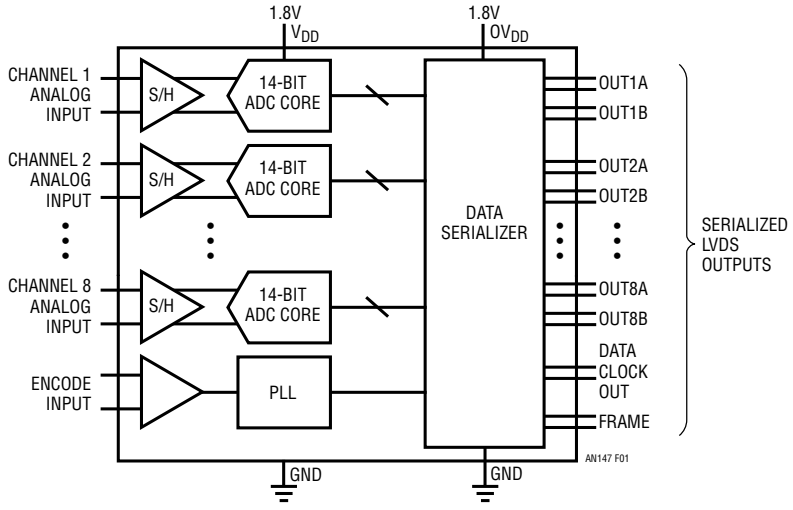

Figure 1. LTM9011 Block Diagram

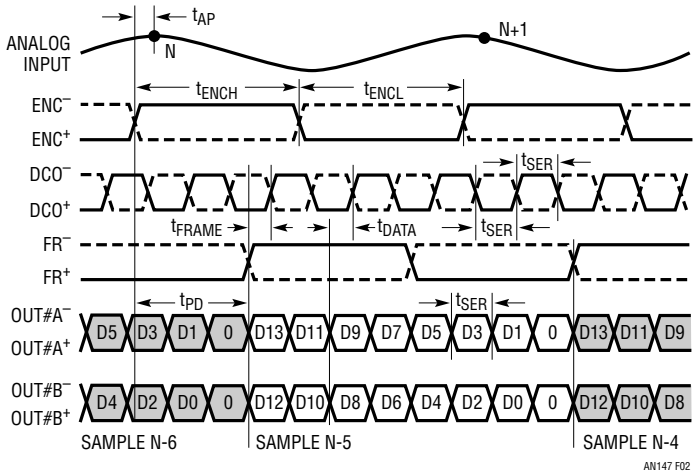

Figure 2. LTM9011 Interface Timing Diagram

Table 1. LTM9011 Interface Timing Diagram

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{AP}	Sample-And-Hold Acquisition Delay		0		ns
t_{ENCL}	Sample Clock Low Time	2	4	100	ns
t_{ENCH}	Sample Clock High Time	2	4	100	ns
t_{SER}	Serial Data Bit Period	1			ns
t_{DATA}	DATA to DCO Delay	0.35	0.5	0.65	ns
t_{FRAME}	FR to DCO Delay	0.35	0.5	0.65	ns
t_{PD}	Propagation Delay	2.7	3.1	3.5	ns

Demonstration System Architecture

The Stratix IV GX FPGA development board is a hardware platform for developing and prototyping low power, high performance and logic-intensive designs. The board contains a Stratix IV GX FPGA EP4SGX230KF40 (BGA 1517 pins) and offers a wide range of peripherals and interfaces to facilitate the development.

The DC1884A demo board is connected to the FPGA board through a high density flexible cable, SAMTEC SCF-156146-02-MA, adapting the SAMTEC SEAF (FMC) connector of the demo board to a high speed mezzanine card (HSMC) connector (J2) of the FPGA board. This connection carries 20 high speed LVDS lines: 16 lines for data OUT#A and OUT#B, two lines for data clock DCOA and DCOB and two lines for the frame signals FRA and FRB, which are generated by the LTM9011 on the DC1884A demo board. The LTM9011 requires an external clock source with ultralow jitter as a sample clock (ENC) and eight analog signal inputs.

The FPGA board includes an embedded USB blaster to allow the host to program the FPGA via a JTAG interface over a type-B USB cable. The host can also use this interface to dynamically capture data and set up parameters from the FPGA internal block memory during operation.

Alternately, the data of a specified channel can be retrieved with an associated clock and control signal through a parallel I/O interface assigned to J1 of the FPGA board.

This FPGA can also drive an LCD module card to display configuration information including buffer size, FPGA status and the channel number, which is specified for the parallel data output. The configuration and display logic utilize a second clock domain, SYSCLK, which is derived from a 50MHz onboard oscillator.

The DC1884A demo board has an SPI interface for the LTM9011 for internal configuration and is controlled by the DC590B USB to SPI controller or DC2026 Linduino microcontroller board.

I/O Architecture of Stratix IV FPGA

The Stratix GX device includes a built-in serializer/deserializer (SERDES) circuit that supports high speed LVDS interfaces at data rates of up to 1.6Gbps. Pin assignment is important in Stratix IV FPGA LVDS applications because only some of the I/O blocks support full LVDS features and only some of the PLLs support these I/Os. The Stratix IV device family supports LVDS on both row and column I/O banks.

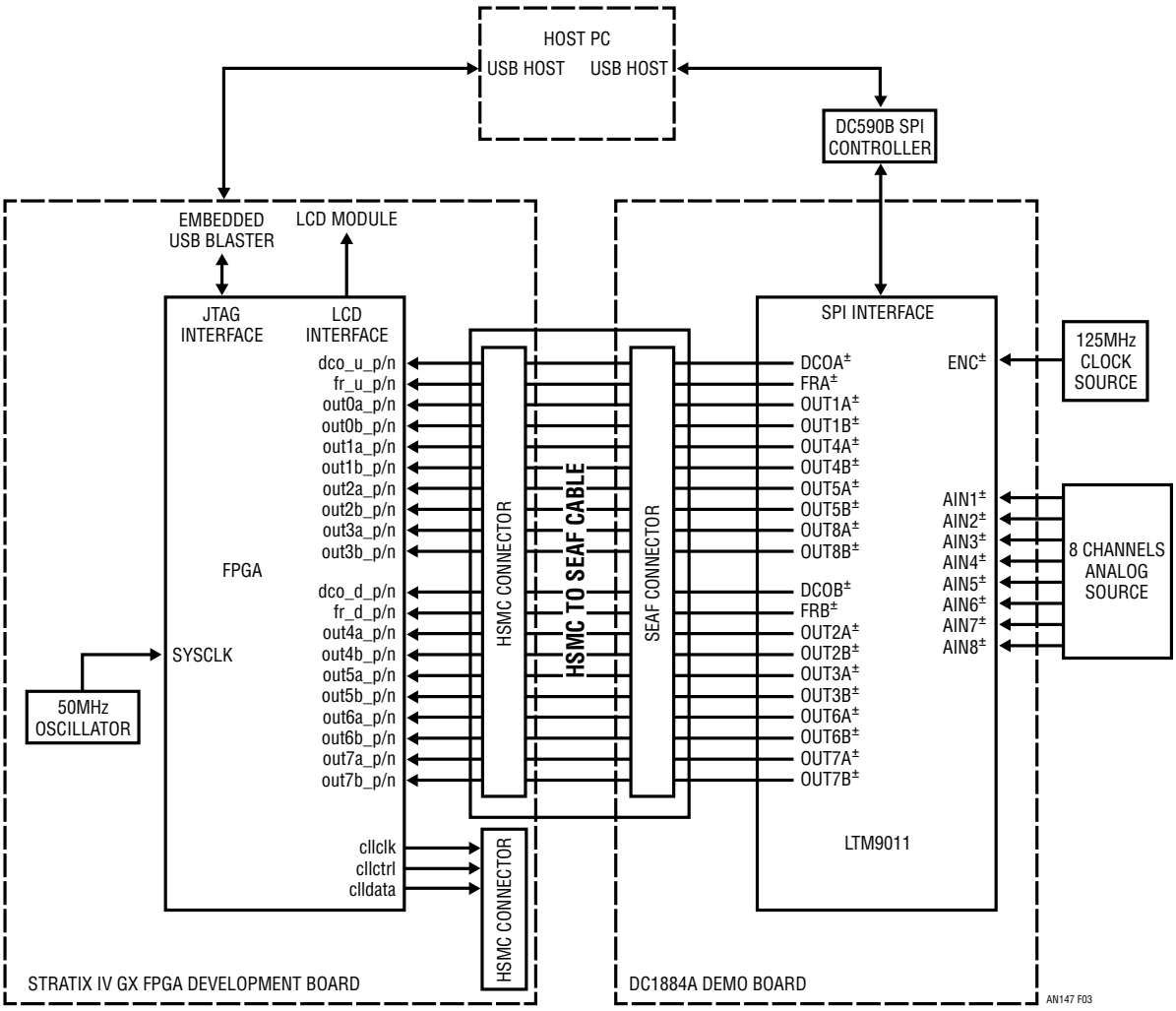

Figure 3. Demonstration System Architecture

- Column I/O buffers (located on top and bottom sides) are connected to single-ended pads and need external termination schemes to support the LVDS I/O standard.
- Row I/O buffers (located on left and right sides) are true LVDS buffers and only PLLs located on the left and right sides support these I/Os.

Dedicated SERDES circuitry is implemented on the row I/O banks with further enhanced LVDS interface performance in the device. For column I/O banks, the SERDES is implemented in the core logic because there is no dedicated SERDES circuitry on column I/O banks. The following dedicated components are contained in the SERDES circuitry:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- DPA (dynamic phase aligner)
- Synchronizer (FIFO buffer)
- Phase-locked loops (PLLs)

The direction of true differential I/O buffers is not configurable. The specific pin only supports one direction of data flow.

This application uses only differential receivers. The receiver has a differential buffer, the left or right PLL that generates the clocks only for SERDES, a DPA block, a synchronizer, a data realignment block and a deserializer. The differential buffer can receive LVDS, mini-LVDS, and RSDS signal levels, which are statically set in QUARTUS II software assignment editor.

The PLL is fed by an external clock, DCO, divided by the serialization factor from the LTM9011, and generates different phases of the same clock. The serial data, one line of data or frame stream in this application, is fed to the DPA circuitry first through differential data input buffers. The DPA block chooses one of the clocks and aligns the incoming data on each line.

The synchronizer circuit is a 1 × 6-bit deep FIFO buffer that compensates for any phase difference between the DPA clock and the data realignment clock.

The user-controlled data realignment circuitry (bit slip) inserts a single bit of latency in the serial bit stream to align to the word boundary.

The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits configured by the serialization factor (×3, ×4, ×6, ×7, ×8, or ×10) to the internal logic. The first bit is the MSB of the parallel data.

The DPA block takes in high speed serial data from the differential input buffer and selects one of the eight phases generated by the left and right PLL—the one closest to the phase of the serial data—to sample the data. The maximum phase offset between the received data and the selected phase is 1/8 UI, the maximum quantization error of the DPA. The eight phases of the clock are equally divided, offering 45° resolution.

Table 1 and Figure 2 illustrate the bit rate of each line going up to 1Gbps, if each channel's maximum sample rate is 125Msps and data format is two lines of 16-bits. If the serialization factor is set to ×8, the parallel data bus generated by the deserializer to the FPGA fabric operates under the clock (RX_SYNCCLOCK) maximum of 125MHz. That is not critical. The ultrahigh speed parts are only handled by the FPGA using dedicated SERDES blocks.

The interesting timing issue may be how to handle channel-to-channel skew caused by the system architecture. The total propagation delay from ENC to the output of the deserializer for each channel of the LTM9011 is:

total propagation delay = jitter of ENC + t_{PD} + t_{AD} + PCB delay (FPGA board + DC1884) + cable delay + input buffer of FPGA delay.

where:

t_{AD} is the analog-to-digital conversion time equal to 5 • (t_{ENCH} + t_{ENCL}).

Max jitter of ENC (73.1dB SNR, analog frequency is 70MHz) is less than 1ps

Max differential of t_{PD} at 125Msps is 0.8ns

Max differential of PCB delay if matching the lengths of the differential traces ±5mil on FR4 is less than 10ps

Max differential of cable delay is less than 10ps

So the maximum skew for channel-to-channel from DCO to the input of the DPA is 0.001 + 0.8 + 0.01 + 0.01, or less than 1ns. Add the additional maximum phase offset of 0.125 • t_{SER} generated by the DPA to calculate the

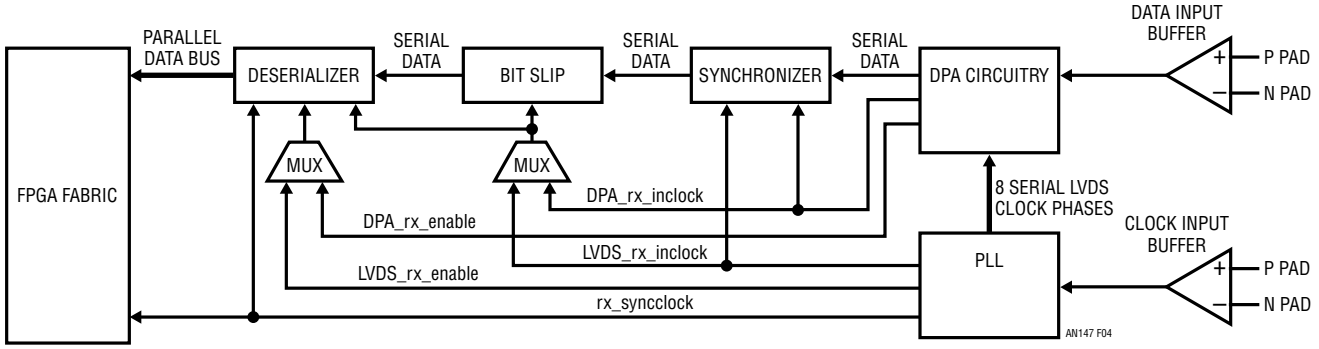

Figure 4. Stratix IV Differential Receiver

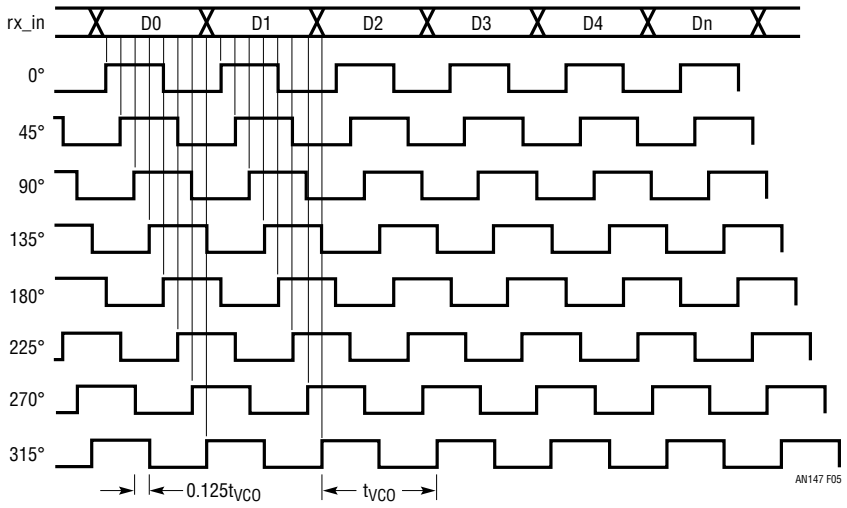

Figure 5. DPA Clock Phase to Serial Data Timing Relationship t_{VCO} Equal to t_{SER}

maximum of skew from DCO to parallel output, or less than 1 + 0.125 • t_{SER} or (1.125/8) • $t_{RX\_SYNCCLOCK}$). It is easy to latch the channels' parallel data bus by shifting RX_SYNCCLOCK more than 1/4 cycle.

There is one factor of uncertainty. The LTM9011 actually integrates two LTC2175-Style quad channel cores into one package, which shares one pair of differential clock pins (ENC). There is some skew between the two ENC inputs of each core, which causes skew between clock domain A (DCOA, FRA, channel 1, 4, 5, 8) and clock domain B (DCOB, FRB, channel 2, 3, 6, 7). The skew is not specified in the LTM9011 data sheet, but test results show that it is negligible in this application.

FPGA Design

In this application, two lines of serial data from one channel in 16-bit format are converted to 16 bits of parallel data, which is synchronized with the clock (RX_SYNCCLOCK) by configuring the serialization factor to ×8. So the eight channels of sixteen lines of serial data with two frame signals from the LTM9011 are converted to a 144-bit wide parallel data bus containing eight samples and two frame signals.

The ALTLVDS MegaWizard Plug-In Manager software allows the user to choose whether to implement the LVDS interface via an external PLL or automatically provide the PLL. With the "Use External PLL" option disabled (Figure 6), the tool automatically creates an LVDS receiver with a PLL. The advantage of this solution is that the clock tree implementation and timing constraints are relatively easy. The disadvantage is that this PLL can't be customized—an additional PLL may be required to divide an external clock source from the LTM9011 by ×8 and generate other necessary clock sources for FPGA logic usage.

With the "Use External PLL" option enabled (Figure 7), the tool generates an LVDS receiver without a PLL. A dedicated PLL must be configured to generate all clock sources for the LVDS receiver to exactly meet its timing requirements and those for other FPGA logic. The advantage of this method is that we have control over the PLL settings, such as dynamically reconfiguring the PLL to support different data rates, dynamic phase shift, and other settings.

Multiple LTM9011 Concept

Figure 8 shows a solution for multiple LTM9011s. To implement the LVDS receivers for LTM9011 A and B in this application, several components on the Stratix IV GX FPGA development board come into play, including HSMC

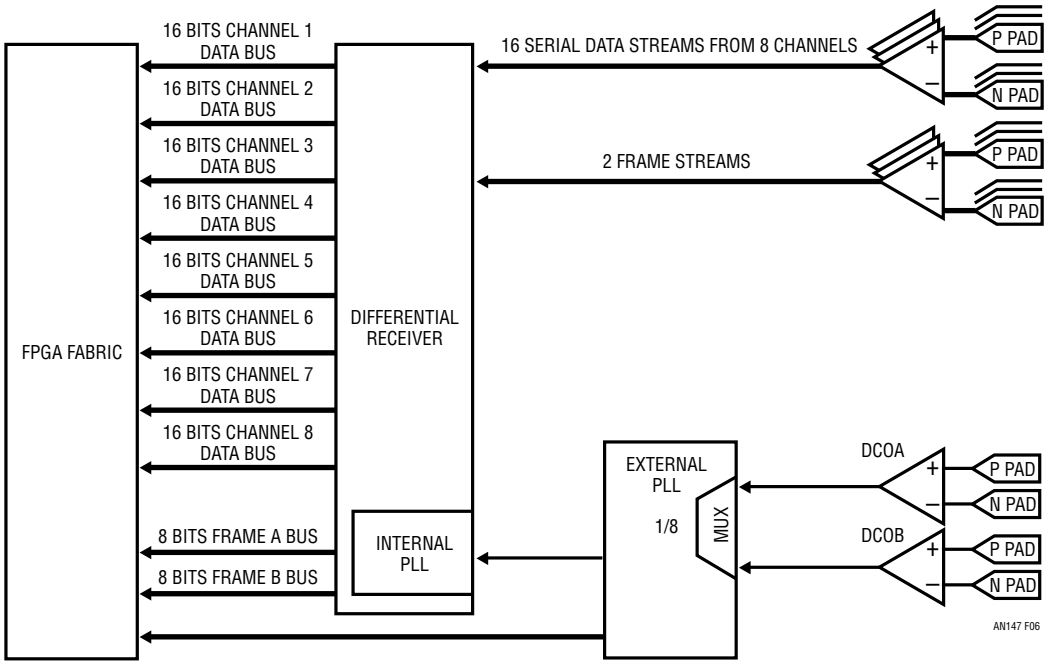

Figure 6. FPGA Design with External PLL Disabled

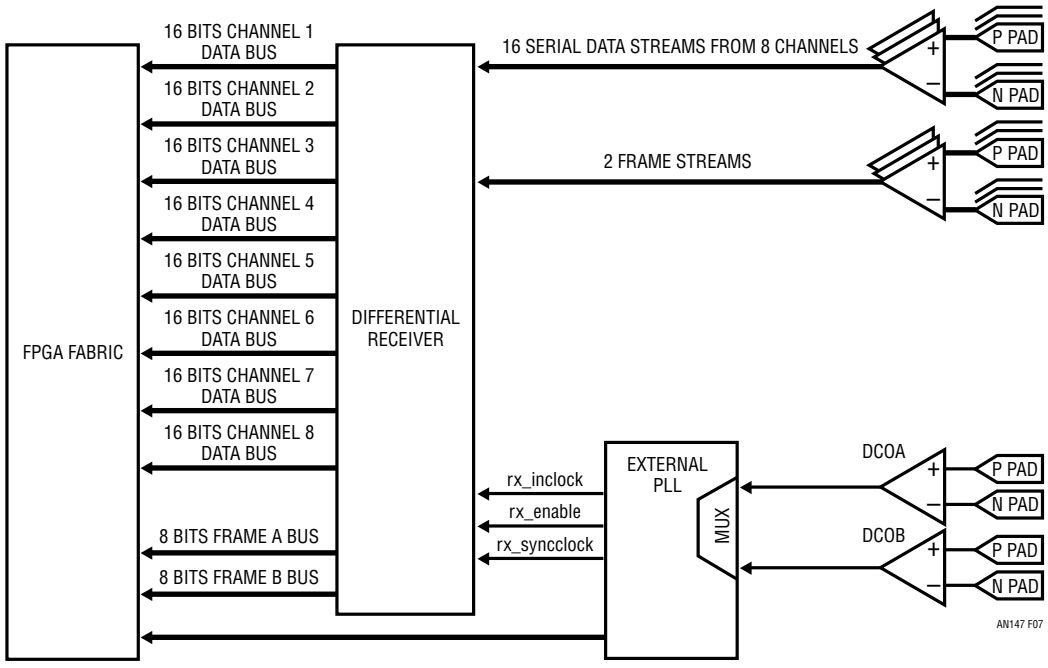

Figure 7. FPGA Design with External PLL Enabled

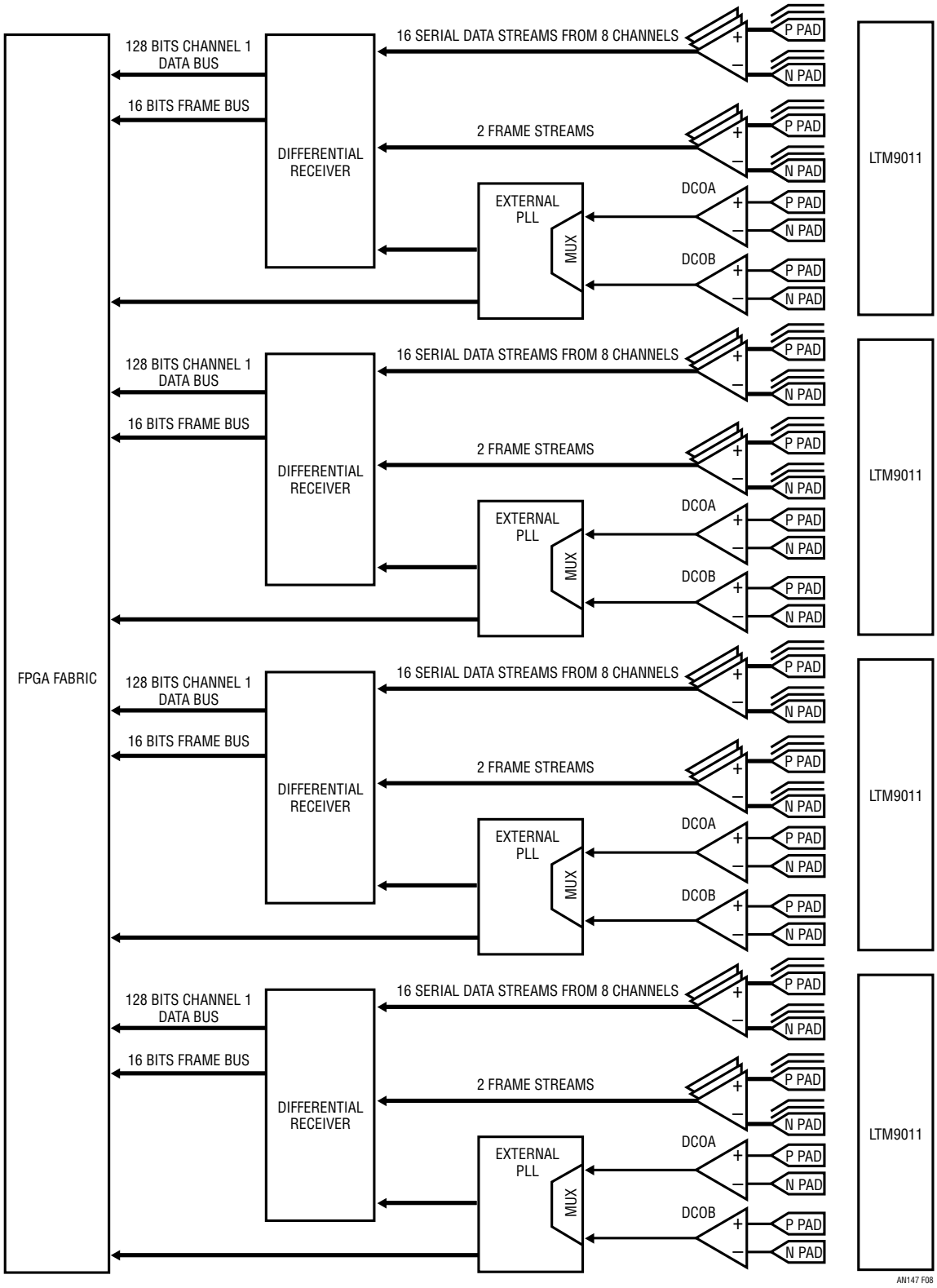

Figure 8. Multi-LTM9011 Solution A

connector J1, the left side true LVDS buffers and two left side PLLs. Likewise, LTM9011 C & D utilize HSMC connector J2, the right side true LVDS buffers and two right side PLLs. The fitter summary report is:

Figure 9 shows an alternative multiple-LTM9011 application, this one designed to maximize resource usage. Generating a super receiver that collects all data and frame streams from four LTM9011s driven by one PLL,

```
+-----------------------------------------------------------------------------+
; Fitter Summary;
+-----------------------------------+-----------------------------------------+
; Fitter Status                     ; Successful - Tue Sep 11 17:01:59 2012     ;
; Quartus II Version                ; 11.0 Build 157 04/27/2011 SJ Full Version ;
; Revision Name                     ; top_FPGA                                  ;
; Top-level Entity Name             ; top_FPGA                                  ;
; Family                            ; Stratix IV                                ;
; Device                            ; EP4SGX230KF40C2                           ;
; Timing Models                     ; Final                                     ;
; Logic utilization                 ; 3 %                                       ;
; Combinational ALUTs               ; 4,153 / 182,400 ( 2 % )                   ;
; Memory ALUTs                      ; 0 / 91,200 ( 0 % )                        ;
; Dedicated logic registers         ; 4,466 / 182,400 ( 2 % )                   ;
; Total registers                   ; 4466                                      ;
; Total pins                        ; 190 / 888 ( 21 % )                        ;
; Total virtual pins                ; 0                                         ;
; Total block memory bits           ; 8,388,864 / 14,625,792 ( 57 % )           ;
; DSP block 18-bit elements         ; 0 / 1,288 ( 0 % )                         ;
; Total GXB Receiver Channel PCS    ; 0 / 24 ( 0 % )                            ;
; Total GXB Receiver Channel PMA    ; 0 / 36 ( 0 % )                            ;
; Total GXB Transmitter Channel PCS ; 0 / 24 ( 0 % )                            ;
; Total GXB Transmitter Channel PMA ; 0 / 36 ( 0 % )                            ;
; Total PLLs                        ; 5 / 8 ( 63 % )                            ;
; Total DLLs                        ; 0 / 4 ( 0 % )                             ;
+-----------------------------------+-----------------------------------------+
```

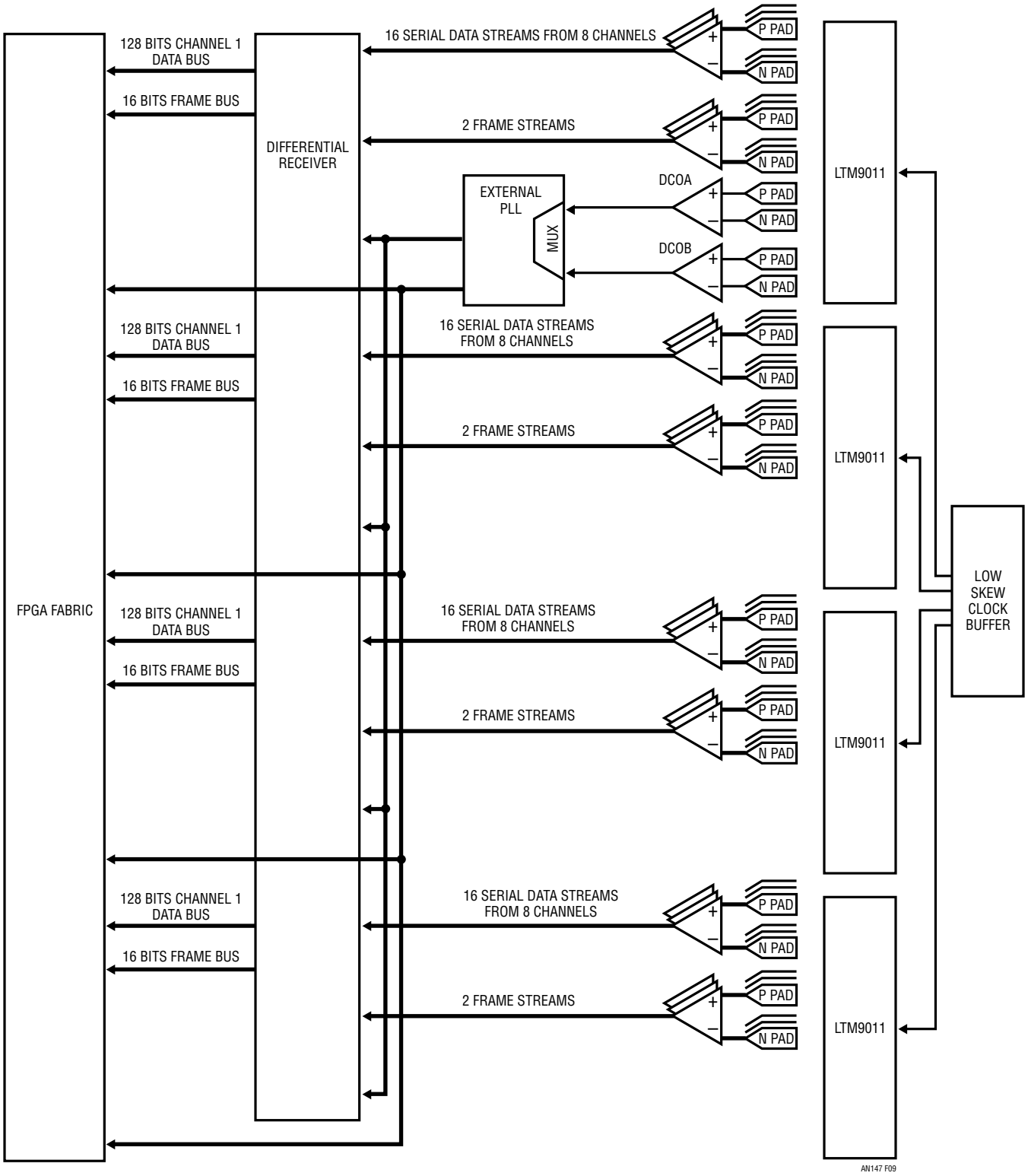

Figure 9. Multi-LTM9011 Solution B

instead of four, requires an ultralow skew clock buffer to distribute DCO to all LTM9011s to minimize clock skew. This solution may not work for EP4SGX230KF40C2 using the Stratix IV GX FPGA development board, because the resources of one side of the FPGA are not sufficient to support four LTM9011s and the SERDES circuitries of each side, which are only supported by the PLLs on the same side.

Single LTM9011 Design Details

Figure 10 shows a block diagram of the tested, single LTM9011 FPGA design. The parallel data from the deserializer are captured and fed into the FPGA internal block RAM (altmem_ram2). The deserialized FRAME bus is synchronized with the data bus, and functions as a reference pattern that is sent to bitslip_gen. This circuitry controls the data realignment circuitry of the LVDS receiver (altlvds_rx1) and inserts appropriate bits of latency in the serial bit stream to align to the word boundary.

The altmem_ram2 block is controlled by address and read/write signals generated by altbram_ctrl and altbram_addr. One 16-bit data output interface (clldata) is implemented for the user to directly collect the data of one of eight channels from the block RAM. A dedicated clock (cllclk) and control signal (cllctrl) are generated for the user to capture and qualify the data (Figure 11). Those signals are assigned to J1 of the FPGA board.

The Stratix IV GX FPGA development board provides many peripheral interfaces such as PCI and USB but it can be easier to build a configuration and data capturing interface to the host by using a special feature of the FPGA, the

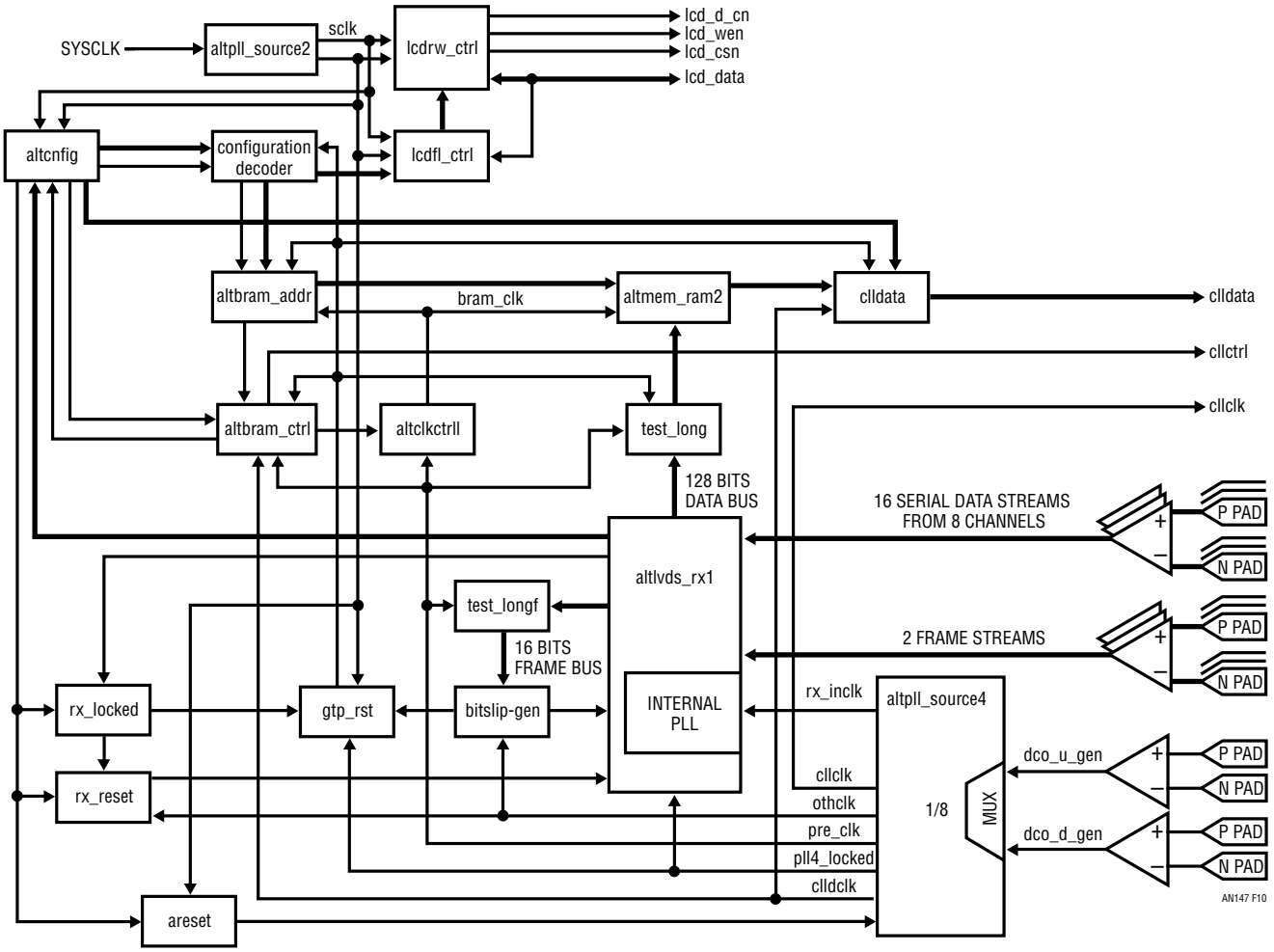

Figure 10. FPGA Design Block Diagram

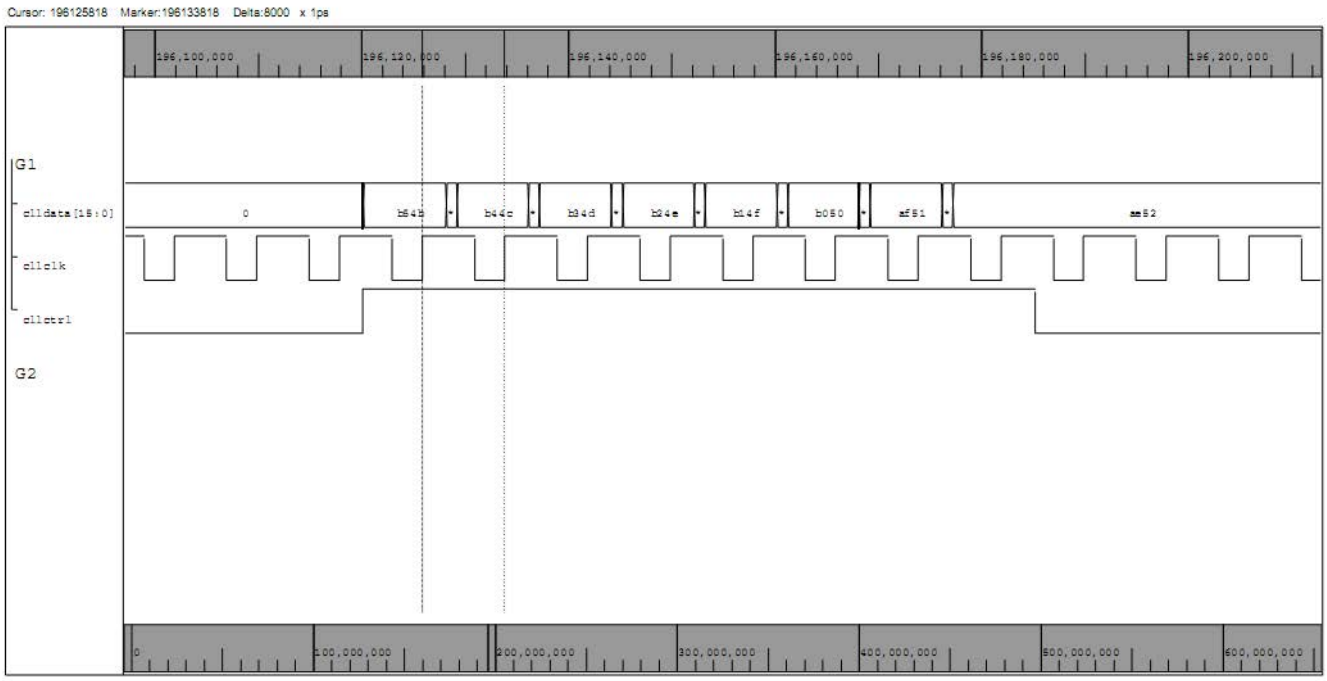

Figure 11. clldata Interface Timing Diagram

In-System Memory Content Editor, without any software or hardware effort. The In-System Memory Content Editor allows access to dense and complex FPGA designs. After programming devices, we have read and write access to the memories and constants through the JTAG interface. So we can not only capture data from block RAM (altmem_ram2) but we can dynamically change the configuration and monitor the FPGA running status from a circuit, altcnfig, which is implemented in 32 bytes of RAM and some small control logic circuitry. The capture buffer size, channel selection for data directly output to I/O (clldata), start and stop capturing, reset, etc., can be set up and controlled by altcnfig. The LVDS receiver, PLL, capture buffer status and flags are also monitored by altcnfig.

The clock, DCO, from LTM9011 is divided by eight by PLL altpll_source4 and fed into the internal PLL of the LVDS receiver. The altpll_source4 generates other clocks for the data capture system. Another clock domain is built by PLL altpll_source2, which references clock SYSCLK provided by the FPGA's on-board 50MHz oscillator.

Table 2. FPGA Clock Tree

CLOCK SOURCE	CLOCK NAME	LOADING	FREQUENCY RATE UP TO
altpll_source4	rx_inclk	altlvds_rx1	125MHz
	cllclk	output pin	125MHz
	othclk	bitslip_gen, rx_reset	125MHz
	pre_clk	test_longf, test_long, altclkctrl, altbram_ctrl	125MHz
	clldclk	Altclkctrl, clldata	125MHz
altpll_source2	sclk	lcdrw_ctrl, lcdfl_ ctrl, altcnfig	500KHz

The PLL altpll_source4 timing relationship is illustrated in Figure 12.

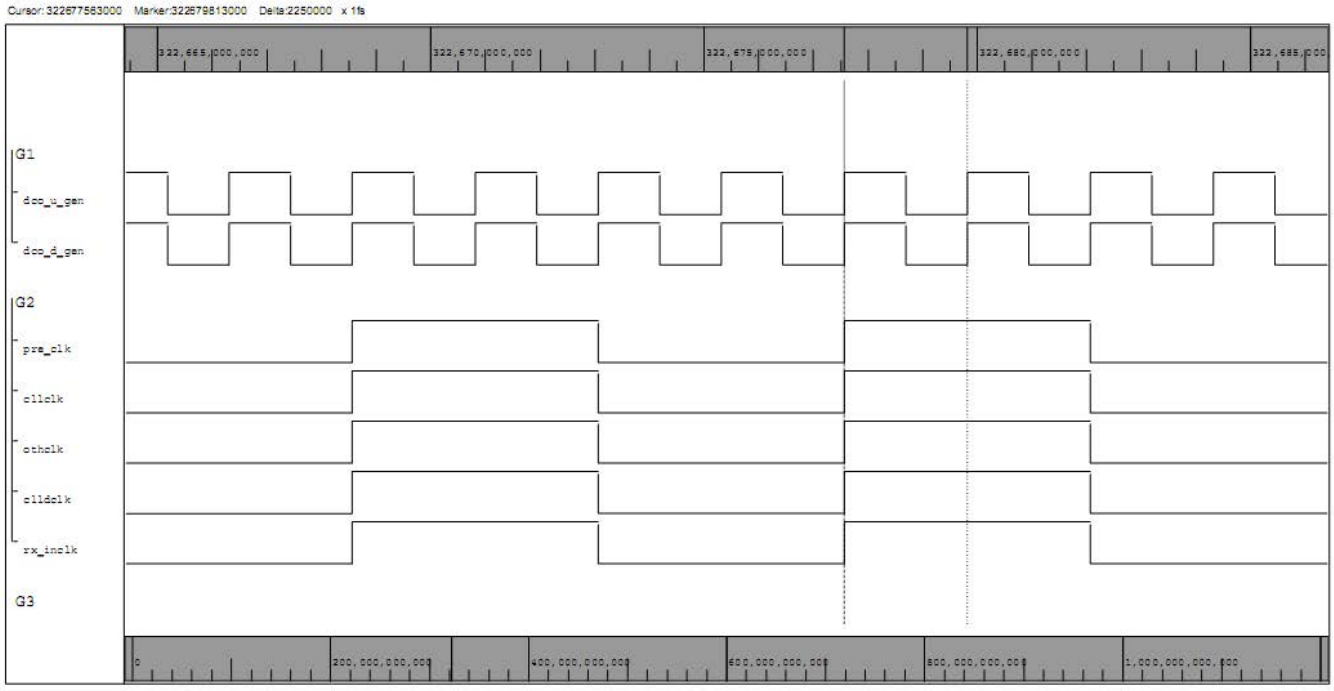

Figure 12. PLL altpll_source4 Timing Diagram

The clock rx_inclk is delivered to the differential receiver to generate a complex internal clock tree for the SERDES circuitry—we don't need to worry too much about that. The clock pre_clk goes through a clock buffer (altclkctrl1), which is controlled by circuit altbram_ctrl, to clock altmem_ram2, which is built by FPGA block RAM, and address generator altbram_addr. The clock othclk is created for other applications such as an LVDS receiver reset generator, bit-slip pulse generator, etc. The clock clldclk drives a 16-bit parallel data bus output and generates the signal cllctrl. The clock cllclk directly drives the output clock pin for user-capture of the 16-bit parallel data.

As mentioned above, we have a controller built by a small block BRAM accessible by the host from the JTAG interface using Altera tools. Here is the register definition:

Address Offset: 0x00

Table 3. DPA Status Register

BIT	7	6	5	4	3	2	1	0
Bit Name	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Read/Write	Read							
Initial Value	0x00							

- CHx: Channelx (0–7) serial line is locked by DPA. 1: locked 0: unlocked

Address Offset: 0x01

Table 4. Capture Configuration Register

BIT	7	6	5	4	3	2	1	0
Bit Name	MEMSIZE				CHSEL			RSV
Read/Write	Write							
Initial Value	0x70							

- RSV: Reserved
- CHSEL: Select Channel for data directly output to HSMC connector J1. Valid numbers 0–7
- MEMSIZE: Buffer size select for date capture space of each channel.

Table 5. Buffer Size Configuration

MEMSIZE	BUFFER SIZE
0	8 Samples
1	16 Samples
2	32 Samples
3	64 Samples
4	128 Samples
5	256 Samples
6	512 Samples
7	1K Samples
8	2K Samples
9	4K Samples
A	8K Samples
B	16K Samples

Address Offset: 0x02

Table 6. Capture Control Register

BIT	7	6	5	4	3	2	1	0
Bit Name	RSV							START
Read/Write	Write							
Initial Value	0x00							

- RSV: Reserved
- START: Start data capture. 1: Start. Need to reset to 0 after writing 1 to complete trigger

Address Offset: 0x03

Table 7. Collection Control Register

BIT	7	6	5	4	3	2	1	0
Bit Name	RSV							START
Read/Write	Write							
Initial Value	0x00							

- RSV: Reserved
- START: Start data collection from J1. 1: Start. Need to reset to 0 after writing 1 to complete trigger

Address Offset: 0x04

Table 8. Capture Status Register

BIT	7	6	5	4	3	2	1	0
Bit Name	FRB	FRA	CAPDONE	CLLDONE	RXLOCK	PLL2LOCK	PLL4LOCK	BSP
Read/Write	Read							
Initial Value	0x00							

- BSP: Bit-slip generator indicates that the data realignment circuitry has aligned to the word boundary successfully. 1: successful 0: Fail
- PLL4LOCK: PLL altpll_source4 is locked. 1: locked 0: unlocked
- PLL2LOCK: PLL altpll_source2 is locked. 1: locked 0: unlocked
- RXLOCK: The internal PLL of LVDS receiver is locked. 1: locked 0: unlocked
- CLLDONE: Data collection is done. 1: done 0: not yet
- CAPDONE: Data capture is done. 1: done 0: not yet
- FRA: Frame A serial line is locked by DPA. 1: locked 0: unlocked
- FRB: Frame B serial line is locked by DPA. 1: locked 0: unlocked

Address Offset: 0x1D

Table 9. Reset Control Register

BIT	7	6	5	4	3	2	1	0
Bit Name	RSV							RST
Read/Write	Write							
Initial Value	0x00							

- RSV: Reserved
- RST: Reset whole circuit except the LCD driver and system controller altcnfig. 1: Reset. Need to release to 0 after writing 1 to complete trigger

After place and routing, here is a simulation at 125MSPS for all channels. The output is from the deserializer and shown as a skew waveform. test_longx is from channelx.

The FPGA design implements a full function LCD driver for FPGA configuration and status display. It supports the Lumex LCD module SML-LX1206GC-TR attached to the Stratix IV GX FPGA development board.

The LCD driver circuits lcdrw_ctrl, lcdfl_ctrl are clocked by a second clock input SYSCLK from the FPGA's on-board 50MHz oscillator. Below are two rows of the LCD 32 characters display:

Table 10. LCD Display

CHARACTERS	DISPLAY	DESCRIPTION
XXX	RDY	FPGA Ready
	RST	FPGA Reset
Y	0 - 7	Channel Selected
ZZZZ	(Samples Counter)	See Table 5 Buffer Size Configuration

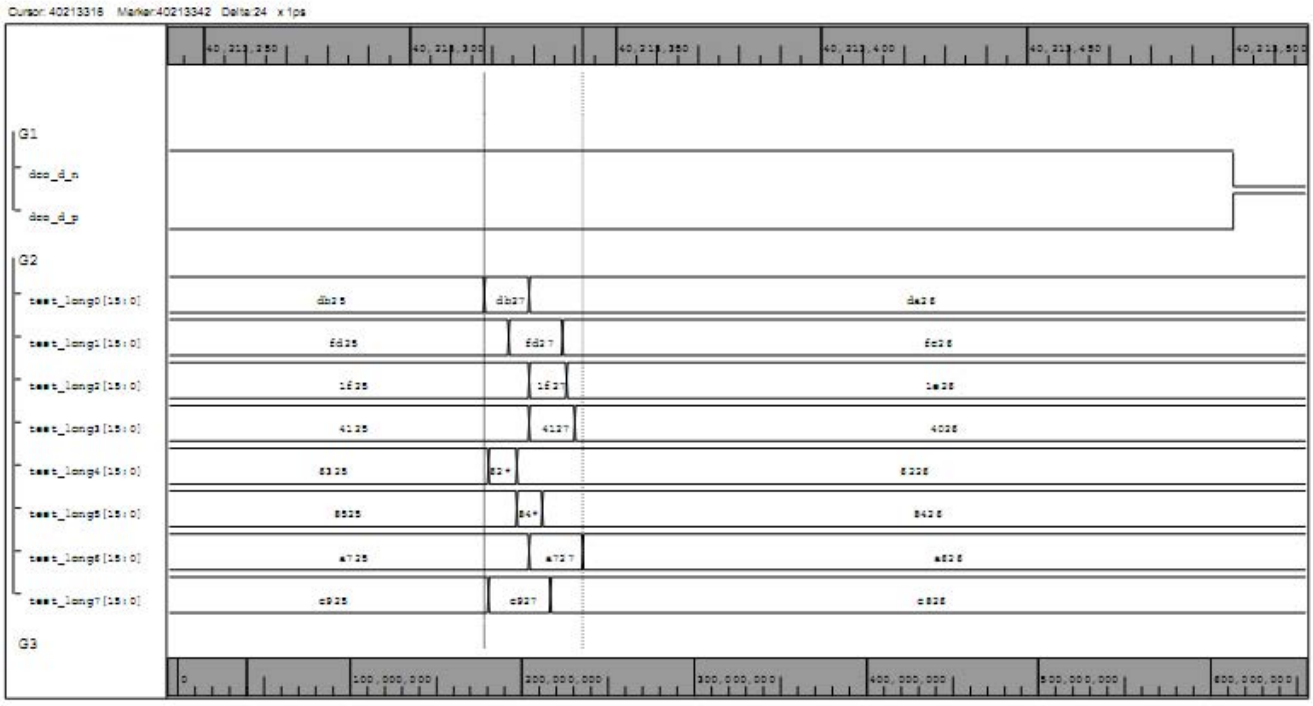

Figure 13. Post Place and Routing Simulation at 125Msps Channel Skew

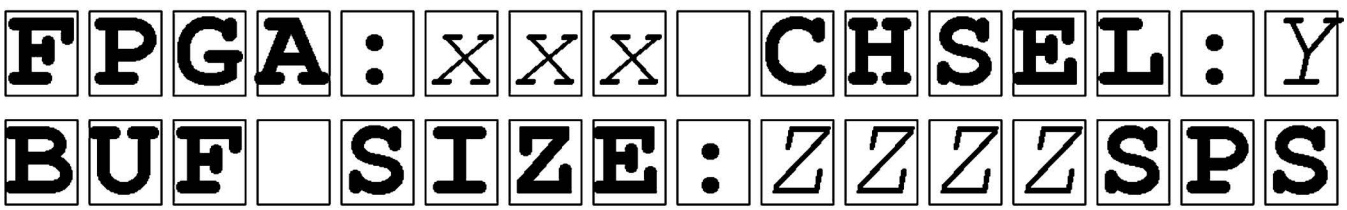

Figure 14. LCD Display

PCB Guidelines

Components should be placed as close as possible to each other on the PCB, aligned according to the pinout of the components. Components should be positioned to minimize the number of turns, corners, and vias. A straight, short connection improves all possible parameters of a PCB layout:

- Signal integrity
- Transmission line effects
- Capacitance and inductance
- Operating frequency

Transmission line effects matter when distances between components are lengthy. All transmission lines should be terminated properly to control reflections.

The key guidelines for PCB designers are:

- Spend sufficient time when placing the different circuit components for the layout.
- Keep trace lengths as short as possible.
- Spend more time on PCB stack-up design to get more strip-line channels for differential traces.
- Match the lengths of the differential traces, such as the 16 pairs of data stream OUT#A, OUT#B, 2 pairs of data clock DCOA, DCOB and 2 pairs of frame signal FRA, FRB ±5mils.
- Make turns with differential traces, take care to balance the number of left and right turns. When making a turn with a differential trace, the inner trace becomes shorter than the outer trace of the pair. When using more turns in one direction, one trace of the differential pair is longer than the other (without direct correction possibilities).
- Spread traces after routing over the available space of the PCB to minimize crosstalk.
- Do not route traces into 90° or 180° turns. Such turns increase the effective width of the trace, contributing to parasitic capacitance. At very fast edge rates, these discontinuities can cause significant signal integrity problems. Instead, use round, circular turns. If this is not possible, use 45° corners.
- Follow the signal return path guidelines.
- Use guard traces where needed.
- Remember the importance of ground planes.

Reference Design

Table 11. Reference Design Matrix

PARAMETER	DESCRIPTION
General	
Developer Name	Gary Yu
Target Devices	Stratix IV GX FPGA EP4SGX230KF40
Source Code Provided	Yes
Source Code Format	Verilog
Design Uses Code or IP from Existing Reference Design, Application Note, 3rd party, or Megawizard Software	Yes
Simulation	
Functional Simulation Performed	Yes
Timing Simulation Performed	Yes
Testbench Provided for Functional and Timing Simulations	Yes
Testbench Format	Verilog
Simulator Software and Version	NCVerilog (64bit) 08.20-s014
SPICE/IBIS Simulations	No
Implementation	
Synthesis Software Tools and Version	QUARTUS II v11.0
Implementation Software Tools and Version	QUARTUS II v11.0
Static Timing Analysis Performed	Yes
Hardware Verification	
Hardware Verified	Yes
Hardware Platform Used for Verification	DC1884A demo board and Stratix IV GX FPGA Development Board

An application on Microsoft Windows is presented to the user for:

- Configuring LTM9011 by SPI.
- Configuring FPGA by JTAG.
- Capturing the datain FPGA internal block RAM during run time by JTAG.
- Creating data file which can be read by PScope™.

The directories are set up as shown in Figure 15.

The whole design, simulation and implementation environment are presented on the Red Hat LINUX operating system. The directories are set up as shown in Figure 16.

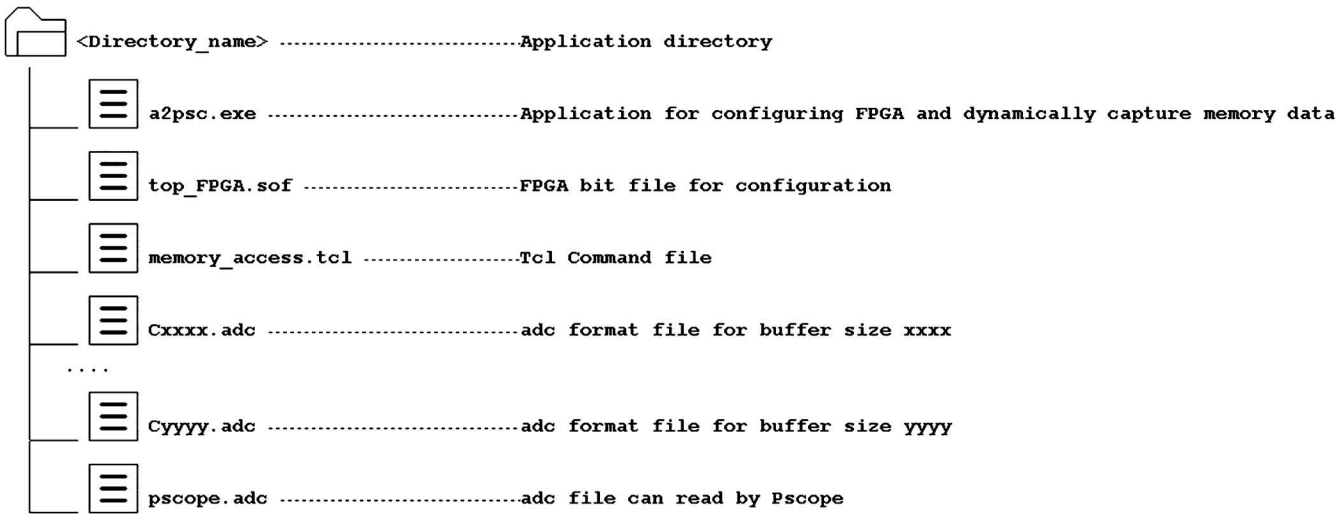

Figure 15. Application Directory Setup

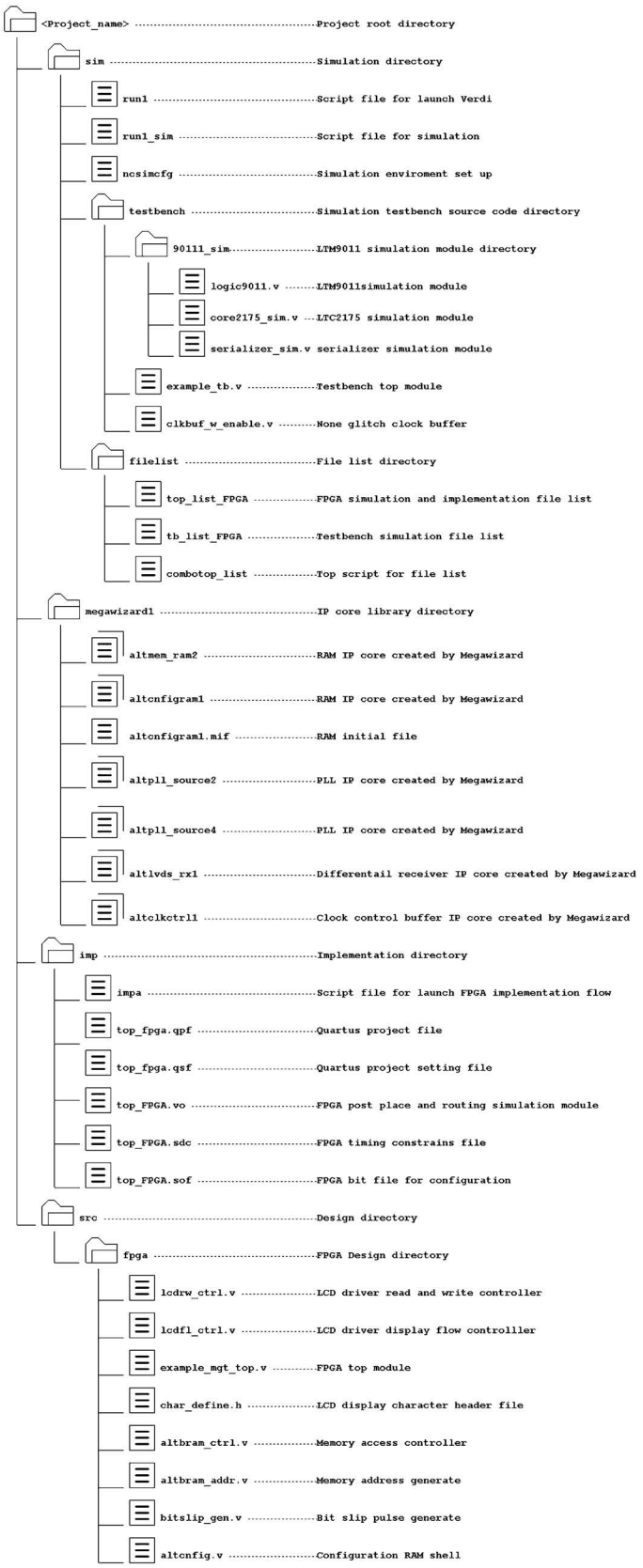

Figure 16. Design Directory Setup

Quick Start Guide

- Connect the LTM9011 demo board DC1884A to the FMC connector of the flexible cable SAMTEC SCF-156146-02-MA. Plug the HSMC connector on the other end to J2 of the Stratix IV GX FPGA development board.
- Connect the DC590B USB-to-SPI controller card to the DC1884A board by a 14-pin ribbon cable.
- Connect DC590B J3 and Stratix IV GX FPGA development board J7 to a host PC with USB cables.
- Connect the clock generator and the analog sources to the DC1884A board (J2, J4-J11). Coaxial cables are recommended.
- Set Jumper JP14 to serial configuration mode and ignore others.
- Power sequence:
  1. Turn on the 5V power supply for the DC1884A board.
  2. Turn on the Stratix IV GX FPGA development board (SW1) and DC590B power.
  3. Turn on the clock generator and the clock divider.
  4. Turn on the analog sources.
- Launch PScope in Windows on the PC.
- Open a DOS window and from the application directory launch a2psc.exe, which performs the following routines:
  1. Configures LTM9011 through the DC590B USB to SPI controller card.
  2. Configures the FPGA.
  3. Captures the data in the FPGA's internal block RAM during run time by JTAG.
  4. PScope then reads the data file created by a2psc and displays the waveform.

The following illustrates that the LTM9011 has been enabled and configured successfully:

1. The current value of the 5V power supply for DC1884A board is changed to 590mA.

The following illustrates that the FPGA has been configured successfully:

1. D26 on FPGA board is on. It illuminates when the MAX II CPLD EPM2210 system controller is actively configuring the FPGA. It is driven by the MAX II CPLD EPM2210 System controller wire-ORed with the Embedded Blaster CPLD.
2. D5 on the FPGA board is on. It illuminates when the FPGA is successfully configured. It is driven by the MAX II CPLD EPM2210 System Controller.
3. The LCD panel displays as in Figure 14. “XXX” should be RDY.

- Change the sample clock frequency generated by the clock generator if it is necessary.
- Configure the capture buffer size using a2psc.exe if desired.

Conclusion

The 1.6Gbps SERDES features of the Altera Stratix IV GX FPGA are an ideal match for the LTM9011 and other serial LVDS output analog to digital converters. The architecture of the ALTLVDS megafunction allows the implementation of ultra-high speed LVDS receivers under very simple timing constraints. The LVDS receivers can properly capture high speed serial data streams without input buffer skew adjustment since the DPA circuitry tracks any dynamic phase variations between the clock and data.

LINEAR TECHNOLOGY

NOW PART OF ANALOG DEVICES

LT 1017 REV A • PRINTED IN USA