



**ASTRO™** Digital SABER™

and

**ASTRO/R**

Portable Radios  
Detailed Service Manual

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68P81076C10-A

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## Related Publications

ASTRO Digital SABER (Model I) User's Guide .....	68P81072C75
ASTRO Digital SABER (Models II and III) User's Guide .....	68P81072C80
ASTRO Digital SABER Portable Radios Basic Service Manual .....	68P81076C05

# Foreword

# 1

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## Safety

### SAFETY AND GENERAL INFORMATION

#### IMPORTANT INFORMATION ON SAFE AND EFFICIENT OPERATION

#### READ THIS INFORMATION BEFORE USING YOUR MOTOROLA TWO-WAY RADIO

The information provided in this document supersedes the general safety information contained in user guides published prior to October 2000. For information regarding radio use in a hazardous atmosphere refer to the Factory Mutual (FM) manual supplement included with radio models that offer this capability and/or the intrinsic safety radio information section of this user manual.

#### Radio Frequency (RF) Operational Characteristics

To transmit (talk) you must push the Push-To-Talk button; to receive (listen) you must release the Push-To-Talk button. When the radio is transmitting, it generates radio frequency (RF) energy; when it is receiving, or when it is off, it does not generate RF energy.

#### Portable Radio Operation and EME Exposure

Your Motorola radio is designed to comply with the following national and international standards and guidelines regarding exposure of human beings to radio frequency electromagnetic energy (EME):

- United States Federal Communications Commission, Code of Federal Regulations; 47 CFR part 2 sub-part J
- American National Standards Institute (ANSI) / Institute of Electrical and Electronic Engineers (IEEE) C95. 1-1992
- Institute of Electrical and Electronic Engineers (IEEE) C95.1-1999 Edition
- National Council on Radiation Protection and Measurements (NCRP) of the United States, Report 86, 1986
- International Commission on Non-Ionizing Radiation Protection (ICNIRP) 1998
- Ministry of Health (Canada) Safety Code 6. Limits of Human

## Exposure to Radio Frequency Electromagnetic Fields in the Frequency Range from 3 kHz to 300 GHz, 1999

- Australian Communications Authority Radiocommunications (Electromagnetic Radiation - Human Exposure) Standard 1999 (applicable to wireless phones only)

**To assure optimal radio performance and make sure human exposure to radio frequency electromagnetic energy is within the guidelines set forth in the above standards, always adhere to the following procedures:**

### Two-way Radio Operation



When using your radio, **hold the radio in a vertical position with the microphone one to two inches (2.5 to 5 centimeters) away from the lips.**

### Body-worn Operation

To maintain compliance with FCC RF exposure guidelines, if you wear a radio on your body when transmitting, always place the radio in a Motorola approved clip, holder, holster, case, or body harness for this product. Use of non-Motorola-approved accessories may exceed FCC RF exposure guidelines. If you do not use a Motorola approved body-worn accessory and are not using the radio in the intended use positions along side of the head in the phone mode or in front of the face in the two-way radio mode, then ensure the antenna and radio is kept the following minimum distances from the body when transmitting:

- Phone or Two-way radio mode: one inch (2.5 centimeters)
- Data operation using any data feature with or without an accessory cable: one inch (2.5 centimeters)

### Antenna Care

**Use only the supplied or an approved replacement antenna.** Unauthorized antennas, modifications, or attachments could damage the radio and may violate FCC regulations.

**DO NOT hold the antenna when the radio is “IN USE”.** Holding the antenna affects call quality and may cause the radio to operate at a higher power level than needed.

### Approved Accessories

For a list of approved Motorola accessories look in the appendix or accessory section of your radio's User Guide.

## Electromagnetic Interference/Compatibility

NOTE: Nearly every electronic device is susceptible to electromagnetic interference (EMI) if inadequately shielded, designed or otherwise configured for electromagnetic compatibility.

### Facilities

To avoid electromagnetic interference and/or compatibility conflicts, turn off your radio in any facility where posted notices instruct you to do so. Hospitals or health care facilities may be using equipment that is sensitive to external RF energy.

### Aircraft

When instructed to do so, turn off your radio when on board an aircraft. Any use of a radio must be in accordance with applicable regulations per airline crew instructions.

### Medical Devices

- Pacemakers

The Health Industry Manufacturers Association recommends that a minimum separation of 6 inches (15 centimeters) be maintained between a handheld wireless radio and a pacemaker. These recommendations are consistent with those of the U.S. Food and Drug Administration.

Persons with pacemakers should:

- ALWAYS keep the radio more than 6 inches (15 centimeters) from their pacemaker when the radio is turned ON.
- not carry the radio in the breast pocket.
- use the ear opposite the pacemaker to minimize the potential for interference.
- turn the radio OFF immediately if you have any reason to suspect that interference is taking place.

- Hearing Aids

Some digital wireless radios may interfere with some hearing aids. In the event of such interference, you may want to consult your hearing aid manufacturer to discuss alternatives.

- Other Medical Devices

If you use any other personal medical device, consult the manufacturer of your device to determine if it is adequately shielded from RF energy. Your physician may be able to assist you in obtaining this information.



## SAFETY AND GENERAL

### Use While Driving

Check the laws and regulations on the use of radios in the area where you drive. Always obey them.

When using your radio while driving, please:

- Give full attention to driving and to the road.
- Use hands-free operation, if available.
- Pull off the road and park before making or answering a call if driving conditions so require.

## OPERATIONAL WARNINGS

### FOR VEHICLES WITH AN AIR BAG



**WARNING**

Do not place a portable radio in the area over an air bag or in the air bag deployment area. Air bags inflate with great force. If a portable radio is placed in the air bag deployment area and the air bag inflates, the radio may be propelled with great force and cause serious injury to occupants of the vehicle.

### POTENTIALLY EXPLOSIVE ATMOSPHERES



**WARNING**

Turn off your radio prior to entering any area with a potentially explosive atmosphere, unless it is a radio type especially qualified for use in such areas as "Intrinsically Safe" (for example, Factory Mutual, CSA, UL, or CENELEC). Do not remove, install, or charge batteries in such areas. Sparks in a potentially explosive atmosphere can cause an explosion or fire resulting in bodily injury or even death.

**NOTE:** The areas with potentially explosive atmospheres referred to above include fueling areas such as below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles, such as grain, dust or metal powders, and any other area where you would normally be advised to turn off your vehicle engine. Areas with potentially explosive atmospheres are often but not always posted.

### BLASTING CAPS AND AREAS



**WARNING**

To avoid possible interference with blasting operations, turn off your radio when you are near electrical blasting caps, in a blasting area, or in areas posted: "Turn off two-way radio." Obey all signs and instructions.

## OPERATIONAL CAUTIONS

### ANTENNAS



**Caution**

Do not use any portable radio that has a damaged antenna. If a damaged antenna comes into contact with your skin, a minor burn can result.

### BATTERIES



**Caution**

All batteries can cause property damage and/or bodily injury such as burns if a conductive material such as jewelry, keys, or beaded chains touch exposed terminals. The conductive material may complete an electrical circuit (short circuit) and become quite hot. Exercise care in handling any charged battery, particularly when placing it inside a pocket, purse, or other container with metal objects.

## INTRINSICALLY SAFE RADIO INFORMATION

### FMRC Approved Equipment

Anyone intending to use a radio in a location where hazardous concentrations of flammable material exist (hazardous atmosphere) is advised to become familiar with the subject of intrinsic safety and with the National Electric Code NFPA 70 (National Fire Protection Association) Article 500 (hazardous [classified] locations).

An Approval Guide, issued by Factory Mutual Research Corporation (FMRC), lists manufacturers and the products approved by FMRC for use in such locations. FMRC has also issued a voluntary approval standard for repair service ("Class Number 3605").

FMRC Approval labels are attached to the radio to identify the unit as being FM Approved for specified hazardous atmospheres. This label specifies the hazardous Class/Division/Group along with the part number of the battery that must be used. Depending on the design of the portable unit, this FM label can be found on the back or the bottom of the radio housing. The FM Approval mark is shown below:



## WARNINGS



### WARNING

- Do not operate radio communications equipment in a hazardous atmosphere unless it is a type especially qualified for such use (e.g., FMRC Approved). An explosion or fire may result.
- Do not operate an FMRC Approved Product in a hazardous atmosphere if it has been physically damaged (e.g., cracked housing). An explosion or fire may result.
- Do not replace or charge batteries in a hazardous atmosphere. Contact sparking may occur while installing or removing batteries and cause an explosion or fire.

## WARNINGS



### WARNING

- Do not replace or change accessories in a hazardous atmosphere. Contact sparking may occur while installing or removing accessories and cause an explosion or fire.
- Do not operate an FMRC Approved Product unit in a hazardous location with the accessory contacts exposed. Keep the connector cover in place when accessories are not used.
- Turn a radio off before removing or installing a battery or accessory.
- Do not disassemble an FMRC Approved Product unit in any way that exposes the internal electrical circuits of the unit.
- Radios must ship from the Motorola manufacturing facility with the hazardous atmosphere capability and FM Approval labeling. Radios will not be “upgraded” to this capability and labeled in the field.
- A modification changes the unit’s hardware from its original design configuration. Modifications can only be made by the original product manufacturer at one of its FMRC-audited manufacturing facilities.

## WARNINGS



**WARNING**

- Failure to use an FMRC Approved Product unit with an FMRC Approved battery or FMRC Approved accessories specifically approved for that product may result in the dangerously unsafe condition of an unapproved radio combination being used in a hazardous location.
- Unauthorized or incorrect modification of an FMRC Approved Product unit will negate the Approval rating of the product.

## Repair of FMRC Approved Products

**REPAIRS FOR MOTOROLA PRODUCTS WITH FMRC APPROVAL ARE THE RESPONSIBILITY OF THE USER.**

You should not repair or relabel any Motorola- manufactured communication equipment bearing the FMRC Approval label (“FMRC Approved Product”) unless you are familiar with the current FMRC Approval standard for repairs and service (“Class Number 3605”).

You may want to consider using a repair facility that operates under 3605 repair service approval.

## WARNINGS



**WARNING**

- Incorrect repair or relabeling of any FMRC Approved Product unit could adversely affect the Approval rating of the unit.
- Use of a radio that is not intrinsically safe in a hazardous atmosphere could result in serious injury or death.

FMRC’s Approval Standard Class Number 3605 is subject to change at any time without notice to you, so you may want to obtain a current copy of 3605 from FMRC. Per the December 1994 publication of 3605, some key definitions and service requirements are as follows:

### *Repair*

A repair constitutes something done internally to the unit that would bring it back to its original condition—Approved by FMRC. A repair should be done in an FMRC Approved facility.

Items not considered as repairs are those in which an action is performed on a unit which does not require the outer casing of the unit to be opened in a manner which exposes the internal electrical circuits of the unit. You do not have to be an FMRC Approved Repair Facility to perform these actions.

### *Relabeling*

The repair facility shall have a method by which the replacement of FMRC Approval labels are controlled to ensure that any relabeling is limited to units that were originally shipped from the Manufacturer with an FM Approval label in place. FMRC Approval labels shall not be stocked by the repair facility. An FMRC Approval label shall be ordered from the original manufacturer, as needed, to repair a specific unit. Replacement labels may be obtained and applied by the repair facility, provided there is satisfactory evidence that the unit being relabeled was originally an FMRC Approved unit. Verification may include, but is not limited to: a unit with a damaged Approval label, a unit with a defective housing displaying an Approval label, or a customer invoice indicating the serial number of the unit and purchase of an FMRC Approved model.

### *Do Not Substitute Options or Accessories*

The Motorola communications equipment certified by Factory Mutual is tested as a system and consists of the FM Approved portable, FM Approved battery, and FM Approved accessories or options, or both. This FM Approved portable and battery combination must be strictly observed. There must be no substitution of items, even if the substitute has been previously Approved with a different Motorola communications equipment unit. Approved configurations are listed in the FM Approval Guide published by FMRC, or in the product FM Supplement. This FM Supplement is shipped from the manufacturer with the FM Approved radio and battery combination. The Approval Guide, or the Approval Standard Class Number 3605 document for repairs and service, can be ordered directly from Factory Mutual Research Corporation located in Norwood, Massachusetts.

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## Manual Revisions

Changes which occur after this manual is printed are described in "FMRs." These FMRs provide complete information on changes including pertinent parts listing data.

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## Computer Software Copyrights

The Motorola products described in this manual may include copyrighted Motorola computer programs stored in semiconductor memories or other media. Laws in the United States and other countries preserve for Motorola certain exclusive rights for copyrighted computer programs, including the exclusive right to copy or reproduce in any form the copyrighted computer program. Accordingly, any copyrighted Motorola computer programs contained in the Motorola products described in this manual may not be copied or reproduced in any manner without the express written permission of Motorola. Furthermore, the purchase of Motorola products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Motorola, except for the normal non-exclusive royalty free license to use that arises by operation of law in the sale of a product.

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## Replacement Parts Ordering

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis. If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Crystal and channel element orders should specify the crystal or channel element type number, crystal and carrier frequency, and the model number in which the part is used.

## Parts Ordering

7:00 A. M. to 7:00 P. M. (Central Standard Time)  
Monday through Friday (Chicago, U. S. A.)  
Domestic (U. S. A.): 1-800-422-420, or 847-538-8023  
1-800-826-1913, or 410-712-6200 (Federal Government)  
TELEX: 280127  
FAX: 1-847-538-8198  
FAX: 1-410-712-4991 (Federal Government)  
Domestic (U. S. A.) after hours or weekends:  
1-800-925-4357  
International: 1-847-538-8023

## Motorola Parts

Accessories and Aftermarket Division  
(United States and Canada)  
Attention: Order Processing  
1313 E. Algonquin Road  
Schaumburg, IL 60196

Accessories and Aftermarket Division  
Attention: International Order Processing  
1313 E. Algonquin Road  
Schaumburg, IL 60196

## Parts Identification

1-847-538-0021 (Voice)  
1-847-538-8194 (FAX)

# Portable Radio Model Numbering System

Typical Model Number: **H 0 4 U C F 9 P W 7 A N S P 0 1**  
 Position: **1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16**

## Position 1 - Type of Unit

H = Hand-Held Portable

## Positions 2 & 3 - Model Series

04 = ASTRO

## Position 4 - Frequency Band

A = Less than 29.7MHz	P = 336 to 410MHz
B = 29.7 to 35.99MHz	Q = 403 to 437MHz
C = 36 to 41.99MHz	R = 438 to 482MHz
D = 42 to 50MHz	S = 470 to 520MHz
F = 66 to 80MHz	T = Product Specific
G = 74 to 90MHz	U = 806 to 870MHz
H = Product Specific	V = 825 to 870MHz
J = 136 to 162MHz	W = 896 to 941MHz
K = 146 to 178MHz	Y = 1.0 to 1.6GHz
L = 174 to 210MHz	Z = 1.5 to 2.0GHz
M = 190 to 235MHz	

*Values given represent range only; they are not absolute.*

## Position 5 - Power Level

A = 0 to 0.7 Watts  
 B = 0.7 to 0.9 Watts  
 C = 1.0 to 3.9 Watts  
 D = 4.0 to 5.0 Watts  
 E = 5.1 to 6.0 Watts  
 F = 6.1 to 10 Watts

## Position 6 - Physical Packages

A = RF Modem Operation  
 B = Receiver Only  
 C = Standard Control; No Display  
 D = Standard Control; With Display  
 E = Limited Keypad; No Display  
 F = Limited Keypad; With Display  
 G = Full Keypad; No Display  
 H = Full Keypad; With Display  
 J = Limited Controls; No Display  
 K = Limited Controls; Basic Display  
 L = Limited Controls; Limited Display  
 M = Rotary Controls; Standard Display  
 N = Enhanced Controls; Enhanced Display  
 P = Low Profile; No Display  
 Q = Low Profile; Basic Display  
 R = Low Profile; Basic Display, Full Keypad

## Position 7 - Channel Spacing

1 = 5kHz	5 = 15kHz
2 = 6.25kHz	6 = 20/25kHz
3 = 10kHz	7 = 30kHz
4 = 12.5kHz	9 = Variable/Programmable

## Positions 13 - 16

"SP" Model Suffix

## Position 12 - Unique Model Variations

C = Cenelec  
 N = Standard Package

## Position 11 - Version

Version Letter (Alpha) - Major Change

## Position 10 - Feature Level

1 = Basic	6 = Standard Plus
2 = Limited Package	7 = Expanded Package
3 = Limited Plus	8 = Expanded Plus
4 = Intermediate	9 = Full Feature/Programmable
5 = Standard Package	

## Position 9 - Primary System Type

A = Conventional  
 B = Privacy Plus®  
 C = Clear SMARTNET™  
 D = Advanced Conventional Stat-Alert™  
 E = Enhanced Privacy Plus®  
 F = Nauganet 888 Series  
 G = Japan Specialized Mobile Radio (JSMR)  
 H = Multi-Channel Access (MCA)  
 J = CoveragePLUS™  
 K = MPT1327\* - Public  
 L = MPT1327\* - Private  
 M = Radiocom  
 N = Tone Signalling  
 P = Binary Signalling  
 Q = Phonenet®  
 W = Programmable  
 X = Secure Conventional  
 Y = Secure SMARTNET™

\* MPT = Ministry of Posts and Telecommunications

## Position 8 - Primary Operation

A = Conventional/Simplex  
 B = Conventional/Duplex  
 C = Trunked Twin Type  
 D = Dual Mode Trunked  
 E = Dual Mode Trunked/Duplex  
 F = Trunked Type I  
 G = Trunked Type II  
 H = FDMA\* Digital Dual Mode  
 J = TDMA\*\* Digital Dual Mode  
 K = Single Sideband  
 L = Global Positioning Satellite Capable  
 M = Amplitude Companded Sideband (ACSB)  
 P = Programmable

\* FDMA = Frequency Division Multiple Access

\*\* TDMA = Time Division Multiple Access

# ASTRO Digital SABER Detailed Model Chart

Model Number											Description		
H04KDC9PW5AN											VHF 1-5 Watt ASTRO Digital SABER Model I		
H04KDF9PW7AN											VHF 1-5 Watt ASTRO Digital SABER Model II		
H04KDH9PW7AN											VHF 1-5 Watt ASTRO Digital SABER Model III		
H04RDC9PW5AN											UHF 1-4 Watt ASTRO Digital SABER Model I		
H04RDF9PW7AN											UHF 1-4 Watt ASTRO Digital SABER Model II		
H04RDH9PW7AN											UHF 1-4 Watt ASTRO Digital SABER Model III		
H04SDC9PW5AN											UHF 1-4 Watt ASTRO Digital SABER Model I		
H04SDF9PW7AN											UHF 1-4 Watt ASTRO Digital SABER Model II		
H04SDH9PW7AN											UHF 1-4 Watt ASTRO Digital SABER Model III		
H04UCC9PW5AN											800MHz 1-3 Watt ASTRO Digital SABER Model I		
H04UCF9PW7AN											800MHz 1-3 Watt ASTRO Digital SABER Model II		
H04UCH9PW7AN											800MHz 1-3 Watt ASTRO Digital SABER Model III		
											<b>Item Number</b>	<b>Description</b>	
		X			X			X		X	NHN6544_	Housing (with display and 3 x 6 keypad)	
	X			X			X			X	NHN6554_	Housing (with display and 3 x 2 keypad)	
X			X			X			X		NHN6555_	Housing (no display and no keypad)	
X	X	X									NLD8892_	VHF Transceiver Board (136-174MHz)	
			X	X	X						NLE4560_	UHF Transceiver Board (403-470MHz)	
						X	X	X			NLE4244_	UHF Transceiver Board (450-512MHz)	
									X	X	X	NUF6411_	800MHz Transceiver Board (806-870MHz)
X	X	X	X	X	X	X	X	X	X	X	X	NTN4595_	Nickel-Cadmium, Ultra-High Capacity (1800mAh), Large-Size Housing (Height 3.9" ) Battery
X	X	X	X	X	X	X	X	X	X	X	X	NTN7061_	Accessory Connector Cover
X	X	X	X	X	X	X	X	X	X	X	X	NTN7268_	Control Top Chassis
X	X	X	X	X	X	X	X	X	X	X	X	NTN7309_	Belt Clip
X			X			X			X			NTN7637_	Non-Display Front Shield
	X	X		X	X		X	X		X	X	NTN7638_	Display Front Shield
X	X	X	X	X	X	X	X	X	X	X	X	NTN7749_	VOCON Kit
X	X	X	X	X	X	X	X	X	X	X	X	0305150X01	VOCON Shield Screws (qty. 4)
X	X	X	X	X	X	X	X	X	X	X	X	1302646J01	Control Top Escutcheon
X	X	X	X	X	X	X	X	X	X	X	X	1302647J01	16-Position Select Knob Escutcheon
X	X	X	X	X	X	X	X	X	X	X	X	2605403X01	VOCON Board Back Shield
X	X	X	X	X	X	X	X	X	X	X	X	2605535W02	Center Transceiver Shield
X	X	X	X	X	X	X	X	X	X	X	X	2605844V01	VOCON Board Top Shield
X	X	X	X	X	X	X	X	X	X	X	X	2805462X01	20-Pin Mating Plug
X	X	X	X	X	X	X	X	X	X	X	X	3205082E48	On/Off/Volume Control Knob O-Ring Gasket
X	X	X	X	X	X	X	X	X	X	X	X	3205082E80	Control Top O-Ring Gasket
X	X	X	X	X	X	X	X	X	X	X	X	3205082E83	Programmable Button O-Ring Gasket
X	X	X	X	X	X	X	X	X	X	X	X	4502640J01	2-Position A/B Switch
X	X	X										8505518V01	VHF Antenna
			X	X	X	X	X	X				8505241U05	UHF Antenna
									X	X	X	8505241U03	800MHz Antenna

X = Indicates one of each is required.



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## Glossary

A/D	Analog to Digital converter; converts an instantaneous dc voltage level to a corresponding digital value.
ABACUS IC	Custom integrated circuit providing a digital receiver IF backend.
ADSIIC	ABACUS/DSP Support IC; custom integrated circuit providing peripheral functions for the DSP.
ALC	Automatic Level Control; a circuit in the transmit RF path that controls RF power amplifier output, provides leveling over frequency and voltage, and protects against high VSWR.
D/A	Digital to Analog converter; converts a digital value to a corresponding dc voltage value.
DTMF	Dual Tone Multi-Frequency
DPL	Digital Private-Line™
DSP	Digital Signal Processor; microcontroller specifically tailored for signal processing computations. In this case refers specifically to Motorola DSP56001.
Firmware	Software or a software/hardware combination of computer programs and data, with a fixed logic configuration stored in a read-only memory; information can not be altered or reprogrammed.
FGU	Frequency Generation Unit
FLASHport™	A Motorola term that describes the ability of a radio to change memory. Every FLASHport radio contains a FLASHport EEPROM memory chip that can be software written and rewritten to, again and again.
Host	Motorola HC11F1 microcontrol unit U204 (see MCU).
Host Port	Parallel memory mapped interface consisting of eight registers in the DSP56001.
IC	Integrated Circuit
IMBE	A sub-band, voice encoding algorithm used in ASTRO digital voice.
ISW	Inbound Signalling Word; data transmitted on the control channel from a subscriber unit to the central control unit.
LSH	Low Speed Handshake; 150 baud digital data sent to the radio during trunked operation while receiving audio.
MCU	MicroControl Unit
MDC	Motorola Digital Communications
OMPAC	Over-Molded Pad-Array Carrier; a Motorola custom IC package, distinguished by the presence of solder balls on the bottom pads.
Open Architecture	A controller configuration that utilizes a microprocessor with extended ROM, RAM, and EEPROM.
OSW	Outbound Signalling Word; data transmitted on the control channel from the central controller to the subscriber unit.
PC Board	Printed Circuit board
PL	Private-Line® tone squelch; a continuous sub-audible tone that is transmitted along with the carrier.
PLL	Phase-Locked Loop; a circuit in which an oscillator is kept in phase with a reference, usually after passing through a frequency divider.
PTT	Push-To-Talk; the switch located on the left side of the radio which, when pressed, causes the radio to transmit.
Registers	Short-term data-storage circuits within the microcontrol unit or programmable logic IC.

Repeater	Remote transmit/receive facility that re-transmits received signals in order to improve communications coverage.
RESET	Reset line; an input to the microcontroller that restarts execution.
RF PA	Radio Frequency Power Amplifier
RSS	Radio Service Software
RPT/TA	RePeaTer/Talk-Around
RX DATA	Recovered digital data line.
Signal Qualifier Mode	An operating mode whereby the radio is muted but still continues to analyze receive data to determine RX signal type.
SCI IN	Serial Communication Interface INput line
SLIC	Support-Logic IC; a custom gate array used to provide I/O and memory expansion for the microcontroller.
Softpot	Software potentiometer; a computer-adjustable electronic attenuator.
Software	Computer programs, procedures, rules, documentation, and data pertaining to the operation of a system.
SPI	Serial Peripheral Interface; how the microcontroller communicates to modules and ICs through the CLOCK and DATA lines.
Squelch	Muting of audio circuits when received signal levels fall below a pre-determined value.
SRAM	Static-RAM chip used for volatile, program/data memory.
SSI	Synchronous Serial Interface on the DSP56001 consisting of six signals and used for an RX and TX modulated data interface to the ADSIC.
Standby Mode	An operating mode whereby the radio is muted but still continues to monitor data.
System Central Controllers	Main control unit of the trunked dispatch system; handles ISW and OSW messages to and from subscriber units (see ISW and OSW).
System Select	The act of selecting the desired operating system with the system-select switch (also, the name given to this switch).
TOT	Time-Out Timer; a timer that limits the length of a transmission.
TSOP	Thin Small-Outline Package
UART	Universal Asynchronous Receiver Transmitter.
$\mu$ C	Microcontrol unit (see MCU).
VCO	Voltage-Controlled Oscillator; an oscillator whereby the frequency of oscillation can be varied by changing a control voltage.
VCOB IC	Voltage-Controlled Oscillator Buffer IC
Vocoder	VOIce enCODER; the DSP-based system for digitally processing the analog signals, includes the capabilities of performing voice compression algorithms or voice encoding.
VOCON	VOcoder/CONtroller board
VSELP	Vector Sum Excited Linear Predictive coding; a voice encoding technique used in ASTRO digital voice.
VSWR	Voltage Standing Wave Ratio



# Introduction

# 2

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## General

This manual includes all the information necessary to maintain peak product performance and maximum working-time. This detailed-level of service (component-level) is typical of some service centers, self-maintained customers, and distributors.

This manual is to be used in conjunction with the ASTRO Digital SABER Portable Radios Basic Service Manual (Motorola part number 68P81076C05), which helps troubleshooting a problem to a particular board. Conduct the basic performance checks first. This will verify the actual need for analyzing the radio and help pinpoint the functional problem area. In addition, the technician will become familiar with the radio test mode of operation, which is a helpful tool. If any basic receive or transmitter parameters fail, then the radio should be aligned per the radio alignment procedure.

Included in other areas of this manual are functional block diagrams, detailed theory of operation, troubleshooting charts and waveforms, schematics, and parts list. The technician should be very familiar with these sections to aid in deducing the problem circuit. Also included are component location diagrams to aid in locating individual circuit components and some IC diagram, which point out some convenient probe points.

The theory of operation sections of this manual contain detailed descriptions of operations of many circuits. Once the area of the problem is located, it would be strongly advisable to review the operation of the circuit pertaining to the troubleshooting flow chart.

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## Notations Used in This Manual

Throughout the text in this publication, you will notice the use of warnings, cautions, and notes. These notations are used to emphasize that safety hazards exist, and care must be taken and observed.

**NOTE:** An operational procedure, practice, or condition, etc., which is essential to emphasize.



**Caution**

**CAUTION:** Indicates a potentially hazardous situation which, if not avoided, may result in equipment damage. To properly word a caution, first identify the gravity of the risk, then describe the nature of the risk, then tell the user how to avoid the risk, and finally communicate this risk clearly to the person exposed to the risk.



**WARNING**

**WARNING:** Indicates a potentially hazardous situation which, if not avoided, could result in death or injury. To properly word a caution, first identify the gravity of the risk, then describe the nature of the risk, then tell the user how to avoid the risk, and finally communicate this risk clearly to the person exposed to the risk.



**DANGER:** Indicates an imminently hazardous situation which, if not avoided, will result in death or injury. To properly word a caution, first identify the gravity of the risk, then describe the nature of the risk, then tell the user how to avoid the risk, and finally communicate this risk clearly to the person exposed to the risk.

You will also find in this publication the use of the asterisk symbol (\*) to indicate a negative or NOT logic true signal.

# General Overview of an ASTRO Digital SABER Radio

## 3

The ASTRO Digital SABER radio is a dual mode (trunked/conventional), microcontroller-based transceiver incorporating a Digital Signal Processor (DSP). The microcontroller handles the general radio control, monitors status, and processes commands input from the keypad or other user controls. The DSP processes the typical analog signals and generates the standard signaling digitally to provide compatibility with existing analog systems. In addition it provides for digital modulation techniques utilizing voice encoding techniques with error correction schemes to provide the user with enhanced range and audio quality all in a reduced bandwidth channel requirement. It allows embedded signaling which can mix system information and data with digital voice to add the capability of supporting a multitude of system features.

The ASTRO Digital SABER radio is available in three models, which are available in the following bands; VHF (136-174MHz), UHF (403-470MHz or 450-512MHz), and 800MHz (806-870MHz).

The ASTRO Digital SABER radio consists of:

- Vocoder/Controller (VOCON) Board
- Band-Dependent Transceiver Board
- Display/Keypad Assembly
- In secure models, a hardware, encryption module is also included.

It is advantageous to think of the vocoder/controller (VOCON) board as two separate functional units; a vocoder and a controller. The vocoder section consists of a Digital Signal Processor (DSP), Static-RAM (SRAM), FLASH program memory, audio power amplifier (audio PA), and a custom ABACUS/DSP support integrated circuit (ADSIC). This section handles all the analog and signaling functions previously accomplished with analog integrated circuits (ICs) by processing the signals digitally. In addition, it provides advanced digital signal processing functions which include digital modulation and voice encoding techniques while still maintaining compatibility with today's analog radio systems. The controller section consists of a microcontroller with FLASH program memory, EEPROM, SRAM, and a custom IC; the SLIC. This section handles general radio control and ergonomics through the various user buttons, and rotary knobs.

The transceiver is frequency dependent, and one transceiver exists for each of the bands; VHF, UHF (range 1 and 2), and 800MHz. The distinction with these transceivers is the incorporation of the ABACUS IC. The ABACUS is a digital IF/Discriminator which provides a true digital interface to the digital circuitry of the vocoder.

The display module is a two-line, liquid crystal display with associated circuitry. The display module is an integral part of the front cover keypad. This module utilizes chip-on-board technology and is not considered field repairable.

The available encryption module connects directly to the VOCON board and interfaces directly to the vocoder digital circuitry. It contains an independent microcontroller, and two custom ICs to perform digital, numerical, encryption algorithms.

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## Analog Mode of Operation

When the radio is *receiving*, the signal comes from the antenna/ antenna-switch connector to the transceiver board, passes through the RX/TX switch and the receiver front end. The signal is then filtered, amplified, and mixed with the first local-oscillator signal generated by the voltage-controlled oscillator (VCO). The resulting intermediate frequency (IF) signal is fed to the IF circuitry, where it is again filtered and amplified. This amplified signal is passed to the digital back-end IC, where it is mixed with the second local oscillator to create the second IF at 450kHz. It is then converted to a digital bit stream and mixed a third time to produce a baseband signal. This signal is passed to the VOCON board through a current-driven differential output. On the VOCON board, the ADSIC (ABACUS DSP Support IC) digitally filters and discriminates the signal, and passes it to the digital-signal processor (DSP). The DSP decodes the information in the signal and identifies the appropriate destination for it. For a voice signal, the DSP will route the digital voice data to the ADSIC for conversion to an analog signal. The ADSIC will then present the signal to the audio power amplifier, which drives the speaker. For signalling information, the DSP will decode the message and pass it to the microcontrol unit.

When the radio is *transmitting*, microphone audio is passed from the audio power amplifier (PA) to the ADSIC, where the signal is digitized. The ADSIC passes digital data to the DSP, where pre-emphasis and low-pass (splatter) filtering are done. The DSP returns this signal to the ADSIC, where it is reconverted into an analog signal and scaled for application to the voltage-controlled oscillator as a modulation signal. Transmitted signalling information is accepted by the DSP from the microcontrol unit, coded appropriately, and passed to the ADSIC, which handles it the same as a voice signal. Analog modulation information is passed to the synthesizer along the modulation line. A modulated carrier is provided to the RF PA, which transmits the signal under dynamic power control.

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## ASTRO Mode (Digital Mode) of Operation

In the ASTRO mode (digital mode) of operation, the transmitted or received signal is limited to a discrete set of four deviation levels. The receiver handles an ASTRO-mode signal identically to an analog-mode signal up to the point where the DSP decodes the received data. In the ASTRO receive mode, the DSP uses a specifically defined algorithm to recover information. In the ASTRO transmit mode, microphone audio is processed identically to an analog mode with the exception of the algorithm the DSP uses to encode the information. This algorithm will result in deviation levels that are limited to four discrete levels.

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## Transceiver Board Overview

The receiver front end consists of a preselector, an RF amplifier, a second preselector, and a mixer. Both preselectors in the VHF and UHF radios are varactor-tuned, two-pole filters controlled by the microcontrol unit through the digital/analog (D/A) IC. On the 800MHz receiver front end, these filters are fixed-tuned. The RF amplifier is a dual-gate, gallium-arsenide based IC. The mixer is a double-balanced, active mixer coupled by transformers. Injection is provided by the VCO through an injection filter. See Table 14 for local oscillator (LO) and first IF information.

The frequency generation function is performed by three ICs and associated circuitry. The reference oscillator provides a frequency standard to the synthesizer/prescaler IC, which controls the VCO IC. The VCO IC actually generates the first LO and transmit-injection signals and buffers them to the required power level. The synthesizer/prescaler circuit module incorporates frequency-division and comparison circuitry to keep the VCO signals stable. The synthesizer/prescaler IC is controlled by the microcontrol unit through a serial bus. Most of the synthesizer circuitry is enclosed in rigid metal cans on the transceiver board to reduce microphonic effects.

The receiver back end consists of a two-pole crystal filter, an IF amplifier, a second two-pole crystal filter, and the digital back-end IC (ABACUS). The two-pole filters are wide enough to accommodate 5kHz modulation. Final IF filtering is done digitally in the ADSIC.

The digital back-end IC (ABACUS) consists of an amplifier, the second mixer, an IF analog-to-digital converter, a baseband down-converter, and a 2.4MHz synthesis circuit to provide a clock to the ADSIC on the VOCON board. The second LO is generated by discrete components external to the IC. The output of the ABACUS IC is a digital bit stream that is current driven on a differential pair for a reduction in noise generation.

The transmitter consists of an RF PA IC that gets an injection signal from the VCO. Transmit power is controlled by two custom ICs that monitor the output of a directional coupler and adjust PA control voltages correspondingly. The signal passes through a RX/TX switch that uses PIN diodes to automatically provide an appropriate interface to transmit or receive signals. Antenna selection is done mechanically in the control top.

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## VOCON Board Overview

The VOCON board contains the radio's microcontrol unit with its memory and support circuits, voltage regulators, audio, DSP, ADSIC, and power control circuits. Connected to the VOCON board are the display board, transceiver board, and control top.

The microcontrol unit (MCU) controls receive/transmit frequencies, power levels, display, and other radio functions, using either direct logic control or serial communications paths to the devices. The microcontrol unit executes a stored program located in the FLASH ROM. Data is transferred to and from memory by the microcontrol unit data bus. The memory location from which data is read, or to which data is written, is selected by the address lines.



The SLIC acts as an extension of the microcontrol unit by providing logic functions such as lower address latch, reset, memory address decoding, and additional control lines for the radio. The microcontrol unit controls the crystal-pull circuit to adjust the crystal oscillator's frequency on the microcontrol unit, so that the E-clock's harmonics do not cause interference with the radio's receive channel.

Switched +5V is used for all circuits on the VOCON board except the audio PA, which is sourced from 7.5V. The regulator automatically provides 5V when the radio is turned on. The regulator's power-down mode is controlled by the microcontrol unit, which senses the position of the on/off/volume control knob.

The DSP performs all signalling and voice encoding and decoding as well as audio filtering and volume control. This includes Private-Line®/Digital Private Line™ (PL/DPL) encode and alert-tone generation. The IC transmits pre-emphasis on analog signals and applies a low-pass (splatter) filter to all transmitted signals. It is programmed using parallel programming from the microcontrol unit and the ADSIC.

The ADSIC performs analog-to-digital and digital-to-analog conversions on audio signals. It contains attenuators for volume, squelch, deviation, and compensation, and it executes receiver filtering and discrimination. The IC requires a 2.4MHz clock to function (generated by the ABACUS IC) and is programmed by the microcontrol unit SPI bus.

# Radio Power

# 4

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## Introduction

This section of the manual provides a detailed circuit description of the power distribution for an ASTRO Digital SABER radio.

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## General

In the ASTRO radio, power is distributed to three boards:

- transceiver
- VOCON
- display

In the case of a secure model radio, the encryption module is supplied also.

Power for the radio is provided through a battery supplying a nominal 7.5Vdc directly to the transceiver. The battery is available in the following forms:

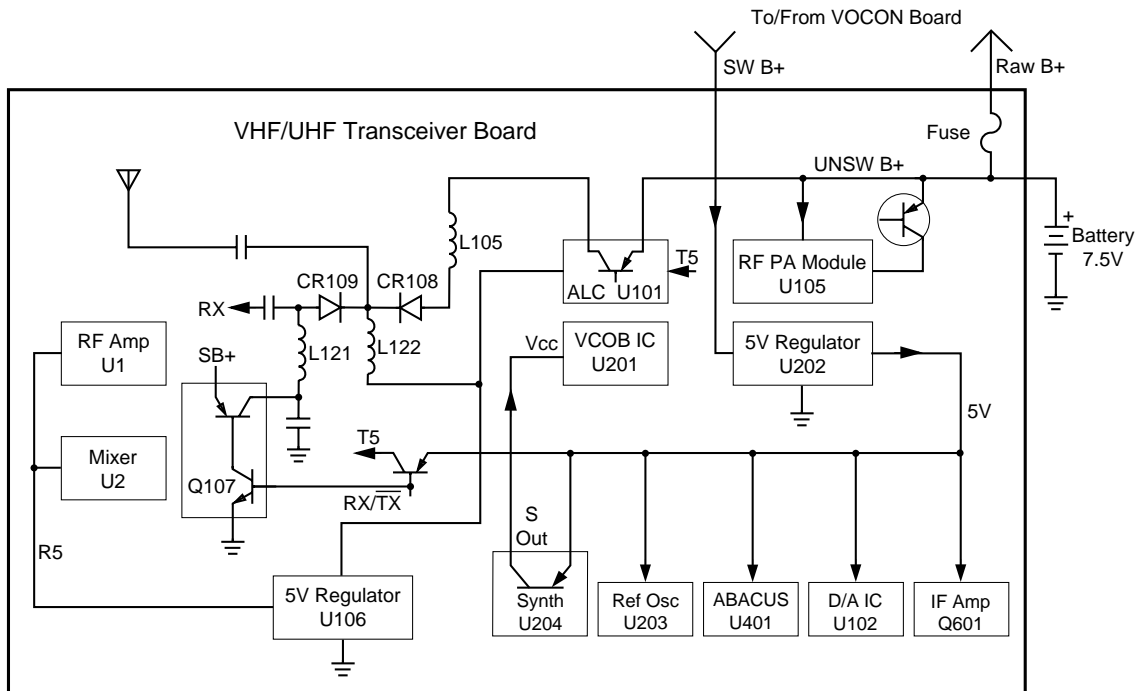
- Nickel-Cadmium, High-Capacity (1100mAh), Medium-Size Housing
- Nickel-Cadmium, High-Capacity (1100mAh), Medium-Size Housing (FM Approved, Submersible)
- Nickel-Cadmium, Ultra-High Capacity (1800mAh), Large-Size Housing
- Nickel-Cadmium, Ultra-High Capacity (1800mAh), Large-Size Housing (FM Approved)
- Nickel-Cadmium, Ultra-High Capacity (1800mAh), Large-Size Housing (FM Approved, Submersible)
- Nickel-Metal-Hydride, Medium-Capacity (950mAh), Small-Size Housing
- Nickel-Metal-Hydride, Ultra-High Capacity (1650mAh), Medium-Size Housing (FM Approved, Submersible)

B+ from the battery is electrically switched to most of the radio, rather than routed through the on/off/volume control knob, S901/R901. The electrical switching of B+ supports a “keep-alive” mode. Under software control, even when the on/off/volume control knob has been turned to the “off” position, power remains on until the MCU completes its power-down, at which time the radio is physically powered-down.

## B+ Routing for VHF/UHF Transceiver Boards

Refer to *Figure 1* and your specific schematic diagram.

Raw B+ (7.5V) from the battery (Batt B+) enters the radio on the transceiver board through a 3-contact spring pin arrangement (J3) as B+, where it is routed through two ferrite beads on the VHF (E1, E101) and three ferrite beads on the UHF (E1, E101, E106) to the RF power amplifier module (U105) and ALC IC (U101, pin 13). Battery B+ is fused, and then routed through the connector J1, pins 19 and 20 to the VOCON board (J401, pins 19 and 20). The B+ supply is routed through the VOCON board to the on/off/volume control knob (S901/R901) on the control top/PTT flex at jack J901, pin 1. With the mechanical on/off switch (S901) placed in the “on” position, switched B+ (B+ SENSE) is routed from the control top flex at connector plug P901, pin 10 and applied to the VOCON board at connector jack J901, pin 10. This signal is also fed to a resistive divider R222, R223 on the VOCON board so that the microcontrol unit (U204) can monitor the battery voltage.



MAEPF-24700-O

*Figure 1 . B+ Routing for VHF/UHF Transceiver Boards*

The switched B+ voltage supplies power to circuits on the transceiver board. The 5-volt regulator (U202), is applied this voltage through decoupling component C125 to produce a stable 5.0 volt output. Raw B+ (7.5V), which is connected to the ALC IC (U101), is switched through the output (CATH1) to another 5-volt regulator (U106).

Regulator U202 supplies those circuits which need to remain on at all times, such as the reference oscillator (U203), fractional-N-synthesizer (U204), D/A IC (U102), and the ABACUS IC (U401). The D/A IC controls dc switching of the transceiver board. The SC1 signal at U102 pin 12 controls transistors Q107, Q111, and the transmit 5 volts (T5).



receive 5 volts (R5). During the receive mode, switch Q503 supplies regulated 5volts (R5) to the receiver front end.

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## B+ Routing for VOCON Boards and Display Modules

Refer to *Figure 3* and your specific schematic diagram.

Power for the radio is derived from a 7.5 volt battery, which is applied to the transceiver board through J3. This Raw B+, or unswitched B+ (UNSW B+), is routed to J1 on the transceiver board and then on to J401 on the VOCON board. Here the UNSW B+ is forwarded to the radio's control top on/off/volume knob through J901 and a flex circuit. The on/off/volume knob controls B+\_SENSE to Q206, which in turn controls Q207. Transistor Q207 is a solid-state power switch, which provides SW B+ to the VOCON board's analog and transceiver 5V regulators, the audio PA, the display module, and back to the transceiver board. In addition, UNSW B+ is routed to the main digital 5V regulator (U409); B+ SENSE provides for enabling or disabling this regulator.

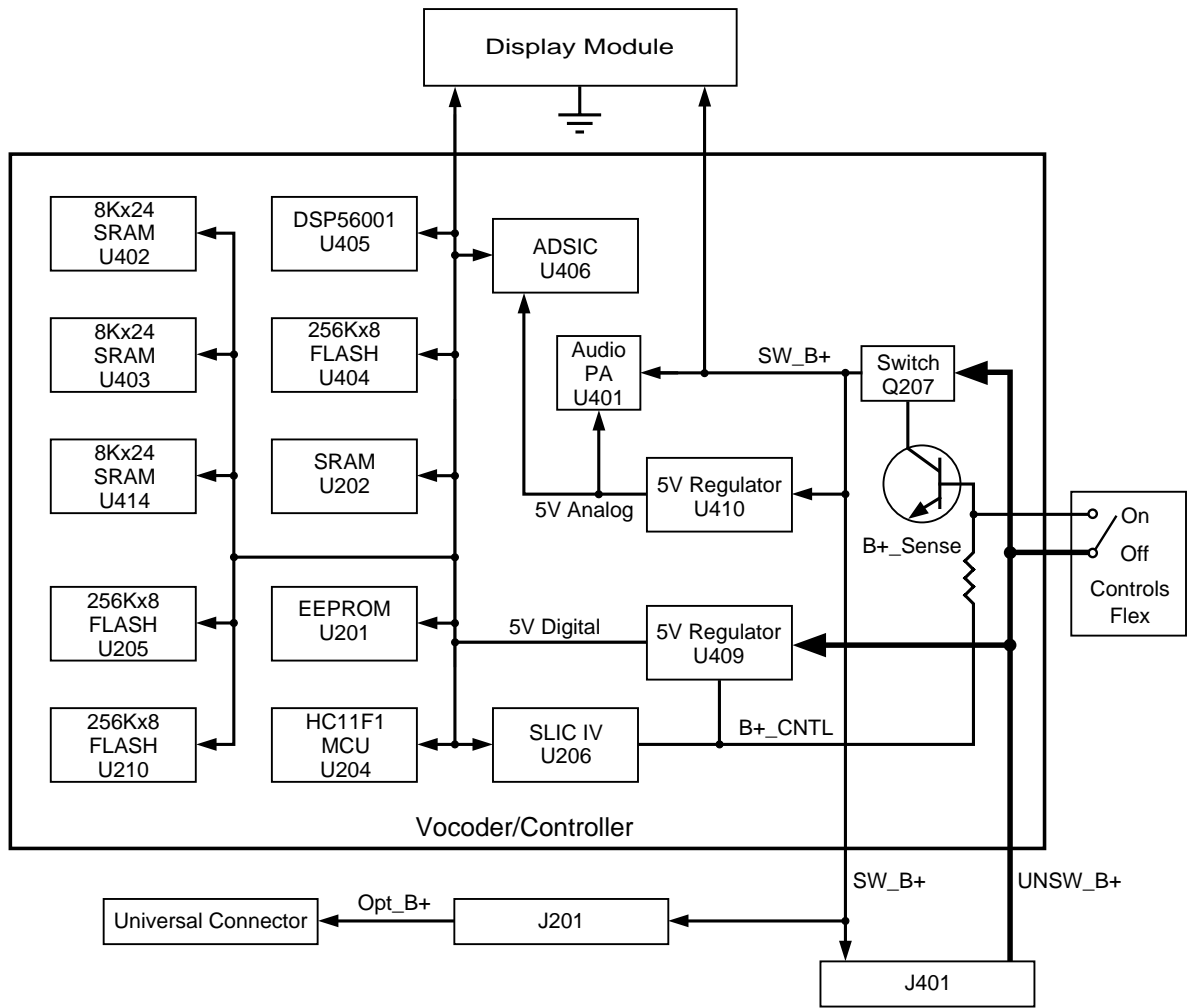
In the case of a secure radio model, SW B+ and UNSW B+ are also supplied to the encryption module through J801.

Q207 is also under the control of the microcontrol unit (MCU - U204) through a port on the SLIC IC (U206). This allows the MCU to follow an orderly power-down sequence when it senses the SW B+ is off. This sense is provided through the resistor network of R222 and R223, which provides an input to the A/D port on the MCU.

The VOCON board contains two 5V regulators partitioned between the digital logic circuitry and the analog circuitry. The 5V regulator for the digital circuitry is comprised of U409, CR403, L402, C470, and associated components. This circuit is a switched mode regulator. Switched mode regulators use a switched storage device (L402) to supply just enough energy to the output to maintain regulation. This allows for much greater efficiency and lower power dissipation.

The analog circuitry of the ADSIC (U406) and the audio PA (U401) is powered through a separate 5V linear regulator (U410).

It should also be noted that a system reset is provided by U407. This device brings the system out of reset on power-up. It provides a system reset to the microcomputer on power-down or if the digital 5V regulator falls out of regulation.



MAEPF-24335-O

Figure 3 . B+ Routing for Vocoder/Controller (VOCON) Boards



# VHF/UHF Transceiver Board Detailed Theory of Operation



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## Introduction

This section of the manual provides a detailed circuit description of an ASTRO Digital SABER VHF and UHF Transceiver Board. When reading the theory of operation, refer to your appropriate schematic and component location diagrams located in the back section of this manual. This detailed theory of operation will help isolate the problem to a particular component. However, first use the ASTRO Digital SABER Portable Radios Basic Service Manual to troubleshoot the problem to a particular board.

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## Frequency Generation Unit (FGU)

The frequency generation unit (FGU) consists of three major sections: the high stability reference oscillator (U203), the fractional-N synthesizer (U204,) and the VCO buffer (U201). A 5V regulator (U202), supplies power to the FGU. The synthesizer receives the 5V REG at U204, and applies it to a filtering circuit within the module and capacitor C253. The well-filtered 5-volt output at U204 pin 19 is distributed to the TX and RX VCOs and the VCO buffer IC. The mixer LO injection signal and transmit frequency are generated by the RX VCO and TX VCO respectively. The RX VCO uses an external active device (Q202), whereas the VHF TX VCO active device is a transistor inside the VCO buffer. The UHF TX VCO uses two active devices, one external (Q203) and the other internal to the VCO buffer. The base and emitter connections of this internal transistor are pins 11 and 12 of U201.

The RX VCO is a Colpitts-type oscillator, with capacitors C235 and C236 providing feedback. The RX VCO transistor (Q202) is turned on when pin 38 of U204 switches from high to low. The RX VCO signal is received by the VCO buffer at U201 pin 9, where it is amplified by a buffer inside the IC. The amplified signal at pin 2 is routed through a low-pass filter (L201 and associated capacitors) and injected as the first LO signal into the mixer (U2 pin 8). In the VCO buffer, the RX VCO signal (or the TX VCO signal during transmit) is also routed to an internal prescaler buffer. The buffered output at U201 pin 16 is applied to a low-pass filter (L205 and associated capacitors). After filtering, the signal is routed to a prescaler divider in the synthesizer at U204 pin 21.

The divide ratios for the prescaler circuits are determined from information stored in a codeplug, which is part of the microcontrol unit (U204 on the VOCON board). The microprocessor extracts data for the division ratio as determined by the position of the channel-select switch (S902), and busses the signal to a comparator in the synthesizer. A 16.8MHz reference oscillator, U203, applies the 16.8MHz signal to the synthesizer at U204 pin 14. The oscillator signal



is divided into one of three pre-determined frequencies. A time-based algorithm is used to generate the fractional-N ratio.

If the two frequencies in the synthesizer's comparator differ, a control (error) voltage is produced. The phase detector error voltage (V control) at pin 31 and 33 of U204, is applied to the loop filter consisting of resistors R211, R212, and R213, and capacitors C244, C246, C247 and C275. The filtered voltage alters the VCO frequency until the correct frequency is synthesized. The phase detector gain is set by components connected to U204 pins 28 and 29.

In the TX mode, U204 pin 38 goes high and U201 pin 14 goes low, which turns off transistor Q202 and turns on the internal TX VCO transistor in U204 and the external TX VCO buffer Q203 on the UHF circuit. The TX VCO feedback capacitors are C219 and C220. Varactor diode CR203 sets the TX frequency while varactor CR202 is the TX modulation varactor. The modulation of the carrier is achieved by using a 2-port modulation technique. The modulation of low frequency tones such as DPL/TPL is achieved by injecting the tones into the A/D section of the fractional-N synthesizer. The digitized signal is modulated by the fractional-N divider, generating the required deviation. Modulation of the high frequency audio signals is achieved by modulating the varactor (CR203) through a frequency compensation network. Resistors R207 and R208 form a potential divider for the higher frequency audio signals.

In order to cover the very wide bandwidths, positive and negative V-control voltages are used. High control voltages are achieved using positive and negative multipliers. The positive voltage multiplier circuit consists of components CR204, C256, C257 and reservoir capacitor C258. The negative multiplier circuit consists of components CR205, CR206, C266, C267 and reservoir capacitor C254 in VHF and UHF radios. Out-of-phase clocks for the positive multiplier appear at U204 pins 9 and 10. Out-of-phase clocks for the negative multiplier appear at U204 pins 7 and 8, and only when the negative V-control is required (i.e., when the VCO frequency exceeds the crossover frequency). When the negative V-control is not required, transistor Q201 is turned on, and capacitor C259 discharges. The 13V supply generated by the positive multiplier is used to power-up the phase detector circuitry. The negative V-control is applied to the anodes of the VCO varactors.

The TX VCO signal is amplified by an internal buffer in U201, routed through a low pass filter and routed to the TX PA module, U105 pin 1. The TX and RX VCOs and buffers are activated via a control signal from U204 pin 38.

The reference oscillator supplies a 16.8MHz clock to the synthesizer where it is divided down to a 2.1MHz clock. This divided-down clock is fed to the ABACUS IC (U401), where it is further processed for internal use.

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## Antenna Switch

Two antenna switches are part of the radio circuitry. One of the switches which is located in the radio casting is mechanical. It switches between the radio antenna and a remote antenna. Switching is accomplished by a plunger located on the accessory connector. With a remote antenna installed, continuity between the radio antenna and the RF input line is broken; continuity is made from the remote antenna to the radio RF line. The second switch is a current device. It is a pair of diodes (CR108/CR109) that electronically steer RF between the receiver and the transmitter. In the transmit mode, RF is routed through transmit switching diode CR108, and sent to the antenna. In the receive mode, RF is received from the antenna, routed through receive switching diode CR109, and applied to the RF amplifier, U1 (UHF), Q1 (VHF). In transmit, bias current, sourced from U101 pin 21, is routed through L105, U104, CR108, and L122 in VHF and L105, CR108, and L122 in UHF. Sinking of the bias current is through the transmit ALC module, U101 pin 19. In the receive mode, bias current, sourced from SB+, is routed through Q107 (pin 3 to pin 2), L123 (UHF), L121, CR109, and L122. Sinking of the bias current is through the 5-volt regulator, U106 pin 8.

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## Receiver Front End

The RF signal is received by the antenna and coupled through the external RF switch. The UHF board applies the RF signal to a low-pass filter comprised of: L126, L127, L128, C149, C150, and C151. The VHF board bypasses the lowpass filter. The filtered RF signal is passed through the antenna switch (CR109) and applied to a bandpass filter comprised of: VHF; L11 through L14, CR1 through CR9, C4, C2, and C3, or UHF; L30, L31, L32, L34, L35, CR6 through CR9, C1, C2, and C3. The bandpass filter is tuned by applying a control voltage to the varactor diodes in the filter. (CR1-CR9 in VHF and CR6-CR9 in UHF.)

The bandpass filter is electronically tuned by the D/A IC (U102) which is controlled by the microcomputer. The D/A output range is extended through the use of a current mirror, transistor Q108 and associated resistors R115 and R116. When Q108 is turned on via R115, the D/A output is reduced due to the voltage drop across R116. Depending on the carrier frequency the microcomputer will turn on or off Q108. Wideband operation of the filter is achieved by retuning the bandpass filter across the band.

The output of the bandpass filter is applied to a wideband GaAs RF amplifier IC, U1 (RF AMP) on the UHF transceiver board. The VHF board uses an active device for RF amplification (Q1). After being amplified by the RF AMP, the RF signal is further filtered by a second broad-band, fixed-tuned, bandpass filter consisting of C6, C7, C8, C80, C86, C87, C88, C97, C99, L3, L4, L5, and L30 (VHF); or C4 through C7, C88 through C94, C99, and L11 through L15 (UHF) to improve the spurious rejection.

Via a broadband 50-ohm transformer, T1, the filtered RF signal is routed to the input of a broadband mixer/buffer (U2). Mixer U2 uses GaAs FETs, in a double-balanced Gilbert Cell configuration. The RF signal is applied to the mixer at U2 pins 1 and 15. An injection signal (1st LO) of about -10dBm, supplied by the FGU, is applied to U2 pin 8. Mixing of the RF and the 1st LO results in an output signal which is

the first IF frequency. The first IF frequency of VHF and UHF bands are 45.15MHz and 73.35MHz respectively. The 1st LO signal for VHF is 45.15MHz higher than the carrier frequency while that for the UHF is 73.35MHz lower than the carrier frequency. The 1st IF signal output, at U2 pins 4 and 6, is routed through transformer T2 and impedance matching components, and applied to a 2-pole crystal filter (FL1), which is the final stage of the receiver front end. The 2-pole crystal filter removes unwanted mixer products. Impedance matching between the output of the transformer (T2) and the input of the filter (FL1) is accomplished by capacitor C605 and inductor L605 (VHF); or C611, C614 and L605 (UHF).

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## Receiver Back End

The output of crystal filter FL1 is matched to the input of IF buffer amplifier transistor Q601 by components C610 and L604 (VHF) and C609, C610, and L600 (UHF). Transistor Q601 is biased by the 5V regulator (U202). The IF frequency on the collector of Q601 is applied to a second crystal filter through a matching circuit. The second crystal filter (FL2) input is matched by C604, C603, and L601 (VHF); or C604, L601, and L602 (UHF). The filter supplies further attenuation at the IF sidebands to increase the radios selectivity. The output of FL2 routed to pin 32 of U401 through a matching circuit which consists of L603, L606, and C608 (VHF); or L603, C606, and C605 (UHF).

In the ABACUS IC, (U401) the first IF frequency is amplified and then down converted to 450kHz, the second IF frequency. At this point, the analog signal is converted into two digital bit streams via a sigma-delta A/D converter. The bit streams are then digitally filtered and mixed down to baseband and filtered again. The differential output data stream is then sent to the ADSIC (U406) on the VOCON board where it is decoded to produce the recovered audio.

The ABACUS IC (U401) is electronically programmable, and the amount of filtering which is dependent on the radio channel spacing and signal type is controlled by the microcomputer. Additional filtering, which used to be provided externally by a conventional ceramic filter, is replaced by internal digital filters in the ABACUS IC. The ABACUS IC contains a feedback AGC circuit to expand the dynamic range of the sigma-delta converter. The differential output data contains the quadrature (I and Q) information in 16-bit words, the AGC information in a 9-bit word, imbedded word sync information and fill bits dependent on sampling speed. A fractional-n synthesizer is also incorporated on the ABACUS IC for 2nd LO generation.

The 2nd LO/VCO is a Colpitts oscillator built around transistor Q401 (VHF) and Q1 (UHF). The VCO has a varactor diode, VR401 (VHF) and CR5 (UHF), to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C426, C428, and R413.

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## Transmitter

The transmitter consists of three major sections:

- Harmonic Filter
- RF Power Amplifier Module
- ALC Circuits

## Harmonic Filter

RF from the power amplifier (PA) module (U105) is routed through the coupler (U104), passed through the transmit antenna switch (CR108), and applied to a harmonic filtering network in UHF. In the case of a VHF transceiver board, RF from the PA module (U105) is routed also through the coupler (U104), then through the harmonic filtering network, and on to the antenna switch (CR108). The harmonic filtering circuit is comprised of the following components: L126, L127, L128, C149, C150, and C151 (for VHF models); or L126, L127, L128, C149, C150, and C151 (for UHF models). Resistor R128 (UHF) or R117 (VHF) provides a current limited 5V to J2 for mobile ASTRO vehicular adapter (AVA) applications.

## RF Power Amplifier Module

The RF power amplifier module (U105) is a wide-band multi-stage amplifier (3 stages for the VHF models and 4 stages for the UHF models). Nominal input and output impedance of U105 is 50 ohms. The dc bias for U105 is on pins 2, 4, 5. In the transmit mode, the voltage on U105 pins 2 and 4 (close to the B+ level) is obtained via switching transistor Q101. Transistor Q101 receives its control base signal as follows:

- the microcomputer keys the D/A IC to produce a ready signal at U102 pin 3
- the ready signal at U102 pin 3 is applied to the TX ALC IC at U101 pin 14 (5V)
- the synthesizer sends a LOC signal to the TX ALC IC (U204 pin 40 to U101 pin 16)

When the LOC signal and the ready signal are both received, the TX ALC IC (pin 13) sends a control signal to turn on transistor Q101.

## ALC Circuits

Coupler module U104 samples the forward power and the reverse power of the PA output voltage. Reverse power is present when there is other than 50 ohms impedance at the antenna port. Sampling is achieved by coupling some of the forward and/or reverse power, and apply it to CR102(VHF) or CR101(UHF) and CR103 for rectification and summing. The resultant dc signal is then applied to the TX ALC IC (U101 pin 2) as RFDET to be used as an RF strength indicator.

The transmit ALC circuit, built around U101, is the heart of the power control loop. Circuits in the TX ALC module compare the signals at U101 pins 2 and 7. The resultant signal, C BIAS, at U101 pin 4 is applied to the base of transistor Q110. In response to the base drive, transistor Q110 varies the dc control voltages applied to the RF PA at U105 pin 3, thus controlling the RF power of module (U105).

Thermistor RT101 senses the temperature of the TX ALC IC. If an abnormal operating condition exists, which causes the PA slab temperature to rise to an unacceptable level, the thermistor forces the ALC to reduce the set power.



# 800MHz Transceiver Board Detailed Theory of Operation



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## Introduction

This section of the manual provides a detailed circuit description of an ASTRO Digital SABER 800MHz Transceiver Board. When reading the theory of operation, refer to your appropriate schematic and component location diagrams located in the back section of this manual. This detailed theory of operation will help isolate the problem to a particular component. However, first use the ASTRO Digital SABER Portable Radios Basic Service Manual to troubleshooting the problem to a particular board.

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## Frequency Synthesis

The complete synthesizer subsystem consists of the reference oscillator (U304), the voltage controlled oscillator (VCO), U307, a buffer IC (U303), and the synthesizer (U302).

The reference oscillator contains a temperature-compensated 16.8MHz crystal. This oscillator is digitally tuned and contains a temperature-referenced 5-bit analog-to-digital (A/D) converter. The output of the oscillator (pin 10 on U304) is applied to pin 14 (XTAL1) on U302 via capacitor C309 and resistor R306.

Module U307 is the voltage controlled oscillator, which is varactor tuned. That is, as the voltage (2-11V) being applied to pins 1 and 7 of the VCO varies, so does the varactor's capacitance, thereby changing the VCO's output frequency. The 800MHz VCO is a dual-range oscillator that covers the 806-825MHz and the 851-870MHz frequency bands. The low-band VCO (777-825MHz) provides the first LO injection frequencies (777-797MHz) that will be 73.35MHz below the carrier frequency. In addition, when the radio is operated through a repeater, the low-band VCO will generate the transmit frequencies (806-825MHz) that will be 45MHz below the receiver frequencies. The low-band VCO is selected by pulling pin 3 high and pin 8 low on U307. When radio-to-radio or talk-around operation is necessary, the high band VCO (851-870MHz) is selected. This is accomplished by pulling pin 3 low and pin 8 high on U307.

The buffer IC (U303) includes a TX, RX, and prescaler buffer whose main purpose is to individually maintain a constant output and provide isolation. The TX buffer is chosen by setting pin 7 of U303 high; the RX buffer is chosen by setting pin 7 of U303 low. The prescaler buffer will always be on. In order to select the proper combination of VCO and buffer, the following conditions must be true at pin 6 of U303 (or pin 38 of U302) and pin 7 of U303 (or pin 39 of U302). For the first LO injection frequencies 777-797MHz, pins 6 and 7 must both be low; for the TX repeater frequencies 806-825MHz pins

6 and 7 must both be high. For talkaround TX frequencies 851-870MHz, pin 6 must be low while pin 7 must be high.

The synthesizer IC (U303) consists of a prescaler, a programmable loop divider, a divider control logic, a phase detector, a charge pump, an A/D converter for low-frequency digital modulation, a balance attenuator to balance the high frequency analog modulation to the low frequency digital modulation, a 13V positive-voltage multiplier, a serial interface for control, and finally a filter for the regulated five volts. This filtered five volts is present at pin 19 of U302, pin 9 of U307, and pins 2, 3, 4, and 15 of U303. It is also applied directly to resistors R309, R315, and R311. Additionally, the 13V, being generated by the positive voltage multiplier circuitry, should be present at pin 35 of U302. The serial interface (SRL) is connected to the microprocessor via the data line (pin 2 of U302), clock line (pin 3 of U302), and chip enable line (pin 4 of U302).

The complete synthesizer subsystem works as follows. The output of the VCO, pin 4 on U307, is fed into the RF input port (pin 9) of U303. In the TX mode, the RF signal will be present at pin 4 of U303. On the other hand, in the RX mode, the RF signal will be present at pin 3 of U303. The output of the prescaler buffer, pin 15 on U303, is applied to the PREIN port (pin 21) of U302. The prescaler in U302 is a dual-modulus type with selectable divider ratios. This divider ratio is controlled by the loop divider, which in turn receives its inputs via the SRL. The loop divider adds or subtracts phase to the prescaler divider by changing the divide ratio via the modulus control line. The output of the prescaler is then applied to the loop divider. The output of the loop divider is then applied to the phase detector. The phase detector will then compare the loop divider's output signal with the signal from U304 (that is divided down after it is applied to pin 14 of U302). The result of the signal comparison is a pulsed dc signal which is applied to the charge pump. The charge pump outputs a current that will be present at pin 32 of U302. The loop filter (which consists of capacitors C322, C317, C318, C329, C324, and C315, and resistors R307, R305, and R314) will transform this current into a voltage that will be applied to pins 1 and 7 of U307, and alter the VCO's output frequency.

In order to modulate the PLL, the two-port modulation method is utilized. The analog modulating signal is applied to the A/D converter as well as the balance attenuator, via U302 pin 5. The A/D converter converts the low-frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high-frequency modulating signals.

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## Antenna Switch

Switching between the standard and external antenna ports is accomplished with the external mechanical switch which is actuated by a plunger located on the accessory connector.

An electronic PIN diode switch steers RF between the receiver and transmitter. The common node of the switch is at capacitor C101. In the transmit mode, RF is routed to the anode of diode CR104. In receive mode, RF is routed to pin 1 of U201. In transmit, bias current sourced from U504 pin 21, is routed through PIN diodes CR104 and

CR102, biasing them to a low-impedance state. Bias current returns to ground through U504 pin 20. In receive, U504 pin 21 is pulled down to ground and pin 20 is pulled up to B+, reverse biasing diodes CR104 and CR102 to a high impedance.

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## Receiver Front End

For the purposes of this discussion, the receiver front end is defined to be the circuitry from the antenna switch to the output of the IF crystal filter. The 800MHz front end is designed to convert the received RF signal to the 1st IF frequency of 73.35MHz, while at the same time providing for spurious immunity and adjacent channel selectivity. A review of the interstage components of the front end will now be presented with emphasis on troubleshooting considerations.

The received RF signal is passed through the antenna switch input matching components C101, L105, and C114 tank components C106 and L103 (which are anti-resonant at the radios transmitter frequencies), and output matching components C103 and L104. Both pin diodes CR102 and CR104 must be back biased to properly route the received signal.

The stage following the antenna switch is a 50-ohm, inter-digitated, 3-pole, stripline preselector (U201). The preselector is positioned after the antenna switch to provide the receiver preamp some protection to strong signal, out-of-band signals.

After the preselector (U201), the received signal is processed through the receiver preamp, U202. The preamp is a dual-gate GaAs MESFET transistor which has been internally biased for optimum IM, NF, and gain performance. Components L201 and L202 match the input (gate 1) of the amp to the first preselector, while at the same time connecting gate 1 to ground potential. The output (drain) of the amp is pin 3 and is matched to the subsequent receiver stage via components L204, C205 and C222. A supply voltage of 5Vdc is provided to pin 3 via an RF choke L203 and bypass C204. The 5 volt supply is also present at pin 4 which connects to a voltage divider network that biases gate 2 (pin 5) to a predefined quiescent voltage of 1.2Vdc. Resistor R202 and capacitor C203 are connected to pin 5 to provide amp stability. The FET source (pin 7) is internally biased at 0.55 to 0.7Vdc for proper operation with bypass capacitors C201 and C202 connected to the same node.

The output of the amp is matched to a second 3-pole preselector (U203) of the type previously discussed. The subsequent stage in the receiver chain is the 1st mixer U205, which uses low-side injection to convert the RF carrier to an intermediate frequency (IF) of 73.35MHz. Since low-side injection is used, the LO frequency is offset below the RF carrier by 73.35MHz, or  $F_{lo} = F_{rf} - 73.35\text{MHz}$ . The mixer utilizes GaAs FETs in a double balanced Gilbert Cell configuration. The LO port (pin 8) incorporates an internal buffer and a phase shift network to eliminate the need for a LO transformer. The LO buffer bypass capacitors (C208, C221, and C216) are connected to pin 10 of U205, and should exhibit a nominal dc voltage of 1.2 to 1.4Vdc. Pin 11 of U205 is LO buffer Vdd (5Vdc) with associated bypass capacitors C226 and C209 connected to the same node. An internal voltage divider network within the LO buffer is bypassed to virtual ground at pin 12



of U205 via bypass C213. The mixer's LO port is matched to the radio's PLL by a capacitive tap, C207 and C206. A balun transformer (T202) is used to couple the RF signal into the mixer. The primary of T202 is matched to the preceding stage by capacitor C223, with C227 providing a dc block to ground. The secondary of T202 provides a differential output, with a 180° phase differential being achieved by setting the secondary center tap to virtual ground using bypass capacitors C210, C211 and C212. The secondary of transformer T202 is connected to pins 1 and 15 of the mixer IC, which drives the source leg of dual FETs used to toggle the paralleled differential amplifier configuration within the Gilbert Cell.

The final stage in the receiver front end is a 2-pole crystal filter (FL1). The crystal filter provides some of the receiver's adjacent channel selectivity. The input to the crystal filter is matched to the 1st mixer using components L605, C611 and C614. The output of the crystal filter is matched to the input of IF buffer amplifier transistor Q601 by components L600, C609, and C610.

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## Receiver Back End

The IF frequency on the collector of Q601 is applied to a second crystal filter (FL2) through a matching circuit consisting of L601, L602, C604, and C612. The filter supplies further attenuation at the IF sidebands to increase the radio's selectivity. The output of FL2 is routed to pin 32 of U401 through a matching circuit which consists of L603, C605, and C606 and dc block capacitor C613.

In the ABACUS IC, (U401) the first IF frequency is amplified and then down converted to 450kHz, the second IF frequency. At this point, the analog signal is converted into two digital bit streams via a sigma-delta A/D converter. The bit streams are then digitally filtered and mixed down to baseband and filtered again. The differential output data stream is then sent to the ADSIC (U406) on the VOCON board where it is decoded to produce the recovered audio.

The ABACUS IC (U401) is electronically programmable, and the amount of filtering which is dependent on the radio channel spacing and signal type is controlled by the microcomputer. Additional filtering, which used to be provided externally by a conventional ceramic filter, is replaced by internal digital filters in the ABACUS IC. The ABACUS IC contains a feedback AGC circuit to expand the dynamic range of the sigma-delta converter. The differential output data contains the quadrature (I and Q) information in 16-bit words, the AGC information in a 9-bit word, imbedded word sync information and fill bits dependent on sampling speed. A fractional-n synthesizer is also incorporated on the ABACUS IC for 2nd LO generation.

The second LO/VCO is a Colpitts oscillator built around transistor Q1. The VCO has a varactor diode (VR401), which is used to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C426, C428, and R413.

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## Transmitter

The 800MHz RF power amplifier (PA) is a 5-stage amplifier (U502). The RF power amplifier has a nominal input and output impedance of 50 ohms.

An RF input drive level of approximately +3dBm, supplied from the VCO buffer IC (U303), is applied to pin 1 of U502. The dc bias for the internal stages of U502 is applied to pins 2, 5, and 6 of the module. Pins 2 and 5 being switched through Q502 and pin 6 being unswitched B+ to the final amplifier stage. Power control is achieved through the varying of the dc bias to pins 3 and 4, the third and fourth amplifier stages of the module. The amplified RF signal leaves the PA module via pin 7 and is applied to the directional coupler (U501).

The purpose of U501 is to sample both the forward power and the reverse power. The reverse power will be present when there is other than a 50-ohm load at the antenna port. The sampling will be achieved by coupling some of the reflected power, forward and/or reverse, to a coupled leg on the coupler. The sampled RF signals are applied to diode CR501 for rectification and summing. The resultant dc signal is applied to the ALC IC (U504 pin 2) as RFDET to be used as an strength indicator of the RF signal being passed through the directional coupler (U501).

The transmit ALC IC (U504) is the heart of the power control loop. The REF V line (U504 pin 7), a dc signal supplied from the D/A IC (U503), and the RF DET signal described earlier, are compared internally in the ALC IC to determine the amount of C BIAS, pin 4, to be applied to the base of transistor Q501. Transistor Q501 responds to the base drive level by varying the dc control voltages applied to pin 3 and 4 of the RF PA, controlling the RF power level of module, U502. The ALC IC also controls the base switching to transistor Q502 via pin 12, BIAS.

The D/A IC (U503) controls the dc switching of the transceiver board. Its outputs, SC1 and SC3, pins 12 and 14 respectively, control transistor Q503, which then supplies TX 5V and RX 5V to the transceiver board. The D/A also supplies the dc bias to the detector diode (CR501) via pin 7, and the REF V signal to the ALC IC (U504).



# VOCON Board

## Detailed Theory of Operation



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### Introduction

This section of the manual provides a detailed circuit description of an ASTRO Digital SABER VOCON (Vocoder/Controller) Board. When reading the theory of operation, refer to your appropriate schematic and component location diagrams located in the back section of this manual. This detailed theory of operation will help isolate the problem to a particular component. However, first use the ASTRO Digital SABER Portable Radios Basic Service Manual to troubleshooting the problem to a particular board.

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### General

The VOCON board consists of two subsystems:

- vocoder
- controller

Although these two subsystems share the same printed circuit board and work closely together, it helps to keep their individual functionality separate in describing the operation of the radio.

The controller section is the central interface between the various subsystems of the radio. It is very similar to the digital logic portion of the controllers on many existing Motorola radios. Its main task is to interpret user input, provide user feedback, and schedule events in the radio operation, which includes programming ICs, steering the activities of the DSP and driving the display.

The vocoder section performs the functions which previously were performed by analog circuitry. This includes all tone signaling, trunking signalling, and conventional analog voice, etc. All analog signal processing is done digitally utilizing a DSP56001. In addition it provides a digital voice plus data capability utilizing VSELP or IMBE voice compression algorithms. Vocoder is a general term used to refer to these DSP based systems and is short for voice encoder.

In addition, the VOCON board provides the interconnect between the microcontrol unit (MCU), DSP, and the encryption board on secure-equipped radios.

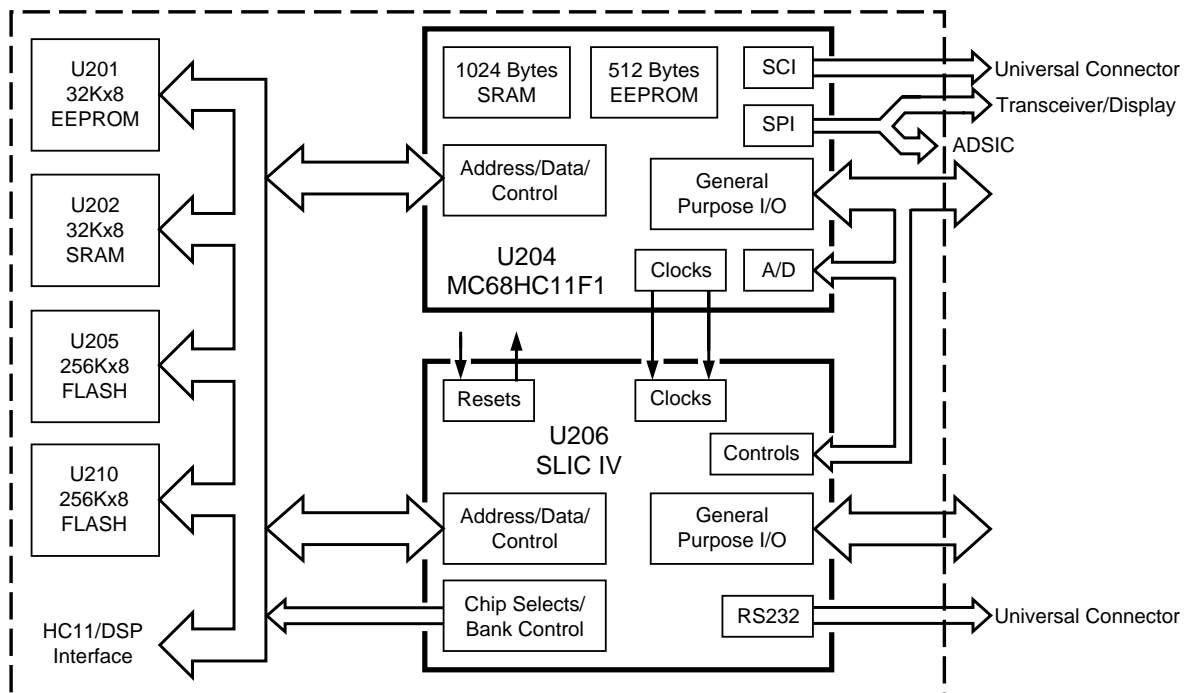
## Controller Section

Refer to *Figure 4* and your specific schematic diagram.

The controller section of the VOCON board consists entirely of digital logic comprised of a microcontrol unit (MCU-U204), a custom support logic IC (SLIC-U206), and memory consisting of: SRAM (U202), EEPROM (U201), and FLASH memory (U205, U210).

The MCU (U204) memory system is comprised of a 32k x 8 SRAM (U202), 32k x 8 EEPROM (U201), and 512k x 8 FLASH ROM (U205, U210). The MCU also contains 1024 bytes of internal SRAM and 512 bytes of internal EEPROM. The EEPROM memory is used to store customer specific information and radio personality features. The FLASH ROM contains the programs which the HC11F1 executes. The FLASH ROM allows the controller firmware to be reprogrammed for future software upgrades or feature enhancements. The SRAM is used for scratchpad memory during program execution.

The SLIC (U206) performs many functions as a companion IC for the MCU. Among these are expanded input/output (I/O), memory decoding and management, and interrupt control. It also contains the universal asynchronous receiver transmitter (UART) used for the RS232 data communications. The SLIC control registers are mapped into the MCU (U204) memory space.



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*Figure 4 . VOCON Board - Controller Section*

The controller performs the programming of all peripheral ICs. This is done through a serial peripheral interface (SPI) bus. ICs programmed through this bus include the synthesizer, DAIC, reference oscillator, display, and ADSIC. On secure-equipped model, the encryption board is also controlled through the SPI bus.

In addition to the SPI bus, the controller also maintains two asynchronous serial busses; the SB9600 bus and an RS232 serial bus. The SB9600 bus is for interfacing the controller section to different hardware option boards, some of which may be external to the radio. The RS232 is used for the function of a common data interface for external devices.

User input is handled by the controller through top rotary controls and side buttons. On models with a display, an additional 3 x 2 or 3 x 6 keypad are also read. User feedback is provided by a single bicolor LED on the top and a two-line, fourteen-character display if equipped.

The controller schedules the activities of the DSP through the host port interface. This includes setting the operational modes and parameters of the DSP. The controlling of the DSP is analogous to programming analog signaling ICs on standard analog radios.

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## Vocoder Section

Refer to *Figure 5* and your specific schematic diagram.

The vocoder section of the VOCON board is made up of a digital signal processor (DSP-U405), 24k x24 static-RAM (SRAMs-U414, U403, and U402), 256kB FLASH ROM (U404), ABACUS/DSP support IC (ADSIC-U406), and an audio PA (U401).

The FLASH ROM (U404) contains the program code executed by the DSP. As with the FLASH ROM used in the controller section, the FLASH ROM is reprogrammable so new features and algorithms can be updated in the field as they become available. Depending on the mode and operation of the DSP, corresponding program code is moved from the FLASH ROM into the faster SRAM, where it is executed at full bus rate.

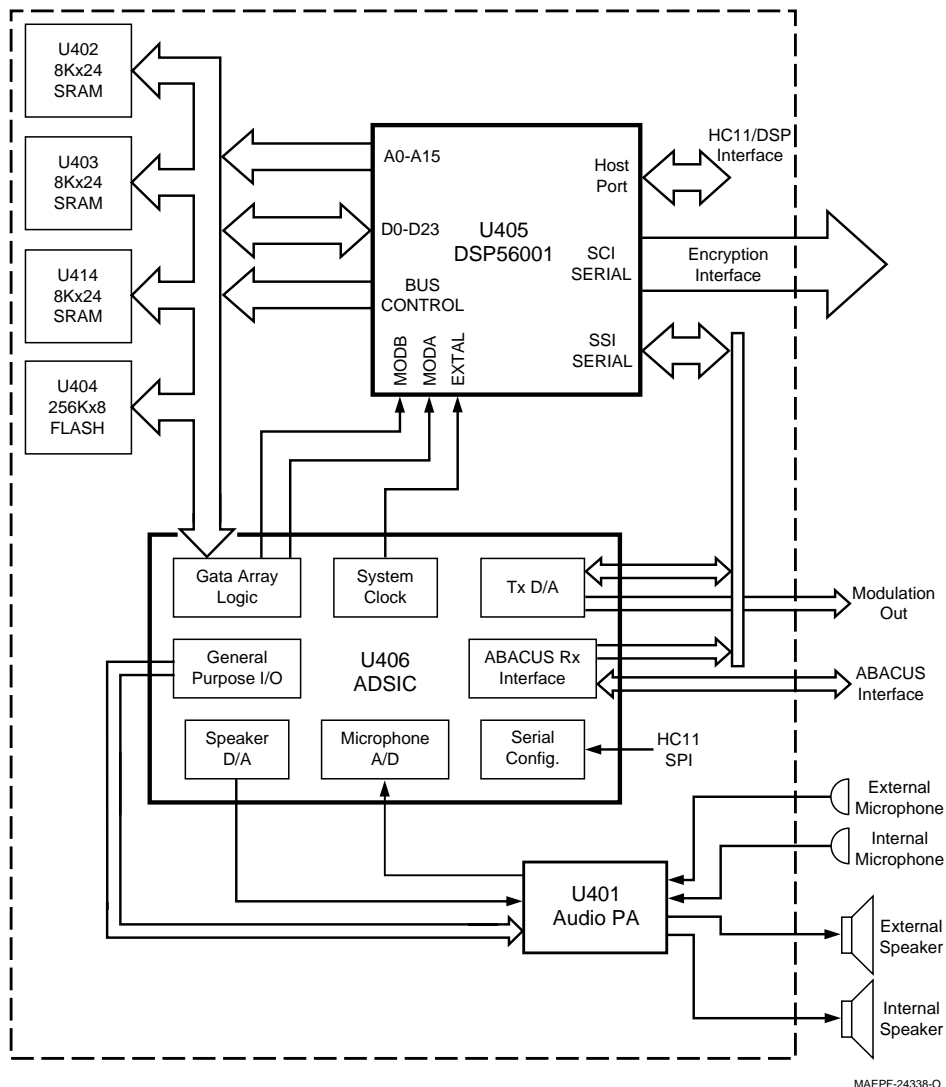
The ADSIC (U406) is basically a support IC for the DSP. It provides among other things, the interface from the digital world of the DSP to the analog world. The ADSIC also provides some memory management and provides interrupt control for the DSP processing algorithms. The configuration programming of the ADSIC is performed by the MCU. However some components of the ADSIC are controlled through a parallel memory mapped register bank by the DSP.

In the receive mode, The ADSIC (U406) acts as an interface to the ABACUS IC, which can provide IF data samples directly to the DSP for processing. Or the IF data can be filtered and discriminated by the ADSIC and data provided to the DSP as raw discriminator sample data. The latter mode, with the ADSIC performing the IF filtering and discrimination, is the typical mode of operation.

In the transmit mode, the ADSIC (U406) provides a serial digital-to-analog (D/A) converter. The data generated by the DSP is filtered and reconstructed as an analog signal to present to the VCO as a modulation signal. Both the transmit and receive data paths between the DSP and ADSIC are through the DSP SSI port.

The only analog device in the vocoder section is the audio PA (U401). This IC is an audio amplifier for the microphone analog input and speaker analog output. The audio PA allows steering between the internal and external microphone and internal and external speaker. Steering is accomplished through four control lines provided by the ADSIC and controlled by the DSP through the ADSIC parallel registers.

The amplified microphone signal is provided to the ADSIC, which incorporates an analog-to-digital (A/D) converter to translate the analog waveform to a series of data. The data is available to the DSP through the ADSIC parallel registers. In the converse way, the DSP writes speaker data samples to a D/A in the ADSIC, which provides an analog speaker audio signal to the audio PA.



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Figure 5 . VOCON Board - Vocoder Section

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## Switched Regulator

All of the digital circuitry on the VOCON is supplied 5 volt regulated dc by a switched mode regulator (refer to *Figure 3 on page 5* of Chapter 4). The fundamental parts of the regulator are U409, L402, C470, CR403, C463, and U407. Module U409 is a pulse width modulating (PWM) switched regulator controller. Coil L402 is an energy storage element, C470 is an output ripple filter, and CR403 is a Schottky diode switch. Capacitor C463 is added for UNSW\_B+ ripple filter and is necessary for stability of the regulator. Module U407 is a supply supervisory IC, which provides a system reset function when the output of the regulator falls out of regulation, typically around 4.6Vdc.

This switched mode regulator works by supplying just sufficient energy to the storage element to maintain the output power of the regulator at 5Vdc. It can be related to a flywheel in the sense that just enough energy can be added to a spinning flywheel to keep it spinning at a constant speed. In contrast to a typical linear type regulator, which basically shunts unused current to ground through an active resistive divider. The switched mode regulator is much more energy efficient. It can be noted that input current to the regulator is less than the load current. In fact, as input voltage to the regulator goes up, current supplied to the regulator actually goes down for a constant load.

Module U409 works off of a clock with a nominal operating frequency of 160kHz (kit number NTN7749E), or 260kHz (kit numbers NTN7749F and NTN7749G). This may vary a little based on the load and input voltage. It maintains regulation by varying the duty cycle of a clock output driving L402. This signal is referred to as Lx on U409 (refer to *Waveform W1*). As long as the clock output is high, current flows from the supply into L402 allowing energy to be stored. When the clock output goes low, the diode CR403 conducts, allowing current to continue to flow from ground through L402. A pulse width on the Lx signal can be obtained, which provides the correct amount of energy to keep the output in regulation. Capacitor C470 is an output filter to reduce ripple on the output from the clock transitions.

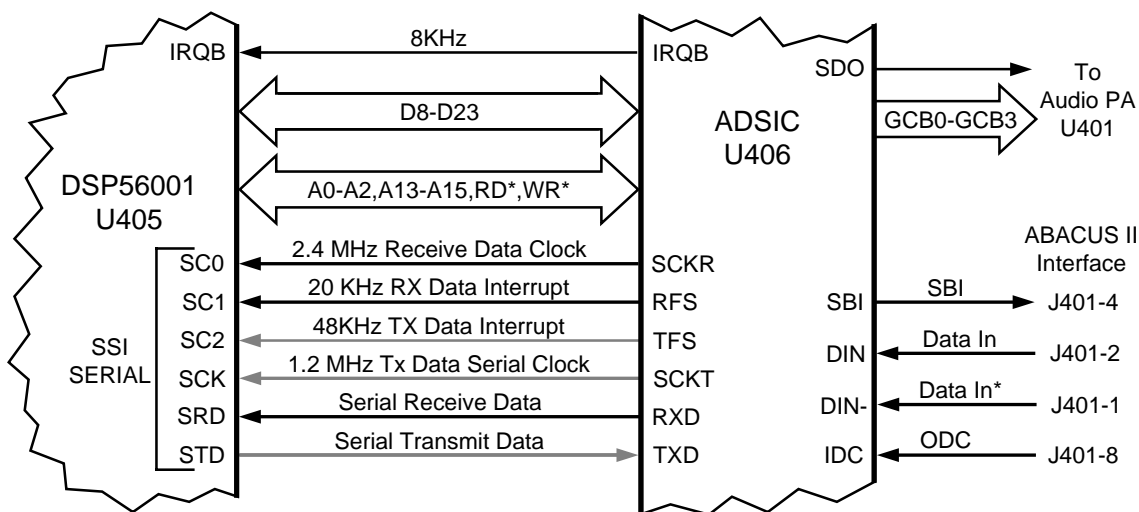
Module U409 is supplied directly from the unswitched battery supply. It is turned on and off through the control line connected to SHDN\*/ON/OFF. This is the same control line from the MCU, which controls the series pass element Q207, which switches SW\_B+. A voltage level of approximately 2Vdc is required to turn the regulator on.



## RX Signal Path

The vocoder processes all received signals digitally. This requires a unique back end from a standard analog radio. This unique functionality is provided by the ABACUS IC with the ADSIC (U406) acting as the interface to the DSP. The ABACUS IC located on the transceiver board provides a digital back end for the receiver section. It provides a digital output of I (In phase) and Q (Quadrature) data words which represent the IF (Intermediate Frequency) signal at the receiver back end (refer to appropriate transceiver section for more details on ABACUS operation). This data is passed to the DSP through an interface with the ADSIC (U406) for appropriate processing.

The ADSIC interface to the ABACUS is comprised of the four signals SBI, DIN, DIN\*, and ODC (refer to *Figure 6*).



MAEPF-24339-O

Figure 6 . DSP RSSI Port - RX Mode

**NOTE:** An asterisk symbol (\*) next to a signal name indicates a negative or NOT logic true signal.

ODC is a clock ABACUS provides to the ADSIC. Most internal ADSIC functions are clocked by this ODC signal at a rate of 2.4MHz and is available as soon as power is supplied to the circuitry. This signal may initially be 2.4 or 4.8MHz after power-up. It is programmed by the ADSIC through the SBI signal to 2.4MHz when the ADSIC is initialized by the MCU through the SPI bus. For any functionality of the ADSIC to exist, including initial programming, this reference clock must be present. SBI is a programming data line for the ABACUS. This line is used to configure the operation of the ABACUS and is driven by the ADSIC. The MCU programs many of the ADSIC operational features through the SPI interface. There are 36 configuration registers in the ADSIC of which four contain configuration data for the ABACUS. When these particular registers are programmed by the MCU, the ADSIC in turn sends this data to the ABACUS through the SBI.

DIN and DIN\* are the data lines in which the I and Q data words are transferred from the ABACUS. These signals make up a differentially encoded current loop. Instead of sending TTL type voltage signals, the data is transferred by flowing current one way or the other through the loop. This helps reduce internally generated spurious emissions on the transceiver board. The ADSIC contains an internal current loop decoder which translates these signals back to TTL logic and stores the data in internal registers.

In the fundamental mode of operation, the ADSIC transfers raw IF data to the DSP. The DSP can perform IF filtering and discriminator functions on this data to obtain a baseband demodulated signal. However, the ADSIC contains a digital IF and discriminator function and can provide this baseband demodulated signal directly to the DSP, this being the typical mode of operation. The internal digital IF filter is programmable up to 24 taps. These taps are programmed by the MCU through the SPI interface.

The DSP accesses this data through its SSI serial port. This is a 6 port synchronous serial bus. It is actually used by the DSP for both transmit and receive data transfer, but only the receive functions will be discussed here. The ADSIC transfers the data to the DSP on the SRD line at a rate of 2.4MHz. This is clocked synchronously by the ADSIC which provides a 2.4MHz clock on SC0. In addition, a 20kHz interrupt is provided on SC1 signaling the arrival of a data packet. This means a new I and Q sample data packet is available to the DSP at a 20kHz rate which represents the sampling rate of the received data. The DSP then processes this data to extract audio, signaling, etc. based on the 20kHz interrupt.

In addition to the SPI programming bus, the ADSIC also contains a parallel configuration bus consisting of D8-D23, A0-A2, A13-A15, RD\*, and WR\*. This bus is used to access registers mapped into the DSP memory starting at Y:FFF0. Some of these registers are used for additional ADSIC configuration controlled directly by the DSP. Some of the registers are data registers for the speaker D/A. Analog speaker audio is processed through this parallel bus where the DSP outputs the speaker audio digital data words to this speaker D/A and an analog waveform is generated which is output on SDO (Speaker Data Out). In conjunction with the speaker D/A, the ADSIC contains a programmable attenuator to set the rough signal attenuation. However, the fine levels and differences between signal types is adjusted through the DSP software algorithms. The speaker D/A attenuator setting is programmed by the MCU through the SPI bus.

The ADSIC provides an 8kHz interrupt to the DSP on IRQB for processing the speaker data samples. IRQB is also one of the DSP mode configuration pins at start up. This 8kHz signal must be enabled through the SPI programming bus by the MCU and is necessary for any audio processing to occur.

For secure messages, the analog signal data may be passed to the secure module prior to processing speaker data for decryption. The DSP transfers the data to and from the secure module through its SCI port consisting of TXD and RXD. The SCI port is a two wire duplex asynchronous serial port. Configuration and mode control of the secure module is performed by the MCU through the SPI bus.

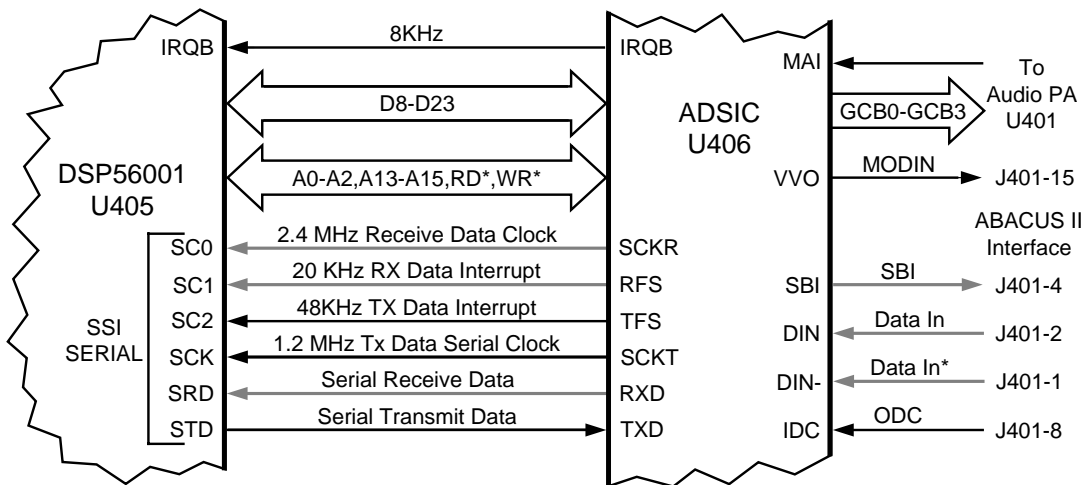
The ADSIC contains four general purpose I/O labeled GCB0 -GCB3. These are connected to the AUDIO PA and are used for enabling the speaker and microphone amplifiers in the IC and for steering the speaker and microphone audio paths from internal to external. These I/O are controlled by the DSP through the ADSIC parallel configuration bus. The DSP then writes speaker data samples to the speaker D/A register through the parallel bus at an 8kHz rate and configures the AUDIO PA enable lines by writing the same bus to the register controlling the I/O.

The audio PA provides about 20dB of gain and a dual ended differential output; SPKR\_COMMON, and EXT\_SPKR or INT\_SPKR. Internal or external speaker drive is achieved by changing the phase of the outputs on INT\_SPKR and EXT\_SPKR to be either in phase or out of phase with SPKR\_COMMON. The signal which is out of phase with SPKR\_COMMON will be driven.

Since all of the audio and signaling is processed in DSP software algorithms, all types of audio and signaling follow this same path.

## TX Signal Path

The transmit signal path follows some of the same design structure as the receive signal path described above in section D (refer to *Figure 7*). It is advisable to read through the section on RX Signal Path prior to this section.



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*Figure 7. DSP RSSI Port - TX Mode*

The ADSIC contains a microphone A/D with a programmable attenuator for coarse level adjustment. As with the speaker D/A attenuator, the microphone attenuator value is programmed by the MCU through the SPI bus. The analog microphone signal from the Audio PA (U401) is input to the A/D on MAI (Mic Audio In). The microphone A/D converts the analog signal to a series of data words and stores them in internal registers. The DSP accesses this data through the parallel data bus parallel configuration bus consisting of D8-D23, A0-A2, A13-A15, RD\*, and WR\*. As with the speaker data

samples, the DSP reads the microphone samples from registers mapped into its memory space starting at Y:FFF0. The ADSIC provides an 8kHz interrupt to the DSP on IRQB for processing these microphone data samples.

As with the received trunking low speed data, low speed data is processed by the MCU and returned to the DSP at the DSP SCLK port connected to the MCU port PA0.

For secure messages, the analog signal may be passed to the secure module for encryption prior to further processing. The DSP transfers the data to and from the secure module through its SCI port consisting of TXD and RXD. Configuration and mode control of the secure module is performed by the MCU through the SPI bus.

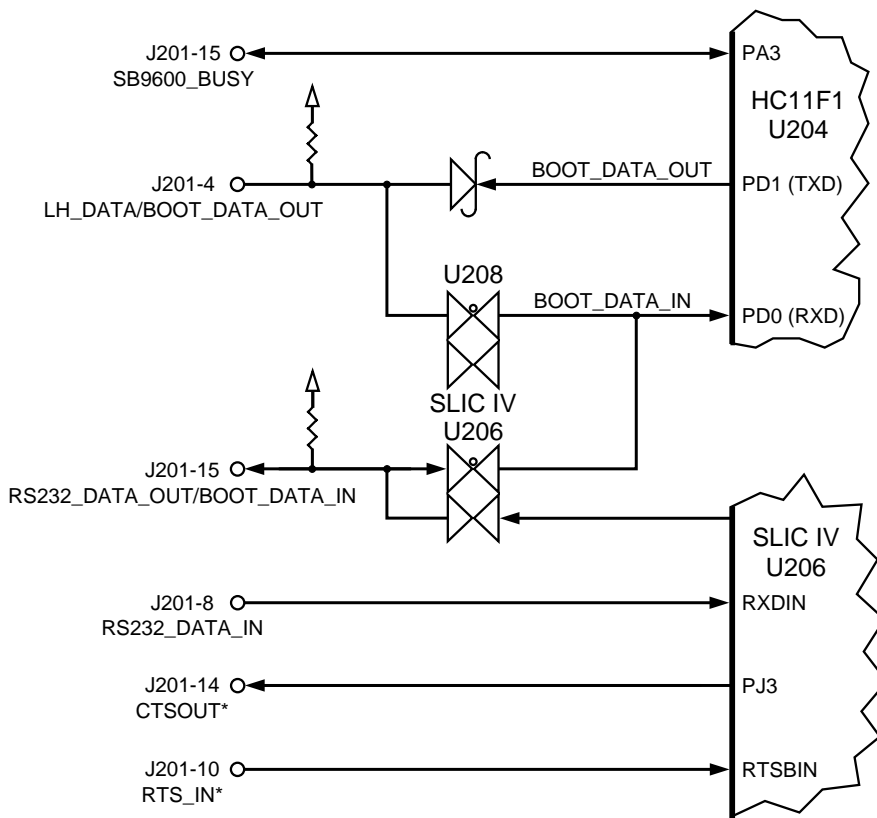
The DSP processes these microphone samples and generates and mixes the appropriate signaling and filters the resultant data. This data is then transferred to the ADSIC IC on the DSP SSI port. The transmit side of the SSI port consists of SC2, SCK, and STD. The DSP SSI port is a synchronous serial port. SCK is the 1.2MHz clock input derived from the ADSIC which makes it synchronous. The data is clocked over to the ADSIC on STD at a 1.2MHz rate. The ADSIC generates a 48kHz interrupt on SC2 so that a new sample data packet is transferred at a 48kHz rate and sets the transmit data sampling rate at 48Ksp. These samples are then input to a transmit D/A which converts the data to an analog waveform. This waveform is actually the modulation out signal from the ADSIC port VVO and is connected directly to the VCO. The transmit side of the transceiver is virtually identical to a standard analog FM radio.

Also required is the 2.4MHz ODC signal from the ABACUS IC. Although the ABACUS IC provides receiver functions it is important to note that this 2.4MHz reference is required for all of the ADSIC operations.

## Controller Bootstrap and Asynchronous Buses

The SB9600 bus is an asynchronous serial communications bus utilizing a Motorola proprietary protocol. Its purpose is a means for the MCU to communicate with other hardware devices. In the ASTRO Digital SABER radio, it communicates with hardware accessories connected to the universal connector.

The SB9600 bus utilizes the UART internal to the MCU operating at 9600 baud. The SB9600 bus consists of a LH\_DATA (J201-4) and SB9600\_BUSY (J201-6) signals. LH\_DATA is actually the SCI TXD and RXD ports (U204 - PD0 and PD1) tied together through the MUX U208 (see *Figure 8*). This makes the bus a simplex single-wire system. SB9600\_BUSY (U204 - PA3) is an active low signal, which is pulled low when a device wants control of the bus.



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*Figure 8 . Host SB9600 and RS232 Ports*

The same UART internal to the MCU is used in the controller bootstrap mode of operation. This mode is used primarily in downloading new program code to the FLASH ROMs on the VOCON board. In this mode, the MCU accepts special code downloaded at 7200 baud through the SCI bus instead of operating from program code resident in its ROMs. It however must operate in a two wire duplex configuration.

A voltage applied to J201-13 (Vpp) of greater than 10 Vdc will trip the circuit consisting of Q203, Q204, and VR207. This circuit sets the MODA and MODB pins of the MCU to bootstrap mode (logic 0,0) and configures the MUX, U208 to separate the RXD and TXD signals of the

MCU SCI port. Now if the Vpp voltage is raised to 12Vdc required on the FLASH devices for programming; the circuit comprised of VR208, Q211, and Q208 will trip supplying Vpp to the FLASH devices U205, U210, and U404. One more complication exists in that the BOOT\_DATA\_IN signal, RXD is multiplexed with the RS232 data out signal RS232\_DATA\_OUT. This multiplex occurs in the SLIC IV U206, which must also be properly configured.

The ASTRO Digital SABER radio has an additional asynchronous serial bus which utilizes RS232 bus protocol. This bus utilizes the UART in the SLIC IC (U206). It is comprised of RS232\_DATA\_OUT (15), RS232\_DATA\_IN (J201-8), CTSOUT\* (J201-14), and RTSIN\* (J201-10). It is a two wire duplex bus used to connect to external data devices.

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## Vocoder Bootstrap

The DSP has two modes of bootstrap; from program code stored in the FLASH ROM U404 or retrieving code from the host port.

During normal modes of operation, the DSP executes program code stored in the FLASH ROM U404. Unlike the MCU, however, the DSP moves the code from the FLASH ROM into the three SRAMs U402, U403, and U414 where it is executed from. Since at initial start-up, the DSP must execute this process before it can begin to execute system code, it is considered a bootstrap process. In this process, the DSP fetches 512 words, 1536 bytes, of code from the FLASH ROM starting at physical address 5C000 and moves it into internal P memory. This code contains the system vectors including the reset vector. It then executes this piece of bootstrap code which basically in turn moves additional code into the external SRAMs.

A second mode of bootstrap allows the DSP to load this initial 512 words of data from the host port, being supplied by the MCU. This mode is used for FLASH programming the DSP ROM when the ROM may initially be blank. In addition, this mode may be used for downloading some diagnostic software for evaluating that portion of the board.

The bootstrap mode for the DSP is controlled by three signals; MODA/IRQA\*, MODB/IRQB\*, and D23 (kit number NTN8250D), or MODC (kit numbers NTN8250E and NTN8250F). All three of these signals are on the DSP (U405). MODA and MODB configure the memory map of the DSP when the DSP reset become active. These two signals are controlled by the ADSIC (U406) during power-up, which sets MODA low and MODB high for proper configuration. Later these lines become interrupts for analog signal processing. D23/MODC controls whether the DSP will look for code from the MCU or will retrieve code from the FLASH ROM. D23 high, or MODC low out of reset, will cause the DSP to seek code from the FLASH ROM (U404). For the second mode of bootstrap, the MCU drives BOOTMODE low, causing D23 to go low and MODC to go high.

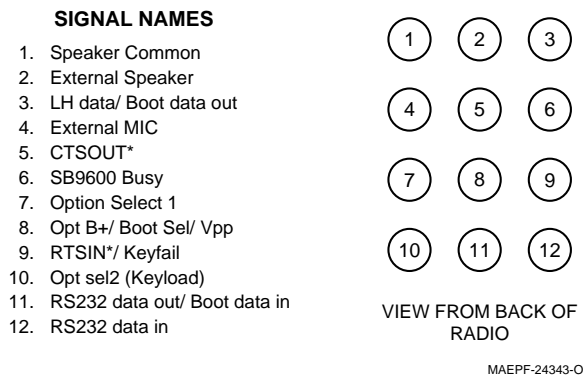
## SPI Bus Interface

This bus is a synchronous serial bus made up of a data, a clock, and an individual IC unique select line. Its primary purpose is to configure the operating state of each IC. ICs programmed by this include; display module, ADSIC, Fractional N Synthesizer, Pendulum Reference Oscillator, DAIC, and if equipped, the secure module.

The MCU (U204) is configured as the master of the bus. It provides the synchronous clock (SPI\_SCK), a select line, and data (MOSI [Master Out Slave In]). In general the appropriate select line is pulled low to enable the target IC and the data is clocked in. Actually the SPI bus is a duplex bus with the return data being clocked in on MISO (Master In Slave Out). The only place this is used is when communicating with the secure module. In this case, the return data is clocked back to the MCU on MISO (master in slave out).

## Universal Connector and Option Selects

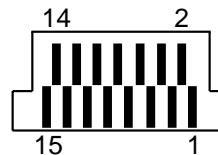
The universal connector is located on the back of the radio. It is the external port or interface to the outside and is used for programming and interfacing to external accessories. The signals are outlined in the following diagram. The universal connector connects to the VOCON board at J201 through a flex circuit routed down the back of the external housing. Connections to the universal connector and J201 on the VOCON board are shown in *Figure 9* and *Figure 10*.



*Figure 9 . Universal Connector*

### VOCON BOARD CONNECTOR

J201-1	N.C
J201-2	N.C.
J201-3	N.C.
J201-4	LH_DATA/BOOT_DATA_OUT
J201-5	Ext Mic
J201-6	SB9600_BUSY
J201-7	Option Select 1
J201-8	RS232_DATA_IN
J201-9	Option Sel 2 (Keyload*)
J201-10	RTSIN*/KEYFAIL*
J201-11	Speaker Common
J201-12	External Speaker
J201-13	OPTB+/Boot Sel/Vpp
J201-14	CTSOUT*
J201-15	RS232 Data Out/ Boot Data In



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*Figure 10 . VOCON Board Connector - J201*

Most of the signals are extensions of circuits described in other areas of this manual. However there are two option select pins used to configure special modes; Option Select 1 and Option Select 2. These pins are controlled by accessories connected to the universal connector. The following table outlines their functions as defined at the universal connector:

*Table 1 . Option Select Functions*

	Opt Sel 1	Opt Sel 2
Keyload	1	0
No Function	1	1
External PTT	0	1

---

## Keypad and Display Module

The front cover assembly contains the internal speaker, and internal microphone. An optional integral 2 line by 14 character LCD display is available with either a 3 x 2 keypad or 3 x 6 keypad. This unit is not considered field repairable.

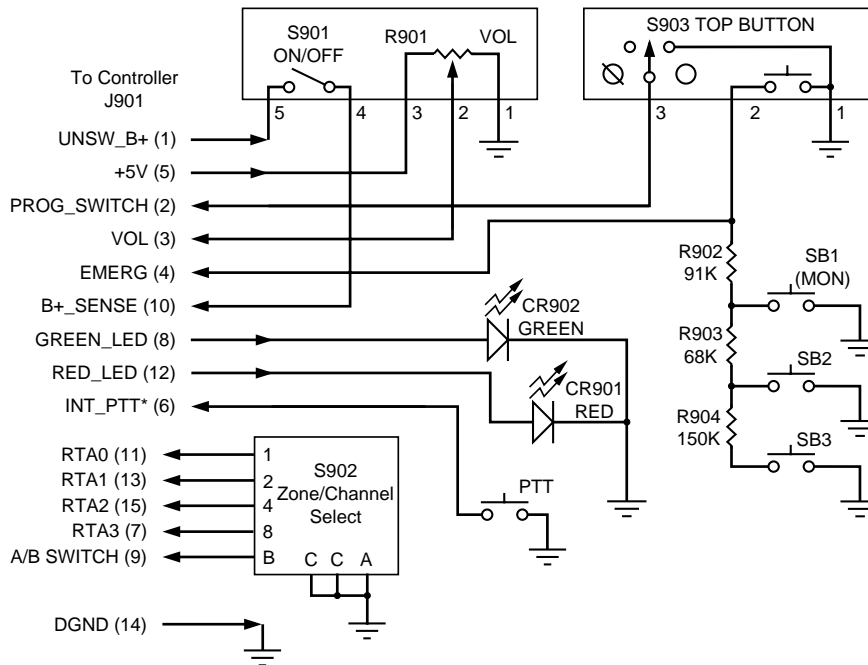
The internal speaker and microphone are connected to the VOCON connector J701 through a flex circuit. This flex circuit along with J701 also contain the keypad control lines. The keypad is read through a row and column matrix made up of ROW1, ROW2, ROW3, ROW4, ROW5, ROW6, and COL1, COL2, and COL3. These signals are input to I/O ports on the SLIC (U206) and individually pulled to a high state through resistors. When a key is pressed the respective signals for a single row and a single column are set to logic zero. The MCU reads these ports through the SLIC parallel registers, provides for key debounce, and determines which key has been pressed.

The display is controlled by the MCU which programs the display through the SPI bus, DISP\_EN\* (select) and DISP\_RST\*. In addition display backlighting is provided by two white LEDs controlled by the BL\_EN signal. SW\_B+ routed to the display is used to power these LEDs. All other circuitry on the display is powered by 5Vdc provided by the VOCON board. The display is connected to the VOCON board at J601 through a separate flex circuit.



## Controls and Control Top Flex

The control top controls include an on/off switch, volume, 16 position mode select switch with two position toggle, and ergo code/clear mode switch. The side controls include three momentary push button switches (monitor, RAT1, RAT2) and PTT. These components are connected through a flex circuit to the controller at J901, see *Figure 11*.



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*Figure 11 . Control Top Flex*

UNSW\_B+ is routed through S901 to provide the B+\_SENSE signal which provides radio power control. Refer to the power distribution section for further details.

Volume control is provided by R901 which is a potentiometer biased between +5Vdc and ground. The VOL signal is a voltage level between +5Vdc and 0Vdc dependent on the position of the rotary knob. VOL is an input to an A/D port on the MCU (U204). The MCU sends the appropriate message to the DSP to adjust speaker volume based on this setting.

Switch S903 is the two-position programmable switch typically used for code or clear mode selection. It is an input to a control I/O with a pull up resistor so the logic defaults high. Selecting clear mode pulls this signal to a logic low. Appropriate operation is configured by the MCU. In addition, this switch contains an additional momentary button typically used for emergency. This button is connected along with the PTT, and programmable side buttons on a resistor divider network biased between +5Vdc and ground. This network made up of R902, R903, and R904 provides a voltage level to an A/D port on the MCU dependent on which button is pressed. The MCU determines which button is pressed based on the value at the A/D port.

S902 is a binary coded switch. The output pins from this switch are connected to I/O ports on the controller. It provides a 4 bit binary word to the MCU indicating which of the 16 positions the rotary is set to. This switch provides an additional output, A/B\_SWITCH, which effectively doubles its range by providing decoding for two sets of 16 positions. A/B\_SWITCH is also read by the MCU on an I/O port.

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## Controller Memory Map

*Figure 12* depicts the controller section memory map for the parallel data bus as used in normal modes of operation. There are three maps available for normal operation, but map 2 is the only one used. In bootstrap mode, the mapping is slightly different and will be addressed later.

The external bus for the host controller (U204) consists of one 32Kx8 SRAM (U202), one 32Kx8 EEPROM (U201), two 256Kx8 FLASH ROMs (U205, U210), and SLIC (U206) configuration registers. In addition the DSP host port is mapped into this bus through the SLIC address space. The purpose of this bus is to interface the MCU (U204) to these devices.

The MCU executes program code stored in the FLASH ROMs. On a power-up reset, it fetches a vector from \$FFFE, \$FFFF in the ROMs and begins to execute code stored at this location. The external SRAM along with the internal 1Kx8 SRAM is used for temporary variable storage and stack space. The internal 512 bytes of EEPROM along with the external EEPROM are used for non volatile storage of customer specific information. More specifically the internal EEPROM space contains transceiver board tuning information and on power-down some radio state information is stored in the external EEPROM.

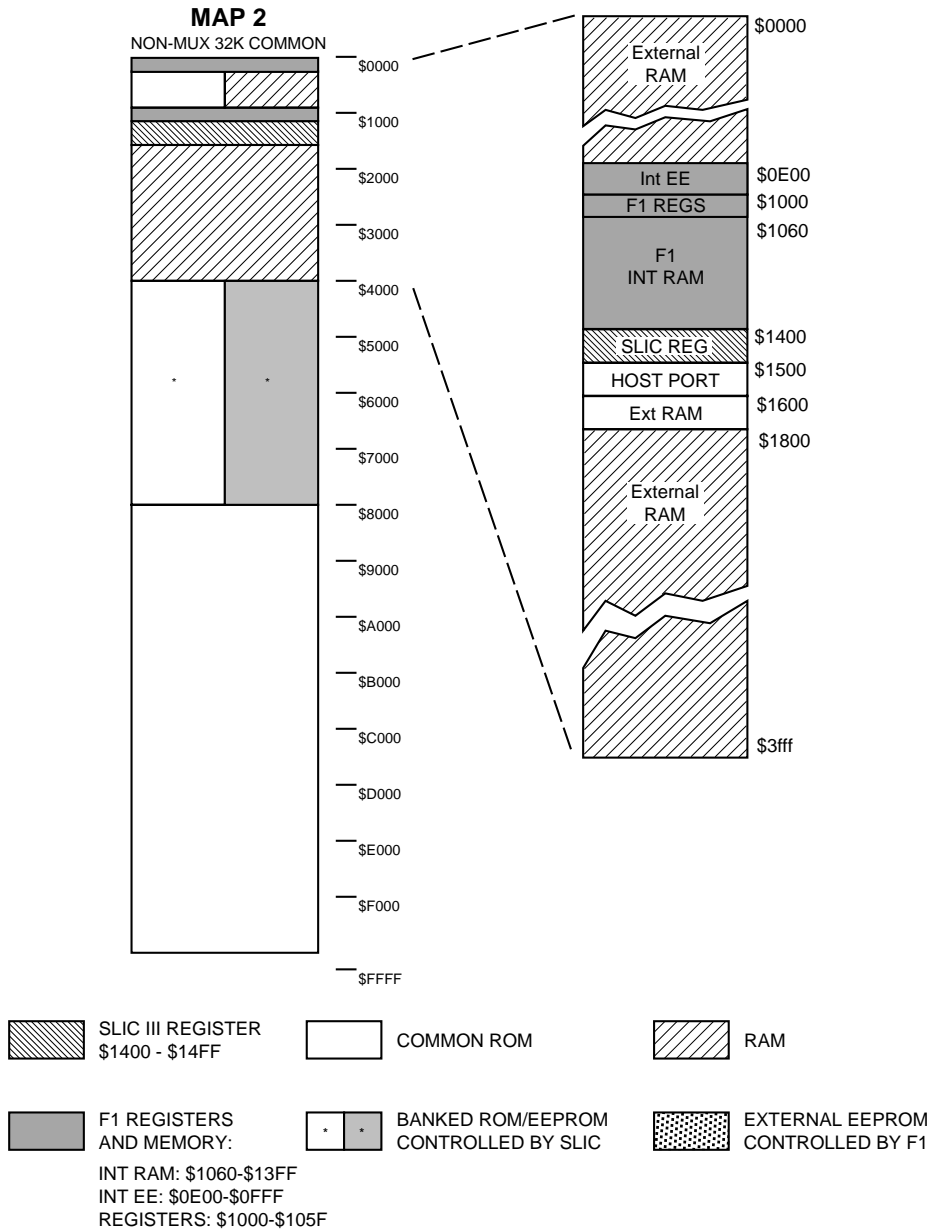
The SLIC is controlled through sixteen registers mapped into the MCU memory at \$1400 - \$14FF. This mapping is achieved by the following signals from the MCU: R/W\*, CSIO1\*, HA0-HA4, HA8, HA9. Upon power-up, the MCU configures the SLIC including the memory map by writing to these registers.

The SLIC memory management functions in conjunction with the chip selects provided by the MCU provide the decoding logic for the memory map which is dependent upon the “map” selected in the SLIC. The MCU provides a chip select, CSGEN\*, which decodes the valid range for the external SRAM. In addition CSIO1\* and CSProg\* are provide to the SLIC decoding logic for the external EEPROM and FLASH ROM respectively. The SLIC provides a chip select and banking scheme for the EEPROM and FLASH ROM. The FLASH ROM is banked into the map in 16KB blocks with one 32KB common ROM block. The external EEPROM may be swapped into one of the banked ROM areas. This is all controlled by EE1CS\*, ROM1CS\*, ROM2CS\*, HA14\_OUT, HA15\_OUT, HA16, and HA17 from the SLIC (U206) and D0-D8 and A0-16 from the MCU (U204).

The SLIC provides three peripheral chip selects; XTSC1B, XTCS2B, and XTCS3B. These can be configure to drive an external chip select when it's range of memory is addressed. XTSC1B is used to address the host port interface to the DSP. XTSC2B is used to address a small portion of

external SRAM through the gate U211. XTSCB3 is used as general purpose I/O for interrupting the secure module.

In bootstrap mode the memory map is slightly different. Internal EEPROM is mapped at \$FE00-\$FFFF and F1 internal SRAM starts at \$0000-\$03FF. In addition a special bootstrap ROM appears in the ROM space from \$B600-\$BFFF. For additional information on bootstrap mode refer to the section Controller Bootstrap and Asynchronous Buses.



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Figure 12 . Controller Memory Mapping

The SLIC is controlled through sixteen registers mapped into the MCU memory at \$1400 - \$14FF. This mapping is achieved by the following signals from the MCU: R/W\*, CSIO1\*, HA0-HA4, HA8, HA9. Upon power-up, the MCU configures the SLIC including the memory map by writing to these registers.

The SLIC memory management functions in conjunction with the chip selects provided by the MCU provide the decoding logic for the memory map which is dependent upon the “map” selected in the SLIC. The MCU provides a chip select, CSGEN\*, which decodes the valid range for the external SRAM. In addition CSIO1\* and CSProg\* are provide to the SLIC decoding logic for the external EEPROM and FLASH ROM respectively. The SLIC provides a chip select and banking scheme for the EEPROM and FLASH ROM. The FLASH ROM is banked into the map in 16KB blocks with one 32KB common ROM block. The external EEPROM may be swapped into one of the banked ROM areas. This is all controlled by EE1CS\*, ROM1CS\*, ROM2CS\*, HA14\_OUT, HA15\_OUT, HA16, and HA17 from the SLIC (U206) and D0-D8 and A0-16 from the MCU (U204).

The SLIC provides three peripheral chip selects; XTSC1B, XTCS2B, and XTCS3B. These can be configure to drive an external chip select when it's range of memory is addressed. XTSC1B is used to address the host port interface to the DSP. XTSC2B is used to address a small portion of external SRAM through the gate U211. XTSCB3 is used as general purpose I/O for interrupting the secure module.

In bootstrap mode the memory map is slightly different. Internal EEPROM is mapped at \$Fe00-\$FFFF and F1 internal SRAM starts at \$0000-\$03fff. In addition a special bootstrap ROM appears in the ROM space from \$B600-\$BFFF. For additional information on bootstrap mode refer to the section Controller Bootstrap and Asynchronous Buses.

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## Vocoder Memory Map

The vocoder (DSP) external bus consists of three 8k x 24 SRAMs (U402, U403, U414), one 256k x 8 FLASH ROM (U404), and ADSIC (U406) configuration registers.

The DSP56001 (U405) has a 24 bit wide data bus (D0-D23) and a 16 bit wide address bus (A0 - A15). The DSP can address three 64k x 24 memory spaces: P (Program), Dx (Data X), and Dy (Data Y). These additional RAM spaces are decoded using PS\* (Program Strobe), DS\* (Data Strobe), and X/Y\*. RD\* and WR\* are separate read and write strobes.

The ADSIC provides additional memory decoding logic for the RAMs in the form of RSEL\* used in decoding U403. RSEL\* provides the logic  $A_{13} \times A_{14}$ . U415 provides logic in the form of  $A_{13} + A_{14}$  for decoding U414. RSEL\* logic is programmed by the MCU through the SPI bus interface.

The ADSIC also provides memory decoding for the FLASH ROM (U404). EPS\* provides the logic  $A_{15} \times (A_{14} \approx A_{13})$  and is use as a select for the ROM. The ADSIC provide three bank lines for selecting 16k byte banks from the ROM. This provides decoding for 128K bytes from

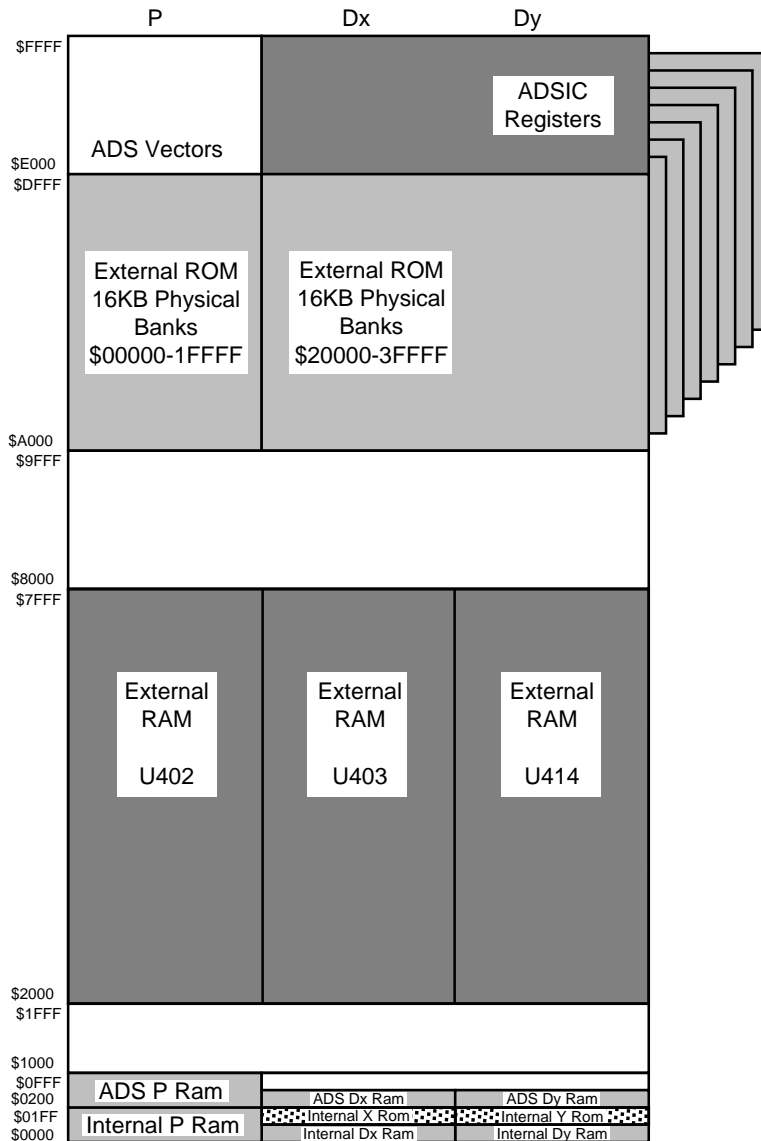


Figure 13. Vocoder Memory Mapping

the ROM in the P: memory space. PS\* is used to select A17 to provide an additional 128k bytes of space in Dx: memory space for the ROM.

The ADSIC internal registers are decoded internally and start at \$E000 in Dy:.. These registers are decoded using A0-A2, A13-15, and PS\* from the DSP. The ADSIC internal registers are 16 bit wide so only D8-D23 are used.

The DSP program code is stored in the FLASH ROM U404. During normal modes of operation, the DSP moves the appropriate program code into the three SRAMs U402, U403, and U414 and internal RAM for execution. The DSP never executes program code from the FLASH ROM itself. At power-up after reset, the DSP downloads 512 words (1536 bytes) from the ROM starting at \$C000 and puts it into the internal RAM starting at \$0000 where it is executed. This segment of

program code contains the interrupt vectors and the reset vector and is basically an expanded bootstrap code. When the MCU messages the DSP that the ADSIC has been configured, the DSP overlays more code from the ROM into external SRAM and begins to execute it. Overlays occur at different times when the DSP moves code from the ROM into external SRAM depending on immediate mode of operation, such as changing from transmit to receive.

---

## MCU System Clock

The MCU (U204) system clock is provided by circuitry internal to the MCU and is based on the crystal reference, Y201. The nominal operating frequency is 7.3728MHz. This signal is available as a clock at 4XECLK on U204 and is provided to the SLIC (U206) for internal clock timing. The MCU actually operates at a clock rate of 1/4 the crystal reference frequency or 1.8432MHz. This clock is available at ECLK on U204.

The MCU clock contains a crystal warp circuit comprised of L201, Q205, and C228. This circuit is controlled by an I/O port (PA6) on the MCU. This circuit moves the operating frequency of the oscillator about 250ppM on certain receive channels to prevent interference from the MCU bus noise.

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## DSP System Clock

The DSP (U405) system clock, DCLK, is provided by the ADSIC (U406). It is based off the crystal reference, Y401, with a nominal operating frequency of 33.0000MHz. ADSIC contains an internal clock divider circuit which can divide the system clock from 33MHz to 16.5 or 8.25MHz operation. The DSP controls this divider by writing to the ADSIC parallel registers. This frequency is determined by the processes the DSP is running and is generally configured to the slowest operating speed possible to reduce system power consumption.

The additional circuitry of CR402, L403, C459, C467, C491, and C490 make up a crystal warp circuit. This circuit is controlled by the OSCw signal from ADSIC which is configured by the host through the SPI bus. This circuit moves the operating frequency of the oscillator about 400ppM on certain receive channels to prevent interference from the DSP bus noise.

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## Radio Power-Up/ Power-Down Sequence

Radio power-up begins when the user closes the radio on/off switch on the control top. This enables 7.5Vdc on the B+\_SENSE signal. This signal enables the pass element Q207 through Q206 enabling SW\_B+ to the VOCON board and transceiver board. B+\_SENSE also enables the +5Vdc regulator U409. When +5Vdc has been established, it is sensed by the supervisory IC U407. U407 disables the system reset through the delay circuit R481 and C482.

When the MCU comes out of reset, it fetches the reset vector in ROM at \$FFFE, \$FFFF and begins to execute the code this vector points to. It configures the SLIC through the parallel bus registers. Among other things it enables the correct memory map for the MCU. It configures all the transceiver devices on the SPI bus. The MCU then pulls the ADSIC out of reset and after a minimal delay the DSP also. It then configures the ADSIC through the SPI bus configuring among other

things, the DSP memory map. While this is happening, the DSP is fetching code from the ROM U404 into internal RAM and beginning to execute it. It then waits for a message from the MCU that the ADSIC has been configured, before going on.

During this process, the MCU does power diagnostics. These diagnostics include verifying the MCU system RAM and verifying the data stored in the internal EEPROM, external EEPROM, and FLASH ROMs. The MCU queries the DSP for proper status and the results of DSP self tests. The DSP self tests include testing the system RAM, verifying the program code in ROM U404, and returning the ADSIC configuration register checksum. Any failures cause the appropriate error codes to be sent to the display. If everything is OK, the appropriate radio state is configured and the unit waits for user input.

On power-down, the user opens the radio on/off switch removing the B+\_SENSE signal from the VOCON board. This does not immediately remove power as the MCU holds this line active through B+\_CNTL. The MCU then saves pertinent radio status data to the external EEPROM. Once this is done, B+\_CNTL is released shutting off SW\_B+ at Q207 and shutting down the 5Vdc regulator U409. When the regulator slumps to about 4.6Vdc, the supervisory IC U407 activates a system reset to the SLIC which in turn resets the MCU.

# Secure Modules




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## Introduction

The secure modules are designed to digitally encrypt and decrypt voice and ASTRO data in ASTRO SABER™ radios. This section covers the following secure modules:

- NTN7770
- NTN7771
- NTN7772
- NTN7773
- NTN7774
- NTN7329
- NTN7332
- NTN7331
- NTN3330
- NTN7370
- NTN1146
- NTN1152
- NTN1153
- NTN1158
- NTN1147
- NTN1367
- NTN1368
- NTN1369
- NTN1370
- NTN1371
- NTN8967

*NOTE:* The secure modules are NOT serviceable. The information contained in this chapter is only meant to help determine whether a problem is due to a secure module or the radio itself.

The secure module uses a custom encryption integrated circuit (IC) and an encryption key variable to perform its encode/decode function. The encryption key variable is loaded into the secure module, via the radio’s universal (side) connector, from a hand-held, key variable loader (KVL). The encryption IC corresponds to the particular encryption algorithm purchased. The encryption algorithms and their corresponding kit numbers are:

KITS:		TANAPAS:	
DVP	NTN7770	DVP	NTN1146
DES	NTN7771	DES	NTN1152
DES-XL	NTN7772	DES-XL	NTN1153
DVI-XL	NTN7773	DVI-XL	NTN1158
DVP-XL	NTN7774	DVP-XL	NTN1147
DVI-XL & DVP	NTN7329	DVI-XL & DVP	NTN1367
DES-XL & DVP	NTN7332	DES-XL & DVP	NTN1368
DES-XL & DVP-XL	NTN7731	DES-XL & DVP-XL	NTN1369
DVP & DVP-XL	NTN7330	DVP & DVP-XL	NTN1370
DVP-XL & DVI-XL	NTN7370	DVP-XL & DVI-XL	NTN1371
All, except DVP	NTN8967		



---

## Circuit Description

The secure module operates from three power supplies (UNSW\_B+, SW\_B+, and +5V). The +5V and the SW\_B+ are turned on and off by the radio's on/off switch. The UNSW\_B+ provides power to the secure module as long as the radio battery is in place.

Key variables are loaded into the secure module through connector J601, pin 15. Up to 16 keys (depending on the type of encryption module) can be stored in the module at a time. The key can be infinite key retention or 30-seconds key retention, depending on how the code plug is setup.

The radio's host processor communicates with the Secure Module on the Serial Peripheral Interface (SPI) bus. The host processor is the master on this bus, while the secure module is a slave on the bus. The SPI bus consists of five signal lines. Refer to Table 1 for signal information. A communications failure between the host processor and the secure module will be indicated as an "ERROR 09/10" message on the radio display.

---

## Troubleshooting Secure Operations

Refer to the Basic Service Manual, Motorola publication number 68P81076C05 for disassembly and reassembly information. A key variable loader (KVL) and oscilloscope are needed to troubleshoot the secure module.

*NOTE:* The secure module itself is not serviceable. If the secure module is found to be defective, it must be replaced.

## Error 09/10, Error 09/90

The ASTRO Digital XTS 3000 radio automatically performs a self test on every power-up. Should the radio fail the self tests, the display will show "ERROR 09/10" or "ERROR 09/90" accompanied by a short beep. If the display shows "ERROR 09/10" or "ERROR 09/90," the radio failed the secure power-up tests and the host microcontroller was unable to communicate with the secure module via the SPI bus. Turn the radio off and back on. If the radio still does not pass the self tests, then a problem exists with the secure operations of the radio.

Troubleshooting information for "ERROR 09/10" is found in Troubleshooting Charts.

## Keyload

When the keyloading cable is attached to the ASTRO Digital XTS 3000 radio and "KEYLOADING" is not displayed on the radio's display, then the radio has not gone into KEYLOAD mode. For troubleshooting "KEYLOAD" failure, refer to Troubleshooting Chart, "Key Load Fail."

*NOTE:* ASTRO Digital SABER radios need a keyloader that has the ability to keyload an ASTRO Digital SABER radio. The keyloader must be either a "T - - - CX" or a "T - - - - DX" keyloader.

# Troubleshooting Procedures

# 9

---

## Introduction

The purpose of this section is to aid in troubleshooting a malfunctioning ASTRO Digital SABER radio. It is intended to be detailed enough to localize the malfunctioning circuit and isolate the defective component.



### Caution

Most of the ICs are static sensitive devices. Do not attempt to troubleshoot or disassemble a board without first referring to the following Handling Precautions section.

---

## Handling Precautions

Complementary metal-oxide semiconductor (CMOS) devices, and other high-technology devices, are used in this family of radios. While the attributes of these devices are many, their characteristics make them susceptible to damage by electrostatic discharge (ESD) or high-voltage charges. Damage can be latent, resulting in failures occurring weeks or months later. Therefore, special precautions must be taken to prevent device damage during disassembly, troubleshooting, and repair. Handling precautions are mandatory for this radio, and are especially important in low-humidity conditions. **DO NOT** attempt to disassemble the radio without observing the following handling precautions.

1. Eliminate static generators (plastics, Styrofoam, etc.) in the work area.
2. Remove nylon or double-knit polyester jackets, roll up long sleeves, and remove or tie back loose hanging neckties.
3. Store and transport all static-sensitive devices in ESD-protective containers.
4. Disconnect all power from the unit before ESD- sensitive components are removed or inserted unless otherwise noted.
5. Use a static-safeguarded workstation, which can be accomplished through the use of an anti-static kit (Motorola part number 01-80386A82). This kit includes a wrist strap, two ground cords, a static-control table mat and a static-control floor mat. For additional information, refer to Service and Repair Note SRN-F1052, "Static Control

Equipment for Servicing ESD Sensitive Products,” available from Literature Distribution.

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Literature Distribution  
2290 Hammond Drive  
Schaumburg, IL 60173  
(708) 576-2826

6. Always wear a conductive wrist strap when servicing this equipment. The Motorola part number for a replacement wrist strap that connects to the table mat is 42-80385A59.

---

## Voltage Measurement and Signal Tracing

It is always a good idea to check the battery voltage under load. This can be done by measuring the OPT\_B+ pin at the universal connector on the back of the radio, with the radio keyed. The battery voltage should remain at or above 7.0Vdc. The battery should be recharged or replaced as necessary prior to analyzing the radio.

In most situations, the problem circuit may be identified using a dc voltmeter, RF millivoltmeter, and oscilloscope (preferably with 100MHz bandwidth or more). The “Recommended Test Equipment, Service Aids, and Tools” section in the ASTRO Digital SABER Portable Radios Basic Service Manual outlines the recommended tools and service aids which would be useful. Of special note is the REX-4200A Housing Eliminator, which allows the technician to open the radio to probe points while in operation.

In some cases dc voltages at probe points are shown in red on the schematics. In other areas diagrams are included to show time varying signals which should be present under the indicated circumstances. It is recommended that a thorough check be made prior to replacement of any IC or part. If the probe point does not have a signal reasonably close to the indicated one, a check of the surrounding components should be made prior to replacing any parts.



### Caution

When checking a transistor or module, either in or out of circuit, do not use an ohmmeter having more than 1.5 volts dc appearing across test leads or use an ohms scale of less than x100.

## Power-Up Self-Check Errors

Each time the radio is turned on the MCU and DSP perform some internal diagnostics. These diagnostics consist of checking the programmable devices such as the FLASH ROMs, internal and external EEPROMs, SRAM devices, and ADSIC configuration bus checksum. At the end of the power-up self-check routines, if an error exists, the appropriate error code is displayed on the display. For non-display radios, the error codes may be read using the Radio Service Software (RSS) from the SB9600 bus on the universal connector. The following lists valid checksums, the related failure, and a reference section for investigating the cause of the failure.

Error Code	Description	Page
01/81	Chart 6. 01/81 Host ROM Checksum Failure . . . .	10-5
01/82	Chart 7. 01/82 or 002, External EEPROM Checksum Failure. . . . .	10-6
01/84	Chart 8. 01/84 SLIC Initialization Failure . . . . .	10-6
01/88	Chart 9. 01/88 MCU (Host $\mu$ C) External SRAM Failure . . . . .	10-7
01/92	Chart 10. 01/92, Internal EEPROM Checksum Failure. . . . .	10-7
02/A0	Chart 11. 02/A0, ADSIC Checksum Failure . . . . .	10-8
02/81	Chart 12. 02/81, DSP ROM Checksum Failure . . . .	10-8
02/88	Chart 13. 02/88, DSP External SRAM Failure U414.	10-9
02/84	Chart 14. 02/84, DSP External SRAM Failure U403.	10-9
02/82	Chart 15. 02/82, DSP External SRAM Failure U402	10-10
02/90	Chart 16. 02/90, General DSP Hardware Failure . .	10-10
09/10	Chart 17. 09/10, Secure Hardware Failure . . . . .	10-11
09/90	Chart 18. 09/90, Secure Hardware Failure . . . . .	10-11
001	Chart 31. VHF/UHF Frequency Generation Unit (FGU) . . . . .	10-19
001	Chart 32. 800MHz Frequency Generation Unit (FGU) . . . . .	10-20
002	Chart 7. 01/82 or 002, External EEPROM Checksum Failure. . . . .	10-6

In the case of multiple errors, the codes are logically OR'd and the results displayed. As an example, in the case of an ADSIC checksum failure and a DSP ROM checksum failure, the resultant code would be 02/A1. Following is a series of troubleshooting flowcharts which relate to each of these failure codes.

## Power-Up Sequence

Upon RESET\* going active, the MCU begins to execute code which is pointed to by the vector stored at \$FFFE, \$FFFF in the FLASH ROM. The execution of this code is as follows:

1. Initialize the MCU (U204). Green LED on.
2. Initialize the SLIC (U206).
3. CONFIG register check. If the CONFIG register is not correct, the MCU will repair it and loop.
4. Start ADSIC/DSP:
  - Bring the ADSIC reset line high.
  - Wait 2ms.
  - Bring the DSP reset line high.

5. Start EMC:
  - Set the EMC wake-up line low (emc irq line).
  - Wait 5ms.
  - Set the EMC wake-up line high.
  - Wait 10ms.
  - Set the EMC wake-up line low (emc irq line).
  - Wait 5ms.
  - Set the EMC wake-up line high.
6. Begin power-up self-tests.
7. Begin RAM tests:
  - External RAM (\$1800-3FFF).
  - Internal RAM (\$1060-\$1300).
  - External RAM (\$0000-\$0DFF).
  - Display 01/88 if failure.

The radio will get stuck here if the internal RAM is defective. The radio uses the internal RAM for stack. The RAM routines use subroutines. Thus, if the internal RAM is defective, the radio will get lost testing the external RAM.

8. Display "Self Test" (these routines use subroutines too). It is almost impossible to display an error message if the internal RAM is defective.
9. Begin MCU (host  $\mu$ C) ROM checksum test.
  - Fail 01/81 if this routine fails.
10. Begin DSP power-up tests. The MCU will try this five times before it fails the DSP test.
  - Check for HF2.
    - Fail 02/90 if 100ms.
  - Program the ADSIC.
  - Wait for the DSP power-up message.
    - Fail 02/90 if 300ms.
    - Fail 02/90 if wrong message from the DSP.
  - Wait for the DSP status information.
    - Fail 02/90 if 100ms.
    - Fail 02/88 if DSP RAM (U414) fails.
    - Fail 02/84 if DSP RAM U403 fails.
    - Fail 02/82 if DSP RAM U402 fails.

- Fail 02/81 if DSP RAM fails.
- Wait for the ADSIC checksum.
  - Fail 02/90 if 100ms.
  - Fail 02/90 if failure.
- Wait for the first part of the DSP version number.
  - Fail 02/90 if 100ms.
- Wait for the second part of the DSP version number.
  - Fail 02/90 if 100ms.
- 11. Display errors if a fatal error exists at this point.
- 12. Checksum the codeplug.
  - Test internal codeplug checksums.
    - Fail 01/92 if failure.
  - Test external codeplug checksums.
    - Error 01/82 if non-fatal error; fail 01/82 if fatal error.
- 13. Power-up the EMC (if it is enabled in the codeplug).
- 14. Turn off the green LED.
- 15. Start up operating system.

## Standard Bias Table

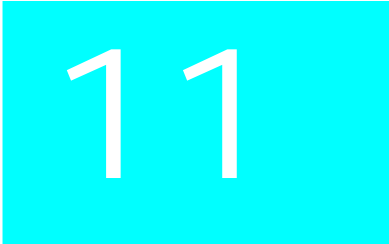
Table 3, below, outlines some standard supply voltages and system clocks which should be present under normal operation. These should be checked as a first step to any troubleshooting procedure.

*Table 2 . Standard Operating Bias*

Signal Name	Nominal Value	Tolerance	Source
UNSW_B+	7.5Vdc	6.0-9.0Vdc	J401
SW_B+	7.5Vdc	6.0-9.0Vdc	Q207
+5V	5.0Vdc	±10%	U409
+5VA	5.0Vdc	±10%	U410
RESET	5.0Vdc	+0.7, - 1.0Vdc	U407
POR*	5.0Vdc	+0.7, - 1.0Vdc	U206
DSP_RST*	5.0Vdc	+0.7, -1.0Vdc	U204
ADSIC_RST*	5.0Vdc	+0.7, -1.0Vdc	U204
DCLK	33.0000MHz <sup>a</sup>	±500ppM	U406
ODC	2.4MHz	±30ppM	ABACUS
ECLK	1.8432MHz	±500ppM	U204
IRQB*	8kHz <sup>b</sup>	±500ppM	U406
+5V	5.0Vdc	±10%	U202
RX_5V <sup>c</sup>	5.0Vdc	±10%	U106

- a. This is number may vary due to the operating mode of the radio when it is measured. The ADSIC contains a divider which may divide the clock by a modulus of 2. Therefore the actual frequency measured may be  $\text{clock}/2^N$ . The most common frequency will be 16.5000MHz nominal.
- b. This 8kHz clock will be present only after the MCU has successfully programmed the ADSIC after power-up. This is a good indication that the ADSIC is at least marginally operational.
- c. Receive mode only.

# Troubleshooting Waveforms



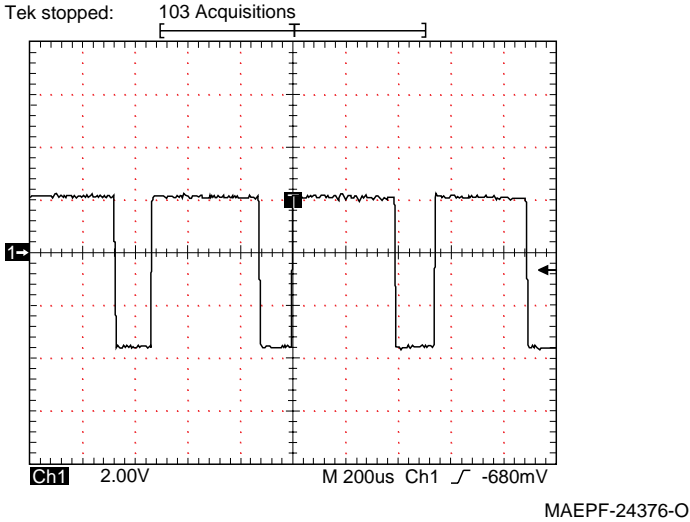
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## Introduction

This section contains images of waveforms which may be useful in verifying operation of certain parts of the circuitry. These waveforms are for reference only; the actual data depicted will vary depending upon operating conditions.

---

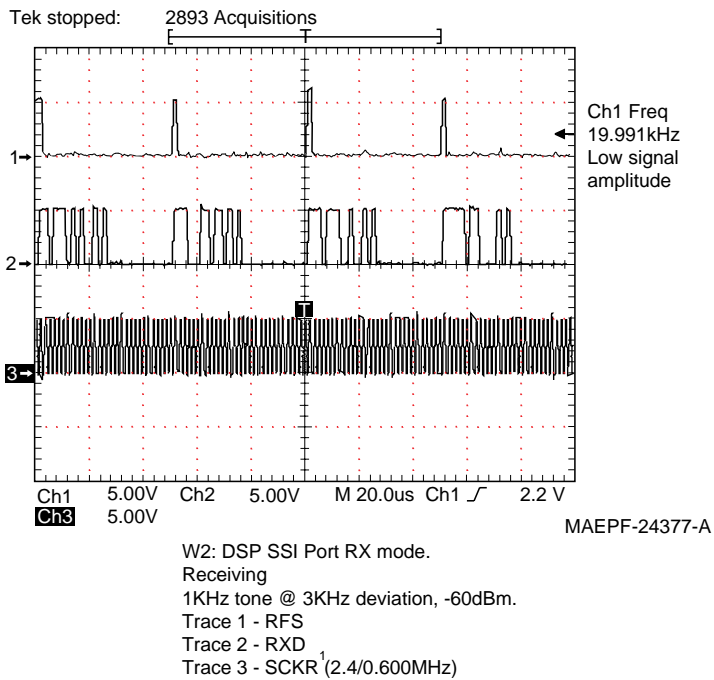
## Waveforms



W1: Switched Regulator Clock Out  
Trace 1 - (U409)LX measured with radio in standby mode with UNSW\_B+ at 7.5VDC.

*Figure 14 . Waveform W1*





Note 1: Typically SCKR is a 2.4 MHz clock. In low power modes, as shown here, SCKR is 600KHz.

Figure 15 . Waveform W2

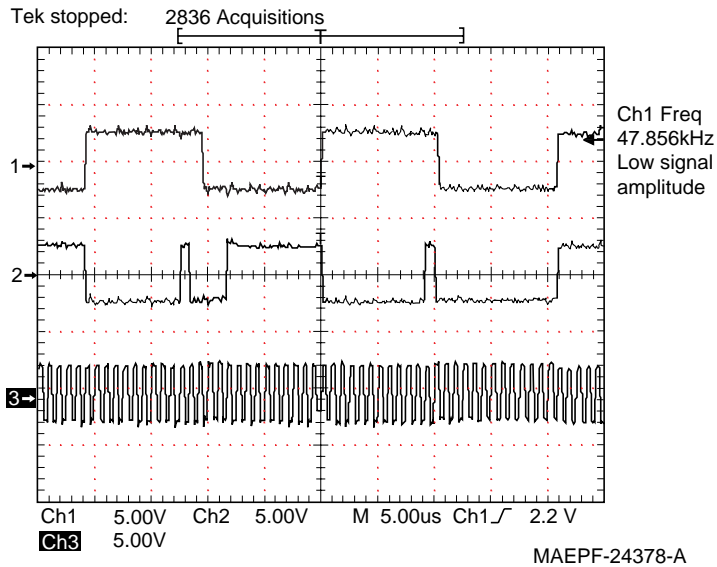
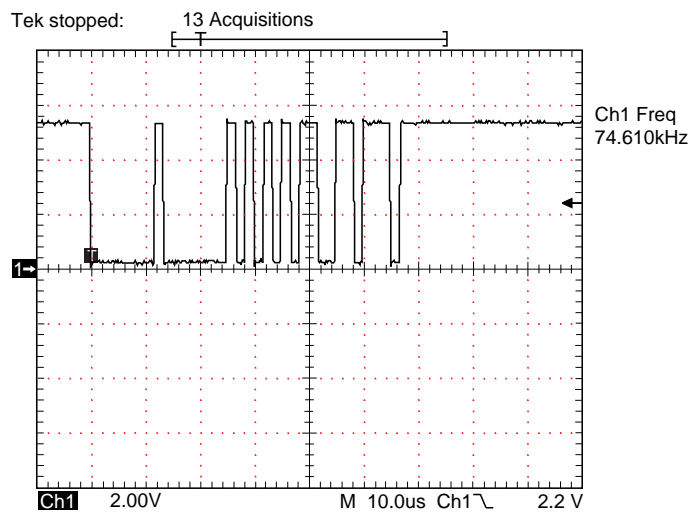


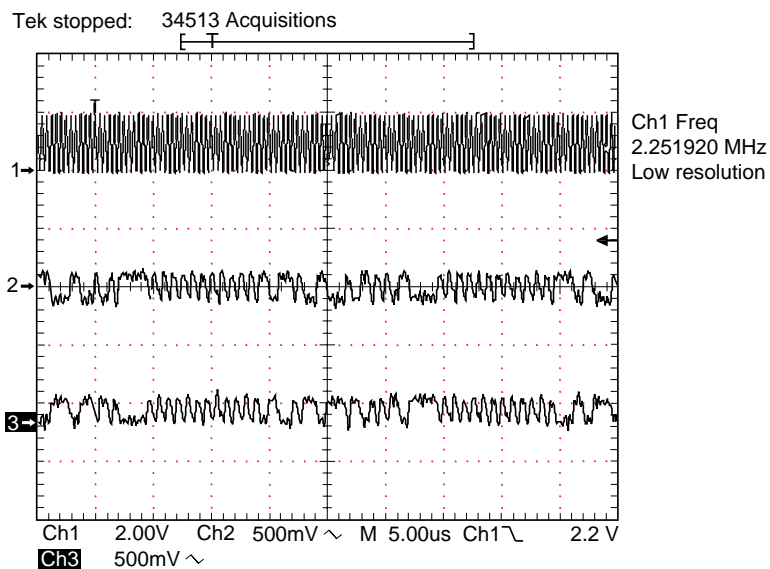
Figure 16 . Waveform W3



W4: ABACUS programming captured during mode change.  
Trace 1 - (ADSIC) SBI

MAEPF-24379-O

Figure 17. Waveform W4

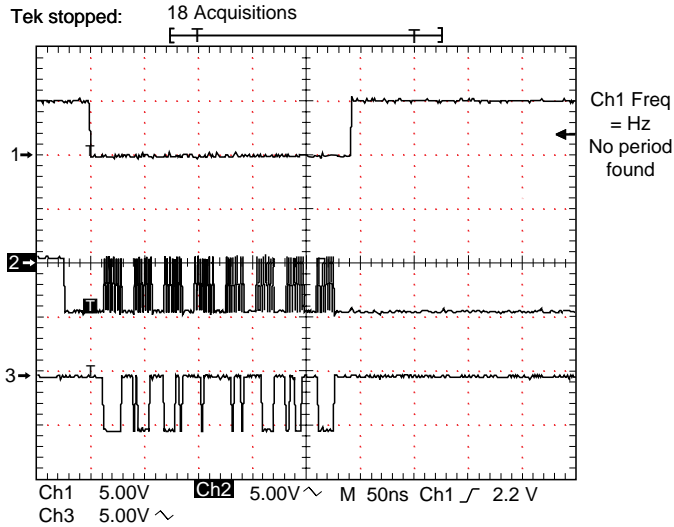


W5: ABACUS/ADSIC Interface.  
Receiving 1KHz tone @ 3KHz deviation, -60dbm.  
Trace 1 -IDC (2.4MHz)  
Trace 2 - DOUT<sup>2</sup>  
TRACE 3 - DOUT\*

MAEPF-24380-A

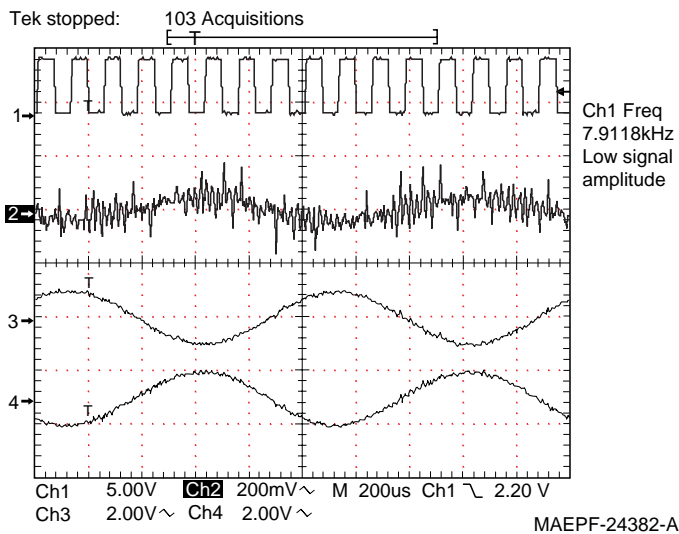
Note 2: Since these signals are a differential current loop these voltages are very low.

Figure 18. Waveform W5



W6: SPI Bus Programming ADSIC. MAEPF-24381-A  
 Trace 1 - ADSIC\_SEL\*  
 Trace 2 - SPL\_SCK  
 Trace 3 - MOSI  
 Note: These waveforms are typical to any device on the SPI bus.

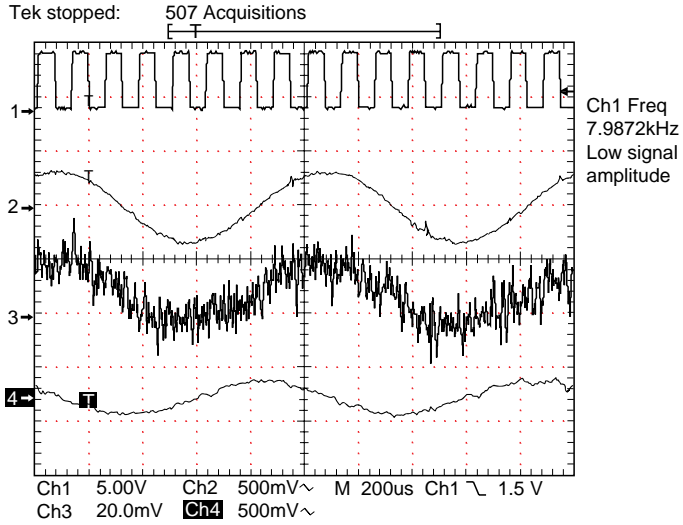
Figure 19 . Waveform W6



W7: Receive audio: Receiving  
 1KHz tone @ 3KHz deviation, -60dBm.  
 Trace 1 - IRQB @ DSP (8KHz)  
 Trace 2 - SD0 @ C404  
 Trace 3 - SPKR\_COMMON  
 Trace 4 - INT\_SPKR<sup>3</sup>

Note 3: Actual level is dependent upon volume setting.

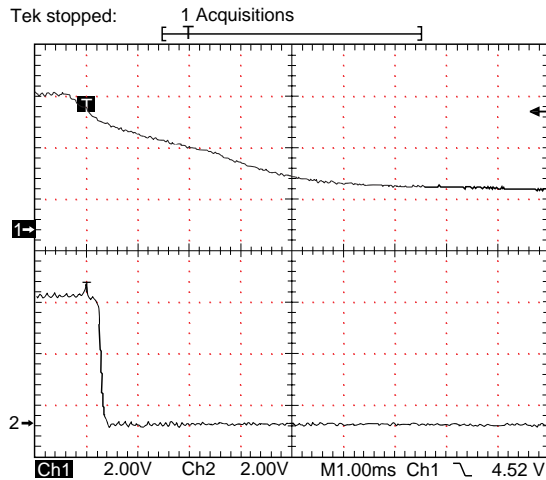
Figure 20 . Waveform W7



MAEPF-24383-A

W8: Transmit Audio. 1KHz Tone  
which provides 3KHz deviation.  
Trace 1 - IRQB @ DSP (8KHz)  
Trace 2 - MODIN  
Trace 3 - EXT MIC @ node C484/R408  
Trace 4 - MAI @ node R492/U401  
MICAMPOUT

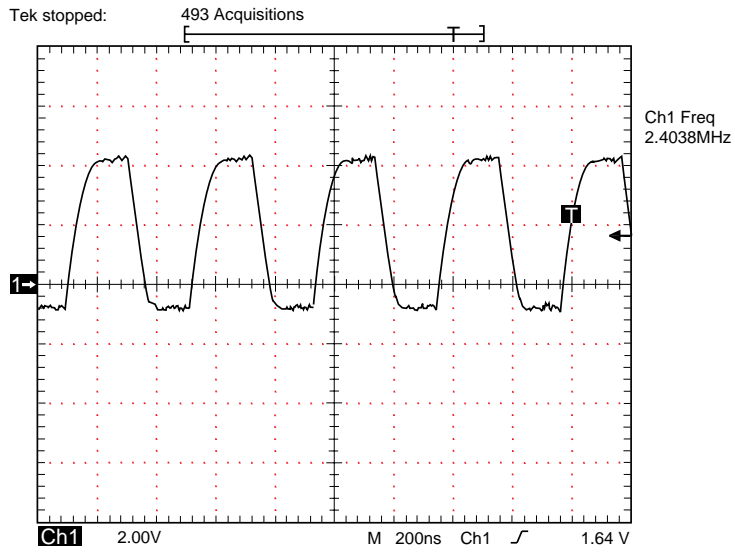
Figure 21 . Waveform W8



MAEPF-24384-O

W9: Power Down Reset.  
Trace 1 - +5V @ U407 (VDD)  
Trace 2 - Reset @ U407 (OUT)

Figure 22 . Waveform W9



W10 ADSIC 2.4 MHz Reference  
Trace 1 - IDC @ U406

MAEPF-24385-O

*Figure 23 . Waveform W10*

# Troubleshooting Diagrams




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## Introduction to This Section

This section contains troubleshooting diagrams necessary to isolate a problem to the component level. Use these diagrams in conjunction with the theory of operation, troubleshooting procedures, charts, and waveforms.

Table 3 . J201  
VOCON Board to Universal Connector

J201 Pin #	Description	To/From	UC Pin #
1	Removed		
2	n/c		
3	n/c		
4	LH DATA/BOOT DATA OUT	U208-1	3
5	EXT MIC	U411-6	4
6	SB9600 BUSY	U204-J3	6
7	OPT SEL 1	U206-G3 (EXT PTT) Q210	7
8	RS232 DATA IN	U206-B2	12
9	OPT SEL2 (KEYLOAD*)	U206-C6	10
10	KEYFAIL*/RTSIN*	U206-J8 J801-15	9
11	SPKR COMMON	U401-A3 U204-B3 J701-14	1
12	EXT SPKR	U401-A5 U204-C4	2
13	OPTB+/BOOT SEL/VPP*	CR201/Q21	8
14	CTSOUT*	U206-B6	5
15	RS232 DATA OUT/BOOT DATA IN	U206-A5	11

Table 4 . J601  
VOCON Board to Display Board

J601 Pin #	Description	To/ From
1	MOSI	U204-J6 J801-8 J401-9
2	SPI SCK	U204-G5 J801-9 J401-10
3	SW B+	J401-17
4	DISP EN*/ LATCH SEL*	U206-G8
5	DISP RST*	U204-F5
6	BL EN	U206-E7
7	+5V	U409-12
8	n/c	
9	+5V	U709-9

Table 5 . J701  
VOCON Board to Keypad

J701 Pin #	Description	To/From
1	ROW 5/5V-EN*	U206-F8
2	GROUND/MIC RETURN	
3	ROW 2/SPK EN	U206-G4
4	INT MIC	U411-2
5	COL2	U206-D5
6	COL3/MOB IRQ*	U206-B4
7	GROUND	
8	n/c	
9	ROW4/TXPA EN*	U206-G9
10	COL1	U206-A7
11	ROW3/BUSY OUT	U206-K8
12	ROW6/MIC EN	U206-G7
13	ROW1	U206-J3
14	SPKR COMMON	U401-A3 J201-11 U401-A3 U204-B3
15	INT SPKR	U401-B2

Table 6 . J1/J401  
Transceiver Board to VOCON Board

J1/ J401 Pin #	Description	Transceiv Board	VOCON Board
1	DOUT*	U401-4	U406-H3
2	DOUT	U401-5	U406-K3
3	GROUND		
4	SBI	U401-6	U406-J3
5	GROUND		
6	POR*RSSI	U305-5 U503-19	U407-1
7	DA SEL* DA CE	U503-16	U204-H5
8	ODC 2.4MHz	U401-7	U406-F3
9	MOSI DATA	U503-18 U302-2 U304-25	
10	SPI SCK*	U503-17 U302-3 U304-22 (CLOCK)	U204-G5
11	ROSC/PSC CE*	U304-24 (REF OSC EN)	U204-F6
12	GROUND		
13	LOCK DET*	U302-41 CR502	U206-K2
14	SYN SEL*	U302-4 (SYN CE)	U204-H7
15	MOD IN	U302-5	U406-B2
16	GROUND		
17	SW B+	U305-8	U409, J801-1, Q206
18	GROUND		
19	UNSW B+	J3-1 U105-5 U502-6 (RAW B+)	U409-1
20	UNSW B+	J3-1 U105-5 U502-6 (RAW B+) J801-20	U409-1 Q207

Table 7 . J801  
VOCON Board to Encryption Board

J801 Pin #	Description	To/From
1	SW B+	J401-17
2	SW B+	J401-17
3	EMC RXO	U405-B7
4	EMC TXO	U405-A7
5	n/c	
6	GROUND	
7	MISO	U204-H6
8	MOSI	U204-J6 J601-1
9	SPI SCK	U204-G5 J601-2
10	EMC EN*	U206-D6
11	EMC REQ*	U206-H3
12	EMC MAKEUP*	U206-K7
13	n/c	
14	n/c	
15	KEYFAIL*/RTSIN*	U206-J8
16	n/c	
17	n/c	
18	n/c	
19	n/c	
20	UNSW B+	J401-19
21	GROUND	
22	GROUND	
23	n/c	
24	n/c	
25	n/c	

Table 8 . J901  
VOCON Board to Control Top Flex

J901 Pin #	Description	To/From
1	UNSW B+	J401-19
2	TG1/PROG SWITCH	U204-D3
3	VOL	U204-C3
4	EMERG	U204-A3
5	+5V	U409-12
6	INT PTT*	U204-H2
7	RTA3	U206-H1
8	GRN LED DRIVER	U206-E8
9	TG2 A/B SWITCH*	U204-A2
10	B+ SENSE	
11	RTA0	U206-F3
12	RED LED DRIVER	U206-H9
13	RTA1	U206-F4
14	GROUND	
15	RTA2*	U206-F2
16	n/c	
17	n/c	
18	n/c	
19	n/c	
20	UNSW B+	J401-19
21	GROUND	
22	GROUND	
23	n/c	
24	n/c	
25	n/c	







68P81076C10-A

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# Troubleshooting Charts

This section contains detailed troubleshooting flowcharts. These charts should be used as a guide in determining the problem areas. They are not a substitute for knowledge of circuit operation and astute troubleshooting techniques. It is advisable to refer to the related detailed circuit descriptions in the theory section prior to troubleshooting a radio.

Most troubleshooting charts end up by pointing to an IC to replace. It is not always noted, but is good practice to verify supplies and grounds to the affected IC and to trace continuity to the malfunctioning signal and related circuitry before replacing any IC. For instance, if a clock signal is not available at a destination IC, continuity from the source IC should be checked before replacing the source IC.

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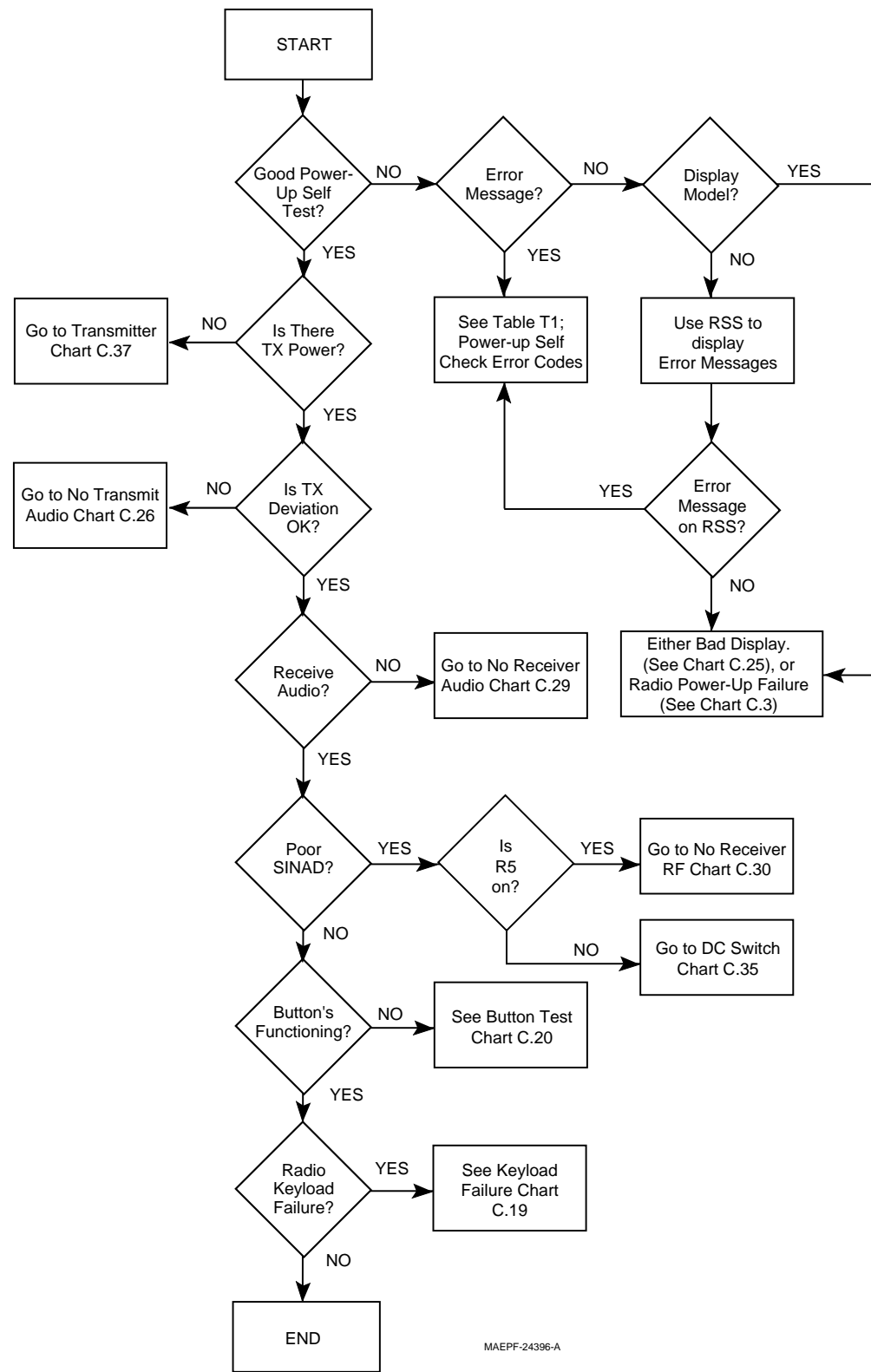


Chart 1 . 800MHz Radio Main Troubleshooting Chart

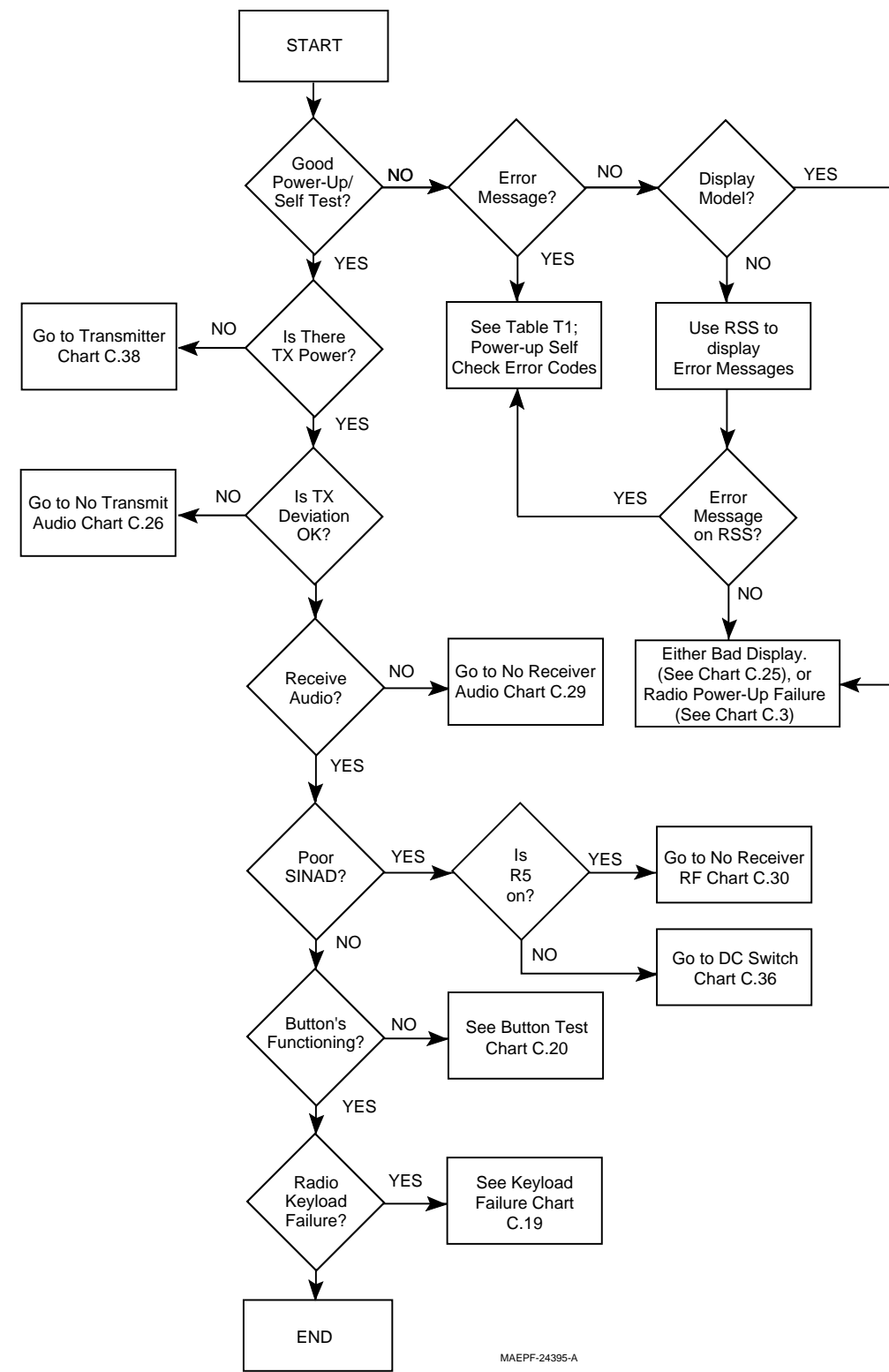
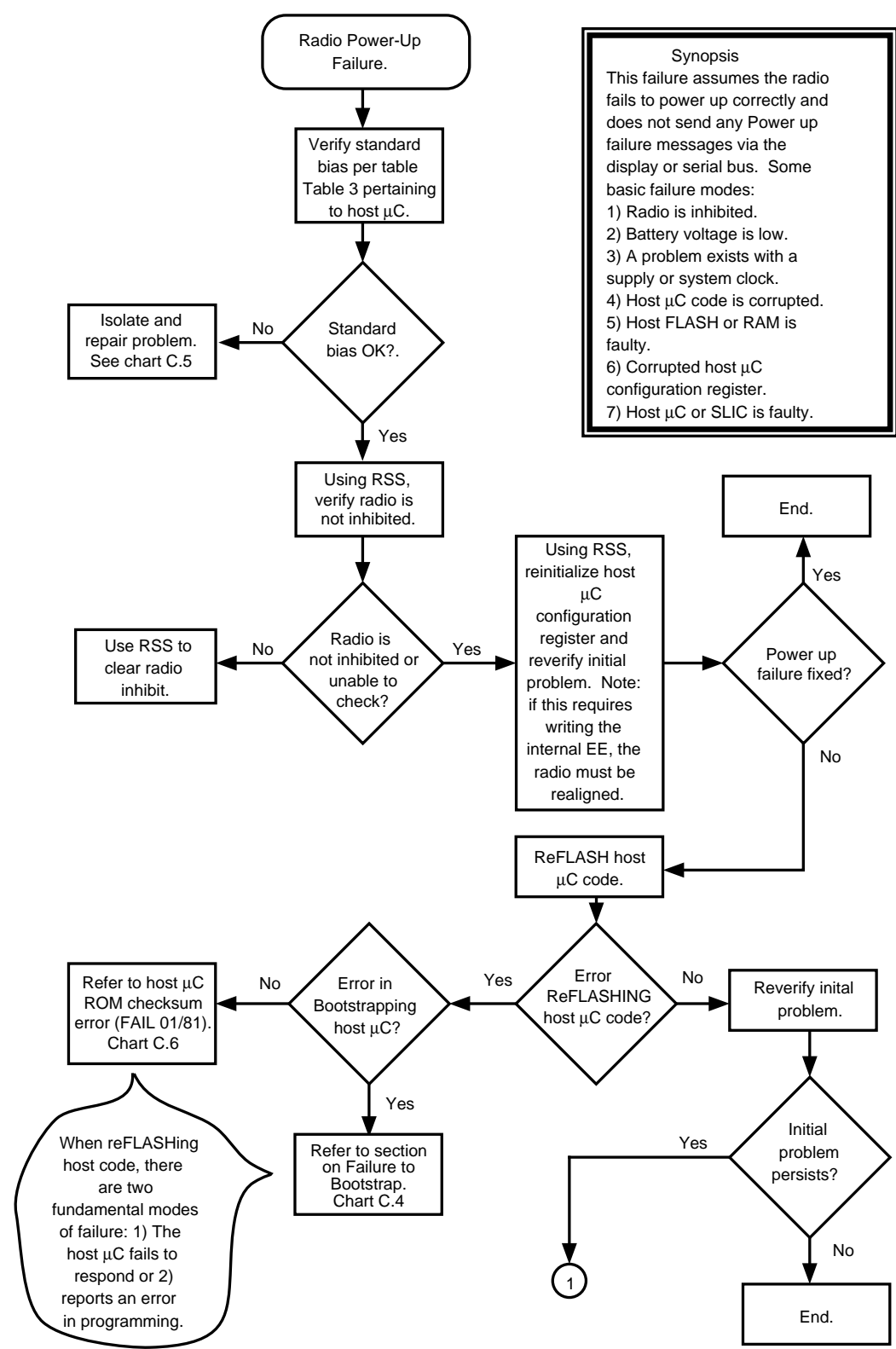


Chart 2 . VHF/UHF Radio Main Troubleshooting Chart



When reFLASHing host code, there are two fundamental modes of failure: 1) The host  $\mu$ C fails to respond or 2) reports an error in programming.

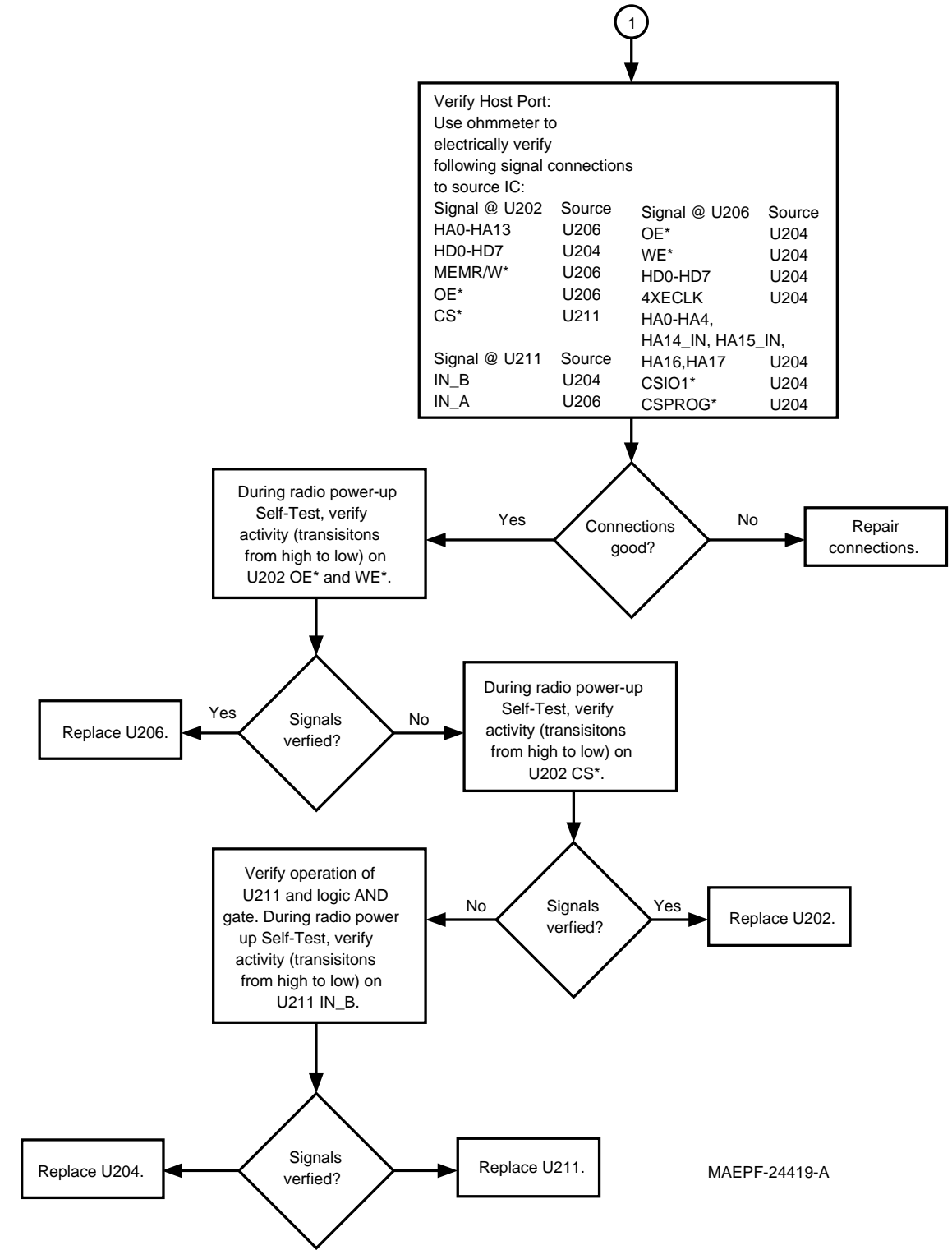
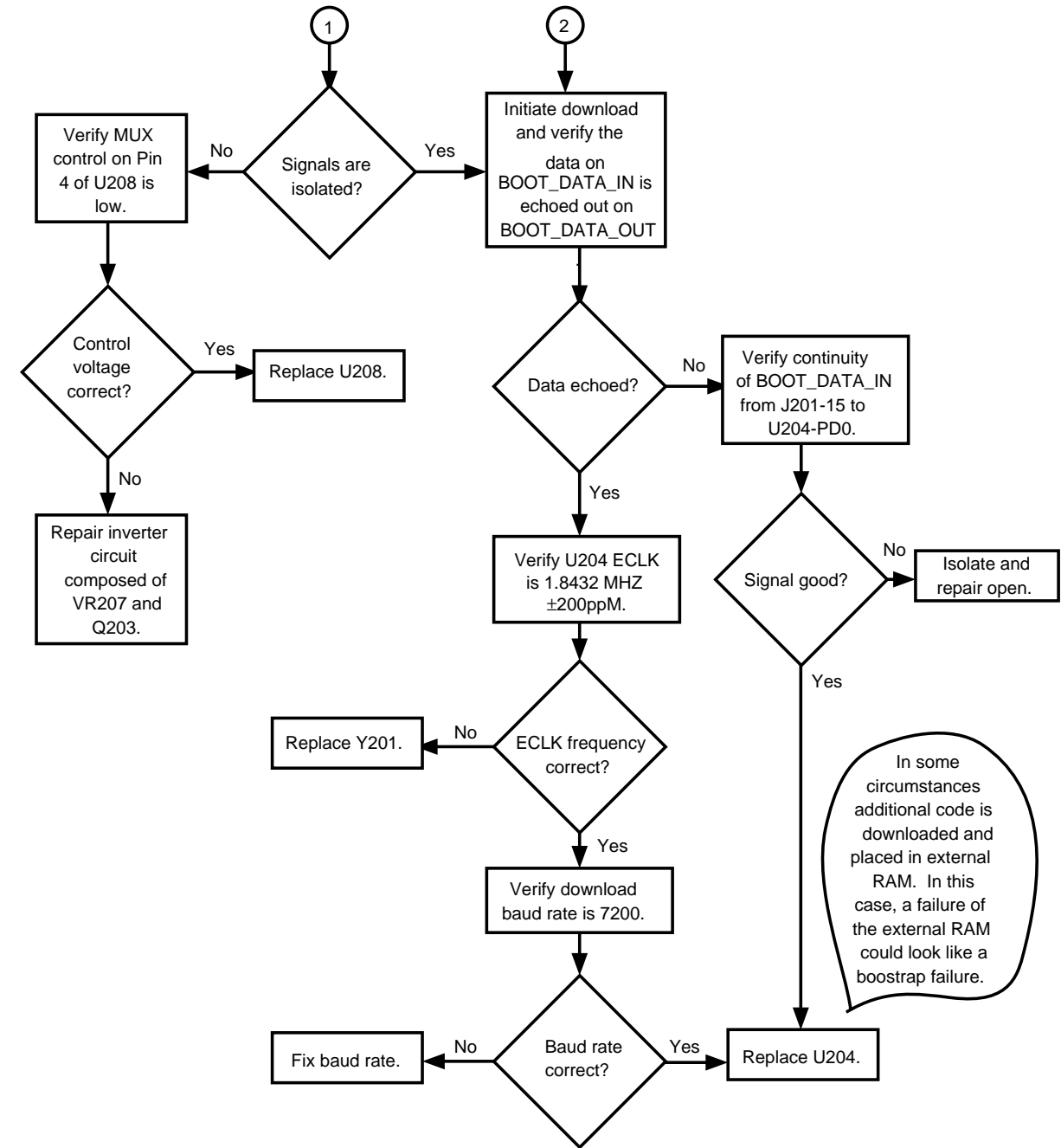
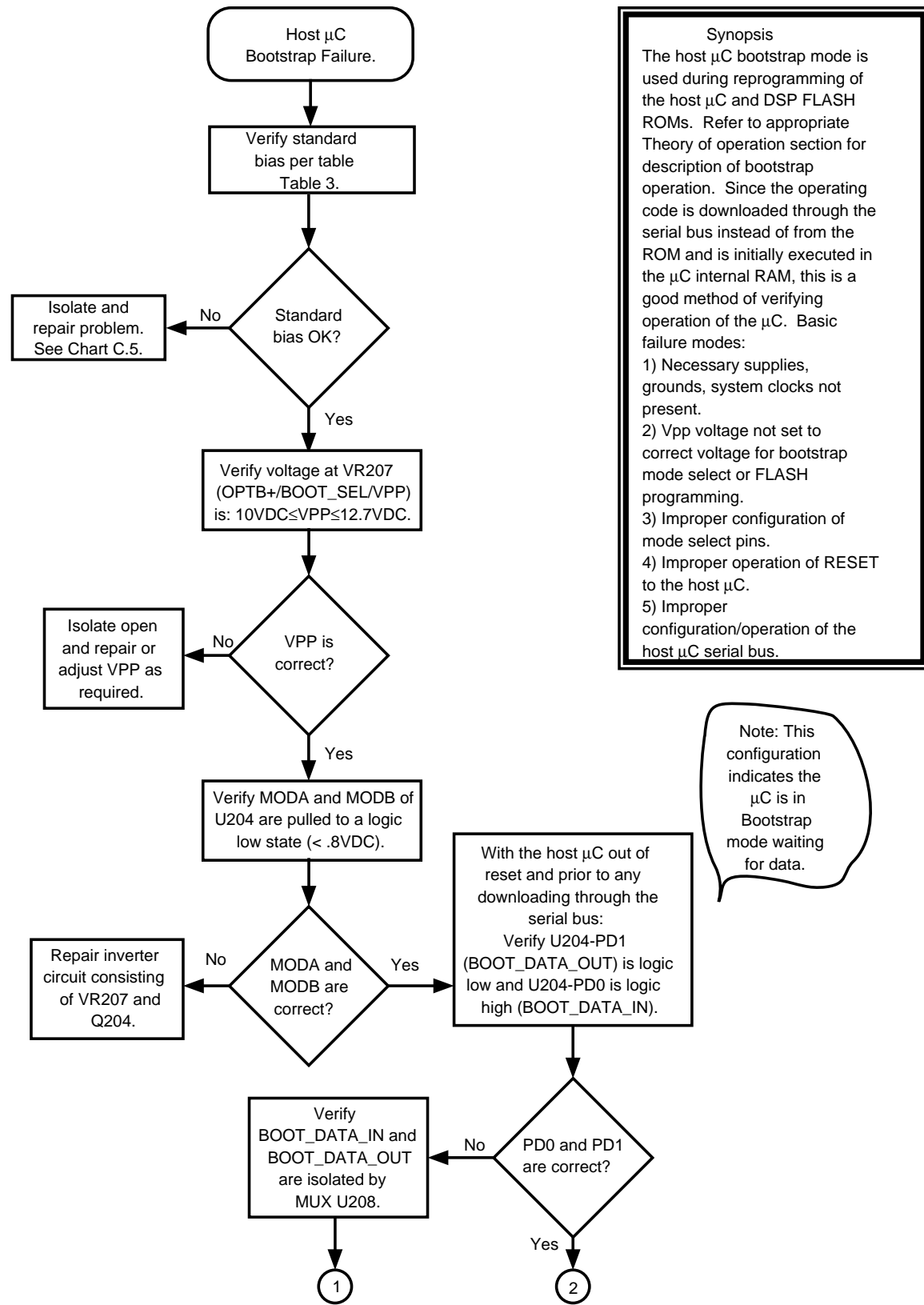


Chart 3 . Radio Power-Up Fail



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Chart 4 . Bootstrap Fail

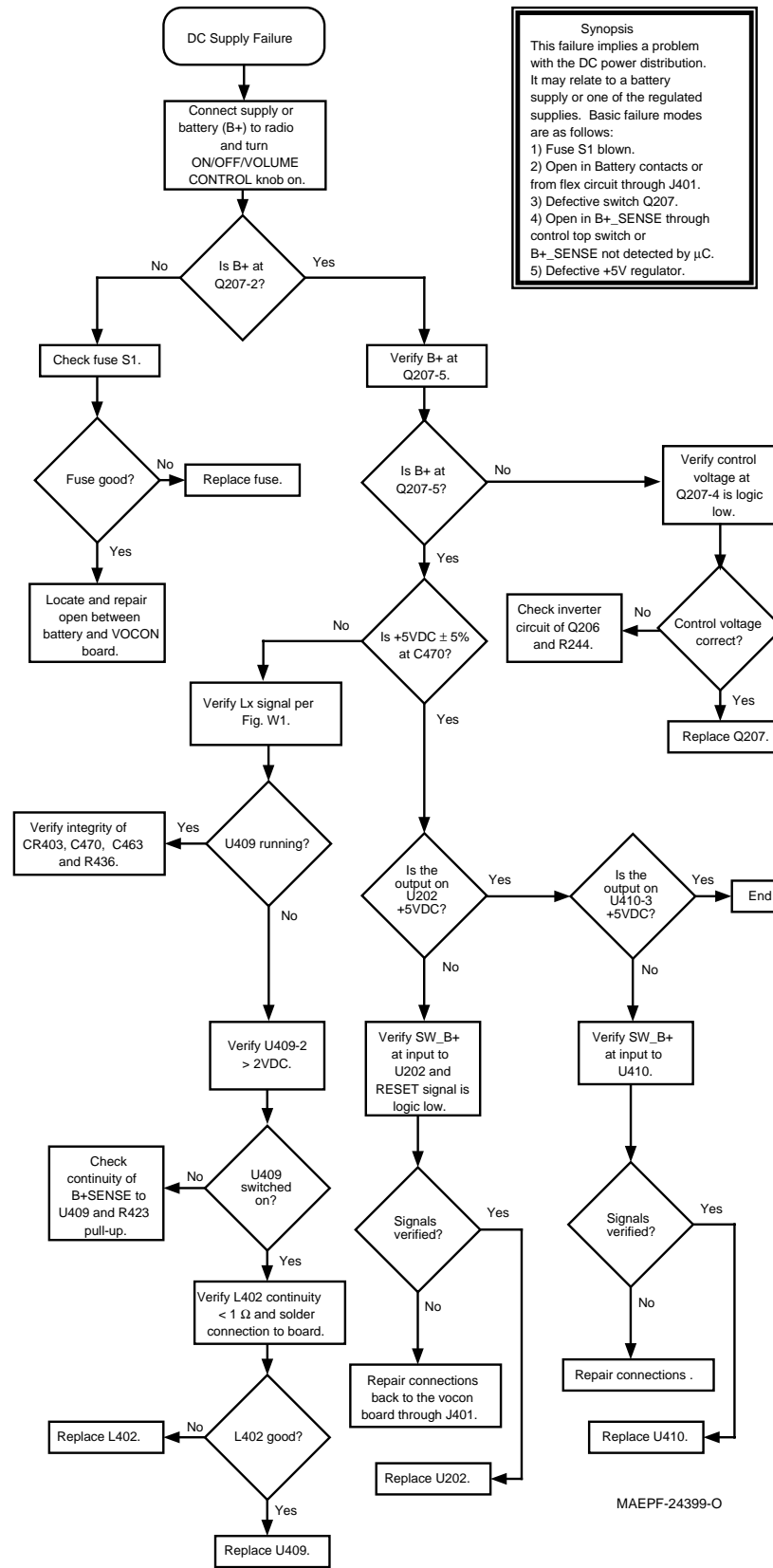


Chart 5 . DC Supply Failure

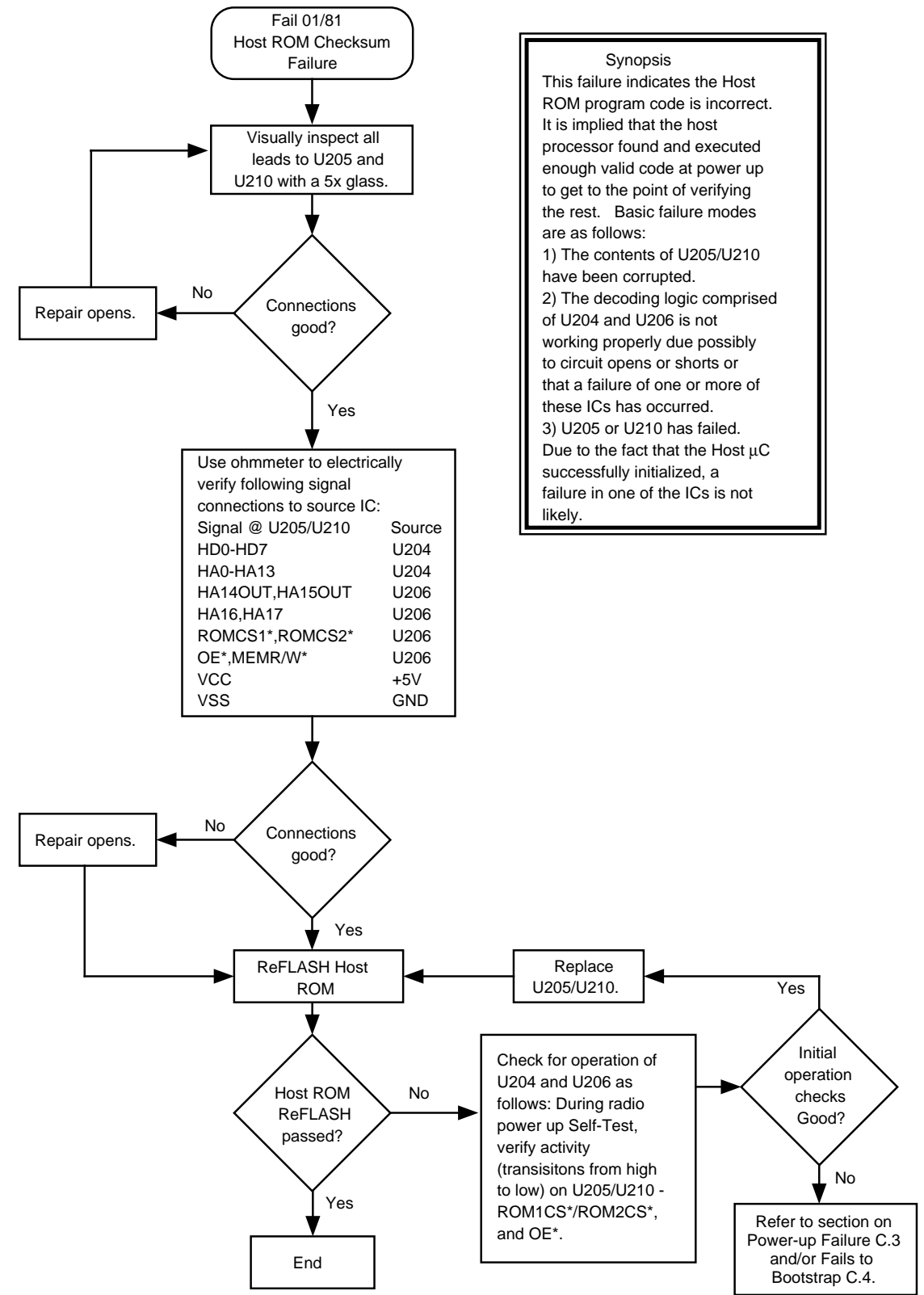


Chart 6 . 01/81 Host ROM Checksum Failure

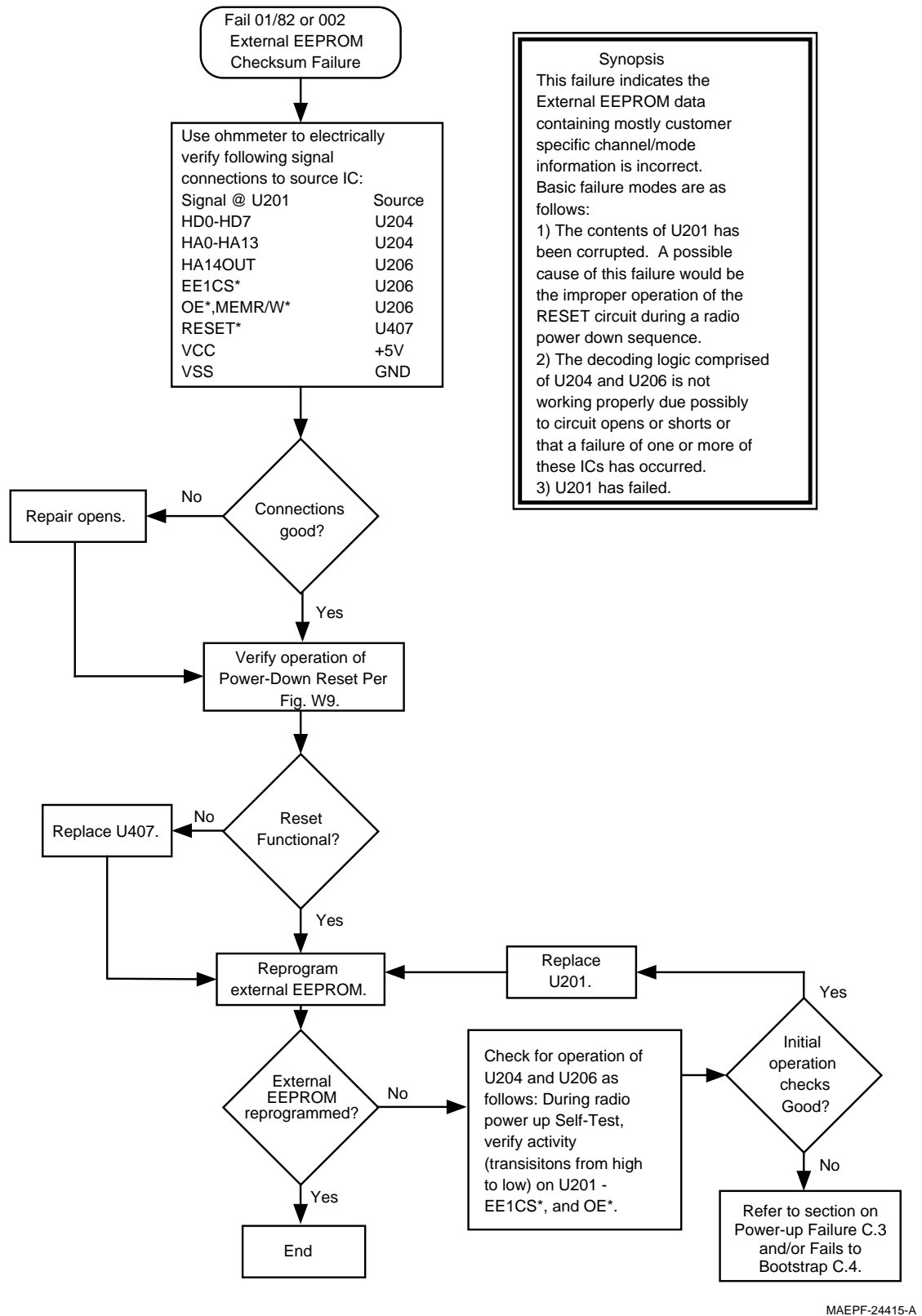


Chart 7 . 01/82 or 002, External EEPROM Checksum Failure

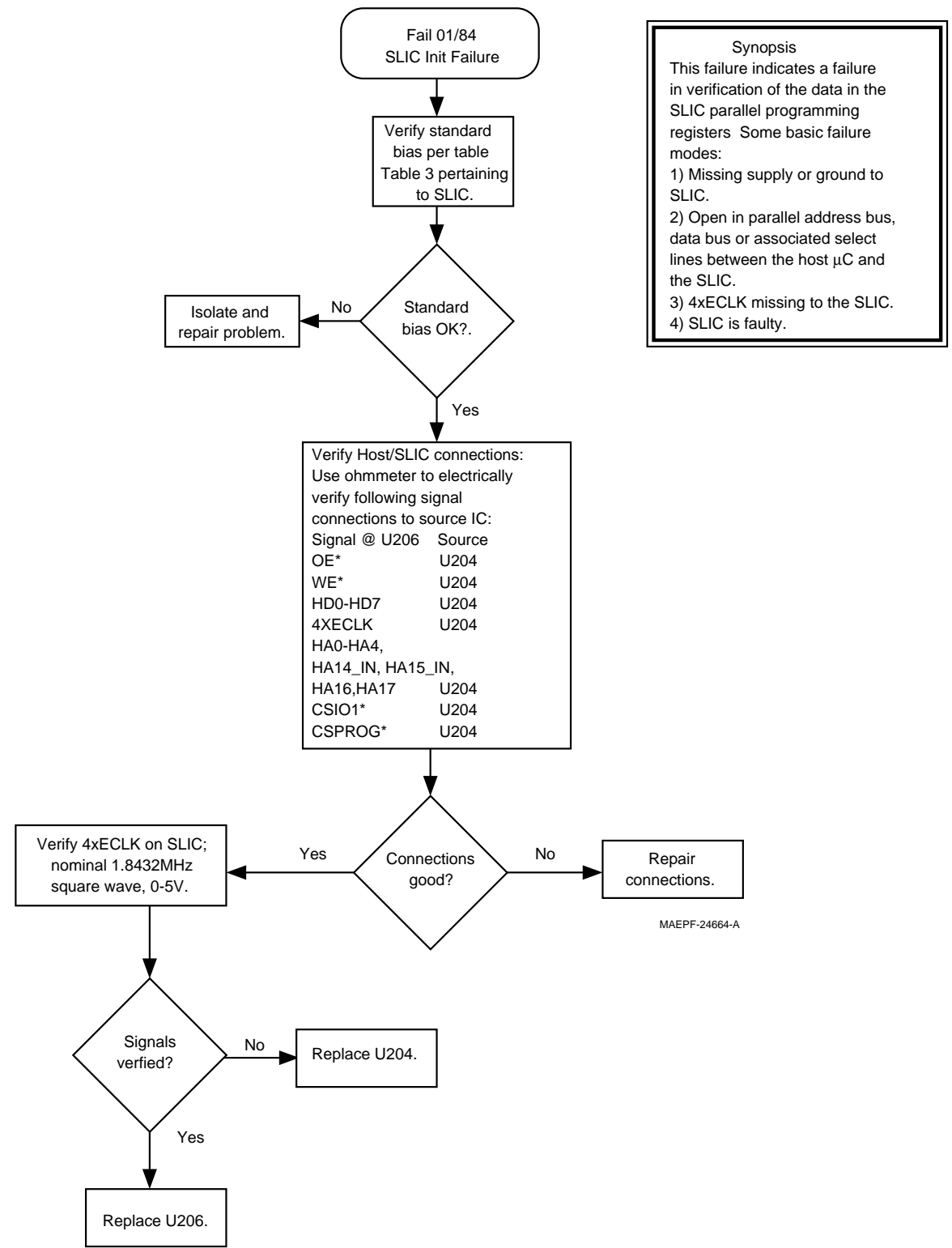


Chart 8 . 01/84 SLIC Initialization Failure



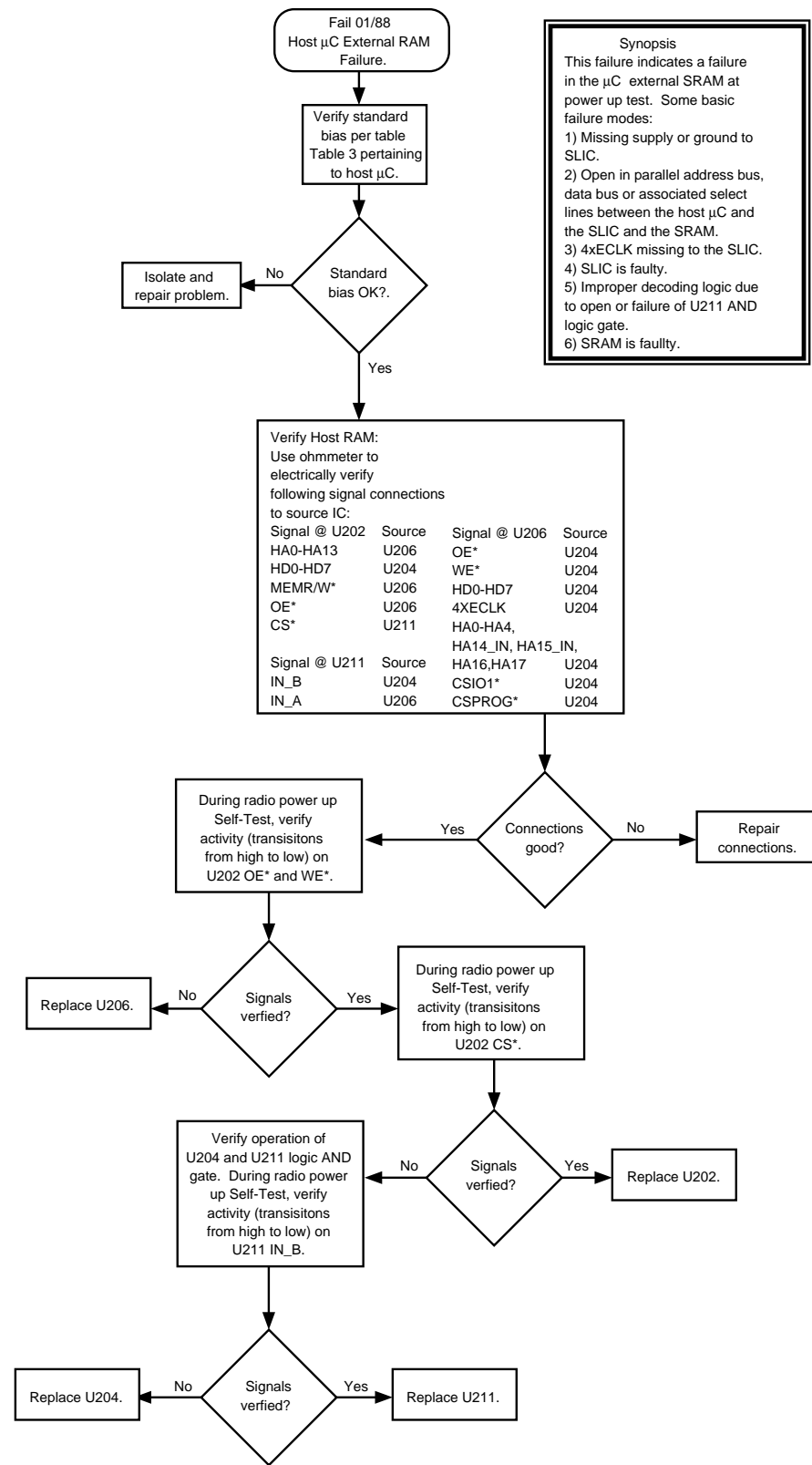


Chart 9 . 01/88 MCU (Host  $\mu$ C) External SRAM Failure

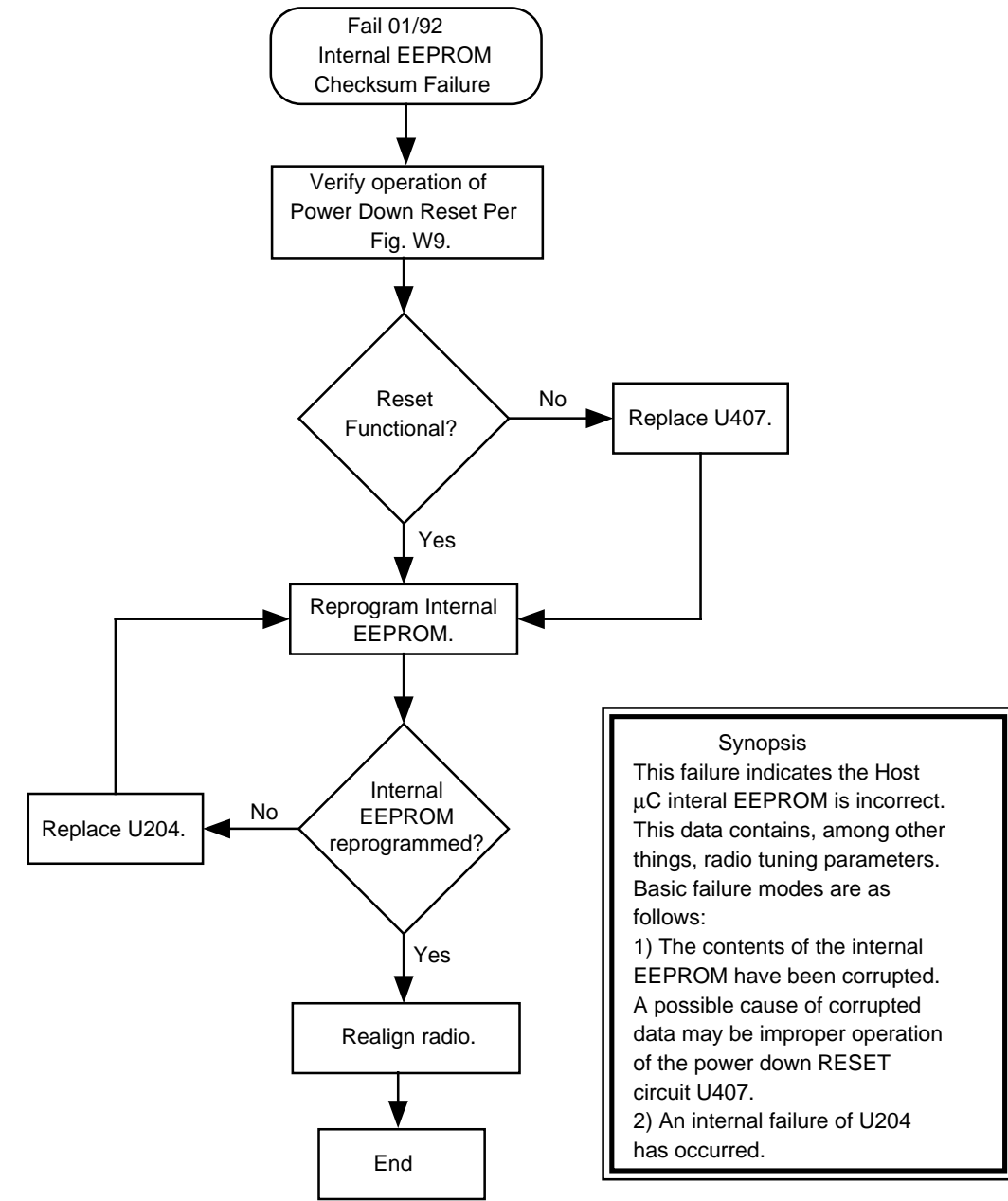


Chart 10 . 01/92, Internal EEPROM Checksum Failure

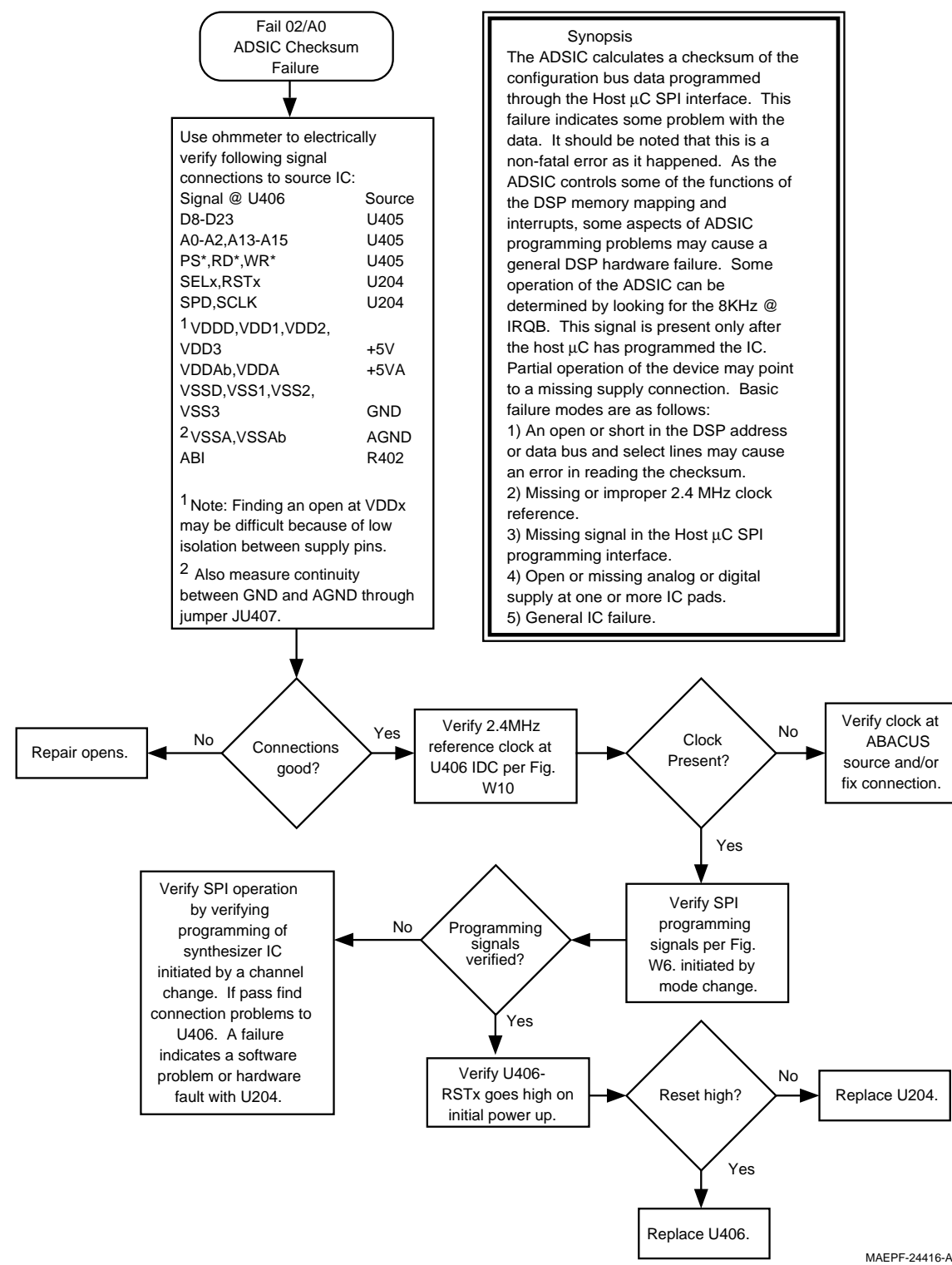


Chart 11 . 02/A0, ADSIC Checksum Failure

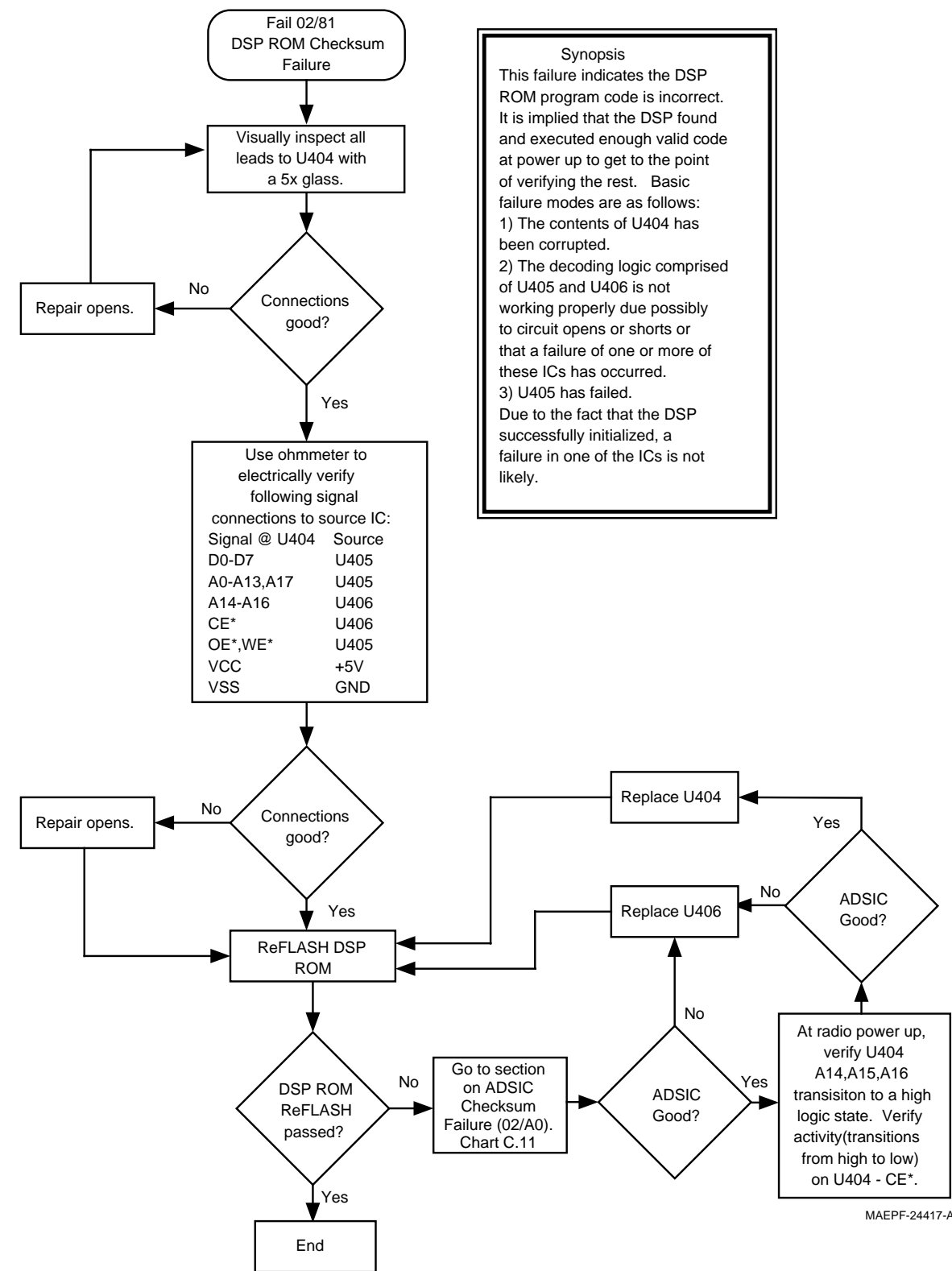


Chart 12 . 02/81, DSP ROM Checksum Failure

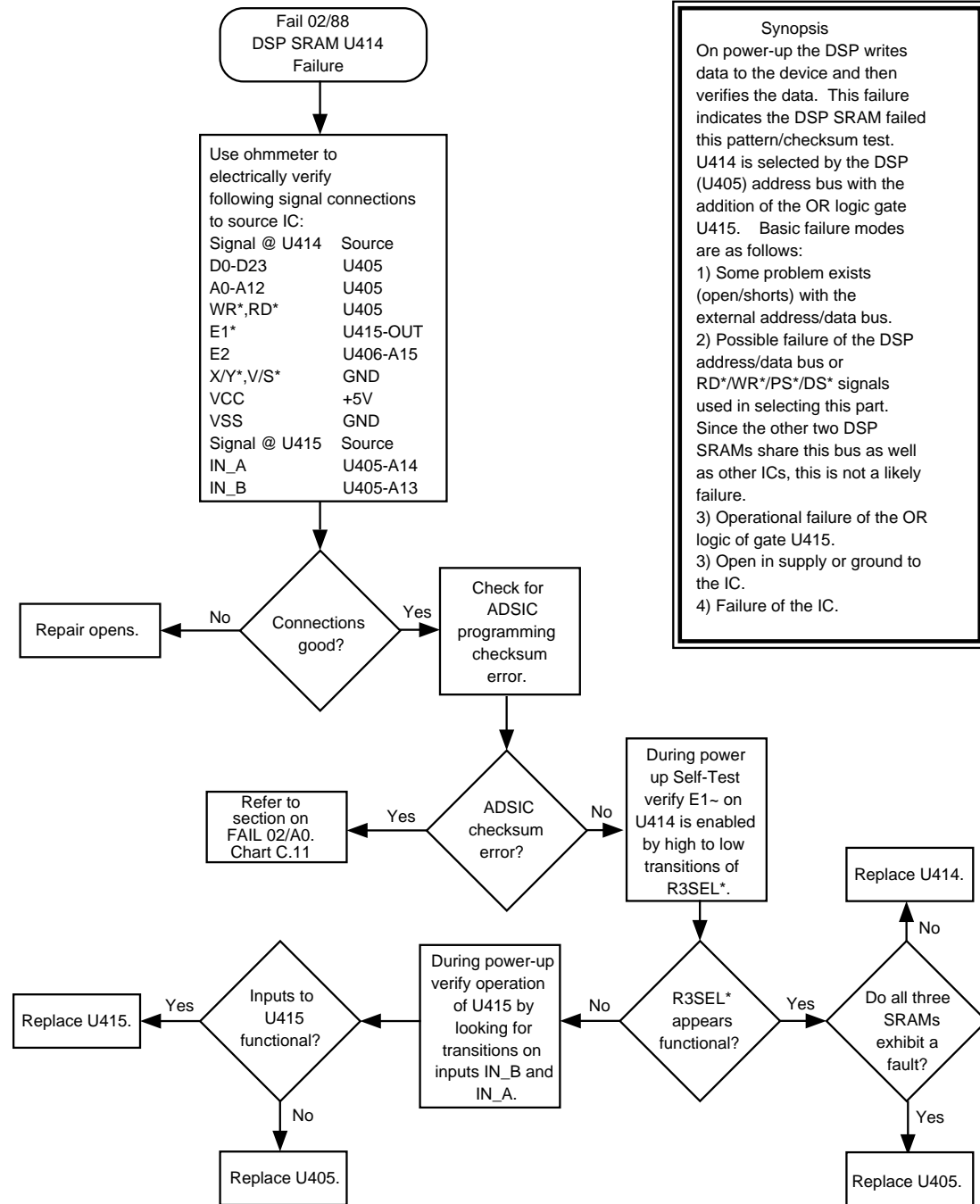


Chart 13 . 02/88, DSP External SRAM Failure U414

Synopsis  
On power-up the DSP writes data to the device and then verifies the data. This failure indicates the DSP SRAM failed this pattern/checksum test. U414 is selected by the DSP (U405) address bus with the addition of the OR logic gate U415. Basic failure modes are as follows:

- 1) Some problem exists (open/shorts) with the external address/data bus.
- 2) Possible failure of the DSP address/data bus or RD\*/WR\*/PS\*/DS\* signals used in selecting this part. Since the other two DSP SRAMs share this bus as well as other ICs, this is not a likely failure.
- 3) Operational failure of the OR logic of gate U415.
- 3) Open in supply or ground to the IC.
- 4) Failure of the IC.

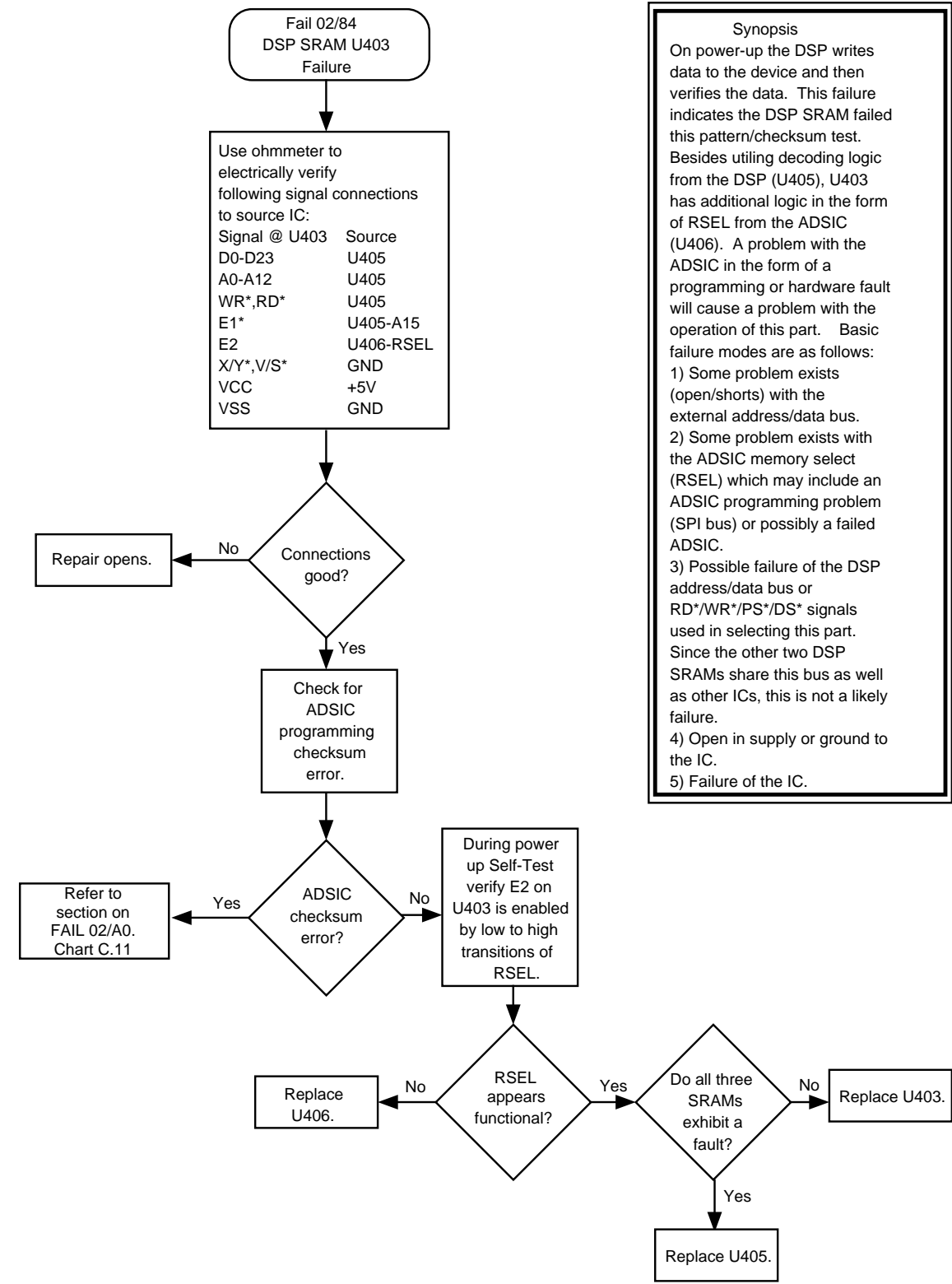


Chart 14 . 02/84, DSP External SRAM Failure U403

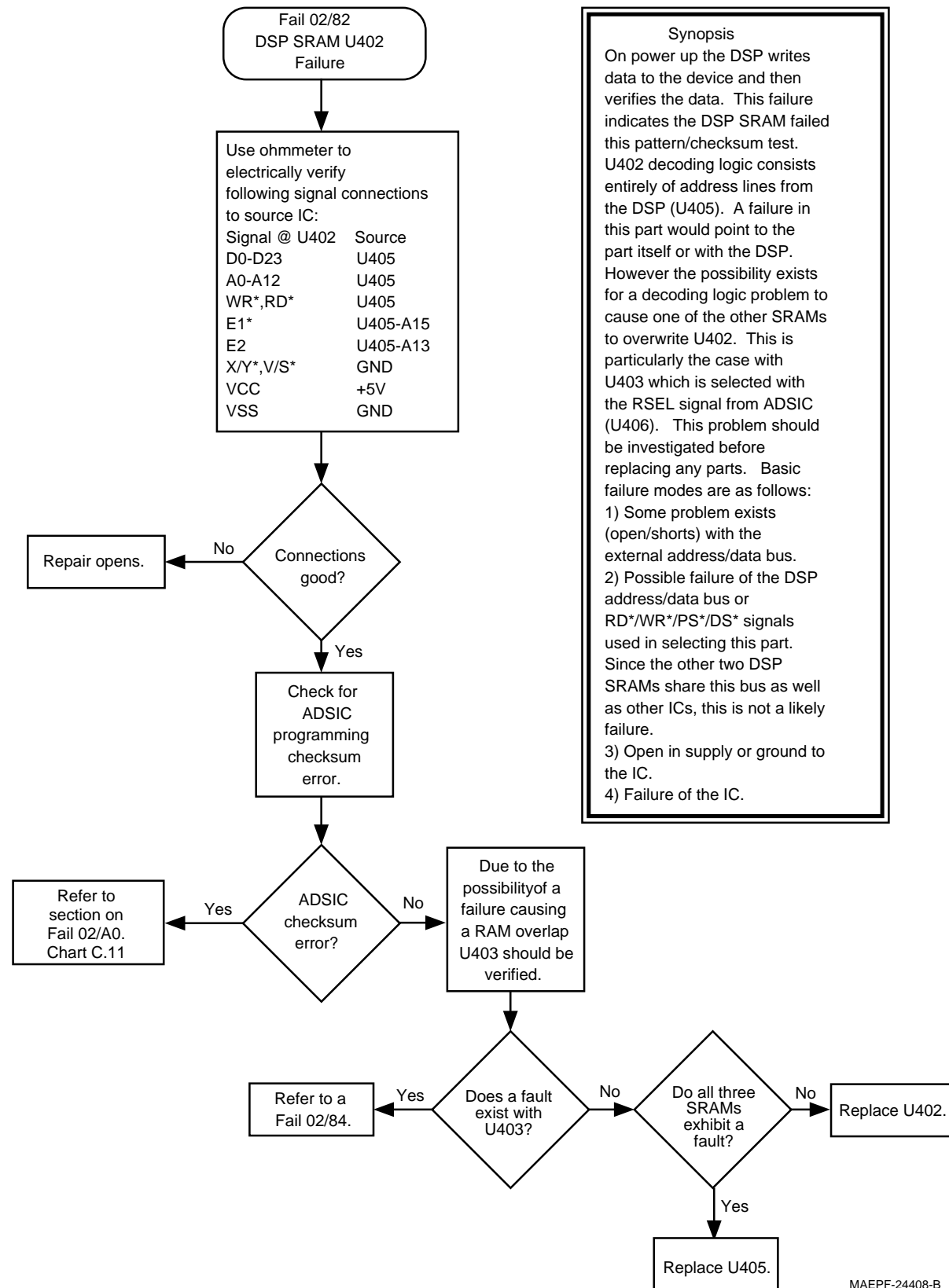


Chart 15 . 02/82, DSP External SRAM Failure U402

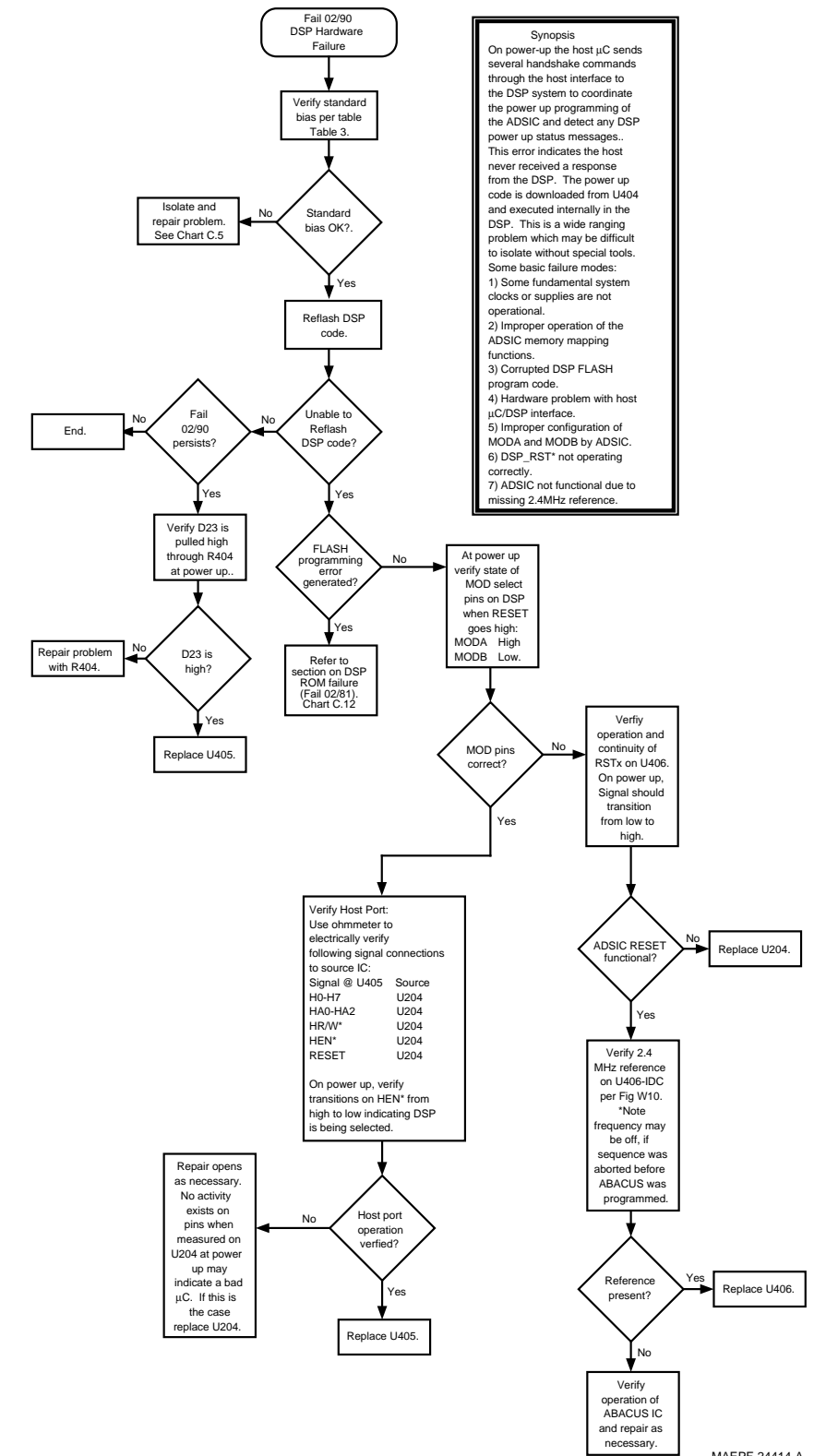


Chart 16 . 02/90, General DSP Hardware Failure

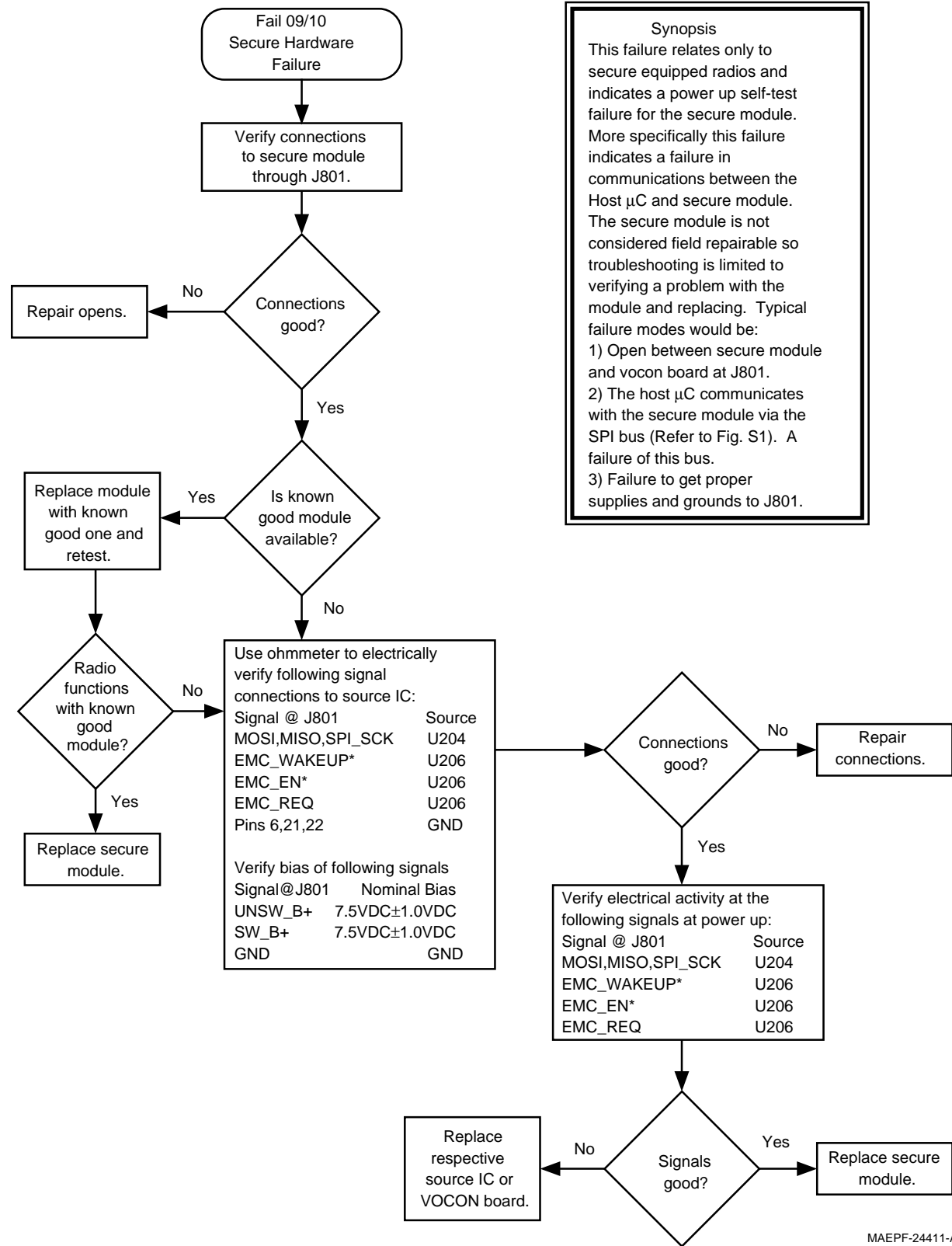


Chart 17 . 09/10, Secure Hardware Failure

MAEPF-24411-A

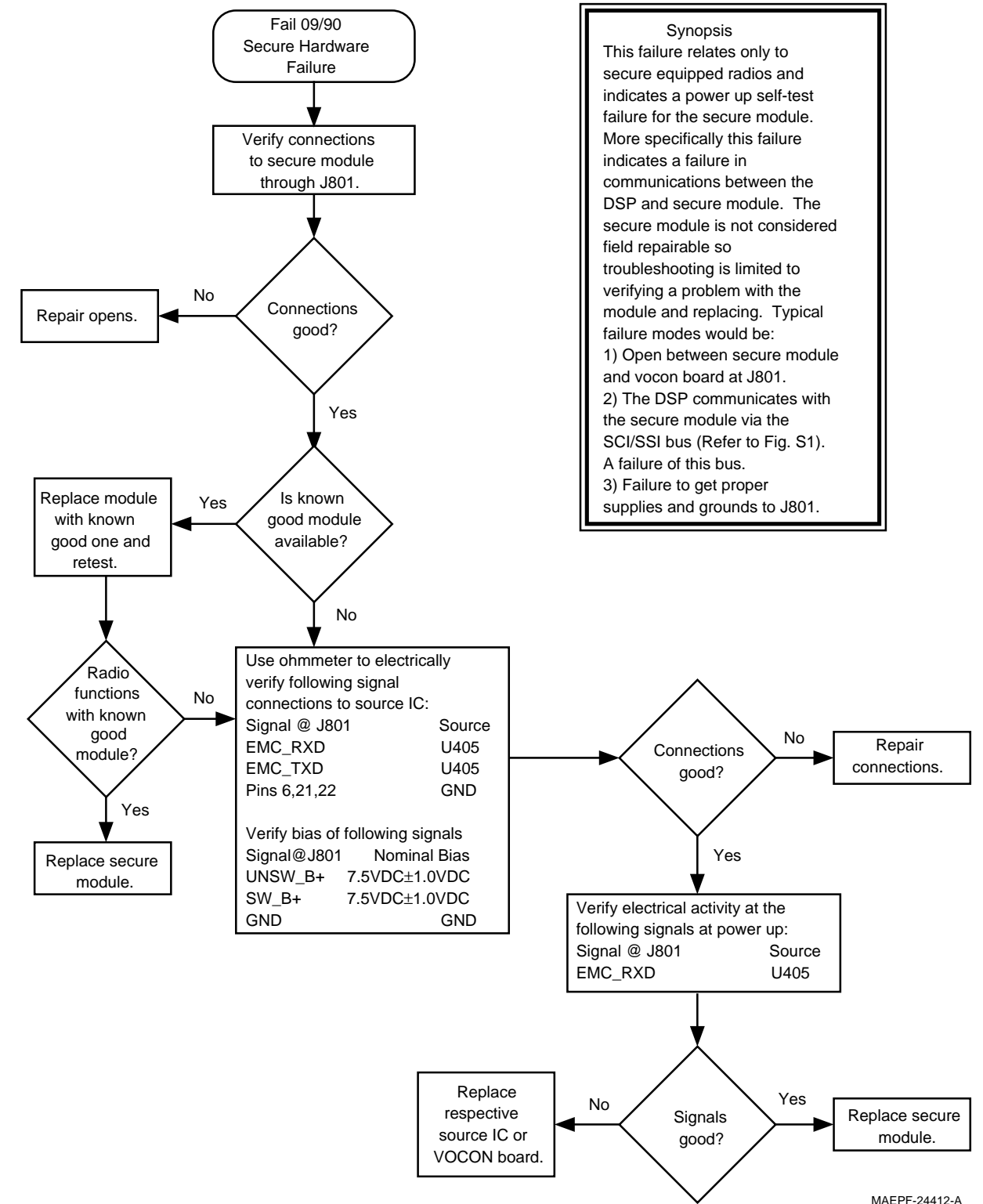


Chart 18 . 09/90, Secure Hardware Failure

MAEPF-24412-A

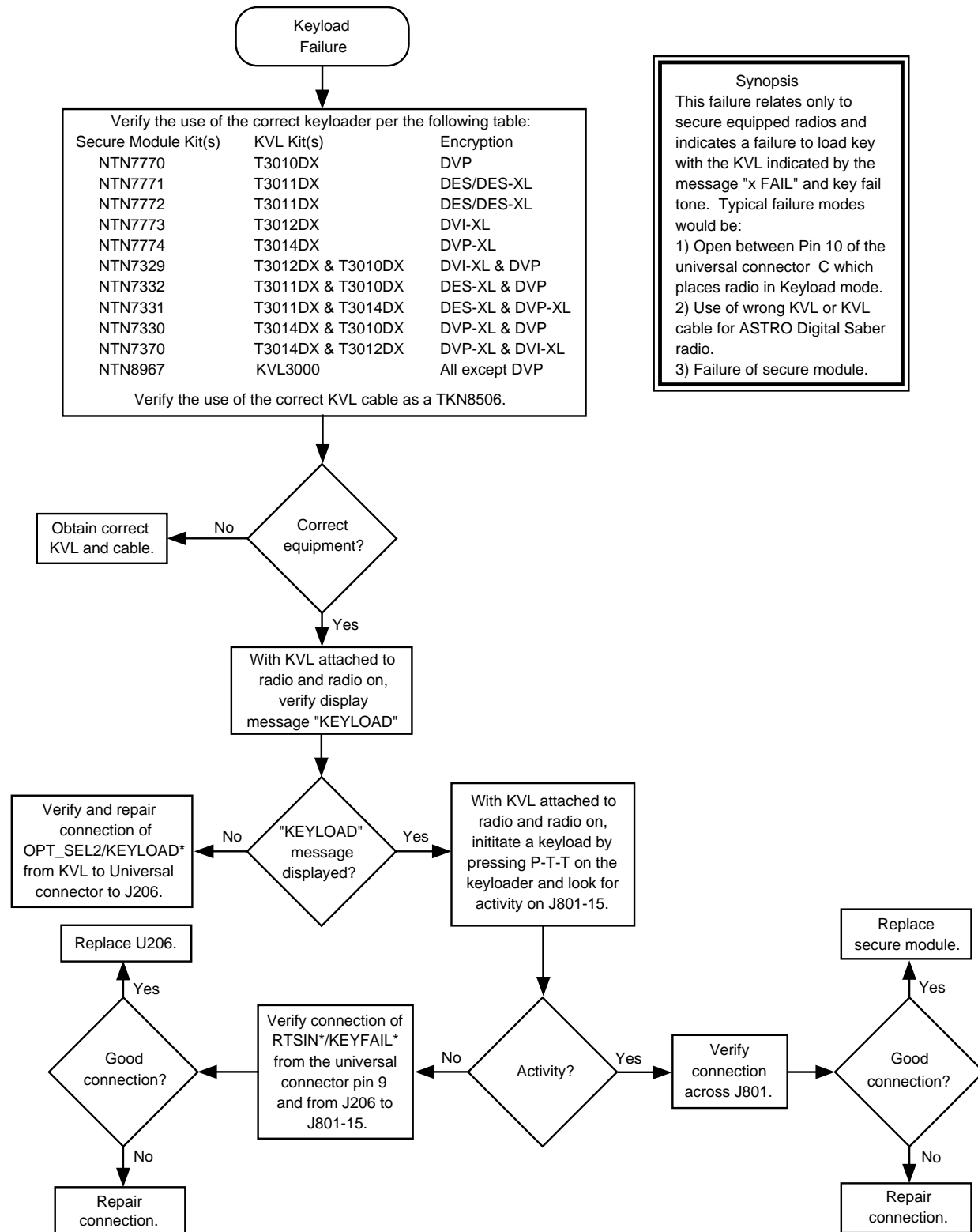


Chart 19 . Key Load Fail

MAEPF-27147-O

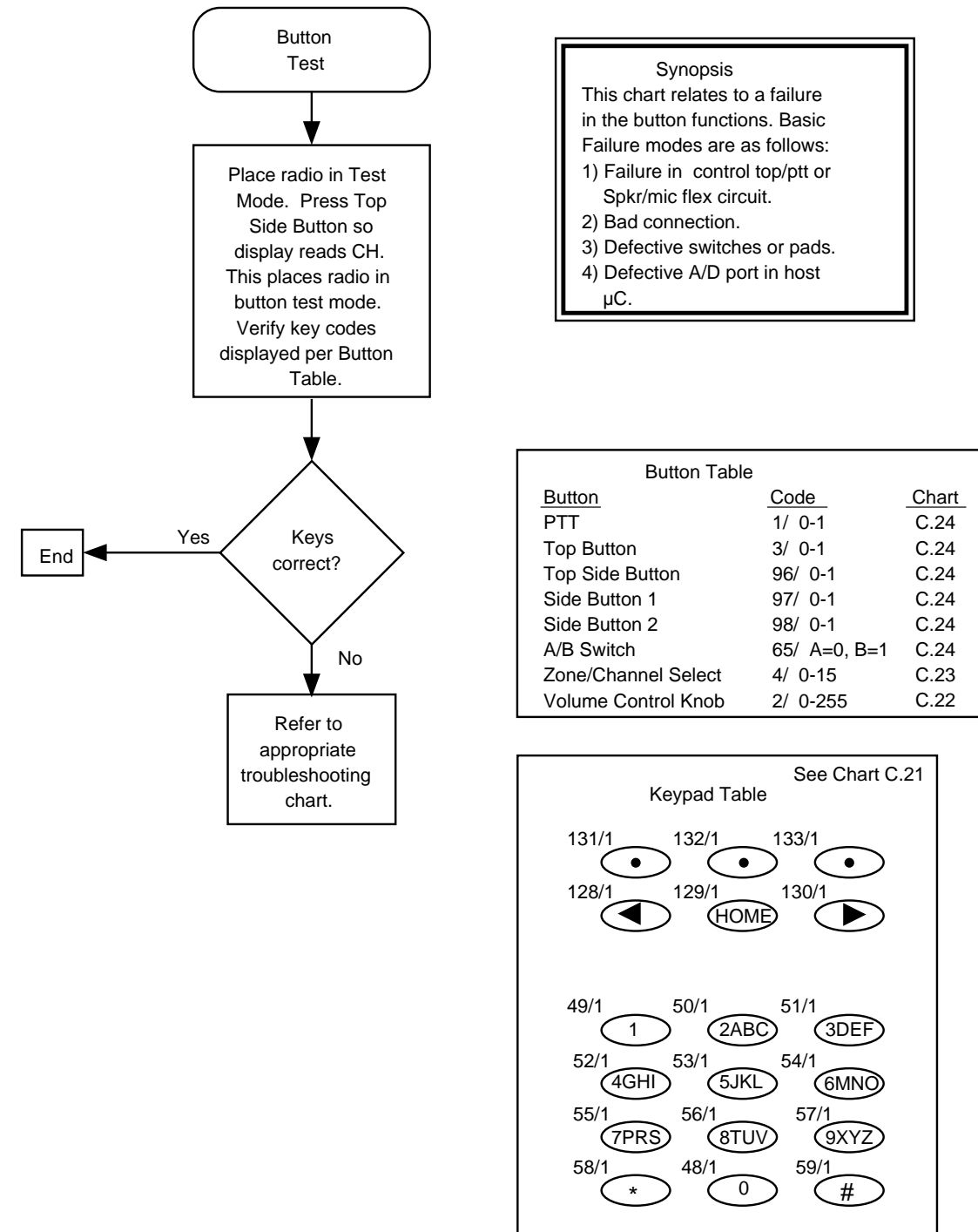
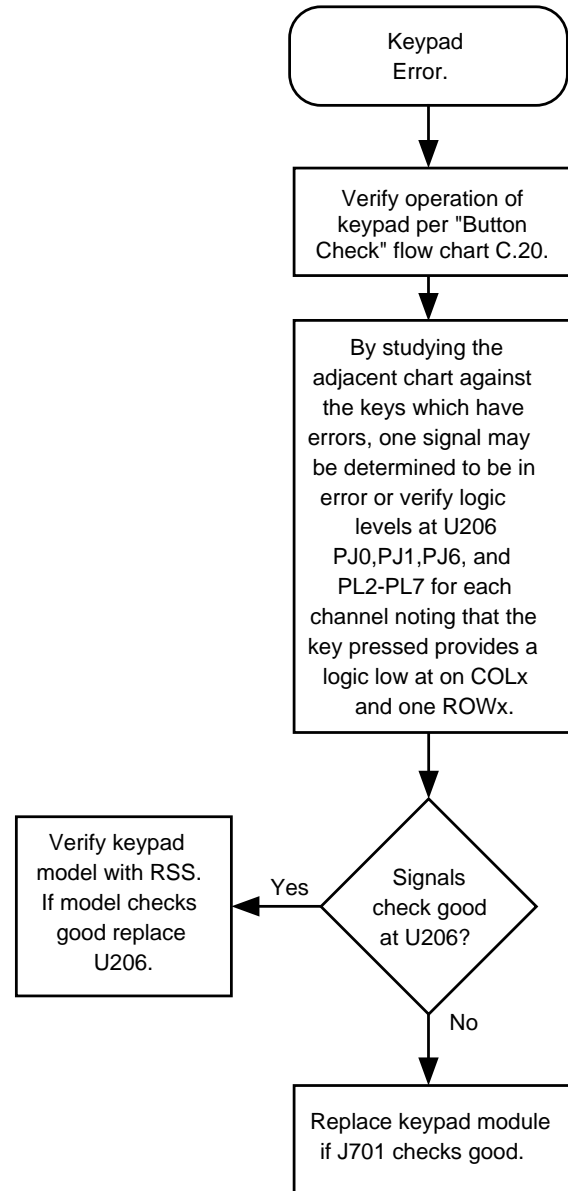
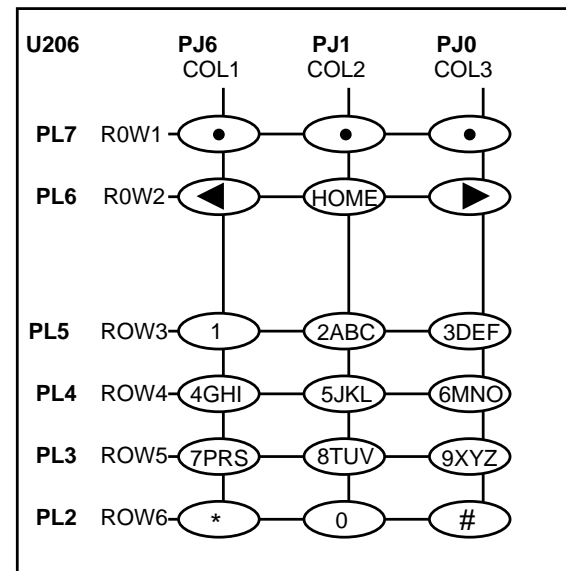


Chart 20 . Button Test

MAEPF-24397-O

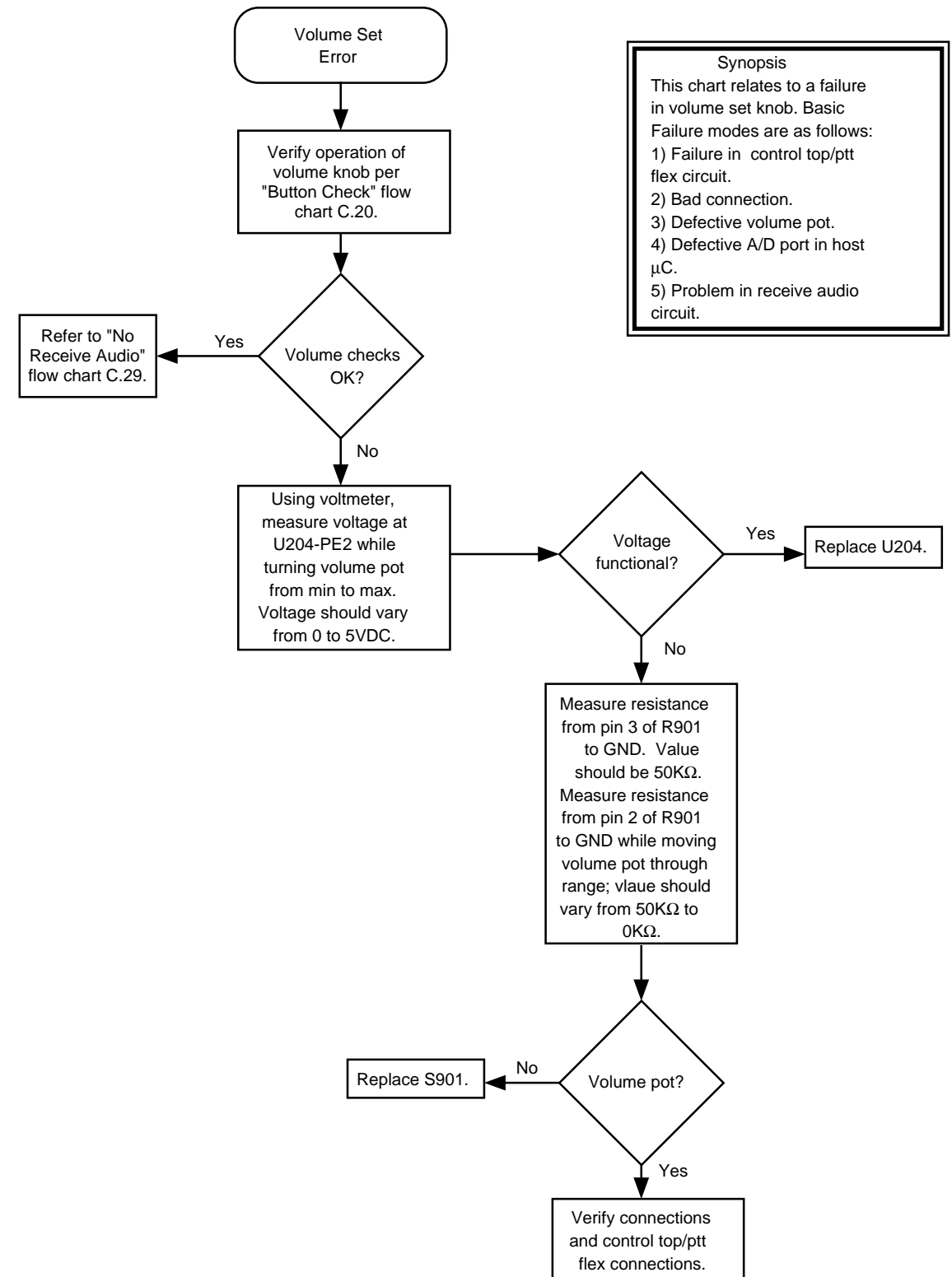


**Synopsis**  
 This chart relates to a failure in reading the keypad. Basic Failure modes are as follows:  
 1) Failure in flex circuit.  
 2) Bad connection.  
 3) Defective keypad.  
 4) Defective port in SLIC.



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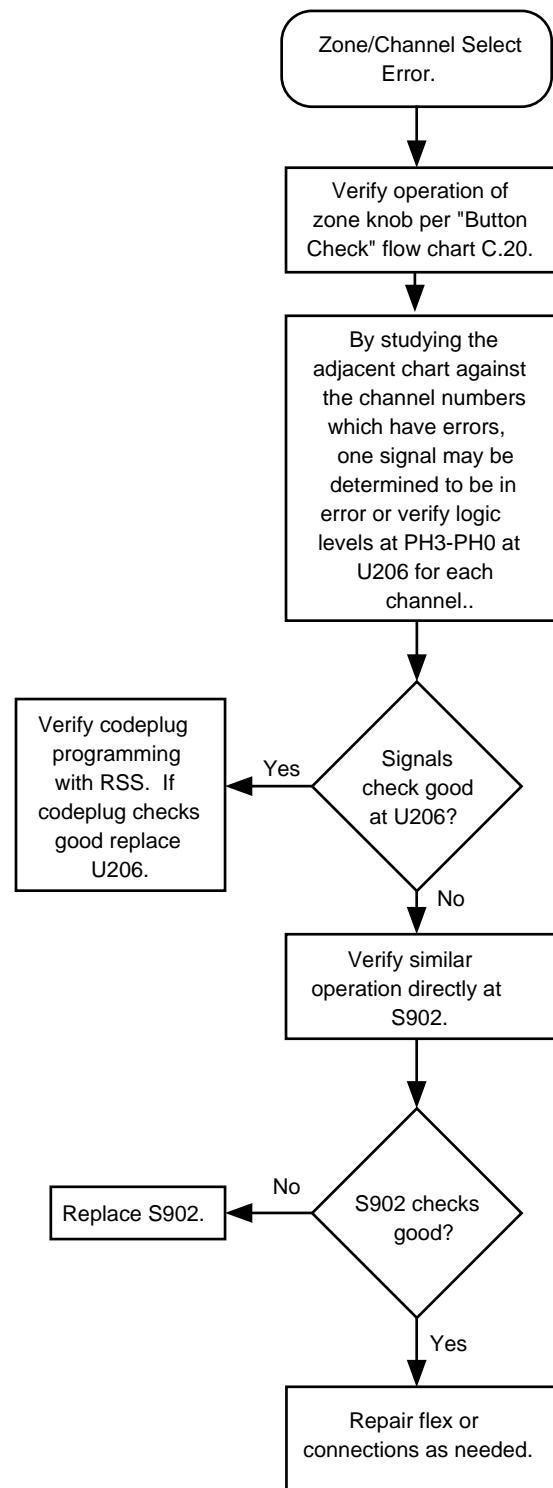
Chart 21 . Keypad Error



**Synopsis**  
 This chart relates to a failure in volume set knob. Basic Failure modes are as follows:  
 1) Failure in control top/ptt flex circuit.  
 2) Bad connection.  
 3) Defective volume pot.  
 4) Defective A/D port in host μC.  
 5) Problem in receive audio circuit.

MAEPF-24401-A

Chart 22 . Volume Set Error

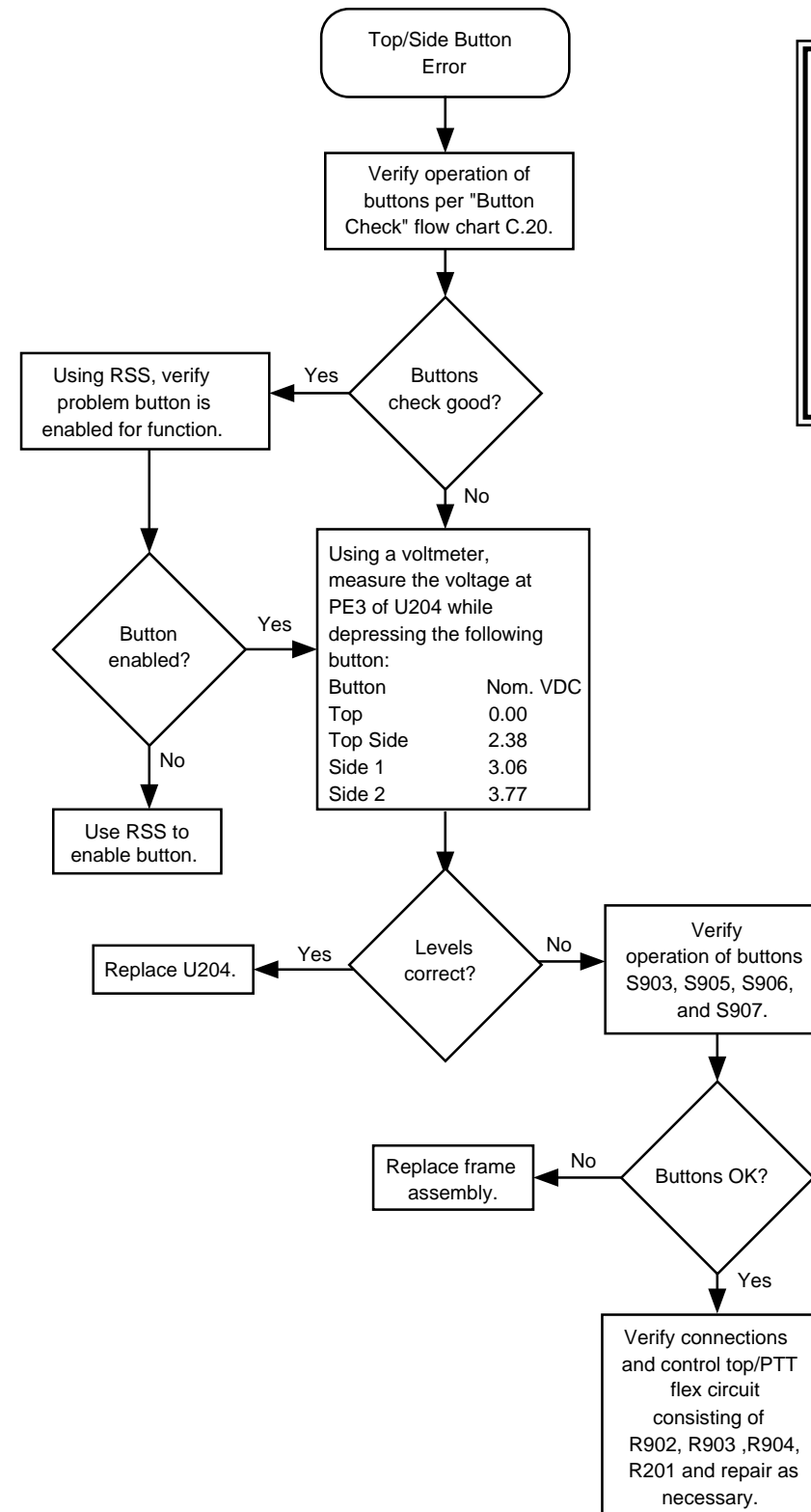


MAEPF-24402-A

Chart 23 . Zone/Channel Select Error

**Synopsis**  
 This chart relates to a failure in reading the zone/channel select knob. Basic Failure modes are as follows:  
 1) Failure in flex circuit.  
 2) Bad connection.  
 3) Defective switch.  
 4) Defective port in SLIC.

Channel	RTA3	RTA2	RTA1	RTA0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

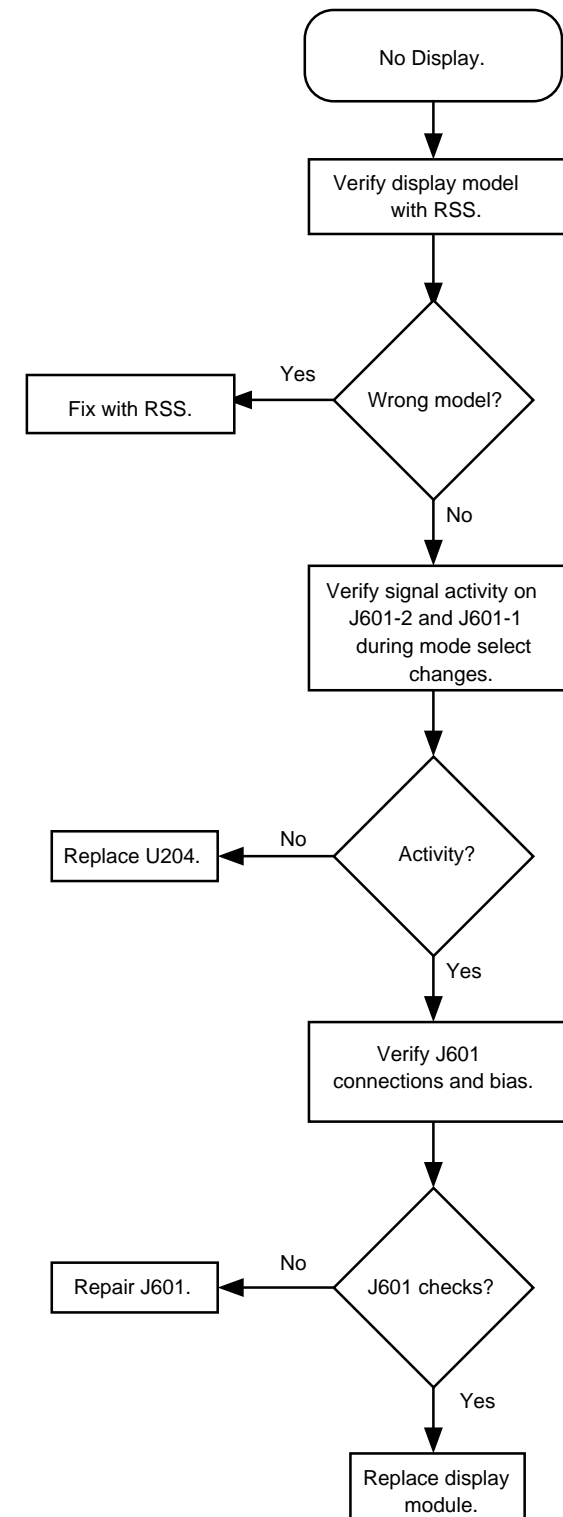


MAEPF-24400-A

Chart 24 . Top/Side Button Error

**Synopsis**  
 This chart relates to a failure in reading the buttons: Top, Top Side, Side Button 1, or Side Button 2. Basic Failure modes are as follows:  
 1) Failure in flex circuit consisting of R902, R903, R904, R201.  
 2) Bad connection.  
 3) Defective switch.  
 4) Defective A/D port in host  $\mu$ C.





MAEPF-24403-A

**Synopsis**  
 This chart relates to a failure in the display. The display is considered not field repairable and must be replaced as a unit. Basic Failure modes are as follows:  
 1) Non-display model radio.  
 2) Bad connection.  
 3) Defective  $\mu$ C.

Chart 25 . No Display

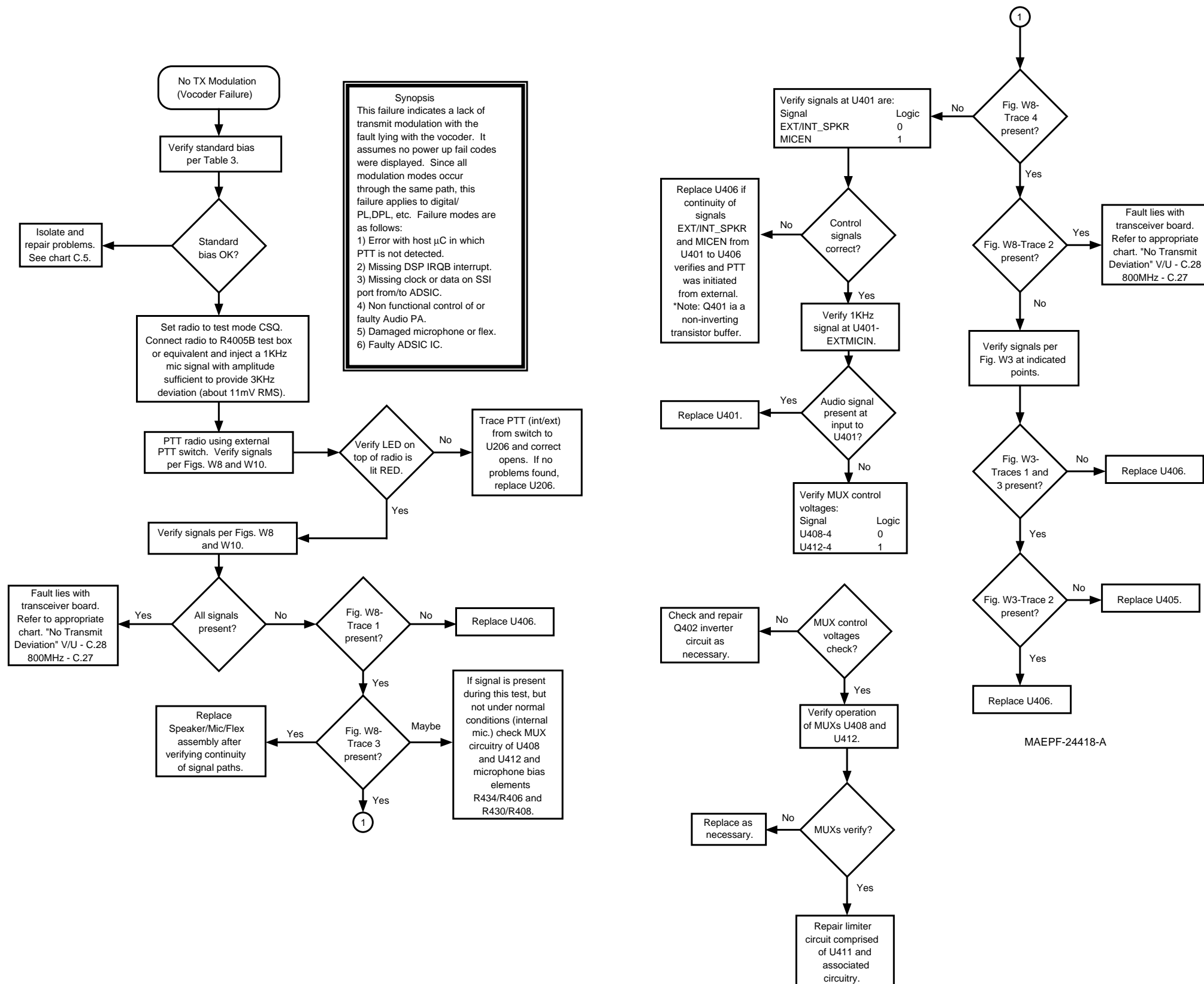
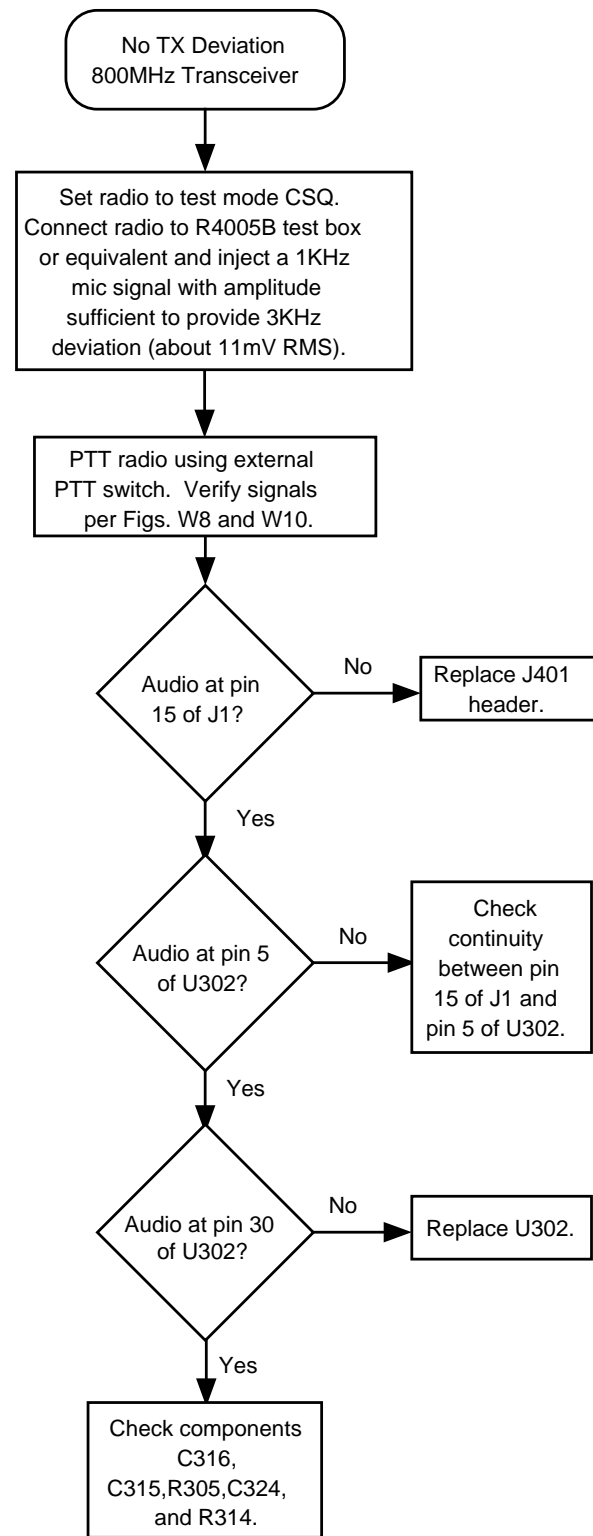
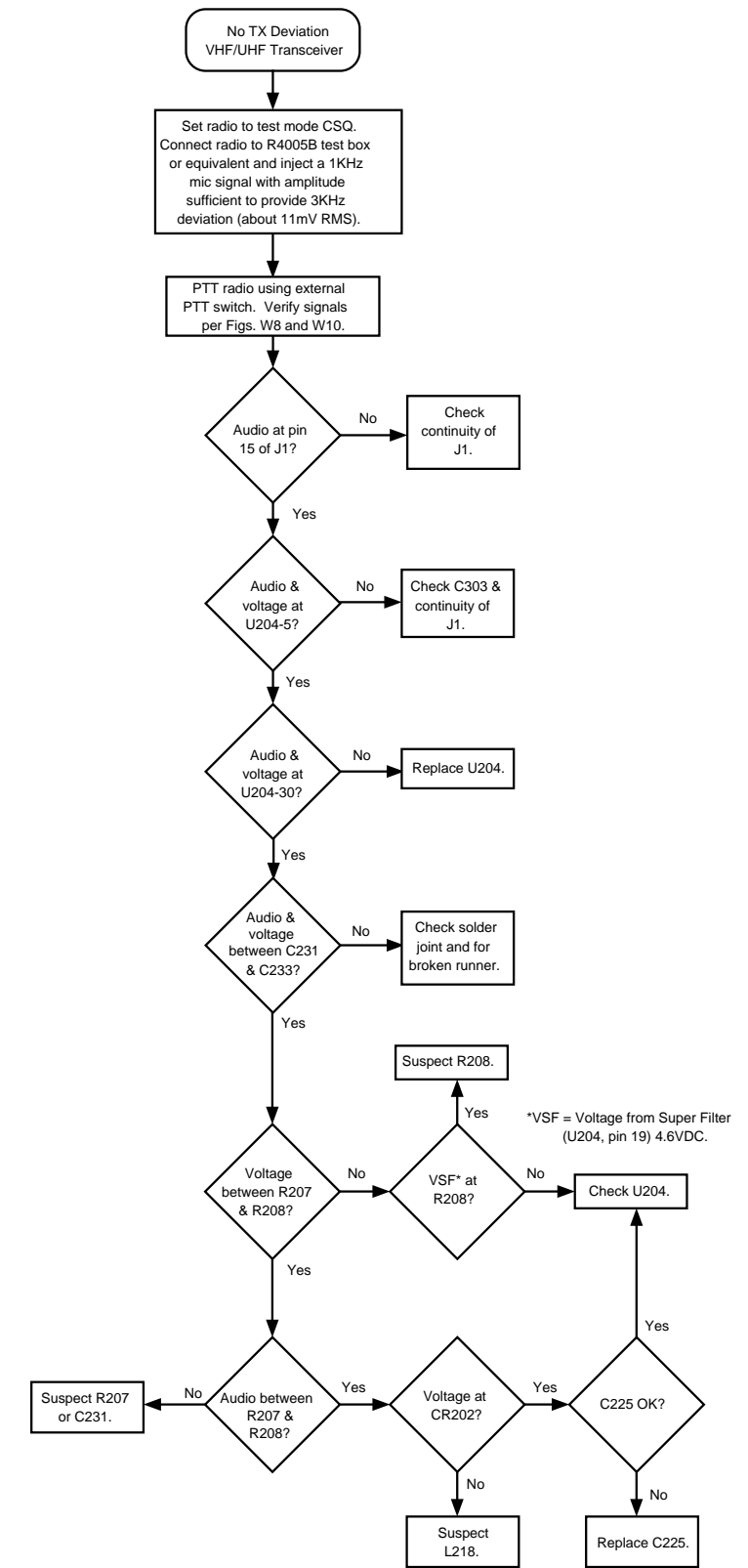


Chart 26 . No TX Modulation



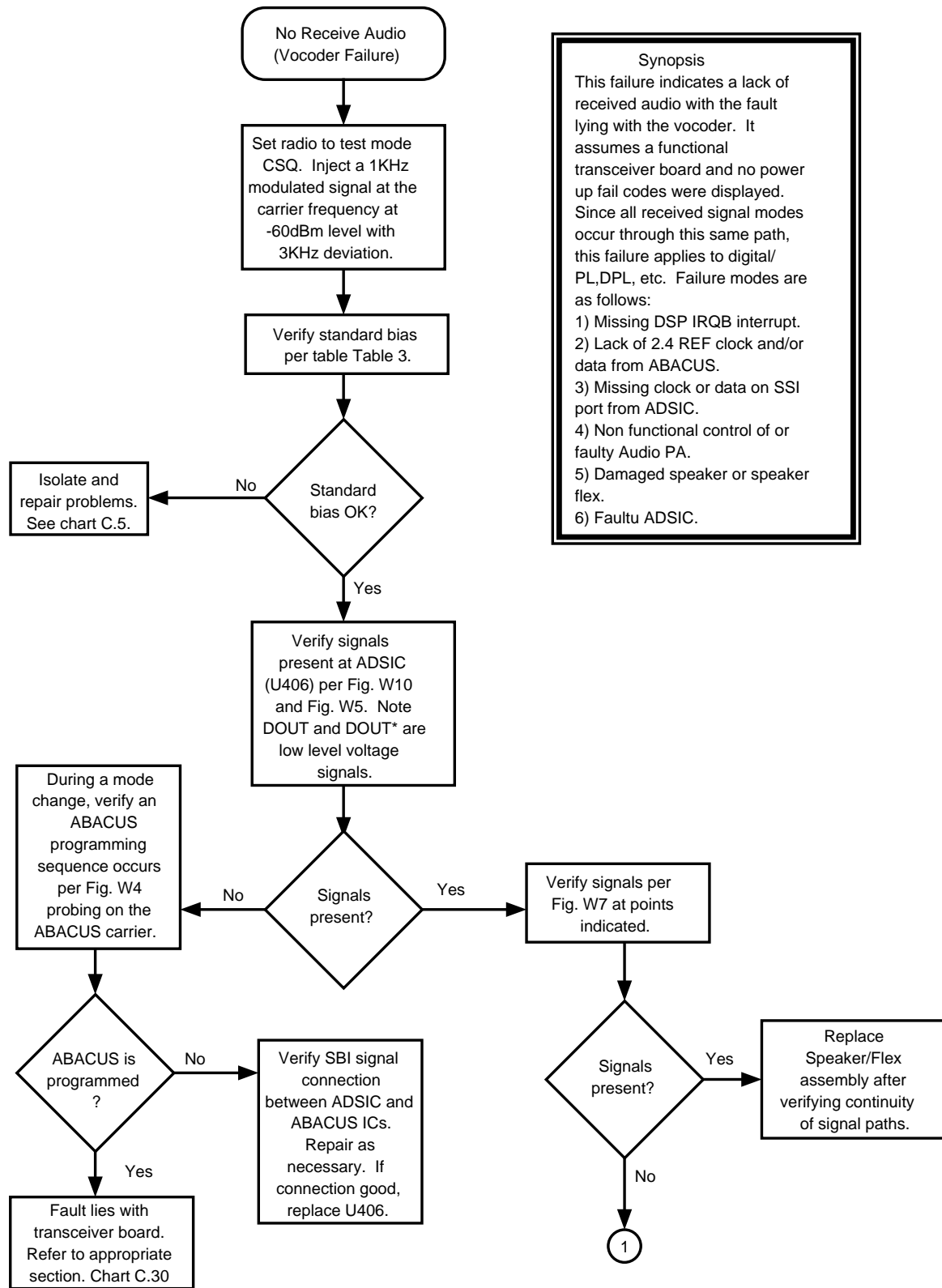
MAEPF-24405-O

Chart 27 . 800MHz No TX Deviation



MAEPF-24404-O

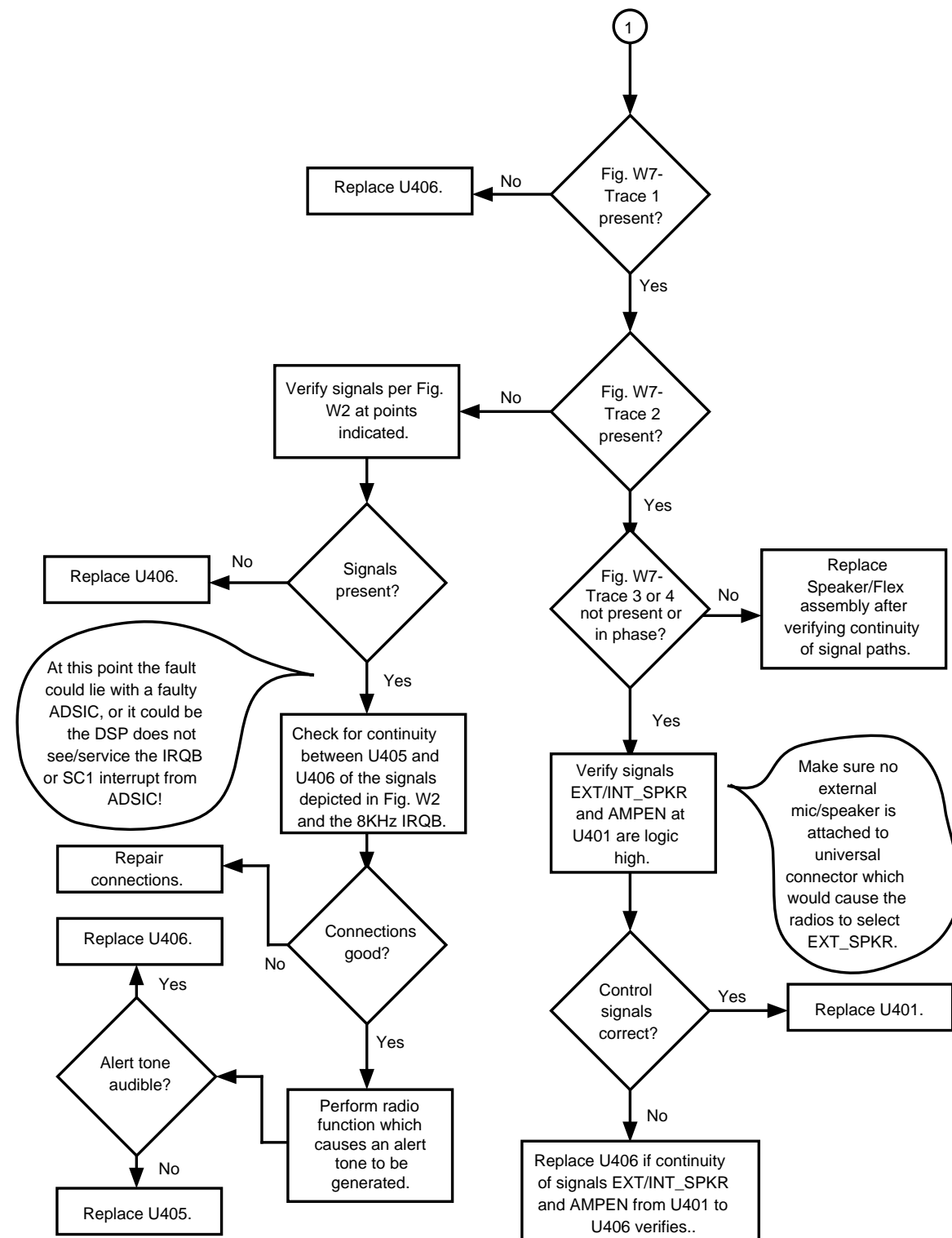
Chart 28 . VHF/UHF No TX Deviation



**Synopsis**

This failure indicates a lack of received audio with the fault lying with the vocoder. It assumes a functional transceiver board and no power up fail codes were displayed. Since all received signal modes occur through this same path, this failure applies to digital/ PL,DPL, etc. Failure modes are as follows:

- 1) Missing DSP IRQB interrupt.
- 2) Lack of 2.4 REF clock and/or data from ABACUS.
- 3) Missing clock or data on SSI port from ADSIC.
- 4) Non functional control of or faulty Audio PA.
- 5) Damaged speaker or speaker flex.
- 6) Faulty ADSIC.



MAEPF-24406-A

Chart 29 . No RX Audio

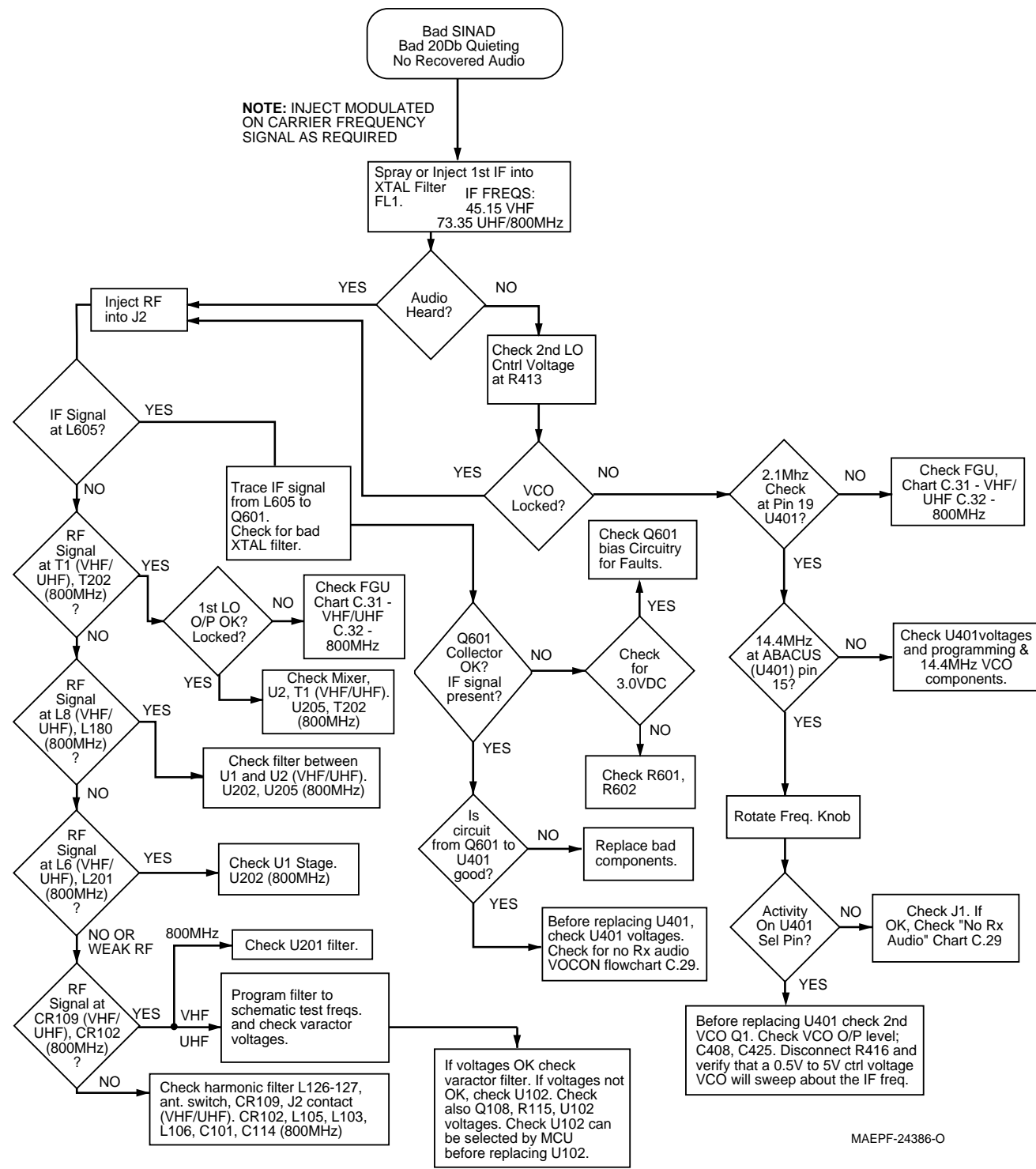


Chart 30 . VHF/UHF/800MHz Receiver RF

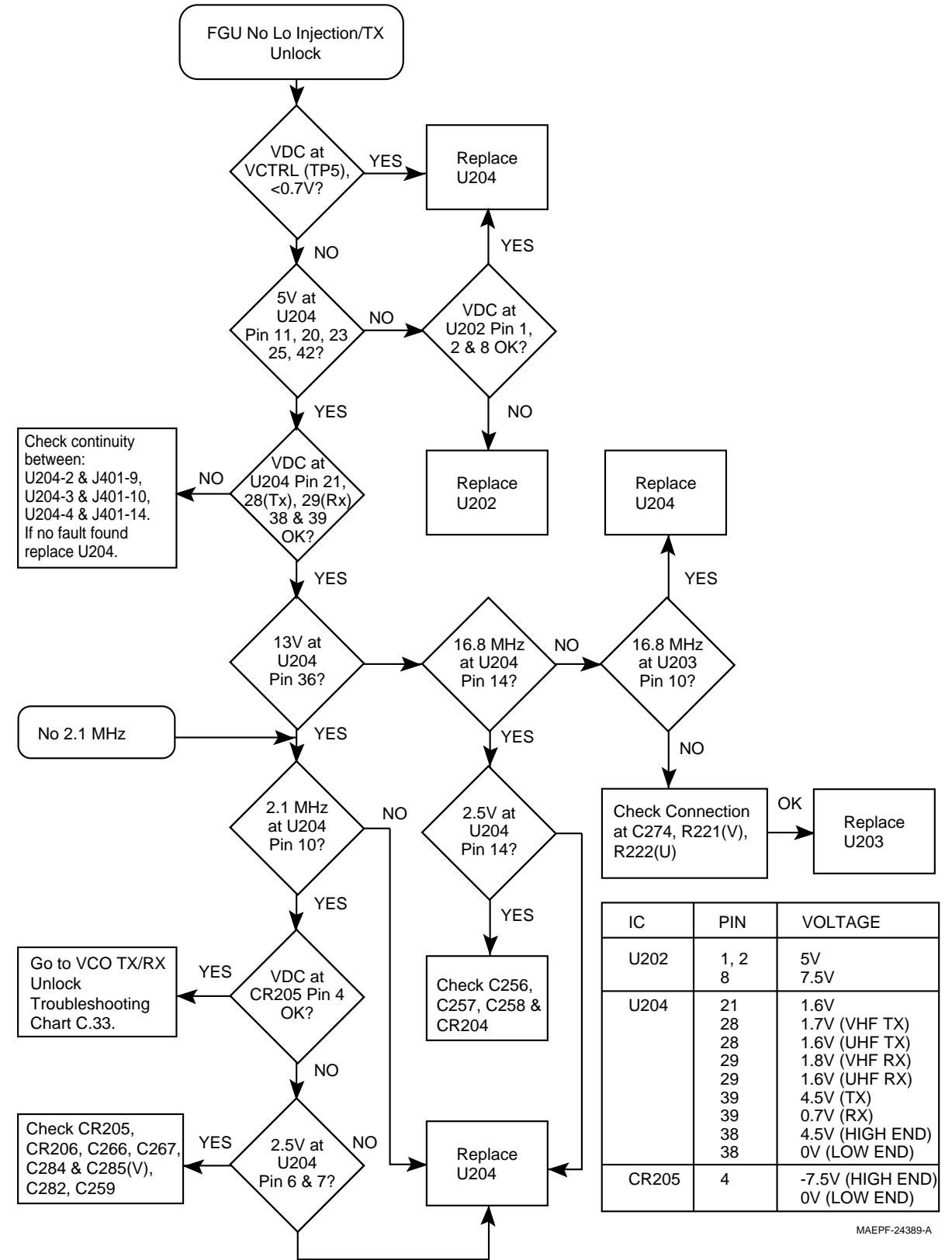
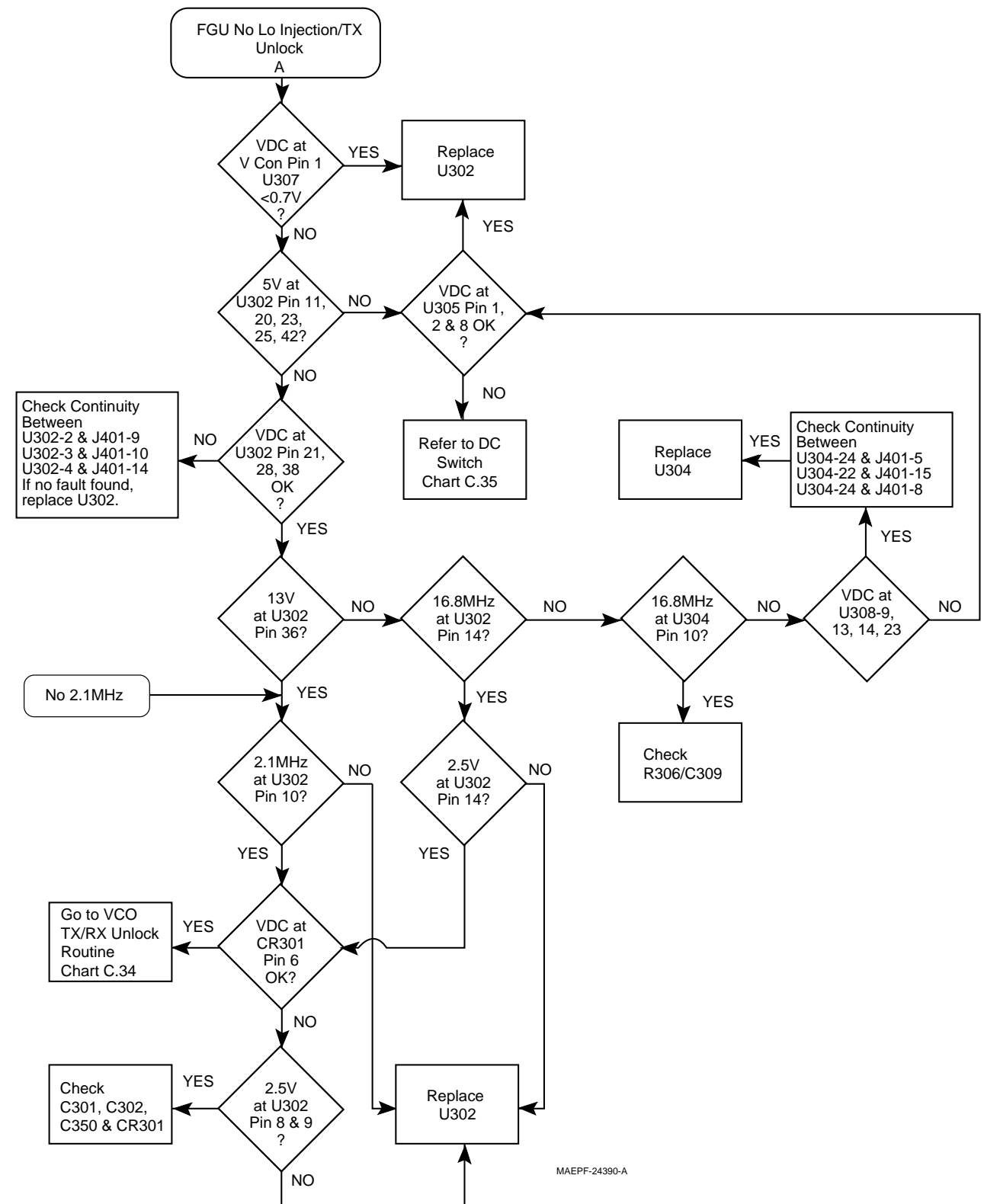
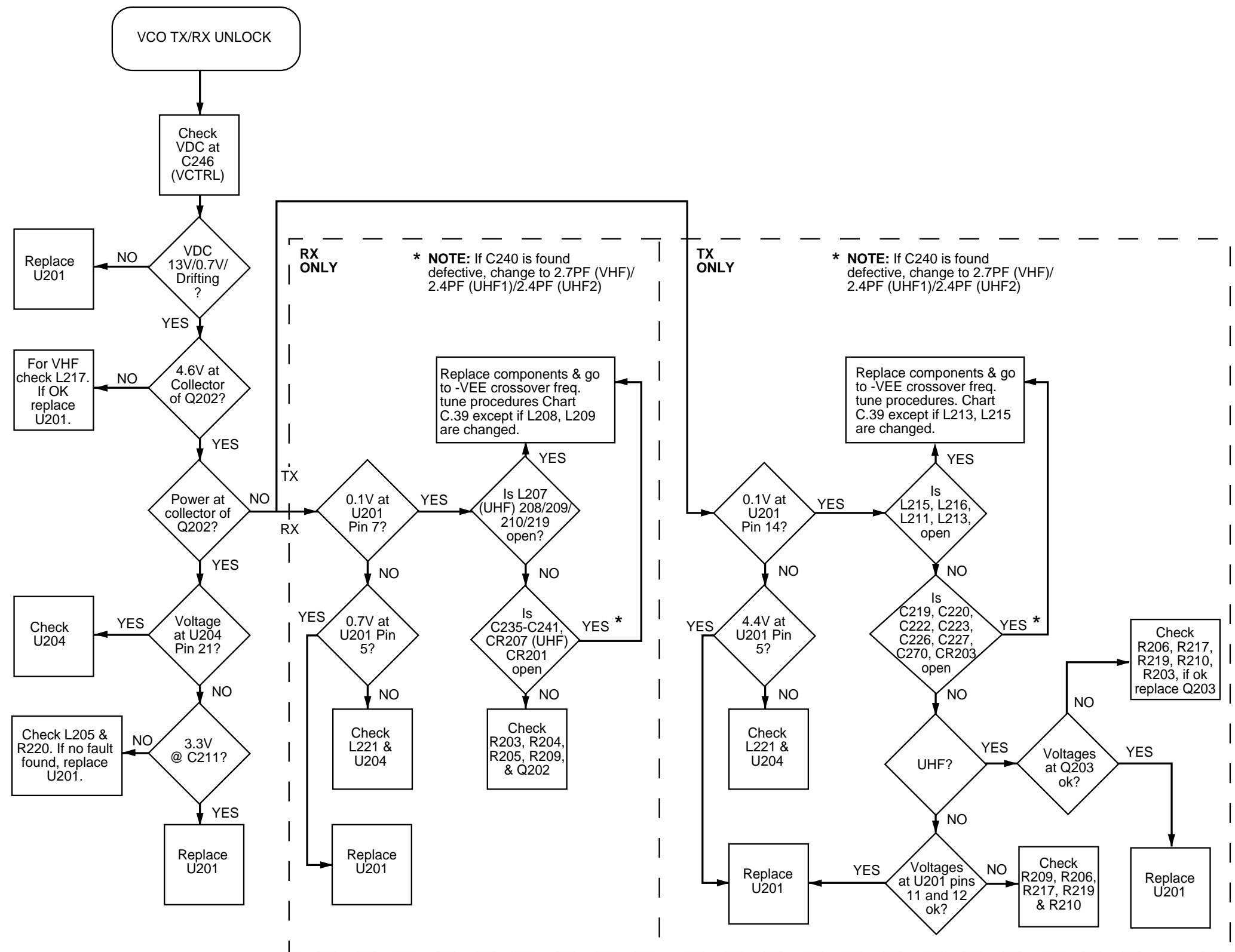


Chart 31 . VHF/UHF Frequency Generation Unit (FGU)



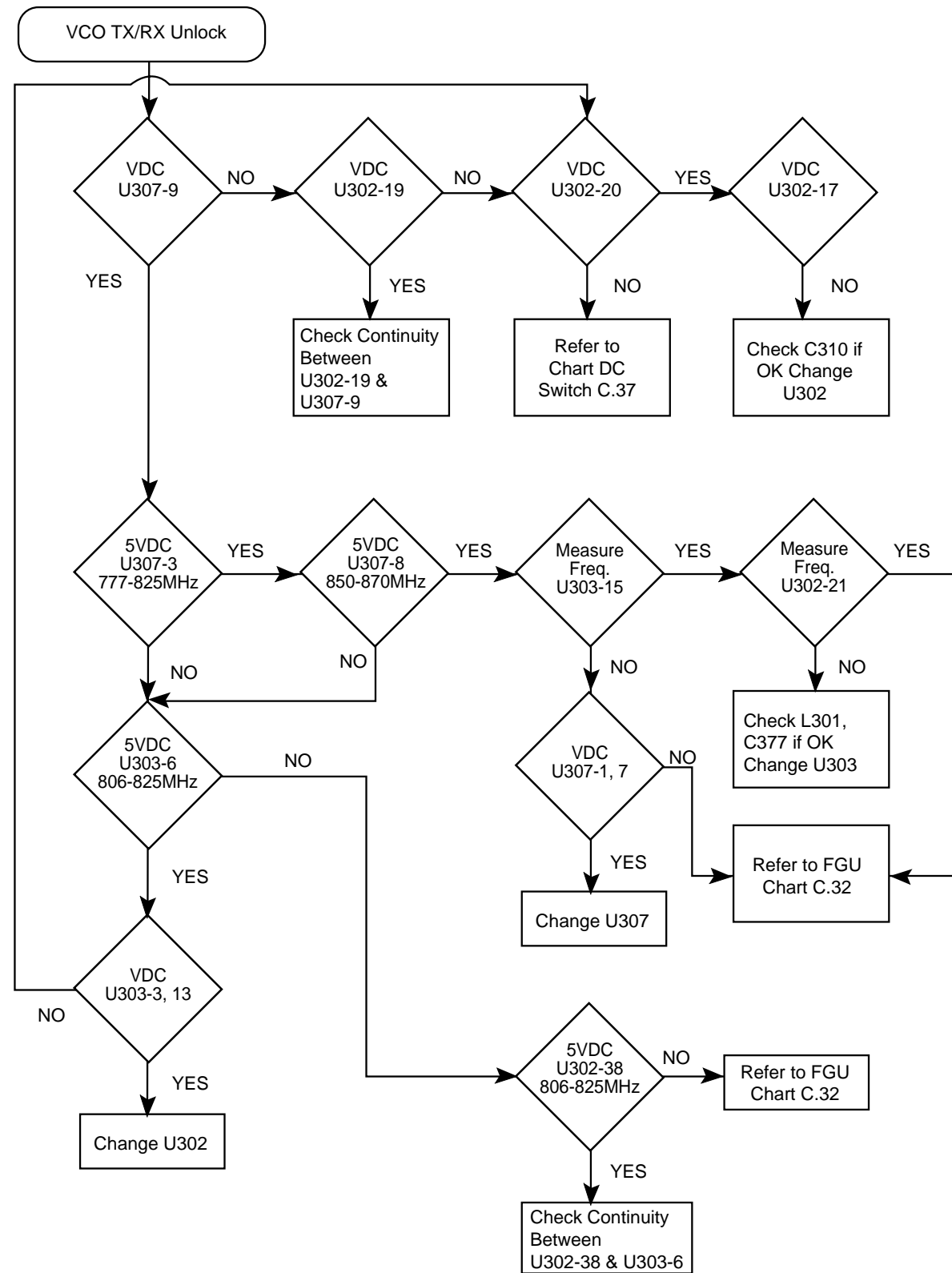
MAEPF-24390-A

Chart 32 . 800MHz Frequency Generation Unit (FGU)



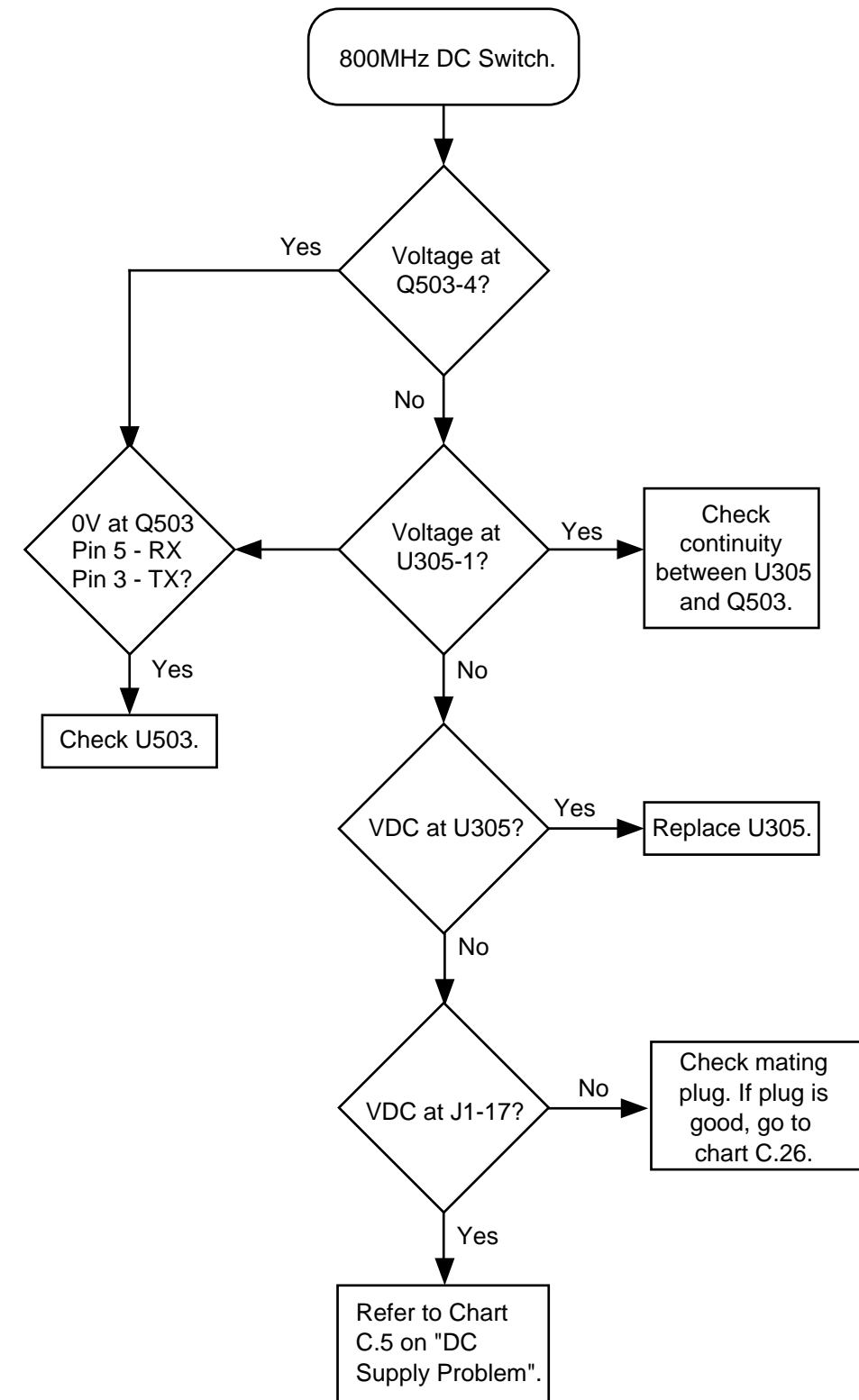
MAEPF-24387-A

Chart 33 . VHF/UHF Voltage Controlled Oscillator (VCO)



MAEPF-24388-A

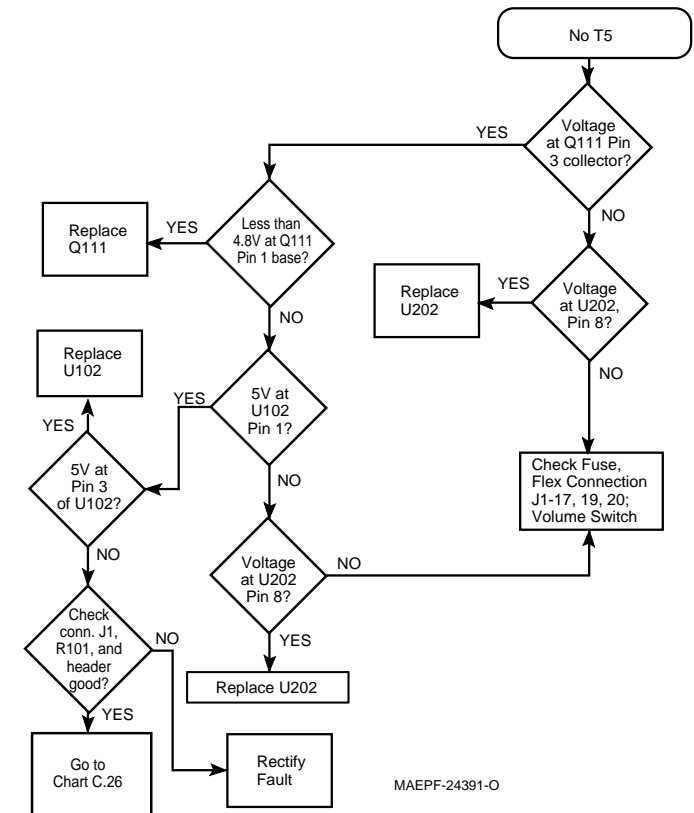
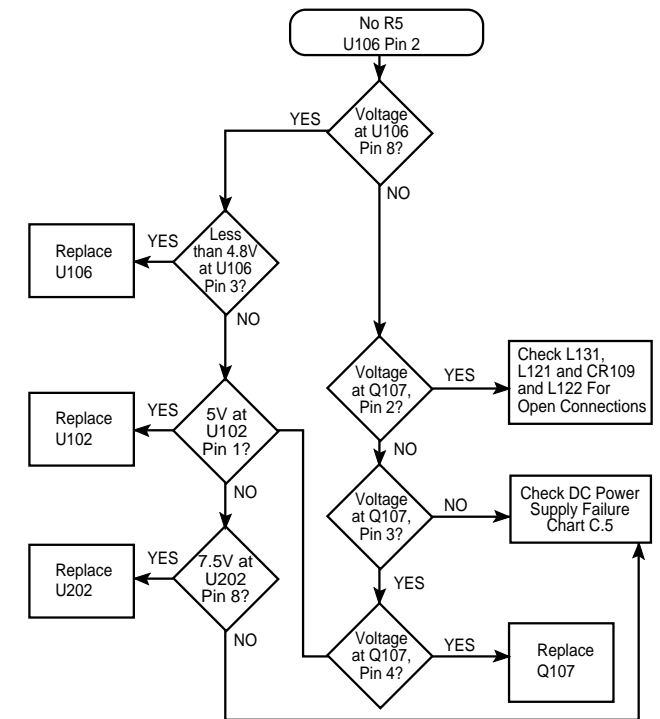
Chart 34 . 800MHz Voltage Controlled Oscillator (VCO)



MAEPF-24392-A

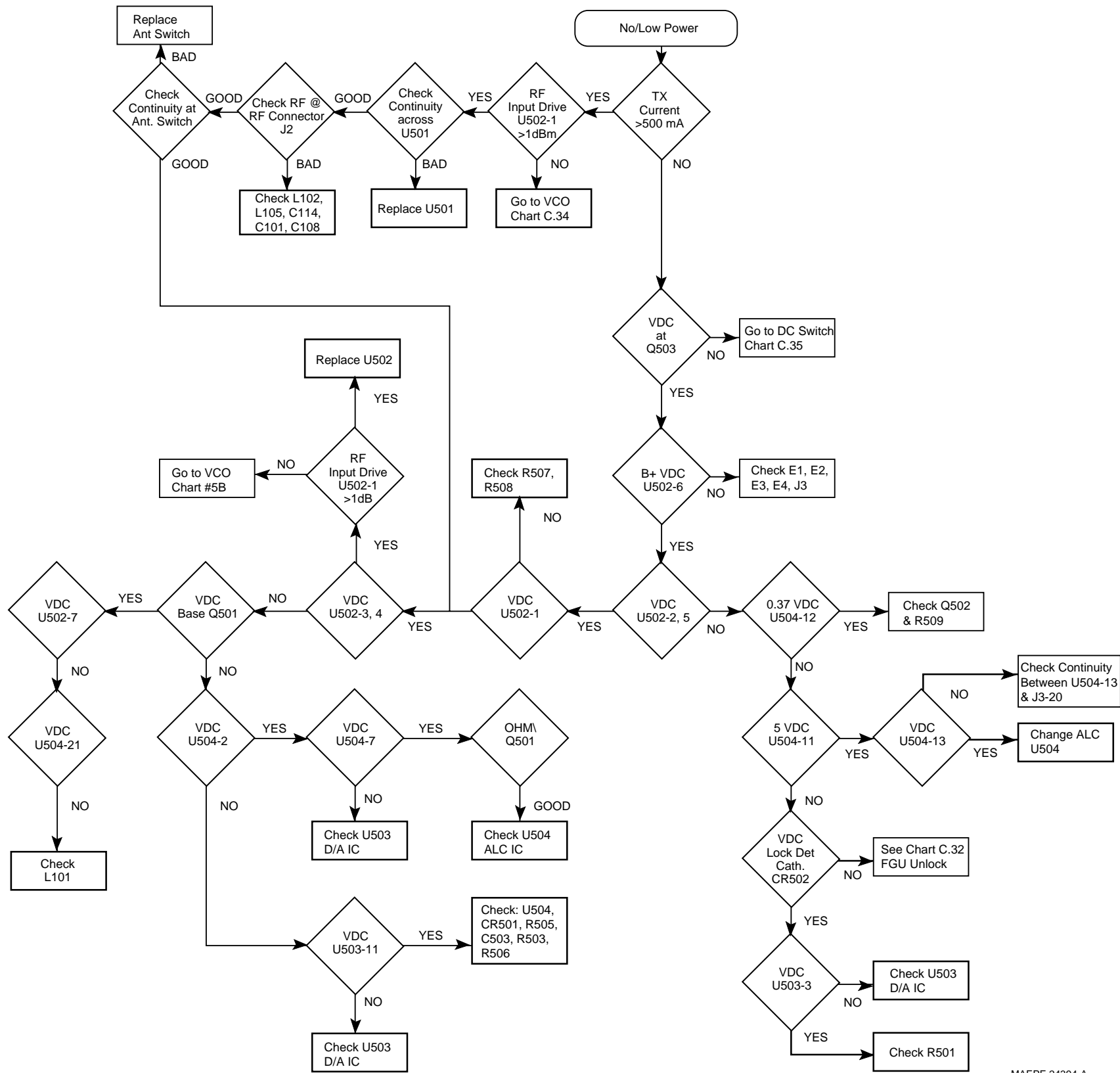
Chart 35 . 800MHz DC Switch





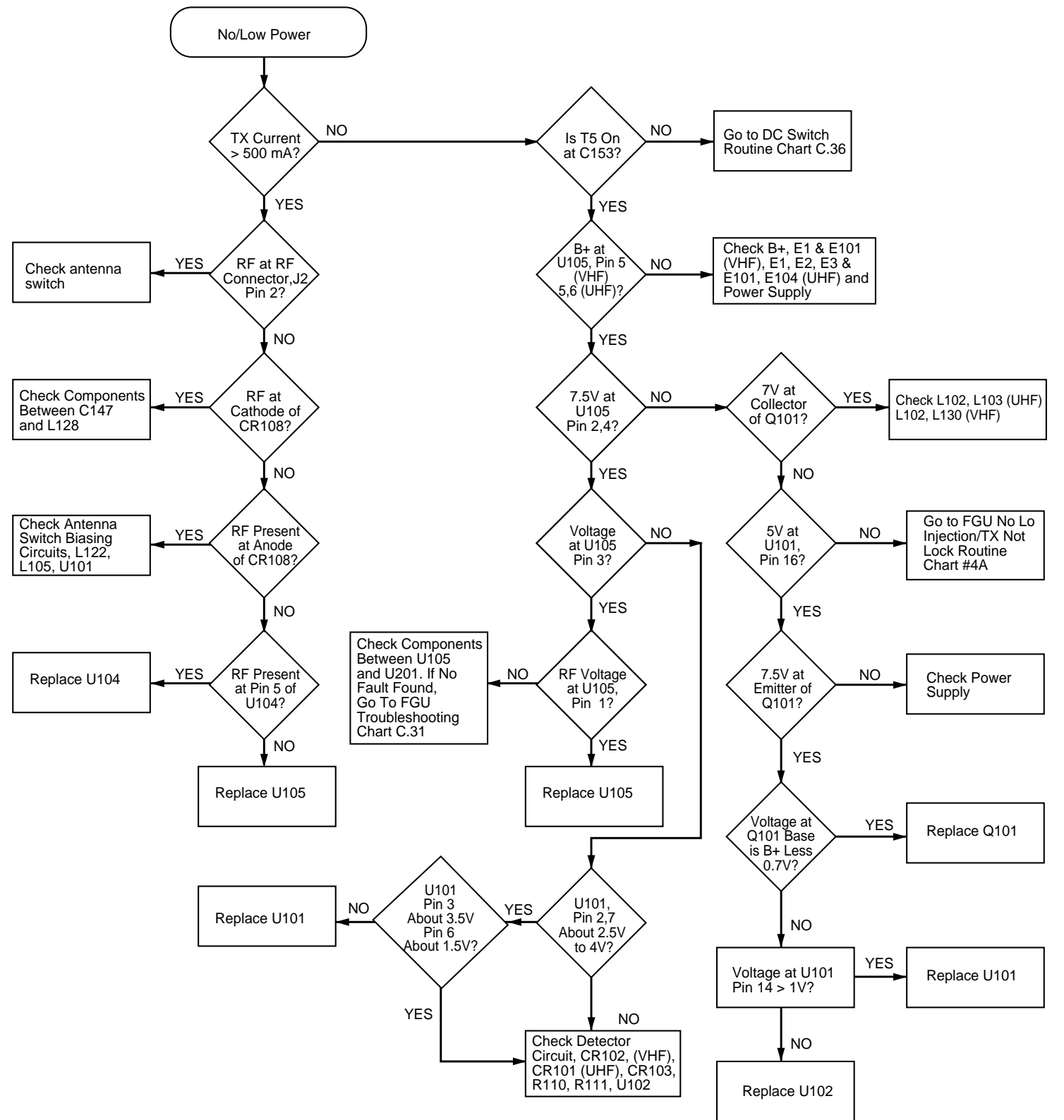
MAEPF-24391-O

Chart 36 . VHF/UHF DC Switch



MAEPF-24394-A

Chart 37 . 800MHz Transmitter RF



MAEPF-24393-O

Chart 38 . VHF/UHF Transmitter RF

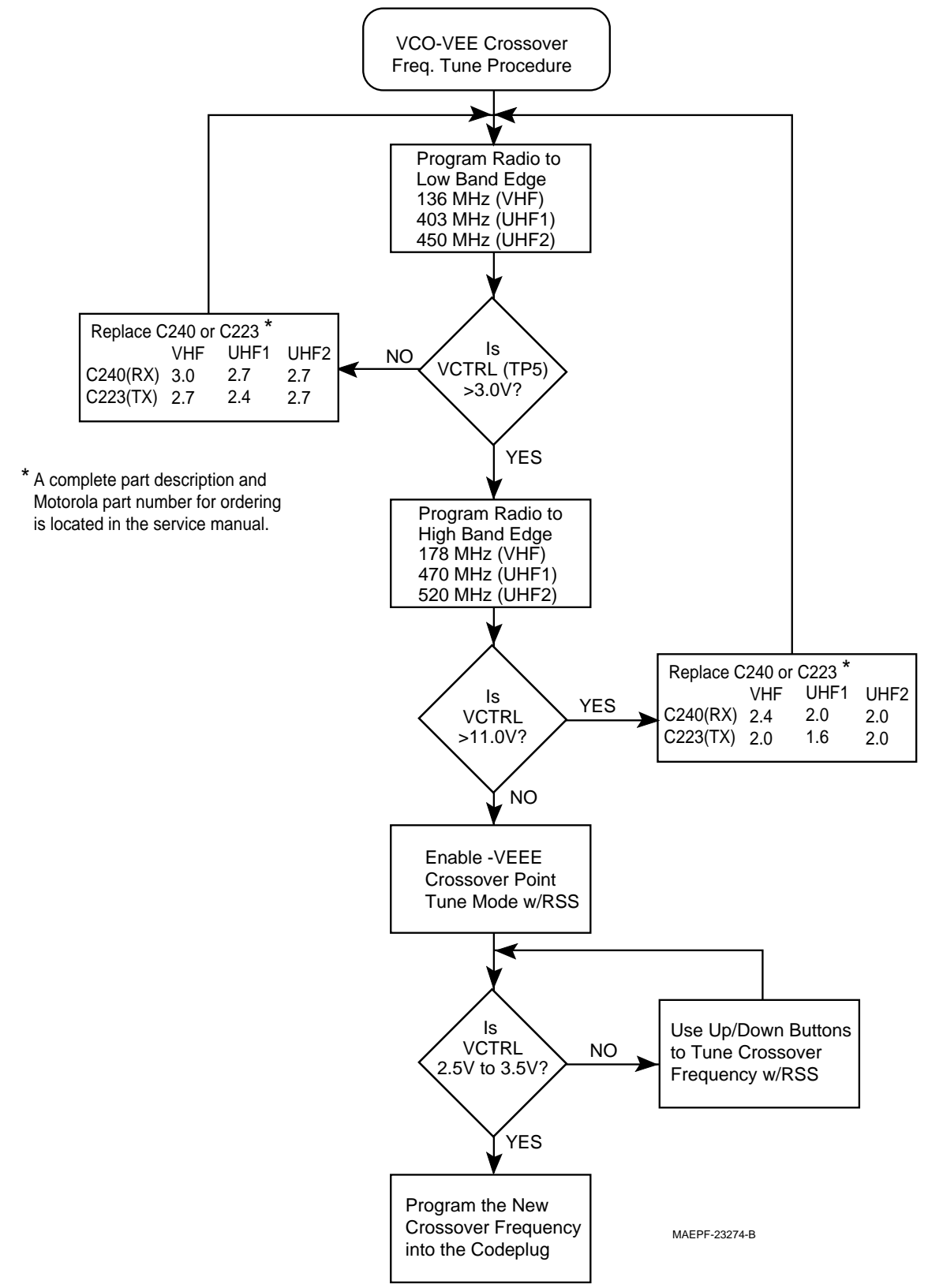
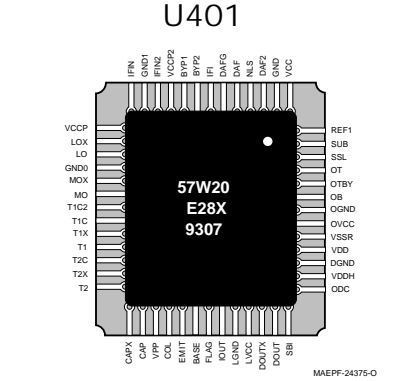
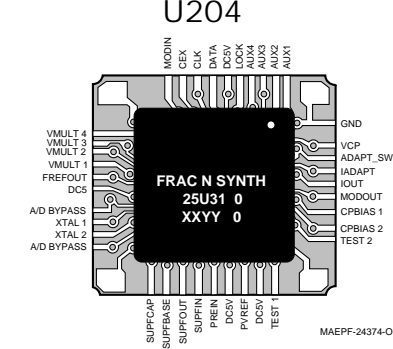
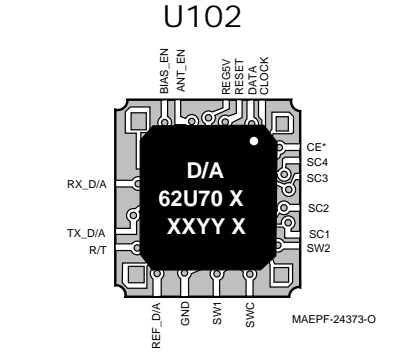
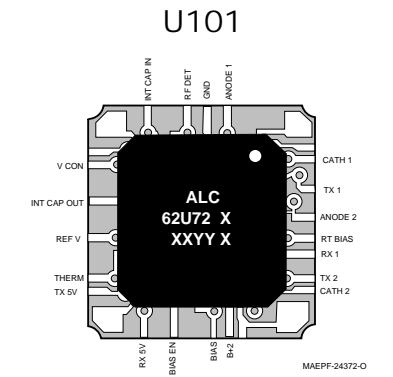
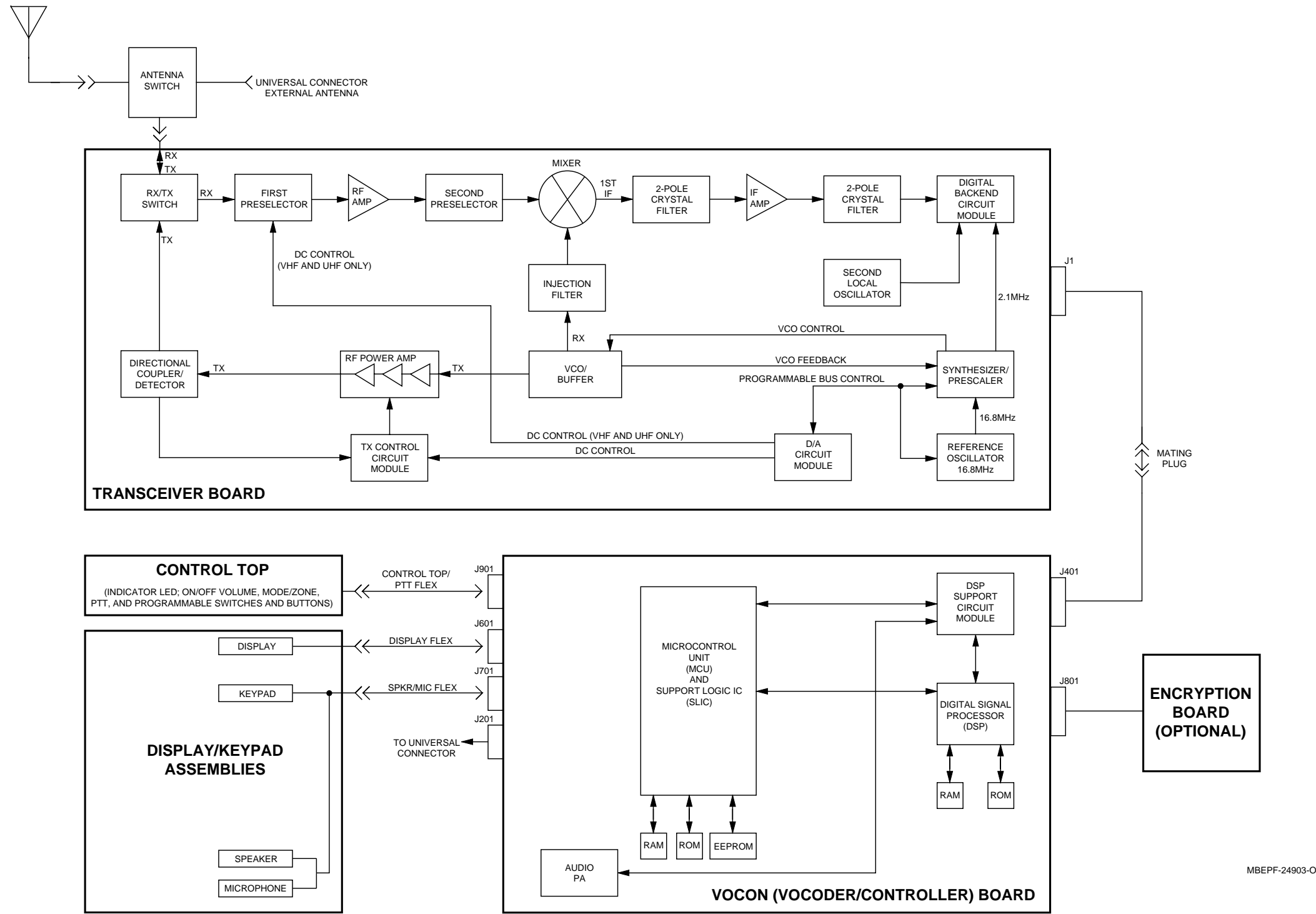


Chart 39 . VHF/UHF Only, VCO Crossover Frequency Tune

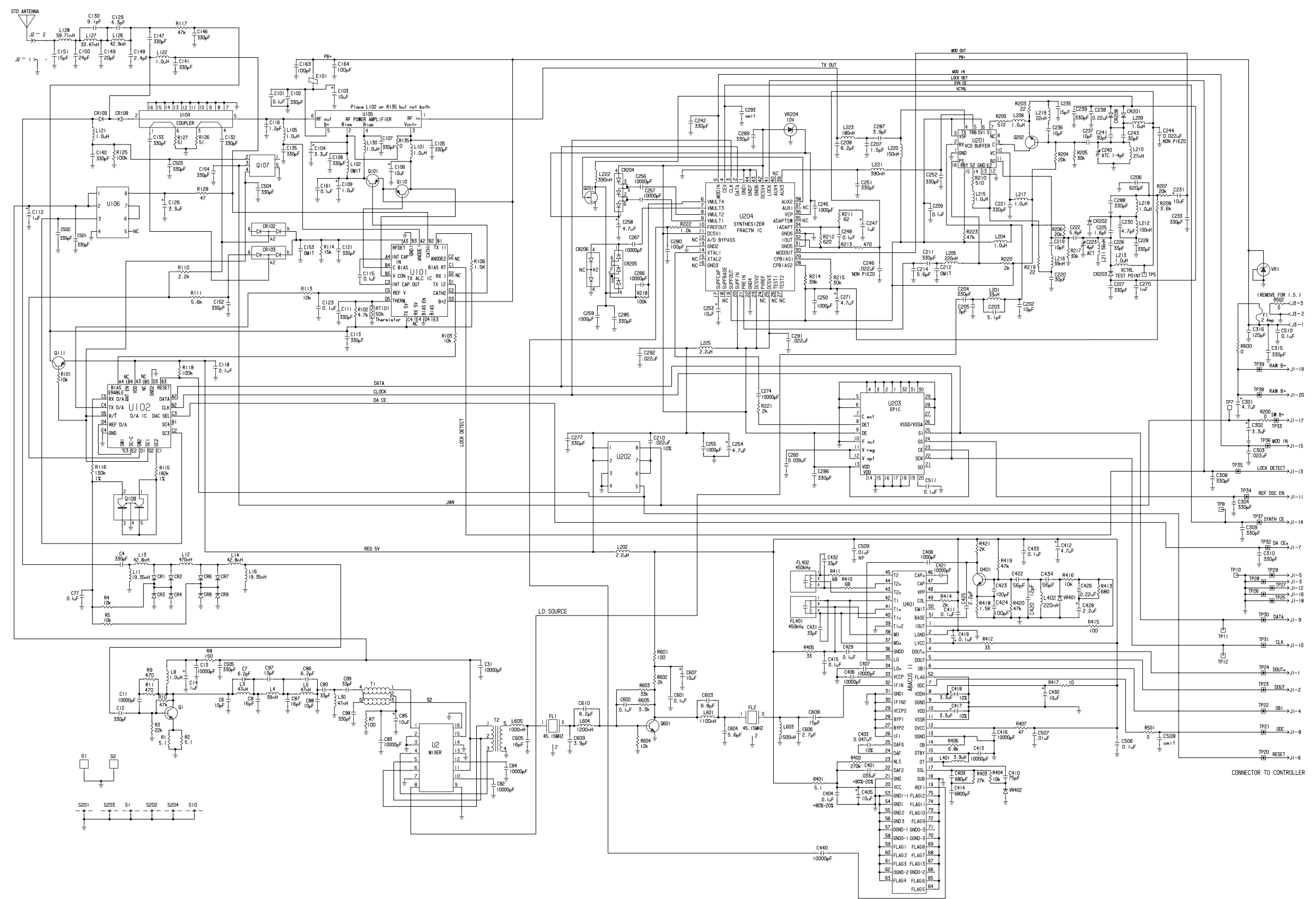
Block Diagrams, Schematics,  
Electrical Parts Lists,  
and Circuit Board Details

13

# Transceiver Board Integrated Circuit Modules



Radio Interconnect Diagram



63B81094C71-0

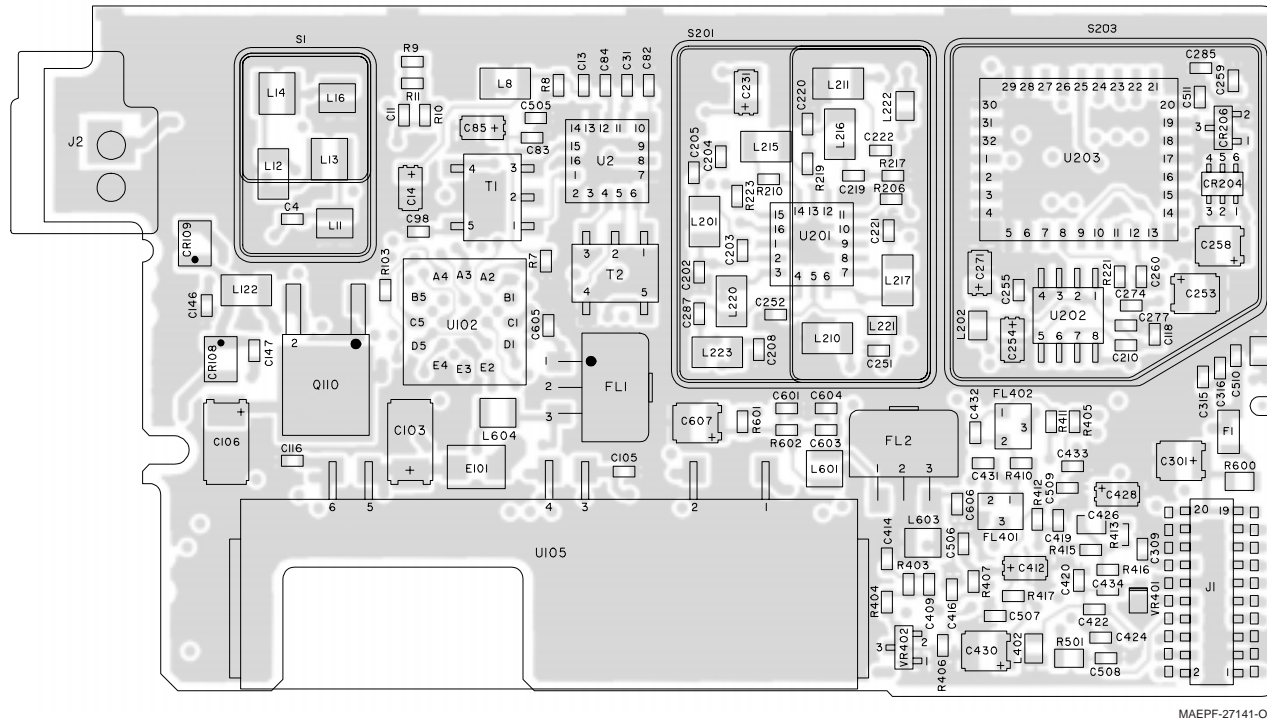
NLD8892R VHF Transceiver Board Schematic Diagram

NLD8892R VHF Transceiver Board  
Electrical Parts List

ITEM	MOTOROLA PART NUMBER	DESCRIPTION
		<b>CAPACITOR, Fixed: pF ±5%; 50V unless otherwise stated</b>
C4	2113931F13	330
C6	2113930F27	10
C7	2113930F22	6.2 pF 50V ±0.25 pF 50V
C8	2113930F32	16
C11	2113931F49	10 nF
C12	2113931F13	330
C13	2113931F49	10 nF
C14	2311049A07	1 uF
C31	2113931F49	10 nF
C77	2113932K15	0.1 uF +80/-20% 16V
C80	2113930F39	33 pF
C82 thru C84	2113931F49	10 nF
C85	2311049A60	10 uF
C86	2113930F22	6.2 pF 50V ±0.25 pF 50V
C87	2113930F32	16
C88	2113930F27	10
C97	2113740A32	13
C98	2113931F13	330
C99	2113930F39	33
C101	2113932K15	0.1 uF +80/-20% 16V
C102	2113931F13	330
C103	2311049J26	10 uF
C104	-----	Not Placed.
C105	2113931F13	330
C106	2311049J26	10 uF
C107	2113931F13	330
C108	-----	Not Placed.
C109	2311049A07	1 uF
C111	2113931F13	330
C112	2311049A07	1 uF
C113	2113931F13	330
C115	2113743A19	0.1 uF 10%
C116	2113930F05	1.2 pF 50V ±0.1 pF 50V
C118	2113932K15	0.1 uF +80/-20% 16V
C121	2113931F13	330
C123	2113932K15	0.1 uF +80/-20% 16V
C126	2311049A54	3.3 uF
C129	2113930F03	1.0 pF 50V ±0.1 pF 50V
C130	2113930F27	10
C132, C133	2113931F13	330
C135	2113931F13	330
C140, C141	2113931F13	330
C146, C147	2113931F13	330
C147	2113931F13	330
C148	2113930F03	1 pF 50V ±0.1 pF 50V
C149, C150	2113930F36	24
C151	2113930F29	12
C152	2113931F13	330
C153	-----	Not Placed.
C154	2113931F13	330
C161	2113932K15	0.1 uF +80/-20% 16V
C163, C164	2113930F51	100
C202	2113930F27	10
C203	2113930F20	5.1 pF 50V ±0.25 pF 50V
C204	2113931F13	330
C205	2113930F14	3 pF 50V ±0.25 pF 50V
C206	2113931F20	620
C207	2113930F07	1.5 pF 50V ±0.1 pF 50V
C208	2113930F22	6.2 pF 50V ±0.25 pF 50V

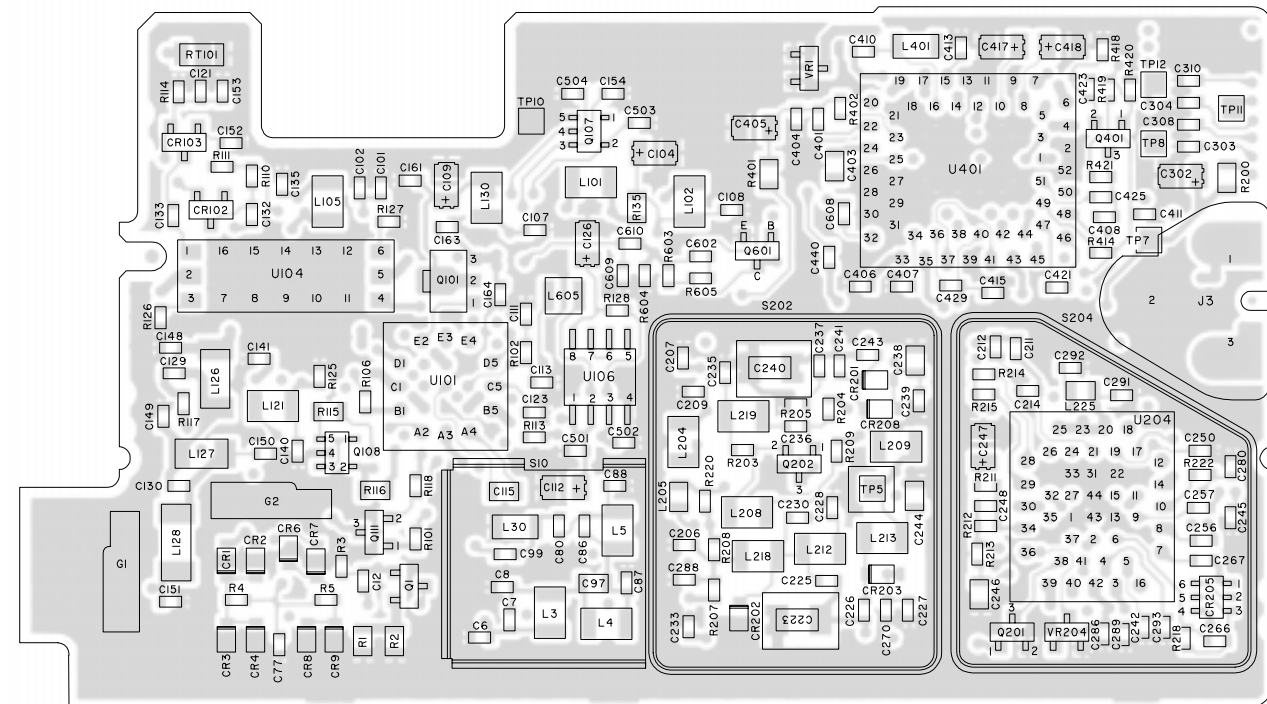
C209	2113932K15	0.1 uF +80/-20% 16V
C210	2113932E07	.022 uF 10% 16V
C211	2113931F13	330
C212	-----	Not Placed.
C214	2113930F21	5.6 pF 50V ±0.25 pF 50V
C219	2113930F27	10
C220	2113930F38	30
C221	2113931F13	330
C222	2113930F21	5.6 pF 50V ±0.25 pF 50V
C223	2113906C02	4 pF ATC
C225	2113930F08	1.6 pF 50V ±0.1 pF 50V
C226	2113930F39	33
C227, C228	2113931F13	330
C230	2113930F29	12
C231	2311049A60	10 uF
C233	2113931F13	330
C235	2113930F31	15
C236, C237	2113930F27	10
C238	2113743A23	0.22 uF 10%
C239	2113931F13	330
C240	2113906C02	4 pF ATC
C241	2113930F38	30
C242	2113931F13	330
C243	2113930F36	24
C244	2109720D09	.022 uF
C245	2113931F25	1 nF
C246	2109720D09	.022 uF
C247	2311049A07	1 uF
C248	2113932K15	0.1 uF +80/-20% 16V
C250	2113931F25	1 nF
C251, C252	2113931F13	330
C253	2311049J23	10 uF
C254	2311049A56	4.7 uF
C255	2113931F25	1 nF
C256, C257	2113931F49	10 nF
C258	2311049J11	4.7 uF
C259	2113931F25	1 nF
C260	2113932K05	.039 uF +80/-20% 16V
C266, C267	2113931F49	10 nF
C270	2113931F25	1 nF
C271	2311049A56	4.7 uF
C274	2113931F49	10 nF
C277	2113931F13	330
C280	2113930F51	100
C285, C286	2113931F13	330
C287	2113930F14	3 pF 50V ±0.25 pF 50V
C288, C289	2113931F13	330
C291, C292	2113932E03	.015 uF 10% 16V
C293	-----	Not Placed.
C301	2311049J11	4.7 uF
C302	2311049A54	3.3 uF
C303	2113932E03	.015 uF 10% 16V
C304	2113931F13	330
C308 thru C310	2113931F13	330
C315	2113931F13	330
C316	2113930F53	120
C401	2113932K03	.033 uF +80/-20% 16V
C403	2113743A13	.047 uF
C404	2113932K15	0.1 uF +80/-20% 16V
C405	2311049A60	10 uF
C406, C407	2113931F49	10 nF
C408	2113931F25	1 nF
C409	2113931F21	680
C410	2113930F48	75
C411	2113932K15	0.1 uF +80/-20% 16V

VIEWED FROM SIDE 1



MAEPF-27141-0

VIEWED FROM SIDE 2



MAEPF-27142-0



C412	2311049A03	0.22 uF
C413	2113931F49	10 nF
C414	2113931F45	6.8 nF
C415	2113932K15	0.1 uF +80/-20% 16V
C416	2113931F49	10 nF
C417, C418	2311049A42	3.3 uF
C419	2113932K15	0.1 uF +80/-20% 16V
C420	2113930F32	16
C421	2113931F49	10 nF
C422	2113930F45	56
C423, C424	2113930F51	100
C425	2113930F35	22
C426	2113743A23	0.22 uF 10%
C428	2311049A40	2.2 uF
C429	2113932K15	0.1 uF +80/-20% 16V
C430	2311049J23	10 uF
C431, C432	2113930F39	33
C433	2113932K15	0.1 uF +80/-20% 16V
C434	2113930F45	56
C440	2113931F49	10 nF
C501 thru C505	2113931F13	330
C506	2113932K15	0.1 uF +80/-20% 16V
C507	2113931F49	10 nF
C508	-----	Not Placed.
C509	2113931F49	10 nF
C510, C511	2113932K15	0.1 uF +80/-20% 16V
C601, C602	2113932K15	0.10 uF +80/-20% 16V
C603	2113930F23	6.8 pF 50V ±0.25 pF 50V
C604	2113930F21	5.6 pF 50V ±0.25 pF 50V
C605	2113930F32	16
C606	2113930F13	2.7 pF 50V ±0.25 pF 50V
C607	2311049J23	10 uF
C608	2113930F31	15
C609	2113930F17	3.9 pF 50V ±0.25 pF 50V
C610	2113930F22	6.2 pF 50V ±0.25 pF 50V
		<b>DIODE:</b> See Note 1.
CR1 thru CR4	4862824C01	Varactor
CR6 thru CR9	4862824C01	Varactor
CR102, CR103	4805129M67	Dual
CR108, CR109	4802482J02	PIN
CR201	4802245J29	Varactor
CR202, CR203	4862824C03	Varactor
CR204, CR205	4802233J09	Triple
CR206	4805129M06	Triple
CR208	4802245J29	Varactor
		<b>CORE:</b>
E101	2484657R01	Inductor Bead
		<b>FUSE:</b>
F1	6505757V02	2 Amp
		<b>FILTER:</b> See Note 2.
FL1, FL2	4805245J32	45.15 MHz
FL401, FL402	9105398W01	450 kHz
		<b>CONTACT:</b>
G1, G2	3905643V01	Antenna Ground
		<b>JACK:</b>
J1	0905461X03	Transceiver/VOCON Connector
J2	3905113W03	Antenna Connector
J3	3902625J04	B+ Contact
		<b>COIL, RF:</b>
L3	2462587T42	47 nH
L4	2462587T41	39 nH
L5	2462587T42	47 nH
L8	2462587T30	1 uH
L11	2460591M12	21.95 nH
L12	2462587T23	470 nH

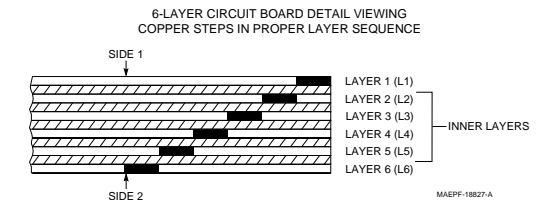
L13, L14	2460591N36	43.67 nH
L16	2460591M12	21.95 nH
L30	2462575A21	47 nH
L101	2462587T30	1 uH
L102	-----	Not Placed.
L105	2462587T30	1 uH
L121, L122	2462587T30	1 uH
L126	2460591H40	42.90 nH
L127	2460591G24	33.47 nH
L128	2460591K40	59.71 nH
L130	2462587T30	1 uH
L201	2462587T40	33 nH
L202	2462587Q20	2.2 uH
L204	2462587T30	1 uH
L205	2462587V38	220 nH
L208, L209	2462587T30	1 uH
L210	2462587T39	27 nH
L211	2462587T12	56 nH
L212	2462587T14	82 nH
L213	2462587T30	1 uH
L215	2462587T30	1 uH
L216	2462587T41	39 nH
L217, L218	2462587T30	1 uH
L219	2462587T38	22 nH
L220	2462587T17	150 nH
L221, L222	2462587Q42	390 nH
L223	2462587T16	120 nH
L225	2462587Q20	2.2 uH
L401	2462575A16	3.9 uH
L402	2462587V38	220 nH
L601	2405452C61	1.1 uH
L603	2405452C64	1.5 uH
L604	2405452C62	1.2 uH
L605	2405452C60	1 uH
		<b>TRANSISTOR:</b> See Note 1.
Q101	4805128M27	NPN
Q107	4805921T02	Switching
Q108	4802245J10	Dual NPN
Q110	4813822A10	PNP
Q111	4805128M16	PNP
Q201	4802245J15	JFET P-Channel
Q202	4805218N55	NPN
Q401	4805218N55	NPN
		<b>RESISTOR, Fixed: Ω±5%; 1/8W</b> Unless otherwise stated.
R1, R2	0660079U18	5.1
R3	0662057A81	22k
R4, R5	0662057A73	10k
R7	0662057A25	100
R8	0662057A29	150
R9	0662057A41	470
R10	0662057A89	47k
R11	0662057A41	470
R101	0662057A73	10k
R102	0662057A65	4.7k
R103	0662057A73	10k
R106	0662057A56	2k
R110	0662057A57	2.2k
R111	0662057A67	5.6k
R113	0662057A73	10k
R114	0662057A77	15k
R115	0662057G27	182k
R116	0662057G19	130k
R117	0662057A89	47k
R118	0662057A97	100k

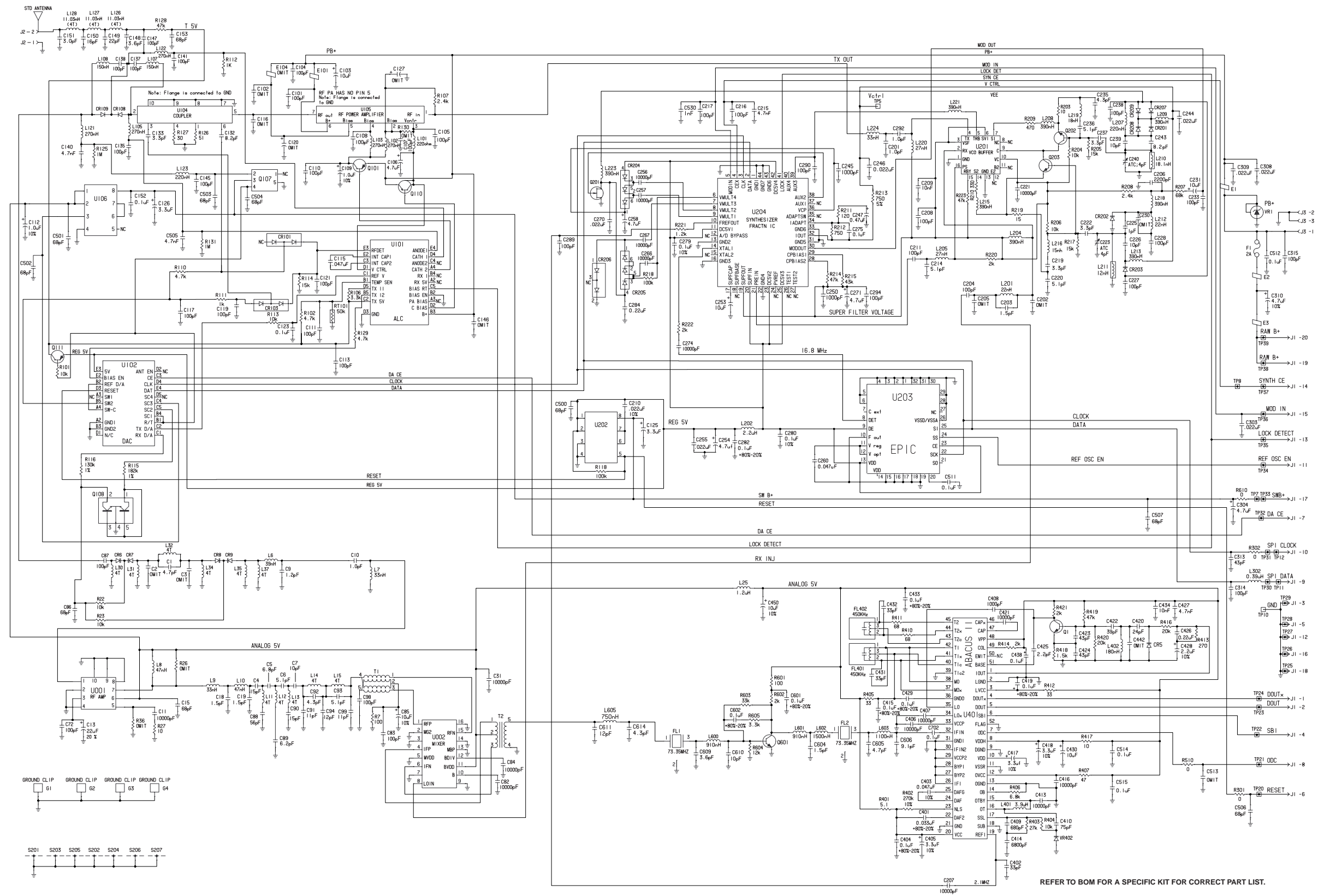
R125	0662057A97	100k
R126, R127	0662057A18	51
R128	0662057A17	47
R135	-----	Not Placed.
R200	0662057C01	0 ±.050
R203	0662057A09	22
R204	0662057A80	20k
R205	0662057A84	30k
R206	0662057A80	20k
R207	0662057A80	20k
R208	0662057A69	6.8k
R209, R210	0662057A42	510
R211	0662057A20	62
R212	0662057A44	620
R213	0662057A41	470
R214	0662057A87	39k
R215	0662057A84	30k
R217	0662057A84	30k
R218	0662057A97	100k
R219	0662057A09	22
R220, R221	0662057A56	2k
R222	0662057A49	1k
R223	0662057A89	47k
R401	0660079U18	5.1
R402	0662057B08	270k
R403	0662057A83	27k
R404	0662057A73	10k
R405	0662057A13	33
R406	0662057A69	6.8k
R407	0662057A17	47
R410, R411	0662057A21	68
R412	0662057A13	33
R413	0662057A45	680
R414	0662057A56	2k
R415	0662057A25	100
R416	0662057A73	10k
R417	0662057A01	10
R418	0662057A53	1.5k
R419, R420	0662057A89	47k
R421	0662057A56	2k
R501, R502	0662057C01	0 ±.05
R600	0662057C01	0 ±.05
R601	0662057A25	100
R602	0662057A56	2k
R603	0662057A85	33k
R604	0662057A75	12k
R605	0662057A61	3.3k
		<b>THERMISTOR:</b>
RT101	0605621T02	50k
		<b>SHIELD:</b>
S1	2602661J01	Varactor Filter
S010	2602815X01	Fixed Tuned Filter
S201	2602657J01	VCO
S202	2602674J02	VCO Back
S203	2602658J01	Pendulum
S204	2602675J01	Synthesizer, Back
		<b>TRANSFORMER:</b>
T1	2505515V08	4:1
T2	2505515V11	16:1
		<b>INTEGRATED CIRCUIT MODULE:</b> See Note 1.
U2	5105329V26	Mixer
U101	5105835U52	TX (ALC)
U102	5105835U51	D/A Converter
U104	5102001J69	Coupler

U105	5105385Y36	RF Power Amplifier
U106	5105469E65	5 Volt Regulator
U201	5102227J37	VCO Buffer
U202	5105469E65	5 Volt Regulator
U203	5105385Y42	16.8 MHz Reference Oscillator
U204	5105457W81	Fractional-N-Synthesizer
U401	5105835U90	ABACUS
		<b>DIODE:</b> See Note 1.
VR001	4813830A33	Zener, 20V
VR204	-----	Not Placed.
VR401	4862824C01	Varactor
VR402	4805129M58	Varactor

**Notes:**

- For optimum performance, order replacement diodes, transistors, and circuit modules by Motorola part number only.
- When ordering crystals, specify carrier frequency, crystal frequency, crystal type number, and Motorola part number.
- Part value notations:  
 $p=10^{-12}$   
 $n=10^{-9}$   
 $\mu=10^{-6}$   
 $m=10^{-3}$   
 $k=10^3$   
 $M=10^6$
- ITEM refers to the component reference designator.
- The VHF Transceiver Board uses a 6-layer printed circuit board.

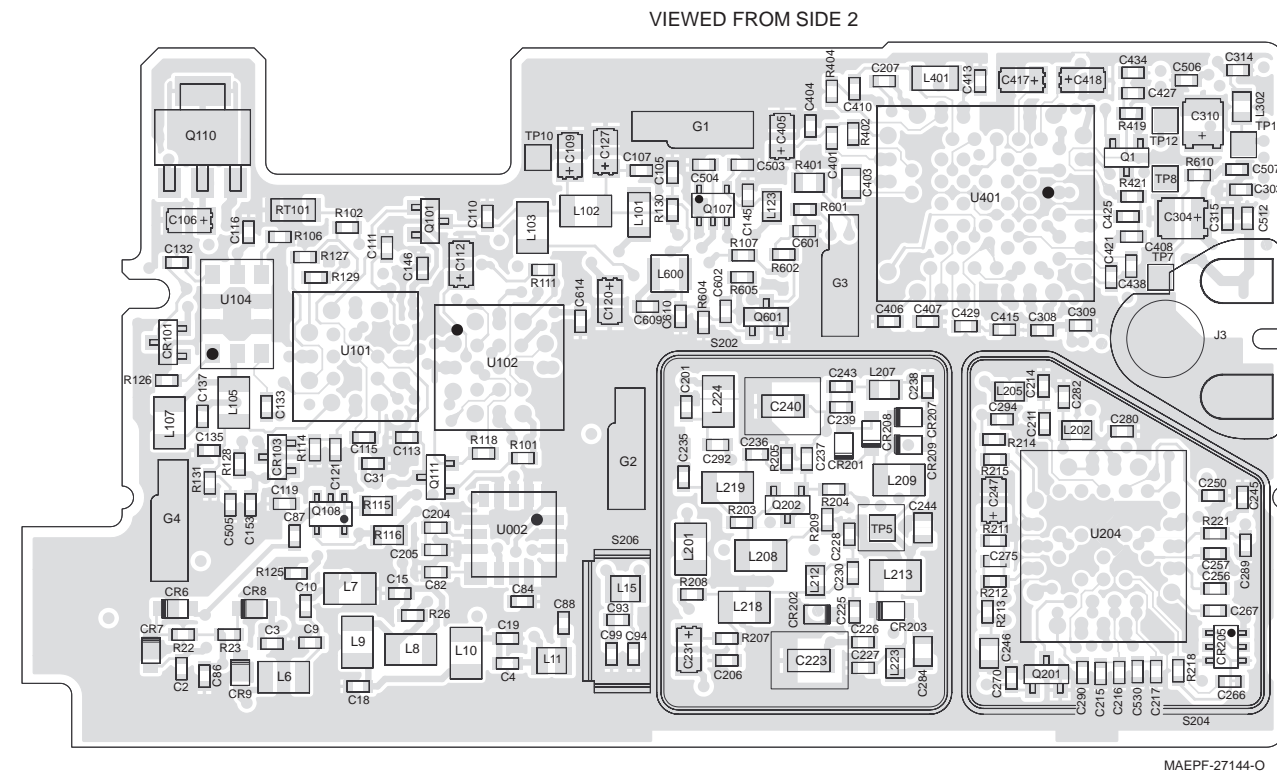
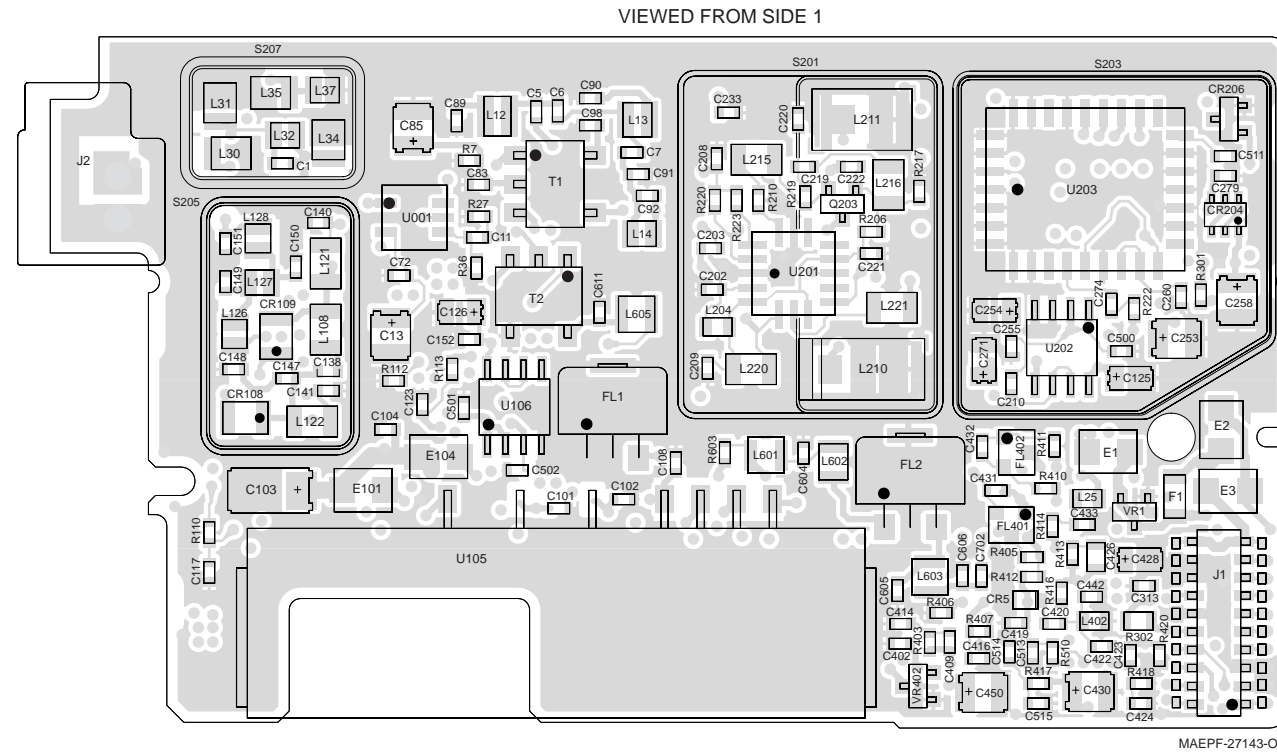




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NLE4560K UHF Range 1 Transceiver Board Schematic Diagram

NLE4560K UHF Range 1 Transceiver Board  
Electrical Parts List



NLE4560K UHF Range 1 Transceiver Circuit Board Details and Parts List

ITEM	MOTOROLA PART NUMBER	DESCRIPTION
		<b>CAPACITOR, Fixed: pF ±5%; 50V unless otherwise stated</b>
C1	2113930F19	4.7 pF 50V ±0.25 pF 50V
C2, C3	-----	Not Placed.
C4	2113930F31	15
C5	2113930F23	6.8 pF 50V ±0.25 pF 50V
C6	2113930F20	5.1 pF 50V ±0.25 pF 50V
C7	2113930F27	10
C9	2113930F05	1.2 pF 50V ±0.1 pF 50V
C10	2113930F03	1.0 pF 50V ±0.1 pF 50V
C11	2113931F49	.01 uF
C13	2311049A66	22 uF
C15	2113930F47	68 pF
C18, C19	2113930F07	1.5 pF 50V ±0.1 pF 50V
C31	2113931F49	.01 uF
C72	2113930F51	100
C82	2113931F49	.01 uF
C83	2113930F51	100
C84	2113931F49	.01 uF
C85	2311049J23	10 uF
C86	2113930F47	68 pF
C87	2113930F51	100
C88	2113930F45	56
C89	2113930F22	6.2 pF 50V ±0.25 pF 50V
C90	2113930F31	15
C91	2113930F28	11
C92	2113930F18	4.3 pF 50V ±0.25 pF 50V
C93	2113930F20	5.1 pF 50V ±0.25 pF 50V
C94	2113930F29	12
C098	2113930F51	100
C099	2113930F28	11
C101	2113930F51	100
C102	-----	Not Placed.
C103	2311049J26	10 uF
C104, C105	2113930F51	100
C106	2311049A56	4.7 uF
C107, C108	2113930F51	100
C109	2311049A07	1 uF
C110, C111	2113930F51	100
C112	2311049A07	1 uF
C113	2113930F51	100
C115	2113932K07	.047 uF +80/-20% 16V
C116	-----	Not Placed.
C117, C119	2113930F51	100
C120	-----	Not Placed.
C121	2113930F51	100
C123	2113932K15	0.1 uF +80/-20% 16V
C125, C216	2311049A54	3.3 uF
C127	-----	Not Placed.
C132	2113930F25	8.2 pF 50V ±0.25 pF 50V
C133	2113930F15	3.3 pF 50V ±0.25 pF 50V
C135	2113930F51	100
C137, C138	2113930F51	100
C140	2113931F41	4.7 nF
C141	2113930F51	100
C145	2113930F51	100
C146	-----	Not Placed.
C147	2113930F51	100
C148	2113930F16	3.6 pF 50V ±0.25 pF 50V
C149	2113930F35	22
C150	2113930F32	16
C151	2113930F14	3.0 pF 50V ±0.25 pF 50V
C152	2113932K15	0.1 uF +80/-20% 16V

C153	2113930F47	68
C201	2113930F03	1 pF 50V ±0.1 pF 50V
C202	-----	Not Placed.
C203	2113930F07	1.5 pF 50V ±0.1 pF 50V

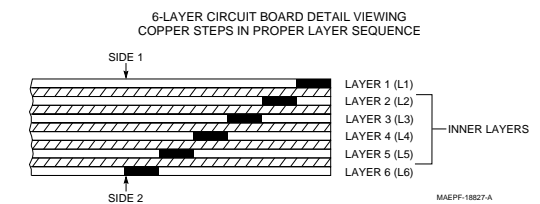
C408	2113931F25	1 nF
C409	2113931F21	680
C410	2113930F48	75
C413	2113931F49	10 nF
C414	2113931F45	6.8 nF
C415	2113932K15	0.1 uF +80/-20% 16V
C416	2113931F49	10 nF
C417, C418	2311049A42	3.3 uF
C419	2113932K15	0.1 uF +80/-20% 16V
C420	2113930F36	24
C421	2113931F49	10 nF
C422	2113930F41	39
C423, C424	2113930F42	43
C425	2113930F11	2.2 pF 50V ±0.25 pF 50V
C426	2113743A23	0.22 uF 10%
C427	2113931F41	4.7 nF
C428	2311049A40	2.2 uF
C429	2113932K15	0.1 uF +80/-20% 16V
C430	2311049J23	10 uF
C431, C432	2113930F39	33
C433	2113932K15	0.1 uF +80/-20% 16V
C434	2113931F49	10 nF
C438	2113932K15	0.1 uF +80/-20% 16V
C442	-----	Not Placed.
C450	2311049J23	10 uF
C500 thru C504	2113930F47	68
C505	2113931F41	4.7 nF
C506, C507	2113930F47	68
C511, C512	2113932K15	0.1 uF +80/-20% 16V
C513	-----	Not Placed.
C514, C515	2113932K15	0.1 uF +80/-20% 16V
C530	2113931F25	1
C601, C602	2113932K15	0.1 uF +80/-20% 16V
C604	2113930F07	1.5 pF 50V ±0.1 pF 50V
C605	2113930F19	4.7 pF 50V ±0.25 pF 50V
C606	2113930F26	9.1 pF 50V ±0.25 pF 50V
C609	2113930F16	3.6 pF 50V ±0.25 pF 50V
C610	2113930F27	10
C611	2113930F29	12
C614	2113930F18	4.3 pF 50V ±0.25 pF 50V
C702	2113932K15	0.1 uF +80/-20% 16V DIODE: See Note 1.
CR5 thru CR9	4862824C01	Varactor
CR101	4805129M67	Dual
CR103	4805129M67	Dual
CR108, CR109	4802482J02	PIN
CR201	4802245J29	Varactor
CR202	4862824C01	Varactor
CR203	4862824C03	Varactor
CR204, CR205	4802233J09	Triple
CR206	4805129M06	Triple
CR207 thru CR209	4802245J29	Varactor
E1 thru E3	2484657R01	Inductor Bead
E101	2484657R01	Inductor Bead
E104	2484657R01	Inductor Bead
F1	6505757V02	2 Amp FUSE: FILTER: See Note 2.
FL1, FL2	4805245J33	73.35 MHz
FL401, FL402	9105398W01	450 kHz CONTACT:
G1 thru G4	3905643V01	Antenna Ground JACK:
J1	0905461X03	Transceiver/VOCON Connector
J2	3905113W03	Antenna Connector
J3	3902625J04	Contact B+

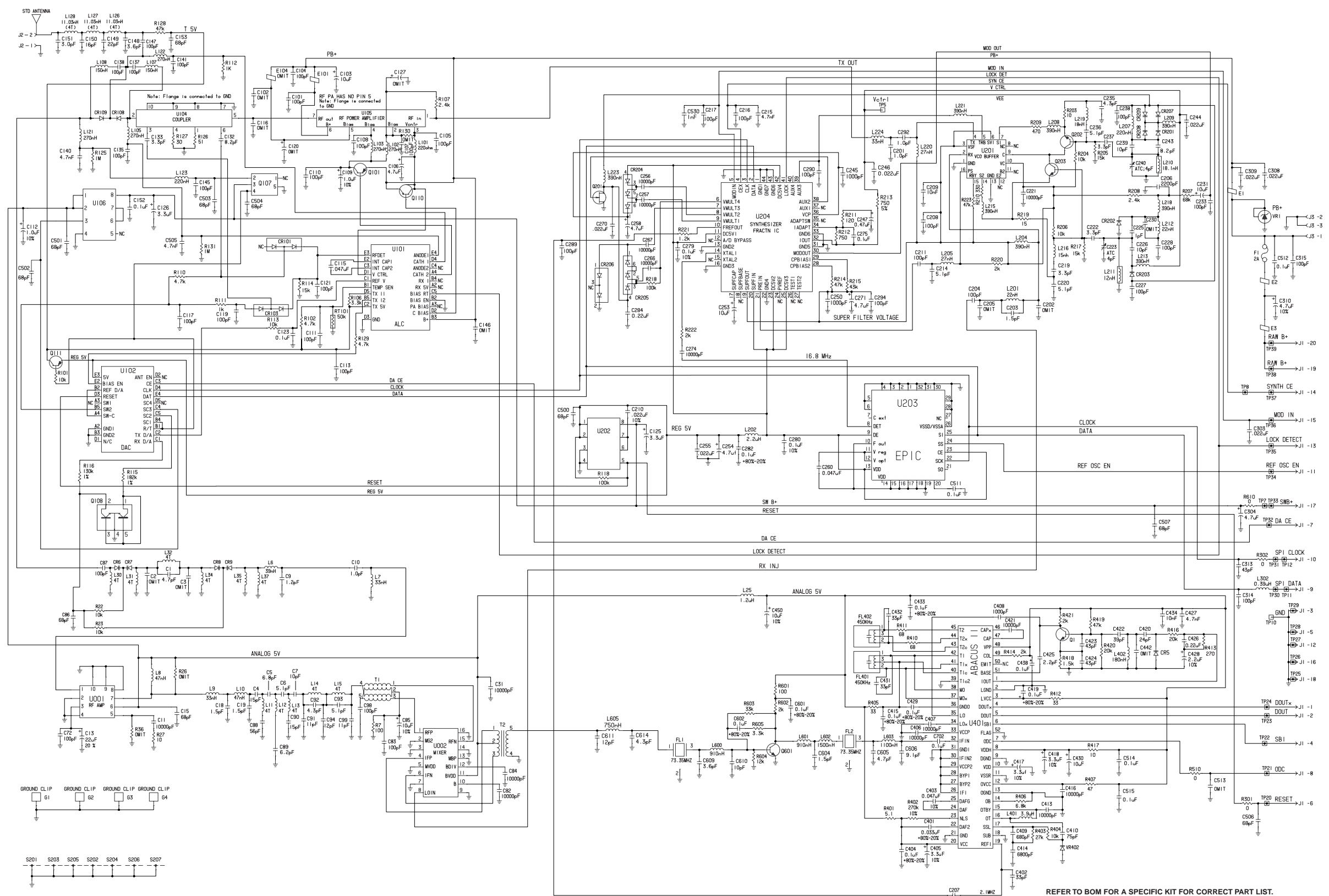
L6	2462587T41	COIL, RF: 39 nH
L7	2462587T40	33 nH
L8	2462587T42	47 nH
L9	2462587T40	33 nH
L10	2462587T42	47 nH
L11	2460591B04	11.03 nH
L12	2460591M32	27.42 nH
L13	2460591B80	19.61 nH
L14, L15	2460591B04	11.03 nH
L25	2462587Q48	1.2 uH
L30, L31	2460591B22	8.67 nH
L32	2460591B04	11.03 nH
L34, L35	2460591B22	8.67 nH
L37	2460591B04	11.03 nH
L101, L102	2462587T20	270 nH
L103	-----	Not Placed.
L105	2462587T20	270 nH
L107, L108	2462587T17	150 nH
L121, L122	2462587T20	270 nH
L123	2462587V38	220 nH
L126 thru L128	2460591B04	11.03 nH
L201	2462587T38	22 nH
L202	2462587Q20	2.2 uH 20%
L204	2462587Q42	390 nH 10%
L205	2462587V27	27 nH
L207	2462587V38	220 nH
L208, L209	2462587T22	390 nH
L210	2405619V01	18.1 nH
L211	2405619V05	12 nH
L212	2462587V26	22 nH
L213	2462587T22	390 nH
L215	2462587T22	390 nH
L216	2462587T05	15 nH 10%
L218	2462587T22	390 nH
L219	2462587T37	18 nH
L220	2462587T39	27 nH
L221	2462587T22	390 nH
L223	2462587Q42	390 nH 10%
L224	2462587T40	33 nH
L302	2462587Q42	390 nH 10%
L401	2462575A16	3.9 uH 10%
L402	2462587V37	180 nH
L600, L601	2405452C59	910 nH
L602	2405452C64	1.5 uH
L603	2405452C61	1.1 uH
L605	2462587N65	750 nH
Q1	4805218N55	TRANSISTOR: See Note 1. NPN
Q101	4805128M16	PNP
Q107	4805921T02	Switching
Q108	4802245J10	Dual NPN
Q110	4802245J12	Switching
Q111	4805128M16	PNP
Q201	4802245J15	JFET P-Channel
Q202, Q203	4805218N55	NPN
R7	0662057A25	100
R22, R23	0662057A73	10k
R26	-----	Not Placed.
R27	0662057A01	10
R36	-----	Not Placed.
R101	0662057A73	10k
R102	0662057A65	4.7k
R106	0662057A61	3.3k
R107	0662057A58	2.4k
R110	0662057A65	4.7k

R111, R112	0662057A49	1k
R113	0662057A73	10k
R114	0662057A77	15k
R115	0662057G27	182k
R116	0662057G19	130k
R118	0662057A97	100k
R125	0662057B22	1M
R126	0662057A18	51
R127	0662057A12	30
R128	0662057A89	47k
R129	0662057A65	4.7k
R130	-----	Not Placed.
R131	0662057B22	1M
R203	0662057A01	10
R204	0662057A73	10k
R205	0662057A77	15k
R206	0662057A73	10k
R207	0662057A93	68k
R208	0662057A58	2.4k
R209	0662057A41	470
R210	0662057A37	330
R211	0662057A27	120
R212, R213	0662057A46	750
R214	0662057A89	47k
R215	0662057A88	43k
R217	0662057A77	15k
R218	0662057A97	100k
R219	0662057A05	15
R220	0662057A56	2k
R221	0662057A51	1.2k
R222	0662057A56	2k
R223	0662057A89	47k
R301	0662057B47	0 ±.050
R302	0662057C01	0 ±.050
R401	0660079U18	5.1
R402	0662057B08	270k
R403	0662057A83	27k
R404	0662057A73	10k
R405	0662057A13	33
R406	0662057A69	6.8k
R407	0662057A17	47
R410, R411	0662057A21	68
R412	0662057A13	33
R413	0662057A35	270
R414	0662057A56	2k
R416	0662057A80	20k
R417	0662057A01	10
R418	0662057A53	1.5k
R419	0662057A89	47k
R420	0662057A80	20k
R421	0662057A56	2k
R510	0662057B47	0 ±.050
R601	0662057A25	100
R602	0662057A56	2k
R603	0662057A85	33k
R604	0662057A75	12k
R605	0662057A61	3.3k
R610	0662057B47	0 ±.050
RT101	0605621T02	THERMISTOR: TMTR CHIP SURFACE MT
S201	2602657J01	SHIELD: VCO
S202	2602674J02	VCO, Back
S203	2602658J01	Pendulum
S204	2602675J01	Synthesizer, Back
S205	2602660J01	Harmonic Filter, UHF
S206	2602686J01	Coil
S207	2605547X01	Varactor

T1	2505515V08	TRANSFORMER: 4:1
T2	2505515V11	16:1
U1	5105329V20	INTEGRATED CIRCUIT MODULE: See Note 1
U2	5105329V26	RF Amplifier
U101	5105835U52	Mixer
U102	5105835U51	TX (ALC)
U104	5102001J68	D/A Converter
U105	5105385Y10	Coupler
U106	5105385Y10	RF Power Amplifier
U201	5105469E65	5 Volt Regulator
U202	5102227J37	VCO Buffer
U203	5105469E65	5 Volt Regulator
U204	5105385Y42	16.8 MHz Reference Oscillator
U401	5105457W81	Fractional-N-Synthesizer
VR001	4813830A33	ABACUS DIODE: See Note 1.
VR402	4805129M58	Zener, 20V Varactor

- Notes:
- For optimum performance, order replacement diodes, transistors, and circuit modules by Motorola part number only.
  - When ordering crystals, specify carrier frequency, crystal frequency, crystal type number, and Motorola part number.
  - Part value notations:  
 $p=10^{-12}$   
 $n=10^{-9}$   
 $\mu=10^{-6}$   
 $m=10^{-3}$   
 $k=10^3$   
 $M=10^6$
  - ITEM refers to the component reference designator.
  - The UHF RF Board uses a 6-layer printed circuit board.





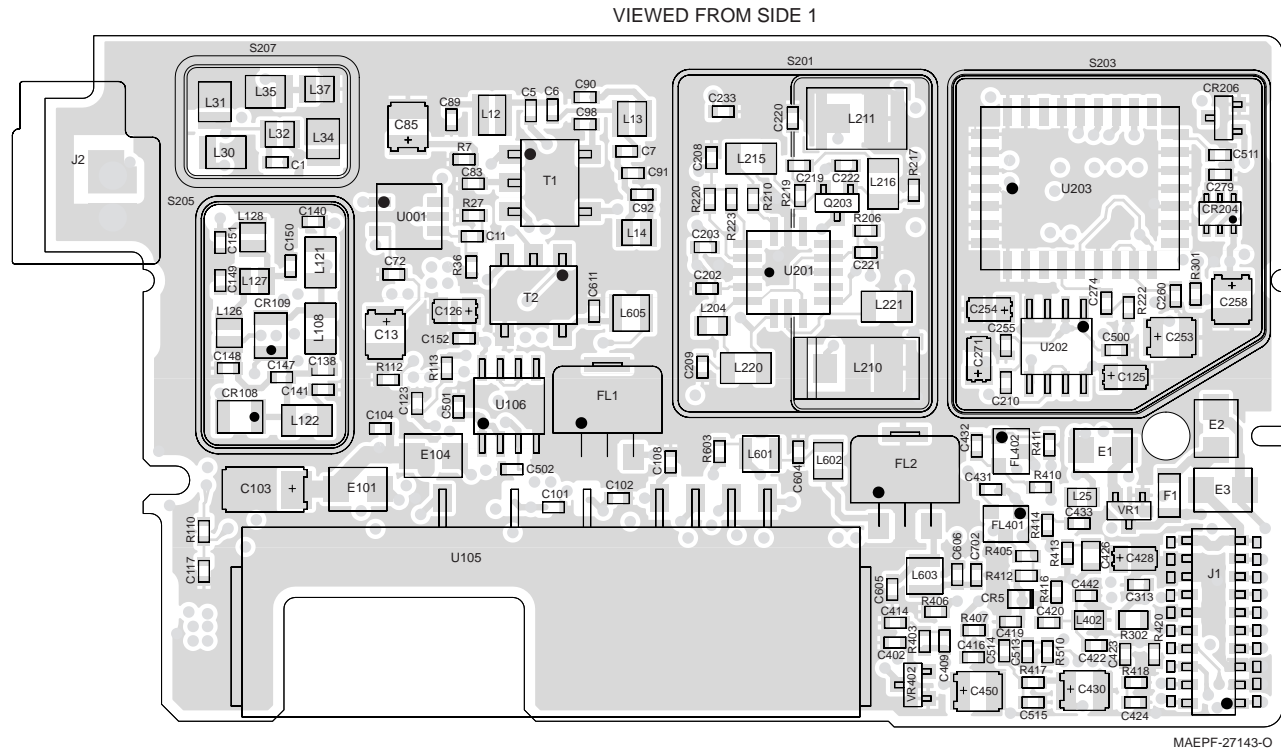
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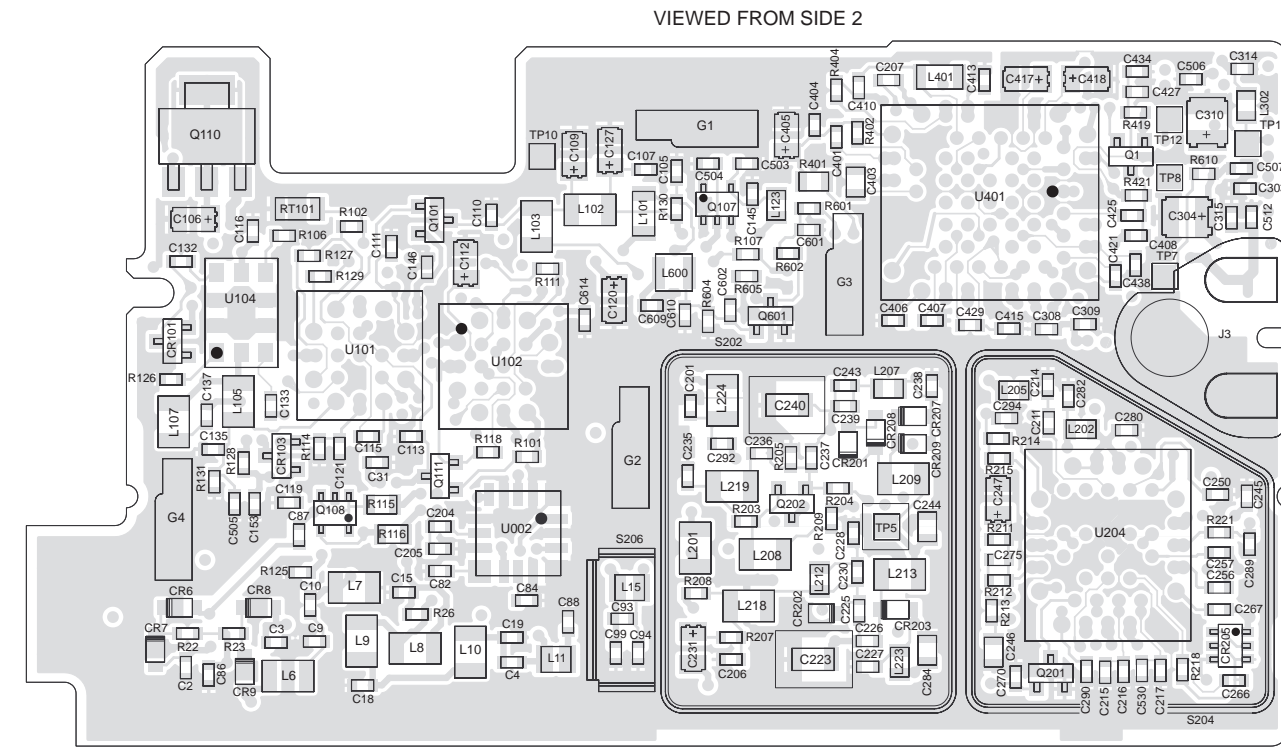
NLE4244P UHF Range 2 Transceiver Board Schematic Diagram



NLE4244P UHF Range 2 Transceiver Board  
Electrical Parts List



MAEPF-27143-O



MAEPF-27144-O

ITEM	MOTOROLA PART NUMBER	DESCRIPTION
		<b>CAPACITOR, Fixed: pF ±5%; 50V unless otherwise stated</b>
C1	2113930F15	3.3 pF 50V ±0.25 pF 50V
C2, C3	2113930F12	2.4 pF 50V ±0.25 pF 50V
C4	2113930F36	24
C5, C6	2113930F20	5.1 pF 50V ±0.25 pF 50V
C7	2113930F28	11
C9	2113930F15	3.3 pF 50V ±0.25 pF 50V
C10	2113930F29	12 pF
C11	2113931F49	.01 uF
C13	2311049A66	22 uF
C15	2113930F47	68
C18	-----	Not Placed.
C19	2113930F19	4.7 pF 50V ±0.25 pF 50V
C31	2113931F49	.01 uF
C72	2113930F51	100
C82	2113931F49	.01 uF
C83	2113930F51	100
C84	2113931F49	.01 uF
C85	2311049J23	10 uF
C86	2113930F47	68
C87	2113930F51	100
C88	2113930F45	56
C89	2113930F19	4.7 pF 50V ±0.25 pF 50V
C90	2113930F26	9.1 pF 50V ±0.25 pF 50V
C91	2113930F28	11
C92	2113930F09	1.8 pF 50V ±0.1 pF 50V
C93	2113930F17	3.9 pF 50V ±0.25 pF 50V
C94	2113930F27	10
C98	2113930F51	100
C99	2113930F21	5.6 pF 50V ±0.25 pF 50V
C101	2113930F51	100
C102	-----	Not Placed.
C103	2311049J26	10 uF
C104, C105	2113930F51	100
C106	2311049A56	4.7 uF
C107, C108	2113930F51	100
C109	2311049A07	1 uF
C110, C111	2113930F51	100
C112	2311049A07	1 uF
C113	2113930F51	100
C115	2113932K07	.047 uF +80/-20% 16V
C116	-----	Not Placed.
C117	2113930F51	100
C119	2113930F51	100
C120	-----	Not Placed.
C121	2113930F51	100
C123	2113932K15	0.1 uF +80/-20% 16V
C125, C126	2311049A54	3.3 uF
C127	-----	Not Placed.
C132	2113930F25	8.2 pF 50V ±0.25 pF 50V
C133	2113930F09	1.8 pF 50V ±0.1 pF 50V
C135	2113930F51	100
C137, C138	2113930F51	100
C140	2113931F41	4.7 nF
C141	2113930F51	100
C145	2113930F51	100
C146	-----	Not Placed.
C147	2113930F51	100
C148	2113930F11	2.2 pF 50V ±0.25 pF 50V

C149	2113930F27	10
C150	2113930F23	6.8 pF 50V ±0.25 pF 50V
C151	2113930F17	3.9 pF 50V ±0.25 pF 50V
C152	2113932K15	0.1 uF +80/-20% 16V
C153	2113930F47	68
C201, C202	-----	Not Placed.
C203	2113930F07	1.5 pF 50V ±0.1 pF 50V
C204	2113930F51	100
C205	-----	Not Placed.
C206	2113931F33	2.2 nF
C207	2113931F49	.01 uF
C208	2113930F51	100
C209	2113931F49	.01 uF
C210	2113932E07	.022 uF 10% 16V
C211	2113930F51	100
C214	2113930F14	3.0 pF 50V ±.25 pF 50V
C215	2113931F41	4.7 nF
C216, C217	2113930F51	100
C219	2113930F11	2.2 pF 50V ±0.25 pF 50V
C220	2113930F22	6.2 pF 50V ±0.25 pF 50V
C221	2113931F49	.01 uF
C222	2113930F18	4.3 pF 50V ±0.25 pF 50V
C223	2113906C02	4
C225	2113930F03	1 pF 50V ±0.1 pF 50V
C226	2113930F26	9.1 pF 50V ±0.25 pF 50V
C227, C228	2113930F51	100
C230	-----	Not Placed.
C231	2311049A60	10 uF
C233	2113930F51	100
C235	2113930F20	5.1 pF 50V ±0.25 pF 50V
C236	2113930F18	4.3 pF 50V ±0.25 pF 50V
C237	2113930F15	3.3 pF 50V ±0.25 pF 50V
C238	2113930F51	100
C239	2113930F23	6.8 pF 50V ±0.25 pF 50V
C240	2113906C02	4
C243	2113930F23	6.8 pF 50V ±0.25 pF 50V
C244	2109720D09	.022 uF
C245	2113931F25	1 nF
C246	2109720D09	.022 uF
C247	2311049A05	0.47 uF
C250	2113931F25	1 nF
C253	2311049J23	10 uF
C254	2311049A56	4.7 uF
C255	2113932E07	.022 uF 10% 16V
C256, C257	2113931F49	.01 uF
C258	2311049J11	4.7 uF
C260	2113932K07	.047 uF +80/-20% 16V
C266, C267	2113931F49	10 nF
C270	2113932E07	.022 uF 10% 16V
C271	2311049A56	4.7 uF
C274	2113931F49	.01 uF
C275	2113932K15	0.1 uF +80/-20% 16V
C279, C280	2113932K15	0.1 uF +80/-20% 16V
C282	2113932K15	0.1 uF +80/-20% 16V
C284	2113743A23	0.22 uF 10%
C289, C290	2113930F51	100
C292	2113930F51	100
C294	2113930F51	100
C303	2113932E07	.022 uF 10% 16V
C304	2311049J11	4.7 uF
C308, C309	2113932E07	.022 uF 10% 16V
C310	2311049J11	4.7 uF
C313	2113930F42	43
C314, C315	2113930F51	100
C401	2113932K03	.033 uF +80/-20% 16V

NLE4244P UHF Range 2 Transceiver Circuit Board Details and Parts List

C402	2113930F39	33
C403	2113743A13	.047 uF
C404	2113932K15	0.1 uF +80/-20% 16V
C405	2311049A42	3.3 uF
C406, C407	2113931F49	.01 uF
C408	2113931F25	1 nF
C409	2113931F21	680 pF
C410	2113930F48	75
C413	2113931F49	.01 uF
C414	2113931F45	6.8 nF
C415	2113932K15	0.1 uF +80/-20% 16V
C416	2113931F49	.01 uF
C417, C418	2311049A42	3.3 uF
C419	2113932K15	0.1 uF +80/-20% 16V
C420	2113930F36	24
C421	2113931F49	.01 uF
C422	2113930F41	39
C423, C424	2113930F42	43
C425	2113930F11	2.2 pF 50V ±0.25 pF 50V
C426	2113743A23	0.22 uF 10%
C427	2113931F41	4.7 nF
C428	2311049A40	2.2 uF
C429	2113932K15	0.1 uF +80/-20% 16V
C430	2311049J23	10 uF
C431, C432	2113930F39	33
C433	2113932K15	0.1 uF +80/-20% 16V
C434	2113931F49	.01 uF
C438	2113932K15	0.1 uF +80/-20% 16V
C442	-----	Not Placed.
C450	2311049J23	10 uF
C500 thru C504	2113930F47	68
C505	2113931F41	4.7 nF
C506, C507	2113930F47	68
C511, C512	2113932K15	0.1 uF +80/-20% 16V
C513	-----	Not Placed.
C514, C515	2113932K15	0.1 uF +80/-20% 16V
C530	2113931F25	1 nF
C601, C602	2113932K15	0.1 uF +80/-20% 16V
C604	2113930F07	1.5 pF 50V ±0.1 pF 50V
C605	2113930F19	4.7 pF 50V ±0.25 pF 50V
C606	2113930F26	9.1 pF 50V ±0.25 pF 50V
C609	2113930F16	3.6 pF 50V ±0.25 pF 50V
C610	2113930F27	10
C611	2113930F29	12 pF
C614	2113930F18	4.3 pF 50V ±0.25 pF 50V
C702	2113932K15	0.1 uF +80/-20% 16V
CR5 thru CR9	4862824C01	Varactor
CR101	4805129M67	Dual
CR103	4805129M67	Dual
CR108, CR109	4802482J02	PIN
CR201	4802245J29	Varactor
CR202	4862824C01	Varactor
CR203	4862824C03	Varactor
CR204, CR205	4802233J09	Triple
CR206	4805129M06	Triple
CR207 thru CR209	4802245J29	Varactor
E1 thru E2	2484657R01	Inductor bead
E101	2484657R01	Inductor bead
E104	-----	Not Placed.
F1	6505757V02	2 Amp
FL1, FL2	4805245J33	73.35 MHz

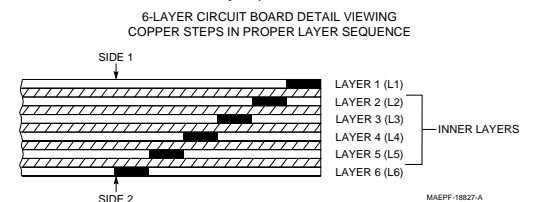
FL401, FL402	9105398W01	450kHz
G1 thru G4	3905643V01	<b>CONTACT:</b> Antenna Ground
J1	0905461X03	<b>JACK:</b> Transceiver/VOCON Connector
J2	3905113W03	Antenna Connector
J3	3902625J04	Contact B+
L6, L7	2462587T38	<b>COIL, RF:</b> 22 nH
L8	2462587T20	270 nH
L9	2462587T38	22 nH
L10	2462587T05	15 nH
L11	2460591B04	11.03 nH
L12	2460591M32	27.42 nH
L13	2460591B80	19.61 nH
L14, L15	2460591B04	11.03 nH
L25	2462587Q48	1.2 uH
L30, L31	2460591A01	4.22 nH
L32	2460591B04	11.03 nH
L34, L35	2460591A01	4.22 nH
L37	2460591B04	11.03 nH
L101, L102	2462587T20	270 nH
L103	-----	Not Placed.
L105	2462587T20	270 nH
L107, L107	2462587T17	150 nH
L121, L122	2462587T20	270 nH
L123	2462587V38	220 nH
L126 thru L128	2460591B04	11.03 nH
L201	2462587T37	18 nH
L202	2462587Q20	2.2 uH
L204	2462587Q42	390 nH
L205	2462587V26	22 nH
L207	2462587V36	150 nH
L208, L209	2462587T22	390 nH
L210	2405619V03	15.1 nH
L211	2405619V07	9 nH
L212	2462587V25	18 nH
L213	2462587T22	390 nH
L215	2462587T22	390 nH
L216	2462587T05	15 nH
L218	2462587T22	390 nH
L219	2462587T37	18 nH
L220	2462587T12	56 nH
L221	2462587T22	390 nH
L223	2462587Q42	390 nH
L224	2462587T42	47 nH
L302	2462587Q42	390 nH
L401	2462575A16	3.9 uH
L402	2462587V37	180 nH
L600, L601	2405452C59	910 nH
L602	2405452C64	1.5 uH
L603	2405452C61	1.1 nH
L605	2462587N65	750 nH
Q1	4805218N55	<b>TRANSISTOR:</b> See Note 1. NPN
Q101	4805128M16	PNP
Q107	4805921T02	Switching
Q108	4802245J10	Dual NPN
Q110	4802245J12	Switching
Q111	4805128M16	PNP
Q201	4802245J15	JFET P-Channel
Q202, Q203	4805218N55	NPN
Q601	4882022N70	NPN
		<b>RESISTOR, Fixed:</b> Ω ±5%; 1/8W Unless otherwise stated.

R7	0662057A25	100
R22, R23	0662057A73	10k
R026	-----	Not Placed.
R027	0662057A01	10
R036	-----	Not Placed.
R101	0662057A73	10k
R102	0662057A65	4.7k
R106	0662057A61	3.3k
R107	0662057A58	2.4k
R110	0662057A65	4.7k
R111, R112	0662057A49	1k
R113	0662057A73	10k
R114	0662057A77	15k
R115	0662057G27	182k
R116	0662057G19	130k
R118	0662057A97	100k
R125	0662057B22	1M
R126	0662057A18	51
R127	0662057A12	30
R128	0662057A89	47k
R129	0662057A65	4.7k
R130	-----	Not Placed.
R131	0662057B22	1M
R203	0662057A01	10
R204	0662057A73	10k
R205	0662057A77	15k
R206	0662057A73	10k
R207	0662057A93	68k
R208	0662057A58	2.4k
R209	0662057A41	470
R210	0662057A37	330
R211	0662057A27	120
R212, R213	0662057A46	750
R214	0662057A89	47k
R215	0662057A88	43k
R217	0662057A77	15k
R218	0662057A97	100k
R219	0662057A09	22
R220	0662057A56	2k
R221	0662057A51	1.2k
R222	0662057A56	2k
R223	0662057A89	47k
R301	0662057B47	0 ±.050
R302	0662057C01	0 ±.050
R401	0660079U18	5.1
R402	0662057B08	270k
R403	0662057A83	27k
R404	0662057A73	10k
R405	0662057A13	33
R406	0662057A69	6.8k
R407	0662057A17	47
R410, R411	0662057A21	68
R412	0662057A13	33
R413	0662057A35	270
R414	0662057A56	2k
R416	0662057A80	20k
R417	0662057A01	10
R418	0662057A53	1.5k
R419	0662057A89	47k
R420	0662057A80	20k
R421	0662057A56	2k
R510	0662057B47	0 ±.050
R601	0662057A25	100
R602	0662057A56	2k
R603	0662057A85	33k

R604	0662057A75	12k
R605	0662057A61	3.3k
R610	0662057B47	0 ±.050
RT101	0605621T02	50k
S201	2602657J01	<b>SHIELD:</b> VCO
S202	2602674J02	VCO, Back
S203	2602658J01	Pendulum
S204	2602675J01	Synthesizer, Back
S205	2602660J01	Harmonic Filter, UHF
S206	2602686J01	Coil
S207	2605547X01	Varactor
T1	2505515V08	4:1
T2	2505515V11	16:1
U1	5105329V20	<b>TRANSFORMER:</b> RF Amplifier
U2	5105329V26	Mixer
U101	5105835U52	TX (ALC)
U102	5105835U51	D/A Converter
U104	5102001J68	Coupler
U105	5105385Y11	RF Power Amplifier
U106	5105469E65	5 Volt Regulator
U201	5102227J37	VCO Buffer
U202	5105469E65	5 Volt Regulator
U203	5105385Y42	16.8 Reference Oscillator
U204	5105457W81	Fractional-N-Synthesizer
U401	5105835U90	ABACUS
VR1	4813830A33	<b>DIODE:</b> See Note 1. Zener, 20V
VR402	4805129M58	Varactor

**Notes:**

- For optimum performance, order replacement diodes, transistors, and circuit modules by Motorola part number only.
- When ordering crystals, specify carrier frequency, crystal frequency, crystal type number, and Motorola part number.
- Part value notations:  
 $p=10^{-12}$   
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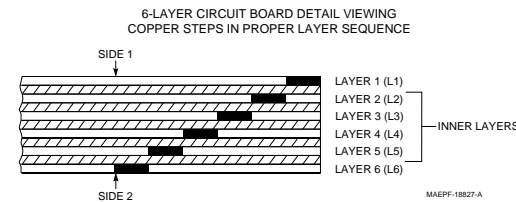


C605	2113930F16	3.6 pF 50V ±0.25 pF 50V
C606	2113930F24	7.5 pF 50V ±0.25 pF 50V
C609	2113930F15	3.3 pF 50V ±0.25 pF 50V
C610	2113930F24	7.5 pF 50V ±0.25 pF 50V
C611	2113930F27	10
C612	2113930F14	3 pF 50V ±0.25 pF 50V
C613	2113932K15	.1 uF +80/-20% 16V
C614	2113930F21	5.6 pF 50V ±0.25 pF 50V
		<b>DIODE:</b> See Note 1.
CR102	4805129M96	Dual
CR104	4805129M96	Dual
CR301	4802233J09	Triple
CR501, CR502	4805218N57	Dual
		<b>CORE:</b>
E1 thru E4	2484657R01	Inductor Bead
		<b>FUSE:</b>
F1	6505757V02	2 Amp
		<b>FILTER:</b> See Note 2.
FL1, FL2	4805245J33	73.35 MHz
FL401, FL402	9105398W01	450 kHz
		<b>CONTACT:</b>
G1 thru G4	3905643V01	Antenna Ground
		<b>JACK:</b>
J1	0905461X03	Transceiver/VOCON Connector
J2	3905113W03	Antenna Connector
J3	3902625J04	Contact, B+
		<b>COIL, RF:</b>
L101	2462587V37	180 nH
L102	2462587V24	15 nH
L103	2462587V37	180 nH
L104, L105	2460591A11	7.66 nH
L106	2462587V37	180 nH
L108	2462587V37	180 nH
L201	2460591C40	17.02 nH
L202	2460591E24	23.75 nH
L203	2462587V37	180 nH
L204	2460591E24	23.75 nH
L301	2462587V24	15 nH
L302	2462587Q59	10 uH
L401	2462575A16	3.9 uH
L402	2462587N56	180 nH
L600, L601	2405452C59	910 nH
L602	2405452C64	1.5 uH
L603	2405452C61	1.1 uH
L605	2462587N65	750 nH
		<b>TRANSISTOR:</b> See Note 1.
Q1	4805218N55	NPN
Q501	4805218N45	Switching
Q502	4805128M27	PNP
Q503	4805921T06	Dual PNP
		<b>RESISTOR, Fixed: Ω±5%; 1/8W</b> Unless otherwise stated.
R101	0662057A90	51k
R202	0662057A01	10
R204	0662057A25	100
R304	0662057A90	51k
R305	0662057A56	2k
R306	0662057A65	4.7k
R307	0662057A49	1k
R309	0662057A90	51k
R310	0662057A49	1k
R311	0662057A77	15k
R314	0662057A18	51
R315	0662057A87	39k
R326 thru R328	0662057C01	0 ±.050
R401	0660079U18	5.1
R402	0662057B08	270k
R403	0662057A83	27k

R404	0662057A73	10k
R405	0662057A13	33
R406	0662057A69	6.8k
R407	0662057A17	47
R410, R411	0662057A21	68
R412	0662057A13	33
R413	0662057A35	270
R414	0662057A56	2k
R416	0662057A80	20k
R417	0662057A01	10
R418	0662057A53	1.5k
R419, R420	0662057A89	47k
R421	0662057A58	2.4k
R501	0662057A73	10k
R503	0662057A73	10k
R505	0662057A77	15k
R506	0662057A69	6.8k
R507	0662057A61	3.3k
R508	0662057A49	1k
R509	0662057C75	1k
R510	0662057B22	1 M
R511	0662057A56	2k
R514	0662057A73	10k
R601	0662057A25	100
R602	0662057A56	2k
R603	0662057A85	33k
R604	0662057A75	12k
R605	0662057A61	3.3k
		<b>THERMISTOR:</b>
RT501	0605621T02	50k
		<b>SHIELD:</b>
SH1	2605258V01	Synthesizer
SH2	2605259V01	Diode
SH3	2605260V01	RF Switch
SH4	2605418V01	Transformer
SH5	2605263V01	Filter, 3-Pole
SH6	2605634V01	Antenna
SH7	2605890U03	VCO
		<b>TRANSFORMER:</b>
T201	2505515V07	25:1
T202	2505515V04	5:1
		<b>INTEGRATED CIRCUIT MODULE:</b>
		See Note 1.
U201	5105279V15	3-Pole Filter
U202	5105329V21	RF Amplifier
U203	5105279V15	3-Pole Filter
U205	5105329V26	Mixer Buffer
U302	5105457W81	Fractional-N-Synthesizer
U303	5105662U76	VCO Buffer
U304	5105385Y61	16.8 MHz Reference Oscillator
U305	5105469E65	5-Volt Regulator
U307	5105238U94	VCO
U401	5105835U90	ABACUS
U501	5105279V26	Coupler
U502	5108038H12	RF Power Amplifier
U503	5105835U51	D/A Converter
U504	5105835U52	TX ALC
		<b>DIODE:</b> See Note 1.
VR001	4813830A33	Zener, 20V
VR002	-----	Not Placed.
VR401	4862824C01	Varactor
VR402	4805129M58	Varactor

Notes:

- For optimum performance, order replacement diodes, transistors, and circuit modules by Motorola part number only.
- When ordering crystals, specify carrier frequency, crystal frequency, crystal type number, and Motorola part number.
- Part value notations:  
 $p=10^{-12}$   
 $n=10^{-9}$   
 $\mu=10^{-6}$   
 $m=10^{-3}$   
 $k=10^3$   
 $M=10^6$
- ITEM refers to the component reference designator.
- The 800 MHz Transceiver Board uses a 6-layer printed circuit board.



## VOCON Board Signals

Due to the nature of the schematic-generating program, signal names must be different when they are not directly connected to the same point. The following tables provide a cross-reference to the various pinouts for the same functional signal.

### VOCON Board Address Bus (A) Pinouts

Bus	U402	U403	U404	U405	U406	U414	U415
A0	A4/21	A4/21	20	C2/83	E9/11	A4/21	--
A1	B4/23	B4/23	19	D3/84	E10/10	B4/23	--
A2	A3/24	A3/24	18	D2/86	E8/8	A3/24	--
A3	B3/25	B3/25	17	E2/87	--	B3/25	--
A4	A2/26	A2/26	16	D4/88	--	A2/26	--
A5	B2/1	B2/1	15	B1/92	--	B2/1	--
A6	J6/2	J6/2	14	E3/95	--	J6/2	--
A7	K7/3	K7/3	13	F1/96	--	K7/3	--
A8	J7/4	J7/4	3	F2/97	--	J7/4	--
A9	K8/5	K8/5	2	F3/98	--	K8/5	--
A10	B8/6	B8/6	31	G1/100	--	B8/6	--
A11	A8/7	A8/7	1	J2/101	--	A8/7	--
A12	B7/8	B7/8	12	K1/102	--	B7/8	--
A13	J3/9	--	4	H3/104	D9/7	--	2
A14	--	--	5	G2/106	B9/6	--	1
A15	K3/20	K3/20	11	H2/107	D10/5	J3/20	--

### VOCON Board Address Bus (HA) Pinouts

Bus	U201	U202	U204	U205	U206	U210	U405
HA0	13	10	D2/17	20	D7	20	E9/25
HA1	11	9	C2/16	19	C7	19	F8/24
HA2	10	8	C1/15	18	C8	18	F9/22
HA3	8	7	D1/14	17	D8	17	--
HA4	2	6	E3/13	16	E6	16	--
HA5	7	5	E2/12	15	--	15	--
HA6	6	4	E1/11	14	--	14	--
HA7	5	3	E4/10	13	--	13	--
HA8	27	25	F1/9	3	F6	3	--
HA9	12	24	F3/8	2	F7	2	--
HA10	24	21	F2/7	31	--	31	--
HA11	26	23	G1/6	1	--	1	--
HA12	4	2	F4/5	12	--	12	--
HA13	28	26	G2/4	4	--	4	--
HA14	3	1	H1-In/3	5	H8-In	5	--
HA15	--	--	H2-In/78	11	H7-In	11	--
HA16	--	--	--	10	K6	10	--
HA17	--	--	--	6	G5	6	--

### VOCON Board Data Bus (HD) Pinouts

Bus	U201	U202	U204	U205	U206	U210	U405
HD0	14	1	C6/40	21	C3	21	C7/44
HD1	15	12	B8/43	22	B1	22	B8/43
HD2	16	13	C7/44	23	C2	23	D7/41
HD3	18	15	D5/45	25	D4	25	A9/39
HD4	19	16	C8/46	26	C1	26	C9/38
HD5	20	17	D7/47	27	D2	27	C10/35
HD6	21	18	D6/48	28	D3	28	D8/33
HD7	23	19	D8/49	29	D1	29	C8/32

### VOCON Board Data Bus (D) Pinouts

Bus	U402	U403	U404	U405	U406	U414
D0	B9/11	B9/-	21	G3/110	--	B9/-
D1	C8/12	C8/-	22	J1/111	--	C8/-
D2	C9/13	C9/-	23	K3/113	--	C9/-
D3	D9/15	D9/-	25	L3/114	--	D9/-
D4	E8/16	E8/-	26	J3/116	--	E8/-
D5	E9/17	E9/-	27	K4/117	--	E9/-
D6	F9/18	F9/-	28	H4/119	--	F9/-
D7	G9/19	G9/-	29	L2/120	--	G9/-
D8	G8/-	G8/11	--	K2/121	H10/21	G8/-
D9	H8/-	H8/12	--	J4/122	H9/22	H8/-
D10	J9/-	J9/13	--	K5/126	H8/23	J9/-
D11	J8/-	J8/15	--	L5/128	J8/26	J8/-
D12	J2/-	J2/16	--	J5/130	L9/27	J2/-
D13	J1/-	J1/17	--	K6/131	K8/28	J1/-
D14	H2/-	H2/18	--	J6/133	L8/29	H2/-
D15	G2/-	G2/19	--	H7/134	J7/30	G2/-
D16	G1/-	G1/-	--	L9/135	K7/31	G1/11
D17	F1/-	F1/-	--	K8/136	L7/33	F1/12
D18	E1/-	E1/-	--	K7/138	J6/34	E1/13
D19	E2/-	E2/-	--	J7/139	K6/35	E2/15
D20	D1/-	D1/-	--	L8/141	J5/37	D1/16
D21	C1/-	C1/-	--	K10/142	L6/38	C1/17
D22	C2/-	C2/-	--	J9/2	L5/39	C2/18
D23	B1/-	B1/-	--	J10/3	K5/41	B1/19

### VOCON U405 (DSP)

U405 Pin #	Description	To/From
C1/82	PS*	U404-6 U406-D8
C3/80	DS*	
A3/68	RD*	U404-32 U406-F8
C4/67	WR*	U404-7 U406-G10
B3/78	X/Y*	
H10/6	MODA/IRQA*	U204-G4 U406-F10
H9/5	MODB/IRQB*	U406-F9
J8/17	XTAL	R415
K9/19	EXTAL	U406-G9 (DCLK)
A2/53	TXD/STD	U406-H1
C5/59	SRD/RXD	U406-L3
B6/51	SCK SCKT 1.2 MHz	U406-G3
B2/52	SC2 TFS 48 kHz	U406-H2
B5/56	SC1 RFS 20 kHz	20 kHz
B9/49	SC0 SCKR 2.4 MHz	U406-K4
C6/48	SCLK	U204-G3 U406-C9
A7/46	TXD/EMC RXD	J801-3
B7/45	RXD/EMC TXD	J801-4
G9/10	RESET/DSP RST*	U204-H8
E10/26	HACK*	R409
B10/31	HREQ*	U204-H3
E8/28	HEN*	U206-J7
D9/30	HR/W*	U204-B6
/4	MODC/NMIX	Q1

### U204 (MCU)

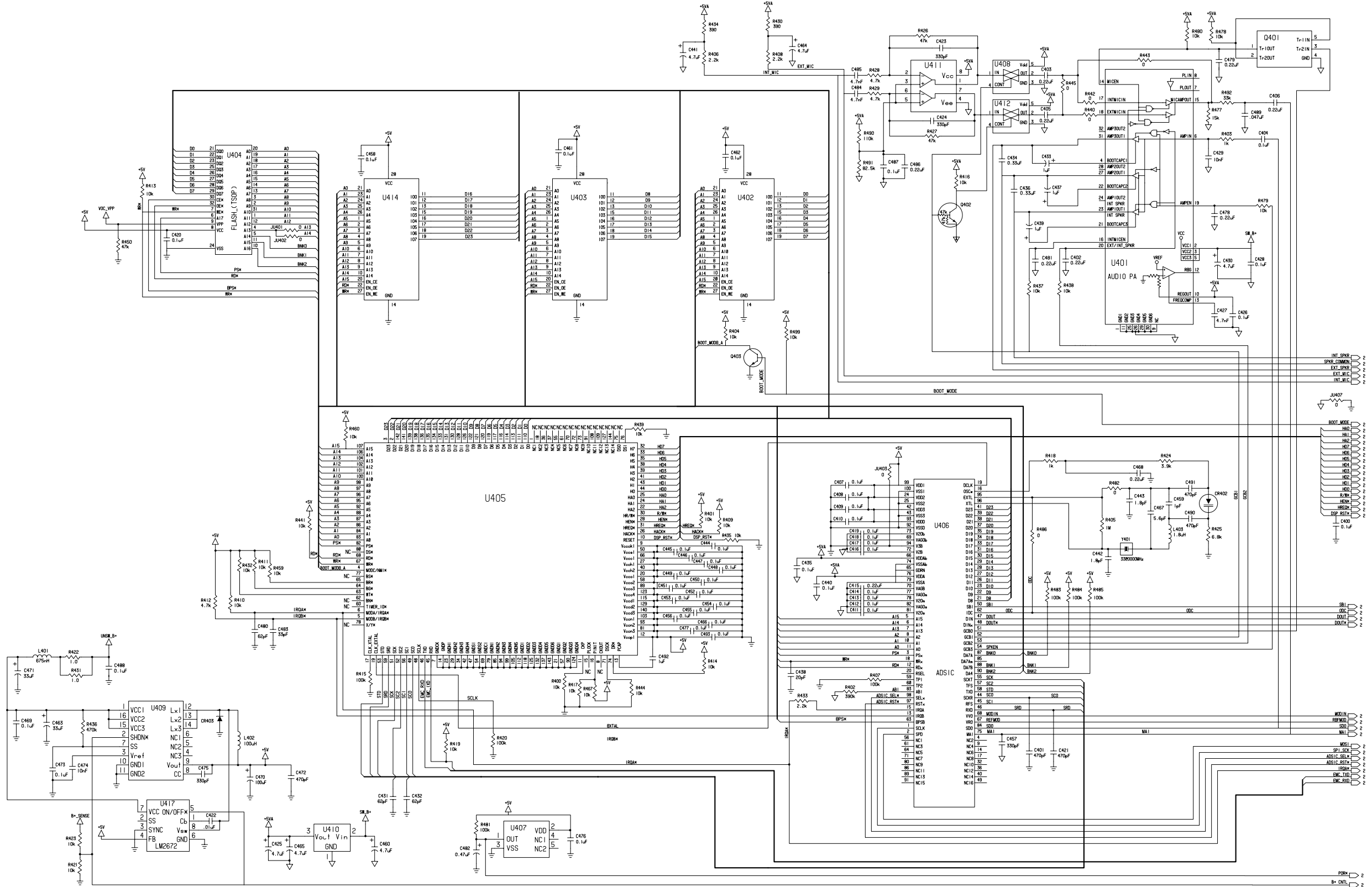
U204 Pin #	Description	To/From
B1/18	PE0	R260
B2/23	PE1 B SENSE/LBAT/ PWR DWN	VR214
C3/25	PE2 VOL	J901-3
A3/27	PE3 EMERG	J901-4
D3/19	PE4 TG1 PROG SWITCH	J901-2
A2/24	PE5 TG2 A/B SWITCH	J901-9
B3/26	PE6 SPKR COM-MON	U401-A3 J201-11 J701-14
C4/28	PE7 EXT SPKR	U401-A5 J-201-12 U206-A3
B7/39	4XECLK (7.3726MHz)	U206-A3
J7/63	PD0 BOOT DATA IN (RXD)	J201-15 U206
G6/64	PD1 BOOT DATA OUT (TXD)	J201-4 U208
H6/65	PD2 MISO	J801-7
J6/66	PD3 MOSI	J601-1 J801-8
G5/67	PD4 SPI SCK	J601-2 J801-9
H5/68	PD5 DA SEL*	J401-7
C5/33	MOD A	Q204C
B5/32	MOD B	Q204C
G3/77	PA0 SCLK	U405-C6 U406-C9
J2/76	PA1 BOOT MODE	U405
H3/75	PA2 HREQ*	U405-B10
J3/74	PA3 SB9600 BUSY	J201-6
G4/73	PA4 IRQA*	U406-F10 U405-H10
H4/72	PA5 BOOTSTRAP*	U206-E5
J4/71	PA6 ECLK SHIFT	Q205B
F5/70	PA7 DISP RST*	J601-5
E5/50	RESET/RESET*	U201-31 U206-E4
E6/53	PG7 CSProg*	U206-E3
F8/54	PG6 CSGEN*	U211-1
G8/55	PG5 CS101*	U206-G1
G7/56	PG4 ADSIC RST*	U406-A8
F7/57	PG3 ADSIC SEL*	U406-B8
H8/58	PG2 DSP RST*	U405-G9
F6/59	PG1 ROSC/PSC CE*	J401-11
H7/62	PG0 SYN SEL*	J401-14
B6/35	R/W*	U405-D9 U206-B3
H2/78	HA15 IN INT PTT*	J901-6
A5/34	ECLK (1.8432MHz)	U206-A4
E8/51	HIRO*	R233
E7/52	IRQ*	U206-E2
A6/36	EXTAL 7.3728MHz	Y201
A7/37	XTAL	Q205C

### U206 (SLIC)

U206 Pin #	Description	To/From
F3	PH0 RTA0	J901-11
F4	PH1 RTA1	J901-13
F2	PH2 RTA2	J901-15
H1	PH3 RTA3	J901-7
G3	PH4 EXT PTT/OPT SEL 1	J201-7 U206-G3
H2	PH5 INT PTT*	J901-6 U206-H2
H3	PH6 EMC REQ	J801-11
K2	PH7 LOCK DET*	J401-13 U302-41 CR502
B4	PJ0 COL3 MOB IRQ*	J701-6
D5	PJ1 COL2	J701-5
A5	RS232 DATA OUT/BOOT DATA IN	J201-15
B6	PJ3 CTSOUT*	J201-14
A6	PJ4	R268
C6	PJ5 OPT SEL2 (KEYLOAD*)	J201-9
A7	PJ6 COL1*	J701-10
D6	PJ7 EMC EN*	J801-10
C9	POR*	U409-2
E4	HC11RST*/RESET*	U204-E5 U201-31
C4	OE*	U201-25 U202-22 U205-32 U210-32
B3	R/W*	U405-D9/30 U204-B6 U204-H4
E5	BOOTSTRAP*	J201-6
A2	MEM R/W*	U201-29 U202-27 U204-E6
E3	AV*/CSProg*	U204-G8
G1	CE*/CS101*	R252
G2	SCNSLB	U205-30 U210-30
K5	ROM1CS*	U201-22
F5	ROM2CS*	J801-15
J4	EE1CS*	J201-10
J8	TRSBIN/RTSIN*/KEYFAIL*	J201-8
B2	RXDIN/RS232 DATA IN	J201-15 U204-J7
J2	BOOTRX/BOOT DATA IN	U204-B7
A3	4XECLK	U204-A5
A4	ECLK	J701-13
J3	ROW1	J701-3
G4	ROW2 SPKREN*	J701-11
K8	ROW3 BUSY OUT*	J701-9
G9	ROW4 TXPA EN*	J701-1
F8	ROW5 5V EN*	J701-12
G7	ROW6 MICEN	U409-2 Q206B
J9	B+ CNTL	J601-6
E7	BL EN	J801-12 U211-2
K7	CS3B EMC MAKEUP*	U405-E8/28
G6	CS2B RAM SEL*	J601-4
J7	CS1B HEN*	J901-12
G8	DISP EN*/LATCH SEL*	J901-8
H9	RED LED	J901-8
E8	GRN LED	U204-E7
E2	IRQ*	

### VOCON U406 (ADSIC)

U406 Pin #	Description	To/From
D8/3	PS*	U404-6 U405-C1
G10/18	WR*	U405-C4 U404-7 U402/3/14-K2
F8/12	RD*	U405-A3 U404-32 U402/3/14-K6
J9/20	RSEL	U403-J3 U414-K3
G2/59	TP1	R407
G1/60	TP2	n/c
A4/83	AB1	R402
B8/98	SEL*/ADSIC SEL*	U204-F7
A8/97	RST*/ADSIC RST*	U204-G7
F10/15	IRQA/IRQA*	U204-G4 U405-H10
F9/13	IROB/IROB* 8kHz	U405-H9
F2/63	SSW/EP5*	U404-30
C9/1	SCLK/SPI SCK	U204-G5 J401-10 J601-2 J801-9
C10/2	SPD/MOSI	J401-9 J601-1 J801-8
C1/75	MAI	U401-F2
B5/84	SDO	U401-C6
B1/	VRO REFMOD	
B2/68	MODIN	J401-15
L3/46	RXD SRD 2.4 MHz	U405-C5
J4/45	RFS SC1 20 kHz	U405-B5
K4/44	SCKR SCD 2.4 MHz	U405-B9
H1/58	TXD STD	U405-A2
H2/57	TFS SC2 48kHz	U405-B2
G3/55	SCKT SCK 1.2MHz	U405-B6
C8/90	DA4 BNK2	U404-10
C3/88	DA7B BNK1	U404-11
B6/87	DA7A BNK0	U404-5
J1/54	GCB3 SPKEN	U401-D1
J2/53	GCB2 (EXT/INT SPKR)	U401-C1
K1/52	GCB1	U408-4 U401-E2 (INT MICEN)
K2/51	GCB0 MICEN	Q401 U401
H3/48	DIN*/DOUT*	J401-1
K3/47	DIN/DOUT	J401-2
F3/62	IDC ODC 2.4MHz	J401-8
J3/50	SBI	J401-4
C7/96	XTL 33MHz	Y401
C6/95	EXTL	Y401
K9/16	OSCW	CR402
G9/19	DCLK	U405-K9



NTN7749G VOCON (Vocoder/Controller) Board Schematic Diagram, Sheet 1 of 2







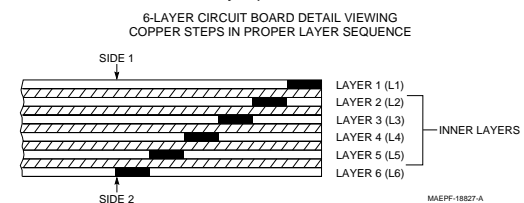
Q403	4805128M12	NPN RESISTOR, Fixed: $\Omega \pm 5\%$ ; 1/8W Unless otherwise stated.
R199	-----	Not Placed.
R200	0662057A65	4.7k
R201 thru R205	0662057A97	100k
R206, R207	0662057A73	10k
R208, R209	0662057A29	150
R210	0683962T45	68
R211	0662057A97	100k
R212	0662057A73	10k
R213, R214	0662057C55	150
R215	0662057A97	100k
R216	0662057A73	10k
R217	0662057C55	150
R218	0662057A65	4.7k
R219	0662057A97	100k
R220, R221	0662057A73	10k
R222	0662057G08	82.5k
R223	0662057R92	47.5k
R224	0662057A85	33k
R225	0662057B47	0 $\pm$ .050
R226, R227	0662057A97	100k
R228	0662057A73	10k
R229	0662057A97	100k
R230	0662057A65	4.7k
R231	0662057B22	1 M
R232	0662057A65	4.7k
R233	0662057A85	33k
R234, R235	0662057A73	10k
R236	0662057A97	100k
R237	0662057A73	10k
R238	0662057A97	100k
R239, R240	0662057A65	4.7k
R241	0662057A89	47k
R242	0662057A65	4.7k
R243 thru R248	0662057A97	100k
R249	0662057A57	2.2k
R250	0662057A73	10k
R251	0662057B47	0 $\pm$ .050
R252	0662057A97	100k
R253 thru R256	0662057C55	150
R257 thru R260	0662057A97	100k
R261	0662057A73	10k
R262	0662057A89	47k
R263	0662057A73	10k
R264	0662057A82	24k
R265, R266	0662057A97	100k
R267	0662057A73	10k
R268	0662057A97	100k
R269	0662057A85	33k
R270, R271	0662057A97	100k
R272	0662057A73	10k
R273	0662057A97	100k
R274 thru R282	0662057A85	33k
R283	0662057A89	47k
R284	0662057A97	100k
R285	0662057A49	1k
R286	0662057B47	0 $\pm$ .050
R287	0662057A49	1k
R288	0662057A97	100k
R289 thru R295	0662057A49	1k
R296	0662057B47	0 $\pm$ .050
R297 thru R307	0662057A49	1k
R308	0662057B47	0 $\pm$ .050
R400, R401	0662057A73	10k
R402	0662057B12	390k
R403	0662057A49	1k

R404	0662057A73	10k
R405	0662057B22	1 M
R406	0662057A57	2.2k
R407	0662057A97	100k
R408	0662057A57	2.2k
R409 thru R411	0662057A73	10k
R412	0662057A65	4.7k
R413, R414	0662057A73	10k
R415	0662057A97	100k
R416, R417	0662057A73	10k
R418	0662057A49	1k
R419	0662057A73	10k
R420	0662057A97	100k
R421	0662057A73	10k
R422	0662057C03	1
R423	0662057A73	10k
R424	0662057A63	3.9k
R425	0662057A69	6.8k
R426, R427	0662057B02	150K
R428, R429	0662057A81	22K
R430	0662057A39	390
R431	0662057C03	1
R432	0662057A73	10k
R433	0662057A57	2.2K
R434	0662057A39	390
R435	0662057A73	10K
R436	0662057B14	470K
R437	-----	Not Placed.
R438, R439	0662057A73	10k
R440	-----	Not Placed.
R441	0662057A73	10k
R442	-----	Not Placed.
R443	0662057B47	0 $\pm$ .050
R444	0662057A73	10k
R445	0662057B47	0 $\pm$ .050
R450	0662057A89	47k
R459	0662057A73	10k
R460	0662057A73	10k
R467	-----	Not Placed.
R477, R478	-----	Not Placed.
R479	0662057A73	10k
R480	-----	Not Placed.
R481	0662057A97	100k
R482	0662057B47	0 $\pm$ .050
R483 thru R485	0662057A97	100k
R486	-----	Not Placed.
R490	0662057G14	110k 1%
R491	0662057G08	82.5k 1%
R492	0662057A82	24k
R499	0662057A73	10k
<b>INTEGRATED CIRCUIT MODULE:</b>		
See Note 1.		
U201	5105109Z72	32k x 8 EEPROM
U202	5185748L01	32k X 8 SRAM, 28 Pin
U204	5113802A75	MCU (Microcontrol Unit, type MC68HC11F1)
U205	5185963A84	FLASH (TSOP)
U206	5185765B19	SLIC (Support Logic IC)
U208	5105750U28	MUX
U211	5105279V65	AND Gate
U214	5105279V65	AND Gate
U215, U216	5105750U28	MUX
U401	5105457W68	Audio PA (Power Amplifier)
U402, U403	5185963A18	8k x 24 DSPRAM
U404	5185130C54	FLASH (TSOP)
U405	5105457W66	DSP (Digital Signal Processor)
U406	5185963A10	ADSIC (ABACUS/DSP Support IC)
U407	5105492X73	Voltage Detector

U408	5105750U28	MUX
U409	5105625U38	5-Volt Regulator, Digital
U410	5105625U41	5-Volt Regulator, Analog
U411	5105364W01	Low-power Op Amp
U412	5105750U28	MUX
U414	5185963A18	8k x 24 DSPRAM
U417	-----	Not Placed.
VR201 thru VR203	4813830A15	Zener, 5.6V
VR204	4813830A28	Zener, 15V
VR205	4813830A15	Zener, 5.6V
VR206	4813830A31	Zener 18V
VR207	4813830A22	Zener, 9.1V
VR208	4813830A24	Zener, 11
VR209	4813830A15	Zener, 5.6V
VR210	4813830A24	Zener, 11V
VR211 thru VR214	4813830A15	Zener, 5.6V
VR215, VR216	4813830A24	Zener, 11V
VR217, VR218	4813830A15	Zener, 5.6V
VR219, VR220	4813830A24	Zener, 11V
VR221	4813830A28	Zener, 15V
VR222, VR223	4813830A15	Zener, 5.6V
Y201	4805574W01	7.3728 MHz
Y401	4805573W01	33 MHz

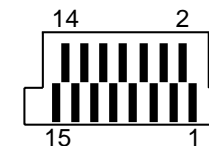
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 $M=10^6$
- ITEM refers to the component reference designator.
- The VOCON Board uses a 6-layer printed circuit board.



**J201 VOCON/Universal Connector**

- J201-1 N.C
- J201-2 N.C.
- J201-3 N.C.
- J201-4 LH\_DATA/BOOT\_DATA\_OUT
- J201-5 Ext Mic
- J201-6 SB9600\_BUSY
- J201-7 Option Select 1
- J201-8 RS232\_DATA\_IN
- J201-9 Option Sel 2 (Keyload\*)
- J201-10 RTSIN\*/KEYFAIL\*
- J201-11 Speaker Common
- J201-12 External Speaker
- J201-13 OPTB+/Boot Sel/Vpp
- J201-14 CTSOUT\*
- J201-15 RS232 Data Out/ Boot Data In



MAEPF-24344-0

