THS4561 Low-Power, High Supply Range, 70-MHz, Fully Differential Amplifier

1 Features

- Bandwidth: 70 MHz (G = 1 V/V)
- Differential Output Slew Rate: 130 V/µs
- Gain Bandwidth Product: 60 MHz
- Negative Rail Input (NRI)
- Rail-to-Rail Output (RRO)
- Wide Output Common-Mode Control Range
- Single-Supply Operating Range: 2.85 V to 12.6 V
- Trimmed-Supply Current: 830 µA at ±5 V
- 25°C Input Offset: ±200 µV (Maximum)
- Input Offset Voltage Drift: ±2 µV/°C (Maximum)
- Differential Input Voltage Noise: 4.5 nV/$\sqrt{\text{Hz}}$
- Very Low 50–Hz 1/f Voltage Noise Corner
- Very Low Harmonic Distortion
  - HD2: –115 dBc at 2-V_{PP}, 100-kHz
  - HD3: –110 dBc at 2-V_{PP}, 100-kHz
- < 4-V Step Response Settling to 0.01%: < 100 ns

2 Applications

- 16-Bit to 20-Bit, Differential, High-Speed SAR Drivers
- Differential Active Filters
- Differential Transimpedance Amplifiers
- High Output Swing PCM Audio DAC Outputs
- Ultrasound Differential TGC Drivers
- Lower Power Alternate to the THS4551

3 Description

The THS4561 fully differential amplifier (FDA) offers a simple interface from single-ended sources to the differential output required by high-precision analog-to-digital converters (ADCs). Designed for exceptional dc accuracy, low noise, and ultra-low harmonic distortion, the device is well suited for data acquisition systems where high precision is required with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4561 features the required negative rail input when interfacing a dc-coupled, ground-centered, source signal to a single-supply, differential-input ADC. Very low dc error and drift terms support the emerging 16-bit to 20-bit successive approximation register (SAR) input requirements. A 2.85-V to 12.6-V supply range with a flexible output common-mode setting with low headroom to the supplies supports a wide range of ADC input and digital-to-analog converter (DAC) output requirements.

The THS4561 will be available in a dual-channel device as the THS4562 in a VQFN-24 package.

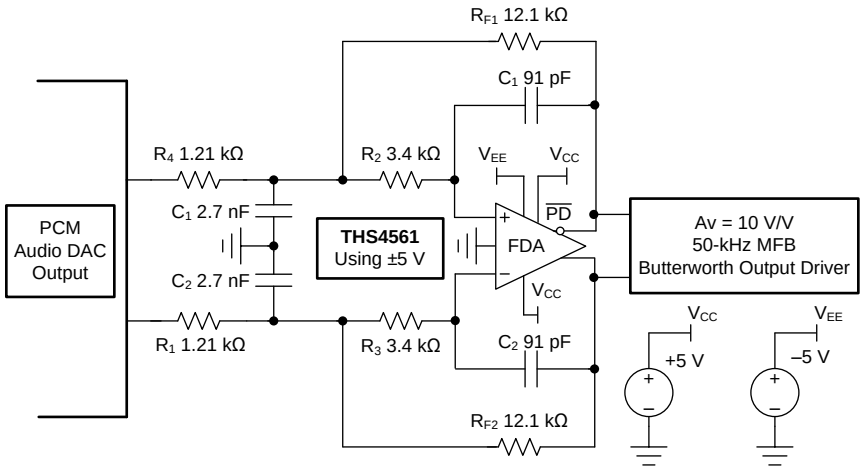
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4561	VSSOP (8)	3.00 mm × 3.00 mm
	VQFN (16)	3.00 mm × 3.00 mm
	VQFN (10)	2.00 mm × 2.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

ADVANCE INFORMATION

Gain of 10 V/V PCM Audio DAC Output With Second-Order MFB Filter at 50 kHz



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4 Revision History

DATE	REVISION	NOTES
August 2017	*	Advance information release.

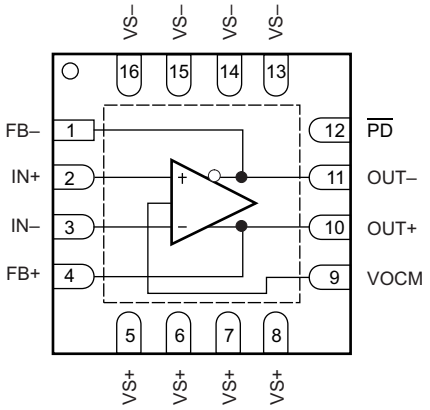
5 Device Comparison Table

DEVICE	BW, G = 1 (MHz)	I_Q, 5 V (mA)	INPUT NOISE (nV/√Hz)	THD (dBc) 2 V_{PP} AT 10 kHz	RAIL-TO-RAIL	DUAL VERSIONS
THS4551	150	1.37	3.3	–138	Negative in and out	THS4552
THS4521	145	1.14	5.6	–120	Negative in and out	THS4522
THS4531A	36	0.25	10	–118	Negative in and out	THS4532
THS4520	620	14.2	2	–105	Out	—
THS4541	620	10.1	2.2	–140	Negative in and out	—

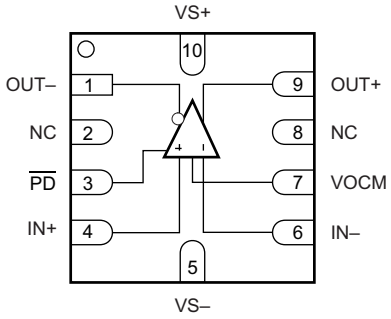
ADVANCE INFORMATION

6 Pin Configuration and Functions

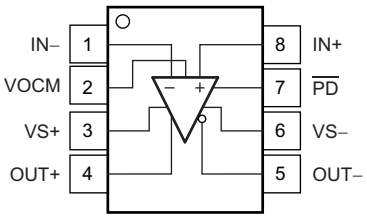
RGT Package
16-Pin VQFN With Exposed Thermal Pad
Top View



RUN Package
10-Pin WQFN
Top View



DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	RGT[1]	RUN	DGK		
FB–	1	—	—	O	Inverting (negative) output feedback
FB+	4	—	—	O	Noninverting (positive) output feedback
IN–	3	6	1	I	Inverting (negative) amplifier input
IN+	2	4	8	I	Noninverting (positive) amplifier input
NC	—	2, 8	—	—	No internal connection
OUT–	11	1	5	O	Inverting (negative) amplifier output
OUT+	10	9	4	O	Noninverting (positive) amplifier output
$\overline{PD}$	12	3	7	I	Power down. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VOCM	9	7	2	I	Common-mode voltage input
VS–	13-16	5	6	I	Negative power-supply input
VS+	5, 6, 7, 8	10	3	I	Positive power-supply input

(1) Solder the exposed RGT package thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, (V_{S+}) – ($V_{S–}$)		13.5	V
	Supply turn-on/off maximum dV/dT(2)		±0.35	V/µs
	Input/output voltage range	TBD	TBD	V
	Differential input voltage		TBD	
Current	Continuous input current		±10	mA
	Continuous output current(3)		±20	
Temperature	Junction, T_J		150	°C
	Operating free-air, T_A	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Stay below this ± supply turn-on edge rate to make sure that the edge-triggered ESD absorption device across the supply pins remains off.
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply positive voltage	2.85	10	12.6	V
T_A	Operating free-air temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS4561 RGT(2) (VQFN) 16 PINS	THS4561 RUN (WQFN) 10 PINS	THS4561 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal impedance for RGT reported with backside thermal pad soldered to heat spreading plane.

ADVANCE INFORMATION

7.5 Electrical Characteristics: $V_{S+} - V_{S-} = 10$ V

at T_A = 25°C, V_{S+} = 5.0 V, V_{S-} = –5.0 V, V_{OCM} = ground, V_O = 2 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_o = 100 mV_{PP}, 1-dB peaking		70		MHz	C
		V_o = 100 mV_{PP}, G = 2 V/V		35		MHz	C
		V_o = 100 mV_{PP}, G = 5 V/V		12		MHz	C
		V_o = 100 mV_{PP}, G = 10 V/V		6		MHz	C
GBP	Gain-bandwidth product	V_o = 100 mV_{PP}, G = 10 V/V		60		MHz	C
LSBW	Large-signal bandwidth			30		MHz	C
	Bandwidth for 0.1-dB flatness			5		MHz	C
SR	Slew rate	Derived from V_o = 2 V_{PP} large-signal bandwidth		130		V/µs	C
	Over- and undershoot	V_o = 2-V step, input t_r = 20 ns		5%			C
	Rise and fall time	V_o = 2-V step, input t_r = 20 ns		22		ns	C
	Settling time	to 0.1% of final value, V_o = 2-V step, input t_r = 20 ns		40		ns	C
		to 0.01% of final value, V_o = 2-V step, input t_r = 20 ns		90		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz		–115		dBc	C
		f = 100 kHz, V_o = 8 V_{PP}		–105		dBc	C
HD3	Third-order harmonic distortion	f = 100 kHz, V_o = 2 V_{PP}		–115		dBc	C
		f = 100 kHz, V_o = 8 V_{PP}		–100		dBc	C
e_n	Input differential voltage noise	f = 200 kHz		5		nV/√Hz	C
e_i	Input current noise, each input	f = 100 kHz		0.4		pA/√Hz	C
	Overdrive recovery time	G = 2 V/V, 2x output overdrive, dc-coupled		300		ns	C
z_O	Closed-loop output impedance	f = 100 kHz (differential)		0.07		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	V_o = ±2 V	104	115		dB	A
	Input-referred offset voltage	T_A = 25°C	–200	±50	200	µV	A
		T_A = 0°C to 70°C	TBD	±100	TBD	µV	B
		T_A = -40°C to 85°C	TBD	±100	TBD	µV	B
		T_A = –40°C to 115°C	TBD	±100	TBD	µV	B
	Input offset voltage drift	T_A = –40°C to 125°C	–2	±0.3	2	µV/°C	B
	Input bias current (positive current out of node)	T_A = 25°C	0.25	0.4	0.6	µA	A
		T_A = 0°C to 70°C		TBD		µA	B
		T_A = –40°C to 85°C		TBD		µA	B
		T_A = –40°C to 125°C		TBD		µA	B
	Input bias current drift	T_A = –40°C to 125°C		4	8	nA/°C	B
	Input offset current	T_A = 25°C	–20	±2	20	nA	A
		T_A = 0°C to 70°C	TBD	TBD	TBD	nA	B
		T_A = –40°C to 85°C	TBD	TBD	TBD	nA	B
		T_A = –40°C to 125°C		TBD		nA	B
	Input offset current drift	T_A = –40°C to 125°C	–120	±50	150	pA/°C	B
INPUT							
	Common-mode input low	T_A = 25°C		V_{S-} – 0.1	V_{S-}	V	A
		T_A = –40°C to 125°C		V_{S-} – 0.1	V_{S-}	V	B
	Common-mode input high	T_A = 25°C	V_{S+} – 1.2	V_{S+} – 1.1		V	A
		T_A = –40°C to 125°C	V_{S+} – 1.35	V_{S+} – 1.2		V	B
CMRR	Common-mode rejection ratio	Inputs at (V_{S+} – V_{S-}) / 2	95	110		dBc	A
	Input impedance differential mode	Inputs at (V_{S+} – V_{S-}) / 2		150||2.4		kΩ || pF	C

ADVANCE INFORMATION

Electrical Characteristics: $V_{S+} - V_{S-} = 10$ V (continued)

at T_A = 25°C, V_{S+} = 5.0 V, V_{S-} = –5.0 V, V_{OCM} = ground, V_O = 2 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
OUTPUT							
V_{OCRL}	Output voltage range low	T_A = 25°C		V_{S-} + 0.2	V_{S-} + 0.35	V	A
		T_A = –40°C to 125°C		V_{S-} + 0.2	V_{S-} + 0.35	V	C
V_{OCRH}	Output voltage range high	T_A = 25°C	V_{S+} – 0.35	V_{S+} – 0.2		V	A
		T_A = –40°C to 125°C	Vs+ - 0.35	V_{S+} – 0.2		V	C
	Continuous output current	T_A = 25°C, V_o = ±3.2 V, R_L = 110 Ω, V_{OCM} offset < 15 mV	±28	±35		mA	A
		T_A = –40°C to 125°C, , V_o = ±2.0 V, R_L = 110 Ω, V_{OCM} offset < 15 mV	±17			mA	B
	Linear output current	T_A = 25°C, V_o = ±4.7 V, R_L = 198 Ω, A_{OL} > 80 dB	±22	±27		mA	A
		T_A = –40°C to 125°C, V_o = ±3.1 V, R_L = 198 Ω, A_{OL} > 80 dB	±15			mA	B
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL							
	Small-signal bandwidth from V_{OCM} pin	V_{OCM} = 100 mV_{PP}		25		MHz	C
	Large-signal bandwidth from V_{OCM} pin	V_{OCM} = 1 V_{PP}		2		MHz	C
	Slew rate from V_{OCM} pin	V_{OCM} = 0.5-V step		4.4		V/µs	C
	DC output balance	V_{OCM} fixed midsupply, V_{OD}/V_{OCM} (V_o = ±1 V)	75	82		dB	A
	Output balance SSBW	V_{OCM} fixed midsupply, V_o/V_{OCM} (–3 dB from dc)		700		kHz	C
	Output balance LSBW	V_{OCM} fixed midsupply, V_o/V_{OCM} with V_o = 1 V_{PP} (–3 dB from dc)		500		MHz	C
	Gain from V_{OCM} pin	V_{OCM} = 0 V	0.997	0.999	1.001	V/V	A
	Input bias current		–0.2	-.1	0.2	µA	A
	+PSR to output Vocm	V_{OCM} pin driven to dc low impedance at midsupply	72	78		dB	A
	–PSR to output Vocm	V_{OCM} pin driven to dc low impedance at midsupply	70	76		dB	A
	Input impedance			200||1.5		kΩ || pF	C
	Default V_{OCM} offset from (Vs+ - Vs-) / 2	V_{OCM} input pin floating	–40	20	40	mV	A
	Default V_{OCM} offset voltage drift	T_A = –40°C to 125°C	120	200	300	µV/°C	B
	V_{OCM} common-mode offset voltage	T_A = 25°C, V_{OCM} input driven to (V_{S+} – V_{S-}) / 2	–3.5	±1	3.5	mV	A
	V_{OCM} common-mode offset voltage drift	T_A = –40°C to 125°C	–15	±2	15	µV/°C	B
	V_{OCM} headroom to negative supply voltage	T_A = 25°C, < ±4-mV shift from midsupply offset		0.45	0.5	V	A
		T_A = –40°C to 125°C, < ±4-mV shift from midsupply offset			0.6	V	B
	V_{OCM} headroom to positive supply voltage	T_A = 25°C, < ±4-mV shift from midsupply offset		1.1	1.2	V	A
		T_A = –40°C to 125°C, < ±4-mV shift from midsupply offset			1.3	V	B

ADVANCE INFORMATION

Electrical Characteristics: $V_{S+} - V_{S-}$ = 10 V (continued)

at T_A = 25°C, V_{S+} = 5.0 V, V_{S-} = –5.0 V, V_{OCM} = ground, V_O = 2 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
POWER SUPPLY							
	Specified operating voltage		2.85	10	12.6	V	A
I_Q	Quiescent operating current	T_A = 25°C	798	850	901	µA	A
		T_A = –40°C to 125°C	TBD		TBD	mA	B
		T_A = 25°C, 13.5 V total supply	817	870	923	µA	D
PSRR	Power-supply rejection ratio	Either supply to differential output	92	110		dB	A
POWER DOWN							
V_T	Enable voltage threshold	Specified *on* within 0.5 V of V_{S+}	4.5		5	V	A
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	-5		3.5	V	A
	Disable pin bias current	Specified for PD 0.5V below +V_{CC}	–2.5	0	2.5	µA	A
	Power-down quiescent current		5	20	33	µA	A
	Turn-on time delay	Time to V_O = 90% of final value		1		µs	C
	Turn-off time delay	Time to V_O = 10% of original value		5		µs	C

ADVANCE INFORMATION

7.6 Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V

at T_A = 25°C, V_{S+} = 5.0 V, V_{S-} = 0 V, V_{OCM} = Open, V_O = 2 V_{PP}, R_F and R_G = 1.5 kΩ, R_L = 1 kΩ, 50–Ω Input Match, Differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_o = 100 mV_{PP}, 1-dB peaking		65		MHz	C
		V_o = 100 mV_{PP}, G = 2 V/V		35		MHz	C
		V_o = 100 mV_{PP}, G = 5 V/V		12		MHz	C
		V_o = 100 mV_{PP}, G = 10 V/V		6		MHz	C
GBP	Gain-bandwidth product	V_o = 100 mV_{PP}, G = 10 V/V		60		MHz	C
LSBW	Large-signal bandwidth			25		MHz	C
	Rise and fall time			5		MHz	C
SR	Slew rate	Derived from V_o = 2 V_{PP} large signal bandwidth		110		V/µs	C
	Over- and undershoot	V_o = 1-V step, input t_r = 10 ns		7%			C
	Rise and fall time	V_o = 1-V step, input t_r = 10 ns		11		ns	C
	Settling time	to 0.1% of final value, V_o = 1-V step, input t_r = 10 ns		30		ns	C
		to 0.01% of final value, V_o = 1-V step, input t_r = 10 ns		80		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz		–110		dBc	C
		f = 100 kHz, V_o = 8 V_{PP}		–100		dBc	C
HD3	Third-order harmonic distortion	f = 100 kHz		–115		dBc	C
		f = 100 kHz, V_o = 8 V_{PP}		–95		dBc	C
e_n	Input differential voltage noise	f = 100 kHz		5		nV/√Hz	C
e_i	Input current noise, each input	f = 100 kHz		0.4		pA/√Hz	C
	Overdrive recovery time	G = 2 V/V, 2x output overdrive, dc-coupled		300		ns	C
z_O	Closed-loop output impedance	f = 100 kHz (differential)		0.07		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain		104	115		dB	A
	Internal feedback trace resistance	RGT only (between pins 1,11 and 4,10)	8.3	8.5	8.7	Ω	A
	Internal feedback trace resistance mismatch	RGT only (between pins 1,11 and 4,10)	–1.0		1.0	Ω	A
	Input-referred offset voltage	T_A = 25°C	–200	±50	200	µV	A
	Input offset voltage drift	T_A = –40°C to 125°C	–2	±0.3	2	µV/°C	B
	Input bias current (positive current out of node)	T_A = 25°C	0.25	0.4	0.6	µA	A
	Input bias current drift	T_A = –40°C to 125°C		-5	8	nA/°C	B
	Input offset current	T_A = 25°C	–20	±2	20	nA	A
	Input offset current drift	T_A = –40°C to 125°C	–120	±50	120	pA/°C	B
INPUT							
	Common-mode input low	T_A = 25°C		V_{S-} – 0.2	V_{S-}	V	A
		T_A = –40°C to 125°C		V_{S-} – 0.1	V_{S-}	V	B
	Common-mode input high	T_A = 25°C	V_{S+} – 1.2	V_{S+} – 1.1		V	A
		T_A = –40°C to 125°C	V_{S+} – 1.35	V_{S+} – 1.2		V	B
CMRR	Common-mode rejection ratio	Inputs at (V_{S+} – V_{S-}) / 2	95	110		dBc	A
	Input impedance differential mode	Inputs at (V_{S+} – V_{S-}) / 2		150||2.4		kΩ || pF	C
OUTPUT							
V_{OCRL}	Output voltage range low	T_A = 25°C		V_{S-} + 0.2	V_{S-} + 0.25	V	A
		T_A = –40°C to 125°C		V_{S-} + 0.2	V_{S-} + 0.35	V	C
V_{OCRH}	Output voltage range high	T_A = 25°C	V_{S+} – 0.25	V_{S+} – 0.2		V	A
		T_A = –40°C to 125°C	V_{S+} – 0.35	V_{S+} – 0.2		V	C

ADVANCE INFORMATION

Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V (continued)

at T_A = 25°C, V_{S+} = 5.0 V, V_{S-} = 0 V, V_{OCM} = Open, V_O = 2 V_{PP}, R_F and R_G = 1.5 kΩ, R_L = 1 kΩ, 50–Ω Input Match, Differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
	Continuous output current	T_A = 25°C, ±1.45 V, R_L = 50 Ω, V_{OCM} offset < ±15 mV	±27	±35		mA	A
		T_A = –40°C to 125°C, ±0.85 V, R_L = 50 Ω, V_{OCM} offset < ±15 mV	±16			mA	B
	Linear output current	T_A = 25°C, ±2.7 V, R_L = 124 Ω, A_{OL} > 80 dB	±20	±24		mA	A
		T_A = –40°C to 125°C, ±1.8 V, R_L = 124 Ω, A_{OL} > 75 dB	±14			mA	B
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL							
	Small-signal bandwidth from V_{OCM} pin	V_{OCM} = 100 mV_{PP}		20		MHz	C
	Large-signal bandwidth from V_{OCM} pin	V_{OCM} = 1 V_{PP}		2		MHz	C
	Slew rate from V_{OCM} pin	V_{OCM} = 0.5-V step		4.4		V/µs	C
	DC output balance	V_{OCM} fixed midsupply, V_o/V_{OCM} (V_o = ±1 V)	75	82		dB	A
	Output balance SSBW	V_{OCM} fixed midsupply, V_o/V_{OCM} (–3 dB from dc)		600		kHz	C
	Output balance LSBW	V_{OCM} fixed midsupply, V_o/V_{OCM} with V_o = 8 V_{PP} (–3 dB from dc)		500		kHz	C
	Gain from V_{OCM} pin	V_{OCM} = 0 V	0.997	0.999	1.001	V/V	A
	Input bias current	V_{OCM} pin	–0.2	-0.1	0.2	µA	A
	+PSR to output common mode	V_{OCM} driven to dc at midsupply	72	78		dB	A
	-PSR to output common mode	V_{OCM} driven to dc at midsupply	70	76		dB	A
	Input impedance	V_{OCM} pin		200||1.5		kΩ || pF	C
	Default V_{OCM} offset from (V_{S+} - V_{S-}) / 2	V_{OCM} input pin floating	–40	±10	40	mV	A
	Default V_{OCM} offset voltage drift	T_A = –40°C to 125°C	120	200	300	µV/°C	B
	V_{OCM} common-mode offset voltage	T_A = 25°C, V_{OCM} input driven to (V_S+ – V_S–) / 2	–3.5	±1	3.5	mV	A
		T_A = –40°C to 125°C		TBD		mV	B
	V_{OCM} common-mode offset voltage drift	T_A = –40°C to 125°C	–15	±2	15	µV/°C	B
	V_{OCM} headroom to negative supply voltage	T_A = 25°C, < ±4-mV shift from midsupply offset		0.45	0.5		A
		T_A = –40°C to 125°C, < ±4-mV shift from midsupply offset			0.6	V	B
	V_{OCM} headroom to positive supply voltage	T_A = 25°C, < ±4-mV shift from midsupply offset		1.1	1.2		A
		T_A = –40°C to 125°C, < ±4-mV shift from midsupply offset			1.3	V	B
POWER SUPPLY							
	Specified operating voltage		2.85	5	12.6	V	A
I_Q	Quiescent operating current	T_A = 25°C, 5-V total supply	760	820	880	µA	A
		T_A = –40°C to 125°C, 5-V total supply	TBD		TBD	µA	B
	Supply current temperature coefficient	T_A = –40°C to 125°C		0.5	1.3	µA/°C	B
PSRR	Power-supply rejection ratio	Either supply to differential output	92	110		dB	A
POWER DOWN							
V_T	Enable voltage threshold	Specified *on* within 0.5 V of V_{S+}	4.5		5	V	A
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	0		3.5	V	A
	Disable pin bias current	PD is 0.5 V below V_{S+}	-2.5	0	2.5	µA	A
	Power-down quiescent current		3	15	28	µA	A
	Turn-on time delay	Time to V_O = 90% of final value		1		µs	C
	Turn-off time delay	Time to V_O = 10% of original value		5		µs	C

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7.7 Electrical Characteristics: $V_{S+} - V_{S-} = 3$ V

at T_A = 25°C, V_{S+} = 3.0 V, V_{S-} = 0 V, V_{OCM} = Open, V_O = 1 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_o = 100 mV_{PP}, 1-dB peaking		65		MHz	C
		V_o = 100 mV_{PP}, G = 2 V/V		35		MHz	C
		V_o = 100 mV_{PP}, G = 5 V/V		11		MHz	C
		V_o = 100 mV_{PP}, G = 10 V/V		5.5		MHz	C
GBP	Gain-bandwidth product	V_o = 100 mV_{PP}, G = 10 V/V		55		MHz	C
LSBW	Large-signal bandwidth			20		MHz	C
	Bandwidth for 0.1-dB flatness			6		MHz	C
SR	Slew rate	Derived from V_o = 2 V_{PP} large signal bandwidth		80		V/µs	C
	Over- and undershoot	V_o = 1-V step input t_r = 10 ns		10%			C
	Rise and fall time	V_o = 1-V step, input t_r = 10 ns		17		ns	C
	Settling time	to 0.1% of final value, V_o = 1-V step, input t_r = 10 ns		40		ns	C
		to 0.01% of final value, V_o = 1-V step, input t_r = 10 ns		100		ns	C
HD2	Second-order harmonic distortion	f = 100 kHz		–110		dBc	C
		f = 100 kHz, V_o = 4 V_{PP}		–105		dBc	C
HD3	Third-order harmonic distortion	f = 100 kHz		–115		dBc	C
		f = 100 kHz, V_o = 4 V_{PP}		–105		dBc	C
e_n	Input differential voltage noise	f = 200 Hz		5		nV/√Hz	C
e_i	Input current noise, each input	f = 20 kHz		0.35		pA/√Hz	C
	Overdrive recovery time	G = 2 V/V, 2x output overdrive, dc-coupled		300		ns	C
z_O	Closed-loop output impedance	f = 100 kHz (differential)		0.08		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain		102	110		dB	A
	Internal feedback trace resistance	RGT only (between pins 1,11 and 4,10)	8.3	8.5	8.7	Ω	A
	Internal feedback trace resistance mismatch	RGT only (between pins 1,11 and 4,10)	–0.25		0.25	Ω	A
	Input-referred offset voltage	T_A = 25°C	–200	±50	200	µV	A
		T_A = 0°C to 70°C	TBD	±100	TBD	µV	B
		T_A = –40°C to 85°C	TBD	±100	TBD	µV	B
		T_A = –40°C to 115°C	TBD	±100	TBD	µV	B
	Input offset voltage drift	T_A = –40°C to 125°C	–2	±0.3	2	µV/°C	B
	Input bias current (positive current out of node)	T_A = 25°C	0.15	0.35	0.6	µA	A
		T_A = 0°C to 70°C		TBD		µA	B
		T_A = –40°C to 85°C		TBD		µA	B
		T_A = –40°C to 125°C		TBD		µA	B
	Input bias current drift	T_A = –40°C to 125°C		4	6	nA/°C	B
	Input offset current	T_A = 25°C	–20	±2	20	nA	A
		T_A = 0°C to 70°C	TBD	TBD	TBD	nA	B
		T_A = –40°C to 85°C	TBD	TBD	TBD	nA	B
		T_A = –40°C to 125°C		TBD		nA	B
	Input offset current drift	T_A = –40°C to 125°C	–120	±50	120	pA/°C	B
INPUT							
	Common-mode input low	T_A = 25°C		V_{S-} – 0.1	V_{S-}	V	A
		T_A = –40°C to 125°C		V_{S-} – 0.1	V_{S-}	V	B
	Common-mode input high	T_A = 25°C	V_{S+} – 1.2	V_{S+} – 1.1		V	A
		T_A = –40°C to 125°C	V_{S+} – 1.35	V_{S+} – 1.2		V	B

ADVANCE INFORMATION

Electrical Characteristics: $V_{S+} - V_{S-} = 3$ V (continued)

at T_A = 25°C, V_{S+} = 3.0 V, V_{S-} = 0 V, V_{OCM} = Open, V_O = 1 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
CMRR	Common-mode rejection ratio	Inputs at (V_{S+} – V_{S-}) / 2	90	105		dBc	A
	Input impedance differential mode	Inputs at (V_{S+} – V_{S-}) / 2		150||2.4		kΩ || pF	C
OUTPUT							
V_{OCRL}	Output voltage range low	T_A = 25°C		V_{S-} + 0.15	V_{S-} + 0.21	V	A
		T_A = –40°C to 125°C		V_{S-} + 0.2	V_{S-} + 0.35	V	C
V_{OCRH}	Output voltage range high	T_A = 25°C	V_{S+} – 0.21	V_{S+} – 0.15		V	A
		T_A = –40°C to 125°C	V_{S+} – 0.35	V_{S+} – 0.2		V	C
	Continuous output current	T_A = 25°C, V_o = ±0.9 V, R_L = 50 Ω, V_{OCM} offset < ±15 mV	±18	±35		mA	A
		T_A = –40°C to 125°C, V_o = ±0.75 V, R_L = 50 Ω, V_{OCM} offset < ±15 mV	±14			mA	B
	Linear output current	T_A = 25°C, V_o = ±1.9 V, R_L = 124 Ω, A_{OL} > 80 dB	±14	±18		mA	A
		T_A = –40°C to 125°C, V_o = ±1.3 V, R_L = 124 Ω, A_{OL} > 75 dB	±10			mA	B
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL							
	Small-signal bandwidth from V_{OCM} pin	V_{OCM} = 100 mV_{PP}		20		MHz	C
	Large-signal bandwidth from V_{OCM} pin	V_{OCM} = 0.6 V_{PP}		3		MHz	C
	Slew rate from V_{OCM} pin	V_{OCM} = 0.5-V step		3.1		V/µs	C
	DC output balance	V_{OCM} fixed midsupply, V_o/V_{OCM} (V_o = ±1 V)	75	80		dB	A
	Output balance SSBW	V_{OCM} fixed midsupply, V_o/V_{OCM} (–3 dB from dc)		600		kHz	C
	Output balance LSBW	V_{OCM} fixed midsupply, V_o/V_{OCM} with V_o = 5 V_{PP} (–3 dB from dc)		400		kHz	C
	Gain from V_{OCM} pin	V_{OCM} = 0 V	0.997	0.999	1.001	V/V	A
	Input bias current V_{OCM} pin		–0.2	–0.1	0.2	µA	A
	Input impedance V_{VOCM} pin			200||1.5		kΩ || pF	C
	Default V_{OCM} offset from (V_{S+} – V_{S-}) / 2	V_{OCM} input pin floating	–40	±10	40	mV	A
	V_{OCM} common-mode offset voltage	T_A = 25°C, V_{OCM} input driven to (V_{S+} – V_{S-}) / 2	–3.5	±1	3.5	mV	A
		T_A = 0°C to 70°C, V_{OCM} input driven to (V_{S+} – V_{S-}) / 2				mV	B
		T_A = –40°C to 85°C, V_{OCM} input driven to (V_{S+} – V_{S-}) / 2				mV	B
		T_A = –40°C to 125°C, V_{OCM} input driven to (V_{S+} – V_{S-}) / 2				mV	B
	V_{OCM} common-mode offset voltage drift	T_A = –40°C to 125°C	–15	±2	15	µV/°C	B
	V_{OCM} headroom to negative supply voltage	T_A = 25°C, < ±5-mV shift from midsupply offset		0.45	0.5	V	A
		T_A = –40°C to 125°C, < ±5-mV shift from midsupply offset			0.6	V	B
	V_{OCM} headroom to positive supply voltage	T_A = 25°C, < ±5-mV shift from midsupply offset		1.1	1.2	V	A
		T_A = –40°C to 125°C, < ±5-mV shift from midsupply offset			1.3	V	B

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Electrical Characteristics: $V_{S+} - V_{S-} = 3$ V (continued)

at T_A = 25°C, V_{S+} = 3.0 V, V_{S-} = 0 V, V_{OCM} = Open, V_O = 1 V_{PP}, R_F = 1.5 kΩ, R_L = 1 kΩ, 50-Ω input match, differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
POWER SUPPLY							
	Specified operating voltage		2.85	5	12.6	V	A
I_Q	Quiescent operating current	T_A = 25°C, 3-V total supply	0.748	0.8	0.852	mA	A
		T_A = –40°C to 125°C, 3-V total supply	TBD		TBD	mA	B
		T_A = 25°C, 2.85 V total supply	0.748	0.80	.852	mA	D
PSRR	Power-supply rejection ratio	Either supply to diff output	95	105		dB	A
POWER DOWN							
V_T	Enable voltage threshold	Specified *on* within 0.5 V of V_{S+}	2.5		3	V	A
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	0		1.5	V	A
	Disable pin bias current	PD is 0.5V below V_{S+}	–2.5	0	2.5	µA	A
	Power-down quiescent current		3	14	23	µA	A
	Turn-on time delay	Time to V_O = 90% of final value		1		µs	C
	Turn-off time delay	Time to V_O = 10% of original value		5		µs	C

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8 Parameter Measurement Information

8.1 Example Characterization Circuits

The THS4561 offers the advantages of a fully differential amplifier (FDA) design with the trimmed input offset voltage and low drift of a precision op amp. The FDA is a flexible device where the main aim is to provide a purely differential output signal centered on a user-configurable common-mode voltage usually matched to the input common-mode voltage required by an analog-to-digital converter (ADC) following this stage. The primary options revolve around the choices of single-ended or differential inputs, ac-coupled or dc-coupled signal paths, gain targets, and resistor value selections. The characterizations described in this section focus on single-ended input to differential output designs as the more challenging application requirement. Differential sources are supported and are simple to implement and analyze.

The characterization circuits are typically operated with a single-ended, matched, 50-Ω, input termination to a differential output at the FDA output pins because most lab equipment is single-ended. The FDA differential output is then translated back to single-ended through a variety of baluns (or transformers) depending on the test and frequency range. DC-coupled step response testing uses two 50-Ω scope inputs with trace math. Single-supply operation is most common in end equipment designs. However, using split balanced supplies allows simple ground referenced testing without adding further blocking capacitors in the signal path beyond those capacitors already within the test equipment. The starting point for any single-ended input to differential output measurements (such as any of the frequency response curves) is shown in Figure 1.

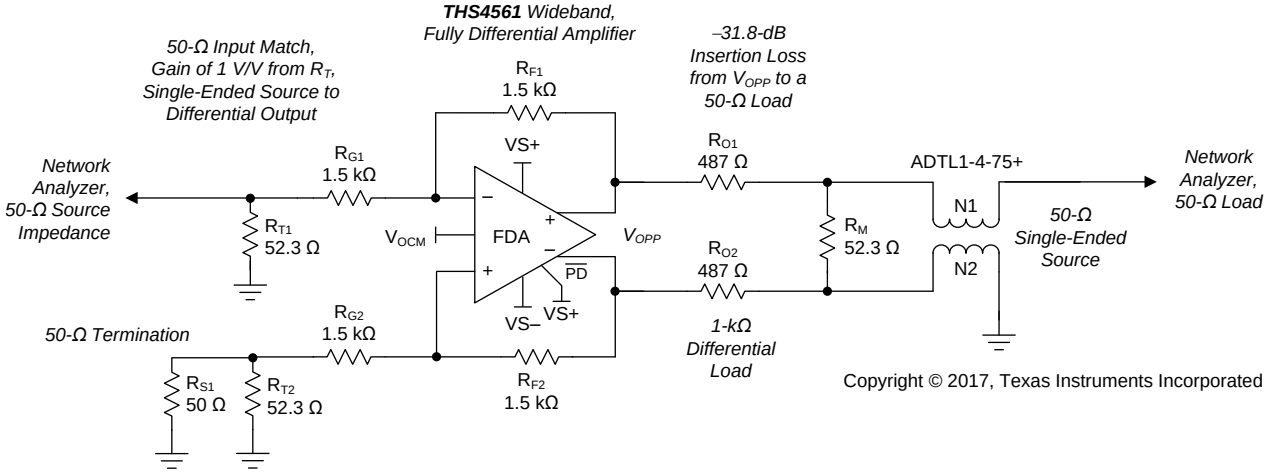

Figure 1. Single-Ended Source to a Differential Gain of a 1-V/V Test Circuit

Most characterization plots fix the R_F (R_{F1} = R_{F2}) value at 1.5 kΩ, as shown in Figure 1. This element value is flexible in application, but 1.5 kΩ provides a good compromise for the parasitic issues linked to this value, specifically:

- Added output loading: The FDA functions similarly to an inverting op amp design with feedback resistors appearing as an added load across the outputs (the approximate total differential load in Figure 1 is 1.5 kΩ || 1 kΩ = 857 Ω). The 1.5-kΩ value reduces the power dissipated in the feedback networks.
- Noise contributions resulting from resistor values: These contributions are both the $4kTR_F$ terms and the current noise times the R_F value to the output (see *Noise Analysis*).
- Parasitic feedback pole at the input summing nodes: this pole is created by the feedback resistor (R_F) value and the 2.4-pF differential input capacitance (as well as any board layout parasitic) and introduces a zero in the noise gain, which decreases the phase margin in most situations. This effect must be managed for best frequency response flatness or step response overshoot.

The frequency domain characterization curves start with the selections of Figure 1. Some of the features in this test circuit include:

- The elements on the non-signal input side match the signal input resistors. This feature closely matches the divider networks on each side of the FDA. The three resistors on the non-signal input side can be replaced by a single resistor to ground using a standard value of 1.5 kΩ with some loss in gain balancing between the two sides; see).

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Example Characterization Circuits (continued)

- Translating from a 1-kΩ differential load to a 50-Ω environment introduces considerable insertion loss in the measurements (–31.8 dB in Figure 1). The measurement path insertion loss normalizes when reporting the frequency response curves to show the gain response to the FDA output pins.
- In the pass band for the output balun, the 50-Ω load of the network analyzer reflects in parallel with the 52.3-Ω shunt termination. These elements combine to show a differential 1-kΩ load at the output pins of the THS4561. The source impedance presented to the balun is a differential 50-Ω source. Figure 2 and Figure 3 show the TINA-TI™ model (available as a TINA-TI™ simulation file) and resulting response flatness for this relatively low-frequency balun providing 0.1-dB flatness through 100 MHz.

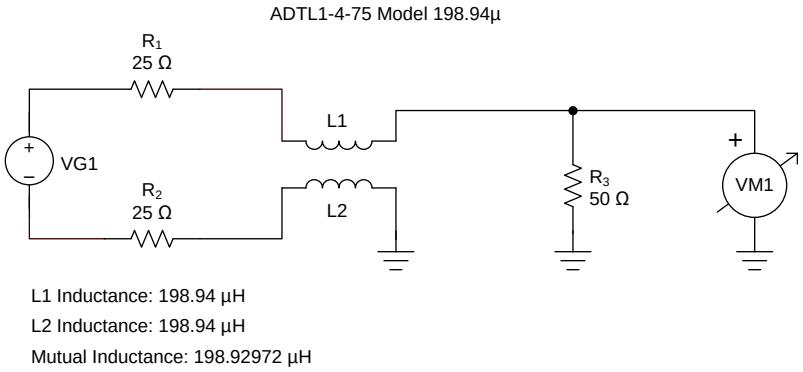

Figure 2. Output Measurement Balun Simulation Circuit in TINA-TI™

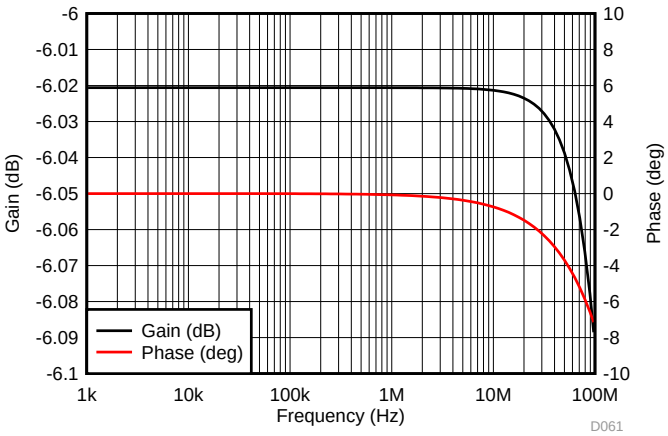

Figure 3. Output Measurement Balun Flatness Test

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Example Characterization Circuits (continued)

Starting from the test circuit of Figure 1, various elements are modified to show the effect of these elements over a range of design targets, specifically:

- The gain setting is changed by adjusting the R_T and the two R_G elements to provide a 50-Ω input match and setting the feedback resistors to 1.5 kΩ.
- Output loading of both resistive and capacitive load testing. Changing to lower resistive loads is accomplished by adding parallel resistors across the output pins in Figure 1. Changing to capacitive loads adds series output resistors to a differential capacitance before the 1-kΩ sense path of Figure 1.
- Power-supply settings. Most often, a single 10-V test uses a ±5-V supply and a 3-V test uses ±1.5-V supplies with the V_{OCM} input control at ground.
- The disable control pin ($\overline{PD}$) is tied to the positive supply (V_{S+}) for any active channel test.

8.2 Output Interface Circuit for DC-Coupled Differential Testing

The pulse response plots were taken using the output circuit of Figure 4. The two sides of this circuit present a 500-Ω load to ground (for a differential 1-kΩ load) with a 50-Ω source to the two scope inputs. Trace math combines the two sides into the pulse response plots of to and to . Use balanced bipolar supplies for this test so that the THS4561 outputs deliver a ground-centered differential swing. This setup produces no dc load currents using the circuit of Figure 4.

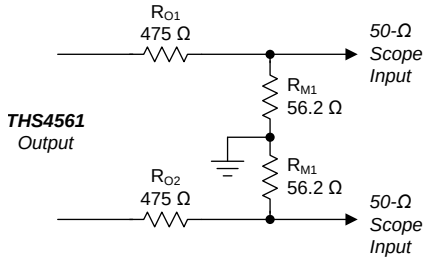

Figure 4. Output Interface for DC-Coupled Differential Outputs

8.3 Output Common-Mode Measurements

The circuit of Figure 5 is a typical setup for common-mode measurements.

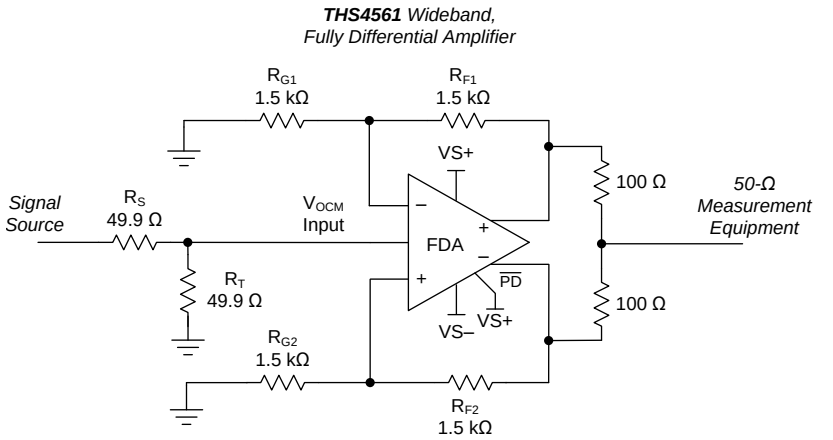

Figure 5. Output Common-Mode Measurements

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Output Common-Mode Measurements (continued)

In Figure 5, the differential path is terminated back to ground on the two 1.5-kΩ input resistors and the V_{OCM} control input is driven from a 50-Ω matched source for the frequency response and step response curves of and . The outputs are summed to a center point (to obtain the average, or common-mode, output) through two 100-Ω resistors. These 100-Ω resistors form an equivalent 50-Ω source to the common-mode output for measurements. This common-mode test circuit is available as a TINA-TI™ simulation file. illustrates the common-mode output noise measurements with a ground on the VOCM input pin or with the VOCM input pin floating. The higher noise in for a floated input can be reduced by including a capacitor to ground at the VOCM control input pin.

8.4 Differential Amplifier Noise Measurements

To extract out the input-referred noise terms from the total output noise, a measurement of the differential output noise is required under two external conditions to emphasize the different noise terms. A high-gain, low resistor value condition is used to emphasize the differential input voltage noise and a higher R_F at low gains is used to emphasize the two input current noise terms. The differential output noise must be converted to single-ended with added gain before being measured by a spectrum analyzer. At low frequencies, a zero 1/f noise, high-gain, differential to single-ended instrumentation amplifier (such as the INA188) is used. At higher frequencies, a differential to single-ended balun is used to drive into a high-gain, low-noise, op amp (such as the LMH6629). In this case, the THS4561 outputs drive 25-Ω resistors into a 1:1 balun where the balun output is terminated single-endedly at the LMH6629 input with 50 Ω. This termination provides a modest 6-dB insertion loss for the THS4561 differential output noise that is then followed by a 40-dB gain setting in the very wideband LMH6629.

8.5 Balanced Split-Supply Versus Single-Supply Characterization

Although most end applications use a single-supply implementation, most characterizations are done on a split balanced supply. Using a split balanced supply keeps the I/O common-mode inputs near midsupply and provides the most output swing with no dc bias currents for level shifting. These characterizations include the frequency response, harmonic distortion, and noise plots. The time domain plots are in some cases done via single-supply characterization to obtain the correct movement of the input common-mode voltage.

8.6 Simulated Characterization Curves

In some cases, a characteristic curve can only be generated through simulation. A good example of this scenario is the output balance plot of . This plot shows the best-case output balance (output differential signal versus output common-mode signal) using exact matching on the external resistors in simulation using a single-ended input to differential output configuration. The actual output balance is set by resistor mismatch at low frequencies but intersects and follows the high-frequency portion of .

The remaining simulated plots include:

- A_{OL} gain and phase; see .
- Large- and small-signal settling times; see and .
- Closed-loop output impedance versus frequency; see .
- CMRR vs frequency; see .
- PSRR vs frequency and output common-mode voltage;see , , and .

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8.7 Terminology and Application Assumptions

There are common terms that are unique to this device. This section identifies and explains these terms.

- Fully differential amplifier (FDA). This term is restricted to devices offering what appears similar to a differential inverting op amp design element that requires an input resistor (not a high-impedance input) and includes a second internal control loop that sets the output average voltage (V_{OCM}) to a default or set point. This second common-mode control loop interacts with the differential loop in certain configurations.
- The desired output signal at the two output pins is a differential signal that swings symmetrically around a common-mode voltage, which is the average voltage for the two outputs.
- Single-ended to differential. The output must always be used differentially in an FDA; however, the source signal can be either a single-ended or a differential source with a variety of implementation details for either source. For an FDA operating in single-ended to differential, only one of the two input signals is applied to one of the input resistors.
- The common-mode control has limited bandwidth from the input VOCM pin to the common-mode output voltage. The internal loop bandwidth beyond the input V_{OCM} buffer is a much wider bandwidth than the reported V_{OCM} bandwidth, but is not directly discernable. A very wide bandwidth in the internal V_{OCM} loop is required to perform an effective and low-distortion single-ended to differential conversion.

Several features in the application of the THS4561 are not explicitly stated, but are necessary for correct operation. These features are:

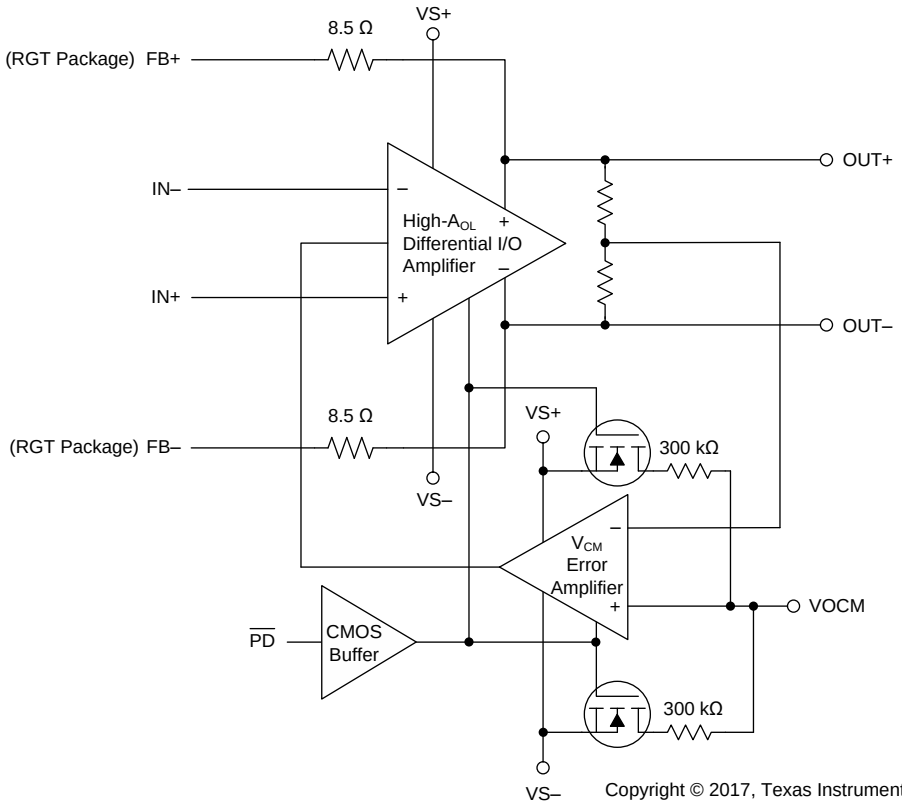
- Good power-supply decoupling is required. Often a larger capacitor (2.2 µF, typical) is used along with a high-frequency, 0.1-µF supply decoupling capacitor at the device supply pins (share this capacitor with the four supply pins in the RGT package). For single-supply operation, only the positive supply has these capacitors. Where a split supply is used, connect these capacitors to ground on both sides with the larger capacitor placed some distance from the package and shared among multiple channels of the THS4561, if used. A separate 0.1-µF capacitor must be provided to each device at the device power pins. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor to the local high-frequency decoupling capacitor is often useful.
- Although often not stated, the power disable pin ($\overline{PD}$) is tied to the positive supply when an enabled channel is desired.
- Virtually all ac characterization equipment expects a 50-Ω termination from the 50-Ω source and a 50-Ω, single-ended source impedance from the device outputs to the 50-Ω sensing termination. This condition is achieved in all characterizations (often with some insertion loss) but is not necessary for most applications. Matching impedance is most often required when transmitting over longer distances. Tight layouts from a source, through the THS4561, and to an ADC input do not require doubly-terminated lines or filter designs. The only exception is if the source requires a defined termination impedance for correct operation (for example, mixer outputs).
- The amplifier signal path is flexible for use as single- or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used as long as the total supply voltage across the TH4561 is less than 12.6 V and the required input, output, and common-mode pin headrooms to each supply are taken into account. When left open, the VOCM pin defaults to near midsupply for any combination of split or single supplies used. The disable pin ($\overline{PD}$) is referenced to the negative rail. Using a negative supply requires that $\overline{PD}$ be pulled down to within TBD V of the negative supply to disable the amplifier.
- External element values are normally assumed to be accurate and matched. In an FDA, this assumption translates to equal feedback resistor values and a matched impedance from each input summing junction to either a signal source or a dc bias reference on each side of the inputs. Unbalancing these values introduces non-idealities in the signal path. For the signal path, imbalanced resistor ratios on the two sides creates a common-mode to differential conversion. Furthermore, mismatched R_F values and feedback ratios create additional differential output error terms from any common-mode dc or ac signal or noise terms. Using standard 1% resistor values is a typical approach and generally leads to some nominal feedback ratio mismatch. Modestly mismatched resistors or ratios do not by themselves degrade harmonic distortion. Where there is a meaningful common-mode noise or distortion coming in that gets converted to differential via an element or ratio mismatch. For the best dc precision, use 0.1% accuracy resistors that are readily available in E96 values (1% steps).

9 Detailed Description

9.1 Overview

The THS4561 is a fully differential amplifier featuring an extremely flexible supply voltage range of 2.85 V to 12.6 V, which makes this device an excellent choice for driving differential ADCs and buffering DAC outputs. This device features a low-power mode with a unique active-pullup resistor that improves EMI reliability of the shutdown pin when left floating. This pin draws very little bias current when enabled, but increases the bias current as it nears the threshold point of shutdown. The increased current prevents the pin from unintentionally turning the device off in the presence of EMI on the enable pin. Similar to other fully differential amplifiers, the THS4561 also includes an output common-mode control pin that can be used to independently set the output common mode to match that of an ADC or other load circuit.

9.2 Functional Block Diagram



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9.3 Feature Description

In addition to the core differential I/O voltage feedback gain block, there are two TBD-kΩ resistors internally across the outputs to sense the average voltage at the outputs. These resistors feed the average voltage back into a V_{CM} error amplifier where the voltage is compared to either a default voltage divider across the supplies or an externally set V_{OCM} target voltage. When the amplifier is disabled, the default midsupply bias string is disabled to save power.

To achieve the very-low noise at the low power provided by the THS4561, the input stage transistors are relatively large, thus resulting in a higher differential input capacitance (2.4 pF in the *Functional Block Diagram*). As a default compensation for the 2.4-pF differential input capacitance and the 1.5-kΩ feedback resistors used in characterization, internal TBD-pF capacitors are placed between the two output and input pins. Adjust any desired external feedback capacitor value to account for these TBD-pF internal elements. When using the 16-pin WQFN package and the internal feedback traces to the input side of the package, include the nominal trace impedance of 3.3 Ω in the design. These elements are not included in the TINA-TI™ model and must be added externally to a design intending to use the RGT package.

9.4 Device Functional Modes

The wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either on with the $\overline{PD}$ pin asserted to a voltage greater than (V_{S+}) – 0.5 V, or turned off by asserting $\overline{PD}$ low (1.5 V below the positive supply). Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors, which provides poor signal isolation from the input to output in power-down mode.

Internal protection diodes remain present across the input pins in both operating and shutdown mode. Large input signals during disable can turn on the input differential protection diodes, thus producing a load current in the supply even in shutdown.

The VOCM control pin sets the output average voltage. Left open, VOCM defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal V_{CM} error amplifier. If floated to obtain a default midsupply reference for VOCM, an external decoupling capacitor is recommended to be added on the VOCM pin to reduce the otherwise high output noise for the internal high-impedance bias (see).

9.4.1 Shutdown Mode

For proper shutdown mode operation, the power down ($\overline{PD}$) pin must be asserted to the desired voltage. An internal pullup resistor is not provided on the $\overline{PD}$ pin so that if the pin is floated, the device defaults to an on state. For applications simply requiring the device to be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

The disable operation is referenced from the positive supply. For an off state condition, the disable control pin must be 1.5 V below the positive supply.

For single-supply operation, a minimum of 0.5 V within the positive supply is required for operation. This logic threshold range allows direct operation from a TBD-V supply logic when the THS4561 operates with a single positive supply and ground.

9.4.2 Single-Ended Source to Differential Output Mode

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. Although the output side is relatively straightforward, the device input pins move in a common-mode manner with the input signal. The common-mode voltage at the input pins, which moves with the input signal, increases the apparent input impedance to be greater than the R_G value. The input active impedance issue applies to both ac- and dc-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as discussed in the *Setting Resistor Values Versus Gain* section.

9.4.2.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversions

When the signal path can be ac-coupled, the dc biasing for the THS4561 becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The ac-coupling issue can be separated for the input and output sides of an FDA design. The input can be ac-coupled and the output dc-coupled, or the output can be ac-coupled and the input dc-coupled, or both can be ac-coupled. One situation where the output can be dc-coupled (for an ac-coupled input), is when driving directly into an ADC where the V_{OCM} control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode voltage to the required ADC input common-mode voltage. In any case, the design starts by setting the desired V_{OCM}. When an ac-coupled path follows the output pins, the best linearity is achieved by operating VOCM at midsupply, which can be easily delivered by floating the VOCM pin. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.6 V greater than the negative supply and 1.3 V less than the positive supply for the full –40°C to +125°C operation). If the output path is also ac-coupled, simply letting the VOCM control pin float is usually preferred in order to obtain a midsupply default V_{OCM} bias with minimal elements. To limit noise, place a 0.1-µF decoupling capacitor on the VOCM control pin to ground.

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Device Functional Modes (continued)

After V_{OCM} is defined, check the target output voltage swing to make certain that the V_{OCM} plus the positive and negative output swing on each side does not clip into the supplies. If the desired output differential swing is defined as V_{OPP}, divide by 4 to obtain the $\pm V_P$ (peak voltage) swing around V_{OCM} at each of the two output pins (each pin operates 180° out of phase with the other). Check that $V_{OCM} \pm V_P$ does not exceed the absolute supply rails for the rail-to-rail output (RRO) device. Common-mode current does not flow from the common-mode output voltage set by the VOCM pin towards the device input pins side, because both the source and balancing resistor on the non-signal input side are dc blocked (see). The ac-coupled input path sets the input pin common-mode voltage equal to the output common-mode voltage. The input pin positive headroom requirement (1.2 V) is less than the V_{OCM} positive headroom (TBD V). If the V_{OCM} is in range, the input pins are also in range for the ac-coupled input configuration. This headroom requirement functions similarly for when the output V_{OCM} voltage approaches the negative supply. The approximate minimum headroom of TBD V to the negative supply on the V_{OCM} voltage is greater than the input pin voltage headroom of approximately 0 V for the negative rail input design. The input common-mode voltage is also in range if the output common-mode voltage is in range and above TBD V from the negative supply because the input common-mode voltage follows the output V_{OCM} setting for ac-coupled input designs.

The input pin voltages move in a common-mode manner with the input signal, as described in the section. Confirm that the V_{OCM} voltage plus the input V_{PP} common-mode swing also stays in range for the input pins.

9.4.2.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversions

The output considerations remain the same as for the ac-coupled design. Again, the input can be dc-coupled when the output is ac coupled. A dc-coupled input with an ac-coupled output can have some advantages to move the input V_{ICM} down by adjusting the V_{OCM} down if the source is ground referenced. When the source is dc-coupled into the THS4561 (see Figure 10), both sides of the input circuit must be dc-coupled to retain differential balance. Normally, the non-signal input side has an R_G element biased to whatever the source midrange is expected to be, provided that this midscale reference gives a balanced differential swing around V_{OCM} at the outputs. Often, R_{G2} is simply grounded for dc-coupled, bipolar-input applications. This configuration provides a balanced differential output if the source swings around ground. If the source swings from ground to some positive voltage, grounding R_{G2} gives a unipolar output differential swing from both outputs at VOCM (when the input is at ground) to one polarity of the swing. Biasing R_{G2} to an expected midpoint for the input signal creates a differential output swing around VOCM.

One significant consideration for a dc-coupled input is that VOCM sets up a common-mode bias current from the output back through R_F and R_G to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this dc current. After the input signal range and biasing on the other R_G element is set, check that the voltage divider from V_{OCM} to V_{IN} through R_F and R_G (and possibly R_S) establishes an input V_{ICM} at the device input pins that is in range. If the average source is at ground, the negative rail input stage for the THS4561 is in range for applications using a single positive supply and a positive output V_{OCM} setting because this dc common-mode current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA). TINA-TI™ simulations of the intended circuit offer a good check for input and output pin voltage swings (see).

9.4.3 Differential Input to a Differential Output Mode

In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, assuming that the two sides of the circuit are balanced with equal R_F and R_G elements, the differential input impedance is now just the sum of the two R_G elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal but must be dc biased in the design range for the input pins and must take into account the voltage headroom required to each supply. Slightly different considerations apply to ac- or dc-coupled differential input to differential output designs, as described in the following sections.

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Device Functional Modes (continued)

9.4.3.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

The most common way to use the THS4561 with an ac-coupled differential source is to simply couple the input into the R_G resistors through the blocking capacitors. Figure 6 shows a typical blocking capacitor approach to a differential input. An optional input differential termination resistor (R_M) is included in this design. The R_M element allows the input R_G resistors to be scaled up and still delivers lower differential input impedance to the source. In this example, the R_G elements sum to show a 1-kΩ differential impedance and the R_M element combines in parallel to provide a net 500-Ω ac differential impedance to the source. Again, the design ideally proceeds by selecting the R_F element values, then the R_G to set the differential gain, and then an R_M element (if needed) to achieve a target input impedance. Alternatively, the R_M element can be eliminated, with the 2 × R_G elements set to the desired input impedance and R_F set to obtain the differential gain (equal to R_F / R_G).

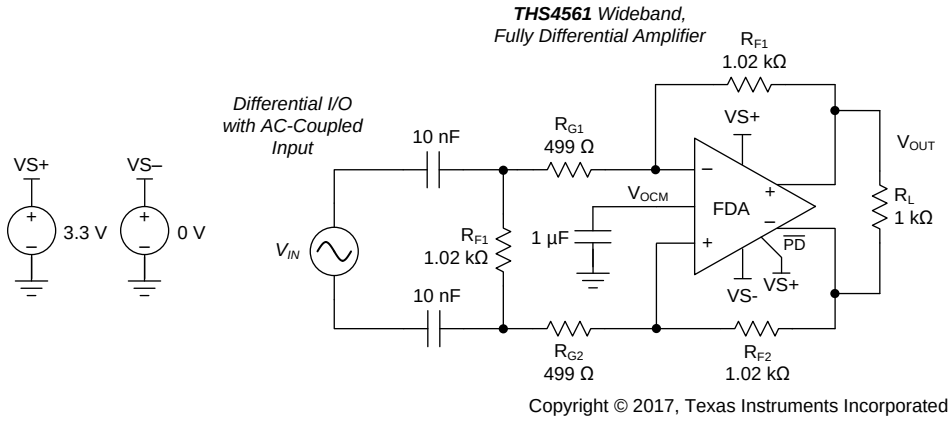

Figure 6. Example AC-Coupled Differential Input Design

The dc biasing for an ac-coupled differential input design is very simple. The output V_{OCM} is set by the input control voltage and, because there is no dc current path for the output common-mode voltage (as long as R_M is only differential and not split and connected to ground for instance), the dc bias also sets the common-mode operating points for the input pins. For a purely differential input, the voltages on the input pins remain fixed at the output V_{OCM} setting and do not move with the input signal (unlike the single-ended input configurations where the input pin common-mode voltages do move with the input signal). The TINA-TI™ simulation file is available for Figure 6.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Most applications for the THS4561 strive to deliver the best dynamic range in a design that delivers the desired signal processing along with adequate phase margin for the amplifier itself. The following sections detail some of the design issues with analysis and guidelines for improved performance.

10.1.1 Differential Open-Loop Gain and Output Impedance

The most important elements to the closed-loop performance are the open-loop gain and open-loop output impedance. Figure 7 and Figure 8 show the simulated differential open-loop gain and phase from the differential inputs to the differential outputs with no load and with a 100-Ω load. Operating with no load removes any effect introduced by the open-loop output impedance to a finite load. This A_{OL} simulation removes the internal feedback capacitors to isolate the forward path gain and phase (see). The internal capacitance becomes part of the feedback network that sets the noise gain and phase combined with the external elements. The simulated differential open-loop output impedance is shown in Figure 9.

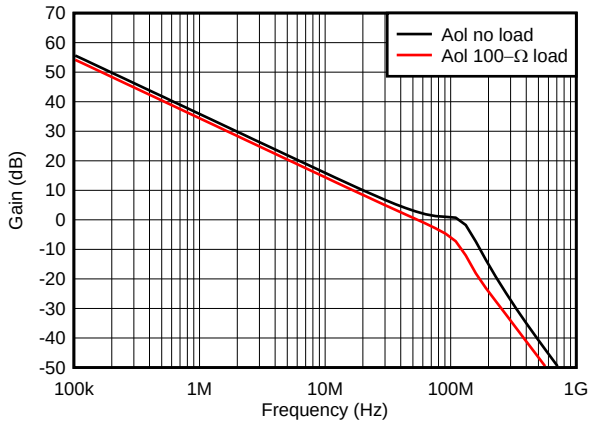

Figure 7. No-Load and 100-Ω Loaded A_{OL} Gain

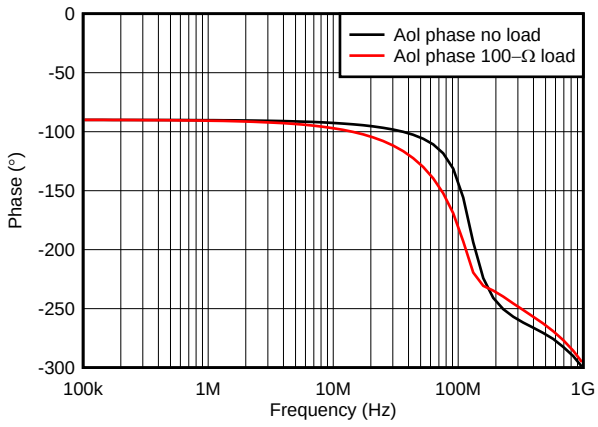

Figure 8. No-Load and 100-Ω A_{OL} Phase

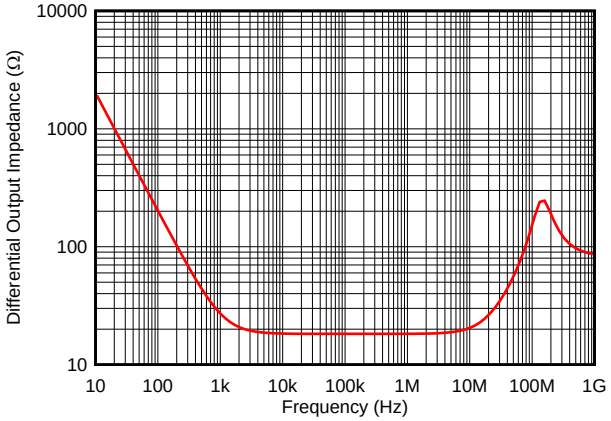

Figure 9. Differential Open-Loop Output Impedance

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Application Information (continued)

This impedance combines with the load to shift the apparent open-loop gain and phase to the output pins when the load changes. The rail-to-rail output stage shows a very high impedance at low frequencies that reduces with frequency to a lower midrange value and then peaks again at higher frequencies. The maximum value at low frequencies is set by the common-mode sensing resistors to be a TBD-kΩ dc value (see the *Functional Block Diagram* section). This high impedance at a low frequency is significantly reduced in closed-loop operation by the loop gain, as shown in the closed-loop output impedance of . Figure 7 compares the no load A_{OL} gain to the A_{OL} gain driving a 100-Ω load that shows the effect of the output impedance. The heavier loads pull the A_{OL} gain down faster to lower crossovers with more phase shift at the lower frequencies.

The much faster phase rolloff for the 100-Ω differential load explains the greater peaked response illustrated in and when the load decreases. This same effect happens for the RC loads common with converter interface designs. Use the TINA-TI™ model to verify loop phase margin in any design.

10.1.2 Setting Resistor Values Versus Gain

The THS4561 offers considerable flexibility in the configuration and selection of resistor values. The design starts with the selection of the feedback resistor value. The 1.5-kΩ feedback resistor value used for the characterization curves is a good compromise between power, noise, and phase margin considerations. With the feedback resistor values selected (and set equal on each side) the input resistors are set to obtain the desired gain with input impedance also set with these input resistors. Differential I/O designs provide an input impedance that is the sum of the two input resistors. Single-ended input to differential output designs present a more complicated input impedance. Most characteristic curves implement the single-ended to differential design as the more challenging requirement over differential-to-differential I/O.

For single-ended, matched, input impedance designs, Table 1 illustrates the suggested standard resistors set to approximately a 1.5-kΩ feedback. This table assumes a 50-Ω source and a 50-Ω input match and uses a single resistor on the non-signal input side for gain matching. Better matching is possible using the same three resistors on the non-signal input side as on the input side. Figure 10 shows the element values and naming convention for the gain of 1-V/V configuration where the gain is defined from the matched input at R_T to the differential output.

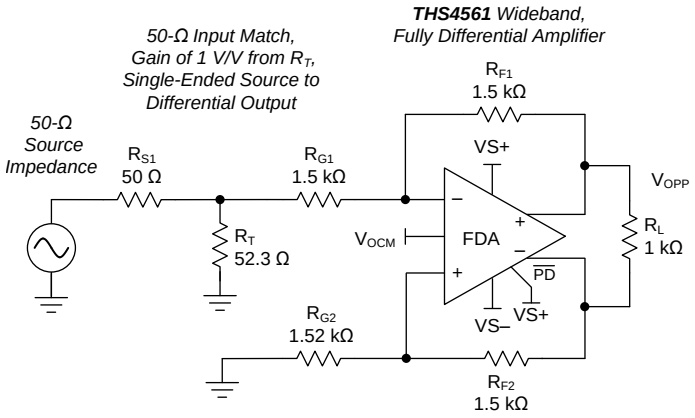

Figure 10. Single-Ended to Differential Gain of 1 V/V with Input Matching Using Standard Resistor Values

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Application Information (continued)

Starting from a target feedback resistor value, the desired input matching impedance, and the target gain (A_V), the required input R_T value is given by solving the quadratic of Equation 1.

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F(2+A_V) - R_S A_V(4+A_V)} - \frac{2R_F R_S^2 A_V}{2R_F(2+A_V) - R_S A_V(4+A_V)} = 0 \quad (1)$$

When this value is derived, the required input side gain resistor is given by Equation 2 and then the single value for R_{G2} on the non-signal input side is given by Equation 3:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \quad (2)$$

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \quad (3)$$

Using these expressions to generate a swept gain table of values results in Table 1, where the best standard 1% resistor values are shown to minimize input impedance and gain error to target.

Table 1. Swept Gain 50-Ω Input Match with R_F = 1.5-kΩ (±1 Standard Values)

GAIN (V/V)	R_F	R_{G1}	R_T	R_{G2}	Z_{IN}	A_V
0.1	1500	15000	49.9	15000	49.74	0.09973
1	1500	1500	51.1	1500	49.82	0.994
2	1500	750	52.3	768	49.98	1.978
5	1500	287	54.9	316	49.6	5.014
10	1500	137	61.9	165	50.4	10.08

Where an input impedance match is not required, simply set the input resistor to obtain the desired gain without an additional resistor to ground (remove R_T in Figure 10). This scenario is common when coming from the output of another single-ended op amp (such as the OPA192). This single-ended to differential stage shows a higher input impedance than the physical R_G as given by the expression for Z_A (active input impedance) shown as Equation 4.

$$Z_A = R_{G1}\frac{\left(1 + \frac{R_{G1}}{R_{G2}}\right)\left(1 + \frac{R_F}{R_{G1}}\right)}{2 + \frac{R_F}{R_{G2}}} \quad (4)$$

Using Equation 4 for the gain of 1 V/V with all resistors equal to 1.5-kΩ shows an input impedance of 2 kΩ. The increased input impedance comes from the common-mode input voltage at the amplifier pins moving in the same direction as the input signal. The common-mode input voltage must move to create the current in the non-signal input R_G resistor to produce the inverted output. The current flow into the signal-side input resistor is impeded because the common-mode input voltage moves with the input signal, thus increasing the apparent input impedance in the signal input path.

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10.1.3 Noise Analysis

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground. Figure 11 shows the simplest analysis circuit with the FDA and resistor noise terms to be considered.

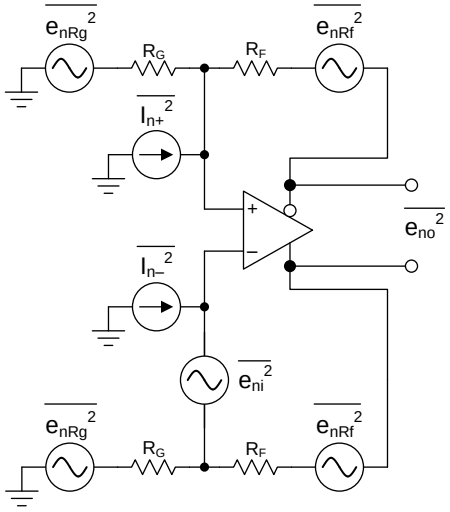

Figure 11. FDA Noise Analysis Circuit

The noise powers are shown in Figure 11 for each term. When the R_F and R_G (or R_I) terms are matched on each side, the total differential output noise is the root sum squared (RSS) of these separate terms. Using NG ≡ 1 + R_F / R_G, the total output noise is given by Equation 5. Each resistor noise term is a 4kT × R power (4kT = 1.6E-20J at 290K).

$$e_o = \sqrt{(e_{ni}NG)^2 + 2(i_N R_F)^2 + 2(4kTR_F NG)} \quad (5)$$

The first term is simply the differential input spot noise times the noise gain, the second term is the input current noise terms times the feedback resistor (and because there are two uncorrelated current noise terms, the power is two times one of them), and the last term is the output noise resulting from both the R_F and R_G resistors, at again twice the value for the output noise power of each side added together. Running a wide sweep of gains when holding R_F close to 1 kΩ and setting the input up for a 50-Ω match gives the standard values and resulting noise listed in Table 2.

When the gain increases, the input-referred noise approaches only the gain of the FDA input voltage noise term at 5 nV/√Hz.

Table 2. Swept Gain of the Output- and Input-Referred Spot Noise Calculations

GAIN (V/V)	R_F	R_{G1}	R_T	R_{G2}	Z_{IN}	A_V	E_O (nV/√Hz)	E_I (nV/√Hz)
0.1	1500	15000	49.9	15000	49.74	0.09973	9.15	91.53
1	1500	1500	51.1	1500	49.82	0.994	14.03	14.03
2	1500	750	52.3	768	49.98	1.978	18.99	9.49
5	1500	287	54.9	316	49.6	5.014	33.20	6.64
10	1500	137	61.9	165	50.4	10.08	55.05	5.51

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10.1.4 Factors Influencing Harmonic Distortion

As illustrated in the swept frequency harmonic distortion plots (and), the THS4561 provides extremely low distortion at lower frequencies. In general, an FDA output harmonic distortion mainly relates to the open-loop linearity in the output stage corrected by the loop gain at the fundamental frequency. When the total load impedance decreases, including the effect of the feedback resistor elements in parallel for loading purposes, the output stage open-loop linearity degrades, thus increasing the harmonic distortion; see and . When the output voltage swings increase, very fine scale open-loop output stage nonlinearities increase that also degrade the harmonic distortion; see and . Conversely, decreasing the target output voltage swings drops the distortion terms rapidly. A nominal swing of 2 V_{PP} is used for harmonic distortion testing where illustrates the effect of going up to an TBD-V_{PP} differential input that is more common with SAR converters.

Increasing the noise gain functions to decrease the loop gain resulting in the increasing harmonic distortion terms; see and . One advantage to the capacitive compensation for the attenuator designs is that the noise gain is shaped up with frequency to achieve a crossover at an acceptable phase margin at higher frequencies. This technique (see the section) holds the loop gain high at frequencies lower than the noise gain zero, thus improving distortion at lower frequencies.

The THS4561 holds nearly constant distortion when the V_{OCM} operating point is moved in the allowed range; see and . Clipping into the supplies with any combination of V_{OCM} and V_{OPP} rapidly degrades distortion performance.

The THS4561 does an exceptional job of converting from single-ended inputs to differential outputs with very low harmonic distortions. External resistors of 1% tolerance are used in characterization with good results. Unbalancing the feedback divider ratios does not degrade distortion directly. Imbalanced feedback ratios convert common-mode inputs to a differential mode at the outputs with the gain described in the section.

10.1.5 Driving Capacitive Loads

The capacitive load of an ADC or some other next-stage device is commonly required to be driven. Directly connecting a capacitive load to the output pins of a closed-loop amplifier such as the THS4561 can lead to an unstable response; see the step response plots into a capacitive load (, , , and). One typical remedy to this instability is to add two small series resistors (R_O) at the outputs of the THS4561 before the capacitive load. and illustrate parametric plots of recommended R_O values versus differential capacitor load values and gains. Operating at higher noise gains requires lower R_O values to obtain a ±0.5-dB flat response for the same capacitive load. Some direct parasitic loading is acceptable without a series R_O that increases with gain setting (see , , , and where the R_O value is 0 Ω). Even when these plots suggest that a series R_O is not required, good practice is to leave a place for the R_O elements in a board layout (a 0-Ω value initially) for later adjustment in case the response appears unacceptable.

The rail-to-rail output stage of the THS4561 has an inductive characteristic in the open-loop output impedance at higher frequencies; see Figure 9. This inductive open-loop output impedance introduces added phase shift at the output pins for direct capacitive loads and feedback capacitors. Larger values of feedback capacitors (greater than 100 pF) can risk a low phase margin. Including a 10-Ω to 15-Ω series resistor with a feedback capacitor can be used to reduce this effect.

The TINA-TI™ simulation model does a good job of predicting these issues and illustrating the effect for different choices of capacitive load isolating resistors (R_O) and different feedback capacitor configurations.

10.1.6 Input Overdrive Performance

illustrates a 2X overdrive triangle waveform for the THS4561. The input resistor is driven with a TBD-V swing for the gain of 2-V/V configuration in the test circuit of Figure 1 using a single 10-V supply. When the output maximum swing is reached at approximately the supply values, the increasing input voltage turns on the internal protection diodes across the two input pins. The internal protection diodes are two diodes in series in both polarities. This feature clamps the maximum differential voltage across the inputs to approximately 1.5 V when the output is limited at the supplies but the input exceeds the available range. The input resistors on both sides limit the current flow in the internal diodes under these conditions.

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10.2 Typical Application

One common application for the THS4561 is to take a single-ended, high V_{PP} voltage swing (from a high-voltage precision amplifier such as the OPA192) and deliver that swing to precision SAR ADC as a single-ended to differential conversion with output common-mode control and implement an active 2nd-order multiple feedback (MFB) filter design. Designing for a 40-V_{PP} maximum input down to an 8-V_{PP} differential swing requires a gain of 0.2 V/V. Targeting a 100-kHz Butterworth response with the RC elements tilted towards low noise gives the example design of Figure 12. The V_{CM} control is set to half of a 4.096-V reference, which is typical for 5-V differential SAR applications.

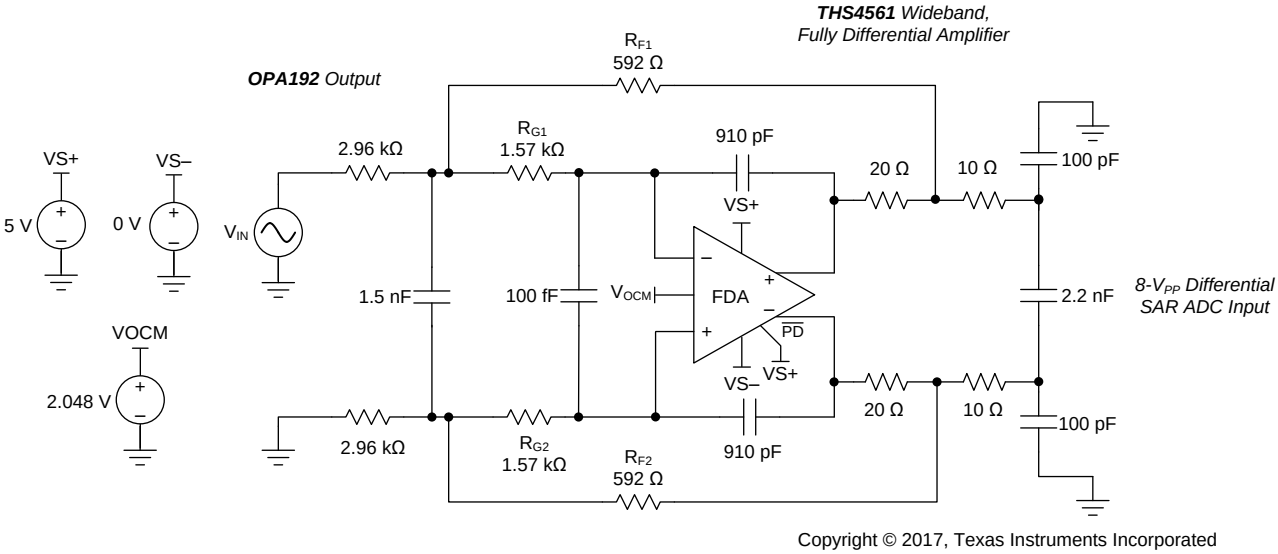

Figure 12. MFB Filter Driving an ADC Application: Example 100-kHz Butterworth Response

10.2.1 Design Requirements

The requirements for this application are:

- Single-ended to differential conversion
- Attenuation by 0.2-V/V gain
- Active filter set to a Butterworth, 100-kHz response shape
- Output RC elements set by SAR input requirements (not part of the filter design)
- Filter element resistors and capacitors are set to limit added noise over the THS4561 and noise peaking

10.2.2 Detailed Design Procedure

The design proceeds using the techniques and tools suggested in the *Design Methodology for MFB Filters in ADC Interface Applications* application note (SBOA114). The process includes:

- Scale the resistor values to not meaningfully contribute to the output noise produced by the THS4561 by itself
- Select the RC ratios to hit the filter targets when reducing the noise gain peaking within the filter design
- Set the output resistor to 10 Ω into a 2.2-nF differential capacitor
- Add 100-pF common-mode capacitors to the load capacitor to improve common noise filtering
- Inside the loop, add 20-Ω output resistors after the filter feedback capacitor to increase the isolation to the load capacitor
- Include a place for a differential input capacitor (illustrated as 100 fF in Figure 12)

ADVANCE INFORMATION

11 Power Supply Recommendations

The THS4561 is principally intended to operate with a nominal single-supply voltage of 3 V to 12 V. Supply voltage tolerances are supported with the specified operating range of 2.85 V (10% low on a 3-V nominal supply) and 12.6 V (5% high on a 12-V nominal supply). Supply decoupling is required, as described in the *Terminology and Application Assumptions* section. Split (or bipolar) supplies can be used with the THS4561, as long as the total value across the device remains less than 12.6 V (absolute maximum). The thermal pad on the RGT package is electrically isolated form the die; connect the thermal pad (RGT package only) to any power or ground plane for reduced thermal impedance to the junction temperature. This pad must be connected to some power or ground plane and not floated.

Using a negative supply to deliver a true swing to ground output when driving SAR ADCs can be desired. Although the THS4561 quotes a rail-to-rail output, linear operation requires approximately 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed, negative-supply generator can accept a 3-V to 5-V positive supply and provides a fixed –230-mV supply for the negative power supply. Using the LM7705 provides an effective solution, as discussed in the *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* TI design (TIDU187)

12 Layout

12.1 Layout Guidelines

12.1.1 Board Layout Recommendations

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. The *THS4561DGKEVM* user guide (TBD) shows a good example of high-frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes that may not apply to some applications. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.1 µF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2 µF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- Higher-speed FDAs such as the THS4561 include a duplicate of the output pins on the input feedback side of the larger 16-pin VQFN (RGT) package. This feature is intended to allow the external feedback resistors to be connected with virtually no trace length on the input side of the package. This internal feedback trace also provides a second feedback path for connecting a feedback capacitor on the input pin sides for band-limited or multiple feedback filter designs. This internal trace shows an approximate 3.3-Ω series resistance that must be considered in any design using that path. The TINA-TI™ model does not include that element (to be generally applicable to all package styles) and must be added externally if the RGT package is used. Use this layout approach without extra trace length on the critical feedback path. The smaller 10-pin WQFN package lines up the outputs and the required inputs on the same side of the package where the feedback R_F resistors must be placed immediately adjacent to the package with minimal trace length.
- The input summing junctions are very sensitive to parasitic capacitance. Any R_G elements must connect into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the R_G elements can have more trace length if needed to the source or to GND.

ADVANCE INFORMATION

12.2 Layout Example

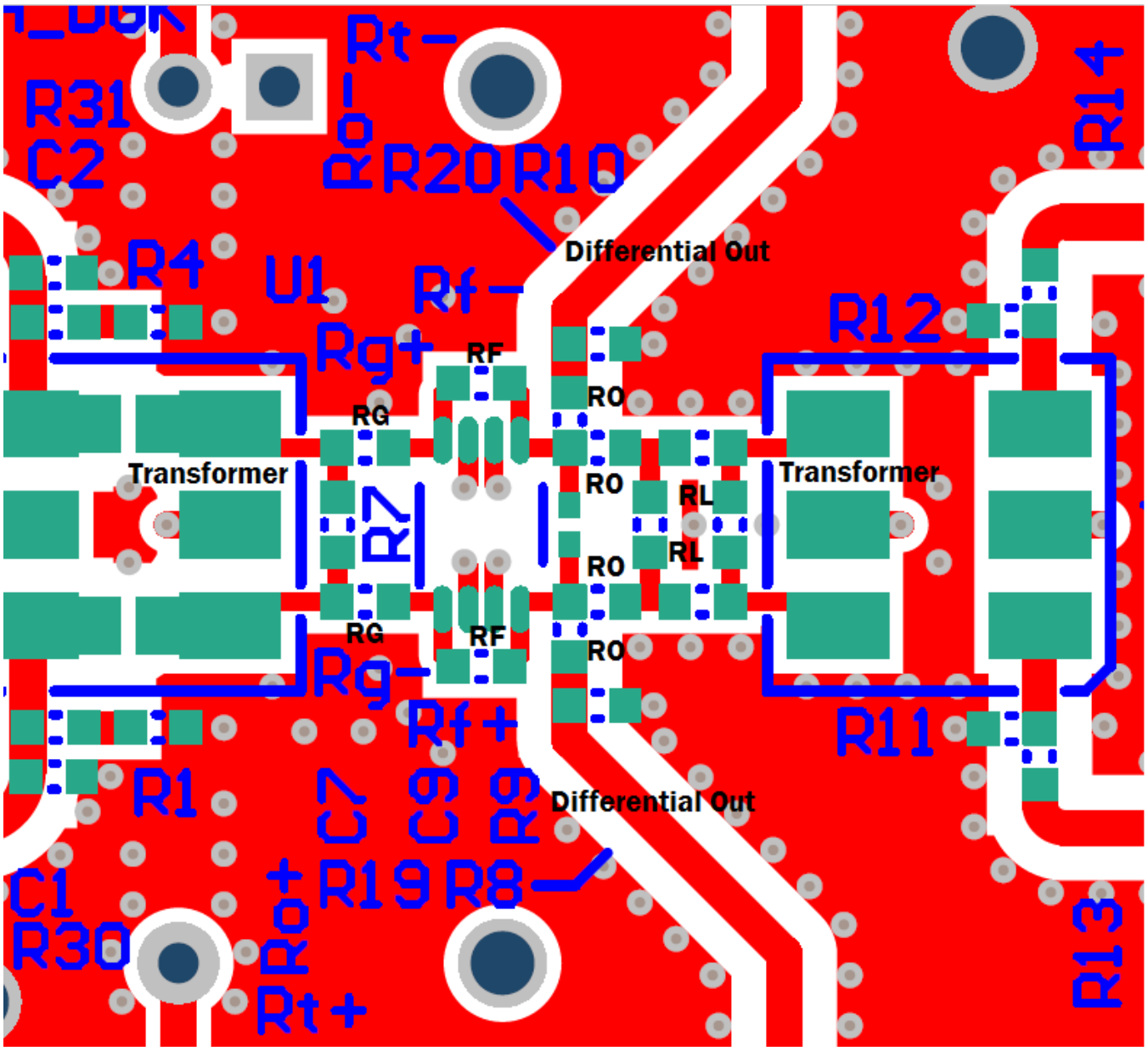

Figure 13. Example Layout

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Documentation Support

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4561IDGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
THS4561IDGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
XTHS4561IDGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
XTHS4561IRGT	ACTIVE	VQFN	RGT	16	50	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

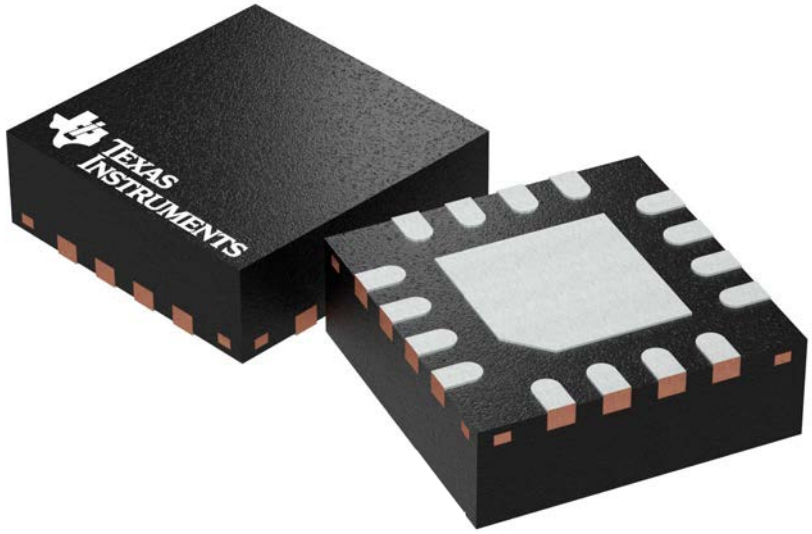
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

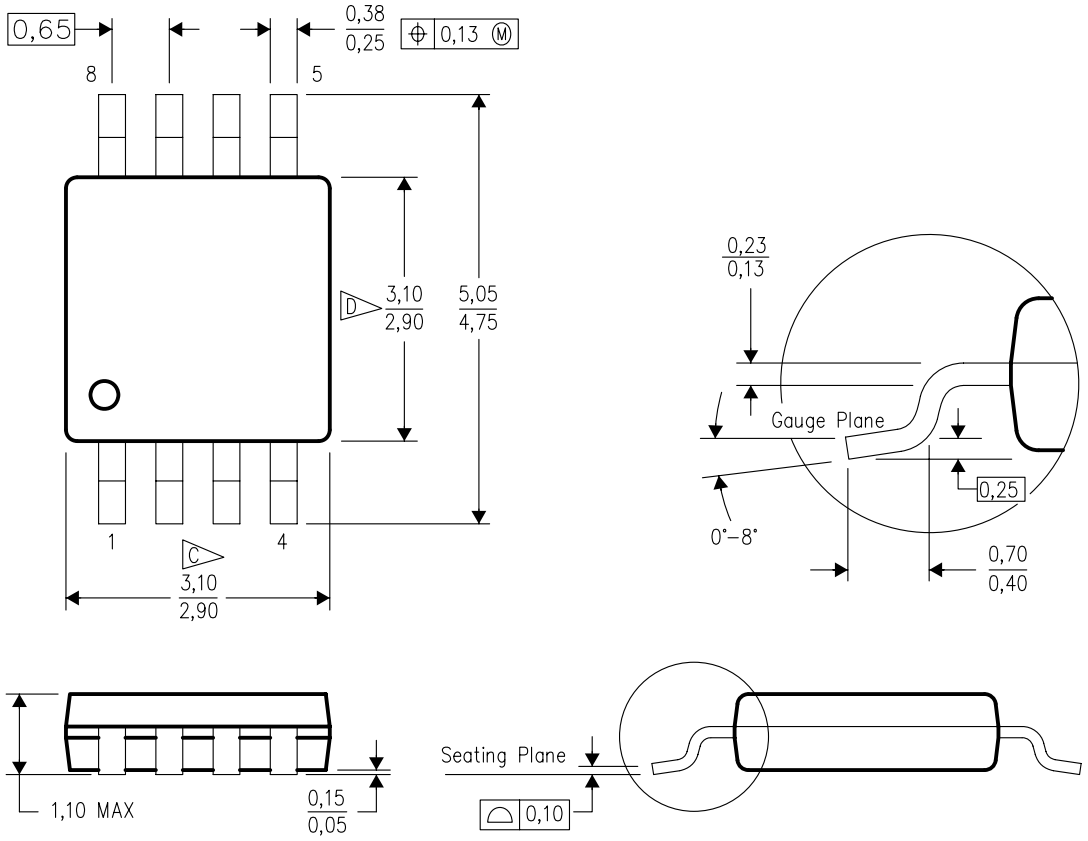
RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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