Application Report
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Voltage Fed Full Bridge DC-DC and DC-AC Converter for High-Frequency Inverter Using C2000

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ABSTRACT

The High-Frequency Inverter is mainly used today in uninterruptible power supply systems, AC motor drives, induction heating and renewable energy source systems. The simplest form of an inverter is the bridge-type, where a power bridge is controlled according to the sinusoidal pulse-width modulation (SPWM) principle and the resulting SPWM wave is filtered to produce the alternating output voltage. In many applications, it is important for an inverter to be lightweight and of a relatively small size. This can be achieved by using a High-Frequency Inverter that involves an isolated DC-DC stage (Voltage Fed Push-Pull/Full Bridge) and the DC-AC section, which provides the AC output. This application report documents the implementation of the Voltage Fed Full Bridge isolated DC-DC converter followed by the Full-Bridge DC-AC converter using TMS320F28069 (C2000™) for High-Frequency Inverters.

Project collateral and source code discussed in this document can be downloaded from this URL: http://www.ti.com/lit/zip/sprabw0.

Contents

List of Figures

Trademarks

1 Basic Inverter Concept

There are basically three different inverter technologies:

- Inverter with a 50 Hz transformer
- Inverter without a transformer
- Inverter with a high-frequency (HF) transformer

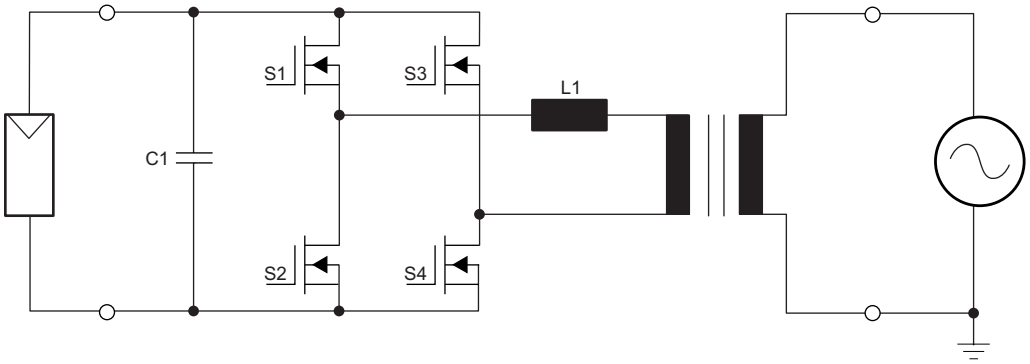

Figure 1. 50 Hz Technology

The applied DC voltage is converted to a 50 Hz AC voltage via a full bridge (S1...S4). This is then transmitted via a 50 Hz transformer and subsequently fed into the public grid.

- Benefits:
  - High degree of reliability due to fewer components
  - Safety through galvanic isolation of the DC and AC sides
- Disadvantages:
  - Low degree of efficiency resulting from high transformer losses
  - Heavy weight and volume (for example, due to 50 Hz transformer)

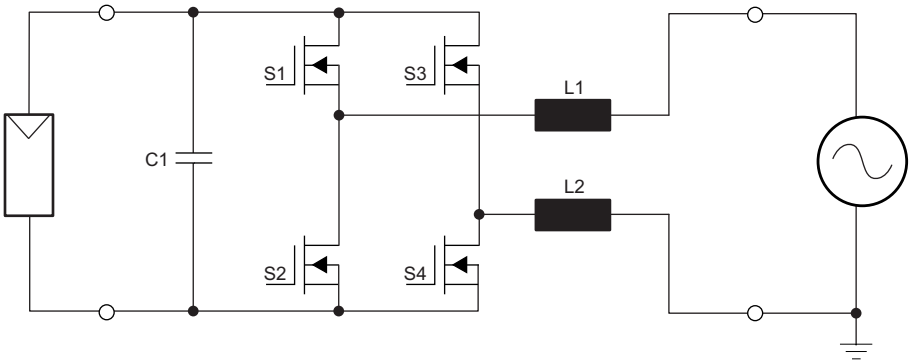

Figure 2. Transformerless Inverter Technology

The existing DC voltage is converted to a square 50 Hz AC voltage via a full bridge (S1...S4), then smoothed to a sinusoidal 50 Hz AC voltage via the chokes (L1+L2) and fed into the public grid.

- Benefits:
  - Compact and light due to lack of transformer
  - Very high degree of efficiency (for example, no transformer losses)
- Disadvantages:
  - Additional safety measures (residual current circuit breaker) required. In some countries, a lack of galvanic isolation between the DC and AC sides is not permitted.
  - Complicated lightning protection
  - Not compatible with modules that must be earthed

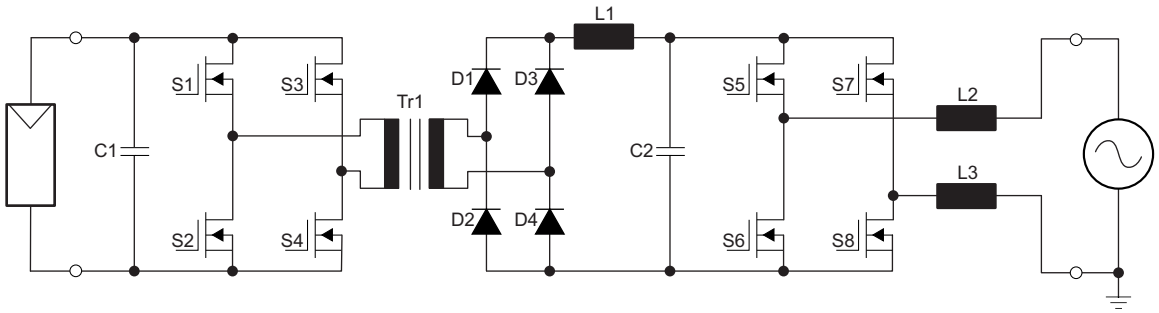

Figure 3. High-Frequency Inverter Technology

The full bridge (S1...S4) generates a high-frequency square-wave signal with 40 – 50 kHz, which is transmitted via the HF transformer (Tr1). The bridge rectifiers (D1...D4) convert the square-wave signal back to DC voltage and store it in the intermediate circuit (L1+C2). A second full bridge (S5...S8) then generates a 50 Hz AC voltage, which is smoothed to a sinusoidal 50 Hz AC voltage via the chokes (L2+L3) before being fed into the public grid.

- Benefits:
  - Compact and light, as the HF transformer is very small and light
  - High degree of efficiency through reduction of transformer losses
  - Safety through galvanic isolation between the DC and AC sides
  - Suitable for all module technologies, as module earthing (positive and negative) is possible

2 High-Frequency Inverter – Block Diagram

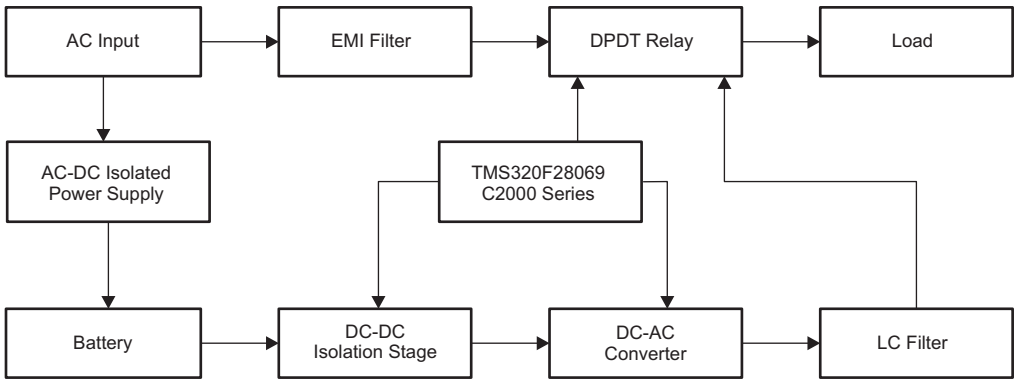

Figure 4. High-Frequency Inverter – Block Diagram

The present application report documents the implementation of the DC-DC isolation and DC-AC conversion stage using TMS320F28069. The F2806x Piccolo™ family of microcontrollers provides the power of the C28x core and the Control Law Accelerator (CLA) coupled with highly integrated control peripherals in low-pin count devices. This family is code-compatible with previous C28x-based code, as well as providing a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the high-resolution pulse width modulator (HRPWM) module to allow for dual-edge control (frequency modulation).

Analog comparators with internal 10-bit references have been added and can be routed directly to control the pulse width modulation (PWM) outputs. The analog-to-digital converter (ADC) converts from 0 to 3.3-V fixed full scale range and supports ratio-metric VREFHI/VREFLO references. The ADC interface has been optimized for low overhead and latency. The above features make the F2806x Piccolo suitable for handling both the stages of the High-Frequency Inverter.

The main blocks of the High-Frequency Inverter include:

- DC-DC isolation stage
- DC-AC converter section

3 DC-DC Isolation Stage - High-Frequency Inverter

The selection of the DC-DC isolation stage for the High-Frequency Inverter depends on the kVA requirements of the inverter. The power supply topologies suitable for the High-Frequency Inverter includes push-pull, half-bridge and the full-bridge converter as the core operation occurs in both the quadrants, thereby, increasing the power handling capability to twice of that of the converters operating in single quadrant (forward and flyback converter). The push-pull and half-bridge require two switches while the full-bridge requires four switches. Generally, the power capability increases from push-pull to half-bridge to full-bridge.

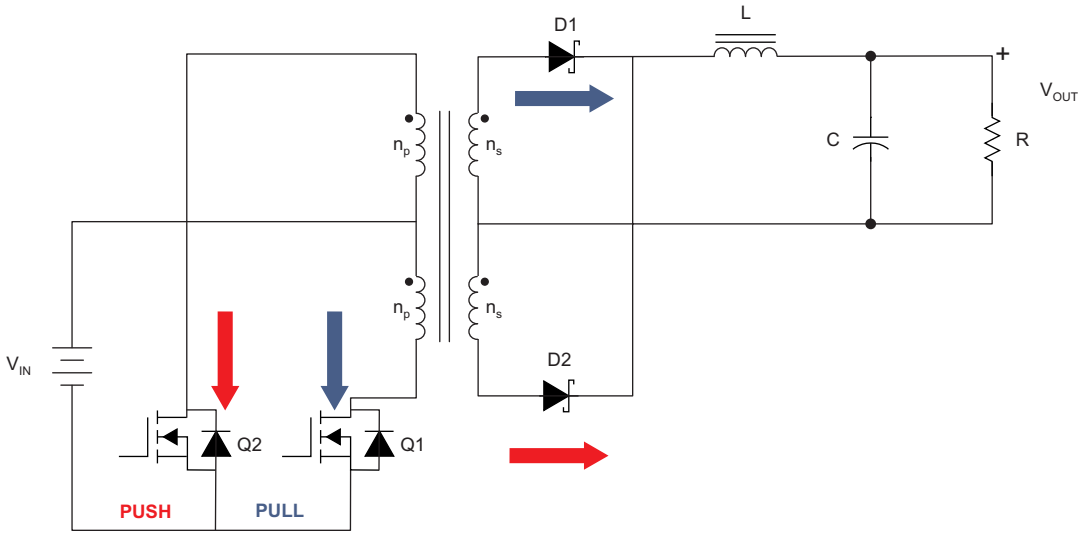

Figure 5. Push-Pull Topology

The Push-Pull topology is basically a forward converter with two primaries. The primary switches alternately power their respective windings. When Q1 is active, current flows through D1. When Q2 is active, current flows through D2. The secondary is arranged in a center tapped configuration as shown in Figure 5. The output filter sees twice the switching frequency of either Q1 or Q2. The transfer function is similar to the forward converter, where “D” is the duty cycle of a given primary switch, which accounts for the “2X” term. When neither Q1 nor Q2 are active, the output inductor current splits between the two output diodes.

A transformer reset winding shown on the forward topology is not necessary, the topology is self resetting.

$$V_{out} = V_{in} \times D \times \frac{Ns}{Np} \times 2 \quad (1)$$

3.1 Half Bridge Converter

The Half Bridge converter is similar to the Push-Pull converter, but a center tapped primary is not required. The reversal of the magnetic field is achieved by reversing the direction of the primary winding current flow. In this case, two capacitors, C1 and C2, are required to form the DC input mid-point. Transistors Q1 and Q2 are turned ON alternately to avoid a supply short circuit, in which case the duty cycle *d* must be less than 0.5.

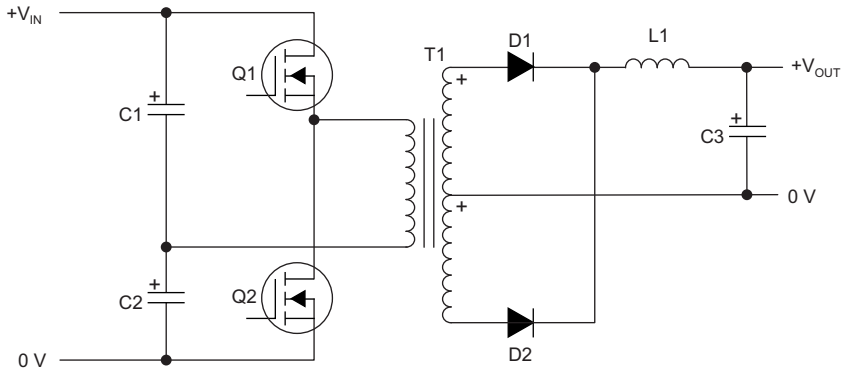

Figure 6. Half Bridge Converter

For the Half-Bridge converter, the output voltage VOUT equals:

$$V_{out} = V_{in} \frac{N_2}{N_1} \times d \quad (2)$$

Where, *d* is the duty cycle of the transistors and 0 < d < 0.5.

N2/N1 is the secondary to primary turns ratio of the transformer.

3.2 Full Bridge Converter

The transformer topology for both the Half Bridge and Full Bridge converter is the same, except that for a given DC link voltage of the Half Bridge transformer sees half the applied voltage as compared with that of the Full Bridge transformer. The current flows in opposite directions during alternate half cycles. So flux in the core swings from negative to positive, utilizing even the negative portion of the hysteresis loop, thereby, reducing the chances of core saturation. Therefore, the core can be operated at greater Bm value here. The largest power is transferred when the duty cycle is less than 50%. Diagonal pairs of transistors (Q1-Q4 or Q2-Q3) conduct alternately, thus, achieving current reversal in the transformer primary.

Output voltage equals:

$$V_{out} = 2 \times V_{in} \frac{N_2}{N_1} \times d \quad (3)$$

Where, *d* is the duty cycle of the transistors and 0 < d < 0.5.

N2/N1 is the secondary to primary turns ratio of the transformer.

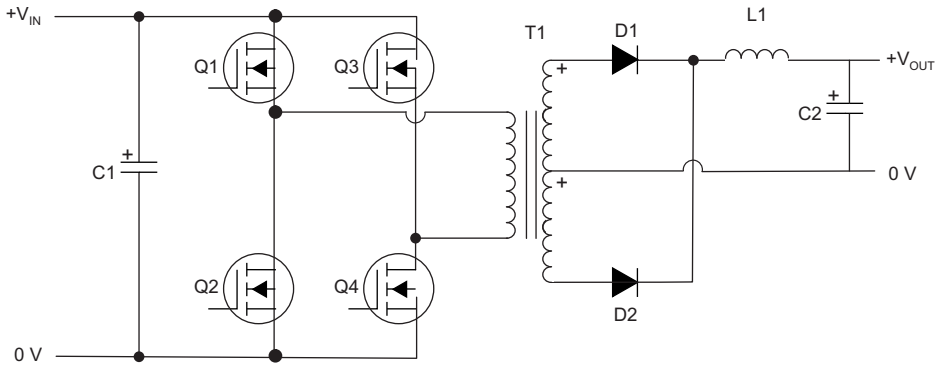

Figure 7. Full Bridge Converter

The choice of the DC-DC isolation stage for the High-Frequency Inverter among the three topologies discussed above depends on the VA requirement. For applications targeting 1KVA and above, the Full Bridge converter is the ideal choice pertaining to the points below:

- For a given input voltage, the voltage stress on the transistors is double in case of the push-pull topology than Half Bridge and Full Bridge configuration.
- The center tapped primary in the case of the push-pull converter limits the operation for a higher VA rating for the same core size when compared to the Half Bridge and Full Bridge converter.
- To prevent flux walking in the DC-DC stage, the current in both the halves need to be sensed and the duty cycle needs to be corrected accordingly.

3.2.1 Flux Walking

Faraday's Law states that the flux through a winding is equal to the integral volt-seconds per turn. This requires that the voltage across any winding of any magnetic device must average zero over a period of time. The smallest DC voltage component in an applied AC waveform will slowly but inevitably "walk" the flux into saturation.

In a low frequency mains transformer, the resistance of the primary winding is usually sufficient to control this problem. As a small DC voltage component pushes the flux slowly toward saturation, the magnetizing current becomes asymmetrical. The increasing DC component of the magnetizing current causes an IR drop in the winding, which eventually cancels the DC voltage component of the drive waveform, hopefully well short of saturation. In a high frequency switchmode power supply, a push-pull driver will theoretically apply equal and opposite volt-seconds to the windings during alternate switching periods, thus, "resetting" the core (bringing the flux and the magnetizing current back to its starting point). But there are usually small volt second asymmetries in the driving waveform due to inequalities in MOSFET RDS_{on} or switching speeds. The resulting small DC component causes the flux to "walk". The high frequency transformer, with relatively few primary turns, has extremely low DC resistance, and the IR drop from the DC magnetizing current component is usually not sufficient to cancel the volt-second asymmetry until the core reaches saturation.

The flux walking problem is a serious concern with any Push-Pull topology (bridge, half-bridge or push-pull CT), when using voltage mode control. One solution is to put a small gap in series with the core. This raises the magnetizing current so that the IR drop in the circuit resistances is able to offset the DC asymmetry in the drive waveform. But the increased magnetizing current represents increased energy in the mutual inductance, which usually ends up in a snubber or clamp, increasing circuit losses. A more elegant solution to the asymmetry problem is an automatic benefit of using the current mode control (peak or average CMC). As the DC flux starts to walk in one direction, due to the volt-second drive asymmetry, the peak magnetizing current becomes progressively asymmetrical in alternate switching periods. However, current mode control senses the current and turns off the switches at the same peak current level in each switching period, so that ON times are alternately lengthened and shortened. The initial volt-second asymmetry is thereby corrected, peak magnetizing currents are approximately equal in both directions, and flux walking is minimized.

However, with the Half Bridge topology this creates a new problem. When current mode control corrects the volt-second inequality by shortening and lengthening alternate pulse widths, an ampere-second (charge) inequality is created in alternate switching periods. This is of no consequence in full bridge or push-pull center-tap circuits, but in the half-bridge, the charge inequality causes the capacitor divider voltage to walk towards the positive or negative rail. As the capacitor divider voltage moves away from the mid-point, the volt-second unbalance is made worse, resulting in further pulse width correction by the current mode control. A runaway situation exists, and the voltage will walk (or run) to one of the rails.

Considering the above points, the Full Bridge converter seems to be the ideal choice for the High-Frequency Inverter rated above 1kVA.

4 DC-AC Converter

The DC-AC Converter section of the High-Frequency Inverter is an H-Bridge, which converts the high voltage DC bus (380 V) into sinusoidal AC waveform.

The sinusoidal PWM generation is done using the PWM interrupt handler in TMS320F28069 by entering into an infinite loop. A look-up table is formed that samples the instantaneous values at specific time intervals based on the operating frequency of the DC-AC section. The DC-AC section is operated at 20 kHz, based on that the total number of samples for half cycle is 200. The instantaneous value is then multiplied by the maximum duty cycle count to get the duty cycle count at the corresponding sample instant. This generates the sinusoidal PWM for the full bridge section. The DC-AC section consists of high-side and low-side drivers to drive the Mosfets in the H-Bridge configuration followed by an output L-C- L filter resulting in sinusoidal sine wave.

5 DC-DC Converter Section (Voltage Fed Full Bridge)

The DC-DC section consists of 120 V boot, 4A peak high frequency high-side and low-side driver UCC27211 for driving the high-side and low-side FET's of the Full Bridge converter.

In UCC27211, the high side and low side each have independent inputs, which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the chip. The UCC27210 is the pseudo-CMOS compatible input version and the UCC27211 is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS}, which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

Figure 8 shows the independent control of the high-side and low-side drivers and the internal bootstrap diode capable of withstanding the reverse voltage up to 120 V.

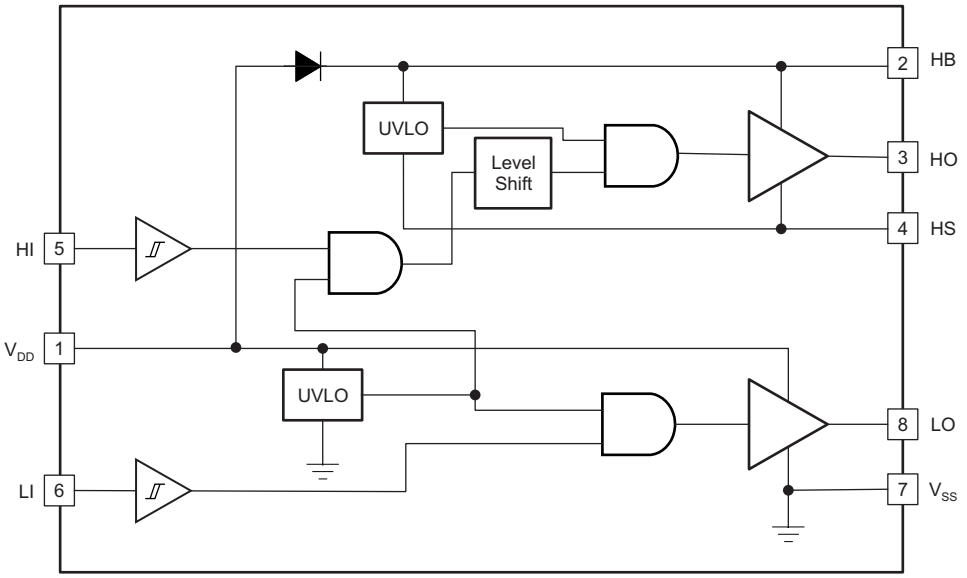

Figure 8. Functional Block Diagram of UCC27211

The V_{DD} supply of the IC is derived from the 12 V battery itself (HF inverter source). The DC-DC stage converts the 12 V input voltage to a regulated 380 V DC bus, which is the input to the DC-AC section. To avoid battery inrush current at the start of the PWM, soft start is implemented that controls the rate of di/dt. The PWM's initially start with a very low duty and finally duty cycle is adjusted as per the regulation point of the DC bus voltage (380 V). The operating frequency for the switches in the DC-DC section is 40 kHz, the output filter sees twice the frequency of the switches M6 or M9 (see Figure 14).

5.1 Voltage Fed Full Bridge Converter Transformer Calculation

- Total Output Power Po = (Vo + Vrl + Vd) Io

Where, Vo = Output voltage
Vrl = Voltage drop due to winding resistance
Vd= Forward voltage drop of the output diode
Io= Output current

- The Area Product for this configuration is given as:

$$Ap = \frac{Po\left[\sqrt{2} + (1/\eta)\right]}{4.Kw.J.Bm.Fsw}$$

Where, η = Efficiency of the Full Bridge converter
Kw = Window factor
J = Current Density (A/m^2)
Bm = Magnetic flux density
Fsw = Switching frequency

- Primary Number of Turns

$$Np = \frac{Vin\,(\text{maximum})}{4.Ac.Bm.Fsw}$$

Where, Ac= Core area

Vin (maximum) = Maximum input voltage applied to the Full Bridge converter

- Turns Ratio

$$n = \frac{(Vo + Vrl + Vd)}{2.D\text{max}.Vin\text{min}}$$

Where, Vin min = Minimum input voltage applied to the Full Bridge converter

Secondary turns Ns = n x Np

- RMS Values of Currents

Isec = Io√Dmax

Ipri = n x Io

Where, Isec = Secondary current

Ipri = Primary current

Using the above calculations, the number of turns can be calculated for the required output power and the rms values of the primary and secondary currents can also be found out for a given core area.

The calculation was done considering 1kVA requirement with battery input as the input voltage (12 V) in EF32 core and the corresponding numbers of turns were calculated for both primary and secondary.

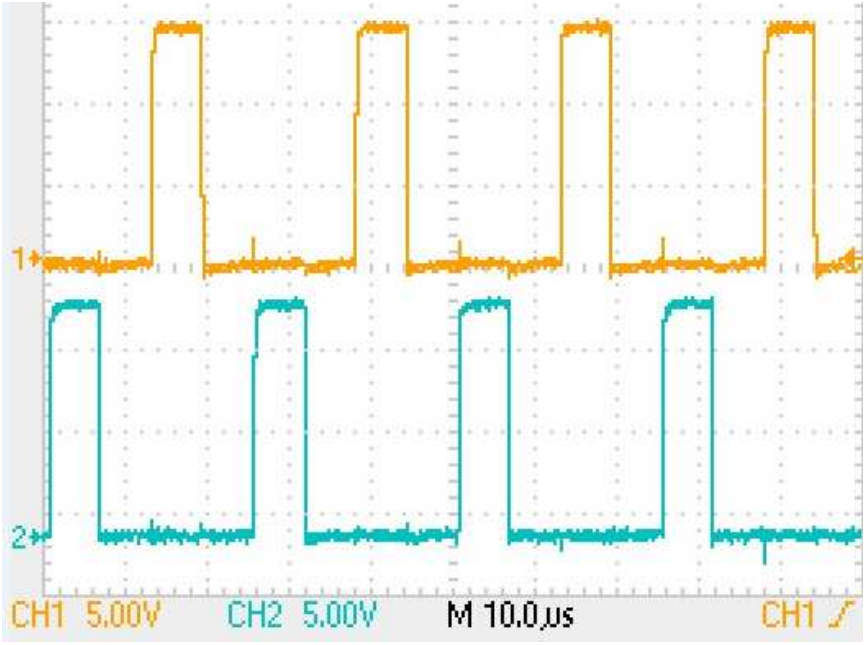

Figure 9. Gate Drive Waveforms for the Full Bridge DC-DC Converter

In order to minimize flux walking, as discussed Section 3.2.1, the peak current in each of the conducting halves can be sensed using the fully differential isolation amplifier AMC1100.

The AMC1100 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide galvanic isolation of up to 4250 V peak, according to UL1577 and IEC60747-5-2. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

After sensing the peak current, the duty cycle is corrected for each of the corresponding halves and volt second asymmetry is thereby corrected, to minimize flux walking.

6 Control Section

The control section consists of TMS320F28069 performing the control operation generating PWM's for both DC-DC section and SPWM's for the DC-AC section using the PWM interrupt handler.

- MCU PWM Outputs
- DC-DC section
  - PWM1DH_MCU = High-Side Input Gate Drive 1
  - PWM1DL_MCU = Low-Side Input Gate Drive 1
  - PWM2DH_MCU = High-Side Input Gate Drive 2
  - PWM2DL_MCU = Low-Side Input Gate Drive 2
- DC-AC section:
  - PWM1AH_MCU = High-Side Input Gate Drive 1 for UCC27712
  - PWM1AL_MCU = Low-Side Input Gate Drive 1 for UCC27712
  - PWM2AH_MCU = High-Side Input Gate Drive 2 for UCC27712
  - PWM2AL_MCU = Low-Side Input Gate Drive 2 for UCC27712
- The Opto couplers HCPL-0211 provides isolated gate drives for the DC-DC section:
  - PWM1DH = High-Side Input Gate Drive for UCC27211 (Driver 1)
  - PWM1DL = Low-Side Input Gate Drive for UCC27211 (Driver 1)
  - PWM2DH = High-Side Input Gate Drive for UCC27211 (Driver 2)
  - PWM2DL = Low-Side Input Gate Drive for UCC27211 (Driver 2)

7 DC-AC Converter Section

The DC-AC converter section consists of high- and low-side driver UCC27712, which is a high-voltage, high-speed power Mosfet and IGBT driver with independent low side and high side referenced output channels. It has a floating channel designed for bootstrap operation and fully operational to +600 V. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration, which operates up to 600 V.

Figure 10 shows the functional block diagram of the driver. The bootstrap diode is placed external to the driver and the device can handle peak currents up to 4A.

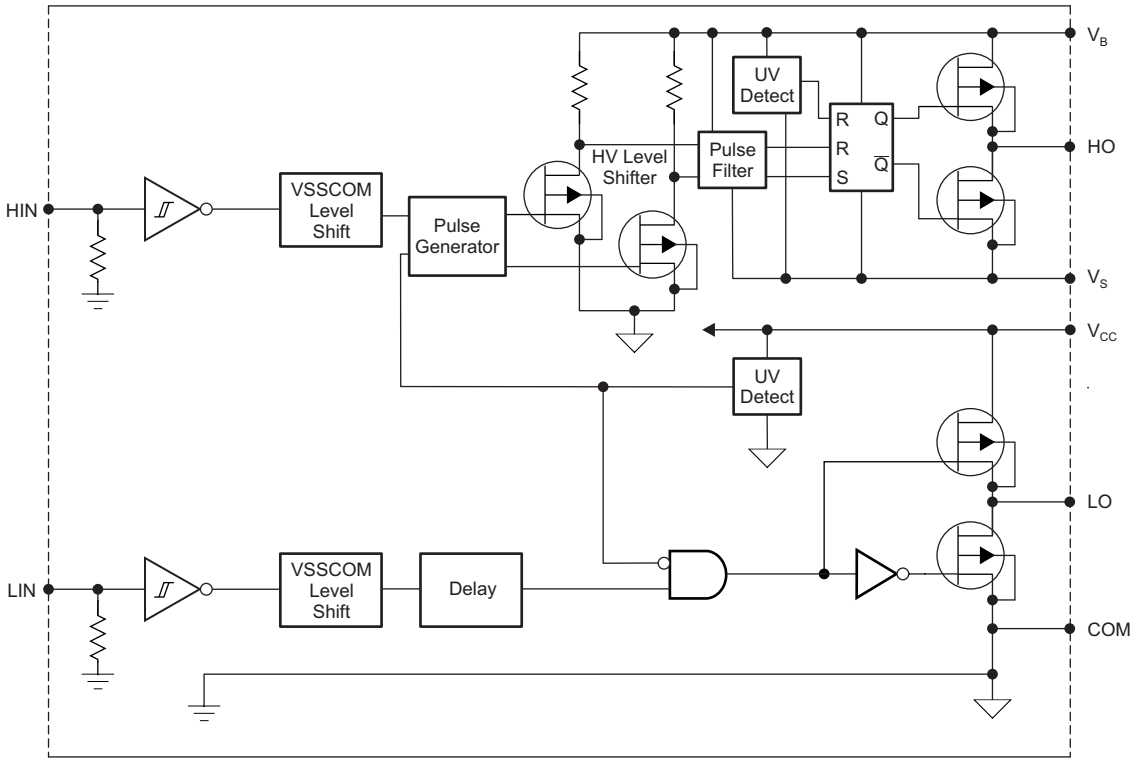

Figure 10. Functional Block Diagram

The AC voltage feedback to the MCU for closed-loop control is given by scaling down the voltage by a resistor divider network and rectifying it by means of a precision rectifier circuit. The precision rectifier circuit is built with the high-speed precision difference amplifier INA143 followed by TL082 powered from a dual supply (±12 V). The rectified and scaled down Sine wave is fed to the MCU for closed-loop control of the output voltage.

The load current sense is done using ACS709, which is a precision linear Hall sensor integrated circuit with copper conduction path. Applied current flows through the copper conduction path, and the analog output voltage from the Hall sensor IC linearly tracks the magnetic field generated by the applied current. The voltage on the overcurrent input (VOC pin) allows to define an overcurrent fault threshold for the device. When the current flowing through the copper conduction path (between the IP+ and IP– pins) exceeds this threshold, the open drain overcurrent fault pin transitions to a logic-low state and can be used to shut down the PWM pulses of the DC-AC section and DC-DC section as well to provide protection against overload and short circuit of the load.

8 Firmware Flowchart

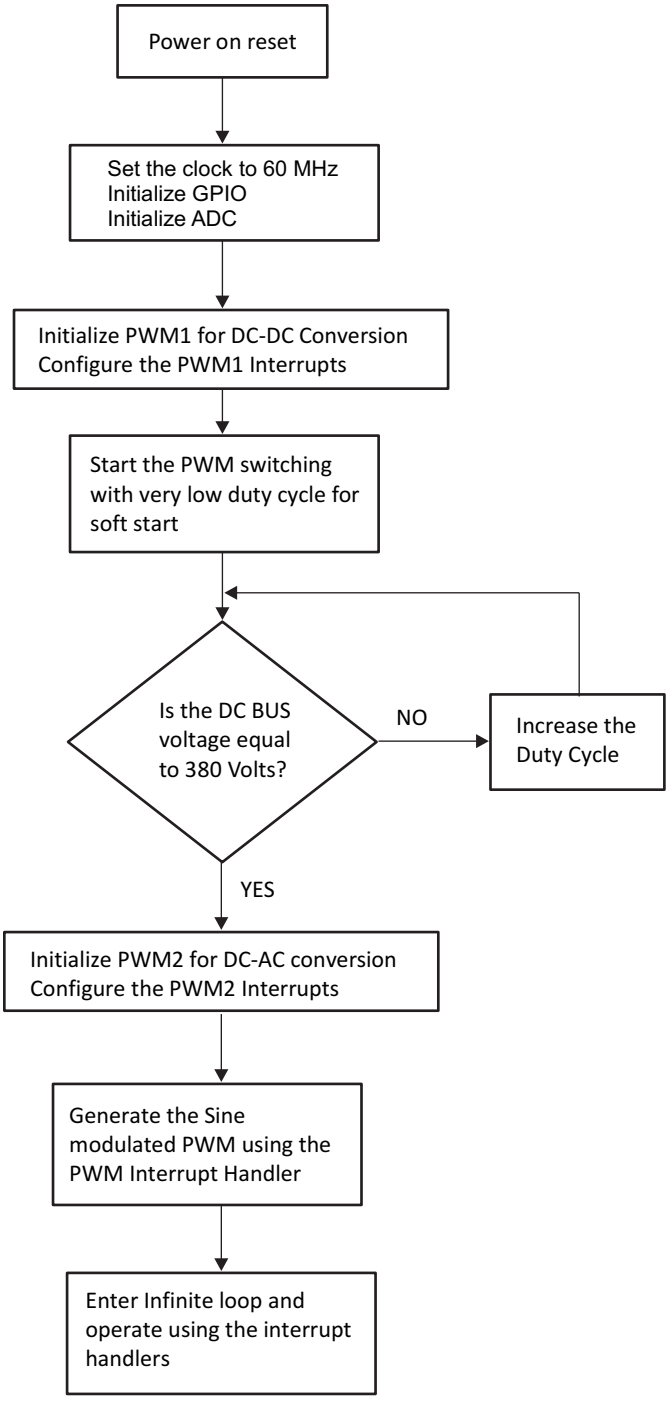

Figure 11. Firmware Flowchart

9 Waveforms

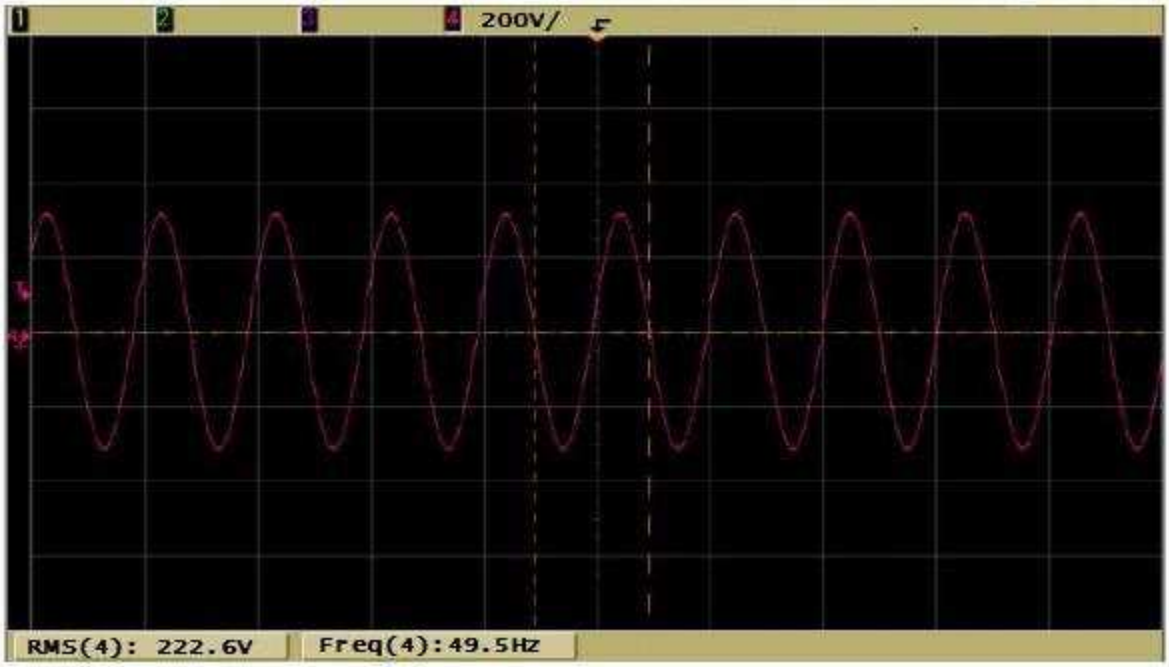

Figure 12. Output Voltage at No Load

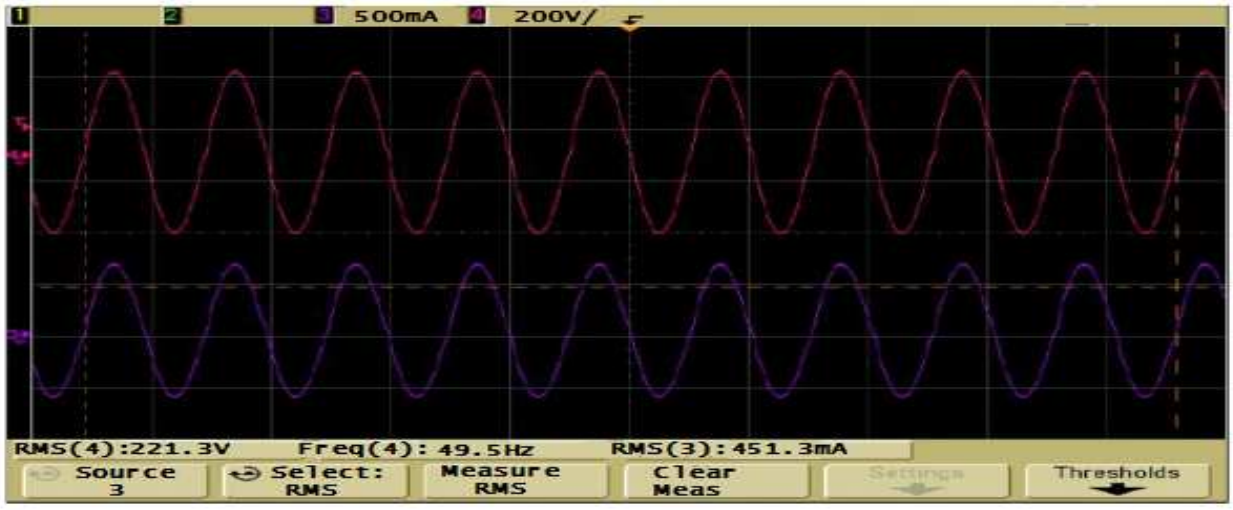

Figure 13. Output Voltage and Current (100W Load)

10 Conclusion

This application report documents the concept reference design for the DC-DC Stage and the DC-AC Converter section that can be used in the High-Frequency Inverter using TMS320F28069, which handles the PWM generation and closed loop control of both the stages.

The reference design was tested for 100W load and can be further tested at higher VA ratings modifying the power components of the DC-AC Converter Section. The reference design is targeted for High-Frequency Inverters rated for higher VA used in the industrial segment.

11 References

1. *Analysis of a Voltage-fed Full Bridge DC-DC Converter in Fuel Cell Systems* by A. Averberg, A. Mertens, Power Electronics Specialists Conference, 2007. PESC 2007. IEEE.
2. *A Current Mode Control Technique with Instantaneous Inductor Current Feedback for UPS Inverter* by H.Wu, D.Lin, D. Zhang, K. Yao, J.Zhang, IEEE transaction, 1999.
3. *Power Electronics Converter, Applications and Design* by Mohan, T.M. Undeland, and W.P. Robbins.
4. *TMS320F28069, TMS320F28068, TMS320F28067, TMS320F28066, TMS320F28065, TMS320F28064, TMS320F28063, TMS320F28062 Piccolo Microcontrollers Data Manual* (SPRS698)

Application Schematic

A.1 Application Schematic

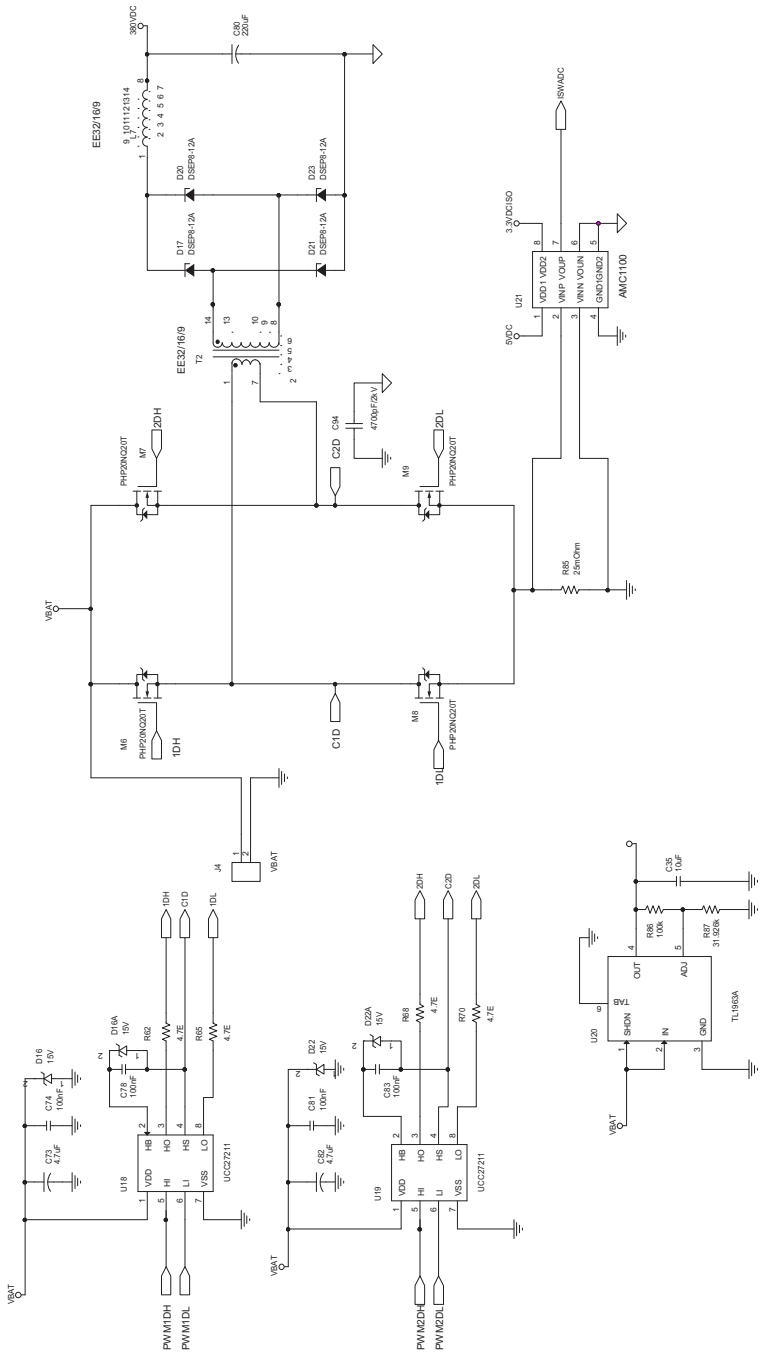

Figure 14. DC-DC Converter Schematic (Voltage Fed Isolated Full-Bridge)

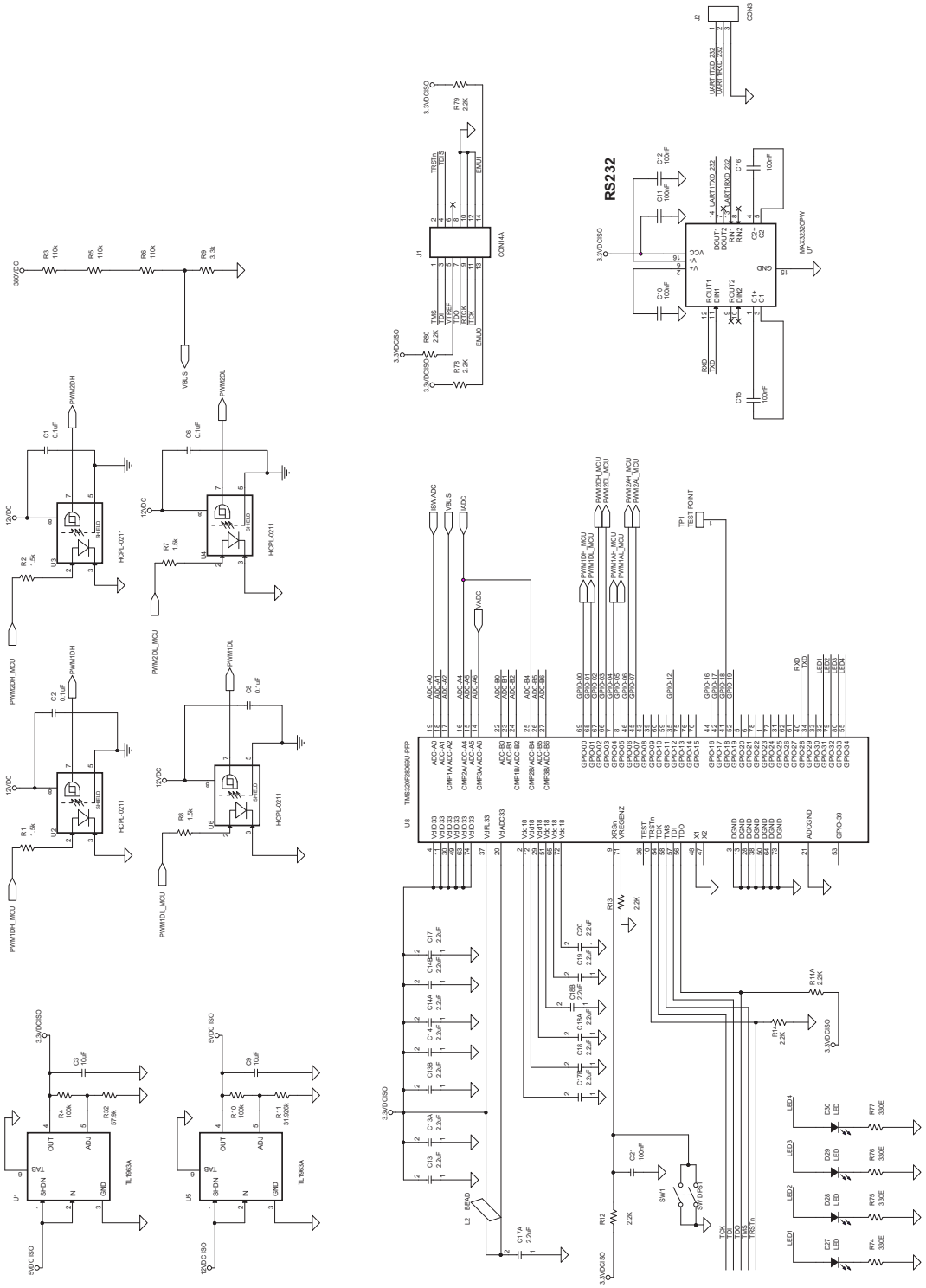

Figure 15. Control Section Schematic

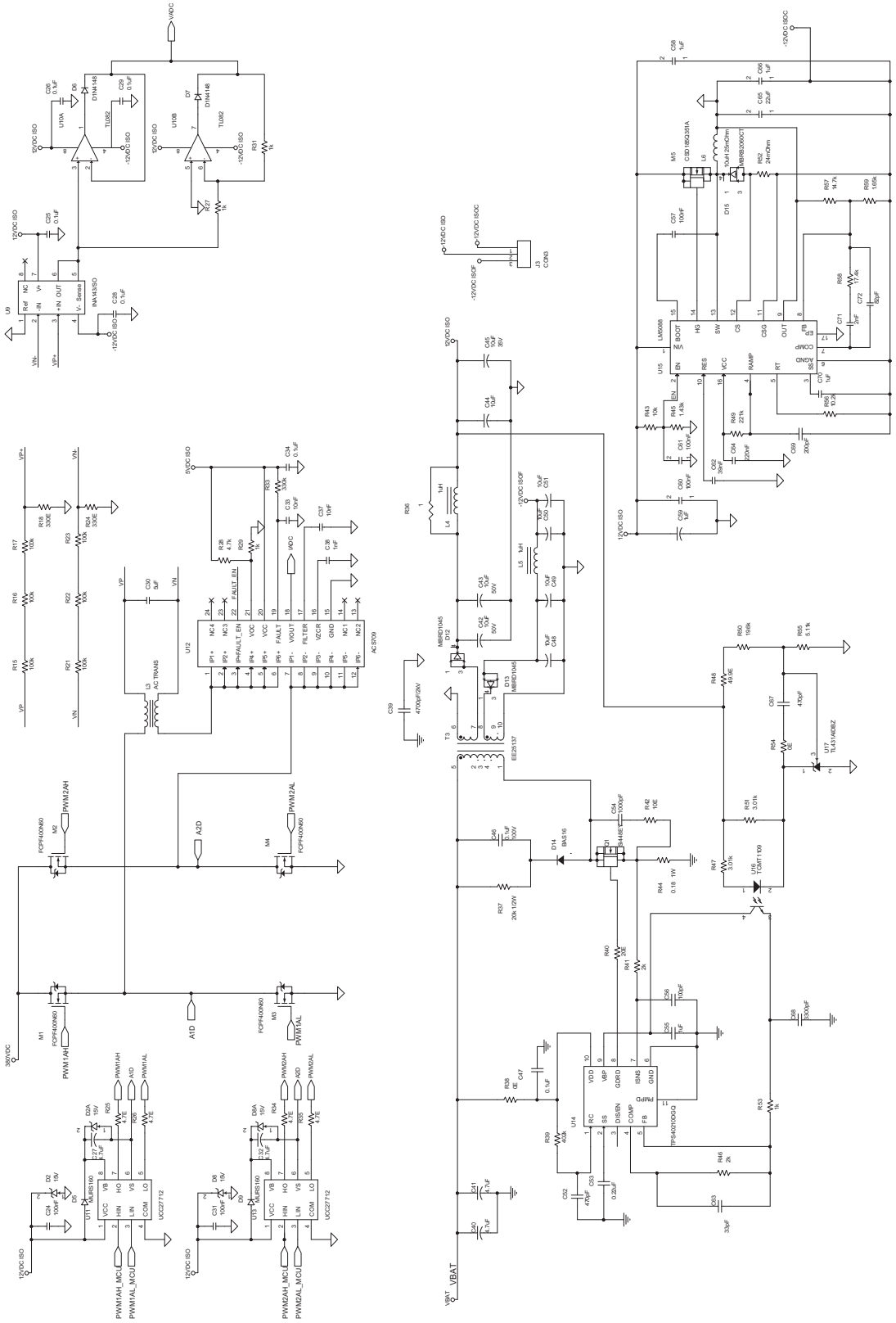

Figure 16. DC-AC Converter Schematic

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (June 2015) to C Revision	Page
• Updates were made in Section 6.	10
• Updates were made in Section 7.	10
• Update was made in Appendix A.	15

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