

Preliminary – subject to change

MPC8569E-MDS-PB

MODULAR DEVELOPMENT SYSTEM

MPC8569E Processor Board

LEGEND:

1. Do Not Place component
2. Component assembled for 8569E device Rev1 only
3. Signals/Components used for Core Issue solution only

Updates:

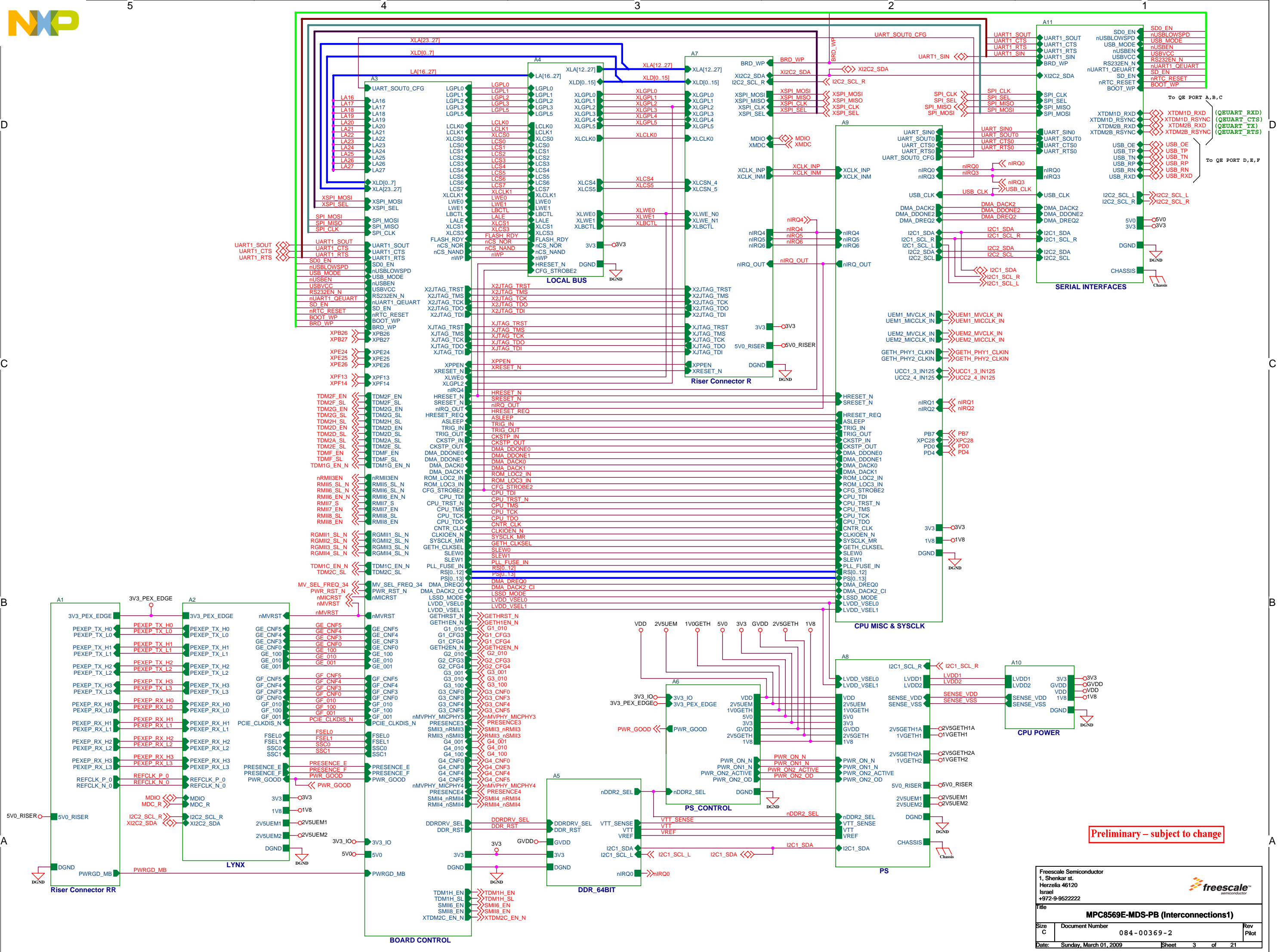
1. Connect U84/A2 to RN1/3
2. Replace R259 for 15K (P/N:006-00697)
3. Replace R263, R276 for 1000Hm (P/N:006-00626)
4. Replace R4 for 1000Hm
5. Add zener: D14 P/N:048-18MA5913BT3 in series with R4
6. Add Q8 and R587 to control USB VCC
7. Replace U38, U53, U120, U121 for NL17S2126XV5T2G (P/N: 051-NL17S2126XV)
8. Change polarity of the signal nUSBVCC for USBVCC
9. Change C212, C226 for 470uF/6.3V (Agile P/N:150-75143)
10. Shift MP1, MP2 for any other free space
11. Add R688 = 10K between U107/2 - U107/5 (PU) to I2C1_CLK out signal
12. Add R689-R691 (separate Cfg_60x & Cfg_Global_waitr)
13. Add PS13 signal to U86 (Altera BCSR)
14. Add SD0_EN signal from Altera U86 to U11 to separate SD control (disconnect U14-U11 SD_EN general control while allow SD operate with Data 0 only)
15. Add PU R691 = 10K to U45/M21 (UDE signal)
16. Add PU R692 = 10K to U45/M22 (MCP signal)
17. Disconnect XPC10 signal from U99/CS (Riser L)
18. Add R694=0R to connect PB11 and PC10
19. Reconnect XPC23 signal from U99/C22 to U99/A1
20. Add C599, C600 10uF (VTT decoupling) near each DDR slot
21. Reconnect signal PE17 from U43/4 to U62/12
22. Reconnect signal XUPC1_TXADDR3 from U43/2 to U62/14
23. Reconnect signal XENETS_RXD1 from U43/3 to U62/13
24. Add R695-697 PD to THERM0-2 pins
25. Reconnect U4/6 form GND to new R698 (PU)
26. Change connection: USB_TN to U4/12, USB_TP to U4/11
27. Add PD 5100Hm P/N:006-00629 to following pins: U99/J10, U99/J11, U99/J15, U99/J21, U99/H27, U99/H29, U99/J24, U99/H30, U99/J16, U99/J22
28. Change R486 for 100R
29. Change R459 for 200R
30. Add optional PD R709 to TRIG_OUT signal
31. Connect TP64 to U86/A5 (LSSD_MODE) Core Issue
32. Add R710 1K PD (UART_RTS0) Core Issue
33. Connect TP66 to U86/A14 (DMA_DREQ0) Core Issue
34. Add R711 1K PU to U55/3 Core Issue
35. Add R712 1K PD to R103/1 (G4TXD2) Core Issue
36. Add R713 1K PD to U55/2 (G4TXD1) Core Issue
37. Connect U97/E7 to U86/F4 (nIRQ4) Core Issue
38. Connect TP45 to U86/D1 (DMA_DACK2_CI) Core Issue
39. Add R714 0R to disable IRQ4 toggle (Core Issue)
40. Add R715 1K to U55/9 (PB16 PD) Core Issue
41. Add R716 1K in serial to DMA_DACK2_CI to isolate SD card operation (Core Issue)
42. Add optional R717-R722 PU 1K (RMII6 issue)
43. Replace R449 for 0R (to provide BootWiz power)
44. Replace R103, R104, R137, R157, R158 for 0R (UCC4 TXD signals amplification)
45. Change R7, R16, R17, R23 and R24 for 0R (UCC4 RXD signals amplification)
46. Add R723, R724 = 10K (PU) on MDIO signal
47. Provide metallization on heatsink holes and slide traces on CS (Pad D should be >=6mm)
48. Add resistor R725 = 1K to split signal UART_SOUT0 and UART_SOUT0_CFG (SD card stability)
49. Add vias to following pins:
 U100 - A28, C28, D26, E3, E5, J13.
 U99 - A1, A3, A5, A7, A13, A22, A28, A30, C10, C28, C30, D8, E1, G5.
 U97 - A28, A30, C30.
50. Replace R92, R95, R96, R100, R101, R102, R115, R441, R442 and R461 for 0R (UCC3 TXD/RXD signals amplification)
51. Replace R48, 49, 52, 63-66, 70, 75-78, 81-84, 98, 99, 113, 132-134, 151, 152, 154-156, 171-174 and R402 for 0R (To improve operation with PIB mounted ETH PHY's)

Plastic Parts:

- 042-00016, NYLON METRICS SCREW 6.4mm M3 LF 3pieces
- 042-00018, HEX NUT M3 3pieces
- 042-00064, SPACER FEM/MALE THREADED 7mm LF 4pieces
- 042-00060, NYLON METRIC SPACER 8mm LF 4pieces
- 042-00073, HEXAGONAL STANDOFF 5mm LF 3pieces

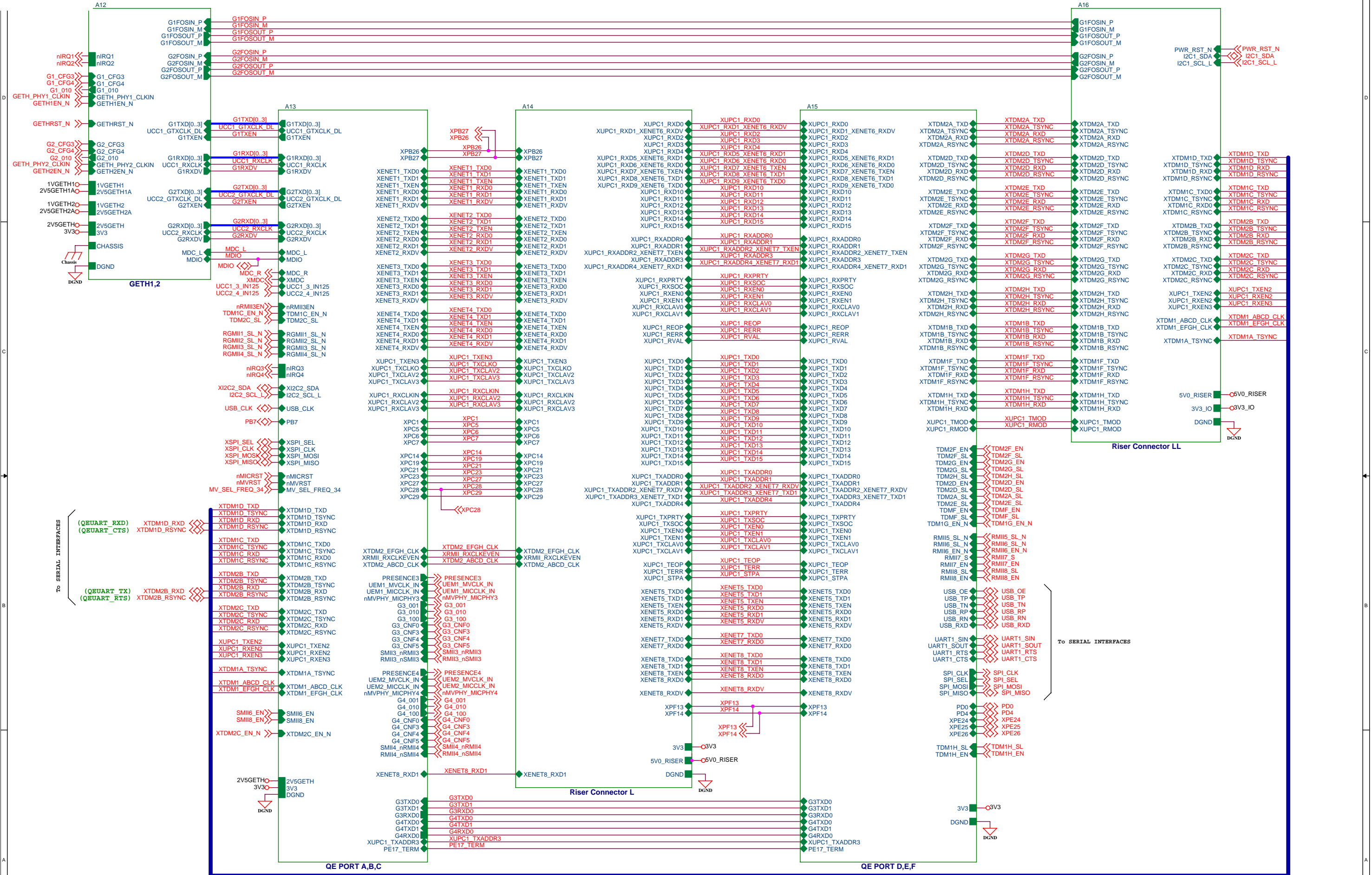
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Freescale Semiconductor 1, Shenkar st. Herzeliya 46120 Israel +972-9-9522222		
Title MPC8569E-MDS-PB (Interconnections1)		
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Freescale Semiconductor
 1, Sherkar st.
 Herzliya 46120
 Israel
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file MPC8569E-MDS-PB (Interconnections2)

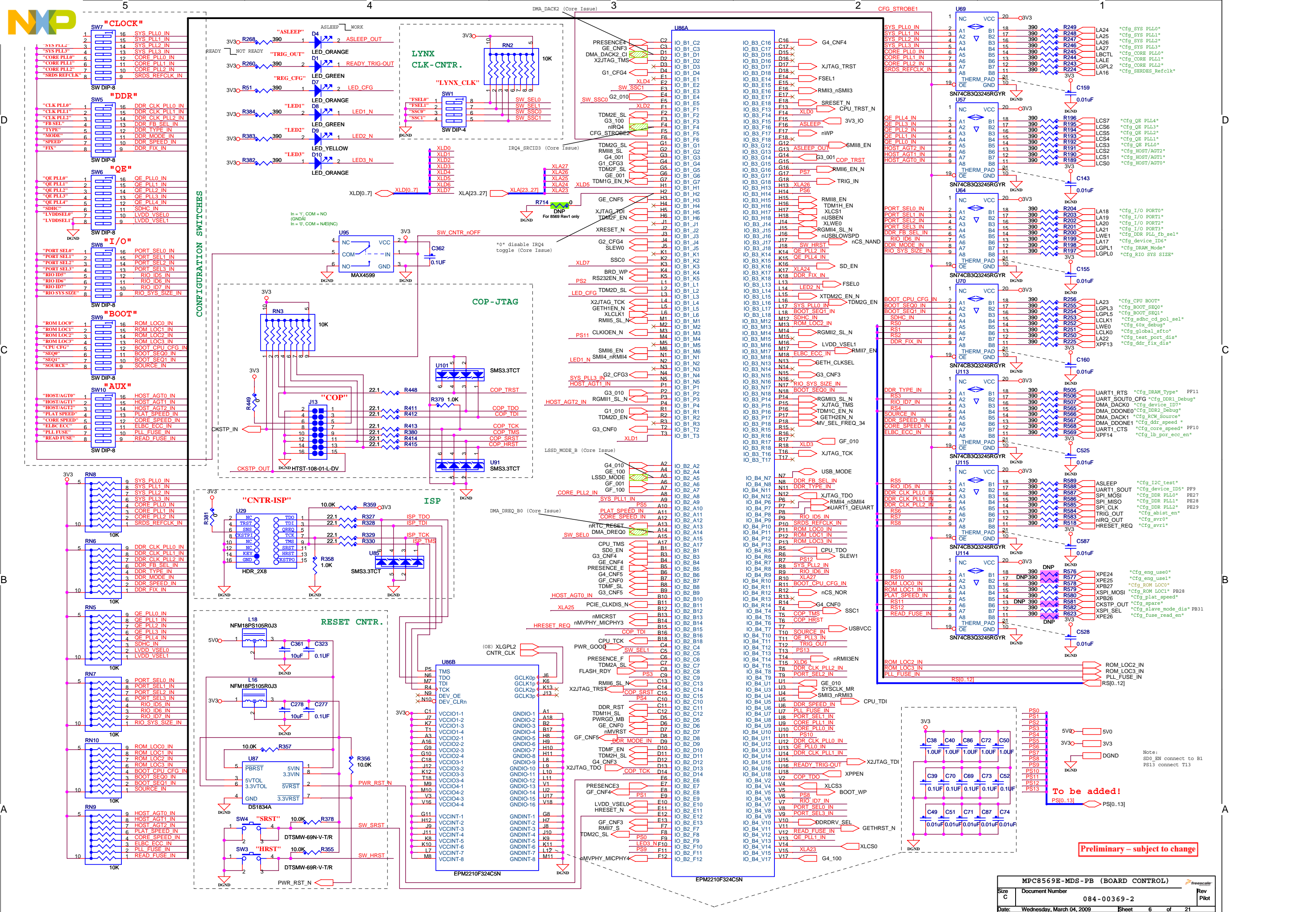
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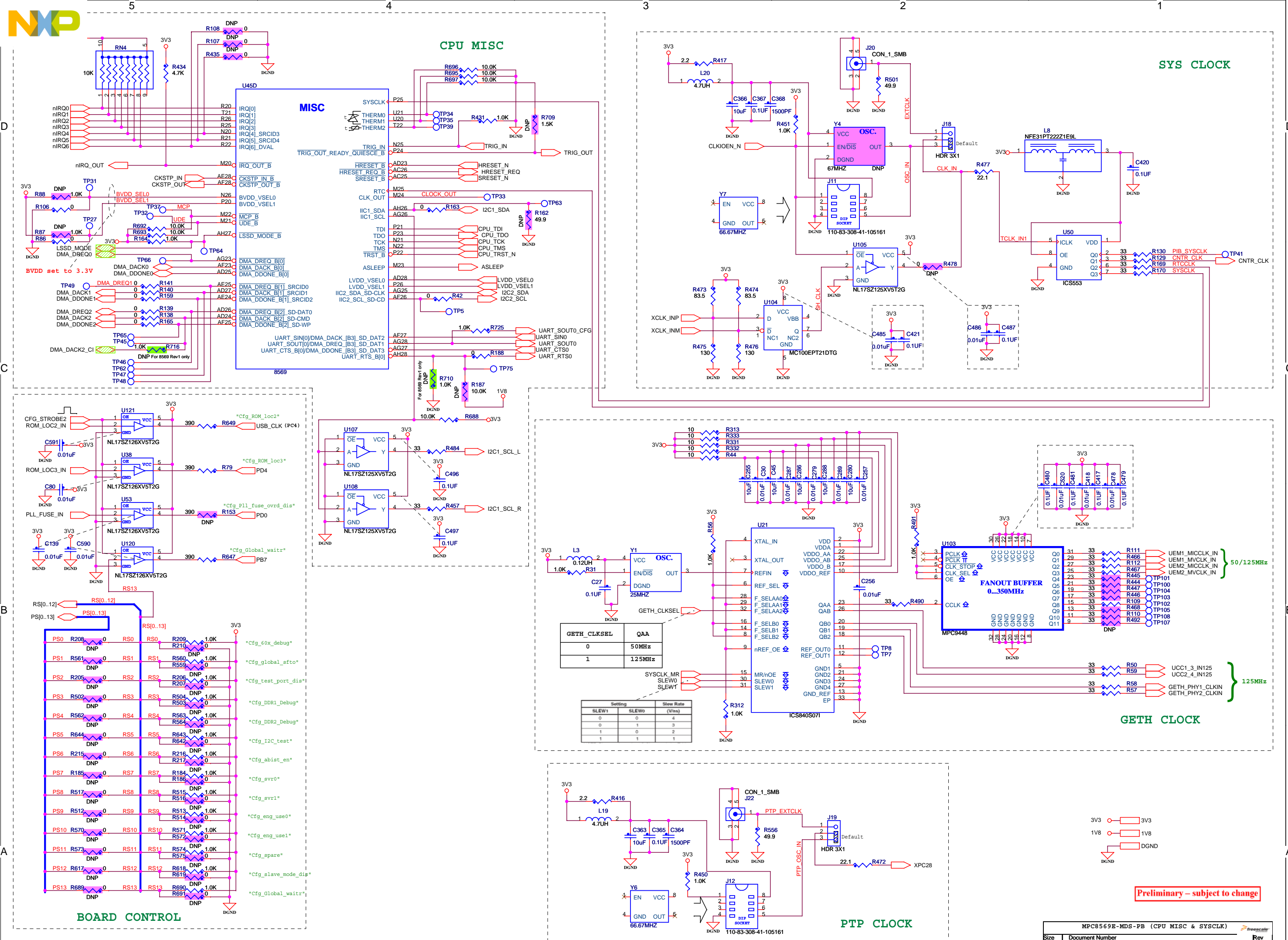
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18	RISER CONNECTOR LL
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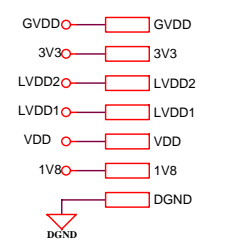
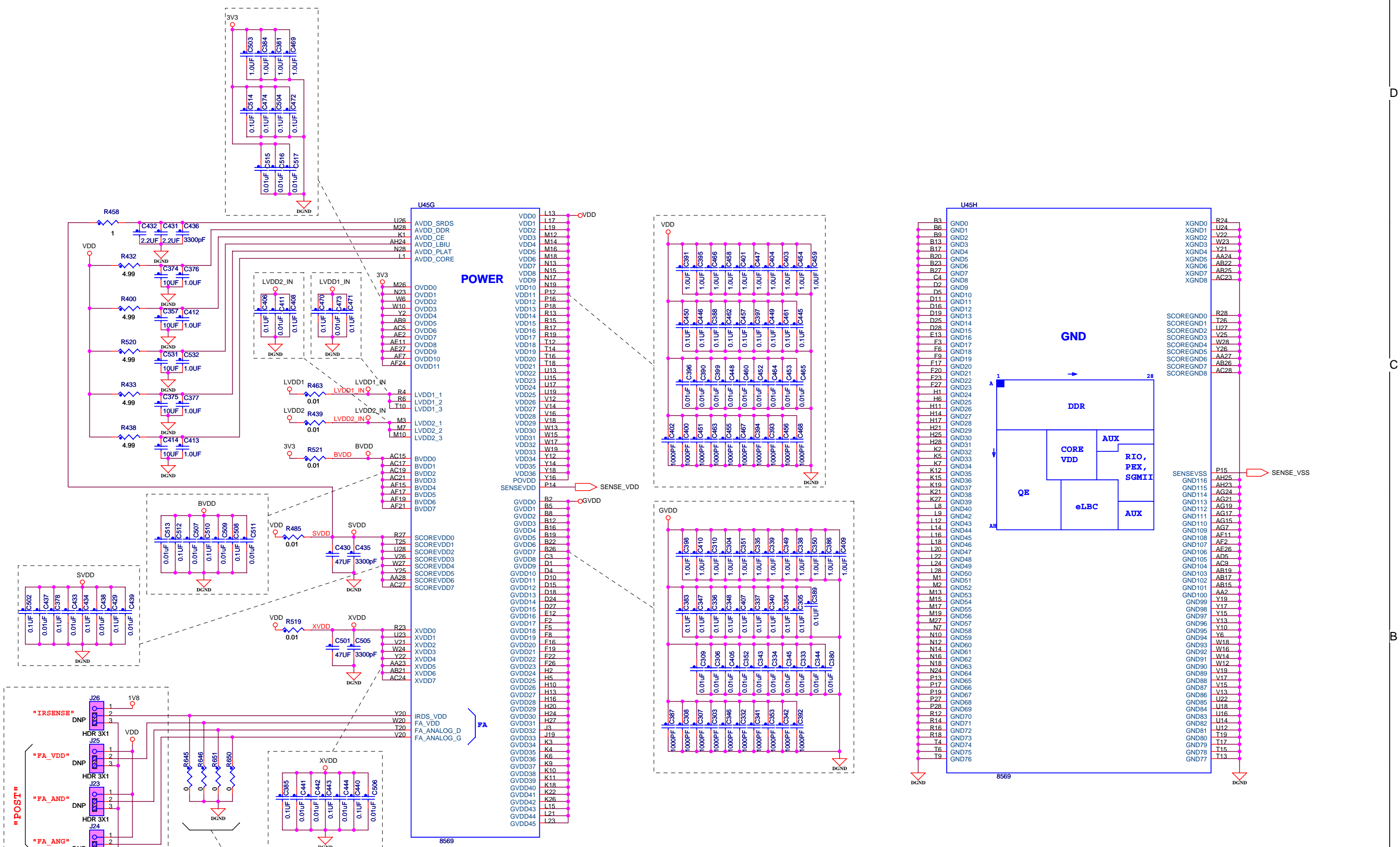
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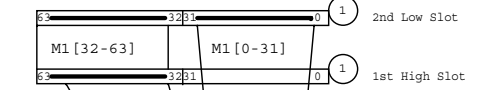
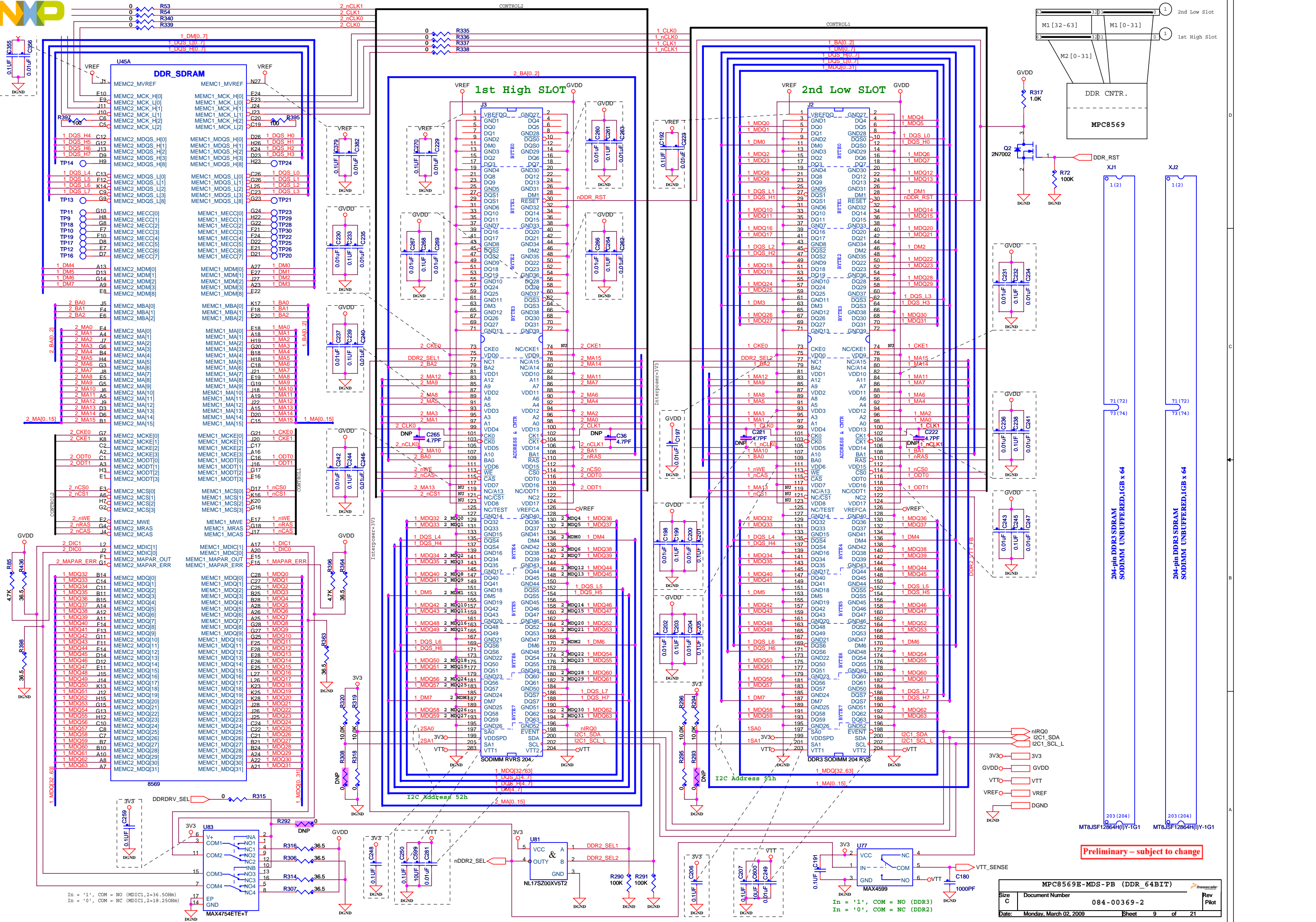


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MPC8569E-MDS-PB (CPU MISC & SYSCLK)		
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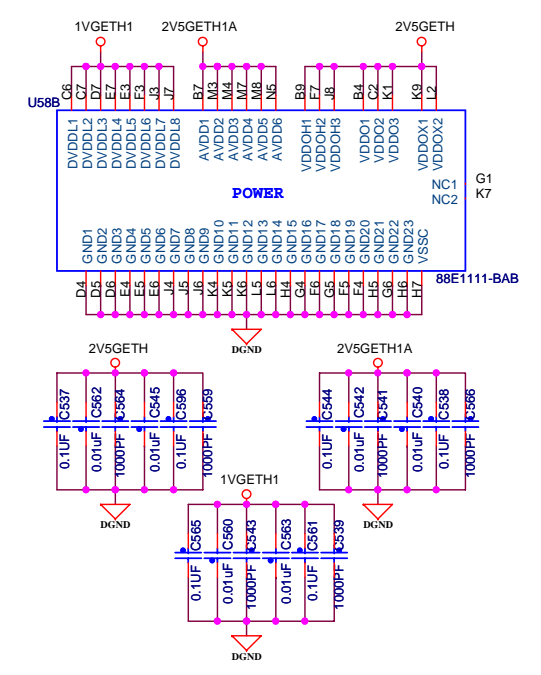
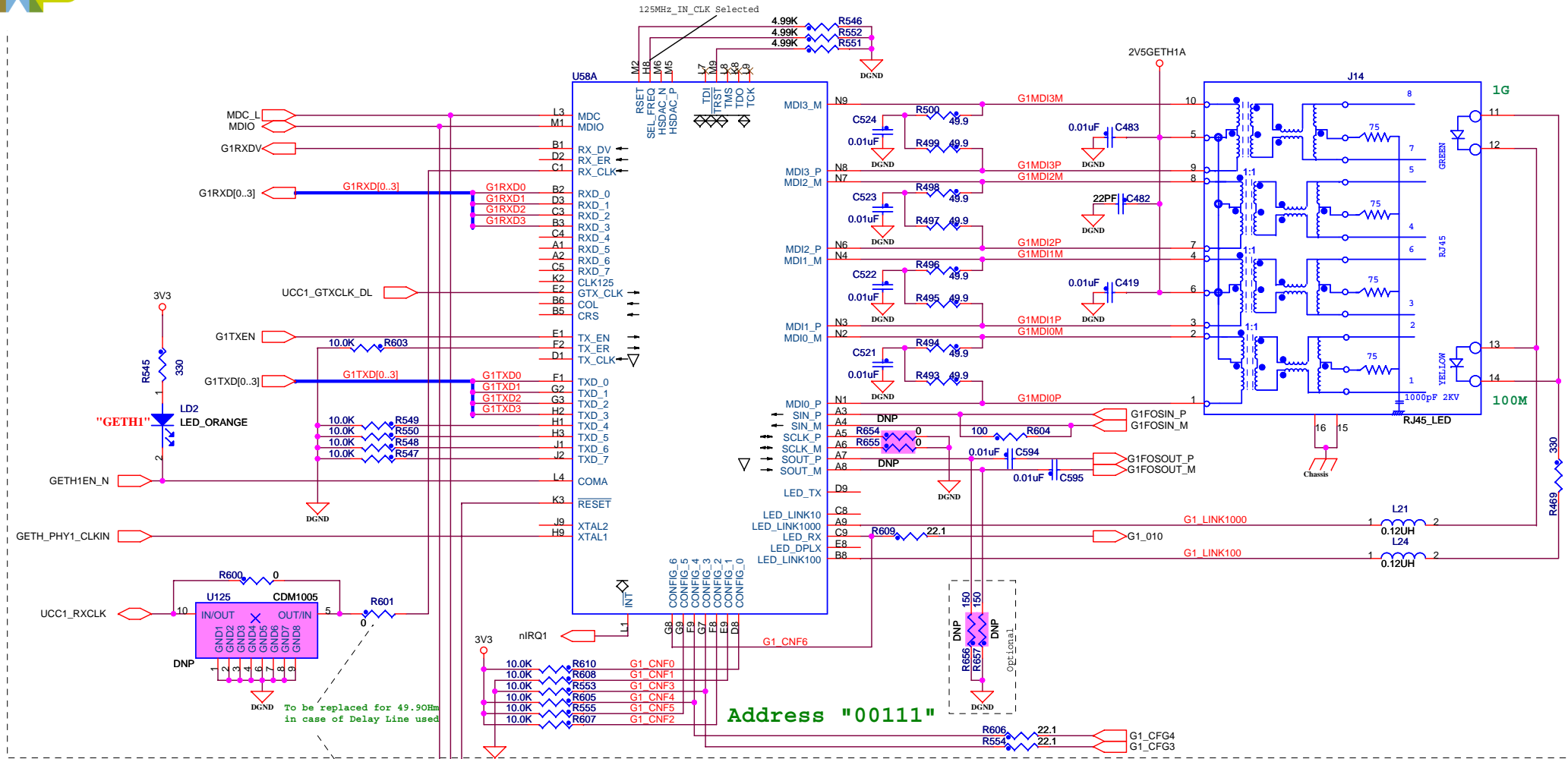
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MPC8569E-MDS-PB (DDR 64BIT)		
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In = '1', COM = NO (MDIC1,2=36.50Hz)
 In = '0', COM = NC (MDIC1,2=18.250Hz)

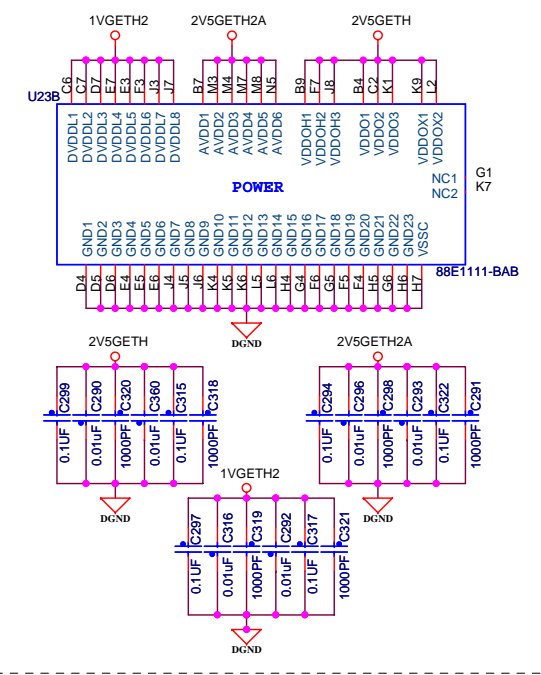
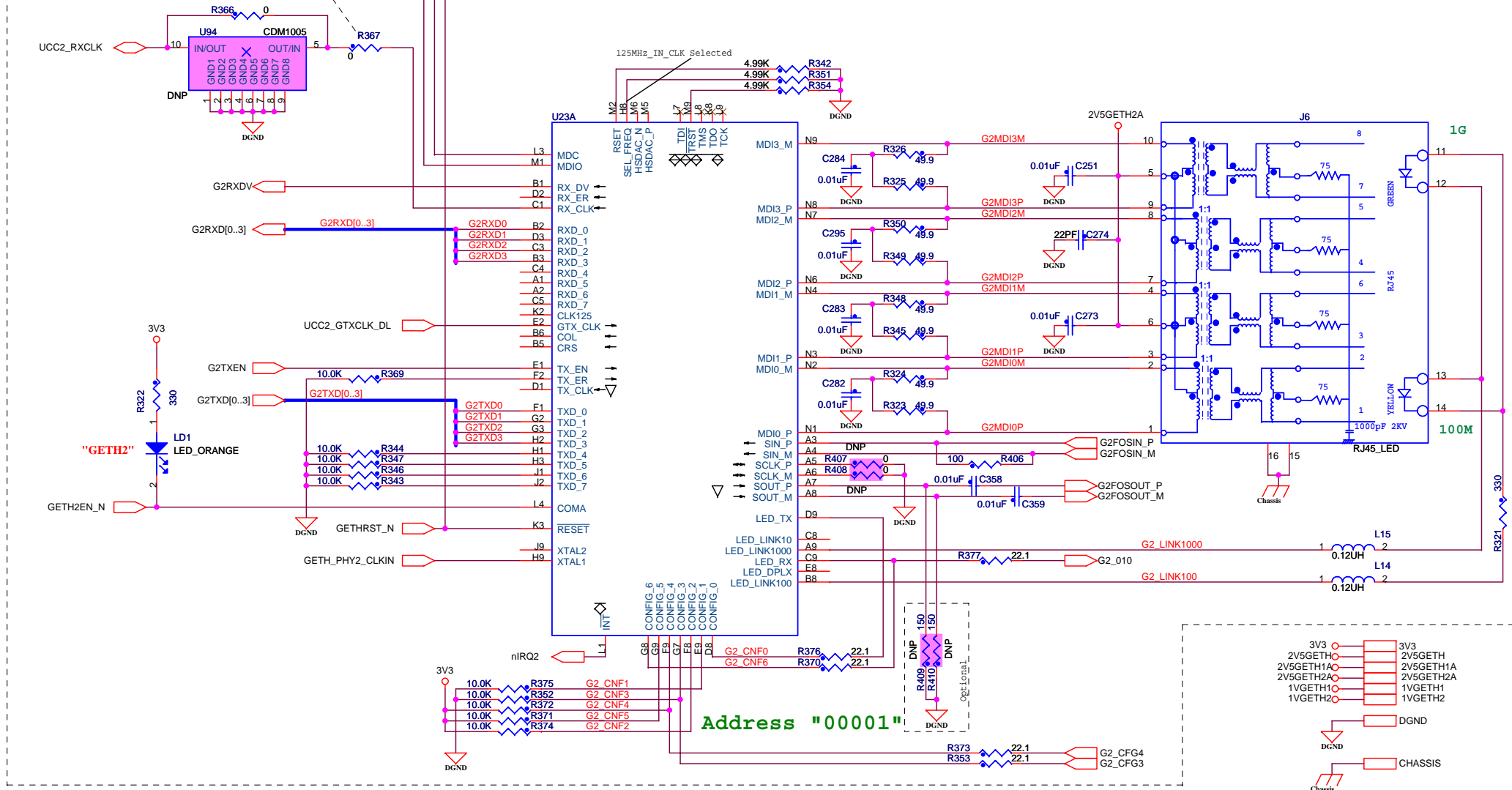
In = '1', COM = NO (DDR3)
 In = '0', COM = NC (DDR2)

GETH1



Address "00111"

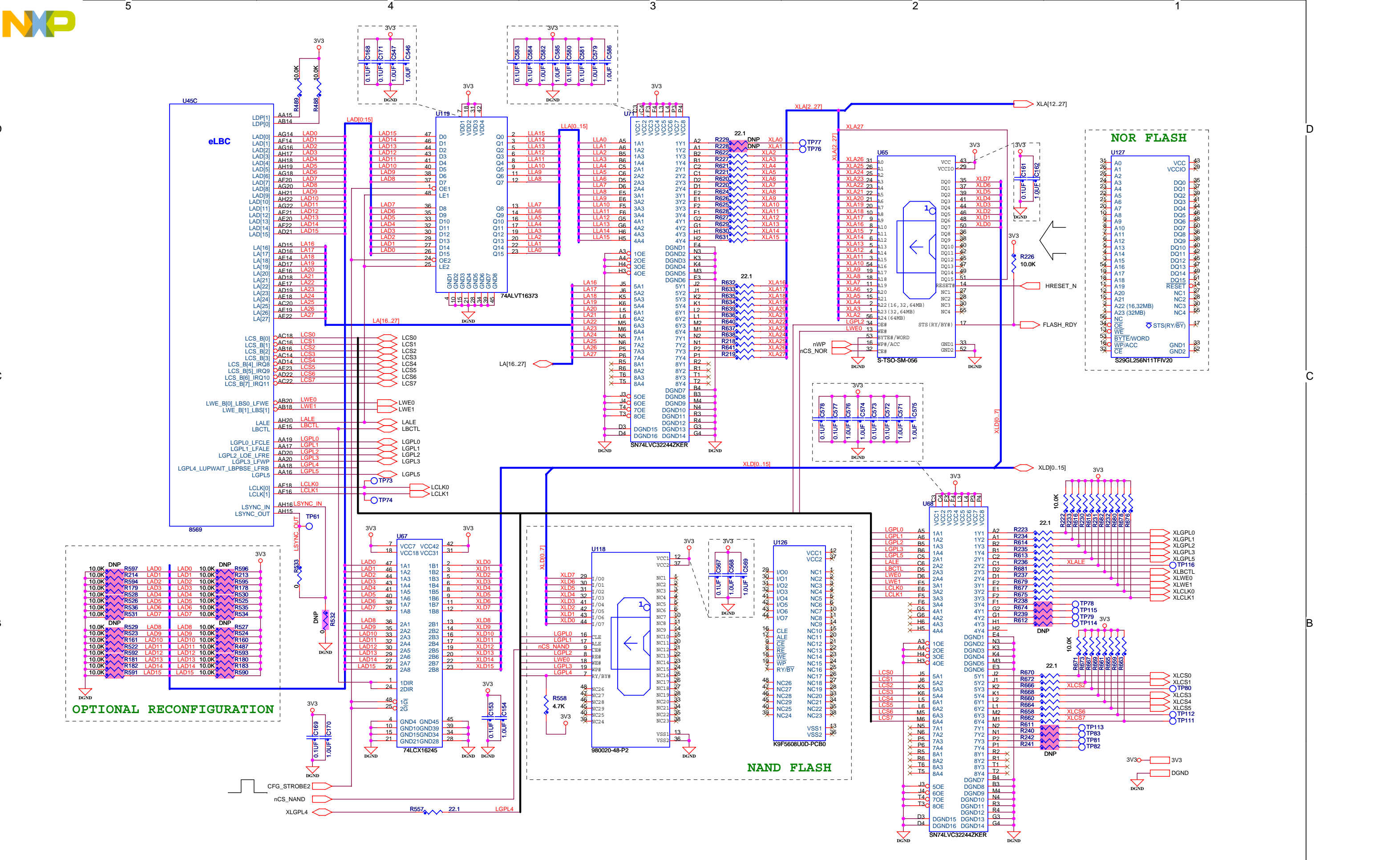
GETH2



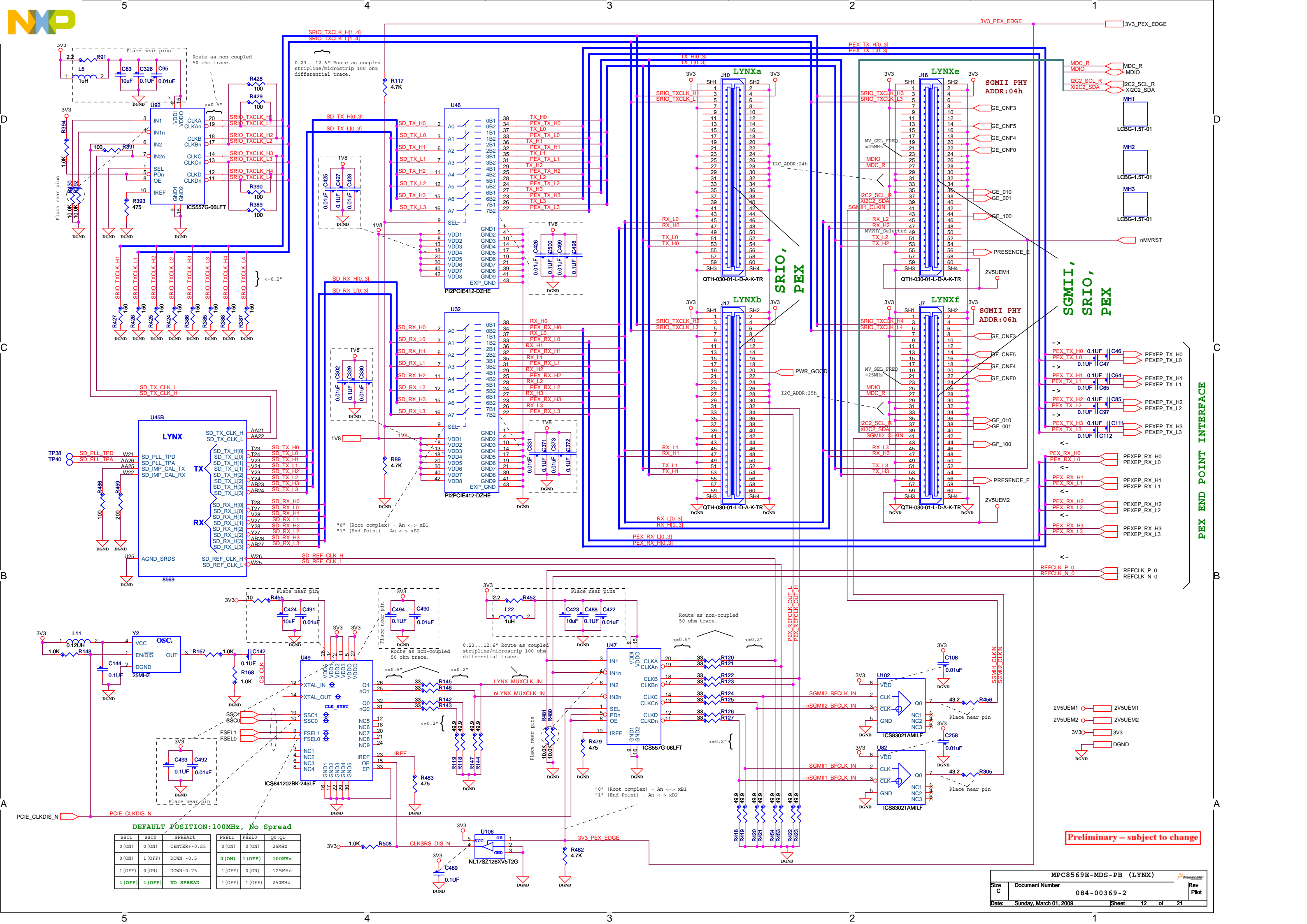
Address "00001"

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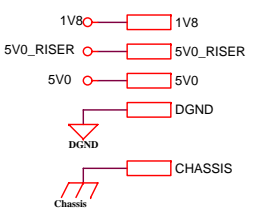
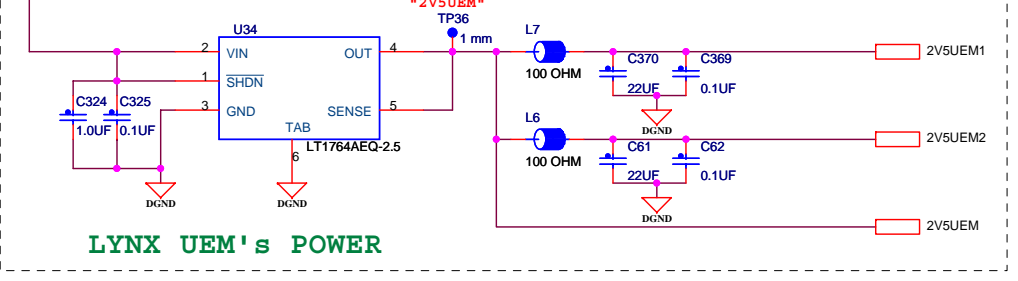
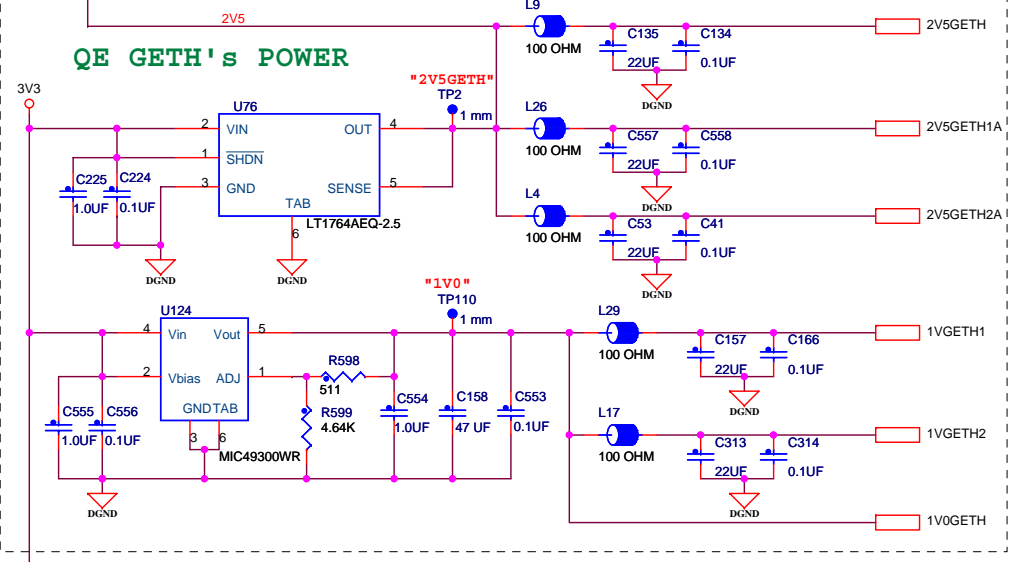
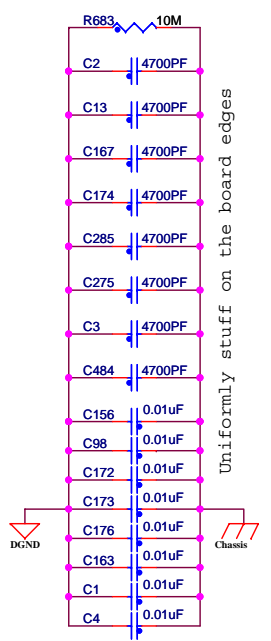
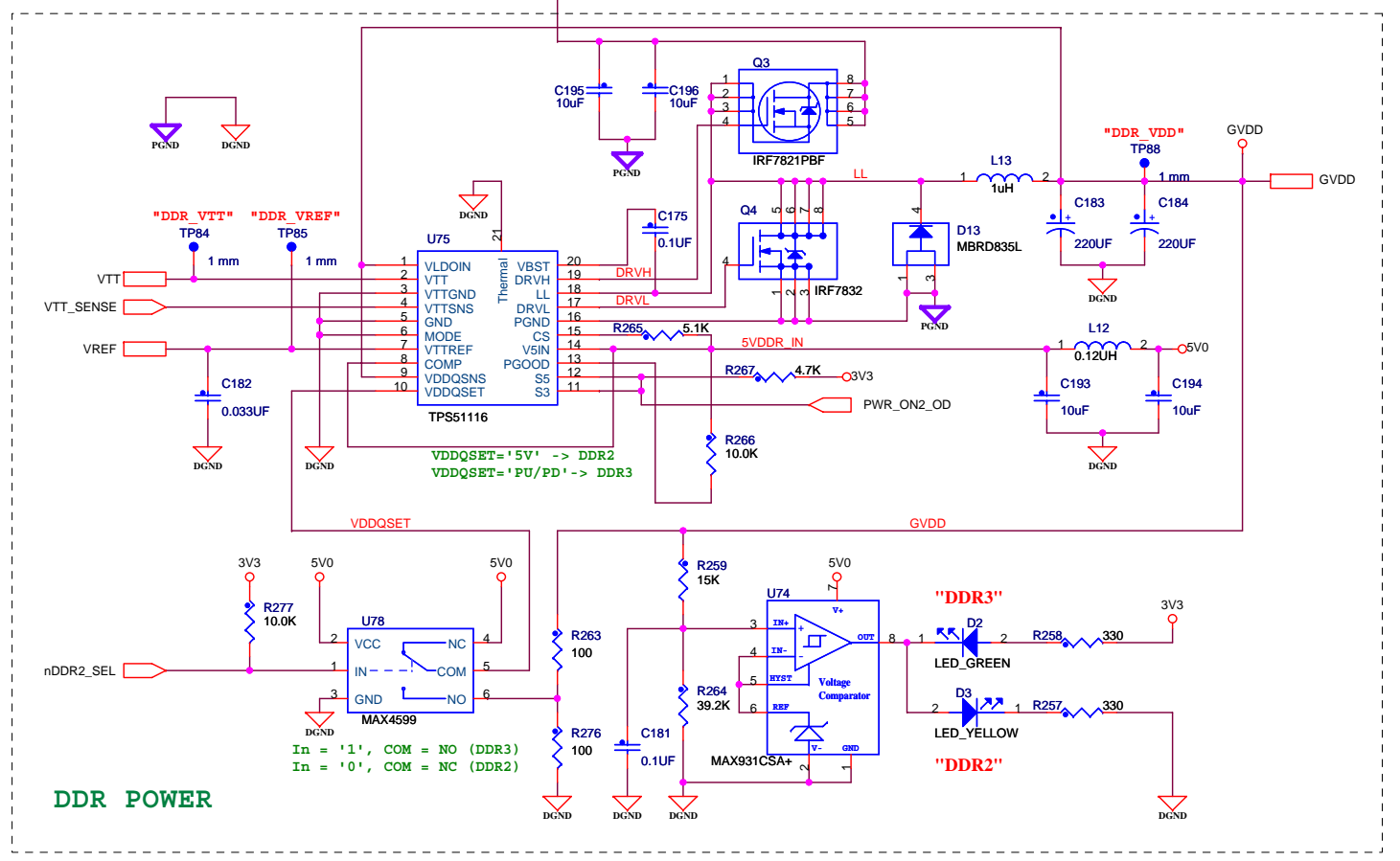
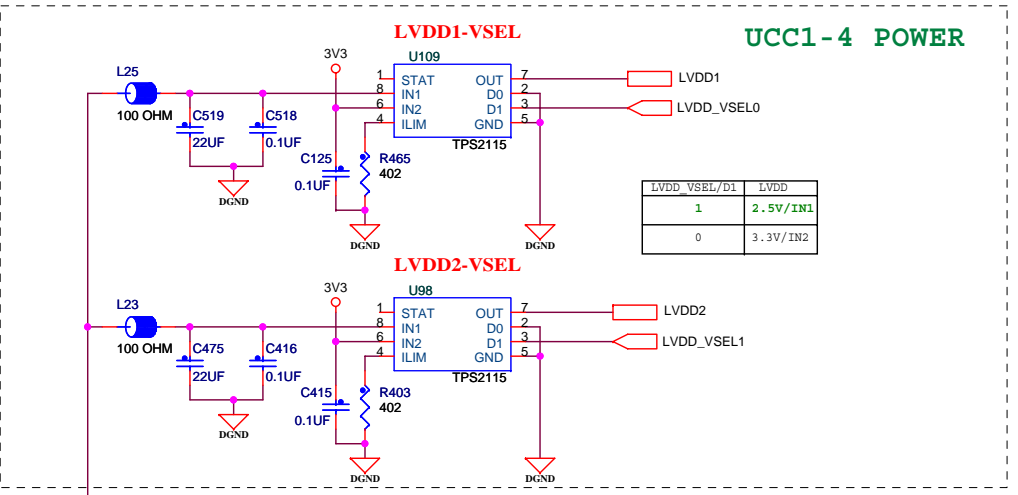
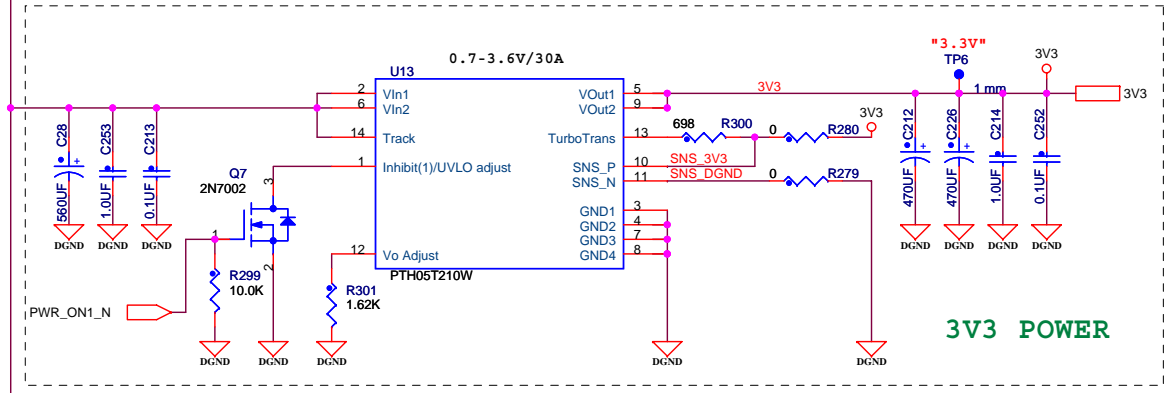
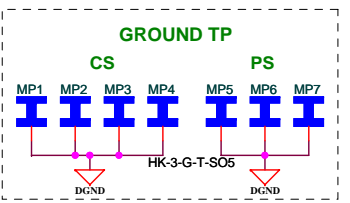
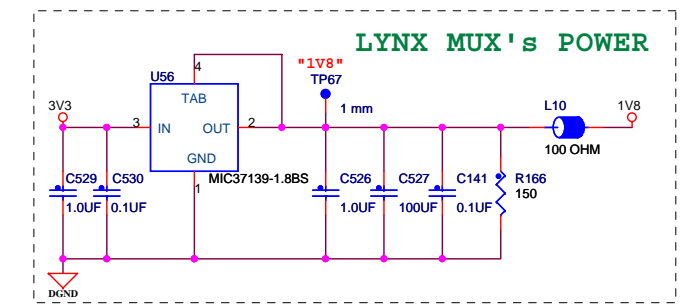
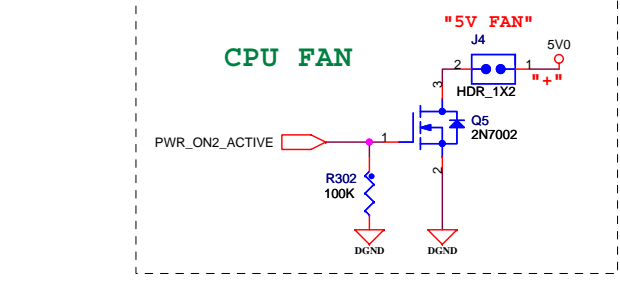
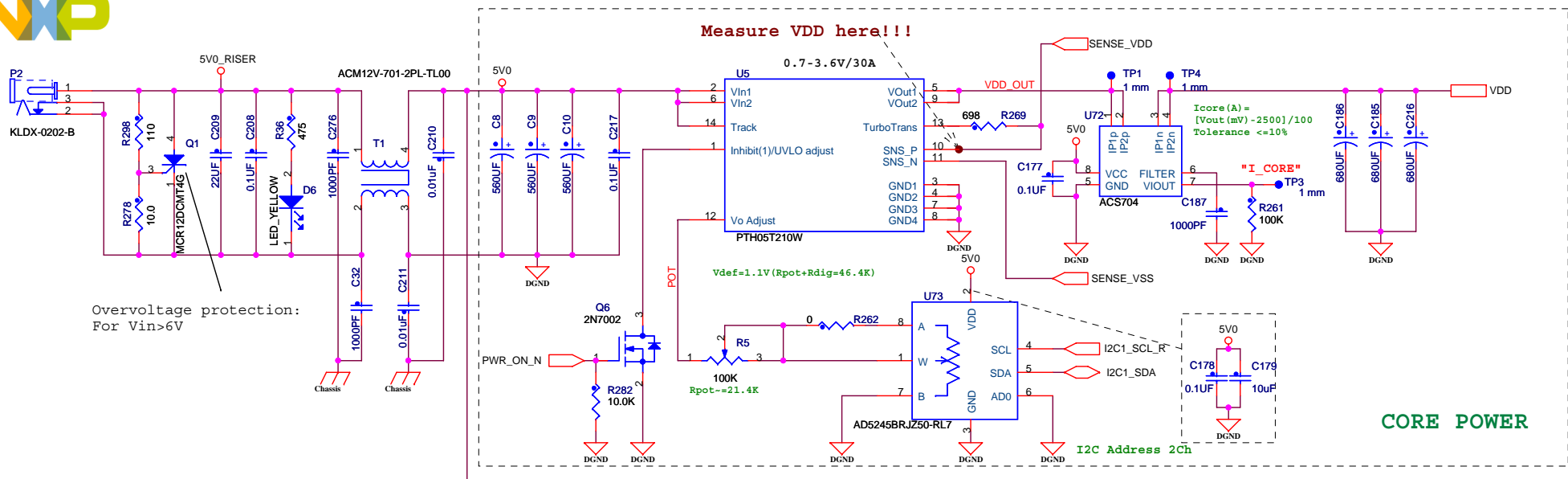
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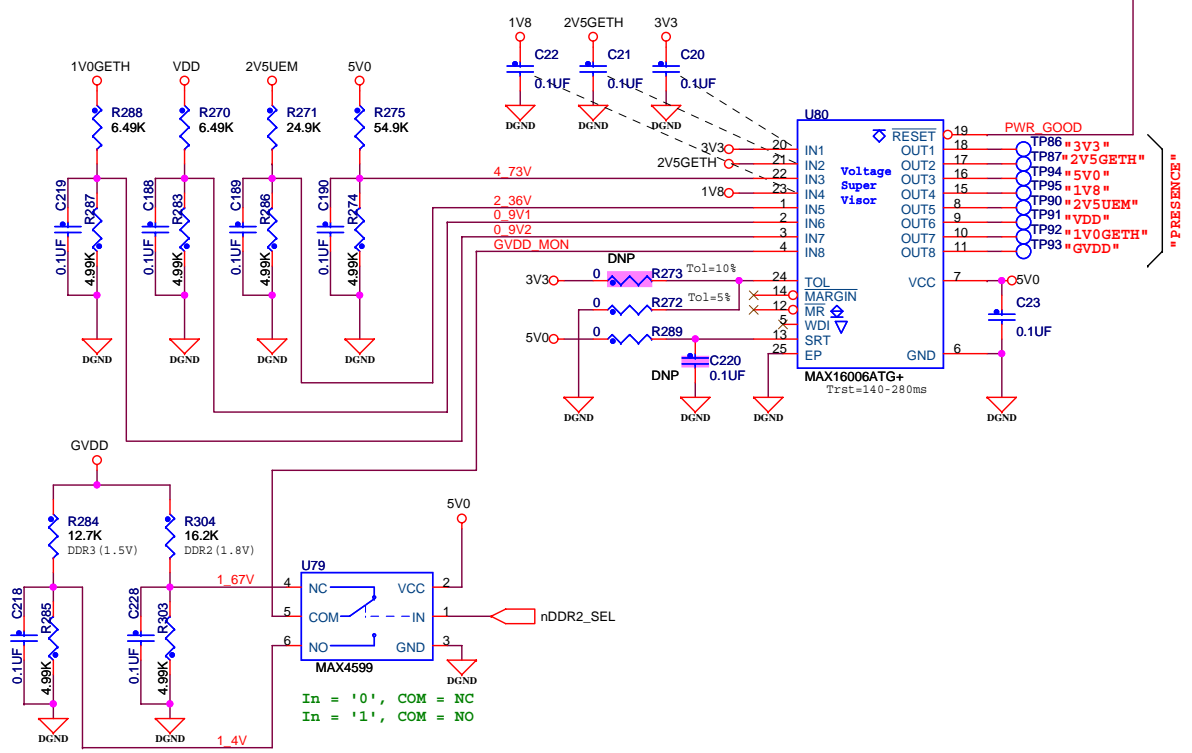
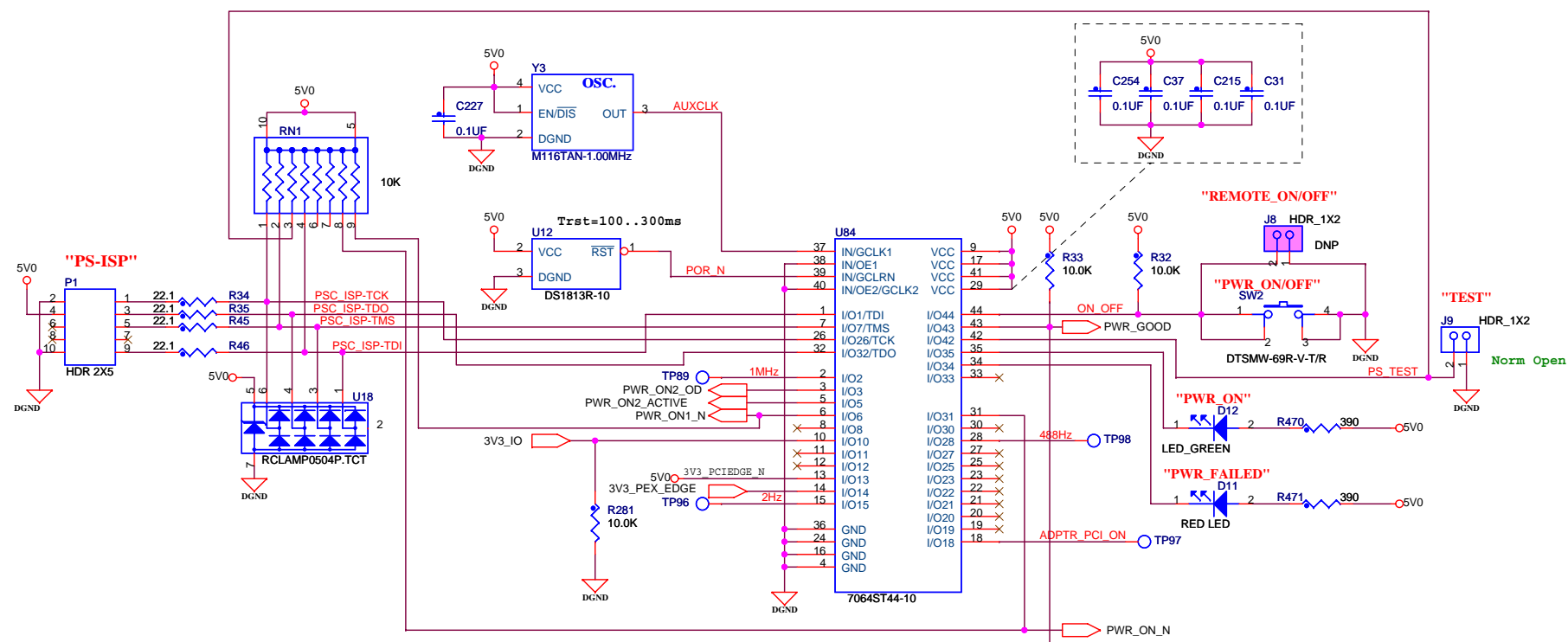
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DEFAULT POSITION: 100MHz, No Spread

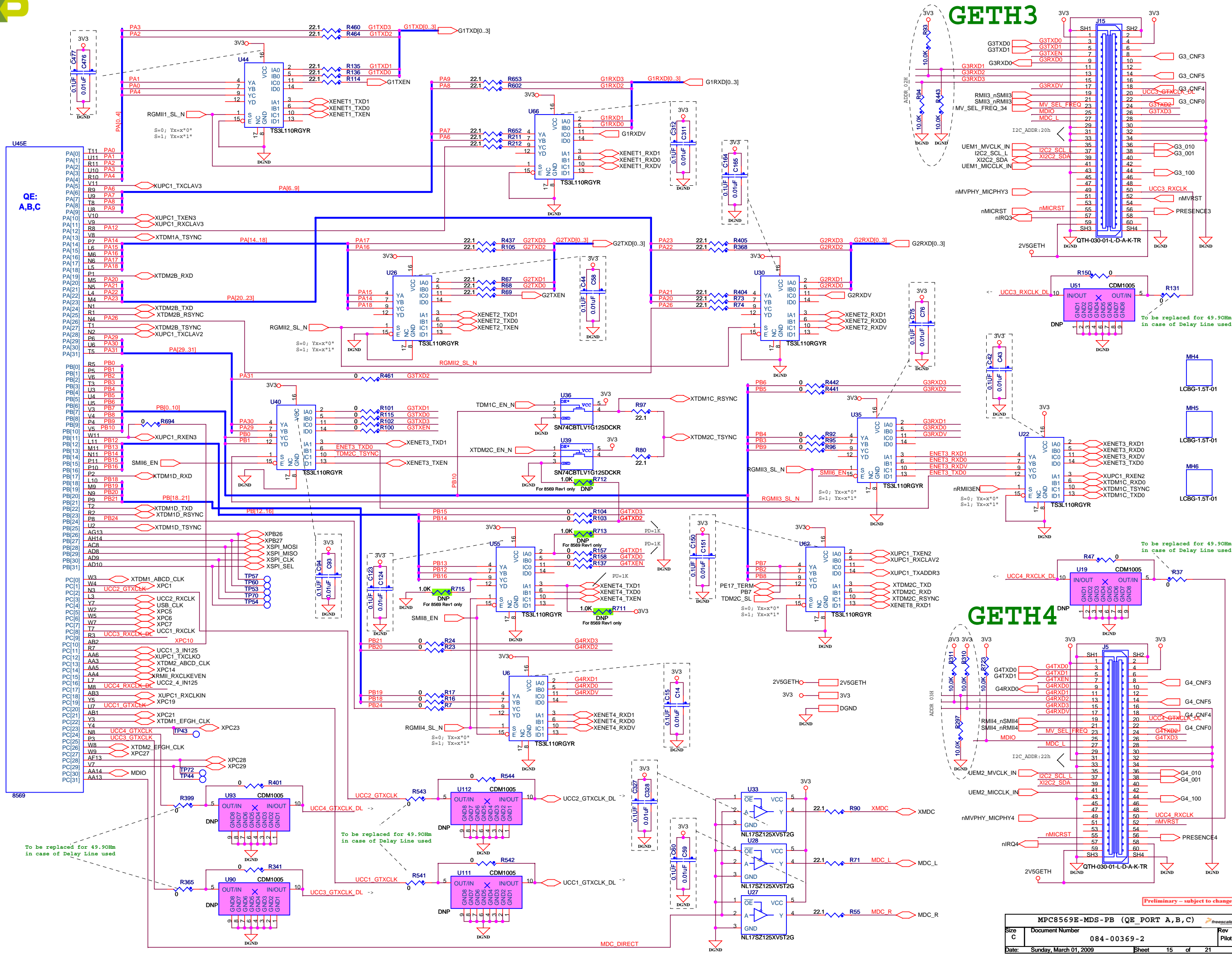
SSC1	SSC0	SPREAD#	FSEL1	FSEL0	Q0:Q1
0 (ON)	0 (ON)	CENTER +0.25	0 (ON)	0 (ON)	25MHz
0 (ON)	1 (OFF)	DOWN -0.5	0 (ON)	1 (OFF)	100MHz
1 (OFF)	0 (ON)	DOWN -0.75	1 (OFF)	0 (ON)	125MHz
1 (OFF)	1 (OFF)	NO SPREAD	1 (OFF)	1 (OFF)	250MHz



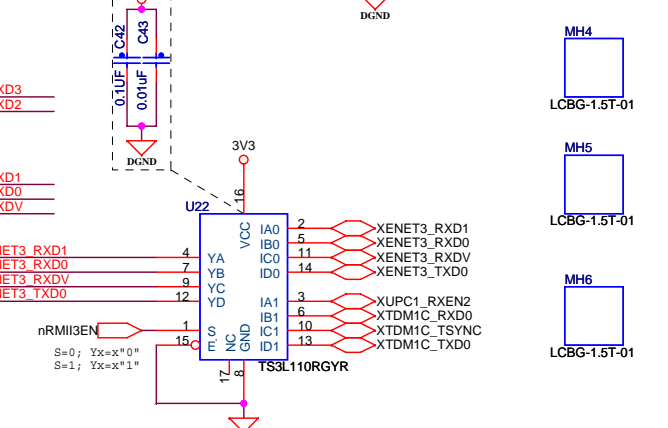
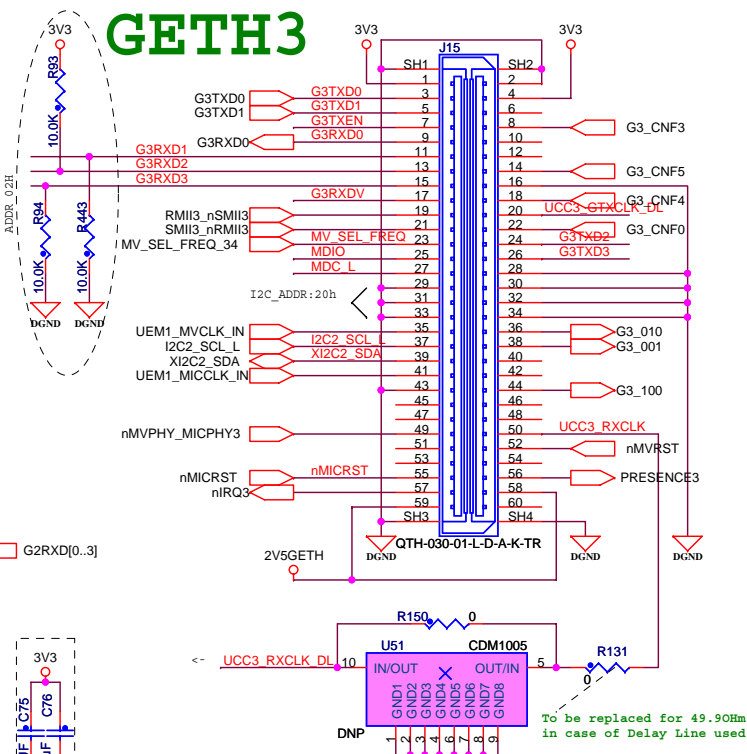
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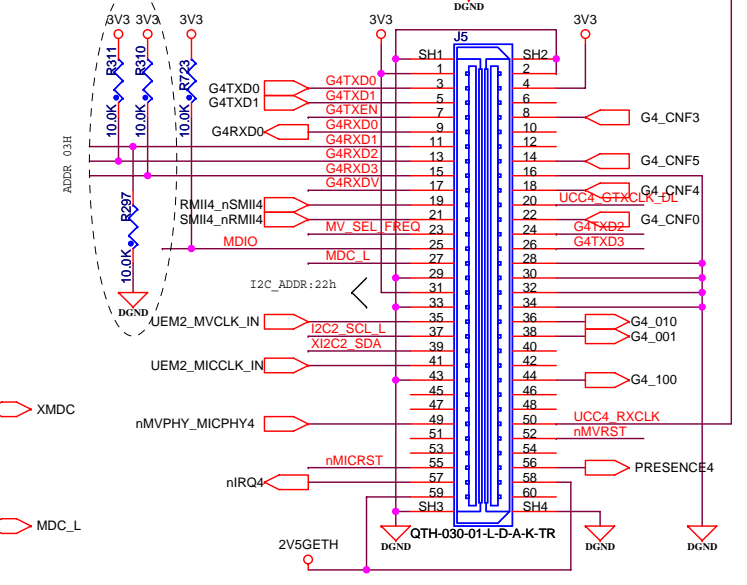
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GETH3



GETH4

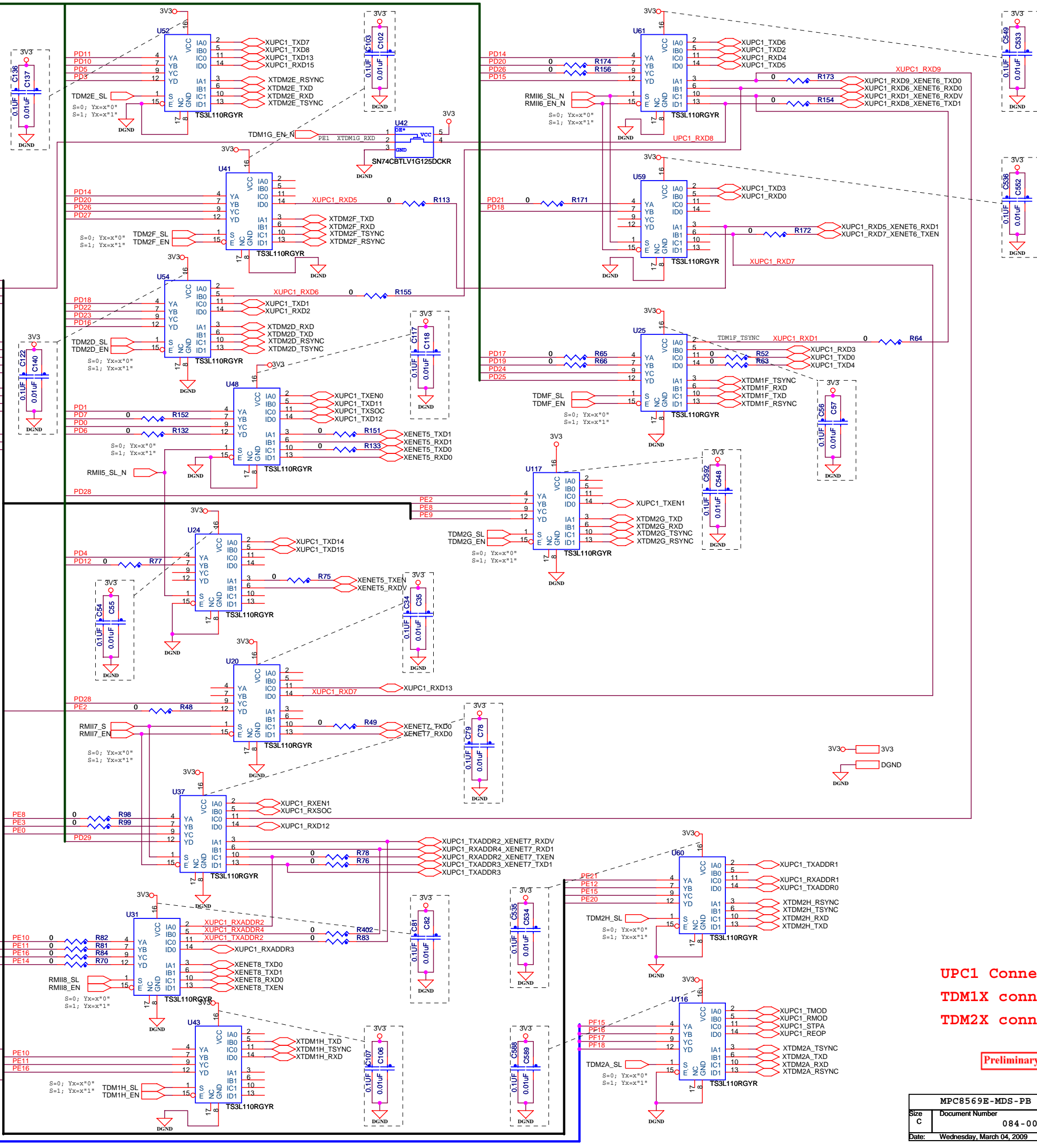
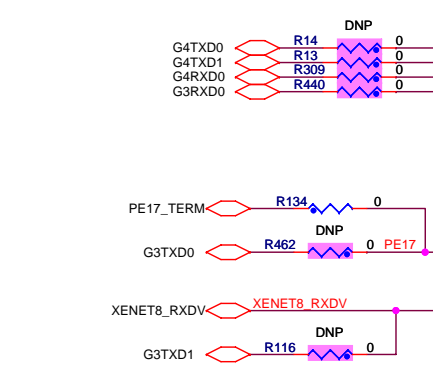
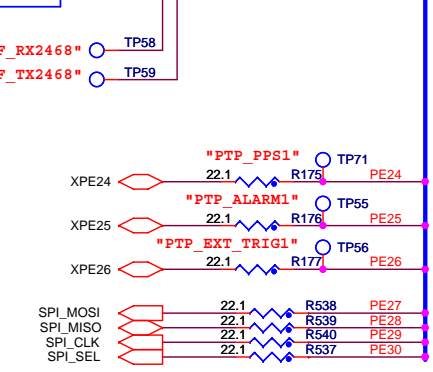
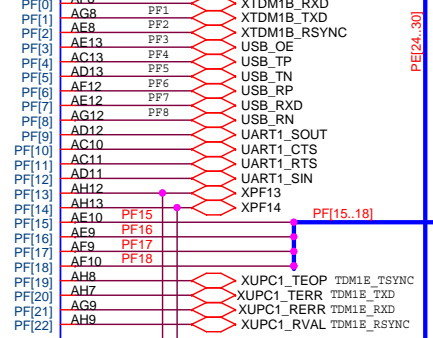
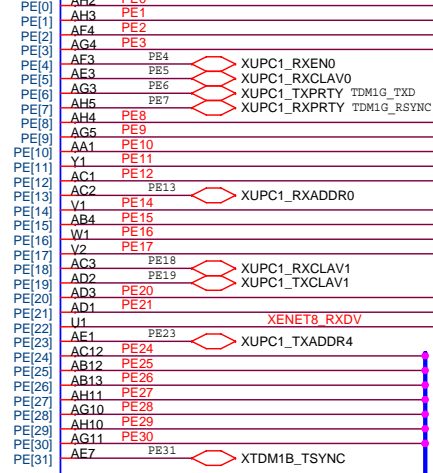
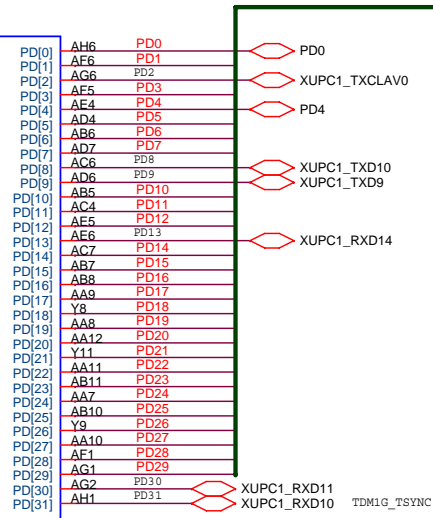


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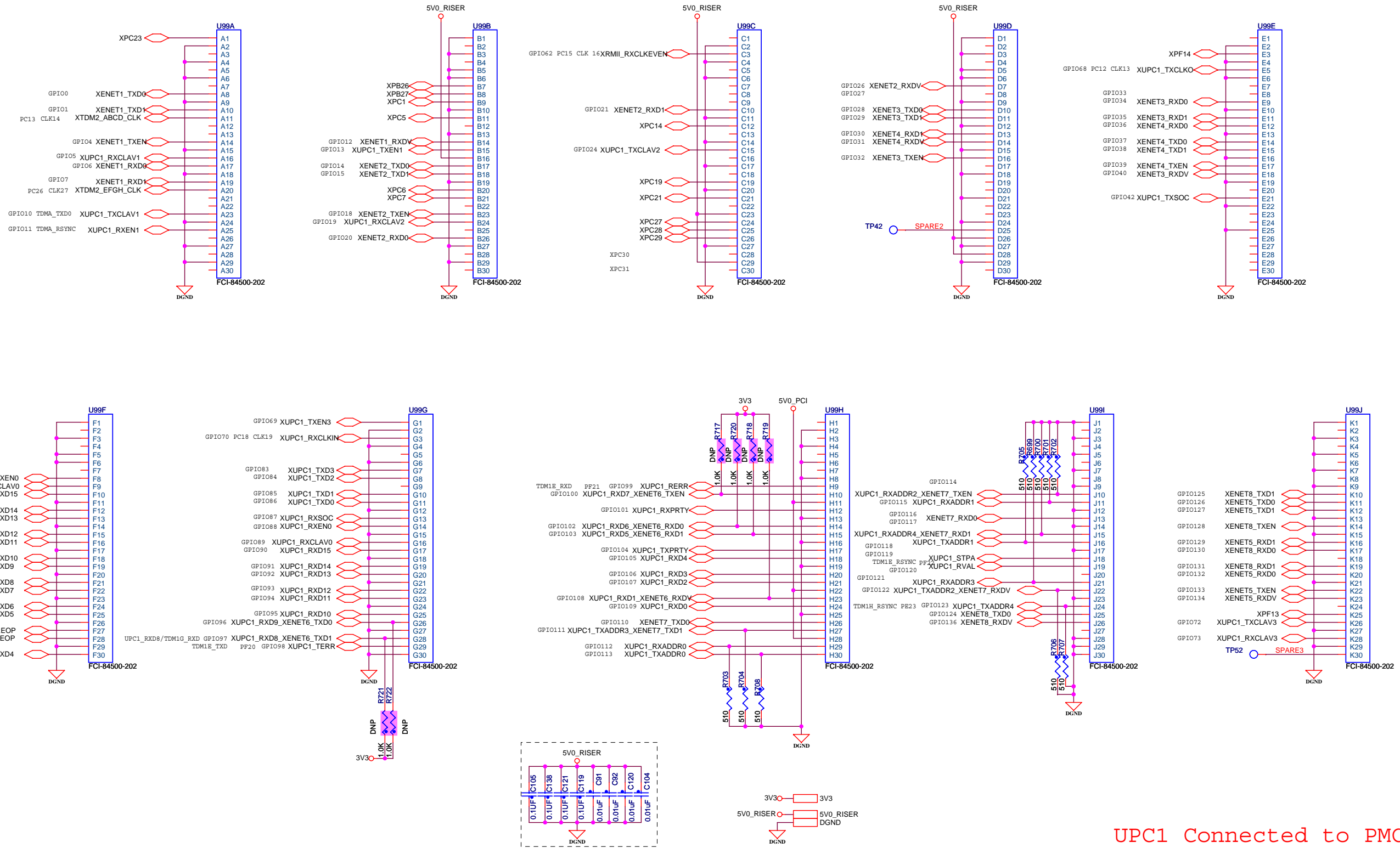
QE:
D,E,F



UPC1 Connected to PMC0
 TDM1X connected to PMC0
 TDM2X connected to PMC1
 Preliminary - subject to change

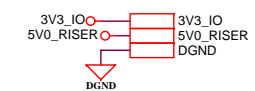
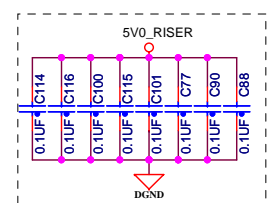
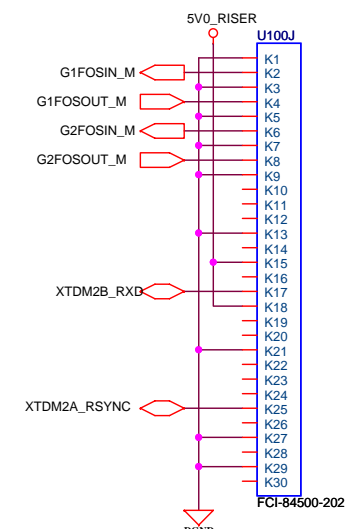
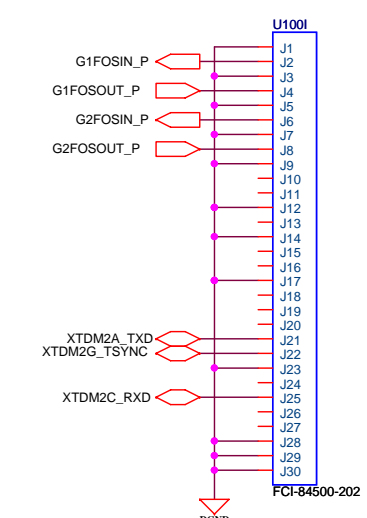
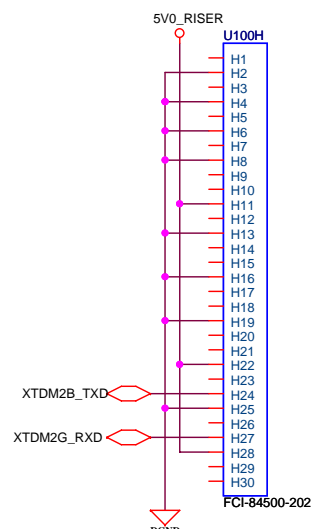
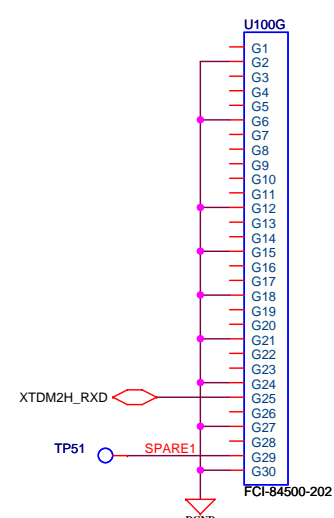
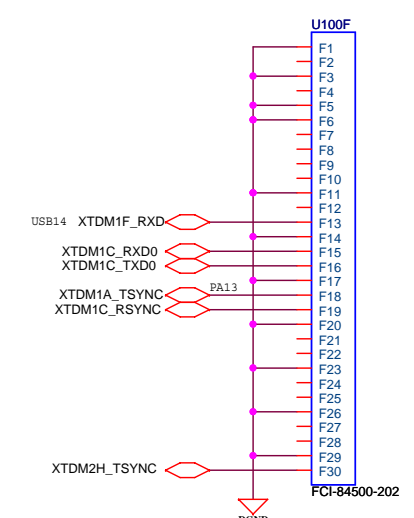
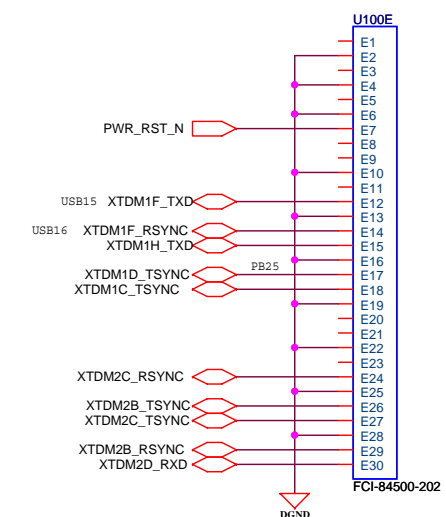
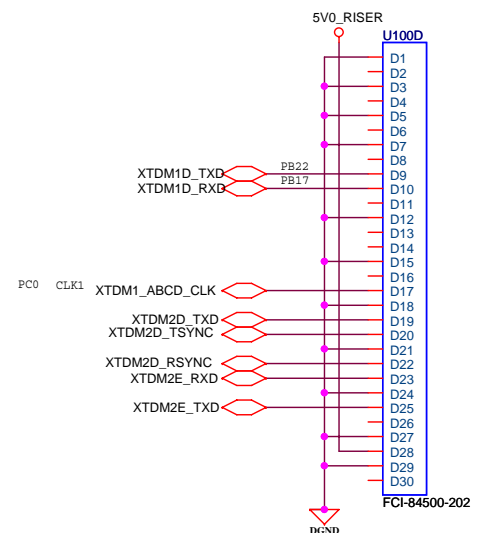
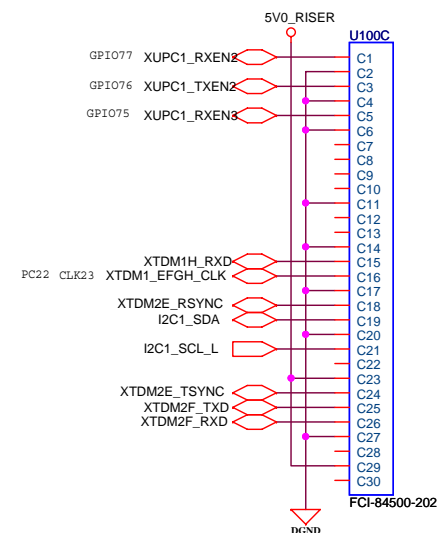
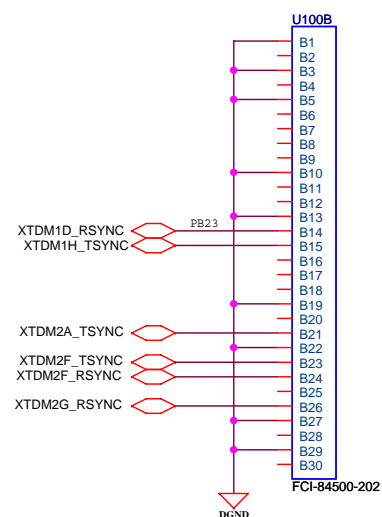
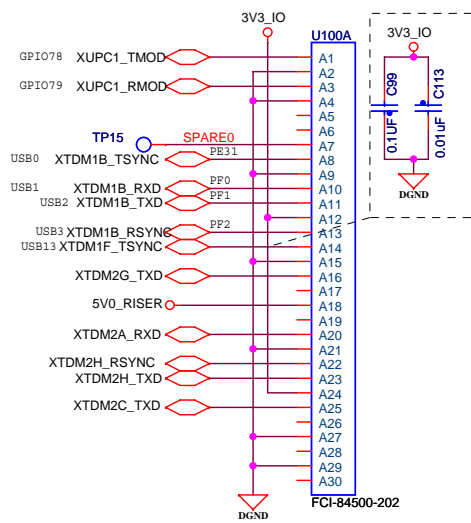
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GPIO



UPC1 Connected to PMC0
TDM1X connected to PMC0
TDM2X connected to PMC1

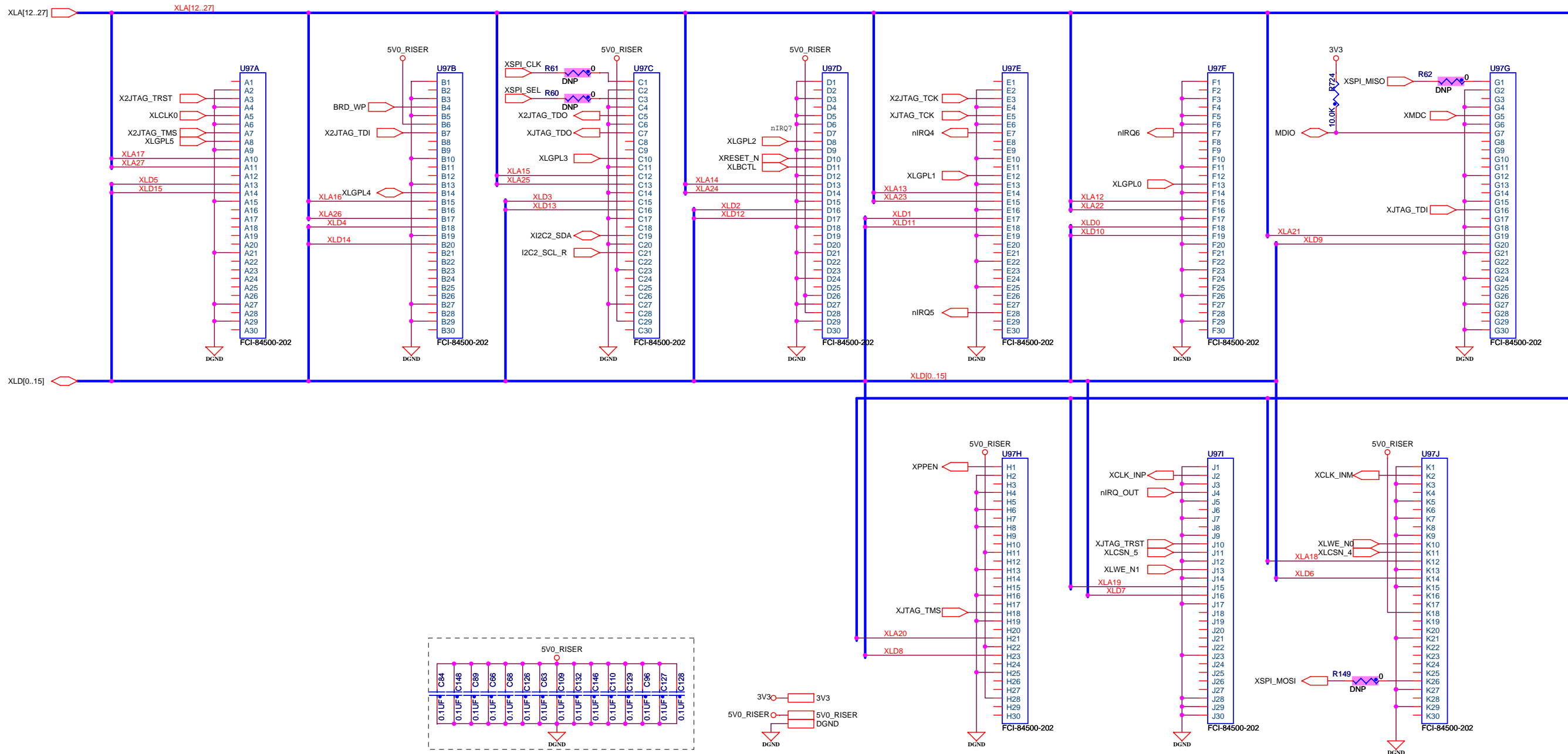
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UPC1 Connected to PMC0
 TDM1X connected to PMC0
 TDM2X connected to PMC1

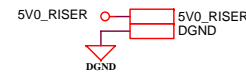
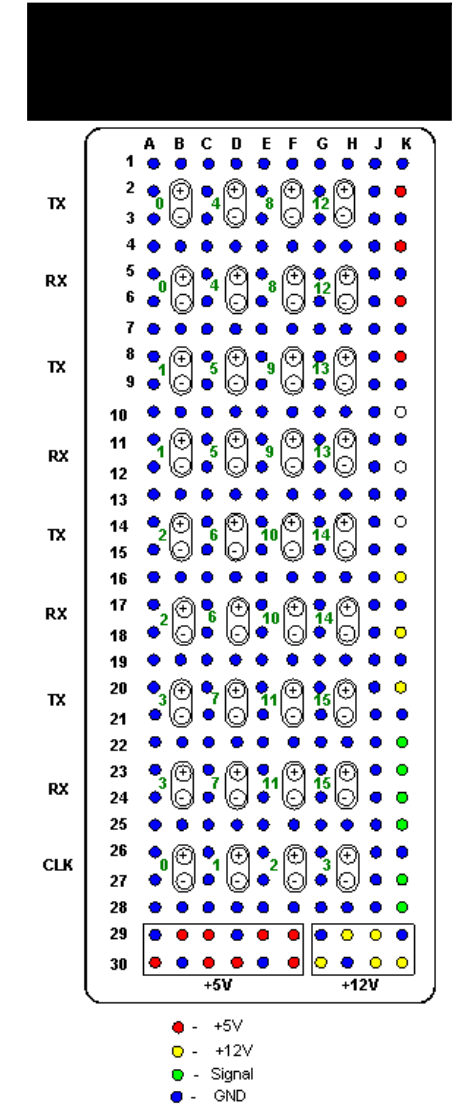
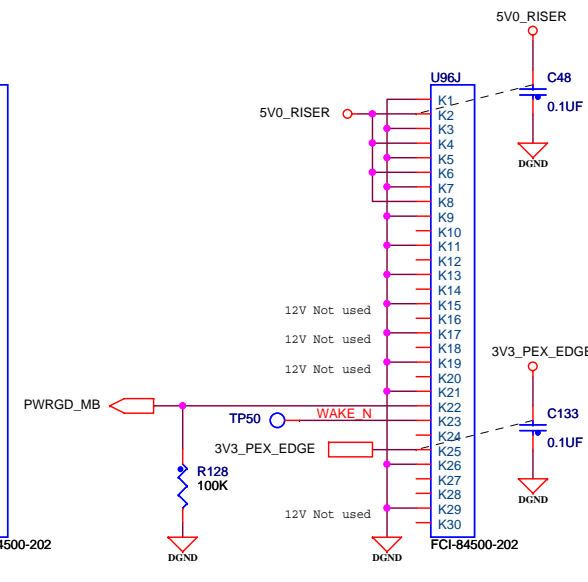
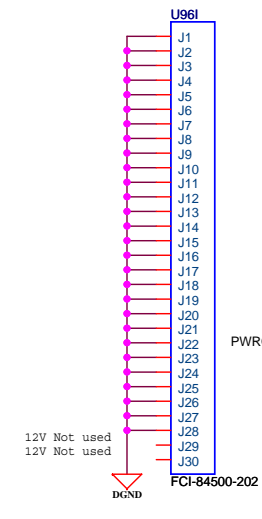
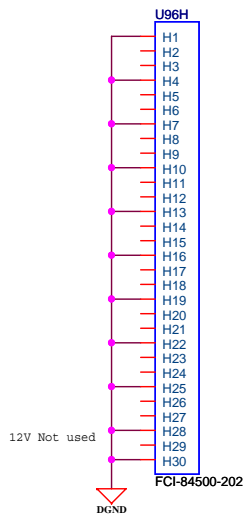
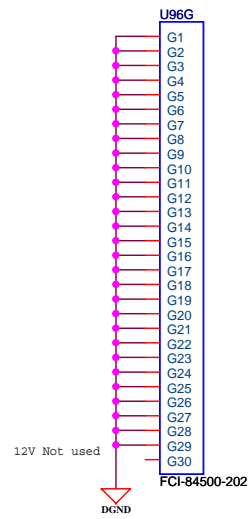
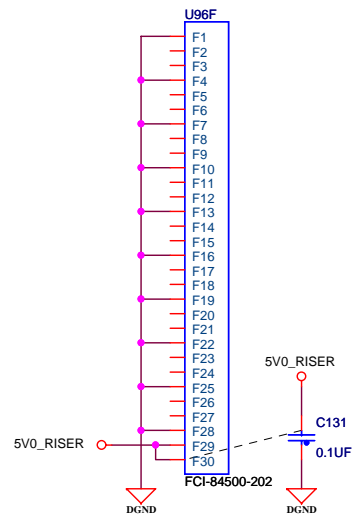
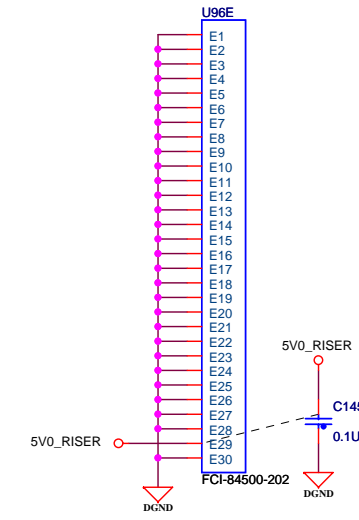
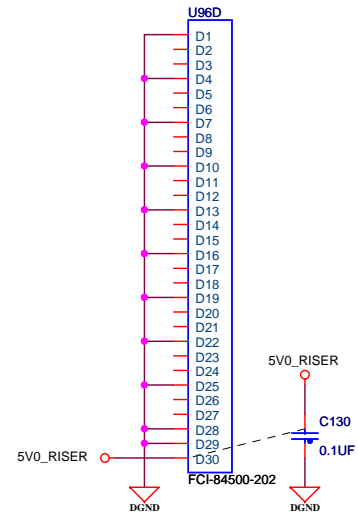
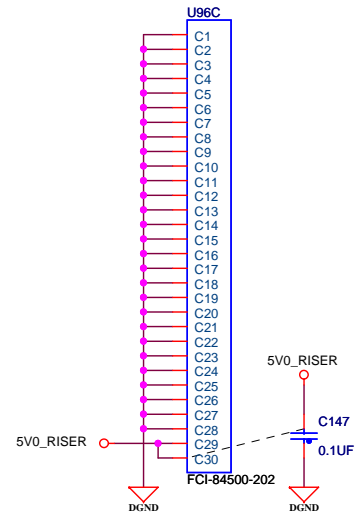
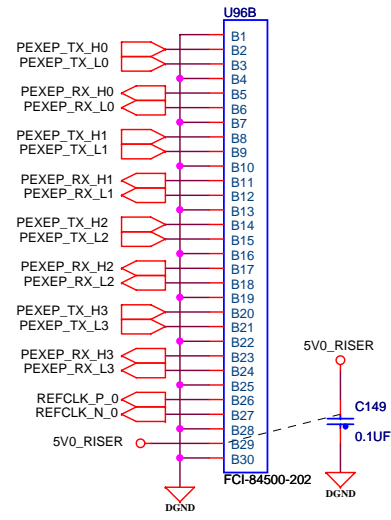
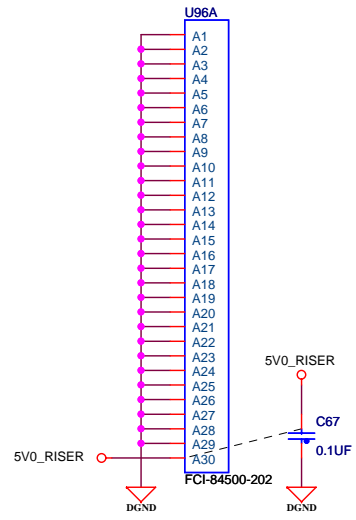
Preliminary – subject to change

Local Bus



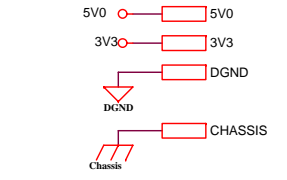
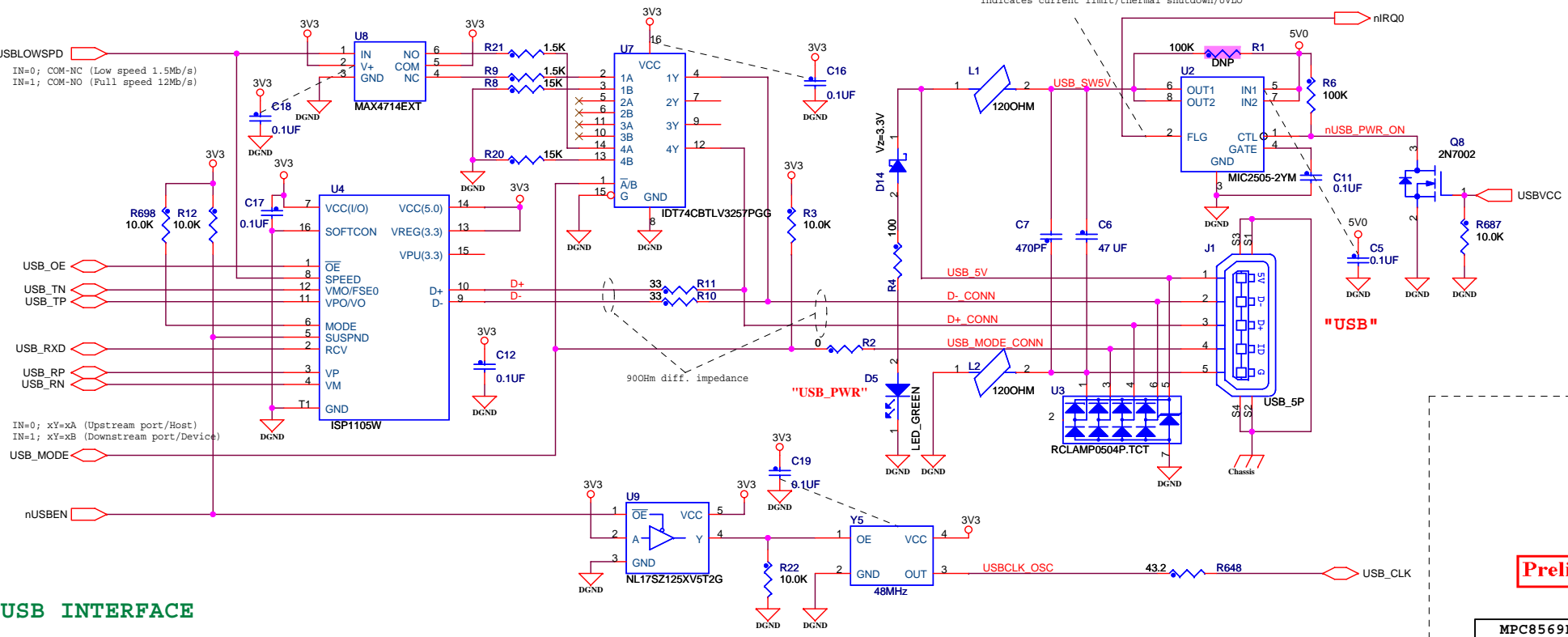
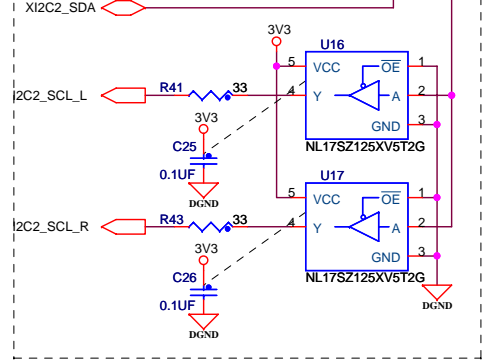
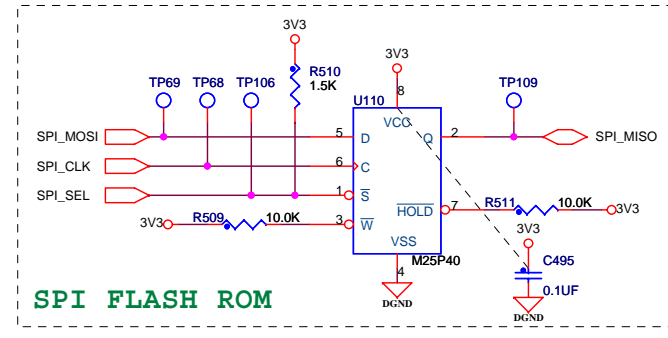
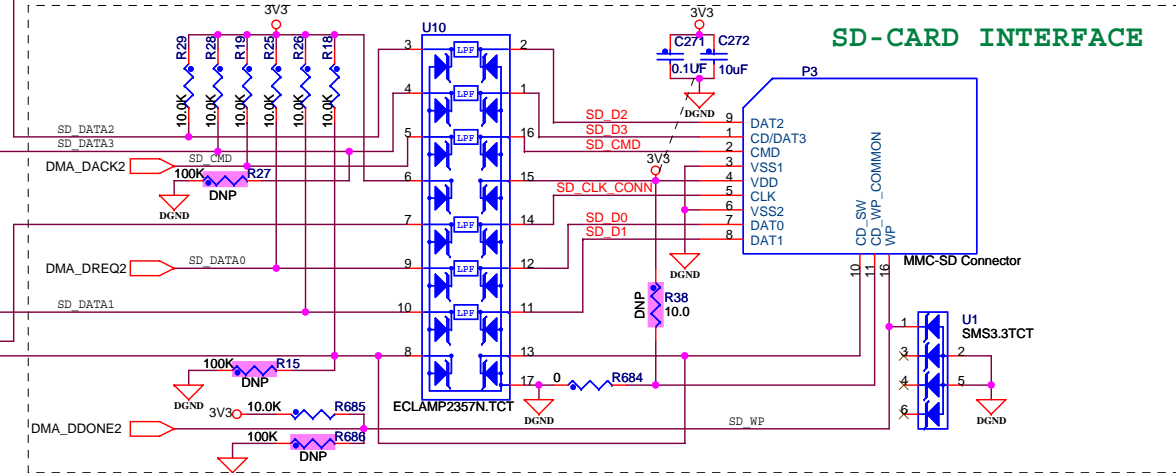
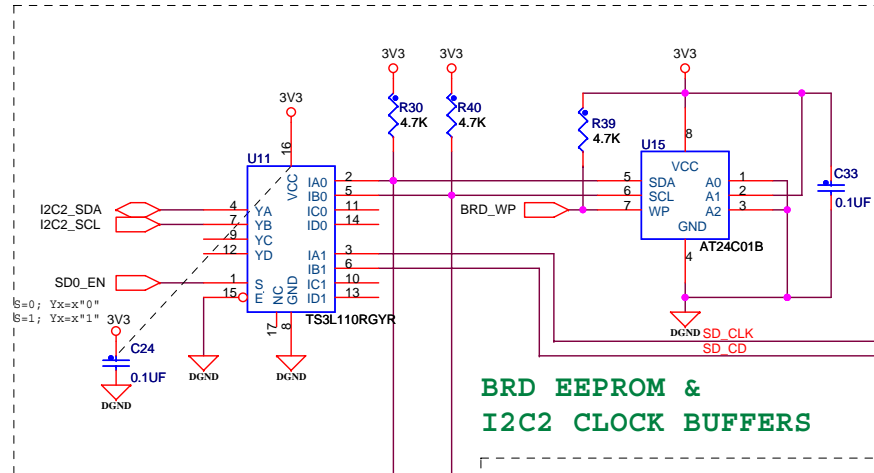
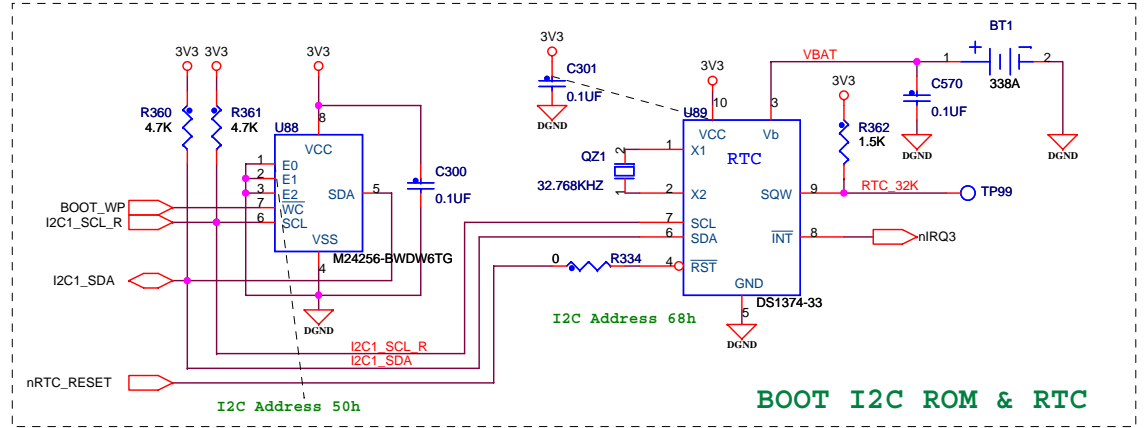
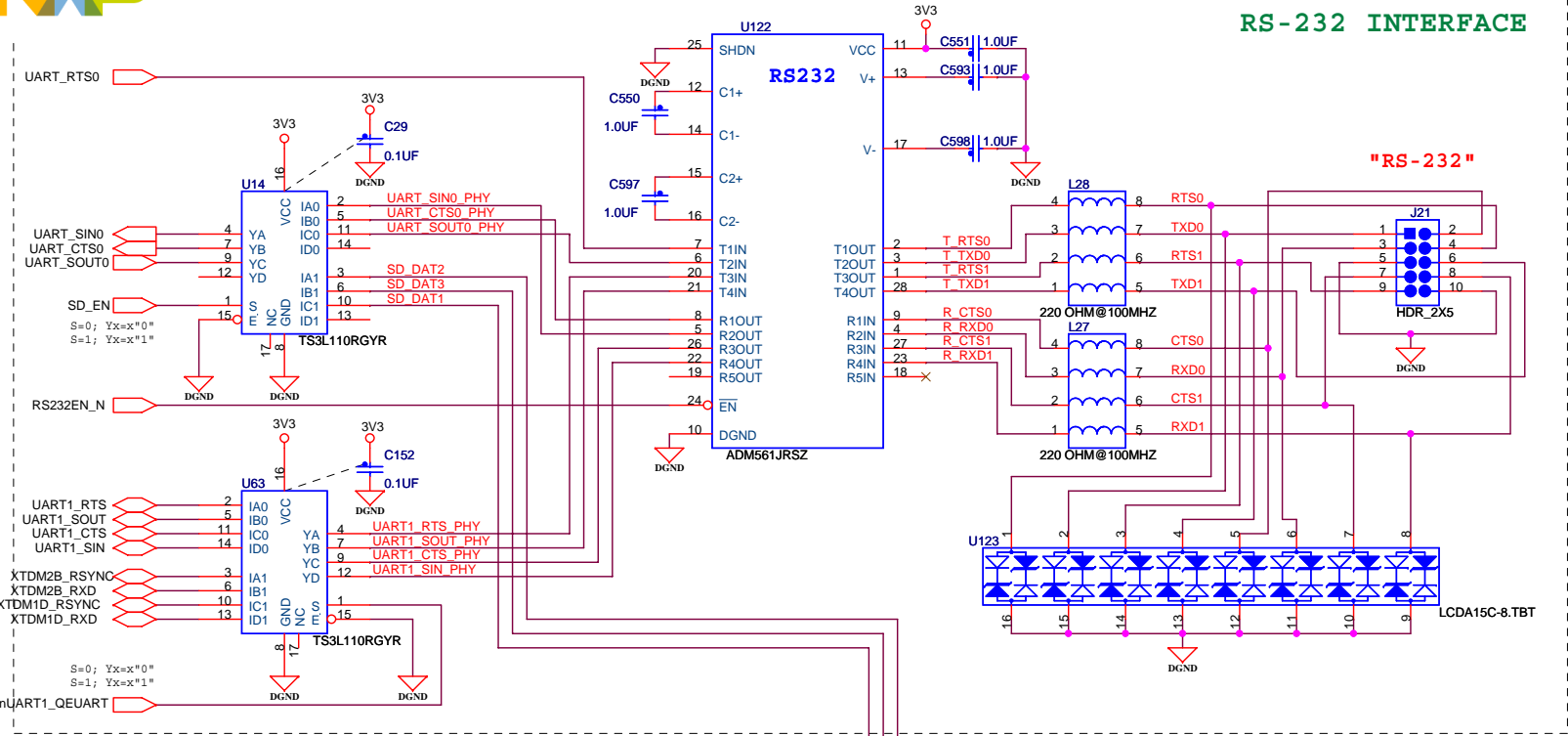
Preliminary – subject to change

LYNX lines



Preliminary – subject to change

RS-232 INTERFACE



Preliminary – subject to change