High-Performance Analog Products

# Analog Applications Journal

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# Contents



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# Introduction

*Analog Applications Journal* is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

# Clock jitter analyzed in the time domain, Part 2

**By Thomas Neu**
*Systems and Applications Engineer*

## Introduction

Part 1 of this three-part article series focused on how to accurately estimate jitter from a clock source and combine it with the aperture jitter of an ADC. In this article, Part 2, that combined jitter will be used to calculate the ADC's signal-to-noise ratio (SNR), which will then be compared against actual measurements.

## Measurements with filtered sampling clock

An experiment was set up to see how well the measured clock phase noise matched the clock jitter extracted from the ADC's measured SNR. As shown in Figure 11, a Texas Instruments (TI) CDCE72010 with a Toyocom 491.52-MHz VCXO was used to generate a 122.88-MHz sampling clock, and the filtered phase-noise output was measured with the E5052A from Agilent. Two different TI data converters (ADS54RF63 and ADS5483) were evaluated by using an input frequency whose SNR was predominantly limited by the sampling-clock jitter. The size of the fast Fourier transform (FFT) was chosen to be 131,000 points.

The plot in Figure 12 illustrates the measured output phase noise of the filtered CDCE72010 LVCMOS output. An FFT size of 131,000 points sets the lower integration bandwidth to ~500 Hz. The upper integration limit is set by the bandpass filter, whose effect is clearly visible in the phase-noise plot. Phase noise beyond the bandpass-filter limit shown in the plot is the noise floor of the E5052A and should not be included in the jitter calculation. The integration of the filtered phase-noise output resulted in a clock jitter of ~90 fs.

Next, a baseline for the thermal noise was established. Both ADCs were sampled with a filtered sampling clock directly from the clock-source generator with ~35 fs of jitter, and the CDCE72010 was bypassed. The input frequency was set to 10 MHz, where no impact on the SNR from clock jitter was expected. Then the aperture jitter for each ADC was determined by increasing the input frequency to where the SNR was mainly jitter-limited. Since the sampling-clock jitter is much lower than the estimated ADC aperture jitter, the calculation should be very accurate. It is also important to remember that the output amplitude of the clock

**Figure 11. Test setup for correlation with filtered clock**

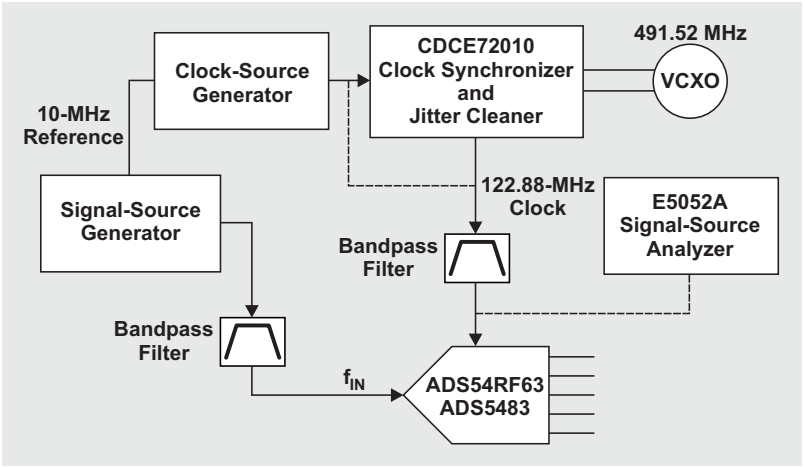
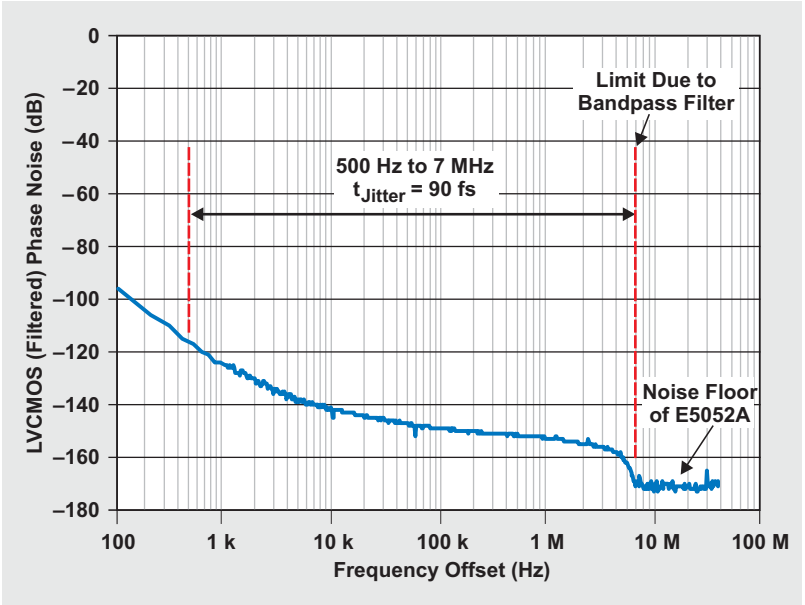



**Figure 12. Measured phase noise of the filtered clock**



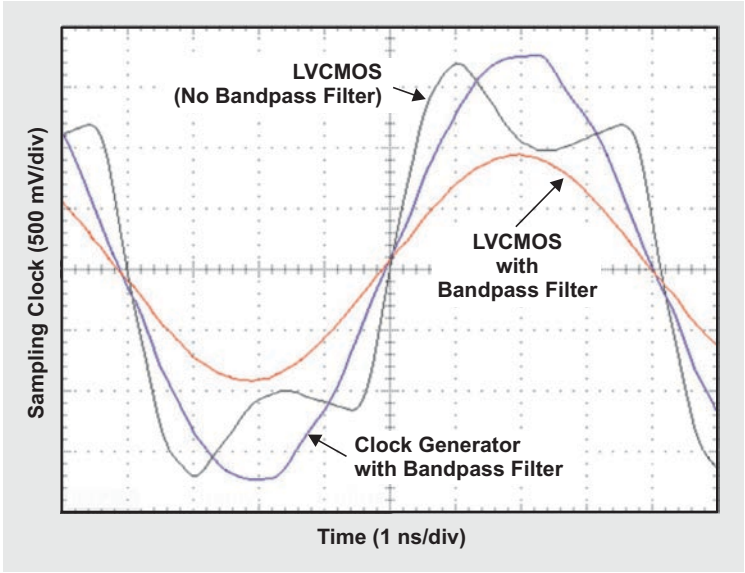
source should be increased (but not so much that it exceeds the maximum ratings of the ADC), boosting the slew rate of the clock signal until the SNR levels off.

Since it is known that the external clock jitter from the filtered output of the clock-source generator is ~35 fs, the ADC aperture jitter can be calculated by using the measured SNR results and solving Equations 1, 2, and 3 in Part 1 (Reference 1) for aperture jitter. Please see Equation 4 below. The measured SNR results as well as the calculated aperture jitter for each ADC are listed in Table 3.

With the ADC aperture jitter and the sampling-clock jitter of the CDCE72010, the ADC's SNR can be calculated and compared against the actual measurement. Using the ADC aperture jitter permits the sampling-clock jitter of the CDCE72010 to be calculated from the measured SNR values, as illustrated in Table 4. At first glance the predicted SNR values are somewhat close to the measured values. However, comparing the calculated sampling-clock jitter for the two ADCs against the measured value of 90 fs reveals a different picture. There is quite a bit of mismatch.

The reason for the mismatch is that the calculated aperture jitter is based on the fast slew rate of the clock-source generator. The bandpass filter on the LVCMOS output of the CDCE72010 eliminates the higher-order harmonics of the clock signal that help create fast rising and falling edges. The scope plot in Figure 13 demonstrates how the bandpass filter drastically reduces the slew rate of the unfiltered LVCMOS output and turns the square wave into a sine wave.

**Figure 13. Impact of clock filter on sampling clock's slew rate**




$$t_{Aperture\_ADC} = \sqrt{\left[\frac{\sqrt{\left(10^{-\frac{SNR_{Measured}}{20}}\right)^2 - \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2}}{2\pi \times f_{IN}}\right]^2 - (t_{Jitter,Clock\_Input})^2} \qquad (4)$$

**Table 3. Measured SNR and calculated jitter**

| DEVICE | THERMAL NOISE (MEASURED SNR AT $f_{IN}$ = 10 MHz) (dBFS) | MEASURED SNR AT HIGH $f_{IN}$ (JITTER-LIMITED) (dBFS) | CALCULATED APERTURE JITTER (fs) |
|---|---|---|---|
| ADS54RF63 | 64.4 | 61.0 ($f_{IN}$ = 1 GHz) | ~115 |
| ADS5483 | 79.1 | 78.2 ($f_{IN}$ = 100 MHz) | ~85 |

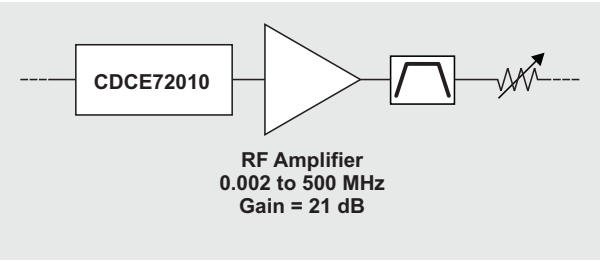
**Table 4. SNR results with 90-fs clock jitter**

| DEVICE | CALCULATED SNR WITH 90-fs CLOCK JITTER (dBFS) | MEASURED SNR (dBFS) | CALCULATED JITTER FROM MEASURED SNR (fs) |
|---|---|---|---|
| ADS54RF63 ($f_{IN}$ = 1 GHz) | 59.9 | 58.7 | ~130 |
| ADS5483 ($f_{IN}$ = 100 MHz) | 77.8 | 77.1 | ~125 |

One way to improve the slew rate is to add a low-noise RF amplifier with a fair amount of gain between the LVCMOS output of the CDCE72010 and the bandpass filter (see Figure 14). The amplifier should be placed before the filter so that its noise contribution to the clock signal is limited to the filter bandwidth and not to the clock input bandwidth of the ADC. Since the amplifier in the next experiment has a gain of 21 dB, a variable attenuator was added after the bandpass filter to match the slew rate of the filtered LVCMOS signal to the filtered output of the clock generator. The attenuator also protects the clock input of the ADCs from exceeding the maximum ratings.

With the low-noise RF amplifier included in the clock's input path, the SNR measurement at high input frequency was repeated for both data converters. The results are shown in Table 5. It can be observed that the measured SNR matches the predicted SNR very well. Using Equation 5 below provided calculated clock-jitter values that are within 5 fs of the 90-fs clock jitter, which was derived from the phase-noise measurement.

**Figure 14. RF amplifier added in front of bandpass filter to reduce slew rate**




## Experiment with unfiltered sampling clock

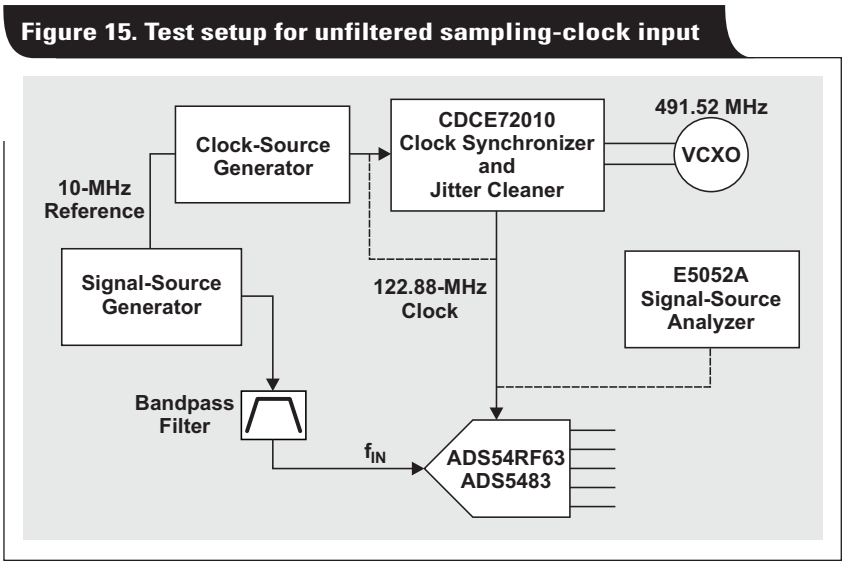
To stress the importance of filtering the sampling clock, the clock bandpass filter was removed from the CDCE72010 output in the next experiment. The E5052A phase-noise analyzer was used to capture the clock phase noise as shown in the setup in Figure 15. Unfortunately, however,

**Table 5. SNR results with 90-fs clock jitter and RF amplifier**

| DEVICE | CALCULATED SNR WITH 90-fs CLOCK JITTER (dBFS) | MEASURED SNR WITH RF AMPLIFIER (dBFS) | CALCULATED JITTER FROM MEASURED SNR (fs) |
|---|---|---|---|
| ADS54RF63 ($f_{IN}$ = 1 GHz) | 59.9 | 60.0 | ~85 |
| ADS5483 ($f_{IN}$ = 100 MHz) | 77.8 | 77.6 | ~95 |

$$t_{Jitter,Clock\_Input} = \sqrt{\left[\frac{\sqrt{\left(10^{-\frac{SNR_{Measured}}{20}}\right)^2 - \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2}}{2\pi \times f_{IN}}\right]^2 - (t_{Aperture\_ADC})^2} \quad (5)$$

**Figure 15. Test setup for unfiltered sampling-clock input**



the analyzer measures the phase noise only up to a 40-MHz offset of the carrier frequency and doesn't give any clue about the phase-noise characteristic beyond that point.

To set the correct upper integration limit when an unfiltered clock is used, the sampling theory has to be reviewed again. The unfiltered clock output of the CDCE72010 looks like a square wave with fast rising and falling edges caused by the higher-order harmonics of the fundamental sinusoid of the clock frequency. These harmonics have lower amplitude than the fundamental, and their amplitude decreases as the harmonic order increases.

At the sampling instant, both the fundamental sine wave and the higher-order harmonics mix with the input signal as illustrated in Figure 16. (For simplification, only one harmonic is shown.) Therefore, the phase noise around the third-order harmonic (for example) mixes with the input signal, and the third harmonic creates a mixing product as well. However, since the third harmonic of the clock signal has lower amplitude, the amplitude of this mixing product is also reduced.

When the two sampled signals are combined, it can be seen that the overall degradation of the phase noise caused by the third harmonic becomes minimal once the amplitude difference exceeds ~3 dB. Since the crossover point between the fundamental and the third harmonic is at $2 \times f_s$, integrating the wideband phase noise to $2 \times f_s$ should give a fairly accurate result.

As shown later in Figure 19, the phase noise of the unfiltered LVCMOS output of the CDCE72010 levels out around –153 dBc/Hz, starting at an offset frequency of

**Figure 16. Clock fundamental and its harmonics mix with input signal at sampling instant**

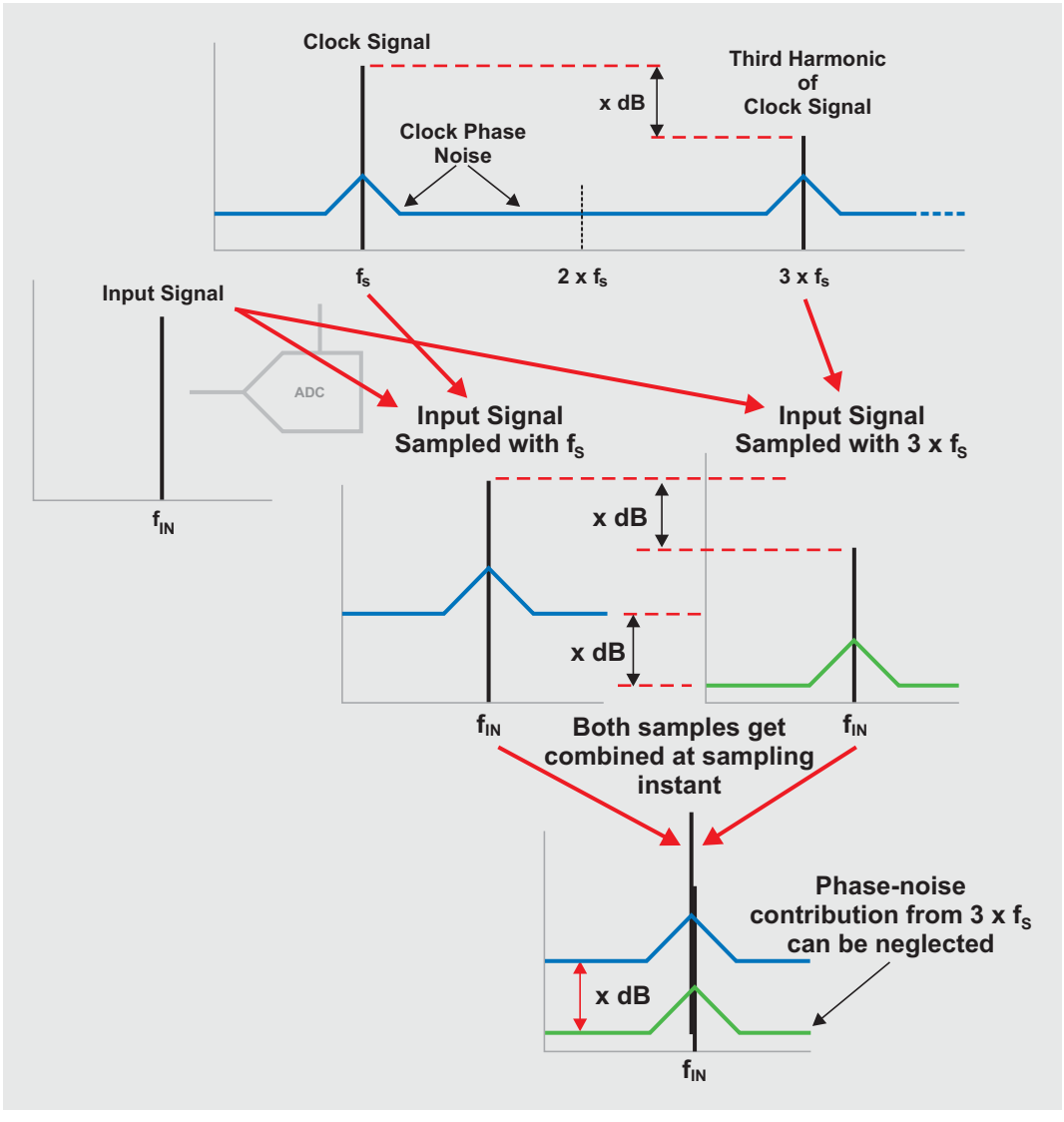


**Table 6. SNR results with 1.27-ps clock jitter**

| DEVICE | CALCULATED SNR WITH 1.27-ps CLOCK JITTER (dBFS) | MEASURED SNR (dBFS) | CALCULATED JITTER FROM MEASURED SNR (fs) |
|---|---|---|---|
| ADS54RF63 ($f_{IN}$ = 1 GHz) | 42.8 | 51.35 | ~450 |

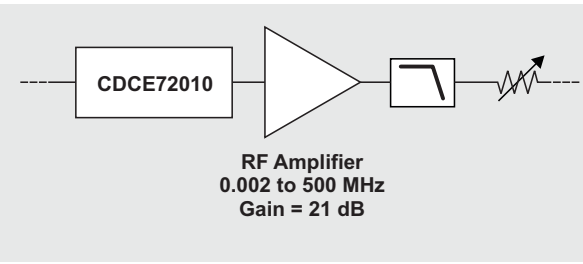
~10 MHz, which is likely due to the thermal noise of the LVCMOS output buffer. The ADS54RF63 EVM has a clock input bandwidth of ~1 GHz (limited by the transformer); hence, theoretically the phase noise should be integrated to ~1 GHz (rolling off at 3 dB at a 900-MHz offset). This would result in ~1.27 ps of sampling-clock jitter and would reduce the SNR at $f_{IN}$ = 1 GHz to ~42.8 dBFS!

The actual SNR measurement was quite a bit better than that, as demonstrated in Table 6. There is a huge gap between the calculated clock jitter and the SNR compared to the actual measurement. This suggests that the phase noise of the LVCMOS output indeed is limited well before the 900-MHz offset boundary set by the transformer.

To prove that the phase noise of the unfiltered clock signal needs to be integrated to roughly twice the sampling frequency, the following experiment was set up: Different low-pass filters were added between the CDCE72010 output and the clock input of the ADS54RF63.

It is important to remember that a low-pass filter with a bandwidth of less than 3x the clock frequency reduces the slew rate of the clock signal just like the bandpass filter did in the earlier experiment. The low-pass filter eliminates the higher-order harmonics that produce the faster rise time and slew rate of the clock signal, thus increasing the aperture jitter of the ADC. For that reason, the same low-noise RF amplifier from the earlier experiment was added to the clock path, and the slew rate was matched to the signal generator by using the variable attenuator (see Figure 17).

**Figure 17. RF amplifier added in front of low-pass filter to reduce slew rate**




Using low-pass filters with different corner frequencies on the sampling clock of the ADS54RF63 (as depicted in Figure 18) resulted in the interesting values in Table 7. The results of this experiment suggest that the phase-noise impact of the LVCMOS output on the clock jitter is limited to roughly 200 to 250 MHz, which corresponds to an 80- to 130-MHz offset from the 122.88-MHz clock signal and is approximately 2x the sampling frequency. Therefore,

**Table 7. Measured SNR for ADS54RF63**

| FILTER TYPE | MEASURED SNR AT $f_{IN}$ = 1 GHz (dBFS) |
|---|---|
| Unfiltered Clock | 51.35 |
| 140-MHz Low-Pass Filter | 54.01 |
| 200-MHz Low-Pass Filter | 51.81 |

**Figure 18. Different low-pass filters limit phase noise**

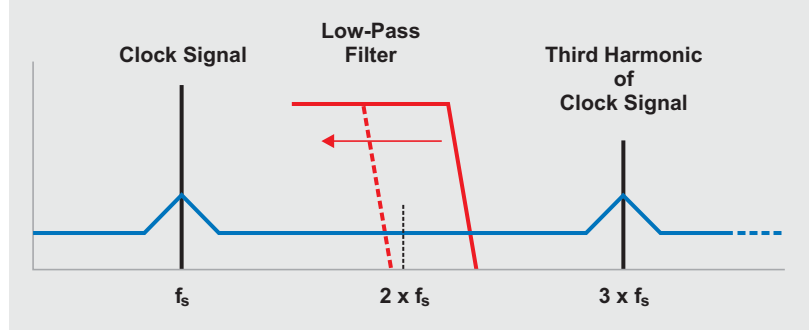


**Table 8. SNR results with 445-fs clock jitter**

| DEVICE | CALCULATED SNR WITH 445-fs CLOCK JITTER (dBFS) | MEASURED SNR (dBFS) | CALCULATED JITTER FROM MEASURED SNR (fs) |
|---|---|---|---|
| ADS54RF63 ($f_{IN}$ = 1 GHz) | 51.6 | 51.35 | ~460 |
| ADS5483 ($f_{IN}$ = 100 MHz) | 71.2 | 70.60 | ~480 |

**Table 9. Measured SNR with filtered and unfiltered clock**

| DEVICE | BANDPASS-FILTERED CLOCK (dBFS) | UNFILTERED CLOCK (dBFS) | BANDPASS-FILTERED CLOCK WITH EXTERNAL AMPLIFIER (dBFS) |
|---|---|---|---|
| ADS54RF63 ($f_{IN}$ = 1 GHz) | 58.7 | 51.35 | 60.0 |
| ADS5483 ($f_{IN}$ = 100 MHz) | 77.1 | 70.60 | 77.6 |

extending the wideband phase noise out to a 123-MHz offset results in a clock jitter of ~445 fs, as can be seen in Figure 19. Ideally the lower integration limit should be at 500 Hz (because of the chosen 131,000-point FFT); however, the jitter contribution from a 500-Hz to 1-kHz offset is extremely low, so it was neglected here in this measurement for simplification.

With the adjusted phase-noise plot, the calculated jitter matches the SNR measurement results very well, to within 10 to 30 fs for both the ADS54RF63 and the ADS5483 (see Table 8). Considering that there is probably a minor clock-jitter contribution from the phase noise around the third harmonic, the calculated SNR is a very close estimation.

## Conclusion

This article has shown how to properly estimate a data converter's SNR when a filtered or unfiltered clock source is used. The results are summarized in Table 9. While a bandpass filter on the clock input is necessary to minimize the clock jitter, experiments showed that it reduces the clock slew rate and degrades the aperture jitter of the ADC. Therefore, the optimum clocking solution consists of a bandpass filter to limit the phase-noise contribution as well as some amplification of the clock amplitude and slew rate to minimize the aperture jitter of the ADC.

Part 3 of this article series will show some practical implementations on how to boost the performance of existing clocking solutions.

## Reference

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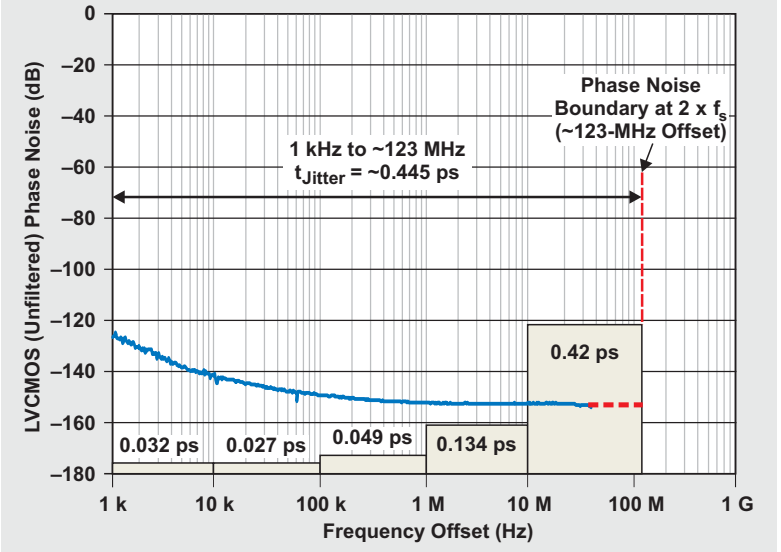
**Figure 19. Unfiltered phase noise extrapolated to 123-MHz offset**



# The IBIS model: A conduit into signal-integrity analysis, Part 1

**By Bonnie Baker**
*Senior Applications Engineer*

Texas Instruments (TI) is developing a new arsenal of digital input/output buffer information specification (IBIS) simulation models to meet a variety of customer needs. This style of model (Figure 1) might be used in a simulation environment to help solve board-level overshoot, undershoot, or crosstalk problems, to name a few. On a more fundamental level, IBIS models provide useful product information, such as the pin capacitance and parasitics or the rise/fall times of the digital output buffers.

This article, Part 1 of a three-part series, shows the fundamental elements of IBIS models and how they are generated in the SPICE environment. Part 2 will investigate IBIS-model validation. Part 3 will show how IBIS users investigate signal-integrity issues and problems during the development phase of a printed circuit board (PCB).

As Figure 1 shows, the IBIS model contains the package parasitics and the silicon input capacitance (C_comp) for all pins. The IBIS model also includes tables of data that represent the product's DC operation within the product's operating range and beyond the power supplies (power-clamp, ground-clamp, pullup, and pulldown boxes). In addition, the output-model structure in Figure 1 provides tables that represent the AC or transient response (rising ramp and falling ramp) within the operating range of the product.

An IBIS model includes AC and DC tables that reflect the operation of the product. This type of model has pin- and package-parasitics elements that complete the interface to the PCB. The simulation model produces the performance of the digital buffer's interaction with the PCB but omits interactions with nodes inside the chip. The IBIS model simulates the system-level PCB behavior, specifically modeling the connection from the outside world to the product's digital input/output (I/O) buffers.

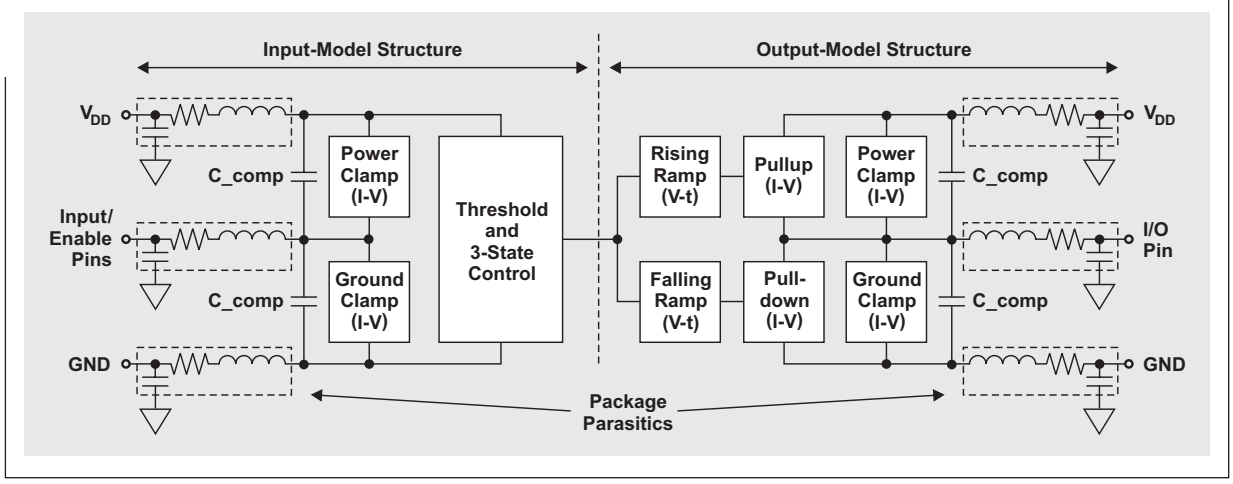
## Foundations of the IBIS model

An IBIS model contains information relating to the digital buffers of an IC chip. The core of the IBIS model contains the product buffer's DC information in the form of current-voltage (I-V) tables, and its AC information in the form of voltage-time (V-t) tables. If these tables are generated with the product's SPICE deck, it is possible to include nominal, strong, and weak corners with variations in process, supply voltage, and temperature. Table 1 shows an example of six corners for the DAC8812, which is a dual serial-input, 16-bit multiplying digital-to-analog converter. Three of these corners (1, 2, and 3) are centered around a nominal digital power-supply voltage ($V_{DD}$) of 3.3 V. The other

**Table 1. Process, voltage, and temperature corners for DAC8812 IBIS model**

| CORNER NUMBER | PROCESS | VOLTAGE (V) | TEMPERATURE (°C) |
|---|---|---|---|
| 1 | Weak | 3.0 | 85 |
| 2 | Nominal | 3.3 | 25 |
| 3 | Strong | 3.6 | –40 |
| 4 | Weak | 4.5 | 85 |
| 5 | Nominal | 5.0 | 25 |
| 6 | Strong | 5.5 | –40 |

**Figure 1. Block diagram of IBIS model with digital I/O buffers**



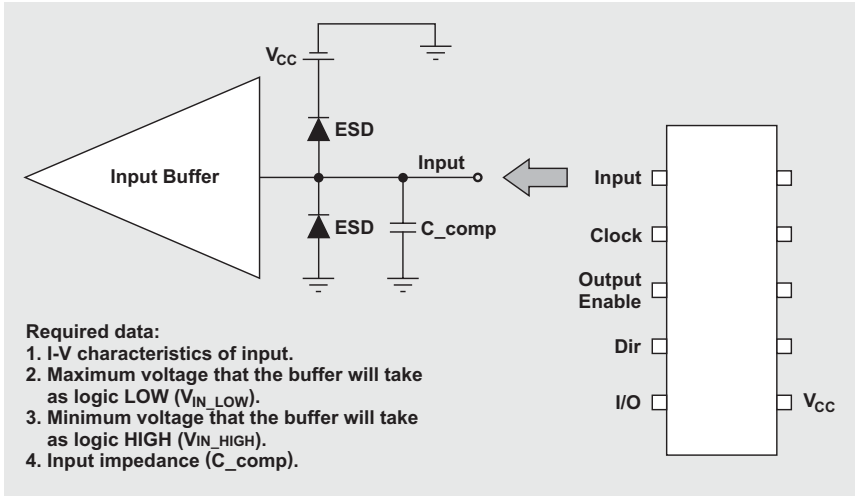
three corners (4, 5, and 6) are centered around a nominal $V_{DD}$ of 5.0 V.

An IBIS model created at the bench is limited to the tests from one to a few devices. The bench-tested IBIS models usually do not show silicon-process variations.

IBIS models can contain data for any of several different buffer types: input, output, I/O, tri-state, terminator, output_open_source, output_open_sink, I/O_open_source, I/O_open_sink, input_ECL, output_ECL, and I/O_ECL.

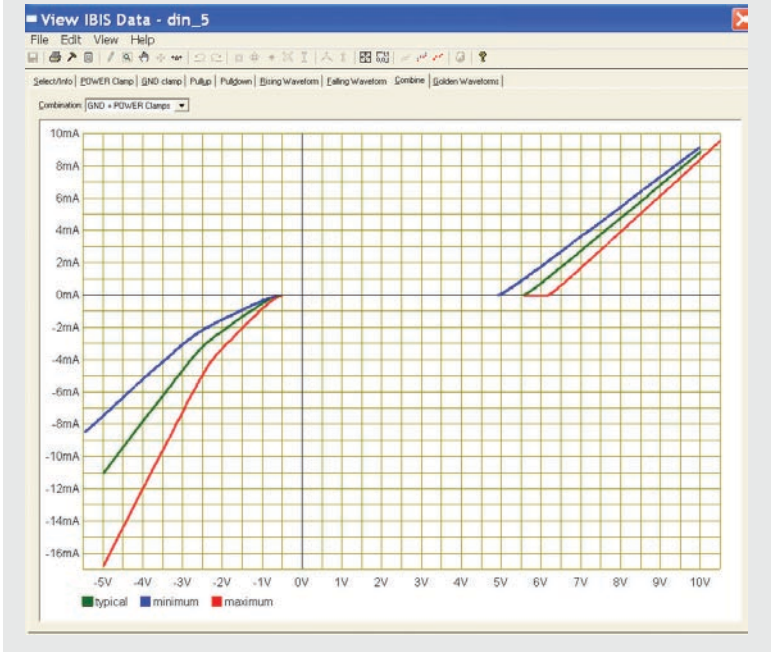
The voltage at an input or output buffer's pin in the DC tables extends beyond the supply voltage ($V_{DD}$) from $-V_{DD}$ to $2 \times V_{DD}$. This exercises the product buffer's ESD structures beyond the supply voltage. In this manner, IBIS models are capable of showing the overshoot and undershoot responses of poorly terminated PCB signals. IBIS models contain I-V data for input and output buffers.

**Figure 2. Example of input buffer's basic functionality for an IBIS model**




The example of an input buffer in Figure 2 shows the input buffer, the ESD cells, and the buffer's capacitance (C_comp). An IBIS model for an input buffer provides I-V tables of data that extend beyond ground and the supply voltage ($V_{DD}$). Note that the IBIS model does not require circuitry beyond the immediate interface. IBIS models do not reflect the product's interior logic and interactions. Figure 3 shows a composite graphical example of an input buffer's power-clamp and ground-clamp I-V tables from an IBIS model.

**Figure 3. Graphical representation of IBIS model's I-V tables**



V-t tables represent the AC behavior of an output buffer like the one in Figure 4. With V-t tables, the output buffer's pin remains inside the product's power-supply rails. IBIS models are capable of simulating the buffer within its operating range, exhibiting accurate simulations of rise and fall times.

Figure 4 shows the pullup and pulldown circuitry as well as the input capacitance of a two-state output buffer. With the output buffer, an IBIS model will typically have I-V tables as well as V-t tables. Once again, the IBIS model does not require circuitry beyond the immediate interface because the model does not reflect the product's interior logic and interactions. Figure 5 shows a graphical example of the rising-time waveform from an IBIS model's V-t table.

**Figure 4. Example of two-state output buffer's basic functionality for an IBIS model**

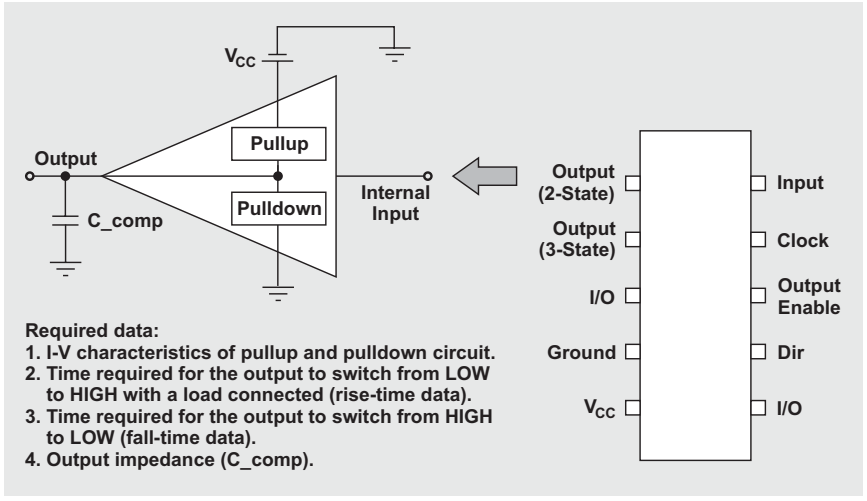
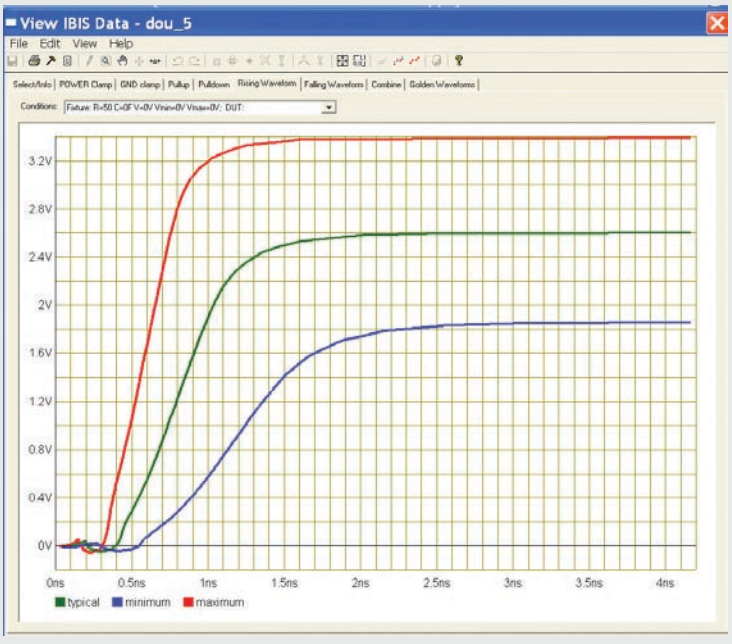



**Figure 5. Graphical representation of rising time from IBIS model's V-t table**



## Format of IBIS model

The format of the IBIS model starts with a header, which is generated by hand and includes a description of the relevant IC or ICs. Following the IC description is general information about the model, including origination date, model source, and user notes. Figure 6 shows an example header of an IBIS model for TI's TMP512 and TMP513, which are temperature and supply-system monitors with an SMBus interface. The "Notes" section is the most important portion of the IBIS model header, where details of the model creation are found along with the basic format of the digital buffers.

The model header is followed by detailed information about the package(s) for the product(s), including values for pin resistance, inductance, and capacitance. To find the total capacitance for a specific pin, the capacitance values in this section are combined with the capacitance (C_comp) values called out next in the buffer tables. The core of the IBIS model follows with I-V and V-t tables buffer by buffer.

## Extracting single-ended SPICE buffer data

The last section of this article will explain how to obtain the I-V and switching information (V-t) from a buffer's transistor-level model. An automated simulation template, an extraction tool (such as S2IBIS3), or manual simulations can be used. This discussion will include only totem-pole CMOS structures.

### Extracting I-V data from SPICE simulations

To extract the I-V data for an IBIS model from a SPICE input buffer, the buffer pad is connected to an independent voltage source ($V_{SOURCE}$). Once the buffer's input is set to its desired state (LOW, HIGH, or OFF), $V_{SOURCE}$ is exercised with a DC-analysis function over the sweep range of $-V_{SWEEP}$ to $2 \times V_{SWEEP}$, where the $V_{SWEEP}$ limit is set by the product's supply voltage ($V_{DD}$). For instance, if the buffer is powered by a 5-V supply, the range of $V_{SWEEP}$ will be –5 V to 10 V. While performing this sweep, the simulator records the current that goes into the buffer.

If the buffer is configured in a high-impedance state (OFF), the data collected produces the ground-clamp and power-clamp tables. The data in the ground-clamp table is referenced to ground, and the data in the power-clamp table is referenced to $V_{DD}$.

Extracting the I-V data for an output buffer's IBIS model results in a pulldown table and a pullup table. Data for the pulldown table is collected while the buffer is in an output LOW state. Data for the pullup table is collected while the buffer is in an output HIGH state. Data in the pulldown table is referenced to ground, and data in the pullup table is referenced to $V_{DD}$.

**Figure 6. IBIS model header for TMP512 and TMP513**

```
|*************************************************************************************
|Texas Instruments Incorporated
|Temperature and Supply System Monitors  SMBus interface
|
| Marketing part#      Digital Voltage   Analog Voltage   Package   # Pins
|                        Range             Range           Type
|TMP512AIDG4           2.1V to 3.6V      3.0V to 26V     SO-14       14
|TMP512AIDRG4          2.1V to 3.6V      3.0V to 26V     SO-14       14
|
|TMP513AIDG4           2.1V to 3.6V      3.0V to 26V     SO-16       16
|TMP513AIDRG4          2.1V to 3.6V      3.0V to 26V     SO-16       16
|TMP513AIRSATG4        2.1V to 3.6V      3.0V to 26V     QFN-16      16
|TMP513AIRSARG4        2.1V to 3.6V      3.0V to 26V     QFN-16      16
|*************************************************************************************
[IBIS Ver]      4.0
[File name]     tmp512_3.ibs
[File Rev]      1.0
[Date]          04/14/2010
[Source]        Texas Instruments Incorporated.
                Analog-eLab , HPA
                12500 TI Blvd
                Dallas, TX -75243
                For Support e-mail: elab_ibis@list.ti.com

[Notes]         Revision History:
                1.0: 04/14/2010
              - Initial version of the model
              - Initial Model generated from simulations in TISPICED
              - Model not matched to measurements
              - Non-monotnic warnings - combined  pulldown and pullup data
                The GPIO non-monotonic current delta is less than 1 mA in a
                full-scale range of ~95 mA. Given these conditions, these
                warnings are deemed insignificant.
                1.1: 04/18/2010 corrected spelling errors
|
[Disclaimer]
|
This product is designed as an aid for customers of Texas Instruments.
No warranties, either expressed or implied, with respect to this third
party software (if any) or with respect to its fitness for any
particular purpose is claimed by Texas Instruments or the author. The
software (if any) is provided solely on an "as is" basis. The entire
risk as to its quality and performance is with the customer
|
[Copyright] (C) Copyright 2009 Texas Instruments Incorporated.
            All rights reserved.
```

### Extracting V-t data from SPICE simulations

When a CMOS buffer is modeled, the required simulations that relate to the ramp rate and V-t tables are straightforward. For each simulation corner (typical, minimum, and maximum), there are four V-t data sets. Data for two of the waveforms is gathered by switching the buffer output from LOW to HIGH with the load referenced to a low voltage. Data for the other two waveforms is collected with a load referenced to $V_{DD}$. For the latter two curves, the buffer's output switches from HIGH to LOW. From these simulations, the ramp rate or dV/dt ratio is extracted as the device is switching HIGH against a low-voltage reference and switching LOW against a high-voltage reference.

## Required and recommended IBIS-model curves

There is a variety of buffer types that the IBIS standard describes with I-V and V-t tables. Tables 2 and 3 from Reference 1 list the required and recommended buffer data for each type of buffer.

## Conclusion

An IBIS model assists PCB designers during their evaluations of signal-integrity issues and problems. The model's silicon-based DC and AC data facilitates the evaluation of over-power-supply behavior as well as rise- and fall-time behavior. In Part 2, the validity of the IBIS model will be evaluated by verifying that it meets IBIS standards and by comparing it to SPICE simulations.

## References

1. The IBIS Open Forum. (2005, Sept. 15). *IBIS Modeling Cookbook for IBIS Version 4.0* [Online]. Available: www.eda.org/ibis/cookbook/cookbook-v4.pdf
2. Roy Leventhal and Lynne Green, *Semiconductor Modeling for Simulating Signal, Power, and Electromagnetic Integrity.* New York: Springer Science+Business Media, LLC, 2006.

## Related Web sites

**dataconverter.ti.com**
**www.ti.com/sc/device/DAC8812**
**www.ti.com/sc/device/TMP512**
**www.ti.com/sc/device/ TMP513**

**Table 2. Required and recommended I-V data versus IBIS buffer types**

| Model_type | [Pullup] | [Pulldown] | [POWER Clamp] | [GND Clamp] | Notes |
|---|---|---|---|---|---|
| Input | n/a | n/a | Recommended | Recommended | |
| I/O | Required | Required | Recommended | Recommended | |
| I/O_open_sink<br>I/O_open_drain | n/a | Required | Recommended | Recommended | 1 |
| I/O_open_source | Required | n/a | Recommended | Recommended | 1 |
| Open_sink<br>Open_drain | n/a | Required | Recommended | Recommended | 4 |
| Open_source | Required | n/a | Recommended | Recommended | 4 |
| Output | Required | Required | Recommended | Recommended | 4 |
| 3-state | Required | Required | Recommended | Recommended | 2 |
| Series_switch | n/a | n/a | n/a | n/a | 3 |
| Series | n/a | n/a | n/a | n/a | 3 |
| Terminator | n/a | n/a | Recommended | Recommended | 3 |
| Input_ECL | n/a | n/a | Recommended | Recommended | |
| I/O_ECL | Required | Required | Recommended | Recommended | 2 |
| Output_ECL | Required | Required | Recommended | Recommended | 4 |
| 3-state_ECL | Required | Required | Recommended | Recommended | 2 |

*1. Keywords listing "n/a" may be included if the currents are set to 0 for all voltage points*
*2. Functionally similar to I/O, but without input threshold information (Vinh, Vinl, etc.)*
*3. Special syntax required; use of clamp data on pins that also feature buffers using these Model_types is allowed*
*4. Clamp data may technically be excluded; however, this data aids analysis of reflections arriving at the driving buffer*

**Table 3. Required and recommended V-t data versus IBIS buffer types**

| | [Rising Waveform] | | [Falling Waveform] | | |
|---|---|---|---|---|---|
| Model_type | Load to Vcc | Load to GND | Load to Vcc | Load to GND | Notes |
| Input | n/a | n/a | n/a | n/a | |
| I/O | Recommended | Recommended | Recommended | Recommended | |
| I/O_open_drain | Recommended | n/a | Recommended | n/a | 1 |
| I/O_open_source | n/a | Recommended | n/a | Recommended | 1 |
| I/O_open_sink<br>I/O_open_drain | Recommended | n/a | Recommended | n/a | 1 |
| Open_source | n/a | Recommended | n/a | Recommended | |
| Open_sink<br>Open_drain | Recommended | n/a | Recommended | n/a | |
| 3-state | Recommended | Recommended | Recommended | Recommended | |
| Series_switch | n/a | n/a | n/a | n/a | 2 |
| Series | n/a | n/a | n/a | n/a | 2 |
| Output | Recommended | Recommended | Recommended | Recommended | |
| Terminator | n/a | n/a | n/a | n/a | |
| Input_ECL | n/a | n/a | n/a | n/a | |
| I/O_ECL | Recommended (to Vcc – 2) | | Recommended (to Vcc – 2) | | 3 |
| Output_ECL | Recommended (to Vcc – 2) | | Recommended (to Vcc – 2) | | 3 |
| 3-state_ECL | Recommended (to Vcc – 2) | | Recommended (to Vcc – 2) | | 3 |

*1. The presence of internal terminations may require adding waveforms in place of "n/a"*
*2. Special syntax required*
*3. For ECL, the fixture is Vcc-2; multiple waveforms to various voltages using the same load impedance may be useful in some contexts*

Tables 2 and 3 from Reference 1 reproduced with permission of the IBIS Open Forum and TechAmerica.

# A low-cost, non-isolated AC/DC buck converter with no transformer

**By Jeff Falin,** *Senior Applications Engineer,*
**and Dave Parks,** *Senior Member, Technical Staff*

## Introduction

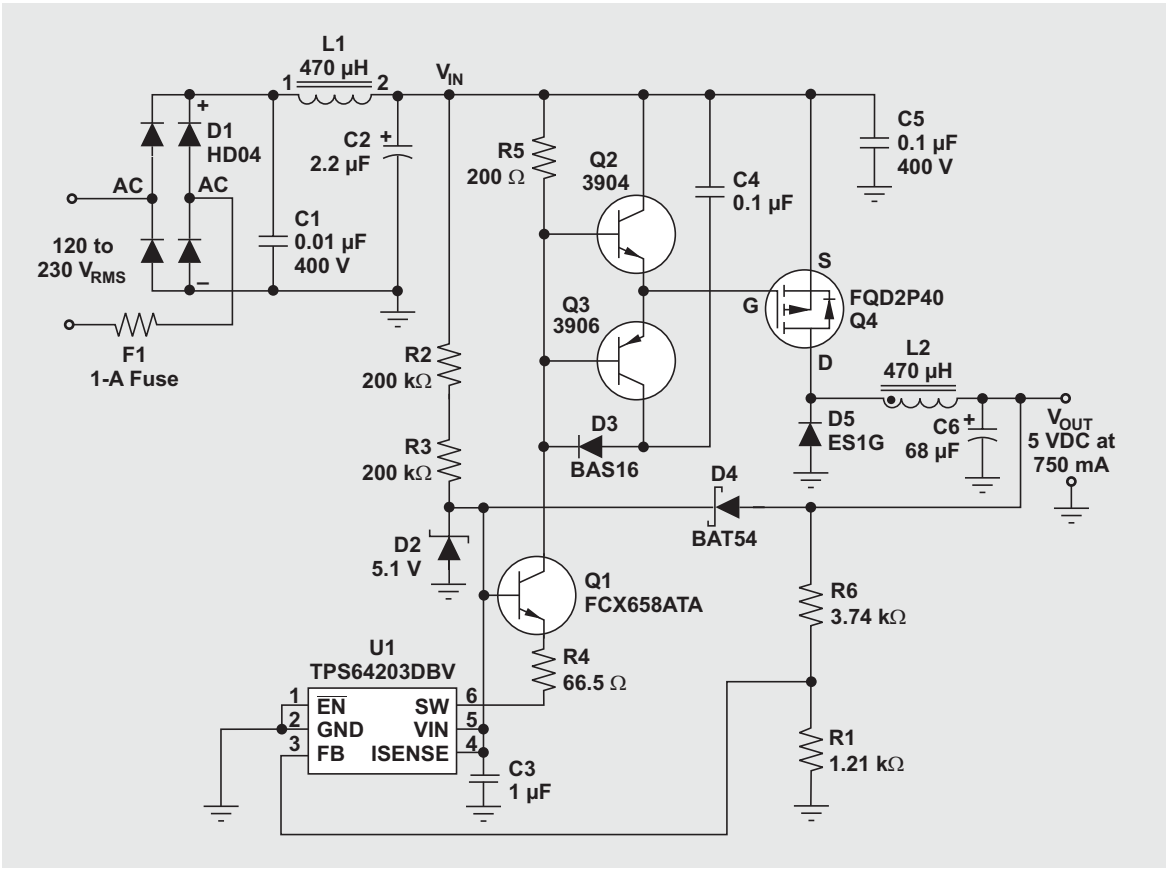
Off-line equipment such as a smart meter or a power monitor has electronics that require non-isolated DC power under 10 W. Until recently, the only practical options for providing a low-power DC power rail from an AC source were to use an extremely inefficient, unregulated resistive/capacitive divider following the rectifier, or a flyback DC/DC converter that was cumbersome to design. Advances in MOSFET technology and an innovative gate-drive circuit for a hysteretic buck controller have resulted in an ultra-low-cost DC power rail.

Figure 1 shows the entire converter. The rectifier circuit uses a standard, fast-switching rectifier diode bridge (D1) and an LC filter (L1 and C2). The remaining components will be explained in more detail.

## The basic buck converter

The TPS64203 is a hysteretic buck controller designed to drive a high-side pFET and has minimum turn-on and minimum turn-off switching-time requirements. Unlike a traditional hysteretic converter with a switching frequency that varies with load current, the minimum on and off times essentially clamp the switching frequency when the converter begins to run in continuous-conduction mode at high output-power levels. Other members of the TPS6420x family actively avoid switching in the audible frequency range, effectively having a maximum on and off time. Originally designed for battery-powered applications, the TPS6420x family has an input-voltage range of 1.8 V to 6.5 V and very low quiescent current (35 µA maximum). During start-up, the TPS64203 is biased by Zener diode

**Figure 1. AC/DC buck-converter circuit**



D2 and high-voltage resistors R2 and R3. After the 5-V rail is up, Schottky diode D4 allows the 5-V output rail to power the controller.

Power FET Q4 must have a high enough $V_{DS}$ voltage rating not to be damaged by the input voltage, and a high enough current rating to handle $I_{PMOS(RMS)} = I_{OUT(max)} \times \sqrt{D_{max}}$. It must also be in a package capable of dissipating $P_{Cond} = (I_{OUT(max)} \times \sqrt{D_{max}})^2 \times R_{DS(on)}$. Traditionally, high-voltage p-channel FETs have had a gate capacitance or turn-on/off times that were too large, a drain-to-source resistance ($R_{DS(on)}$) that was too high, a threshold voltage ($V_{TH}$) that was too large, and/or have simply been too expensive to make a circuit like the one in Figure 1 practical (i.e., efficient enough relative to cost). Since the high line of 230 $V_{RMS}$ + 10% tolerance comes from the 350-$V_{PK}$ AC line, the FET, filter, and input capacitors need to be rated for 400 V.

The FQD2P40 is a relatively new, 400-V p-channel MOSFET. With an $R_{DS(on)}$ of 5.0 Ω from a 10-V gate drive and a total gate charge of less than 13 nC, this FET can easily be switched by the controller—with relatively fewer conductive and switching losses than older FETs—with the help of the innovative drive circuit consisting of Q2, Q3, C4, and D3. The converter's rectifying Schottky diode, D5, is selected with a voltage rating capable of blocking the input voltage, a peak-current rating slightly higher than the output voltage, and an average current rating of $I_{Diode(Avg)} = (1 - D) \times I_{OUT(max)}$. With a $D_{max}$ of 5 V/120 V = 0.04 and such low output power, the peak-current rating and the power dissipation are not a concern in either switch.

The buck power stage's LC filter is designed as explained in the TPS6420x family data sheet. With the input voltage being much larger than the output voltage, all of the TPS6420x controllers will run in minimum-on-time mode. Equation 1 computes the recommended buck-converter inductance at high line, assuming that K = 0.4 for the inductor's ripple-current factor.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{on(min)}}{\Delta I_L} = \frac{(230\ V - 5\ V) \times 0.65\ \mu s}{0.4 \times 0.750\ A} \quad (1)$$

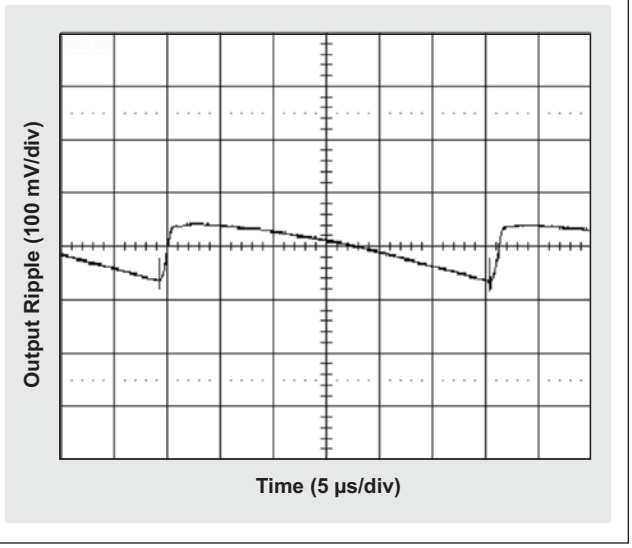
$$= 488\ \mu H \rightarrow 470\ \mu H$$

The relatively high K value minimizes inductor size and proves to be acceptable because the steady-state output-ripple requirement for this particular application was no larger than 0.02 × $V_{OUT}$, or 100 $mV_{PP}$ at high load. Being hysteretic, the TPS6420x controllers typically work best with some ripple on the output voltage. An output capacitor with at least 50-mΩ ESR is recommended and would produce a ripple voltage of $\Delta V_{PP(ESR)} = \Delta I_L \times R_{ESR}$, which typically far exceeds the capacitive component of the voltage ripple. The measured ripple for this application is shown in Figure 2.

Because the TPS64203 is hysteretic, its output voltage will have higher ripple at lower output power when it is running in pulsed-frequency mode. The measured operating frequency of the converter is approximately 32 kHz, which agrees with the predicted value of

$$f_{SW} = \frac{D_{min}}{t_{on(min)}} = \frac{5\ V/250\ V}{0.65\ \mu s} = 31\ kHz.$$

**Figure 2. Output ripple at $V_{IN}$ = 250 VDC and $I_{OUT}$ = 500 mA**




## How the drive circuit works

Bipolar transistor Q1 and resistors R4 and R5 form a constant-current-driven level shifter that allows the low-voltage TPS64203 controller to operate the discrete gate-drive circuit formed by Q2 and Q3. Like the controller, the level shifter is powered by Zener diode D2 at start-up and the regulated 5-V rail, through Schottky diode D4, after start-up. Power FET Q4's gate must be overdriven just enough to provide the required output current with an acceptable $R_{DS(on)}$. Too much drive increases switching losses, while too little increases conduction losses. From a review of the FQD2P40 data sheet and some trial and error, $V_{GS} \cong 12$ V was selected.

Capacitor C4 and diode D3 are critical to the drive circuit's functionality. Resistor R5 is selected to set the gate-drive level of 12 V below the voltage at the rectifier's output. Diode D3 clamps capacitor C4 to this level. Specifically, when U1's switch pin outputs a low signal to turn on the power FET, the signal gets level shifted to the base of Q3. Transistor Q3 turns on and quickly charges Q4's gate-to-source capacitance, $C_{GS}$, to 12 V. Without C4 and D3, turning off Q4 would have required Q3 to be an expensive, high-voltage bipolar transistor with its drain tied to ground. When U1's switch pin outputs a high signal to turn off the power FET, the signal gets level shifted to the base of Q2. Q2 turns on, effectively tying Q4's gate to the input voltage. It is important to note that without capacitor C4 acting as a local power supply, transistors Q2 and Q3 would not be able to provide the fast current spikes necessary to quickly —and therefore efficiently—pull up or pull down Q4's gate

capacitance. Also, the level shifter's current, $I_{LS}$, set by R4, must be high enough to move Q4's gate charge, $Q_{Gate}$, during the $t_{on(min)}$. That is,

$$\frac{I_{LS} = V_{Z(D4)} - V_{BE}}{R4} >> \frac{Q_{Gate}}{t_{on(min)}}.$$

Capacitor C4 is sized to be much larger than Q4's gate capacitance, but it must be small enough that it can be recharged during the shorter of the controller's minimum on and off times. Figure 3 shows the gate and drain turn-on/off times during one switching cycle with an input voltage of 300 V and a 500-mA load. Measured conversion efficiency is shown in Table 1.

## Current limit and soft start

In low-voltage applications, the TPS6420x uses a high-side current-limit circuit to compare the drop across a current-sense resistor, placed between the VIN and ISENSE pins, to a reference voltage. If the voltage across the sense resistor exceeds that voltage, the circuit turns off the switch, thereby implementing a pulse-by-pulse current limit. In a high-voltage application, the current-limit circuit cannot be used without overvoltage on the ISENSE pin, so the ISENSE pin is tied high to VIN. Therefore, the circuit in Figure 1 does not have a current limit. A high-side series fuse is recommended to provide short-circuit protection.

In typical applications during start-up, the TPS64203's current-limit value is slowly ramped up to provide a current-limited, controlled soft start. In this application, the current-limit circuit and therefore the soft start are disabled; therefore, the start-up inrush current may be large and the output voltage may overshoot slightly, as shown in Figure 4.

## Conclusion

Using a level shifter and gate driver with a localized power source allows the use of a low-voltage buck controller to provide a DC voltage from an AC power source. Conversion efficiency near 60% can be achieved by using a simple circuit and no transformer. This circuit can also be used for DC/DC conversion where the input DC voltage is above the maximum rating of the TPS6420x.

## Related Web sites

**power.ti.com**
**www.ti.com/sc/device/TPS64200**

**Figure 3. Q4 gate and drain voltages during one switching cycle**

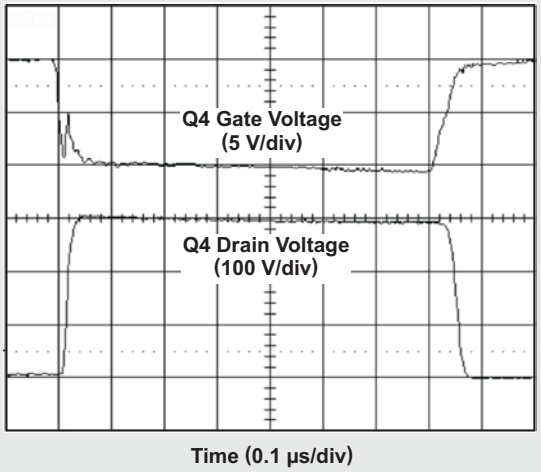
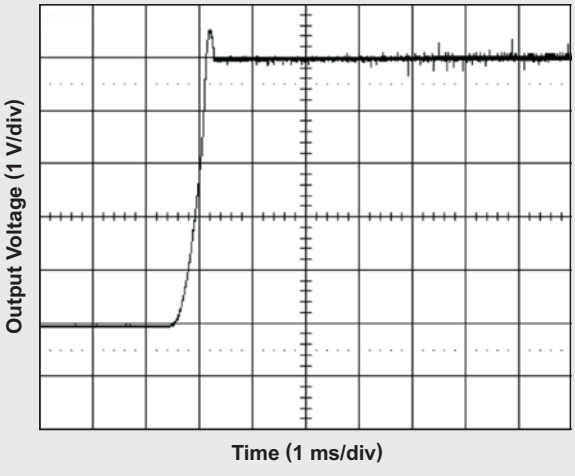



**Table 1. Measured conversion efficiency**

| $V_{IN}$ (V) | $I_{IN}$ (A) | $P_{IN}$ (W) | $I_{OUT}$ (A) | $V_{OUT}$ (V) | $P_{OUT}$ (W) | EFFICIENCY (%) |
|---|---|---|---|---|---|---|
| 100 | 0.043 | 4.3 | 0.5 | 5.023 | 2.5115 | 58.40698 |
| 200 | 0.021 | 4.2 | 0.5 | 5.023 | 2.5115 | 59.79762 |
| 300 | 0.015 | 4.5 | 0.5 | 5.023 | 2.5115 | 55.81111 |
| 100 | 0.066 | 6.6 | 0.75 | 5.023 | 3.76725 | 57.07955 |
| 200 | 0.031 | 6.2 | 0.75 | 5.023 | 3.76725 | 60.7621 |
| 300 | 0.022 | 6.6 | 0.75 | 5.023 | 3.76725 | 57.07955 |

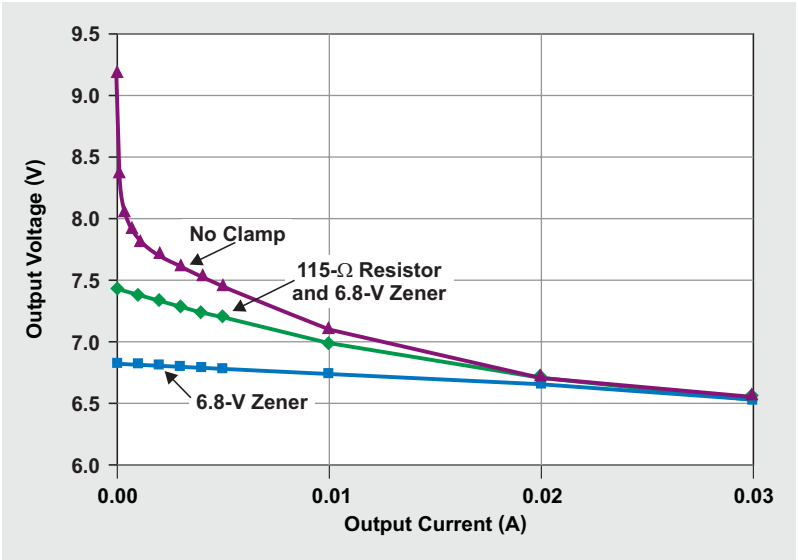
**Figure 4. Start-up into a 10-Ω load with $V_{IN}$ = 300 V**



# Save power with a soft Zener clamp

**By John Betten**
*Applications Engineer and*
*Senior Member, Technical Staff*

**Figure 1. Zener diode with resistor provides soft clamp for no-load output voltage**




Flyback converters are wildly popular due to their low cost, their isolation, and the ease with which additional output voltages can be implemented. For multiple-output flybacks, one output voltage—typically the highest-power output—is tightly regulated by means of feedback to the control circuit. Additional outputs are usually added by tightly coupling transformer windings to the main regulated winding. Linear regulators or DC/DC switchers may be added, or the outputs can be left unregulated. This last option is the most efficient, but many times voltage regulation suffers when the outputs are heavily or lightly loaded while the main output voltage has the opposite load level. This cross-regulation problem is highly dependent on the transformer leakage and winding structure, as well as on other parasitic circuit components. One of the worst scenarios is when the main output is heavily loaded and the unregulated winding is completely unloaded. Any voltage ringing present on the transformer's secondary winding is often peak-detected by the output rectifier, causing the unregulated output voltage to greatly increase. It is not uncommon for the output voltage to rise to twice its nominal voltage in this situation. This can be catastrophic to any downstream load that cannot tolerate a higher voltage or that does not present minimal loading at all times to dissipate the leakage energy.

Several solutions can remedy this no-load overvoltage condition. The simplest solution would be to add a preload to the unregulated output in the form of a resistor. This will load the output enough to dissipate the leakage energy and to lower the output voltage to an acceptable level. Unfortunately, this load will always be present and causes a loss of efficiency that is often considered unacceptable.

A second option is to simply add a Zener diode to the unregulated output. The diode's voltage rating must be set higher than the nominal output voltage after the typical 5% or 10% part tolerance is included. This means the diode won't conduct or dissipate power until the output voltage rises high enough. While this may seem like an ideal solution, several potential problems exist. Once the Zener diode conducts, its impedance drops significantly and provides little resistance to current flow. The current flow into the diode, and hence the power dissipated in it, is determined by parasitic circuit components and thus is hard to control. Higher-power converters can potentially source a large current and easily destroy a Zener diode. For this reason, it is risky to add a small Zener diode and difficult to calculate the power dissipated.

Another option is to use a snubber to dissipate the leakage energy. This generally dissipates more power than using a preload resistor and does not always provide as much no-load voltage reduction on the output.

A soft Zener clamp, which consists of a resistor in series with a Zener diode, can provide a good compromise. It can clamp the unregulated output voltage to a level that is lower than that of the unclamped output voltage but higher than that of a Zener diode alone. To determine the resistor's value, the output can be loaded with just enough current to reduce the high output voltage to the desired safe level. Figure 1 shows an example where the desired no-load output voltage is 7.4 V. The series resistor's value can be calculated by subtracting the Zener diode's nominal voltage from this voltage and dividing the result by the preload current. The benefit of this circuit is that it does not dissipate power at loads that would typically be seen in operation. Under extreme cross-load conditions, this circuit clamps the "runaway" output voltage to a much more predictable level.

## Related Web site

**power.ti.com**

# Interfacing high-voltage applications to low-power controllers

**By Thomas Kugelstadt**
*Senior Applications Engineer*

A common requirement of industrial applications is to interface high-voltage potentials, such as signal outputs of sensor switches and AC rectifiers, to the peripheral input ports of low-voltage microcontrollers (MCUs) and digital signal processors. A new generation of interface circuits providing this function are digital-input serializer (DIS) devices. They can sense digital input voltages ranging from as low as 6 VDC up to 300 VDC and convert them into 5-V serial data streams while consuming almost 80% less power than a discrete design. This capability makes DIS devices the most power- and cost-efficient solution in industrial interface applications.

This article explains the functional principle of a DIS and its configuration in a typical industrial interface design.

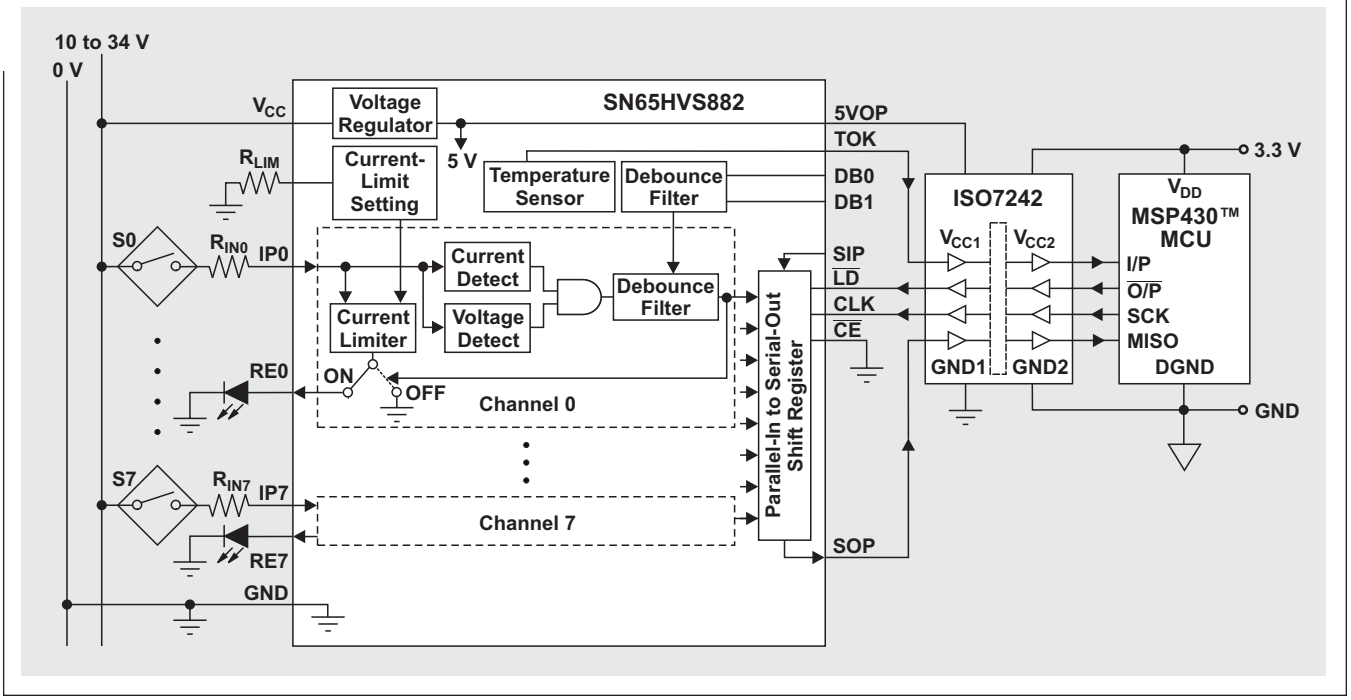
## Functional principle

Understanding the operational principle of a DIS is faster accomplished by seeing the device in the context of an entire interface design as shown in Figure 1. A high-voltage supply in the range of 10 to 34 V supplies the sensor switches, S0 to S7, and the DIS. The ON/OFF status of each sensor switch is detected by the eight parallel field inputs of the device, then internally processed and made available to the low-voltage inputs of a parallel-in, serial-out shift register. An MCU provides the necessary control signal to the serial interface of the DIS via a digital isolator. Firstly, a load pulse at the $\overline{LD}$ input latches the switch's status information into the shift. Then a clock signal applied to the CLK input serially shifts the register content out of the DIS into a controller register via the isolator.

S0 to S7 comprise a wide range of sensor switches, such as proximity switches, relay contacts, limit switches, push buttons, and many more. While the input resistors, $R_{IN0}$ to $R_{IN7}$, are optional, they can serve two purposes when implemented. One is that in high-voltage applications, some industrial standards might require input resistors as a safety precaution to prevent fire hazards in the event of an input short circuit. The other purpose is to raise the ON/OFF threshold voltage of a sensor switch.

Internally, each input signal is checked for signal strength and stability. A current comparator detects whether the input current is higher than a predefined leakage threshold, and a voltage comparator checks whether the input voltage is higher than an internally

**Figure 1. Stand-alone digital-input system**



fixed reference voltage. If both comparator outputs are logic high, a programmable debounce filter checks whether the new input status is caused by a short but strong noise transient, or whether the signal presence outlasts the debounce time and thus presents a true input signal.

For a true input signal, the filter output presents the corresponding logic level to the parallel inputs of the shift register and also switches the output of the internal current limiter accordingly. For an OFF condition (when the switch is open), the filter output is low, and the output of the current limiter is switched to ground. For an ON condition, the filter output is high, and the output of the current limiter is connected to a signal-return output (RE). Connecting a light-emitting diode (LED) to an RE output allows for the visible indication of a switch's status.

## Input configuration

To configure a DIS for various applications, the current and voltage capability of its input, IPx, must be known, as well as its switching thresholds. For that purpose, Figure 2 shows a more detailed block diagram of a channel's input stage. During a sensor switch's OFF-to-ON transition, the two parameters of interest are the positive-going voltage threshold at a device input, $V_{IP\text{-}ON}$, and its selected current limit, $I_{IN\text{-}LIM}$.

While $V_{IP\text{-}ON}$ is internally fixed at 5.2 V, $I_{IN\text{-}LIM}$ can be adjusted via an external precision resistor, $R_{LIM}$. Note that setting the current limit affects all device inputs equally. $I_{IN\text{-}LIM}$ is derived from a reference current, $I_{REF}$, via a current mirror, making $I_{IN\text{-}LIM} = 72 \times I_{REF}$. $I_{REF}$ is determined by the ratio of an internal bandgap reference to the resistor value, $R_{LIM}$ ($I_{REF} = V_{REF}/R_{LIM}$). The current limit can therefore be expressed as a function of $R_{LIM}$:

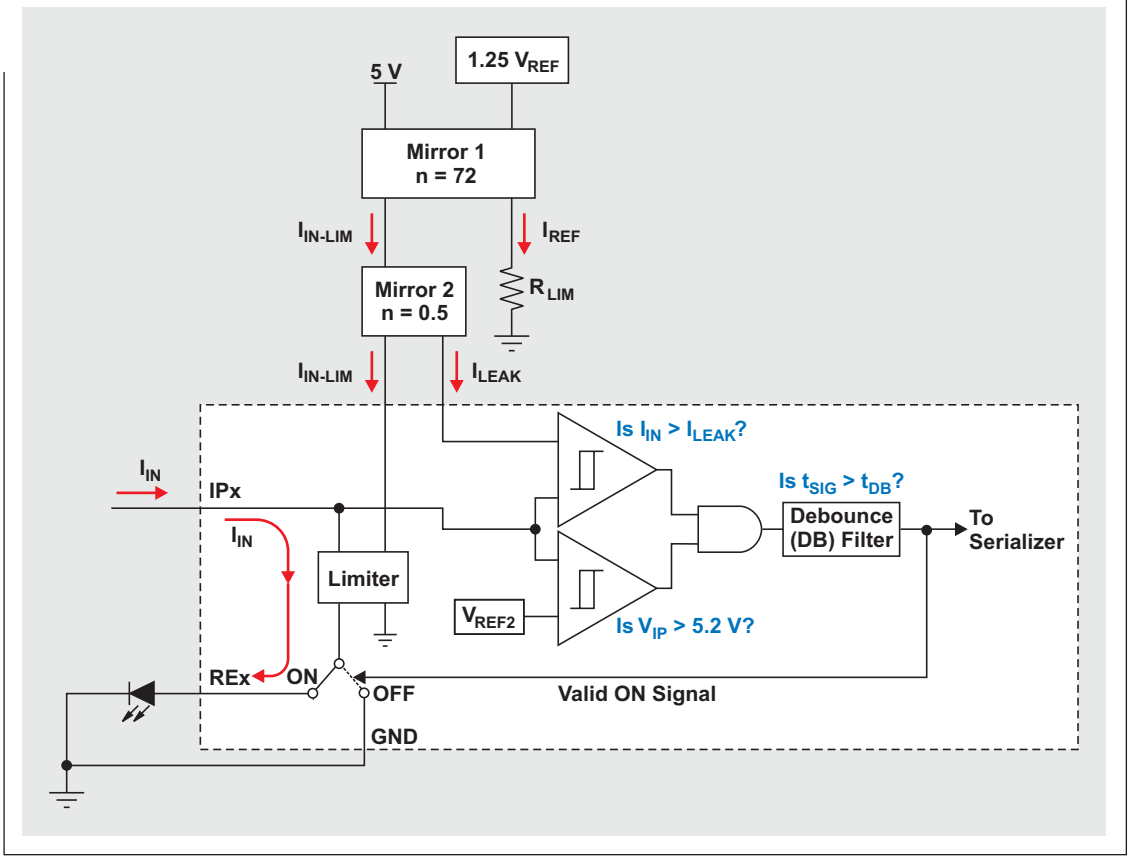
$$I_{IN\text{-}LIM} = 72 \times \frac{1.25\ V}{R_{LIM}} = \frac{90\ V}{R_{LIM}} \quad (1)$$

Solving for $R_{LIM}$ then provides the required resistor value for a desired current limit:

$$R_{LIM} = \frac{90\ V}{I_{IN\text{-}LIM}} \quad (2)$$

For low-voltage applications using a 12-V supply, setting the current limit via $R_{LIM}$ might be the only calculation required. Because the device inputs can tolerate voltages of up to 34 V, switching the 12-V supply directly to a digital

**Figure 2. Simplified block diagram of a single-channel input stage**



input causes no damage to the device. With $V_{IP-ON}$ = 5.2 V, the ON threshold lies almost in the middle of the 12-V input-voltage range. Figure 3 shows the schematic of this simple circuit design. With the low-current LED indicator requiring a forward current of $I_{IN-LIM}$ = 2 mA, $R_{LIM}$ is determined via Equation 2 to be 45 kΩ, with the closest 1% value being 44.8 kΩ.

However, for high-voltage designs using a supply of 24 V or more, an input resistor is needed to raise the ON threshold into the middle of the input-voltage range. Figure 4 presents this case, with the input-current limit assumed to be 2 mA. The input resistor now separates the device's input voltage, $V_{IP}$, from the field input voltage, $V_{IN}$, thus raising the actual ON threshold to $V_{IN-ON} = V_{IP-ON} + R_{IN} \times I_{IN-LIM}$. Inserting the specified 5.2-V threshold for $V_{IP-ON}$ and expressing $I_{IN-LIM}$ through Equation 1 yields $V_{IN-ON} = 5.2\ V + R_{IN} \times 90\ V/R_{LIM}$. Solving for $R_{IN}$ then provides the required input-resistor value for a desired ON threshold:

$$R_{IN} = (V_{IN-ON} - 5.2\ V) \times \frac{R_{LIM}}{90\ V} \quad (3)$$

In order to set the ON threshold in the circuit in Figure 4 to $V_{IN-ON}$ = 12 V, the input resistor is determined via Equation 3:

$$R_{IN} = (12\ V - 5.2\ V) \times \frac{44.8\ k\Omega}{90\ V} = 3.385\ k\Omega,$$

with the closest 1% value being 3.4 kΩ.

This simple design methodology can be applied to input voltages of up to 60 V. Higher voltages, however, will increase $V_{IP}$ above its specified maximum of 34 V, so a

**Figure 3. Switch ON condition: $V_{IP-ON}$ = 5.2 V, $I_{IN-LIM}$ = 90 V/$R_{LIM}$**

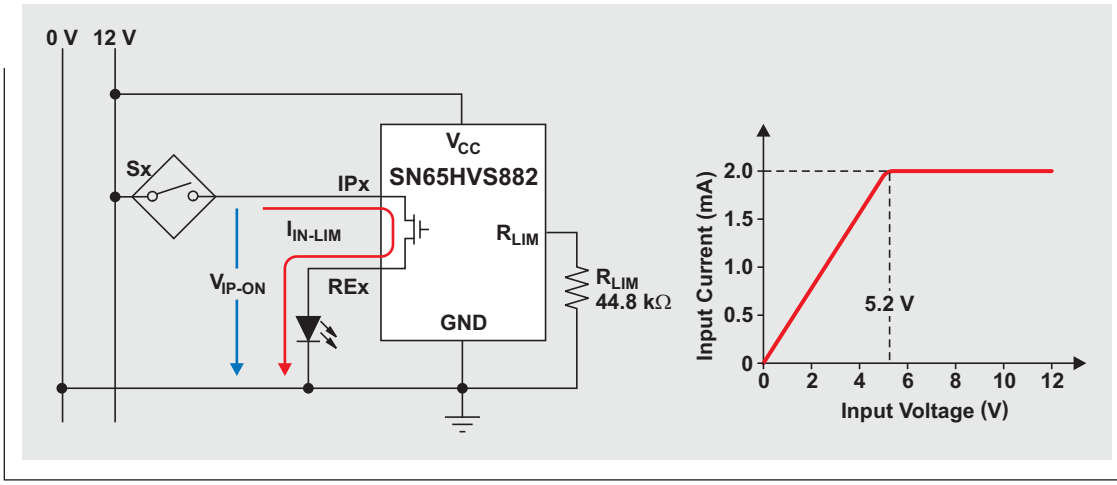
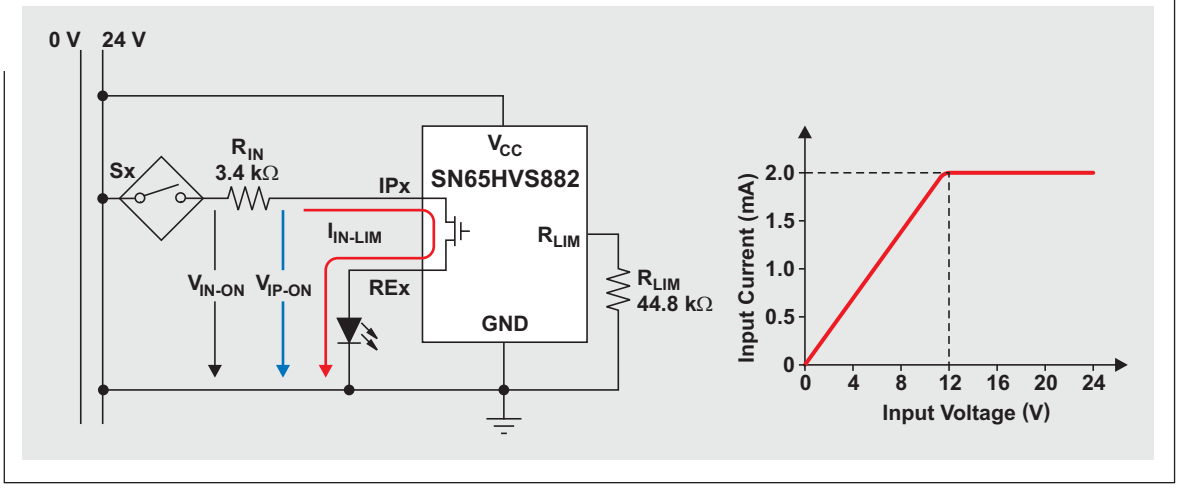



**Figure 4. Switch ON condition: $V_{IN-ON}$ = 12 V, $I_{IN-LIM}$ = 2 mA**



clamping element in the form of a Zener diode is required to prevent the device input from overvoltage stress. Figure 5 gives an example of a mains voltage detector, often used in building automation systems. Here the AC mains voltage of 240 $V_{rms}$ is rectified, thus yielding a peak input of 340 VDC. At such high voltages it is necessary to minimize the $I^2R$ losses within the input resistor. Therefore, the current limit is simply set to 0.5 mA by making $R_{LIM}$ = 90 V/0.5 mA = 180 kΩ.

The ON threshold is set to 150 V by making $R_{IN}$ = (150 V – 5.2 V) × 180 kΩ/90 V = 289.6 kΩ, with 291 kΩ as the closest 1% value. At $V_{IN-ON}$ = 150 V, $V_{IP-ON}$ = 5.2 V, and current limiting sets in. Beyond the ON threshold, $V_{IP}$ increases linearly until the Zener voltage of approximately 30 V is reached. At that moment, the Zener diode starts clamping; and the Zener current, $I_Z$, adds to the current limit ($I_{IN-LIM}$) to make up the total input current, $I_{IN}$.

## Serial interface

Reading the status information of the digital field inputs is easy and can be performed by using either shift register timing or serial peripheral interface timing.

When shift register timing is used, a short low-active pulse applied to the load input ($\overline{LD}$) latches the status information of the digital inputs into the shift register. A subsequent clock signal at CLK, consisting of eight consecutive clock cycles, serially shifts the data out of the DIS register into the input register of an MCU. Each data shift occurs at the rising edge of the clock signal (Figure 6).

**Figure 5. Switch ON condition: $V_{IN-ON}$ = 150 V, $I_{IN-LIM}$ = 0.5 mA**

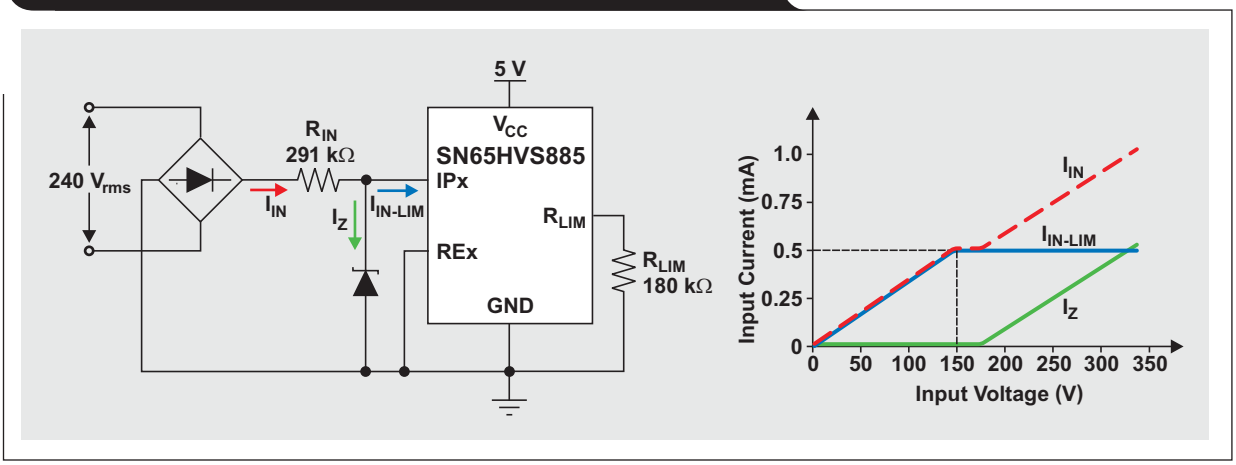
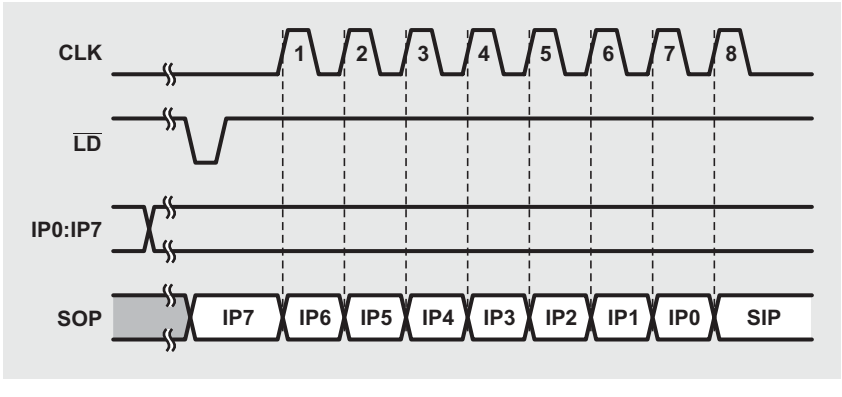



**Figure 6. Serial-interface operation using shift register timing**



Designing input modules with a high channel count is possible by daisy-chaining multiple DIS devices. In this case the serial output of a leading device is connected with the serial input of a following device. Figure 7 shows the simplicity of a daisy-chained, 64-channel digital-input module requiring only three interface lines.

## Powering the interface

DIS devices allow for a variety of power-supply configurations. When powered from an industrial 24-V bus, the DIS can supply 5-V regulated output to digital isolators and MCUs. For 5-V controllers (Figure 8a), the direct connection of supply and serial interface (SIF) lines is straightforward. However, 3.3-V controllers require a low-dropout regulator (LDO) for the supply line and a voltage divider in the serial output (SOP) line (Figure 8b). Control signals from a 3.3-V controller towards the DIS are correctly interpreted.

In applications without a bus supply, it is possible to back-supply a DIS by driving the 5-V output as a supply

**Figure 7. Daisy-chained, 64-channel digital-input module**

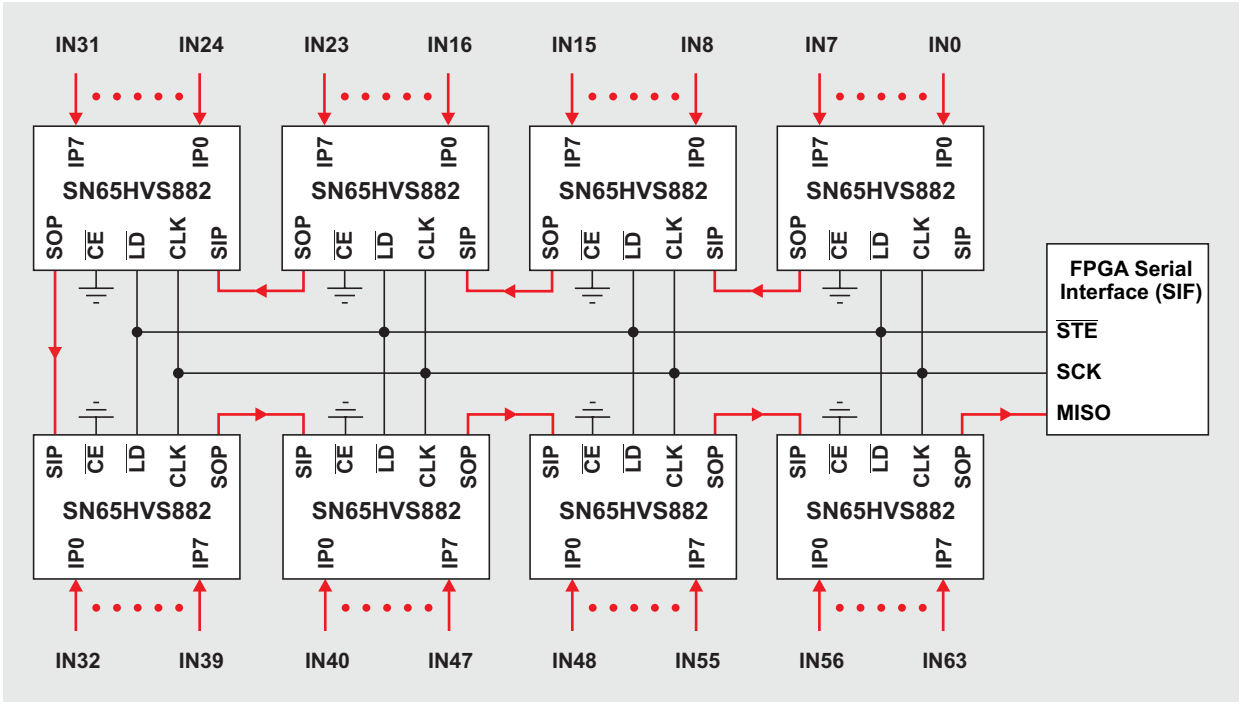



**Figure 8. Bus-powered digital-input system**

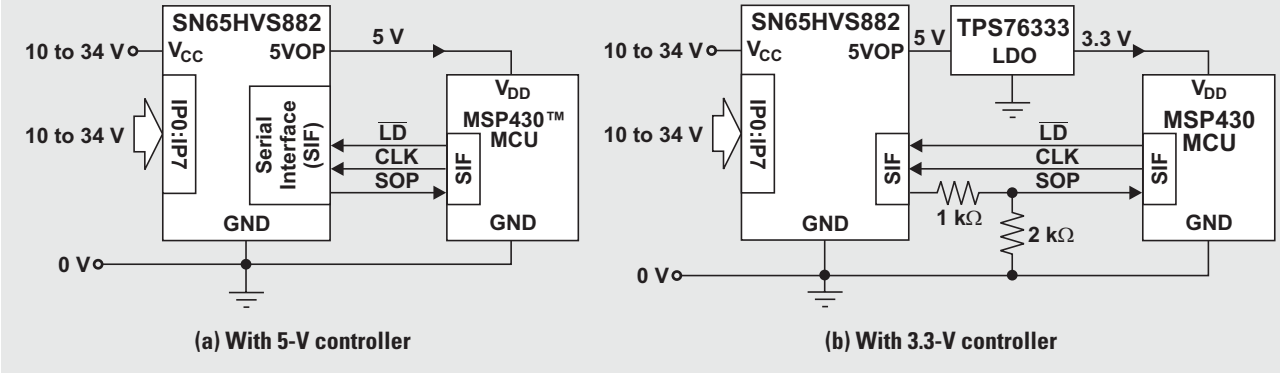
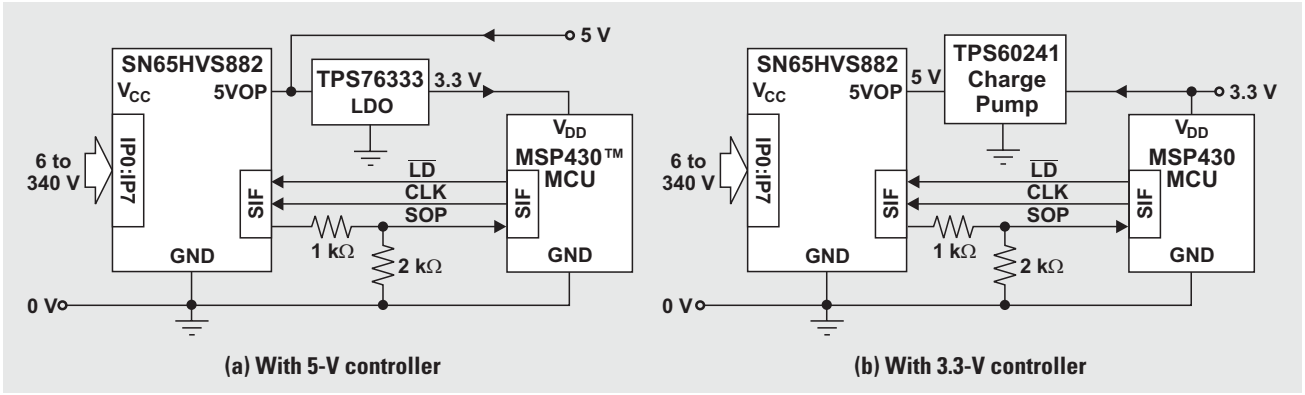


**Figure 9. Back-supplied digital-input system**




input while leaving the normal $V_{CC}$ supply pin floating. Figure 9 shows two back-supply options for interfacing to a 3.3-V controller. In Figure 9a, the 5-V system supply powers the DIS directly but requires an LDO to supply the controller. In Figure 9b, a 3.3-V supply powers the controller directly but requires a charge pump to boost the supply voltage to the required 5-V level of the DIS.

## Conclusion

DIS devices represent the most versatile solution for interfacing a low-power controller to high DC voltages. Supporting the interface design between low-voltage controllers and high-voltage applications, the SN65HVS88x family of DIS devices provides a wide variety of features, such as undervoltage detection, current limiting, debounce filtering, thermal protection, parity generation, and a single 5-V supply.

## References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.


| **Document Title** | **TI Lit. #** |
|---|---|
| 1. Thomas Kugelstadt. (June 28, 2008). New digital input serializers catapult channel count of digital input modules. *EE Times* Industrial Control DesignLine [Online]. Available: http://www.eetimes.com | — |
| 2. SN65HVS880 User's Guide | slau271 |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**www.ti.com/sc/device/***partnumber*
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# Using single-supply fully differential amplifiers with negative input voltages to drive ADCs

**By Jim Karki**
*Member, Technical Staff, High-Performance Analog*

## Introduction

Fully differential amplifiers (FDAs) with a single +5-V supply can be easily used to convert single-ended signals that swing around ground to differential signals that are level-shifted to match the input common-mode requirements of differential-input ADCs. There is no real trick to it, but typically it is best to use a device like the THS4521 with an input common-mode voltage range ($V_{ICR}$) that includes ground. A circuit is proposed and analyzed to show how an FDA with a single +5-V supply can be used to implement the design.

FDAs have been compared to two standard inverting single-ended-output operational amplifiers (op amps) configured in differential architecture and tied together via a common-mode output loop. While this is valid as a concept, there are important differences. For this discussion, an important difference to remember is that when a standard single-ended-output op amp in inverting configuration is used, the input common mode is controlled; but when an FDA is used, the output common mode is controlled.

When a standard single-ended-output op amp in inverting configuration is used, the positive input is not driven from the source and is usually tied to ground or some other reference voltage. The input common-mode voltage at the input pins of the op amp is held at the voltage applied to the positive input by negative feedback, where the op amp drives the error voltage across its input pins to 0 V. This is usually referred to as a virtual short, which is an important concept in op amp theory.

When an FDA is used to convert a single-ended input to a differential output, the alternate input that is not driven by the source is driven by the output through the feedback network. The virtual-short concept is still valid, but the inputs are no longer tied to a reference and move around with the signal. The output common-mode voltage is controlled by the input to the $V_{OCM}$ pin.

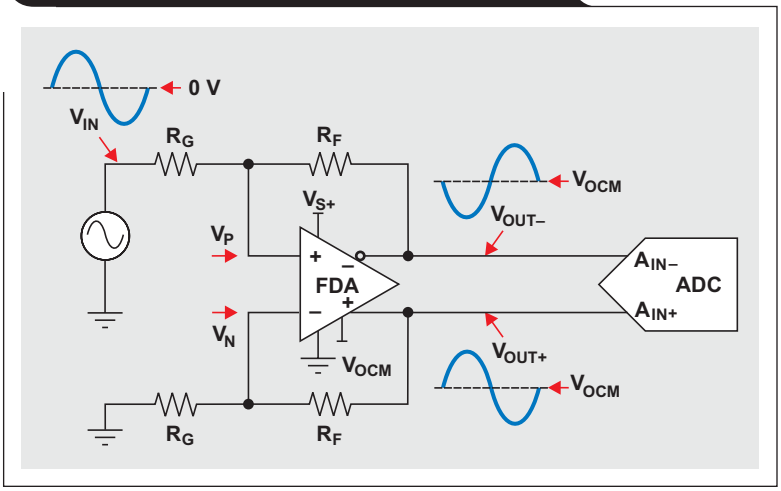
In the following discussion, it is assumed that the reader is familiar with FDA concepts and use. For more information on FDA fundamentals, please see Reference 1.

## Circuit analysis

### Proposed circuit

The proposed circuit for a single-ended bipolar input signal is shown in Figure 1. $V_{S+}$ is the power supply to the amplifier; and the negative supply input is grounded. $V_{IN}$ is the input-signal source. It is shown as a ground-referenced signal swinging around ground (±0 V) and is thus a bipolar signal. $R_G$ and $R_F$ are the main gain-setting resistors for the amplifier. $V_{OUT+}$ and $V_{OUT-}$ are the differential output signals to the ADC. They are 180° out of phase and are level-shifted to $V_{OCM}$.

**Figure 1. Single-ended bipolar input circuit**



### Analysis

For analysis, it is convenient to assume that the FDA is an ideal amplifier with no offset and with infinite gain.

The gain from the single-ended input to the differential output is set by $R_F$ and $R_G$:

$$\frac{V_{OUT\pm}}{V_{IN}} = \frac{R_F}{R_G} \quad (1)$$

Note that there is no multiplication by 2 as with other devices and circuit architectures that can also be used to convert single-ended inputs to differential outputs.

Each single-ended output is half the differential-output common-mode voltage ($+V_{OCM}$):

$$V_{OUT+} = \frac{V_{IN}}{2} \times \frac{R_F}{R_G} + V_{OCM}$$

and

$$V_{OUT-} = \frac{-V_{IN}}{2} \times \frac{R_F}{R_G} + V_{OCM}.$$

For proper operation, the input voltages at $V_P$ and $V_N$ must not exceed the input common-mode voltage range ($V_{ICR}$) of the amplifier, and the outputs must be able to support the voltage-swing requirements of the ADC input. Violating $V_{ICR}$ will lead to nonlinear operation that increases distortion and is sometimes mistaken for output-saturation problems.

To verify that the $V_{ICR}$ is not violated, the virtual-short concept can be used to calculate the voltage at either FDA input pin, since $V_P \approx V_N$. Either of the following two equations can be used, but Equation 3 is easiest.

$$V_P = V_{OUT-} \times \frac{R_G}{R_G + R_F} + V_{IN} \times \frac{R_F}{R_G + R_F} \quad (2)$$

$$V_N = V_{OUT+} \times \frac{R_G}{R_G + R_F} \quad (3)$$

Due to the difference in output and input common-mode voltage, the feedback circuit draws a current equal to the difference in the common-mode voltages divided by $R_F + R_G$. If the gain-setting resistors on the two sides of the FDA are not matched, the difference in common-mode voltage will also cause an offset in the output. So it is important to use resistors with a low tolerance of 1% or better.

### Example

To see how the circuit works, assume that the input signal is 2 $V_{PP}$ and the ADC to be driven is the ADS1278. The ADS1278's full-scale differential input is 5 $V_{PP}$, and the input common-mode voltage is +2.5 V. The THS4521 with a single +5-V supply can be used as the FDA.

It must first be verified that the THS4521 can support the required voltages. The maximum gain to avoid saturating the ADC is 2.5 V/V. Equation 1 can be used to set $R_F$ at 1 kΩ and $R_G$ at 400 Ω. To set the ADC's required input common-mode voltage at +2.5 V, the $V_{OCM}$ of the THS4521 can simply be bypassed to ground with a 0.1-µF capacitor, because $V_{OCM}$ defaults to midsupply (+2.5 V) if not driven. Each output will then swing 2.5 $V_{PP}$ (±1.25 V) around +2.5 V, so the outputs need to support +1.25 V to +3.75 V. A check of the THS4521 data sheet shows that the required output-voltage range is within specification. Note that other converters with different requirements for the input common-mode voltage will need the $V_{OCM}$ pin to be DC-biased to meet those requirements.

Equation 2 can be used to calculate $V_P$ at the positive and negative peaks of the input signal. At $V_{IN}$ = –1 V, $V_{OUT-}$ = +3.75 V.

$$V_P = 3.75\ V \times \frac{400\ \Omega}{1400\ \Omega} - 1\ V \times \frac{1000\ \Omega}{1400\ \Omega} = +0.357\ V$$

At $V_{IN}$ = +1 V, $V_{OUT-}$ = +1.25 V.

$$V_P = 1\ V \times \frac{400\ \Omega}{1400\ \Omega} + 1.25\ V \times \frac{1000\ \Omega}{1400\ \Omega} = +1.071\ V$$

Alternatively, Equation 3 can be used to calculate $V_N$ at the positive and negative peaks of the input signal. At $V_{IN}$ = –1 V, $V_{OUT+}$ = +1.25 V.

$$V_N = 1.25\ V \times \frac{400\ \Omega}{1400\ \Omega} = +0.375\ V$$

At $V_{IN}$ = +1 V, $V_{OUT+}$ = +3.75 V.

$$V_N = 3.75\ V \times \frac{400\ \Omega}{1400\ \Omega} = +1.071\ V$$

The voltages calculated for $V_P$ and $V_N$ are the same as predicted. A check of the THS4521 data sheet shows that the required input-voltage range is within specification.

Even though the input signal swings negative below ground, no negative voltages are required at the FDA pins. When used for conversion from single-ended to differential, the input common-mode voltage to the FDA is modulated with the signal. In contrast, when the input and output are both differential, variation of the input common-mode voltage is much lower and approximately equal to the weighted average (set by $R_F$ and $R_G$) of the output common-mode and input common-mode voltages.

What happens to $V_{ICR}$ when the gain is decreased or increased?

- When the gain decreases, the input voltages ($V_P$ and $V_N$) are driven closer to the output voltage. For a gain of 1, $V_{ICR}$ equals half the output swing on either output. Attenuation, where the gain is less than 1, is a special case; please see Reference 2 for more information.
- When the gain increases, the input voltages ($V_P$ and $V_N$) are driven closer to the input source voltage. As the gain increases, $R_F$ becomes larger and/or $R_G$ becomes smaller; and, assuming that the output-voltage swing is the same, the input-signal swing becomes smaller. $V_{ICR}$ equals the input common mode of the source, which in this case is 0 V, or ground. For a more practical example, given the same 5-$V_{PP}$ differential output as before but with the input reduced so the required gain is 10, $V_{ICR}$ = +0.114 V to +0.341 V.

### Simulation

It is always a good idea to simulate circuit ideas to catch errors and verify that assumptions are valid. Figure 2 shows the result of a transient analysis from TINA-TI™. To see this simulation, go to http://www.ti.com/lit/zip/slyt394 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file THS4521_SE_to_DIFF.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

## Conclusion

Parameters were established for a bipolar single-ended source that needs to be amplified and level-shifted to drive an ADC with a +2.5-V input common-mode voltage and a full-scale input of up to 6 $V_{PP}$. A good option for driving such an ADC is an FDA with a single +5-V supply, a $V_{ICR}$ ranging from –0.1 V to +2 V, and an output voltage ranging from +1 V to +4 V. The THS4521 is an excellent choice for this application, with specifications for a single +5-V supply as follows:

- Input-voltage range = 0 to +3.5 V (minimum to maximum over a temperature range of –40°C to +85°C)
- Output-voltage range = +0.2 to +4.65 V (minimum to maximum over a temperature range of –40°C to +85°C)

Table 1 shows the TI ADCs that are compatible with the output-drive characteristics and performance of the THS4521.

When an FDA with a single +5-V supply is used to drive an ADC with a single +5-V supply (like the THS4521 driving the ADS1278), the potential problem of saturating the ADC's inputs is avoided because its outputs cannot exceed the power-supply voltage.

Please refer to the "Application Information" section of Reference 3 for details on how the THS4521 performs when driving some of these ADCs and for other application information.

**Table 1. TI ADCs compatible with THS4521**

| CONVERTER TYPE | DEVICES |
|---|---|
| Successive approximation register (SAR) | ADS8317/8, ADS8321, ADS8361/4/5, ADS7861/2/3/4/5/9 |
| Delta-sigma | ADS1251/2/3/4/8, ADS1281/2, ADS1158, ADS1271/4/8, ADS1174/8 |
| Audio | PCM1804, PCM3110, PCM3160/8, PCM4201/2/4 |

## References

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1. James Karki, "Fully-differential amplifiers," Application Report. . . . . sloa054
2. Jim Karki, "Using fully differential op amps as attenuators, Part 2: Single-ended bipolar input signals," *Analog Applications Journal* (3Q 2009) . . . . . slyt341
3. "Very low power, negative rail input, rail-to-rail output, fully differential amplifier," THS4521 Data Sheet . . . . . sbos458


## Related Web sites

**amplifier.ti.com**
**www.ti.com/sc/device/ADS1278**
**www.ti.com/sc/device/THS4521**

TINA-TI file for example:
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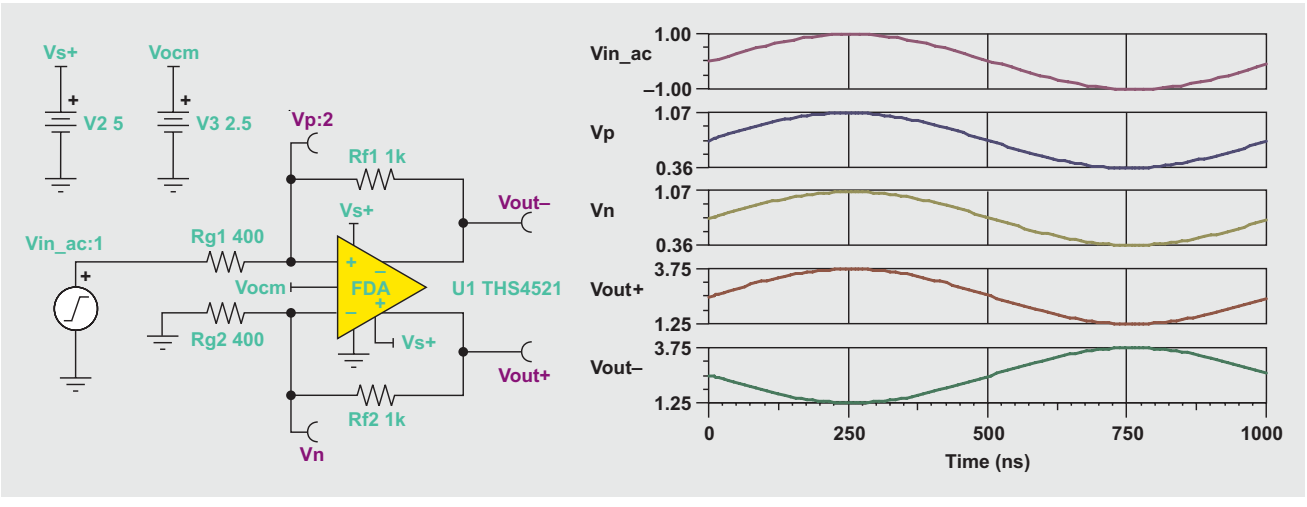
**Figure 2. TINA-TI™ simulation of example circuit**



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