## 1024K (128K x 8) CMOS UV EPROM - OTP ROM

- JEDEC PIN OUT.
- VERY FAST ACCESS TIME : 120 ns .
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
- Active Current 35mA
- Standby Current $200 \mu \mathrm{~A}$
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 12 SECONDS (PRESTO II ALGORITHM).


## DESCRIPTION

The M27C1001 is a high speed 1 Mbit ultraviolet erasable and electrically programmable EPROM ideally suited for 8 -bit microprocessor systems requiring large programs.

It is organized as 131,072 words by 8 bits, and housed in a 32 pin Window Ceramic Frit-Seal package.
The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.
In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIP or PLCC, for One Time Programming only.

PIN FUNCTIONS

| $A O-A 16$ | ADDRESS INPUT |
| :--- | :--- |
| $\overline{\mathrm{CE}}$ | CHIP ENABLE |
| $\overline{\mathrm{OE}}$ | OUTPUT ENABLE |
| PGM | PROGRAM |
| $\mathrm{O} 0-07$ | DATA INPUT/OUTPUT |
| NC | NON CONNECTED |
| $V_{\mathrm{CC}}$ | +5V POWER SUPPLY |
| $V_{\mathrm{PP}}$ | PROGRAMMING VOLTAGE |



Figure 1. Pin Connection


Figure 2 : Block Diagram


## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
| :---: | :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{I}}$ | Input or Output voltages with respect to ground | -0.6 to +7.0 | V |
| $\mathrm{~V}_{\mathrm{PP}}$ | Supply voltage with respect to ground | -0.6 to +14.0 | V |
| $\mathrm{VA}^{2}$ | Voltage on A9 with respect to ground | -0.6 to +13.5 | V |
| $\mathrm{~V}_{\mathrm{cc}}$ | Supply voltage with respect to ground | -0.6 to +7.0 | V |
| $\mathrm{~T}_{\text {bias }}$ | Temperature range under bias | -50 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {stg }}$ | Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

| MODE | PINS |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\mathbf{C E}}$ | OE | A9 | PGM | $V_{\text {PP }}$ | OUTPUT |
| READ | L | L | X | X | $V_{C C}$ | Dout |
| OUTPUT DISABLE | L | H | X | X | $V_{c c}$ | HIGH Z |
| STANDBY | H | X | X | X | $V_{c c}$ | HIGH Z |
| PROGRAM | L | X | X | L | $V_{\text {PP }}$ | Din |
| PROGRAM VERIFY | L | L | X | H | VPP | Dout |
| PROGRAM INHIBIT | H | X | X | X | $V_{\text {PP }}$ | HIGH Z |
| ELECTRONIC SIGNATURE | L | L | $\mathrm{V}_{\mathrm{H}}$ | H | $V_{c c}$ | CODE |

NOTE : $X=$ Don't care ; $V_{H}=12 \mathrm{~V} \pm 0.5 \mathrm{~V} ; \mathrm{H}=$ High ; $\mathrm{L}=$ Low

## READ OPERATION

DC AND AC CONDITIONS

| SELECTION CODE | F1 | F6 | F7 | F3 |
| :--- | :---: | :---: | :---: | :---: |
| Operating Temperature Range | 0 to $+70^{\circ} \mathrm{C}$ | -40 to $+85^{\circ} \mathrm{C}$ | -40 to $+105^{\circ} \mathrm{C}$ | -40 to $+125^{\circ} \mathrm{C}$ |
| SELECTION CODE | $\mathbf{1 2 X F 1 , 1 5 X F 1 , 2 0 X F 1 , 2 5 X F 1}$ |  | $\mathbf{1 2 F 1}, \mathbf{1 5 F 1}, \mathbf{2 0 F 1}, \mathbf{2 5 F 1}$ |  |
| (Example for $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ Oper. Temp. Range) | $5 \mathrm{~V} \pm 5 \%$ |  | $5 \mathrm{~V} \pm 10 \%$ |  |
| $\mathrm{~V}_{\mathrm{CC}}$ |  |  |  |  |

NOTE : "F" stands for ceramic package. Plastic packaged device code features B,M or C.
DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

| Symbol | Parameter | Test Condition | Values |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |
| LI | Input Leakage Current | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}$ to $\mathrm{V}_{\text {cc }}$ | -10 | 10 | $\mu \mathrm{A}$ |
| Loo | Output Leakage Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{CC}}$ | -10 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{IcCl}_{1}$ | Vcc Active Current | $\begin{gathered} \overline{\mathrm{CE}}=\overline{\mathrm{OE}}=\mathrm{V}_{\mathrm{IL}}, \text { lout }=0 \mathrm{~mA} \\ (\mathrm{~F}=5 \mathrm{MHz}) \end{gathered}$ |  | 35 | mA |
| Icce | Vcc Standby Current - TTL | $\overline{\mathrm{CE}}=\mathrm{V}_{\mathrm{IH}}$ |  | 1 | mA |
| $\mathrm{lcCa}^{(4)}$ | Vcc Standby Current - CMOS | $\overline{C E}>\mathrm{V}_{\text {cc }}-0.2 \mathrm{~V}$ |  | 200 | $\mu \mathrm{A}$ |
| IPP1 | Vpp Read Current | $\mathrm{V}_{\mathrm{PP}}=\mathrm{V}_{\mathrm{cc}}$ |  | 10 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {IL }}$ | Input Low Voltage |  | -0.3 | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | Input High Voltage |  | 2.0 | $\mathrm{V}_{\mathrm{cc}+1} .0$ | V |
| VoL | Output Low Voltage | $1 \mathrm{loL}=2.1 \mathrm{~mA}$ |  | 0.4 | V |
| Vон | Output High Voltage | $\begin{aligned} & \begin{array}{l} \mathrm{IOH}=-400 \mu \mathrm{~A} \\ \mathrm{IOH}=-100 \mu \mathrm{~A} \end{array} \end{aligned}$ | $\begin{gathered} 2.4 \\ v_{c c}-0.7 \end{gathered}$ |  | V |

## AC CHARACTERISTICS

| Symbol | Parameter | Test condition | M27C1001 |  |  |  |  |  |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | -12 |  | -15 |  | -20 |  | -25 |  |  |
|  |  |  | Min | Max | Min | Max | Min | Max | Min | Max |  |
| tacc | Address Output Delay | $\overline{C E}=\overline{O E}=V_{\text {IL }}$ |  | 120 |  | 150 |  | 200 |  | 250 | ns |
| tce | $\overline{C E}$ to Output Delay | $\overline{\mathrm{OE}}=\mathrm{V}_{\mathrm{IL}}$ |  | 120 |  | 150 |  | 200 |  | 250 | ns |
| toe | $\overline{O E}$ to Output Delay | $C E=V_{\text {IL }}$ |  | 60 |  | 65 |  | 70 |  | 100 | ns |
| tof $^{(2)}$ | OE High to Output Float | $\overline{C E}=\mathrm{V}_{\text {IL }}$ | 0 | 40 | 0 | 50 | 0 | 60 | 0 | 60 | ns |
| tor | Output Hold from <br> Address, $\overline{C E}$ or $\overline{O E}$ <br> Whichever occured first | $\overline{C E}=\overline{O E}=V_{1 L}$ | 0 |  | 0 |  | 0 |  | 0 |  | ns |

CAPACITANCE ${ }^{(3)}$
( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{f}=1 \mathrm{MHz}$ )

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\mathrm{IN}}$ | Input Capacitance | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ |  | 4 | 6 | pF |
| Cout $^{\text {OUT }}$ | Output Capacitance | V OUT $=0 \mathrm{~V}$ |  | 8 | 12 | pF |

NOTES : 1. VCc must be applied simultaneously or before $V_{P P}$ and removed simultaneously or after Vpp.
2. This parameter is only sampled and not $100 \%$ tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not $100 \%$ tested.
4. From date code 9112.

## AC TEST CONDITIONS

Input Rise and Fall Times Input Pulse Levels
$: \quad \leq 20 \mathrm{~ns}$
: 0.45 to 2.4 V

Figure 3 : AC Testing Input/Output Waveform


Timing Measurement Reference Levels: Inputs : 0.8 and 2V-Outputs : 0.8 and 2 V

Figure 4 : AC Testing Load Circuit


Figure 5 : AC Waveforms


NOTES: 1. Typical values are for $T_{A}=25^{\circ} \mathrm{C}$ and nominal supply voltage.
2. This parameter is only sampled and not $100 \%$ tested.
3. OE may be delayed up to tce - toe after the falling edge CE without impact on tce.
4. TDF is specified from OE or CE whichever occurs first.

## DEVICE OPERATION

The modes of operation of the M27C1001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for VPp and 12V on A9 for Electronic Signature.

## READ MODE

The M27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\overline{\mathrm{CE}}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{\mathrm{OE}}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time ( $t_{A C C}$ ) is equal to the delay from $\overline{C E}$ to output (tCE). Data is available at the output after a delay of toe from the falling edge of $\overline{O E}$, assuming that $\overline{C E}$ has been low and the addresses have been stable for at least tacc-toe.

## STANDBY MODE

The M27C1001 has a standby mode which reduces the active current from 35 mA to 0.2 mA (from date code 9044). The M27C1001 is placed in the standby mode by applying a CMOS high signal to the $\overline{C E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{\mathrm{OE}}$ input.

## TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:
a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.
For the most efficient use of these two control lines, CE should be decoded and used as the primary device selecting function, while $\overline{\mathrm{OE}}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

## SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices.

The supply current, I Icc, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{\mathrm{CE}}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a $1 \mu \mathrm{~F} \mathrm{ce}-$ ramic capacitor be used on every device between $\mathrm{V}_{c c}$ and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a $4.7 \mu \mathrm{~F}$ bulk electrolytic capacitor should be used between $V_{c c}$ and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

## PROGRAMMING

Caution : exceeding 14 V on $V_{p p}$ pin will permanently damage the M27C1001.
When delivered (and after each erasure for UV EPROM), all bits of the M27C1001 are in the "1" state. Data is introduced by selectively programming "Os" into the desired bit locations. Although only "Os" will be programmed, both "1s" and "Os" can be present in the data word. The only way to change a " 0 " to a " 1 " is by die exposition to ultraviolet light (UV EPROM). The M 27 C 1001 is in the programming mode when $\mathrm{V}_{\mathrm{pp}}$ input is at 12.75 V , and CE and PGM are at TTLlow. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. Vcc is specified to be $6.25 \mathrm{~V} \pm 0.25 \mathrm{~V}$.

## PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 12 seconds. Programming with PRESTO II involves in applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

## DEVICE OPERATION (Continued)

## PROGRAM INHIBIT

Programming of multiple M27C1001s in parallel with different data is also easily accomplished. Except for $\overline{\mathrm{CE}}$, all like inputs including $\overline{\mathrm{OE}}$ of the parallel M27C1001 may be common. A TTL low level pulse applied to a M27C1001's $\overline{\mathrm{CE}}$ input, with PGM low and VPP at 12.75 V , will program that M27C1001. A high level $\overline{C E}$ input inhibits the other M27C1001s from being programmed.

## PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{\mathrm{CE}}$ and $\overline{\mathrm{OE}}$ at $\mathrm{V}_{\mathrm{IL}}, \overline{\mathrm{PGM}}$ at $\mathrm{V}_{\mathrm{IH}}, \mathrm{V}_{\mathrm{PP}}$ at 12.75 V and Vcc at 6.25 V .

## ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ} \mathrm{C} \pm 5^{\circ} \mathrm{C}$ ambient temperature range that is required when programming the M27C1001 with $\mathrm{V}_{\mathrm{PP}}=\mathrm{V}_{c c}=5 \mathrm{~V}$. To activate this mode, the programming equipment must force 11.5 V to 12.5 V on address line A 9 of the M 27 C 1001 , with $\mathrm{V}_{\mathrm{pp}}=\mathrm{V}_{c c}=5 \mathrm{~V}$. Two identifier bytes may then be sequenced from the device outputs by toggling address line AO from $\mathrm{V}_{\text {IL }}$ to $\mathrm{V}_{\text {IH }}$. All other address lines must be held at VIL $^{\text {during Electronic Signature mode. }}$

Byte 0 ( $A 0=\mathrm{V}_{\mathrm{IL}}$ ) represents the manufacturer code and byte $1\left(A O=V_{I H}\right)$ the device identifier code. For the SGS-THOMSON M27C1001, these two identifier bytes are given here below, and can be read-out on outputs O 0 to 07.

## ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the $3000-4000 \AA$ range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1001 is exposure to short wave ultraviolet light which has a wavelength of $2537 \AA \AA$. The integrated dose (i.e. UV intensity $x$ exposure time) for erasure should be a minimum of $15 \mathrm{~W}-\mathrm{sec} / \mathrm{cm}^{2}$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 $\mathrm{uW} / \mathrm{cm}^{2}$ power rating. The M27C1001 should be placed within 2.5 cm ( 1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

| IDENTIFIER | PINS |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | AO | 07 | O6 | O5 | O4 | O3 | O2 | 01 | 00 | Hex |
| MANUFACTURER CODE | $V_{\text {IL }}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 |
| DEVICE CODE | $\mathrm{V}_{\mathrm{IH}}$ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |

NOTE : $\mathrm{A} 9=12 \mathrm{~V} \pm 0.5 \mathrm{~V} ; \overline{\mathrm{CE}}=\overline{\mathrm{OE}}=\mathrm{V}_{\mathrm{IL}}, \mathrm{A} 1-\mathrm{A} 8, \mathrm{~A} 10-\mathrm{A} 16=\mathrm{V}_{\mathrm{IL}} ; \mathrm{V}_{\mathrm{PP}}=\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$

## PROGRAMMING OPERATION

( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \pm 5^{\circ} \mathrm{C}, \mathrm{V}_{C C}{ }^{(1)}=6.25 \mathrm{~V} \pm 0.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{PP}}{ }^{(1)}=12.75 \mathrm{~V} \pm 0.25 \mathrm{~V}$ )

## DC AND OPERATING CHARACTERISTICS

| Symbol | Parameter | Test Condition (see note 1) | Values |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |
| ILI | Input Current (All Inputs) | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {IL }}$ or $\mathrm{V}_{\text {IH }}$ |  | 10 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {IL }}$ | Input Low Level (All Inputs) |  | -0.1 | 0.8 | V |
| $\mathrm{V}_{\mathrm{H}}$ | Input High Level |  | 2.4 | $\mathrm{V}_{\mathrm{cc}}+0.5$ | V |
| Vol | Output Low Voltage During Verify | $\mathrm{loL}=2.1 \mathrm{~mA}$ |  | 0.45 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage During Verify | $\mathrm{l}_{\mathrm{OH}}=-400 \mu \mathrm{~A}$ | 2.4 |  | V |
| Icca | V cc Supply Current |  |  | 50 | mA |
| Ipp2 | VPp Supply Current (program) | $\overline{\mathrm{CE}}=\mathrm{V}_{\mathrm{IL}}$ |  | 50 | mA |
| $V_{\text {ID }}$ | A9 Electronic Signature Voltage |  | 11.5 | 12.5 | V |

## AC CHARACTERISTICS

| Symbol | Parameter | Test Condition (see note 1) | Values |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |
| $t_{\text {AS }}$ | Address Setup Time |  | 2 |  | $\mu \mathrm{s}$ |
| toes | OE Setup Time |  | 2 |  | $\mu \mathrm{s}$ |
| tDS | Data Setup Time |  | 2 |  | $\mu \mathrm{s}$ |
| $\mathrm{taH}_{\text {A }}$ | Address Hold Time |  | 0 |  | $\mu \mathrm{s}$ |
| tDH | Data Hold Time |  | 2 |  | $\mu \mathrm{s}$ |
| tbFP(2) | Output Enable Output Float Delay |  | 0 | 130 | ns |
| tvps | Vpp Setup Time |  | 2 |  | $\mu \mathrm{s}$ |
| tvcs | $V_{\text {cc }}$ Setup Time |  | 2 |  | $\mu \mathrm{s}$ |
| tces | $\overline{\mathrm{CE}}$ Setup Time |  | 2 |  | $\mu \mathrm{s}$ |
| tpw | PGM Initial Program Pulse Width |  | 95 | 105 | $\mu \mathrm{s}$ |
| toe | Data Valid from OE |  |  | 100 | ns |

NOTES : 1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. This parameter is only sampled and not $100 \%$ tested. Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

Figure 6 : Programming Waveforms


NOTES: 1. The input timing reference level is 0.8 V for a $\mathrm{V}_{\mathrm{IL}}$ and 2 V for a $\mathrm{V}_{\mathrm{IH}}$.
2. toe and tDPF are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C1001 a $0.1 \mu \mathrm{~F}$ capacitor is required across $\mathrm{V}_{P P}$ and GND to suppress spurious voltage transients which can damage the device.

## PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart


## ORDERING INFORMATION - UV EPROM

| Part Number | Access Time | Supply Voltage | Temp. Range | Package |
| :---: | :---: | :---: | :---: | :---: |
| M27C1001-12XF1 | 120 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-15XF1 | 150 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-20XF1 | 200 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-25XF1 | 250 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-12F1 | 120 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-15F1 | 150 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-20F1 | 200 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-25F1 | 250 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-12XF6 | 120 ns | $5 \mathrm{~V} \pm 5 \%$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-15XF6 | 150 ns | $5 \mathrm{~V} \pm 5 \%$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | FDIP32-W |
| M27C1001-15F6 | 150 ns | $5 \mathrm{~V} \pm 10 \%$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | FDIP32-W |

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

## PACKAGE MECHANICAL DATA

Figure 8 : 32-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL


ORDERING INFORMATION - OTP ROM

| Part Number | Access Time | Supply Voltage | Temp. Range | Package |
| :--- | :---: | :---: | :---: | :---: |
| M27C1001-15XB1 | 150 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PDIP32 |
| M27C1001-20XB1 | 200 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PDIP32 |
| M27C1001-15B1 | 150 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PDIP32 |
| M27C1001-20B1 | 200 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PDIP32 |
| M27C1001-15XB6 | 150 ns | $5 \mathrm{~V} \pm 5 \%$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | PDIP32 |
| M27C1001-15XC1 | 150 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PLCC32 |
| M27C1001-20XC1 | 200 ns | $5 \mathrm{~V} \pm 5 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PLCC32 |
| M27C1001-15C1 | 150 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PLCC32 |
| M27C1001-20C1 | 200 ns | $5 \mathrm{~V} \pm 10 \%$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | PLCC32 |
| M27C1001-15XC6 | 150 ns | $5 \mathrm{~V} \pm 5 \%$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | PLCC32 |

Note : Consult your nearest SGS-THOMSON sales office for availability of other combination.
PACKAGE MECHANICAL DATA - OTP ROM
Figure 9 : 32-PIN PLASTIC DIP


Figure 10 : 32-LEAD PLASTIC LEADED CHIP CARRIER


