Section 54. Graphics LCD (GLCD) Controller

This section of the manual contains the following major topics:

Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices. Please consult the note at the beginning of the **"Graphics LCD (GLCD) Controller"** chapter in the current device data sheet to determine whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Web site at: http://www.microchip.com.

54.1 INTRODUCTION

The Graphics LCD (GLCD) Controller is designed to interface with display glasses using a built-in analog drive to individually control pixels on the screen. The GLCD Controller transfers display data from a memory device and formats it for a display device.The parallel interface at the pins will operate at standard 3.3V output, which requires 28 pins for 24-bit color, and is typically shared by the general purpose I/O functions on the device.

54.1.1 Features

The timing of the programmable vertical and horizontal synchronization signals timing is provided to meet the timing requirements of the display.

Device-specific features include (refer to the specific device data sheet to determine the supported features for your device):

- Supports a variety of color depths and resolutions
- Supports multiple design timing layers, which include:
  - Configurable Alpha Blending
  - Configurable Stride and Pitch
- Supports various input and output formats

Features common to all devices include:

- Dithering for 18-bit displays
- High-quality YUV conversion
- Global color palette look-up table (CLUT) supporting 256 colors
- Global gamma correction, brightness and contrast support
- Programmable cursors supporting 16 colors (including 1 transparent)
- Programmable polarity on HSYNC, VSYNC, DE, and PCLK
- Integrated DMA to offload the CPU
- Programmable (level/edge) interrupt on HSYNC and VSYNC

Figure 54-1 illustrates a block diagram of the GLCD controller.

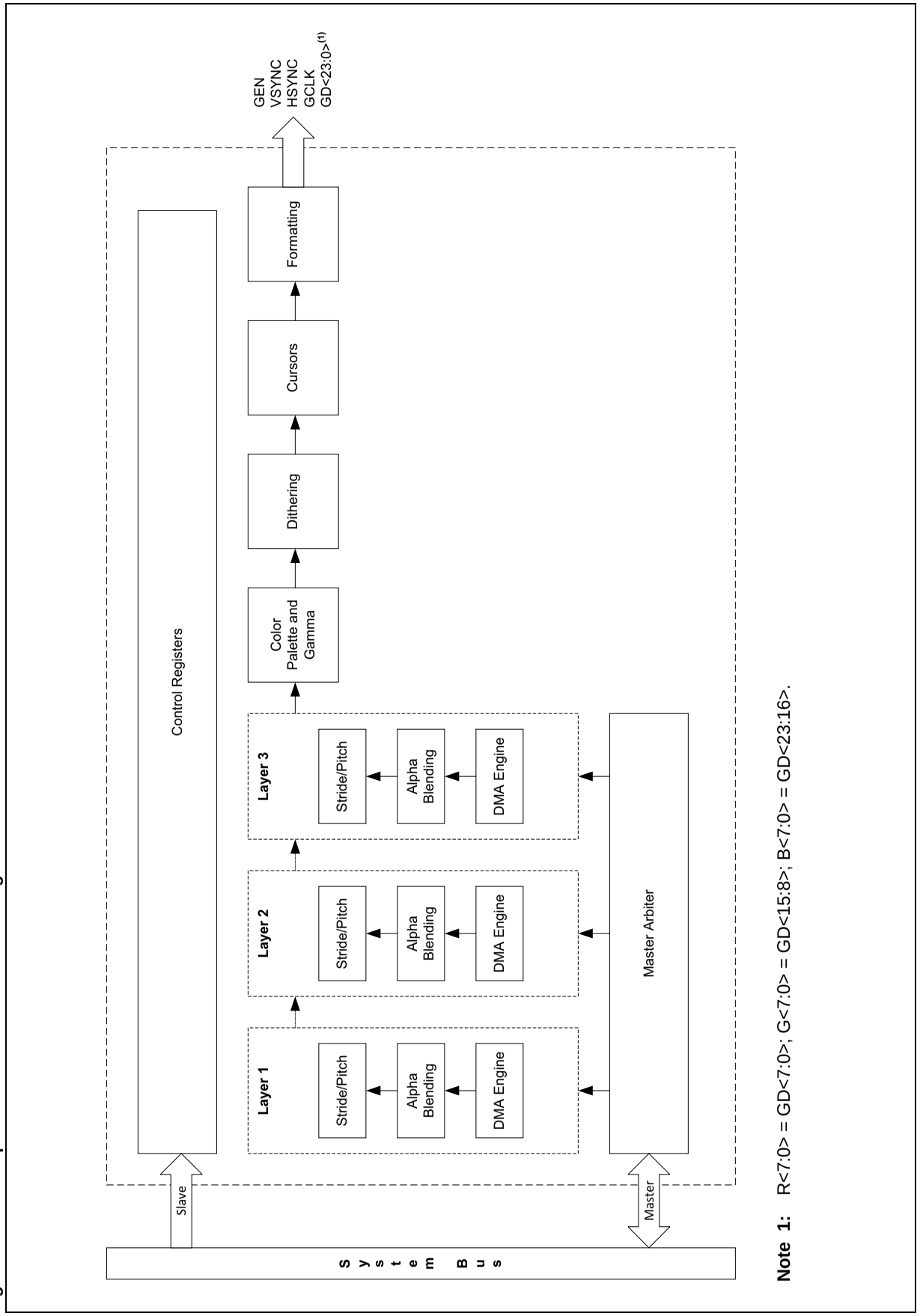


Figure 54-1: Graphics LCD Controller Block Diagram

Note 1: R<7:0> = GD<7:0>; G<7:0> = GD<15:8>; B<7:0> = GD<23:16>.

54.2 CONTROL REGISTERS

The Graphics LCD (GLCD) Controller has the following Special Function Registers (SFRs):

- **GLCDMODE: Graphics LCD Controller Mode Register**

  This register controls the enabling of the GLCD Controller, sets the polarity for the timing signals, and also controls the enabling of the global color look-up table. This register also controls the global color option of RGB, YUV, or Blank. Dithering can be enabled for ramping up color outputs to meet LCD color specifications.

- **GLCDCLKCON: Graphics LCD Controller Clock Control Register**

  This register controls the amount of lines that can be prefetched before starting the frame and also contains the main clock divisor control bits to set up proper timing.

- **GLCDBGCOLOR: Graphics LCD Controller Background Color Register**

  This register contains the 32-bit value that will be the main background color for the GLCD Controller. It accepts a 24-bit RGB color value along with an 8-bit Alpha value.

- **GLCDRES: Graphics LCD Controller Resolution Register**

  This register contains the main X and Y resolutions to be used for the GLCD Controller.

- **GLCDFPORCH: Graphics LCD Controller Front Porch Register**

  This register contains the X and Y dimensions for the Front Porch to be used for the GLCD Controller.

- **GLCDBLANKING: Graphics LCD Controller Blanking Register**

  This register contains the X and Y dimensions for the Blanking period to be used for the GLCD Controller.

- **GLCDBPORCH: Graphics LCD Controller Back Porch Register**

  This register contains the X and Y dimensions for the Blanking period to be used for the GLCD Controller.

- **GLCDCURSOR: Graphics LCD Controller Cursor Register**

  This register contains the X and Y start dimensions for the Cursor of the GLCD Controller.

- **GLCDLxMODE: Graphics LCD Controller Layer ‘x’ Mode Register (‘x’ = 0-2)**

  These registers contain the control for the enabling of the layer. They also support the control for the blending of the layer along with the blending type. Each layer can have its own color mode, which is also selected using this register. Bilinear filtering can be enabled to smooth edges.

- **GLCDLxSTART: Graphics LCD Controller Layer ‘x’ Start Register (‘x’ = 0-2)**

  These registers contain the X and Y start dimensions of the layer to be used.

- **GLCDLxSIZE: Graphics LCD Controller Layer ‘x’ SIZE Register (‘x’ = 0-2)**

  These registers contain the X and Y size of the layer to be used.

- **GLCDLxBADDR: Graphics LCD Controller Layer ‘x’ Base Address Register (‘x’ = 0-2)**

  These registers contain the X and Y start address in memory for the frame buffer to be accessed by the layer.

- **GLCDLxSTRIDE: Graphics LCD Controller Layer ‘x’ Stride Register (‘x’ = 0-2)**

  These registers contain the distance from a frame buffer line to line-in memory. A stride is needed if the frame buffer is not stored continuously.

- **GLCDLxRES: Graphics LCD Controller Layer ‘x’ Resolution Register (‘x’ = 0-2)**

  These registers contain the X and Y dimensions for the resolution of the layer.

- **GLCDINT: Graphics LCD Controller Interrupt Register**

  This register enables timing interrupts from the GLCD Controller, including HSYNC and VSYNC, as well as which type of edge trigger source to be used.

- **GLCDSTAT: Graphics LCD Controller Status Register**

  This register contains the status of the GLCD Controllers including the last row CSYNC, VSYNC, HSYNC, DE, and which state the GLCD Controller is in. The state can either be active or blanking.

- **GLCDCLUTx: Graphics LCD Controller Global Color Lookup Table Register 'x' ('x' = 0-255)**

  These registers contain the global color lookup table component values used by the GLCD controller.

- **GLCDCURDATAx: Graphics LCD Controller Cursor Data 'n' Register ('n' = 0-127)**

  These registers contain the color values for the 32 x 32 pixel Cursor that are to be used with the Cursor LUT.

- **GLCDCURLUTx: Graphics LCD Controller Cursor LUT Register 'x' ('x' = 0-15)**

  These registers contain the 24-bit color values of the LUT used by the Cursor color LUT.

Table 54-1 provides a summary of all Graphics LCD (GLCD) Controller Special Function Registers (SFRs). Corresponding registers appear after the summaries, which include a detailed description of each bit.

Table 54-1: Graphics LCD Controller Register Map

Register Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0
GLCDMODE	31:16	LCDEN	CURSOR EN	—	VSYNC POL	HSYNC POL	DEPOL	—	DITHER	VSYNC CYC	PCLK POL	—	PGRAMP EN	FORCE BLANK	—	—	—
	15:0	—	—	—	—	—	—	YUV OUTPUT	FORMAT CLK	RGBSEQ<2:0>			—	—	—	—	—
GLCDCLKCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	LPREFETCH<5:0>						—	—	CLKDIV<5:0>					
GLCDBGCOLOR	31:16	RED<7:0>								GREEN<7:0>							
	15:0	BLUE<7:0>								ALPHA<7:0>							
GLCDRES	31:16	—	—	—	—	RESX<10:0>											
	15:0	—	—	—	—	RESY<10:0>											
GLCDFPORCH	31:16	—	—	—	—	FPORCHX<10:0>											
	15:0	—	—	—	—	FPORCHY<10:0>											
GLCDBLANKING	31:16	—	—	—	—	BLANKINGX<10:0>											
	15:0	—	—	—	—	BLANKINGY<10:0>											
GLCDBPORCH	31:16	—	—	—	—	BPORCHX<10:0>											
	15:0	—	—	—	—	BPORCHY<10:0>											
GLCDCURSOR	31:16	—	—	—	—	CURSORX<10:0>											
	15:0	—	—	—	—	CURSORY<10:0>											
GLCDL0MODE	31:16	LAYEREN	DISABIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>							
	15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>			
GLCDL0START	31:16	—	—	—	—	STARTX<10:0>											
	15:0	—	—	—	—	STARTY<10:0>											
GLCDL0SIZE	31:16	—	—	—	—	SIZEX<10:0>											
	15:0	—	—	—	—	SIZEY<10:0>											
GLCDL0BADDR	31:16	BASEADDR<31:16>															
	15:0	BASEADDR<15:0>															
GLCDL0STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	STRIDE<15:0>															
GLCDL0RES	31:16	—	—	—	—	RESX<10:0>											
	15:0	—	—	—	—	RESY<10:0>											
GLCDL1MODE	31:16	LAYEREN	DISABIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>							
	15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>			
GLCDL1START	31:16	—	—	—	—	STARTX<10:0>											
	15:0	—	—	—	—	STARTY<10:0>											

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: For the PIXELxy bits, 'x' = 0-31 and 'y' = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

Table 54-1: Graphics LCD Controller Register Map (Continued)

Register Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0
GLCDL1SIZE	31:16	—	—	—	—	SIZEX<10:0>											
	15:0	—	—	—	—	SIZEY<10:0>											
GLCDL1BADDR	31:16	BASEADDR<31:16>															
	15:0	BASEADDR<15:0>															
GLCDL1STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	STRIDE<15:0>															
GLCDL1RES	31:16	—	—	—	—	RESX<10:0>											
	15:0	—	—	—	—	RESY<10:0>											
GLCDL2MODE	31:16	LAYEREN	DISABIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>							
	15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>			
GLCDL2START	31:16	—	—	—	—	STARTX<10:0>											
	15:0	—	—	—	—	STARTY<10:0>											
GLCDL2SIZE	31:16	—	—	—	—	SIZEX<10:0>											
	15:0	—	—	—	—	SIZEY<10:0>											
GLCDL2BADDR	31:16	BASEADDR<31:16>															
	15:0	BASEADDR<15:0>															
GLCDL2STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	STRIDE<15:0>															
GLCDL2RES	31:16	—	—	—	—	RESX<10:0>											
	15:0	—	—	—	—	RESY<10:0>											
GLCDINT	31:16	IRQCON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HSYNCINT	VSYNCINT
GLCDSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	LROW	—	VSYNC	HSYNC	DE	ACTIVE
GLCDCLUTx ('x' = 0-255)	31:16	—	—	—	—	—	—	—	—	RED<7:0>							
	15:0	GREEN<7:0>								BLUE<7:0>							
GLCDCURDATAx ('x' = 0-127)	31:16	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
	15:0	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
GLCDCURLUTx ('x' = 0-15)	31:16	—	—	—	—	—	—	—	—	RED<7:0>							
	15:0	GREEN<7:0>								BLUE<7:0>							

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: For the PIXELxy bits, 'x' = 0-31 and 'y' = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

Register 54-1: GLCDMODE: Graphics LCD Controller Mode Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	LCDEN	CURSOR EN	—	VSYNC POL	HSYNC POL	DEPOL	—	DITHER
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	VSYNC CYC	PCLKPOL	—	PGRAMP EN	FORCE BLANK	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	YUV OUTPUT	FORMAT CLK
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	RGBSEQ<2:0>			—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **LCDEN:** LCD Controller Module Enable bit
1 = LCD Controller module is enabled
0 = LCD Controller module is not enabled

bit 30 **CURSOREN:** Programmable Cursor Enable bit
1 = Programmable cursor is enabled
0 = Programmable cursor is enabled

bit 29 **Unimplemented:** Read as '0'

bit 28 **VSYNCPOL:** Vertical Sync Polarity bit
1 = VSYNC polarity is negative
0 = VSYNC polarity is positive

bit 27 **HSYNCPOL:** Horizontal Sync Polarity bit
1 = HSYNC polarity is negative
0 = HSYNC polarity is positive

bit 26 **DEPOL:** DE Polarity bit
1 = DE polarity is negative
0 = DE polarity is positive

bit 25 **Unimplemented:** Read as '0'

bit 24 **DITHER:** Dithering Enable bit
1 = Dithering is enabled
0 = Dithering is not enabled

bit 23 **VSYNCCYC:** Vertical Sync for Single Cycle Per Line Enable bit
1 = VSYNC for a single cycle per line is enabled
0 = VSYNC for a single cycle per line is not enabled

bit 22 **PCLKPOL:** Pixel Clock Out Polarity bit
1 = Pixel clock out polarity is negative
0 = Pixel clock out polarity is positive

bit 21 **Unimplemented:** Read as '0'

bit 20 **PGRAMPEN:** Palette Gamma Ramp Enable bit
1 = Palette gamma ramp is enabled
0 = Palette gamma ramp is not enabled

Register 54-1: GLCDMODE: Graphics LCD Controller Mode Register (Continued)

bit 19 **FORCEBLANK:** Force Output to Blank bit
1 = Forces output to blank
0 = No effect

bit 18-10 **Unimplemented:** Read as '0'

bit 9 **YUVOUTPUT:** YUV Output Enable bit
1 = YUV is enabled
0 = RGB is enabled

bit 8 **FORMATCLK:** Formatting Clock Divide Enable bit
1 = Formatting clock is not divided
0 = Formatting clock is divided

bit 7-5 **RGBSEQ<2:0>:** RGB Sequential Mode Enable bit
111 = BT.656
110 = YUYV
101 = Reserved
100 = Reserved
011 = Reserved
010 = Reserved
001 = Reserved
000 = Parallel RGB (RGB888, RGB666, RGB323)

bit 4-0 **Unimplemented:** Read as '0'

Register 54-2: GLCDCLKCON: Graphics LCD Controller Clock Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LPREFETCH<5:0>					
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKDIV<5:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **LPREFETCH<5:0>:** Lines Prefetch bits

These bits represent the number of lines to be prefetched before starting the frame (through DMA). The maximum value is $2^{LPREFETCH} = 32$.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **CLKDIV<5:0>:** Clock Divider bits

111111 = Reserved
111110 = Reserved
•
•
•
011111 = Divided by 31
011110 = Divided by 30
011101 = Divided by 29
•
•
•
000011 = Divided by 3
000010 = Divided by 2
000001 = Divided by 1
000000 = Divided by 0

Note: If the value of CLKDIV<5:0> is even, PCLK = (PLL_CLOCK/CLOCKDIV) with a duty cycle of 50%. If the value of CLKDIV<5:0> is odd, PCLK = (PLL_CLOCK/CLOCKDIV) with a duty cycle of 60 to 40%.

Register 54-3: GLCDBGCOLOR: Graphics LCD Controller Background Color Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RED<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALPHA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **RED<7:0>:** Color Red as Background bits
These bits specify that the color red is to be used as the background color.

bit 23-16 **GREEN<7:0>:** Color Green as Background bits
These bits specify that the color red is to be used as the background color.

bit 15-8 **BLUE<7:0>:** Color Blue as Background bits
These bits specify that the color red is to be used as the background color.

bit 7-0 **ALPHA<7:0>:** Color Alpha as Background bits
These bits specify that the color alpha is to be used as the background color.

Note: If all of the bits in this register are set (RED, GREEN, BLUE and ALPHA), RGBA color is used as the background.

Register 54-4: GLCDRES: Graphics LCD Controller Resolution Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESX<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **RESX<10:0>:** X Dimension Pixel Resolution bits
These bits specify the pixel resolution for the X dimension.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **RESY<10:0>:** Y Dimension Pixel Resolution bits
These bits specify the pixel resolution for the Y dimension.

Register 54-5: GLCDFPORCH: Graphics LCD Controller Front Porch Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FPORCHX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FPORCHX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FPORCHY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FPORCHY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **FPORCHX<10:0>:** X Dimension Front Porch Lines bits
These bits specify the front porch X dimension lines.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **FPORCHY<10:0>:** Y Dimension Front Porch Pixel Clocks bits
These bits specify the front porch Y dimension pixel clocks.

Register 54-6: GLCDBLANKING: Graphics LCD Controller Blanking Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BLANKINGX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLANKINGX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BLANKINGY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLANKINGY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **BLANKINGX<10:0>:** X Dimension Blanking Period bits
These bits specify the HSYNC pulse length for the X dimension blanking period.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **BLANKINGY<10:0>:** Y Dimension Blanking Period bits
These bits specify the VSYNC lines for the Y dimension blanking period.

Register 54-7: GLCDBPORCH: Graphics LCD Controller Back Porch Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BPORCHX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BPORCHX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BPORCHY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BPORCHY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **BPORCHX<10:0>:** X Dimension Back Porch Lines bits
These bits specify the front porch X dimension lines.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **BPORCHY<10:0>:** Y Dimension Back Porch Pixel Clocks bits
These bits specify the front porch Y dimension pixel clocks.

Register 54-8: GLCDCURSOR: Graphics LCD Controller Cursor Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CURSORX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CURSORX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CURSORY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CURSORY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **CURSORX<10:0>:** Cursor X Dimension Position bits
These bits specify the X dimension position of the cursor

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **CURSORY<10:0>:** Cursor Y Dimension Position bits
These bits specify the Y dimension position of the cursor

Register 54-9: GLCDLxMODE: Graphics LCD Controller Layer 'x' Mode Register ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	LAYEREN	DISABIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALPHA<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DESTBLEND<3:0>				SRCBLEND<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	COLORMODE<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **LAYEREN:** Layer Enable bit
1 = Layer is enabled
0 = Layer is not enabled

bit 30 **DISABIFIL:** Disable Bilinear Filtering bit
1 = Bilinear filtering is enabled
0 = Bilinear filtering is not enabled

bit 29 **FORCEALPHA:** Force Alpha with Global Alpha bit
1 = Force alpha with global alpha is enabled
0 = Force alpha with global alpha is not enabled

bit 28 **MULALPHA:** Premultiply Image Alpha bit
1 = Premultiply image alpha is enabled
0 = Premultiply image alpha is not enabled

bit 27-24 **Unimplemented:** Read as '0'

bit 23-16 **ALPHA<7:0>:** Layer Alpha bits
These bits contain the Layer Alpha value ranging from 0 to 0xFF.

bit 15-12 **DESTBLEND<3:0>:** Destinary Blending Function bits
1111 = Reserved
1110 = Reserved
1101 = Blend inverted destination
1100 = Reserved
1011 = Reserved
1010 = Blend alpha destination
1001 = Reserved
1000 = Reserved
0111 = Blend inverted source and inverted global
0110 = Blend inverted global
0101 = Blend inverted source
0100 = Blend alpha source and alpha global
0011 = Blend alpha global
0010 = Blend alpha source
0001 = Blend white
0000 = Blend black

Register 54-9: GLCDLxMODE: Graphics LCD Controller Layer 'x' Mode Register ('x' = 0-2) (Continued)

bit 11-8 **SRCBLEND<3:0>:** Source Blending Function bits

1111 = Reserved
1110 = Reserved
1101 = Blend inverted destination
1100 = Reserved
1011 = Reserved
1010 = Blend alpha destination
1001 = Reserved
1000 = Reserved
0111 = Blend inverted source and inverted global
0110 = Blend inverted global
0101 = Blend inverted source
0100 = Blend alpha source and alpha global
0011 = Blend alpha global
0010 = Blend alpha source
0001 = Blend white
0000 = Blend black

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **COLORMODE<3:0>:** Color Mode bits

1111 = Reserved
1110 = Reserved
1101 = Reserved
1100 = Reserved
1011 = RGB888 color format
1010 = YUYV color format
1001 = L4 gray scale/palette format
1000 = L1 gray scale/palette format
0111 = L8 gray scale/palette format
0110 = 32-bit ARGB8888 color format
0101 = 16-bit RGB565 color format
0100 = 8-bit RGB332 color format
0011 = Reserved
0010 = 32-bit RGBA8888 color format
0001 = 16-bit RGBA5551 color format
0000 = 8-bit color palette look-up table (LUT8)

Register 54-10: GLCDLxSTART: Graphics LCD Controller Layer 'x' Start Register ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	STARTX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STARTX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	STARTY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STARTY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **STARTX<10:0>:** Layer Start X Dimension bits
These bits specify the pixel offset of the starting X dimension of the layer.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **STARTY<10:0>:** Layer Start Y Dimension bits
These bits specify the pixel offset of the starting Y dimension of the layer.

Register 54-11: GLCDLxSIZE: Graphics LCD Controller Layer 'x' SIZE Register ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SIZEX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SIZEX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SIZEY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SIZEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **SIZEX<10:0>:** Layer Size X Dimension bits
These bits specify the pixel size of the layer in the X dimension.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **SIZEY<10:0>:** Layer size Y Dimension bits
These bits specify the pixel size of the layer in the Y dimension.

Register 54-12: GLCDLxBADDR: Graphics LCD Controller Layer 'x' Base Address Register ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Base Address of the Framebuffer bits
These bits specify the base address of the framebuffer.

Register 54-13: GLCDLxSTRIDE: Graphics LCD Controller Layer 'x' Stride Register ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRIDE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRIDE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **STRIDE<15:0>:** Layer Stride bits
These bits specify the distance from line to line in bytes.

Register 54-14: GLCDLxRES: Graphics LCD Controller Layer 'x' Resolution Register ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESX<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **RESX<10:0>:** X Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the X dimension.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **RESY<10:0>:** Y Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the Y dimension.

Register 54-15: GLCDINT: Graphics LCD Controller Interrupt Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	IRQCON	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	HSYNCINT	VSYNCINT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **IRQCON:** IRQ Triggering Control bit
1 = Edge triggering is enabled
0 = Level triggering is enabled

bit 30-2 **Unimplemented:** Read as ‘0’

bit 1 **HYSNNCINT:** HSYNC Interrupt Enable bit
1 = HSYNC interrupt is enabled
0 = HSYNC interrupt is not enabled

bit 0 **VSYNCINT:** VSYNC Interrupt Enable bit
1 = VSYNC interrupt is enabled
0 = VSYNC interrupt is not enabled

Register 54-16: GLCDSTAT: Graphics LCD Controller Status Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0	U-0	R-0	R-0	R-0	R-0
	—	—	LROW	—	VSYNC	HSYNC	DE	ACTIVE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **LROW:** Last Row bit
1 = Last row is currently being displayed
0 = Last row is not currently being displayed

bit 4 **Unimplemented:** Read as '0'

bit 3 **VSYNC:** VSYNC Signal Level bit
This bit returns the VSYNC signal level.

bit 2 **HSYNC:** HSYNC Signal Level bit
This bit returns the HSYNC signal level.

bit 1 **DE:** DE Signal Level bit
This bit returns the DE signal level.

bit 0 **ACTIVE:** Active bit
1 = LCD Controller is not in active vertical blanking
0 = LCD Controller is in active vertical blanking

Register 54-17: GLCDCLUTx: Graphics LCD Controller Global Color Lookup Table Register 'x' ('x' = 0-255)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RED<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RED<7:0>:** Global Color Lookup Table Red Component bits

bit 15-8 **GREEN<7:0>:** Global Color Lookup Table Green Component bits

bit 7-0 **BLUE<7:0>:** Global Color Lookup Table Blue Component bits

Register 54-18: GLCDCURDATAx: Graphics LCD Controller Cursor Data 'n' Register ('n' = 0-127)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 27-24 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 23-20 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 19-16 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 15-12 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 11-8 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 7-4 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 3-0 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)

Note 1: For the PIXELxy bits, 'x' = 0-31 and 'y' = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

Register 54-19: GLCDCURLUTx: Graphics LCD Controller Cursor LUT Register 'x' ('x' = 0-15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RED<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RED<7:0>:** Cursor Lookup Table Red Component bit

bit 15-8 **GREEN<7:0>:** Cursor Lookup Table Green Component bit

bit 7-0 **BLUE<7:0>:** Cursor Lookup Table Blue Component bit

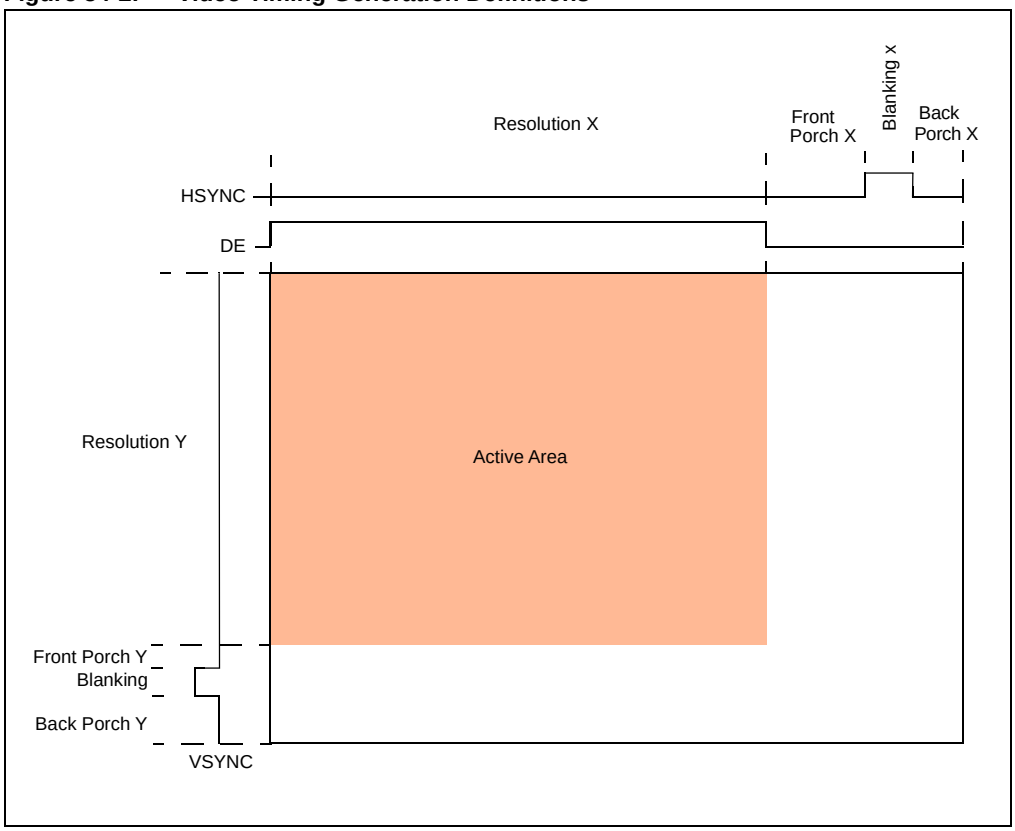
Note: The bits in this register contain the 8-bit RGB color value (0-255).

54.3 OPERATION

The GLCD Controller will continuously refresh the display unit from a defined display buffer while the GPUs access the memory. The refresh rate, resolution, and color depth of the chosen display are used to determine the parameters of the controller.

The GLCD Controller video timing is designed to be easily programmed using timing information. Figure 54-2 shows how the parameters are defined.

Figure 54-2: Video Timing Generation Definitions



Video Timing requires timing parameters for the vertical and horizontal sections. The horizontal timing is all pixel clock-based while the vertical timing is all line-based.

The Controller Video timing is designed using timing information in the same format as X11 Modeline definitions. Equation 54-1 through Equation 54-3 can be used to determine the modeline Front Porch, Back Porch, and Blanking Period.

Equation 54-1: X11 Modeline Horizontal Front Porch Timing

$$FPORCHX = Resolution\ X + Front\ Porch$$

Equation 54-2: X11 Modeline Horizontal Blanking Timing

$$BLANKINGX = FPORCHX + Blanking$$

Equation 54-3: X11 Modeline Horizontal Back Porch Timing

$$BPORCHX = BLANKINGX + Back\ Porch\ X$$

The equations for vertical timing (Equation 54-4 through Equation 54-6) are similar to the horizontal timing, but now they are based on a line basis instead of just a pixel clock cycle.

Equation 54-4: X11 Modeline Vertical Front Porch Timing

$$FPORCHY = Resolution\ Y + Front\ Porch\ Y$$

Equation 54-5: X11 Modeline Vertical Blanking Timing

$$BLANKINGY = FPORCHY + Blanking\ Y$$

Equation 54-6: X11 Modeline Vertical Back Porch Timing

$$BPORCHY = BLANKINGY + Back\ Porch\ Y$$

The frame rate can be derived from the total width and height of the display, see Equation 54-7. The total width and height are also known as horizontal and vertical periods.

Equation 54-7: X11 Modeline Frame Rate

$$Frame\ Rate = GCLK\ Frequency/(BPORCHY\ x\ BPORCHY)$$

Table 54-2 provides the relationship of the display signals to the different parameters of the display controller.

Table 54-2: Display Signal Timing Control Summary

Display Signals	Timing Controlled by Parameters
VSYNC	FPORCHY, RESY, BLANKINGY, BPORCHY
HSYNC	FPORCHX, RESX, BLANKINGX, BPORCHX
DE	HSYNC, VSYNC

Since HSYNC and VSYNC are signals that the display depends on to time sampling of valid data, the overall timing of HSYNC and VSYNC to DE, and valid data must meet the requirement of the display specifications. If the proper requirements are not met, an image may appear on the LCD, but it will be corrupted.

Table 54-3 provides a sample of the configuration of a WVGA TFT display. The WVGA TFT display has the following typical parameters taken from its specifications document:

- Display Clock Period – 33 ns
- Horizontal Period – 928 Clocks
- Horizontal Front Porch – 40 Clocks
- Horizontal Back Porch – 88 Clocks
- Vertical Period – 525 Lines
- Vertical Front Porch – 13 Lines
- Vertical Back Porch – 32 Lines

Table 54-3: WVGA TFT Display Sample Configuration

Parameter	Register	Register Bit(s)	Value	Description
Display Data Bus Enable	GLCDxMODE (Register 54-9)	COLORMODE	0x0101	Display uses all 16-bit data lines so all data bus pins are enabled.
Display Width	GLCDxRES (Register 54-14)	RESX	800	Active frame width.
Display Height		RESY	480	Active frame height.
Display Width Total	GLCDBLANKING (Register 54-6)	BLANKINGX	928	Taken from Equation 54-2.
Display Height Total		BLANKINGY	525	Taken from Equation 54-5.
Display Clock Sampling Edge	GLCDMODE (Register 54-1)	PCLKPOL	1	Display samples data on the falling edge.
Data Enable Signal Active Level		DENPOL	0	Signal is active-high.
VSYNC Signal Active Level		VSYNCPOL	0	Signal is active-low.
HSYNC Signal Active Level		HSYNCPOL	0	Signal is active-low.
VSYNC Start	GLCDFPORCH (Register 54-5)	FPORCHY	493	Taken from Equation 54-4.
HSYNC Start		FPORCHX	840	Taken from Equation 54-1.
VSYNC Length	GLCDBPORCH (Register 54-7)	BPORCHY	528	Taken from Equation 54-6.
HSYNC Length		BPROCHX	968	Taken from Equation 54-3.
Enable Display Controller	GLCDMODE (Register 54-1)	LCDEN	1	Turn on the display controller.

A typical modeline for this display would be as follows:

```
# 800x480 @ 60.00 Hz pclk: 30 MHz
Modeline “800x480_60.00” 30 800 840 928 968 480 493 494 526 -HSync +Vsync
```

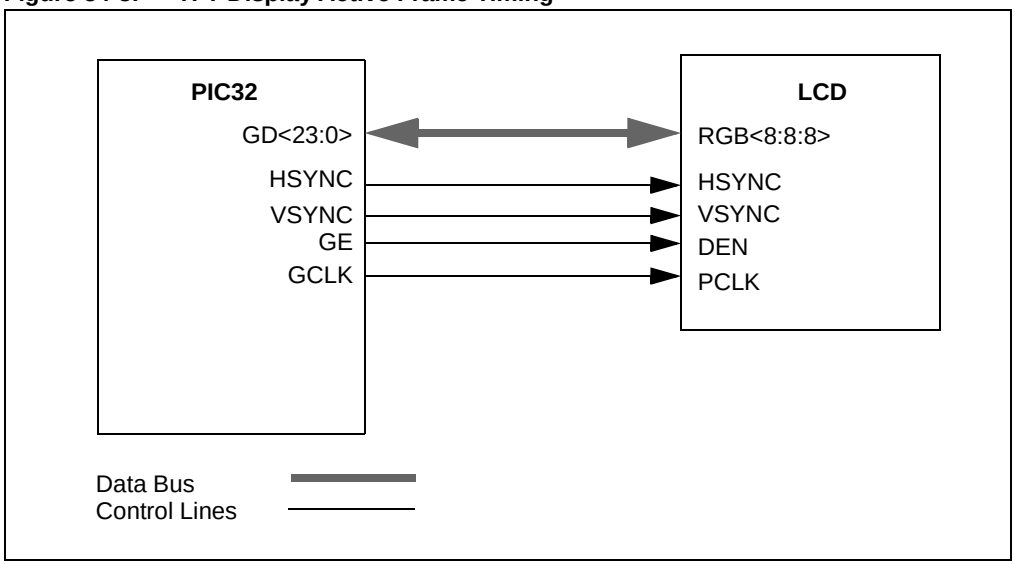

54.3.1 TFT Display Interface

The polarity of the GLCD Controller timing output lines can be changed using the GLCDMODE register (Register 54-1). The pixel clock (GCLK) speed is generated from the GLCDCLKCON register. The speed of this clock should match the timing specifications of the TFT LCD in use.

The display controller continuously reads data from the display buffer and outputs it to the display with the display clock, vertical and horizontal synchronization signals, and enable signal configured to the specifications of the display. Timing of the synchronization signals, polarity of the signals, and required frame rate of the display are determined from the display specifications and translated to values to be programmed into the registers of the display controller.

Different output modes are available through the RGBSEQ<2:0> bits (GLCDMODE<2:0>). To see an image from a frame buffer on a given TFT display at least one layer will need to be defined and set up, refer to **54.4 "Serial Output Formats"**.

Figure 54-3: TFT Display Active Frame Timing



54.3.2 Background Color and Layers

The GLCD Controller supports up to three layers sourced from data memory inside the PIC. The main control register for each layer is the GLCDLxMODE register (Register 54-9). Each layer can have separate color modes, alpha blending, and filtering attributes.

The GLCD Controller layering starts with a 24-bit background color (RGBA), which is applied on the entire screen. If it is not needed, the background register fields can be left blank. The next layer is applied on top of that with a requested blending method. The background color can be used for the blending of two layers and for global values, such as alpha blending and palettes. Its main control register is GLCDBGCOLOR (Register 54-3). If no layer is defined, the background color will only be displayed on the LCD.

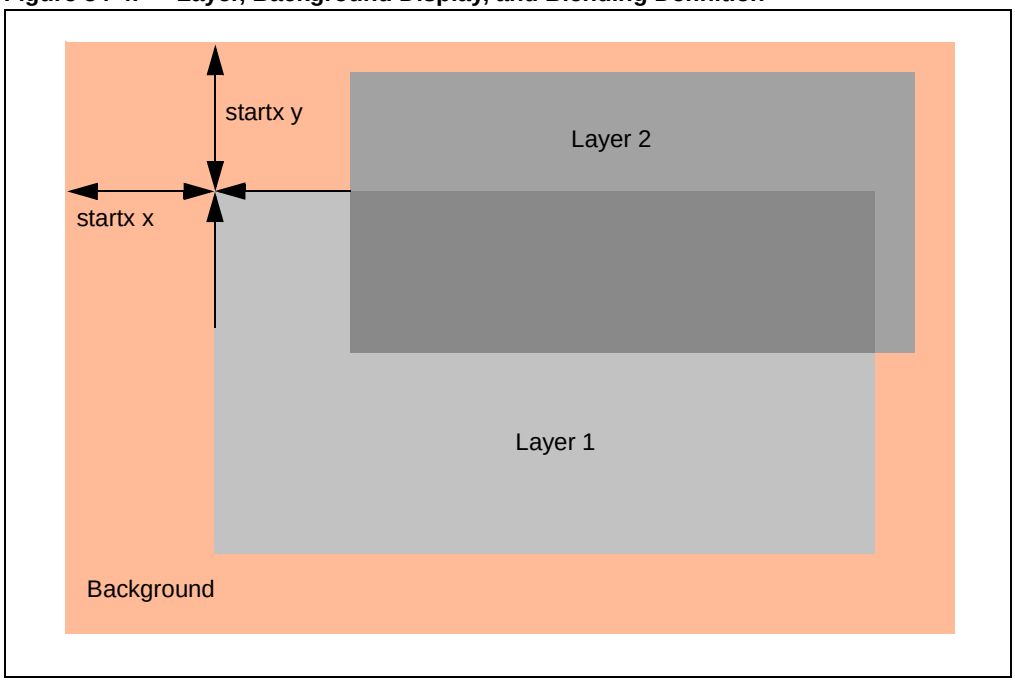
The base frame address is registered inside the GLCDLxBADDR register memory regions (Register 54-12). If the frame buffer is not mapped continuously, the STRIDE<15:0> bits (GLCDLxSTRIDE<15:0>) can be used to add the spacing between the frame lines. The layers overlap in a manner where layer 2 overlaps 1 and so forth. This is not configurable

For each layer, a start GLCDLxSTART (Register 54-10) location and the visible size GLCDLxSIZE (Register 54-11) are needed with a resolution GLCDLxRES (Register 54-14). Alpha Blending takes place if desired.

If no background is desired, the start x,y coordinates can be placed on (0,0) and GLCDLxSIZE can be equal to resolution, GLCDLxRES. In stating this, take note that layers can have different resolutions depending on the layer needs.

In addition, each layer has a choice of color output modes that can be controlled using the COLORMODE<3:0> bits (GLCDLxMODE<3:0>).

Figure 54-4: Layer, Background Display, and Blending Definition



54.3.3 Blending Modes

Blending can be done on a pure layer basis using the DESTBLEND<3:0> bits (GLCDLxMODE<15:12>). The destination refers to the current layer. The source refers to the previous layer. The global refers to the background layer, which is a fixed color.

Each layer is blended on top of the previous generated blended layer with the following function: $c = cs * Fs + cd * Fd$.

Table 54-4 lists the supported blending modes for the Fs and Fd functions.

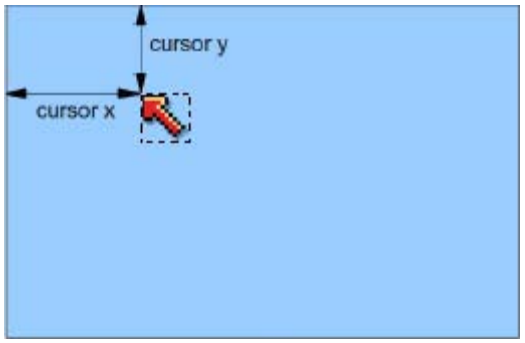
Table 54-4: Supported Blending Modes

Binary	Function	*Fs*	*Fd*
0000	Blend 0s	0	0
0001	Blend 1s	1	1
0010	Blend Alpha Source	*as*	*as*
0011	Blend Alpha Global	*ag*	*ag*
0010	Blend Alpha Source and Global	*as * ag*	*as * ag*
0101	Blend inverted Source	*1 – as*	*1 – as*
0110	Blend Inverted Global	*1 – ag*	*1 – ag*
0111	Blend inverted source and global	*1 – (as * ad)*	*1 – (as * ag)*
1010	Blend Alpha Destination	*ad*	*ad*
1101	Blend Inverted Destination	*1 – ad*	*1 – ad*

54.3.4 Cursor Control

If enabled, the GLCD Controller can support a hardware overlay cursor. This programmable cursor is a fully programmable 32x32 pixel,16-color, and 4-bit cursor with a programmable bit pattern and CLUT memory. Both the cursor pattern and CLUT memory are programmable. Color 0 is reserved for transparency, while the other 15 colors can be set to any 24-bit value using the 16 GLCDCURLUTx registers (Register 54-19). The x,y position of the cursor can be set using the GLCDCURSOR register. Figure 54-5 shows the outline of the 32 pixel x 32 line cursor image of a red arrow. Each individual pixel of the 32 x 32 pixel pattern can be programmed using the 127 GLCDCURDATAx registers (Register 54-18), each of which contains a pixel block of eight specific pixel locations.

Figure 54-5: Cursor Arrow Outline



54.3.5 Palette Control

If an 8-bit palettized color mode is enabled using the PGRAMPEN bit (GLCDMODE<21>), the CLUT memory must be programmed. The GLCDCLUTx registers (Register 54-17) have 256 8 x 3 color bit fields, which hold the RGB value for each of the 256 colors in the palette. The same registers can be used to map RGB values to new RGB values for the purpose of gamma correction. In this mode, the memory area containing the color data to the display will contain the LUT indexes instead of actual color data. Then, the LUT maps these indexes to the color values contained in the palette registers before being sent to the LCD display.

54.4 SERIAL OUTPUT FORMATS

The GLCD controller also supports serial output formats, such as BT.656, Two-Phase Serial 12-bit, Serial 4-beat (RGBA), and Serial 3-beat (RGB) through RGBSEQ<2:0> bits (GLCDMODE<7:5>).

These serial modes have a specific timing requirement and the output is driven on only certain pins. Figure 54-6 through Figure 54-9 represent the timing diagram of the specific modes and data formats.

Figure 54-6: Byte Serial Timing (RGB-3)

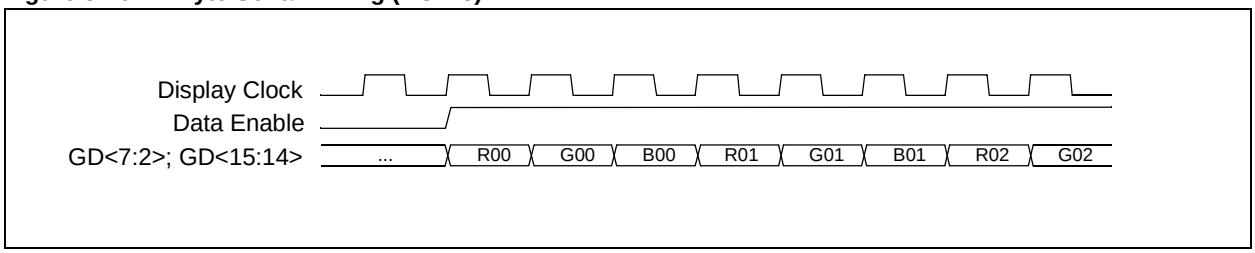


Figure 54-7: Byte Serial Timing (RGBA-4)

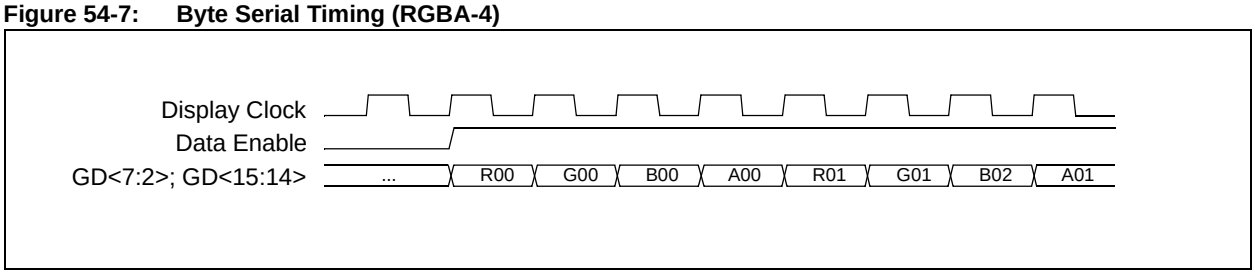


Figure 54-8: Byte Two-Phase 12-bit Mode

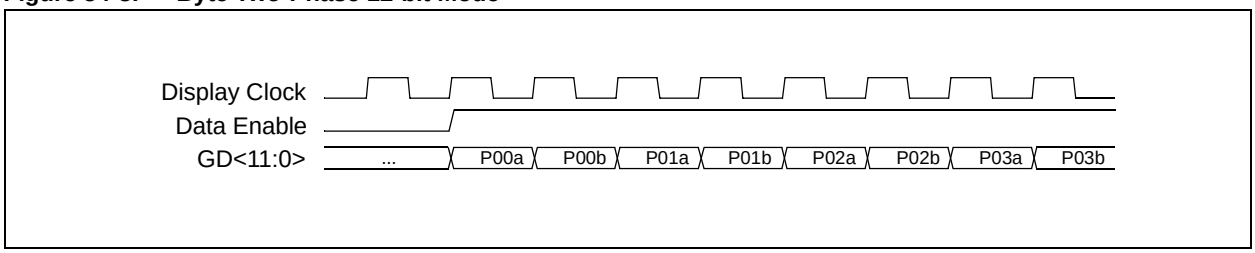
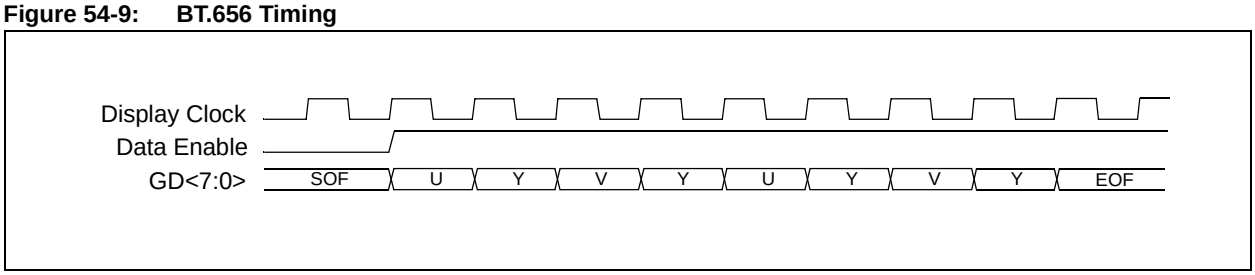


Figure 54-9: BT.656 Timing



54.5 INTERRUPTS

The Graphics LCD Controller module provides two interrupts for horizontal (HSYNC) and vertical (VSYNC) timing. These interrupts can be edge-triggered or level-triggered depending on application requirements. The VSYNC interrupt can be used to monitor the refresh rate of the screen. The HSYNC interrupt can be used to keep track of which line the GLCD Controller is currently displaying.

The GLCDSTAT register (Register 54-16) can be used to check the current status of the controller including the VSYNC, HSYNC, DE levels. The ACTIVE bit (GLCDSTAT<0>) states whether the controller is in an active or blanking period.

54.6 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Graphics LCD (GLCD) Controller include the following:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.

54.7 REVISION HISTORY

Revision A (January 2017)

This is the initial released version of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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