

# **ROCKWELL PARALLEL PROCESSING SYSTEM (PPS)**

## **APPLICATION NOTE for A MICROCOMPUTER BASED CRT/FLOPPY DISK TERMINAL**



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**Microelectronic Device Division**

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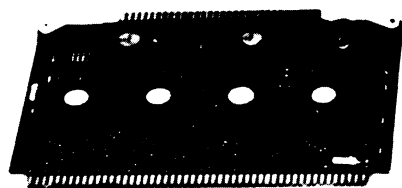
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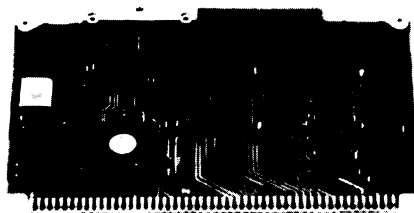
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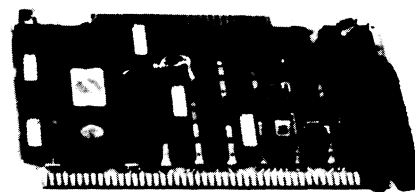
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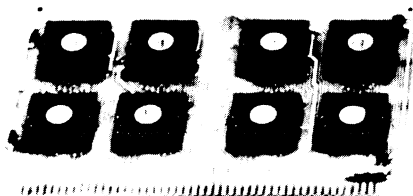
CPU BOARD



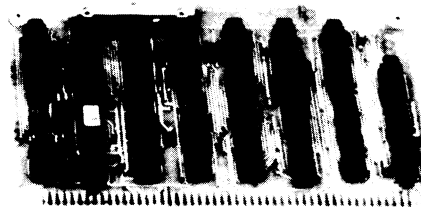
FDC BOARD



CRT/RS-232C INTERFACE



RAM BOARD



CRT CONTROLLER



Figure 1. TYPICAL FDC APPLICATION – FLOPPY DISK/CIRCUIT TERMINAL

# FLOPPY DISK CRT TERMINAL

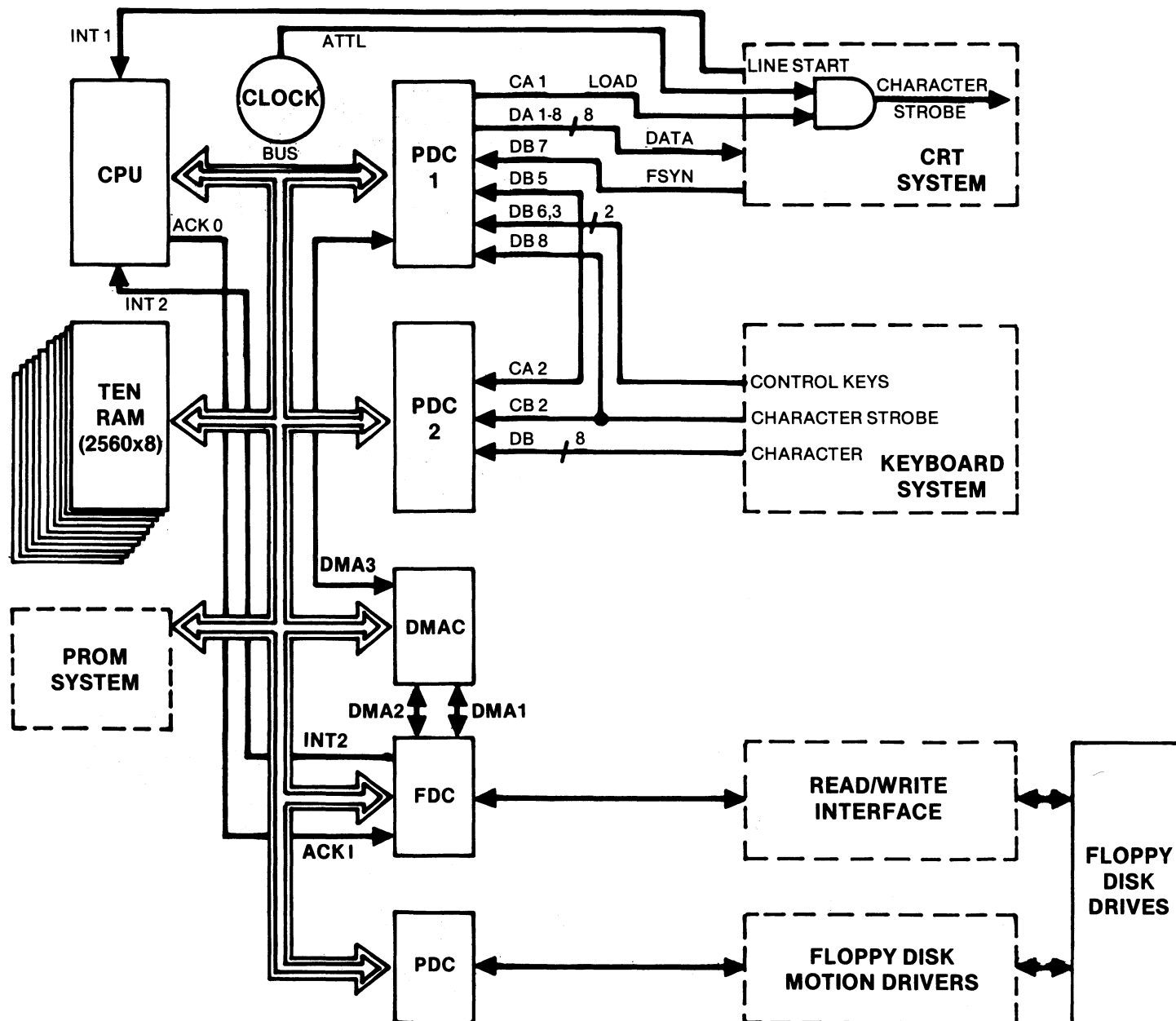


Figure 2.

## INTRODUCTION

This application note describes the hardware and software necessary to implement a PPS-8 microcomputer based intelligent terminal similar to that shown in Figure 1.

The hardware details are presented in the form of block diagrams, schematics and board layouts. The software is detailed with an assembly language listing of the program that controls the system. This program is written as a demonstration program but could be easily changed to solve any problem application for an intelligent terminal.

### CRT/FDC TERMINAL CHARACTERISTICS:

Contains the following six printed circuit modules:

- 1) RAM module - Eight 256 x 8 RAM devices P/N 10809
- 2) ROM module - One 4K x 8 ROM P/N A66XX  
or Two 2K x 8 ROM's P/N A52XX  
or may be a PROM module with  
Two Bus Interface Chips P/N 10738  
Sixteen sockets for 4K x 8 PROM
- 3) Processor II module
  - One PPS-8 CPU P/N 10806
  - One Direct Memory Access P/N 10817
  - Two - 256 x 8 RAM's P/N 10809
  - Two Parallel Data Controller P/N 10453
  - One Clock Generator P/N 10706
- 4) Two CRT Control Modules
  - One Serial Data Controller P/N 10930
  - Forty-one TTL packages
- 5) Floppy Disk Interface Module
  - One Floppy Disk Controller P/N 10936
  - One Parallel Data Controller P/N 10453
  - Twenty-five TTL Packages

ROM Breakdown:	Total Program	2,500 Bytes
CRT Refresh/Keyboard/Editing		850 Bytes
FDC Initialization/Track Selection/Read/Write		400 Bytes
FDC Operator Commands (18 commands)		850 Bytes
EBCDIC/ASCII Conversion Tables		400 Bytes

Other components:

- 1920 Character CRT
- Keyboard w/ASCII Encoding
- Floppy Disk Drive
- Power Supplies

Functionally, the PPS-8 microcomputer performs the following: A. Maintains the CRT screen image and cursor position in RAM memory transferring one 80-byte line to the CRT control logic every 635 microsecond, B. Samples the keyboard for key entries and performs all editing features, and C. Responds to operator commands to perform data transfers to/from the floppy disk.



# **A MICROCOMPUTER-BASED CRT TERMINAL**

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## **INTRODUCTION**

The use of microcomputers as the central control function for CRT terminals offers significant product cost reduction possibilities. While many present CRT products use microcomputers, most of these are used only in the peripheral functions of the system. This paper describes a 1920-character intelligent CRT terminal which uses the Rockwell PPS-8 microcomputer as the primary means of implementation. All system functions are implemented with the PPS-8, including keyboard servicing, CRT refresh from PPS RAM memory, editing, printer interfacing, and communications interfacing.

The paper first describes the functional characteristics of the CRT terminal. Secondly, the PPS-8 microcomputer components are described. Finally, the implementation of the CRT terminal is described in detail.

## **TERMINAL FUNCTIONAL CHARACTERISTICS**

The CRT terminal uses a standard CRT monitor for display. A format of 24 lines of characters with 80 characters per line is provided. Data may be entered through the data entry type alpha-numeric keyboard; external messages may be received through an optional 1200 BPS modem chip. High speed modems may be used in conjunction with our USART-type chip, the Serial Data Controller.

The edit functions include character insert/delete and line insert/delete. Editing is implemented through cursor control in conjunction with cursor control keys and associated function keys on the keyboard. Line Tab, Display Protect, and Line Scroll functions are also provided. A multi-position cursor is provided so that an entire word or phrase may be deleted in one operation instead of one character at a time as is normally done. The display refresh rate is 60 cycles per second, and the monitor is operated in a non-interlaced mode.

Output functions include optional telecommunications and serial party line operations as well as printer options. Telecommunications options provide from 1200 to 9600 BPS operation. The 1200 BPS modem is a single chip configuration with an external analog filter. Printer options consist of 10 to 150 character-per-second alpha-numeric speeds with MOS controllers for full printer control. Higher speed line printers may be interfaced through our PDC I/O chip but require discrete control logic.

The intent of the paper is to illustrate the flexibility of the PPS-8 system in this type of application, and not to describe a finished commercial product. This exercise was undertaken basically for applications know-how. All basic software and hardware design techniques are available to our PPS customers through the Rockwell Applications Engineering staff.

## **THE PPS-8 MICROCOMPUTER SYSTEM**

The PPS-8 microcomputer system is an integrated set of MOS/LSI chips designed primarily for intelligent terminal types of applications. The set is implemented in low cost P-channel technology; system speeds equivalent to, or surpassing, N-channel microcomputers is achieved through system organization. The Rockwell system organization employs a form of distributed processing in which all system chips contain various degrees of intelligence, depending upon their particular function. Some perform dedicated functions, such as printer control or display control; others are programmable through control bytes loaded by the CPU.

We call this approach the Parallel Processing System (PPS). In the Parallel Processing concept, multiple tasks may be executed concurrently in the system. Some tasks will be executed in software; some will be executed in the firmware or dedicated hardware of the intelligent I/O controllers. The CPU becomes the system executive, setting up tasks and assigning them out to the associated controllers. After short data buffer transfers to or from the I/O

### THE PPS-8 MICROCOMPUTER SYSTEM (cont.)

controllers, the CPU is free to attend to the higher level task of the executive software. Normally, detailed CPU intervention in the routine I/O functions of keyboard servicing, display servicing, and block transfer of data into or out of the system is not required. With this approach, system performance may be several times that of CPU-oriented microcomputer alternatives.

A brief discussion of each chip used in the CRT Terminal follows. For a full description of all I/O chips available with the PPS-8 microcomputer, please refer to our marketing literature.

#### CPU

The CPU provides 109 instructions and operates with a four-microsecond instruction cycle. An instruction cycle includes both the instruction fetch and the instruction execute. Most instructions are executed in one cycle. In addition, all Load, Store and Exchange instructions may perform multiple functions in the one cycle to significantly increase system speed. For example, automatic RAM address pointer incrementing/decrementing, testing for loop completion, and switching to a second RAM address pointer can all be accommodated in one basic four-microsecond cycle. This provides for very efficient and fast processing of table-oriented data as is found in an intelligent terminal application. Thus, data bytes may be moved from one table, or buffer, to another at a 12-microsecond/byte rate, including all overhead addressing functions.

The CPU contains many instructions especially useful for intelligent terminal tasks. The ability to set or reset any bit in any byte in RAM memory is provided along with associated conditional branch/skip instructions for any bit condition in RAM memory. The CRT Terminal uses two bits of the 8-bit character code to encode cursor, tab, and protect functions for each individual character or character position, for example. Byte comparisons between the PPS-8 accumulator and addressed RAM locations permit rapid table searching of data with automatic branching or skipping on comparisons or non-comparisons. CPU registers (6) may be loaded directly from ROM memory for subroutine parameters, stored messages, header formats, or form outlines.

The CPU also provides three levels of priority interrupt. The highest priority level is used for power fail detection. The second highest level is useful for a real time clock or a relative time clock. The third level of interrupt is used as the general system interrupt and may be daisy-chained through 15 I/O chips to provide a self-contained priority interrupt structure. The entire interrupt chain may be enabled or disabled, and individual I/O chips in the chain may be individually armed or disarmed to provide a very flexible interrupt structure. This structure is built in the chips, requiring only one external "OR" tie resistor on the interrupt request line. Also, the CPU provides an instruction, Read Interrupt Status, which immediately identifies the I/O device requesting the interrupt and the reason for the interrupt. No software polling of I/O devices is required.

The CPU directly addresses 16K ROM and 16K RAM. An additional chip select line on all ROM's and RAM's provides direct extension to 32K ROM and 32K RAM without any external components. In addition, all ROM's and RAM's directly interface to the CPU address and instruction/data bus without the need for other interface chips. The PPS-8 bus can directly drive up to 350 pF at rated speed. This permits loading the bus with 35-40 chips before being concerned with bus drivers. This is several times the bus driving capability of other systems.

#### DIRECT MEMORY ACCESS CONTROLLER (DMAC)

The DMA Controller provides eight independent channels of DMA capability. Built-in logic provides a DMA priority structure with Channel 0 having the highest priority and Channel 7 having the lowest priority. Each DMA channel is loaded with a starting address and a block length by the CPU. After that, the CPU is free to execute its main line program as the eight individual block transfers set up in the DMAC are executed. At the end of each individual block transfer, the DMAC notifies its appropriate I/O controller. The associated I/O controller may be programmed to respond to the DMA End of Block condition with an interrupt to the CPU or it may be programmed to ignore the EOB condition. On all intermediate transfers within the associated block of data, the I/O devices (independent of the CPU) monitor their control lines and request DMA service from the DMAC when a request for data transfer is received externally. Thus the CPU sets up the DMA channels (up to eight), goes away to work on other tasks, and is informed by the individual I/O controllers by means of interrupts at the end of their block transfer. Data rates on



DMA transfers may vary from 250,000 bytes per second down to one byte per second or less. Again, the CPU is only involved in setting up the initial channel addresses and block lengths and then in responding after a block of data has been completely transferred. Status indicators in the I/O controllers flag any error condition that may have occurred in the block transfer.

The DMA Controller has a Block Repeat function built in for these cases where a continuous repetition of a data block may be required as in a CRT, for example. DMA Channels 0-6 have a repeat control bit which may be set by the CPU. In this mode, the CPU sets the Repeat Bit flag in the channel to be used in the repeat mode and loads the channel starting address and block length in the primary channel (Channel 0-6) as well as in Channel 7, the Refresh channel. Now, when the primary channel reaches the end of the block of data (Block Length = 0) it checks its repeat flag bit and, since it is set, the primary channel transfers the initial address pointer and initial block length stored in Channel 7 into its registers so that it may repeat the block transfer again. At every End of Block condition, the primary channel will again refresh its initial address and block length from Channel 7, thereby continually repeating the block transfer as desired.

### **PARALLEL DATA CONTROLLER (PDC)**

The PDC is a dual 8-bit programmable I/O controller which has the ability to initiate interrupt requests or DMA transfer requests upon the occurrence of external control line transitions. Each 8-bit port contains two programmable control lines whose functions are programmed by the CPU by means of control bytes. In addition, the mode of each port is programmable; i.e., input, output, or input/output. In addition, the type of data transfer is programmable; i.e., static, clocked, or handshake transfer. The ability of the PDC to request interrupts or DMA service may be armed or disarmed by appropriate control byte bit patterns. In addition, the PDC may be programmed to request an interrupt on the DMAC indication of an End of Block transfer or it may be programmed to ignore the EOB condition. Status registers detect the occurrence of any data transfer error (buffer underrun or buffer overrun) which may occur.

### **SERIAL DATA CONTROLLER (SDC)**

The Serial Data Controller is a full duplex, USART chip. The function of the chip is programmable by means of a control byte loaded by the CPU. Controllable parameters include bits per character (5, 6, 7, or 8), number of stop bits for asynchronous operations (1.0, 1.5, 2.0), and for parity insertion/checking (odd, even, none). The SDC contains five RS-232-C interface control lines for convenience in interfacing to high speed modems. The SDC may be used in party line operation between master and slave terminals, for example. The SDC will transmit up to 250,000 bits per second in the synchronous mode. In this mode, the null character, once loaded into the SDC, will be automatically repeated in transmission until another valid data character is sent. Thus, the system will stay in sync even though a transmit buffer may run empty, provided the last character in the buffer is the null character. Double buffering of both the receive and transmit channels is provided.

The SDC also has a Receive Compare register which continuously compares a byte loaded into it by the CPU with incoming data. Upon comparison, the SDC can be programmed to request an interrupt, thereby notifying the CPU of a valid comparison. This function may be used to search for the terminal's address on the party line or multi-drop communication line, for example. Or it may be used to automatically search and verify a sequence of communication protocol control characters. Using this feature, the SDC can be set up to strip off all null (or sync) characters, identify the terminal address, and then start interrupting the CPU, or else requesting DMA service, on each framed input character. This is done independent of the CPU activity after the compare byte has been loaded. Multiple byte addresses or control sequences can be handled by successive recognition and then loading of the next byte of the sequence. Error checking for buffer overrun/framing errors, parity errors or carrier drop-outs is provided. Thus, after a block transfer, the quality of the entire transfer may be quickly checked by the CPU through reading the SDC quality register.

## FLOPPY DISC CONTROLLER (FDC)

The Floppy Disc Controller provides all data formatting required for reading or writing on floppy disc media from byte-oriented RAM storage. Up to four floppy discs may be serviced by one FDC. For Write operations, the FDC provides track address verification and sector address search/comparison logic, preamble and postamble generation, write head current enabling, parallel to serial conversion, and CRC polynomial generation and detecting. For Read operations, the FDC provides track verification and sector address search/comparison logic, CRC polynomial generation from sensed data and comparison with the recorded CRC field, disc format verification, and serial to parallel data conversion.

In addition, the FDC provides a Read Compare register similar to the SDC. This register permits stripping of preamble bits, postamble bits, and address fields from the incoming data stream so that only the addressed sector data is transferred to RAM memory. No CPU processing is required to separate the floppy disc overhead fields (preamble, postamble, address) from the data field of interest.

To implement a full floppy disc memory system, a General Purpose Input/Output chip (GP I/O) is required for disc selection, track position control of the read/write head, head loading/unloading, and status information. External circuitry is needed to combine clock and data for recording and to extract the clock from this data when reading.

The format of the FDC is under software control so that user formats may be used in addition to the compatible IBM format. Non-IBM formats permit much greater data packing density than the IBM format provides. Many users may want to use a packed format for data storage, and then convert to IBM format for interchangeable discs. This can be readily done with the FDC. In fact, each track within the disc may have its own format. In a four disc system, for example, one disc may be recorded in IBM format for interchangeability, while the three other discs are recorded in a packed format for improved data capacity. A software routine would then be used to unpack the packed format and record the data in the less dense IBM compatible format for disc interchange compatibility. Disc commands include Read, Write, Write Format, Read CRC Check, Read Address Field, and Read Status.

## GENERAL PURPOSE INPUT/OUTPUT CONTROLLER (GP I/O)

The GP I/O is a programmable chip which provides twelve discrete input lines and twelve discrete output lines. The input and output lines are addressed in groups of four lines each. Thus, input lines are addressed in terms of Group A, Group B, or Group C. Similarly, the output lines are grouped in terms of Group A, Group B, or Group C. Input lines are static; output lines are latched and maintain their levels until re-loaded.

The CPU addresses the GP I/O and commands it to read from individual input groups or to output to the individual output groups. Also provisions are made to "OR" input groups in one instruction, or to "AND" output groups. Thus, the "OR" condition of all input lines, by group, may be read into the CPU in one instruction. Or, the same bit pattern may be applied to all output groups in one instruction.

## OTHER CONTROLLERS

Other controllers consist of keyboard controllers, display controllers, and printer controllers. The keyboard controllers provide all strobes, strobe return sensing, key debounce, key rollover, and key buffering functions. The CPU is only required to unload the key buffer once each 50-100 milliseconds. Display controllers provide all multiplexing of digit display information as well as digit select strobes. The CPU merely transmits up to a 16-character display buffer to the chip; the chip does the rest. A combination keyboard/display controller, the GP K/D, is available. This chip is used with up to 64-key keyboards and Panaplex<sup>®</sup>, Burroughs' Self Scan<sup>®</sup>, or LED displays. Several Printer Controller chips are also available. For example, a two-chip set is available for control of a 150 cps, alpha-numeric dot matrix printer. The only discrete circuitry required are the power driver transistors. Chip outputs drive one standard TTL load (2.6 ma). A combination Keyboard/Printer chip is also provided to control a 64-key keyboard as well as a 22-column printer.

## TELECOMMUNICATIONS DATA INTERFACE CONTROLLER (TDI)

The TDI chip provides a full duplex programmable UART function as well as a 1200 BPS modem function. The modem may be strapped for Bell 202 or CCITT signaling frequency compatibility. The modem design accommodates 1200 BPS transmission over a dial up, unconditioned telephone line. The UART may be programmed for bits per character (8, 16, 64), parity (none, odd, even), and signaling frequency. The TDI has interrupt capability; up to 16 TDI chips may be incorporated in a single system. A serial mode which utilizes the modem function only and disables the UART function is also provided so that the chip can be used as a stand-alone modem.

Some external circuitry is required for full modem implementation. A four pole analog filter is required on the receiver input and a simple operational amplifier with four summing resistors is required on the transmitter output line.

## RAM'S

The PPS-8 RAM's are 256 x 8 bit RAM's with full address decoding on each chip. The RAM's are dynamic, but appear static to the user since all refresh is done automatically without interference to the user. Standard 4K x 1 RAM's of the 16 pin configuration can be interfaced to the PPS-8 by means of our 4K Interface Controller Chip. This chip provides all interfacing and refresh functions required for standard memory operation. Two interface chips are required per system. These service up to a 16K x 8 RAM and present only two units of load (10pf) to the PPS Bus. Multiple memory modules may be used. The 4K RAM Controller Chip has the ability to float its output lines so that external control of the 4K RAM memory is possible. Thus, the 4K RAM can be loaded externally at the full 4K RAM speed; then the PPS-8 can operate on this data at rates up to 250,000 bytes per second.

## ROM'S

The PPS-8 ROM's are 2048 x 8 bits, also with full address decoding on each chip. Thus, up to 16K of ROM easily fits on one 5½ x 7-inch PC board.

## THE CRT TERMINAL

A basic CRT Terminal will first be discussed. Then an expanded terminal with floppy disc memory and printer will be described. Finally, an expansion of the terminal to graphic display functions will be briefly outlined.

The basic organization of the CRT Terminal includes PPS-8 RAM memory as the data storage media. A DMA channel is then used to load one of two line buffers, each being 80 characters in length. As the DMA loads one line buffer, the other line buffer is driving the CRT monitor. As one line buffer completes its line display function, control logic switches to the other line buffer which has been loaded through DMA. The initial line buffer is then refilled by DMA while the second line buffer is driving the display.

The CRT basic terminal implementation with the PPS-8 is illustrated in *Figure 1*. The system is implemented with a CPU, 2560 x 8 RAM Memory, 2K x 8 ROM/PROM, a DMAC, and a PDC. The CPU, PDC, DMAC, and two RAM chips (512 x 8) are contained on our PPS-8 Processor II evaluation board. The additional 2048 x 8 RAM is contained on our RAM evaluation board. One board of TTL logic contains the double line buffers and associated raster control, character generator and associated control logic. Our PROM evaluation board is presently used for program storage. Eventually, this board will be replaced with one ROM chip mounted on an option board which also contains provision for the Floppy Disc Controller, GP I/O, and SDC or TDI modem. The hardware used in the basic CRT terminal is illustrated in *Figure 10*. The display control word is illustrated in *Figure 2*. Two basic versions are shown. One provides upper/lower case characters plus cursor. The other provides the expanded functional controls of Tab and Display Protect.

## DISPLAY CONTROL

The display is generated from a standard TV raster as shown in *Figure 3*. Eleven scans comprise the formation of one line of characters as illustrated. The display refreshing is accomplished as shown in *Figure 4A* and *4B*. In *Figure 4A*, Line Buffer 1 is driving the display through the character generator and shift register. It is also recirculating on itself corresponding to the eleven scans required to generate the full line of characters. During this time, Line Buffer 2 is being loaded via DMA through PDC 1. Timing for this operation is illustrated in *Figure 5*. After completion of the present line of display, Line Buffer 2, which has just been loaded with the next line of characters, is switched to the active display mode, and Line Buffer 1 is switched to the load mode. This is illustrated in *Figure 4B*.

## CRT REFRESH CONTROL

The CRT refreshing is accomplished under DMAC control. Each data transfer from RAM memory to the CRT line buffers consists of 80 characters. Initially, DMA channel 3 is set up by the CPU to RAM refresh address 0 and with a record length count of 80 characters. After transferring the first line of data of 80 characters in a burst mode, the Channel 3 address pointer in the DMAC will be pointing to address 79 and the block length counter will be decremented to 0. The DMAC will then notify the PDC of an end-of-block condition. The PDC will then interrupt the CPU to notify it of the condition. The CPU will then re-initialize the channel 3 block length to 80, thus setting up the next block transfer which will be 80 characters starting at RAM address 80. At the next end-of-CRT line condition (line interrupt), the PDC will request DMA transfer to refill the CRT line buffer. Characters 80 – 159 will then be transferred in a burst mode to the CRT line buffer. When this transfer is completed the channel 3 address pointer will be setting at RAM address 160 and the block length counter will be decremented to 0. This end-of-block condition, once again, will cause the PDC to interrupt the CPU to restore the channel 3 block length count. This process continues until the entire frame (24 lines) has been displayed. At the end of the frame, an End-of-Frame interrupt is generated on Interrupt level 1. This End-of-Frame interrupt will then cause the CPU to refresh DMAC channel 3, with both RAM address 0 and a block length of 80 characters. Thus, the DMAC channel is now set up to start the next complete frame of refresh.

## CRT EDIT/SYSTEM CONTROL

A CRT line buffer loading requires 320 microseconds to load the 80 characters. During loading the transfer occurs in a burst mode of 250,000 bytes per second. After the line buffer is loaded, the CPU is free for 378 microseconds to perform system edit and control functions. This provides adequate time for all worst case edit functions to occur within 2 frame times. This, of course, appears instantaneous to the operator.

The key to the operation of the expanded system is that all data transfers to the MODEM, party line, line printer, or floppy disc, are also handled by DMA block transfer. The addressing overhead associated with these simultaneous transfers is thereby reduced, for all practical purposes, to virtually nothing. For example, to transmit the CRT display of 1920 characters at 9600 bps (1200 characters per second) requires 1.6 seconds of real time, or 1,600,000 microseconds. The CPU intervention required to control this transfer amounts to the time to load 3 bytes of initial address pointer and block length into the MODEM DMA channel (24 microseconds). The PPS system time required for the transfer is  $1920 \times 4 \text{ sec}$ , or 7,680 microseconds. This amounts to approximately 0.5% of system time. With the priority structure of the DMAC, up to 8 block transfers may be occurring simultaneously (all at different data rates) with all prioritizing between block transfers and addressing overhead for each transfer handled by the DMAC. While the CPU floats in a wait state during DMA transfers, the fact that its chain of operations do not have to be interrupted and then restored for each functional transfer of data greatly reduces system overhead requirements as well as software complexity. The basic CRT terminal program occupies 630 bytes of ROM, for example.

## SYSTEM TIMING

The timing associated with system operation is shown in *Figure 6a*. All numbers relate to PPS-8 system time required. Refreshing the line buffers required 320 microseconds per line time of 698.5 microseconds. Thus, 46% of system time is required for refreshing. At 9600 BPS, the modem servicing time requires 0.48% of system time for data transfer. This does not include modem control overhead. The time left for editing and system control software is approximately 100,000 system cycle times per second, or 40% of the system time. The expanded system with Floppy disc memory, printer, modem, and/or party line control is illustrated in *Figure 7*. Timing for this expanded system is shown in *Figure 6b*.

## GRAPHICS DISPLAY

Addition of a graphics display function is also feasible. For a 125-line by 555-grid, graphic refresh via DMA is feasible. This mode would provide the graphic refresh plus an 800-character refresh capability. To implement the described graphic capability would require an additional 8K of RAM Memory. In addition, a large amount of CPU time would be required for graphic conversion. The PPS-8 implementation for this mode might be as illustrated in *Figure 8*. The additional graphics memory is constructed of standard 4K x 1 RAM chips of the 16 pin configuration. This memory module is interfaced to the PPS-8 CPU by means of a 4K RAM Interface chip now under development. The system in *Figure 8* would be adequate if the graphic data were previously formatted for graphic display prior to loading into the RAM module. Both graphic and character refresh would require approximately 75% of the CPU time. Some additional TTL logic would also be required to "OR" the graphic and character data into the video input of the monitor. If it is desired to do the graphic formatting in the terminal system, a second PPS-8 CPU and its ROM may be added to the system as illustrated in *Figure 9*. In this configuration, CPU-2 and ROM-2 are dedicated to graphics formatting using a 4K RAM Interface chip to access the 4K RAM memory while CPU-1 is providing the character refresh function out of its PPS RAM. When CPU-2 has formatted a graphic display, it then passes control of the 4K RAM module to CPU-1 for display and refresh of the graphic function as well as for a reduced (800) character display and refresh. This mode is feasible since each 4K RAM Interface chip has the ability to float its output lines to the 4K RAM module.

Alternately, a DMAC can be added to CPU-2 so that all graphic formatting display, and refreshing is done by the second system. This will off load System 1 so that all other intelligent terminal functions can be executed in System 1. The addition of System 2 would also permit graphic expansion to 225 x 555 points with the addition of another 8K of RAM memory. System 2 would consist of a single 5 x 7 in. PC board plus the additional 8K of RAM.

## SUMMARY

This application illustrates the power and flexibility of the PPS-8 microcomputer system in both the single and multiprocessor modes. The advantages of a complete set of systems-structured, intelligent controllers are demonstrated with this applications study. Very significant product cost reductions may be achieved with this approach, as demonstrated by the minimal amount of hardware required for this CRT application.

The hardware for the basic display terminal is illustrated in *Figure 10*. The addition of the floppy disc and printer require 3 additional chips from those shown. The addition of the graphics capability requires one additional interface chip plus the expanded 8K of RAM plus additional ROM memory for programming . . . probably one of our 2K x 8 ROM chips.



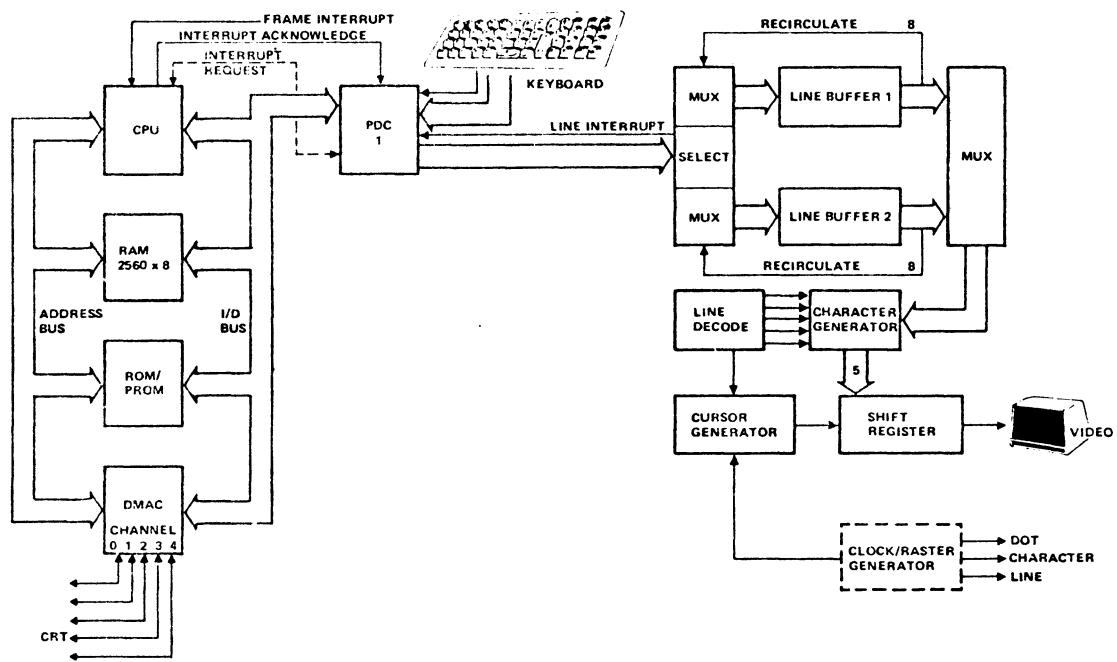


Figure 1. BASIC CRT SYSTEM

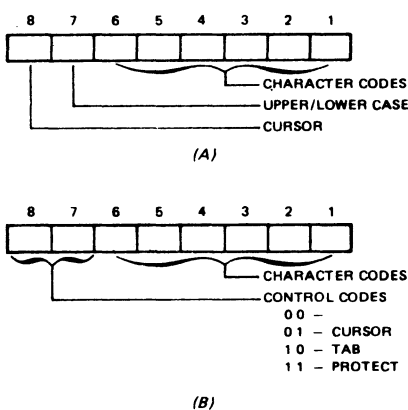


Figure 2. DISPLAY CONTROL

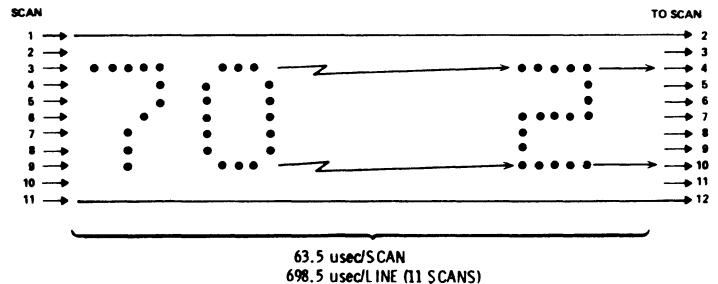


Figure 3. SCAN TIMING

PPS-8 CRT SYSTEM

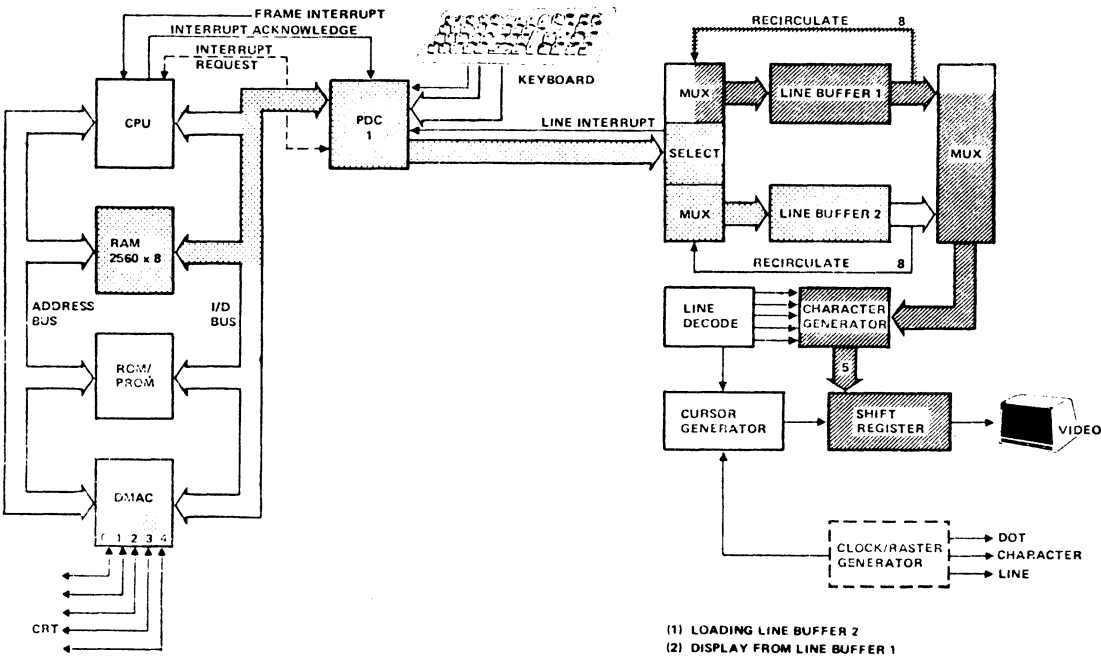


Figure 4a. PPS-8 CRT SYSTEM

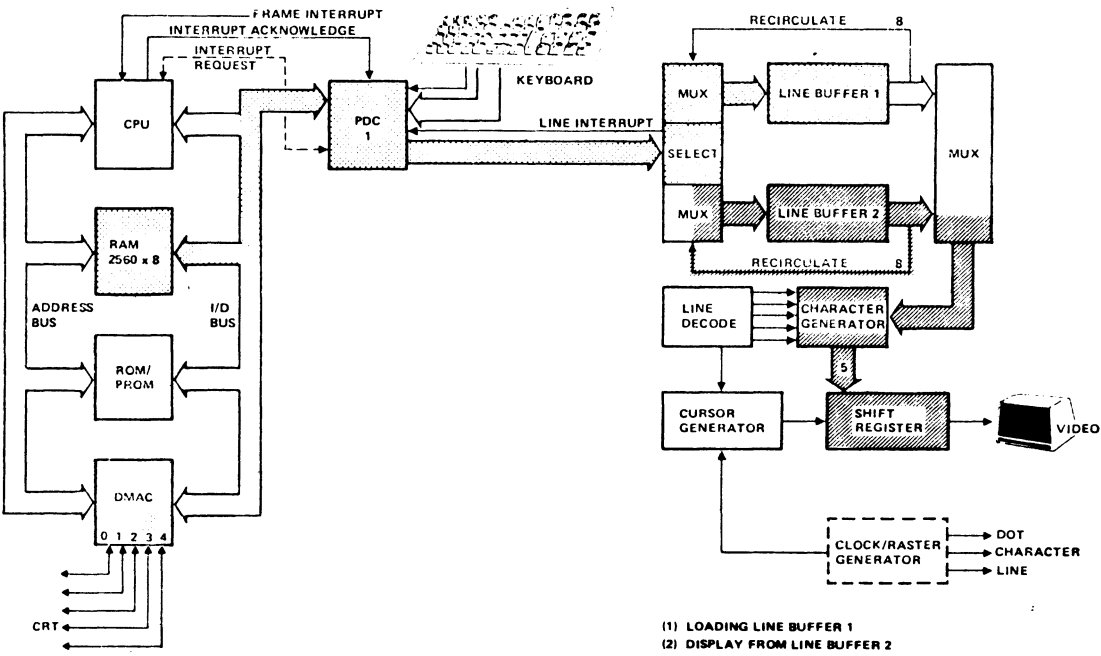


Figure 4b. PPS-8 CRT SYSTEM



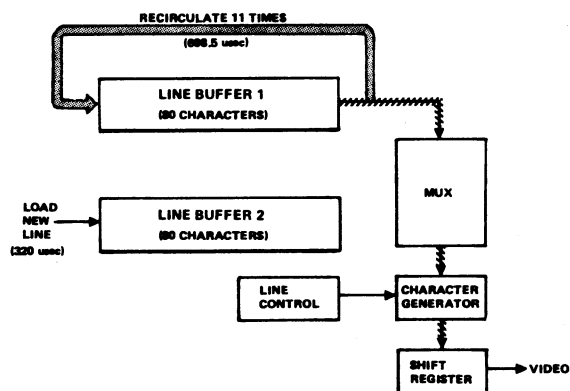


Figure 5. BUFFER TIMING

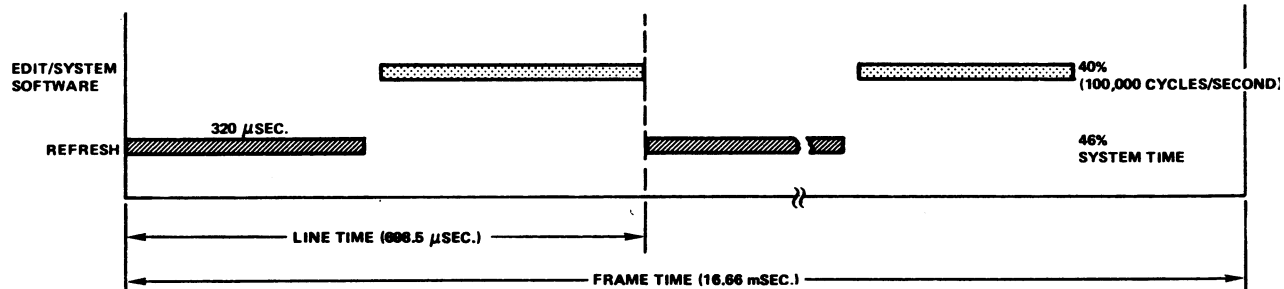


Figure 6a. BASIC SYSTEM TIMING

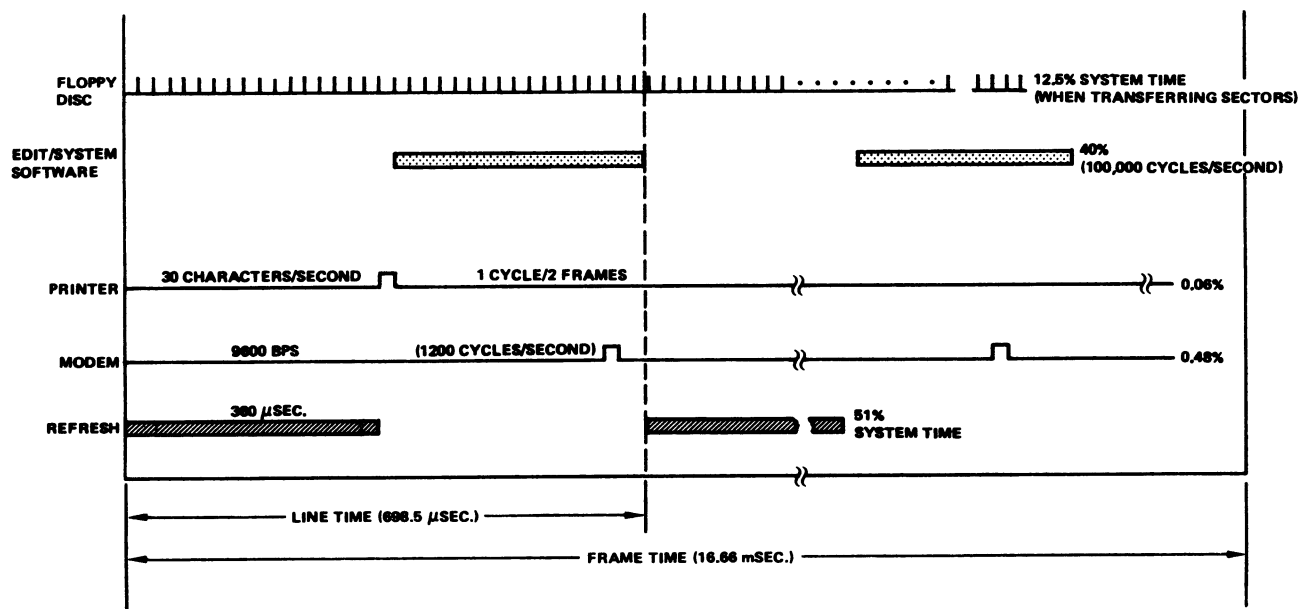


Figure 6b. EXPANDED SYSTEM TIMING

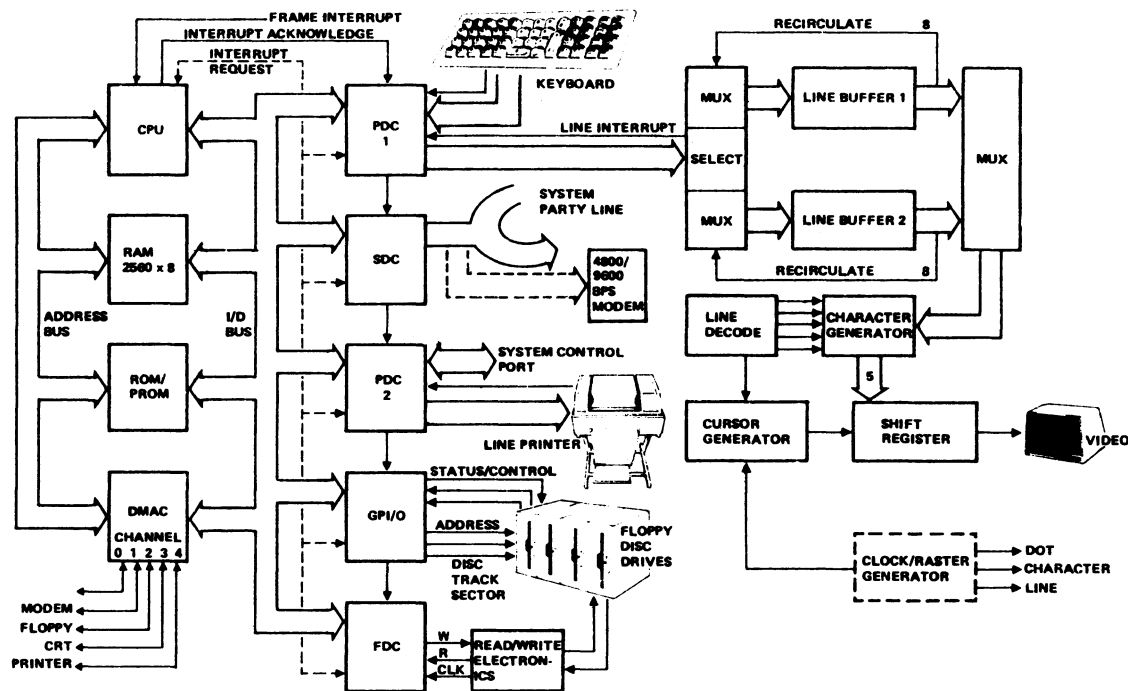


Figure 7. PPS-8 CRT EXPANDED SYSTEM

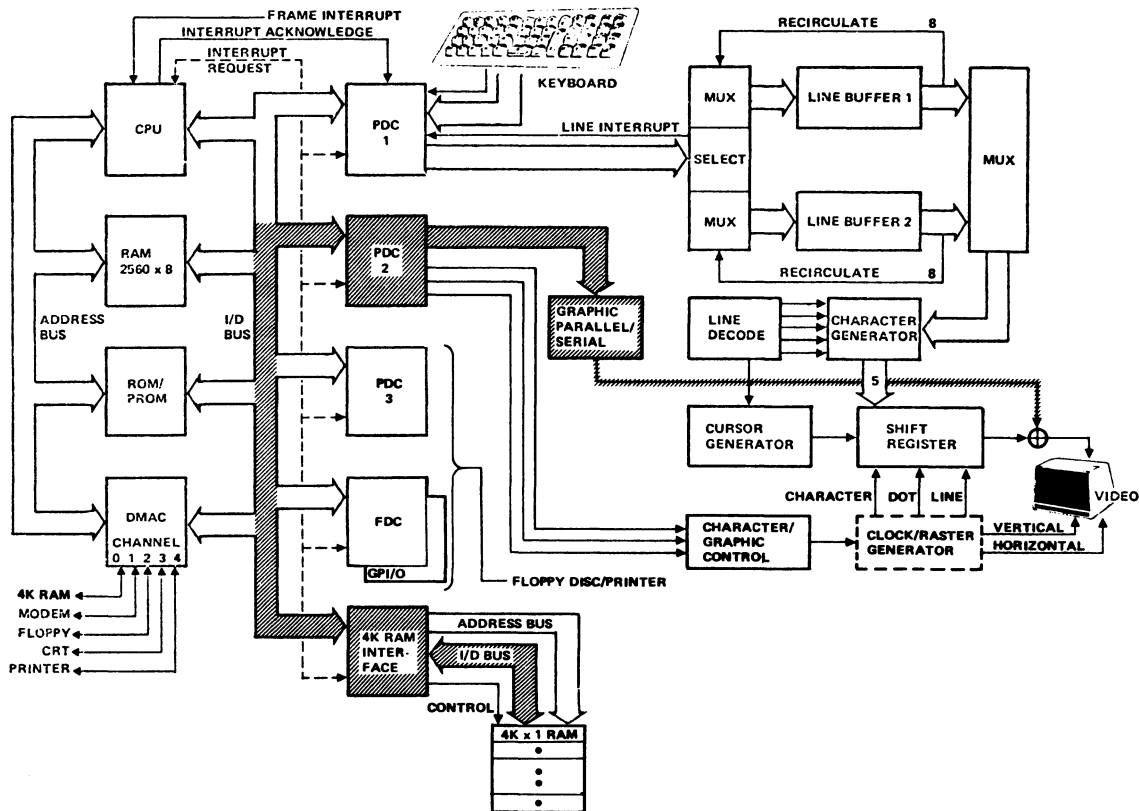


Figure 8. GRAPHIC DISPLAY CONFIGURATION

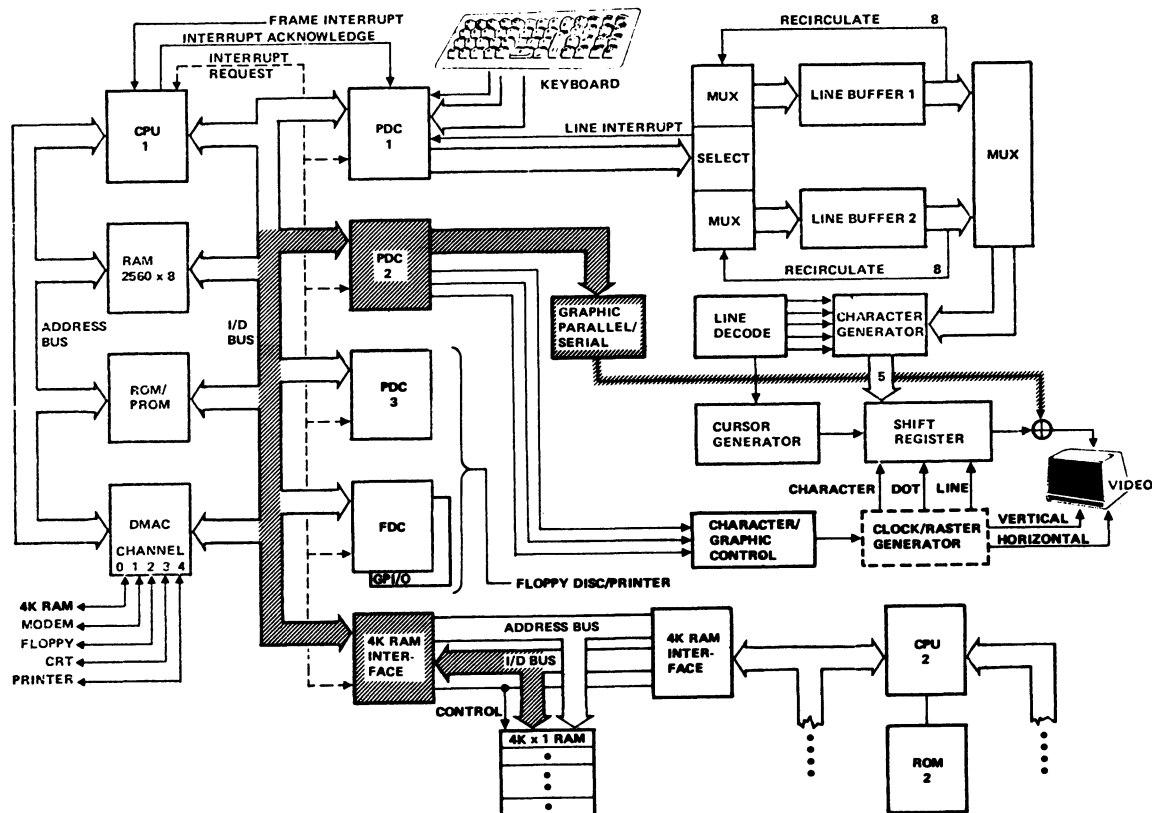


Figure 9. MULTI-PROCESSOR GRAPHIC DISPLAY

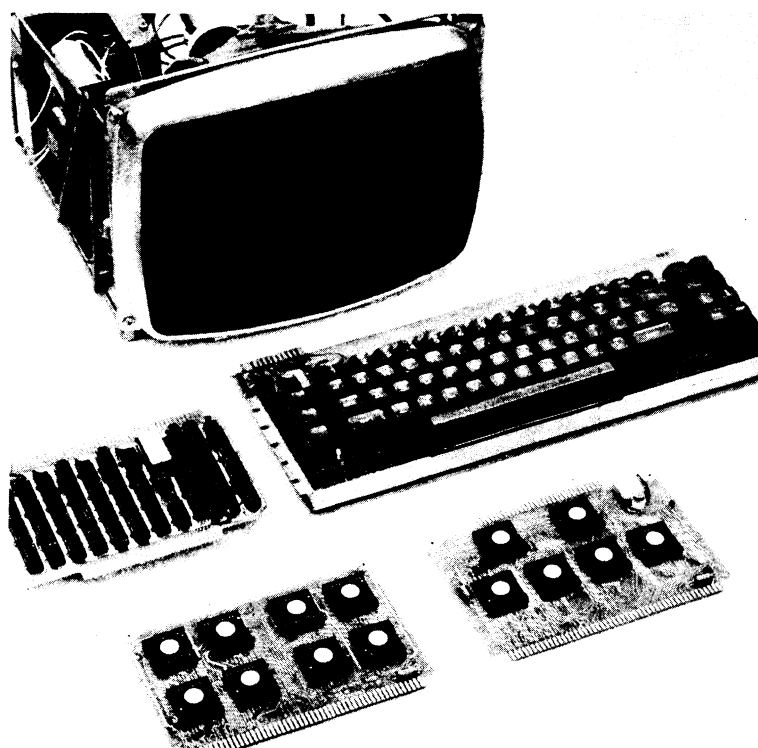


Figure 10. CRT TERMINAL HARDWARE

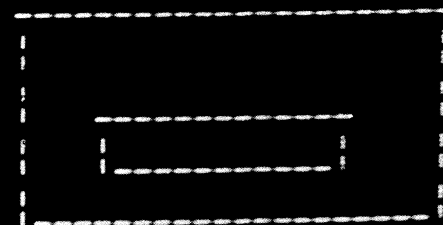
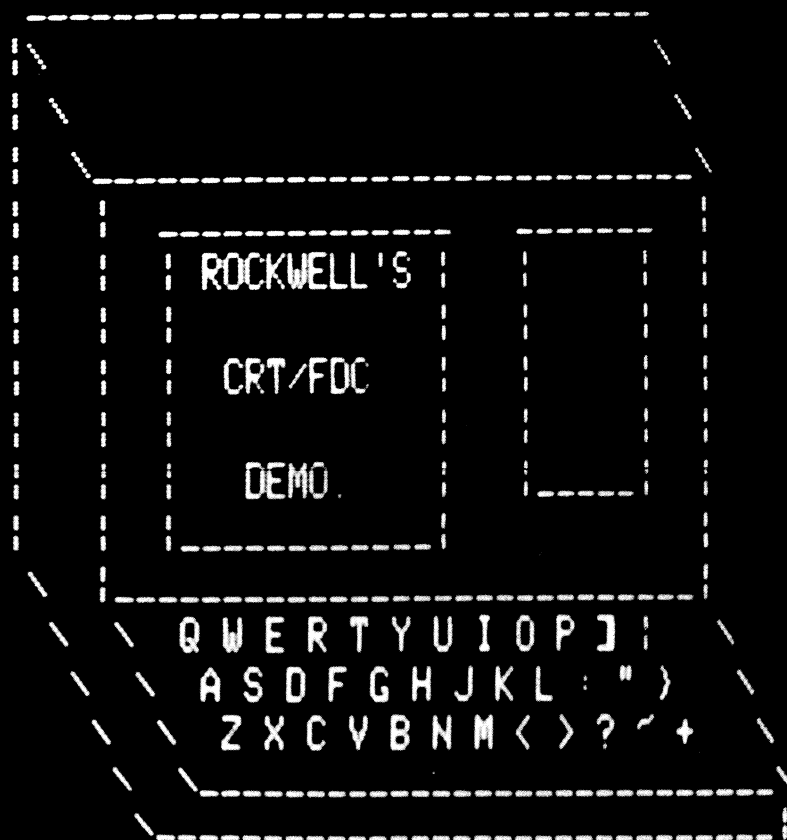


\*\*\* ROCKWELL \*\*\*ROCKWELL \*\*\* ROCKWELL \*\*\*

ROCKWELL'S

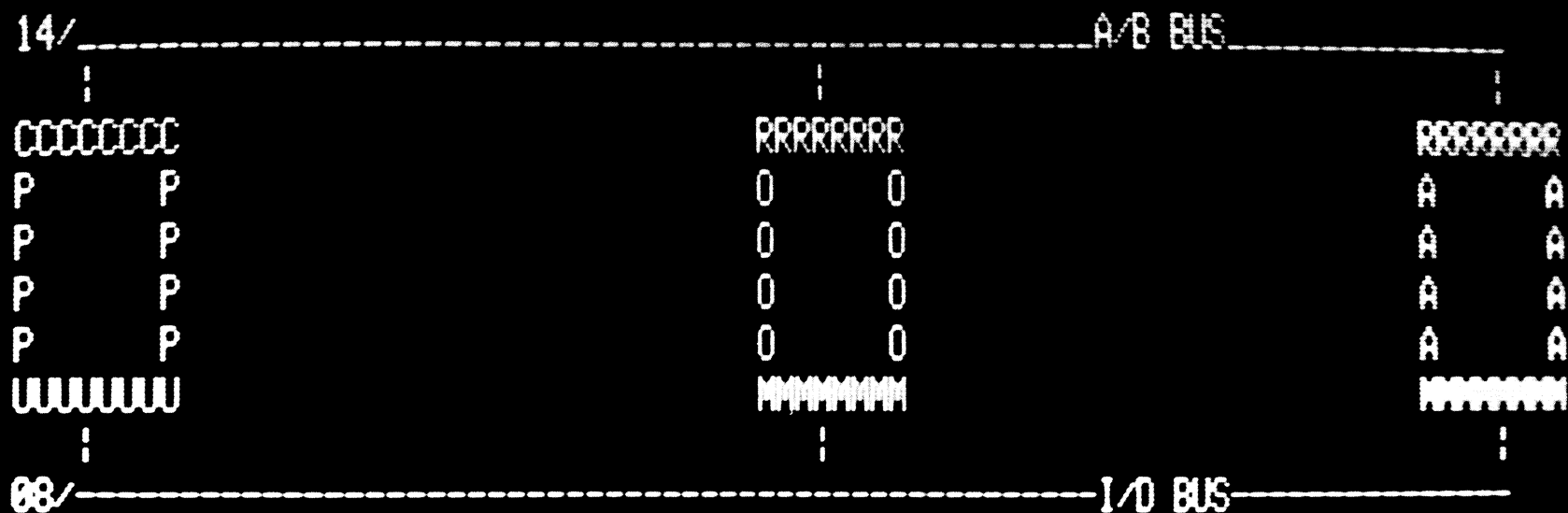
CRT / FLOPPY

DEMONSTRATOR



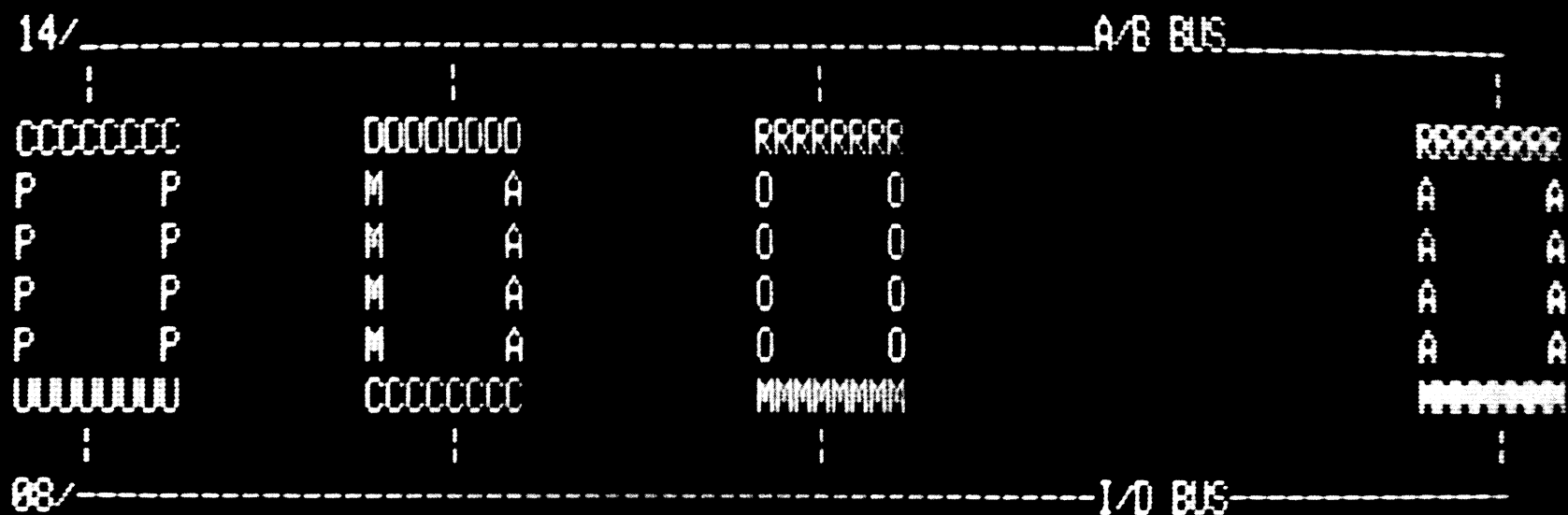
\*\*\* ROCKWELL \*\*\* TRACK 04 \*\*\* ROCKWELL \*\*\*

START WITH A PPS - 8 CPU, ROM, & RAM



\*\*\* ROCKWELL \*\*\* TRACK 05 \*\*\* ROCKWELL \*\*\*

ADD A DIRECT MEMORY ACCESS CONTROLLER ( DMAC )



\*\*\* ROCKWELL \*\*\* TRACK 06 \*\*\* ROCKWELL \*\*\*

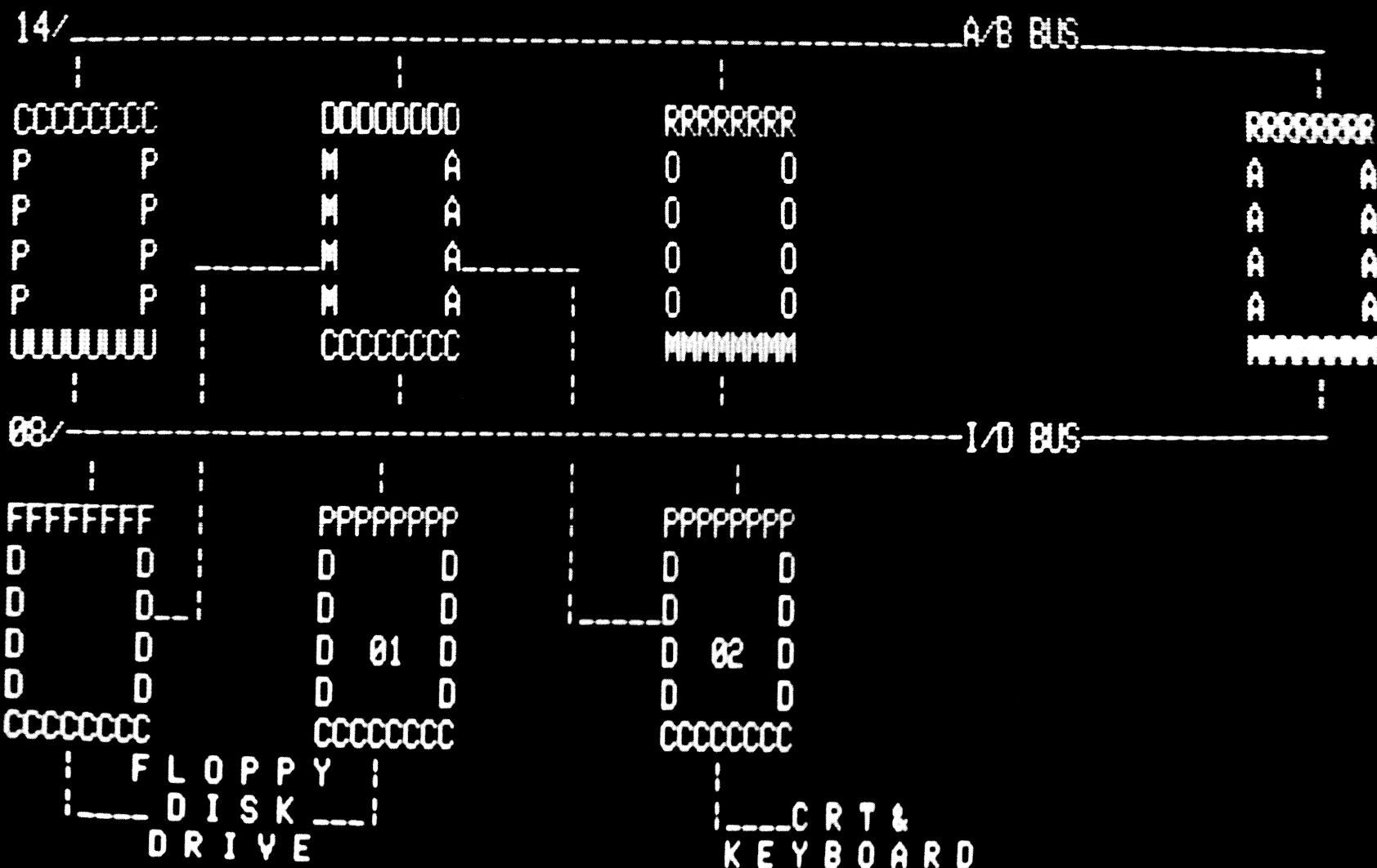
NEXT ADD A FLOPPY DISK CONTROLLER ( FDC ) AND A PARALLEL DATA CONTROLLER ( PDC )





\*\*\* ROCKWELL \*\*\* TRACK 07 \*\*\* ROCKWELL \*\*\*

THEN ANOTHER PARALLEL DATA CONTROLLER ( PDC )





PARALLEL PROCESSING SYSTEM (PPS)  
DATA SHEET

PPS-8 PROCESSOR MODULE

GENERAL DESCRIPTION

The PPS-8 Processor Module (P/N 20180 D07) is another member of the growing family of Rockwell PPS Evaluation Modules that help make design, evaluation, debug and prototype emulation of user systems employing PPS MOS/LSI devices a simple and orderly task.

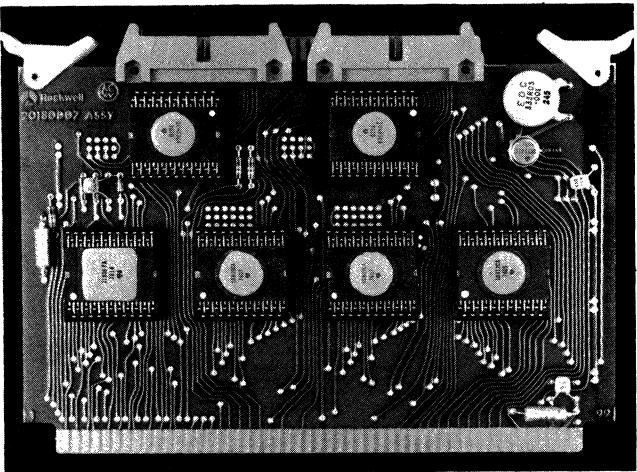
The PPS-8 Processor Module Type II consists of a 5 x 7-inch plug-in circuit card with a power-on initialization circuit, a Clock Generator device (P/N 10706) and 3.579545 MHz Crystal, a PPS-8 Central Processing Unit CPU device (P/N 11806), two PPS-8 Random Access Memories RAM devices (P/N 11809), two Parallel Data Controller PDC devices (P/N 10453), and a Direct Memory Access DMAC device (P/N 10817) all interconnected to provide the basic components of a PPS-8 system.

Any of the other PPS-8 compatible modules may be interfaced to the PPS-8 Processor Module, pin-to-pin. To facilitate this interconnection, the PPS-8 Processor Module power initialization signals (SPO and PO), clock A and B signals, address bus (A/B) lines, instruction/data bus (I/D) lines, write input/output line (W/IO), Read Inhibit (RIH), power inputs, and ground lines are accessible on a 100-pin edge connector. These pin connections are common on all PPS-8 compatible modules.

The PPS-8 Processor Module functions at either of two clock frequencies, 199 kHz or 256 kHz. The clock frequency is selected by making appropriate strap connections in the module. For a clock frequency of 199 kHz, place straps S12 and S14 at VSS and strap S18 at VDD. For a 256 kHz clock frequency, place straps S12 and S18 at VSS and S14 at VDD.

FEATURES

- Full PPS-8 compatibility allows direct interface with any other PPS-8 module.
- 8-bit Parallel CPU with bidirectional Multiplexed Instruction/Data (I/D) Bus and multiplexed Address (A/B) lines.
- Powerful 109 Instructions CPU Repertoire.
- Three level priority interrupt system.
- 8-channel Direct Memory Access Controller (DMAC) for fast data transfer.
- Complete instruction (fetch and execute) in 4  $\mu$ sec.
- 512 word (8-bit) of data storage.
- Four 8-bit I/O channels (bidirectional) with two 8-bit programmable modes.
- Direct addressing of up to 32K bytes of memory (16K ROM and 16K RAM). An additional chip select line provides direct extension to 32K ROM and 32K RAM.
- Crystal controlled system.
- 1 reference clock — TTL compatible.



PPS-8 PROCESSOR MODULE ASSEMBLY 20180D07

PPS-8 PROCESSOR MODULE ASSEMBLY 20180D07

SPECIFICATIONS

Word Size:	Instruction: 8 bits Data: 4 or 8 bits	System Clock:	Crystal controlled, 199 or 256 kHz ( $\pm 0.03\%$ ) Instruction cycle time 5 or 4 $\mu$ sec, respectively
Central Processor:	11806 CPU 8-bit data registers 14-bit address registers Subroutine nesting Interrupt Capability DMA Capability	Processor Components:	One 11806 CPU device, One 10817 DMAC device, Two 10809 RAM devices, Two 10453 PDC devices and One 10706 Clock device with crystal
Instruction Set:	109 instructions for data transfer, skip, branch, register manipulations, logical, binary and decimal arithmetic and input/output.	Board:	5 inch x 7 inch dimensions with 100-pin edge connector
Data Memory Size:	512 x 8-bit words	Edge Connector:	100-pins on 0.125 inch centers
Memory Addressing:	Up to 32K bytes of ROM and 32K bytes of RAM	Connectors Furnished:	One — 100 pin Edge Type — Female Viking — P/N 3VH50/1CND5
DMA:	8 independent DMA channels with data transfer of 250K byte/sec	Operating Temperature:	0°C to 55°C
I/O Channels:	Two sets of two 8-bit channels with two sets of 8 programmable modes. Two control lines per channel for a total of 8 that can be programmed to request interrupt service or DMA	Power Requirements:	+5V @ 135 ma -12V @ 110 ma
I/O Interface:	All I/O channels are TTL Compatible	Logic Levels:	MOS                      TTL
		H	+3.5V to +5.3V      +3.5V to +5.3V
		L (Inputs)	-2.6V to -12.85V    +0.8V to -12.85V
		L (Outputs)	-3.6V to -12.85V    -12.85V

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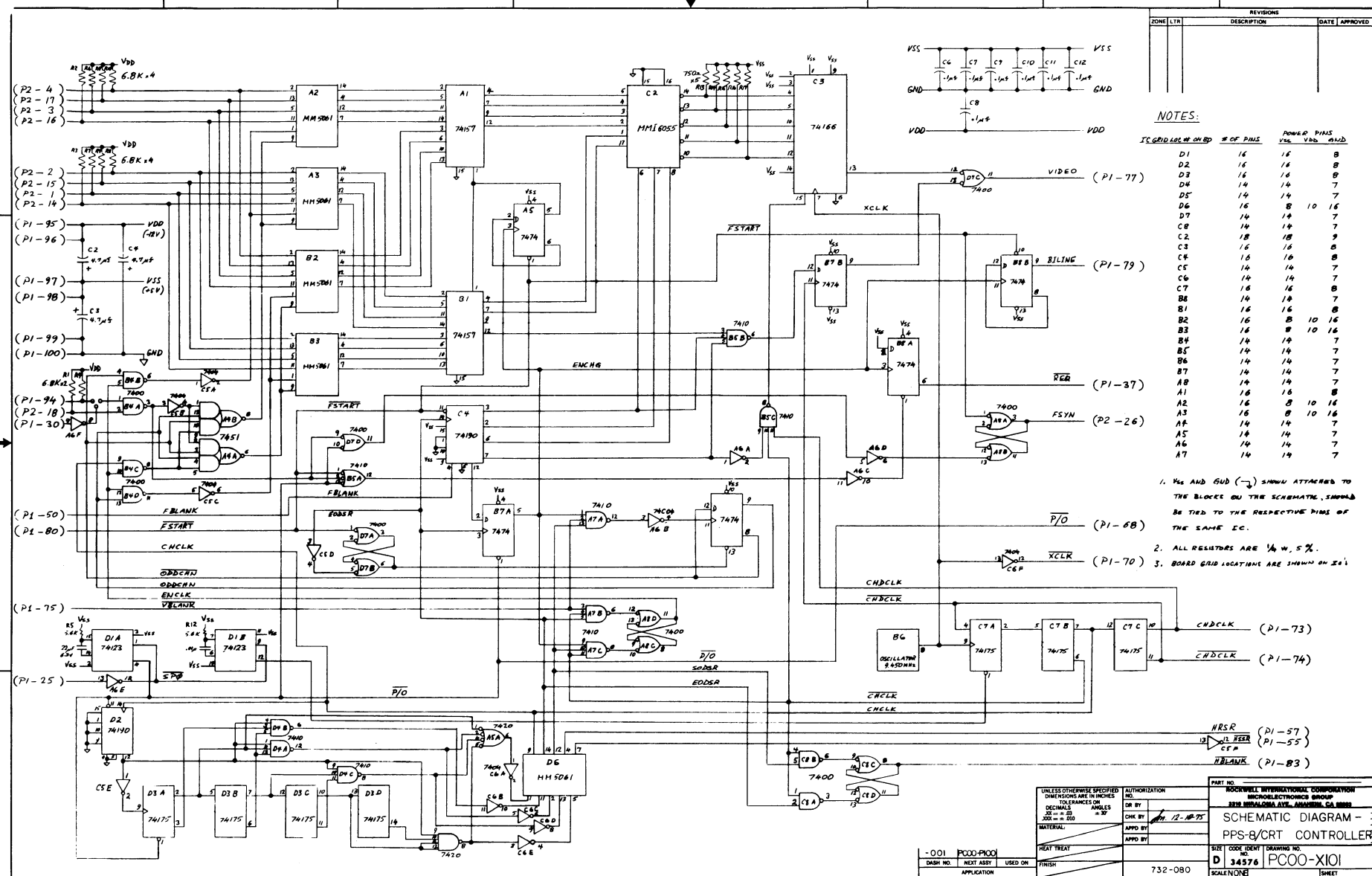
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Rockwell

PARALLEL PROCESSING SYSTEM (PPS)  
DATA SHEET

PPS-8 RAM MODULE

GENERAL DESCRIPTION

The PPS-8 RAM Module (P/N 20180 D01) is another member of the growing family of Rockwell PPS Evaluation Modules that help make design, evaluation, debug and prototype emulation of user systems employing PPS MOS/LSI devices a simple and orderly task.

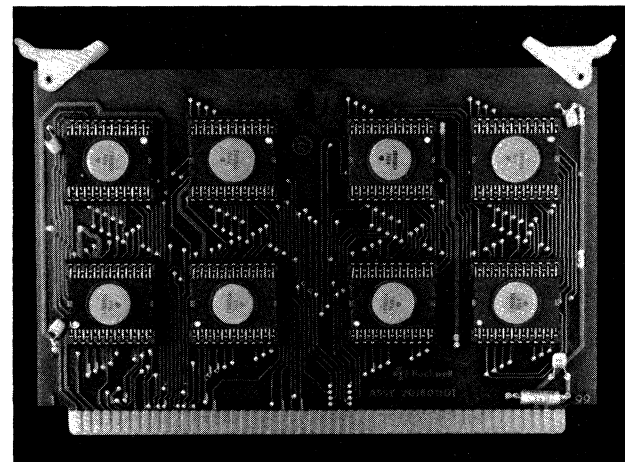
The PPS-8 RAM Module (P/N 20180 D01) is a 5 x 7-inch plug-in board which provides mounting and interface connections for up to eight RAM devices (P/N 10809). Each RAM device provides 256 x 8-bit words of memory, providing up to 2048 x 8-bit words on each RAM Module.

With external clock switching logic, the RAM may be configured for use as a writable control store. In this mode, the RAM is read during the ROM cycle.

The RAM module is functionally divided into an upper RAM bank consisting of four RAM devices and a lower RAM bank consisting of four RAM devices. The address bus (A/B1 through A/B14) and the RAM instruction/data bus (I/D1 through I/D8) are common to both banks. The device select straps SC4, SC5, SC6 and SC7 can be separated into two banks. However, the module is provided with the device select straps tied together. Bank select is provided by connecting AS7 to an I/O discrete output.

FEATURES

- Full PPS-8 compatibility allows direct interface with PPS-8 Processor Module or other PPS-8 Modules.
- 2048 x 8-bit bytes of Read/Write data storage.
- Can operate as a 2048 x 8-bit bytes of Instruction Memory.
- Expandable to 32K x 8-bit bytes of Data or Instruction Memory.



PPS-8 RAM MODULE ASSEMBLY 20180D01

PPS-8 RAM MODULE ASSEMBLY 20180D01

SPECIFICATIONS

Memory Size:	2K Bytes x 8-bits	Edge Connector:	100-pins on 0.125 inch centers
Word Length:	8-bits	Connectors Furnished:	One 100-pin edge type — Female Viking — P/N 3VH50/1CND5
Capacity:	256 to 2048 bytes in 256 byte increments	Operating Temperature:	0°C to 55°C
Memory Expansion:	Up to 32K x 8-bit bytes expandable in 2K bytes	Power Requirements:	+5V @ 110 ma -12V @ 90 ma
Interface:	PPS-8 Compatible	Logic Levels:	MOS
Performance:	1.8 $\mu$ sec access time. Automatic refresh	H	+3.5V to +5.3V
System Clock:	199 or 256 kHz ( $\pm$ 0.03%)	L (Inputs)	-2.6V to -12.85V
Module Components:	Eight 10809 RAM devices	L (Outputs)	-3.6V to -12.85V
Board:	5 inch x 7 inch dimensions with 100-pin edge connector		

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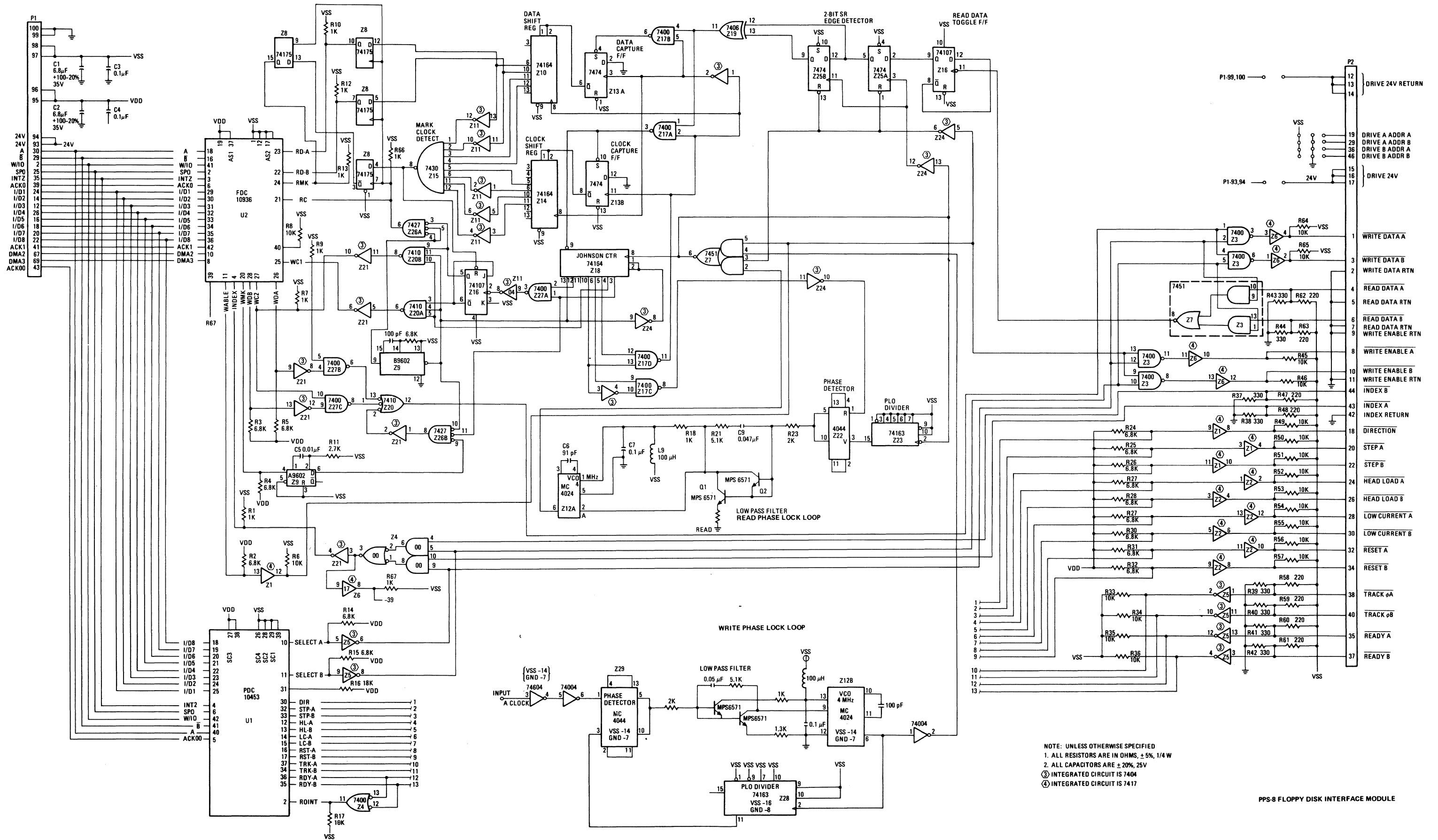
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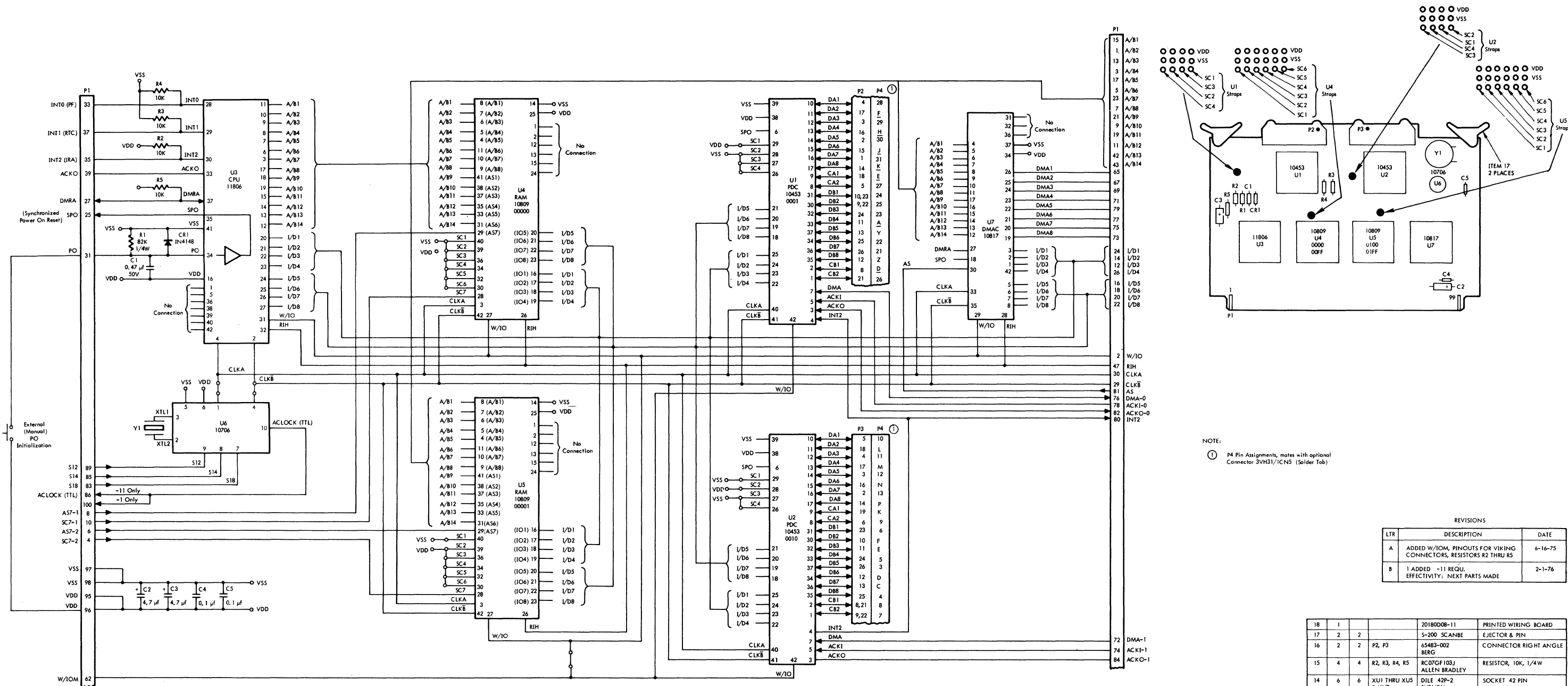
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PPS-8 FLOPPY DISK INTERFACE MODULE



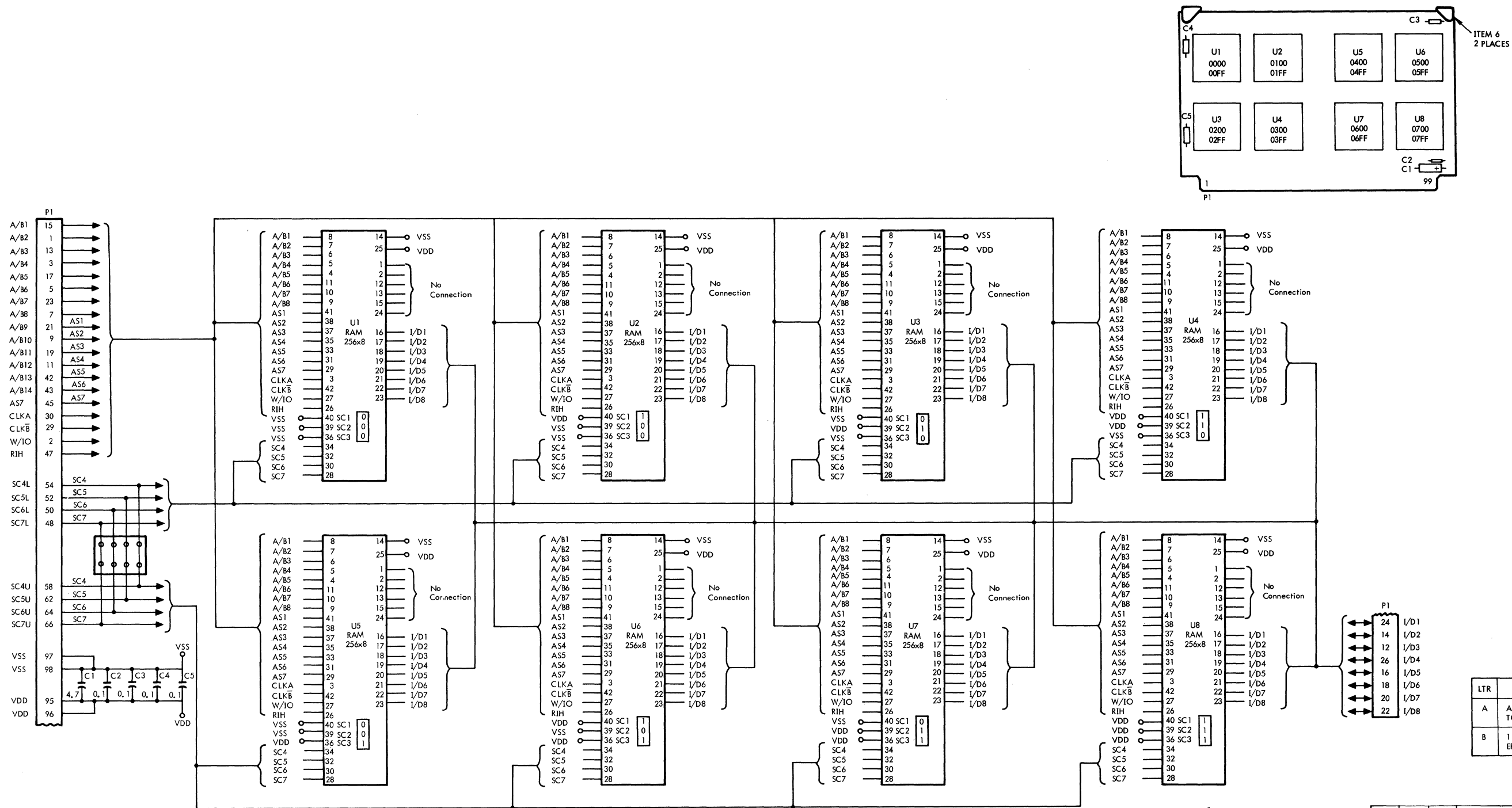
NOTE:  
① P4 Pin Assignments, mates with optional Connector 3VH51/1CN5 (Solder Tab)

REVISIONS		
LTR	DESCRIPTION	DATE
A	ADDED W/10M, PINOUTS FOR VIKING CONNECTORS, RESISTORS R2 THRU R5	6-16-75
B	1 ADDED -11 REQU. EFFECTIVITY: NEXT PARTS MADE	2-1-76

ITEM NO.	QTY REQD	QTY REQD	REFERENCE DESIGNATION	PART OR IDENTIFYING NO.	NOMENCLATURE
18	1			20180D08-11	PRINTED WIRING BOARD
17	2	2		S-200 SCANBE	EJECTOR & PIN
16	2	2	P2, P3	65483-002 BERG	CONNECTOR RIGHT ANGLE
15	4	4	R2, R3, R4, R5	RC07GF103J ALLEN BRADLEY	RESISTOR, 10K, 1/4W
14	6	6	XU1 THRU XU5 & XU7	DILE 42P-2 BURNDY	SOCKET 42 PIN
13	2	2	C4, C5	8121-050-651-104M ERIE	CAPACITOR, 0.1 uF, 50V
12	2	2	C2, C3	150D685X9035B2 SPRAGUE	CAPACITOR, 6.8 uF, 35V
11	1	1	C1	8131-050-651-474M ERIE	CAPACITOR, 0.47 uF, 50V
10	1	1	Y1	333805-001 ELECTRO-DYN	CRYSTAL, 3579.545 KC
9	1	1	CR1	1N4148 MOTOROLA	DIODE
8	1	1	R1	RC07GF823J ALLEN BRADLEY	RESISTOR, 82K, 1/4W
7	1	1	U6	10706	MOS, CLOCK
6	1	1	U7	10817	MOS, DMAC
5	1	1	U2	10453	MOS, PDC
4	1	1	U1	10453	MOS, PDC
3	2	2	U4, U5	10809	MOS, RAM
2	1	1	U3	11806	MOS, CPU
1	1	1		20180D08-1	PRINTED WIRING BOARD
-	-11	-1		20180D07-1, -11	ASSEMBLY

PARTS LIST

PPS-8 Processor Module Wiring Diagram

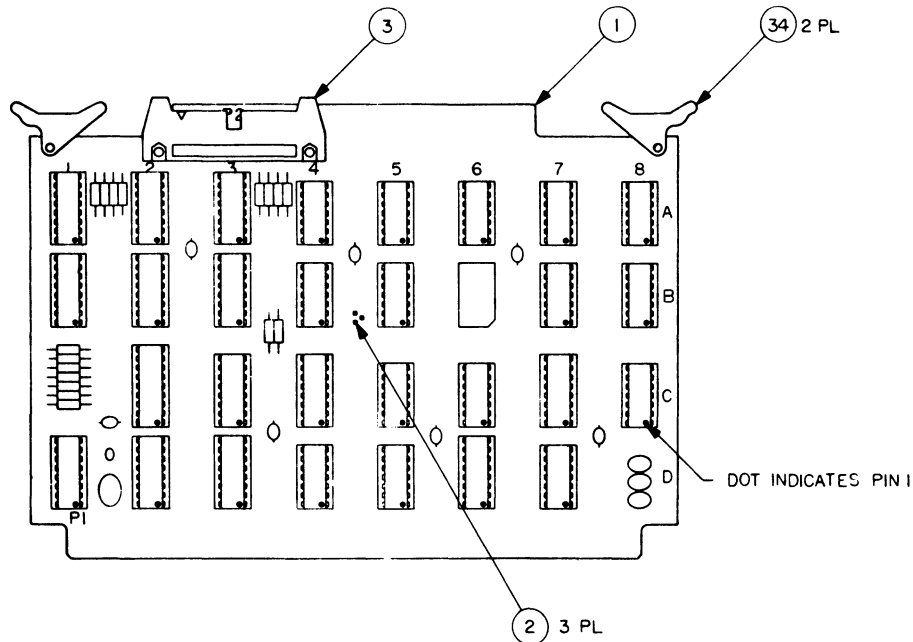


REVISIONS		
LTR	DESCRIPTION	DATE
A	ADDED HEXADECIMAL ADDRESS RANGES TO ASSEMBLY DRAWING	
B	1 ADDED -11 REQU EFFECTIVITY NEXT PARTS MADE	2-1-76

7	1			20180D02-11	PRINTED WIRING BOARD
6	2	2		S-200 SCANBE	EJECTOR & PIN
5	8	8	XU1 THRU XU8	DILE 42 P-2 BURNDY	SOCKET 42 PIN
4	1	1	C1	150D685X903582 SPRAGUE	CAPACITOR, 6.8 uf, 35V
3	4	4	C2 THRU C5	8121-050-651-104M ERIE	CAPACITOR, 0.1 uf, 50V
2	8	8	U1 THRU U8	10809	RAM
1		1		20180D02-1	PRINTED WIRING BOARD
-	-11	-1		20180D01-1,-11	ASSEMBLY
ITEM NO.	QTY REQD	QTY REQD	REFERENCE DESIGNATION	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

PPS-8 RAM Module Wiring Diagram



REVISIONS			
ZONE	LTR	DESCRIPTION	DATE

- NOTE: UNLESS OTHERWISE SPECIFIED
1. ASSEMBLE PER SPECIFICATION 19073A11
  2. REF SCHEMATIC PC00-X101
  3. INSTALL DIP SOCKETS WITH ORIENTATION SLOT DOWN

# COMPONENT PLACEMENT CHART

P-PL	ITEM NO.	COMPONENT TYPE	LOCATION OR REF DESIG
	4	SOCKET	C2
	5	SOCKET	A1 A2 A3 B1 B2 B3 C3 C4 C7 D1 D2 D3 D6
	6	SOCKET	A4 A5 A6 A7 A8 B4 B5 B6 B7 B8 C5 C6 C8 D4 D5 D7
	8	OSC	B6
	9	IC	C2
	10		A2 A3 B2 B3 B6
	11		C4 D2
	12		C7 D3
	13		C3
	14		A1 B1
	15		D1
	16		A5 B7 B8
	17		A4
	18		D5
	19		A7 B5 D4
	20		A6
	21		C5 C6
	22	IC	A8 B4 C8 D7
	24	CAPACITOR	C5
	25		C6 C7 C8 C9 C10 C11 C12
	26		C1
	27	CAPACITOR	C2 C3 C4
	30	RESISTOR	R13 R14 R15 R16 R17
	31	RESISTOR	R5 R12
	32	RESISTOR	R1 R2 R3 R4 R6 R7 R8 R9 R10 R11

SEE SEPARATE PARTS LIST PC00-L100

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		AUTHORIZATION NO.		PART NO. PC00-D100-001	
DECIMALS .XX = .03 .XXX = .010	TOLERANCES ON ANGLES ± 30°	DR BY FM CASTER	CHK BY	ROCKWELL INTERNATIONAL CORPORATION MICROELECTRONICS GROUP 3310 MIRALOMA AVE., ANAHEIM, CA 92805	
MATERIAL:		APPD BY	APPD BY	PPS-8/CRT CONTROLLER	
HEAT-TREAT		7.32.080	7.32.080	SIZE 1 CODE IDENT DRAWING NO. C 34576 PC00-D100	
DASH NO.	NEXT ASSY	USED ON	APPLICATION	SHEET	

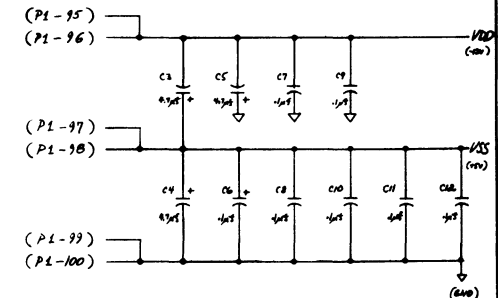


REVISIONS		DATE	APPROVED
ZONE	LTR		

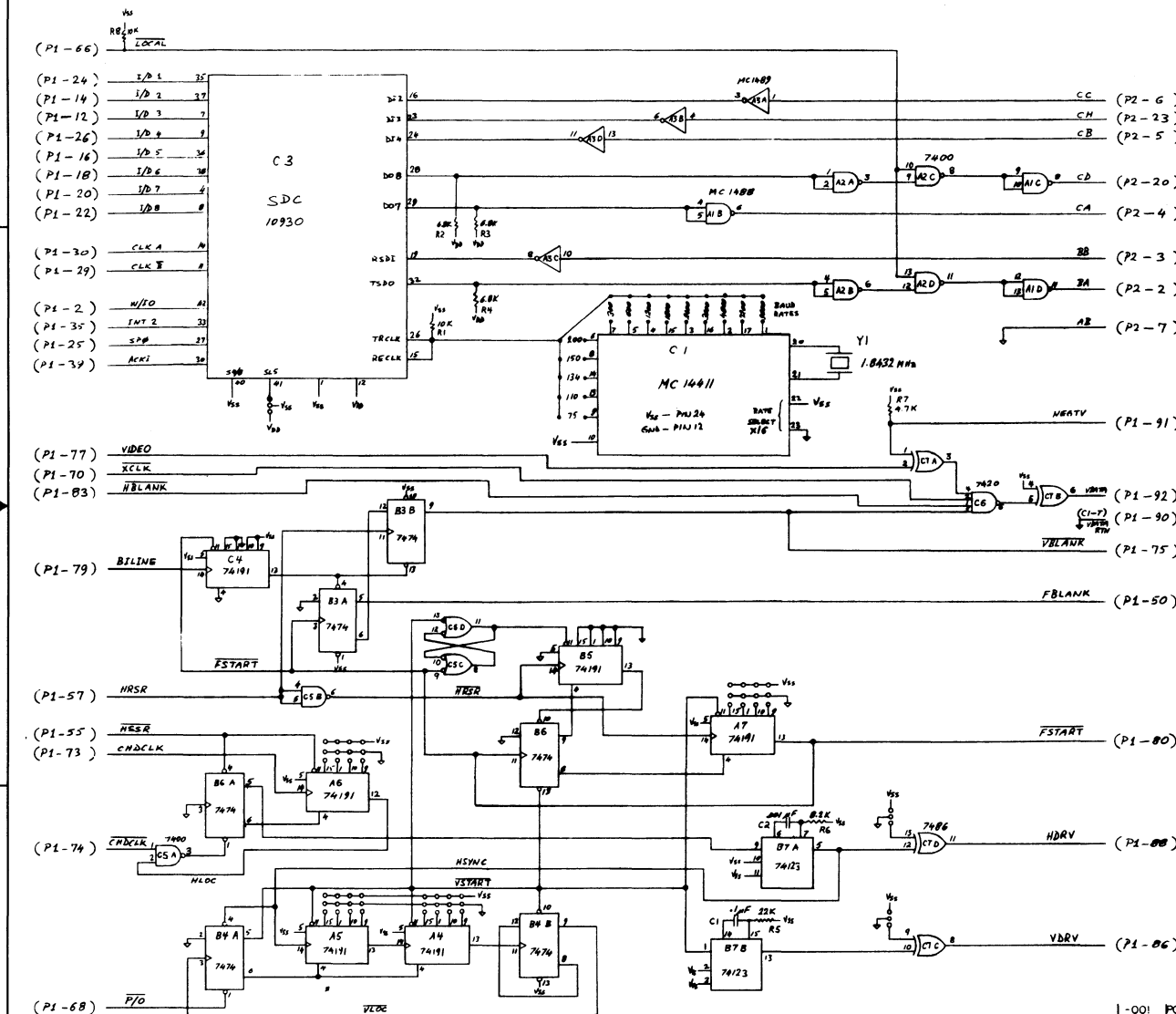
# NOTES

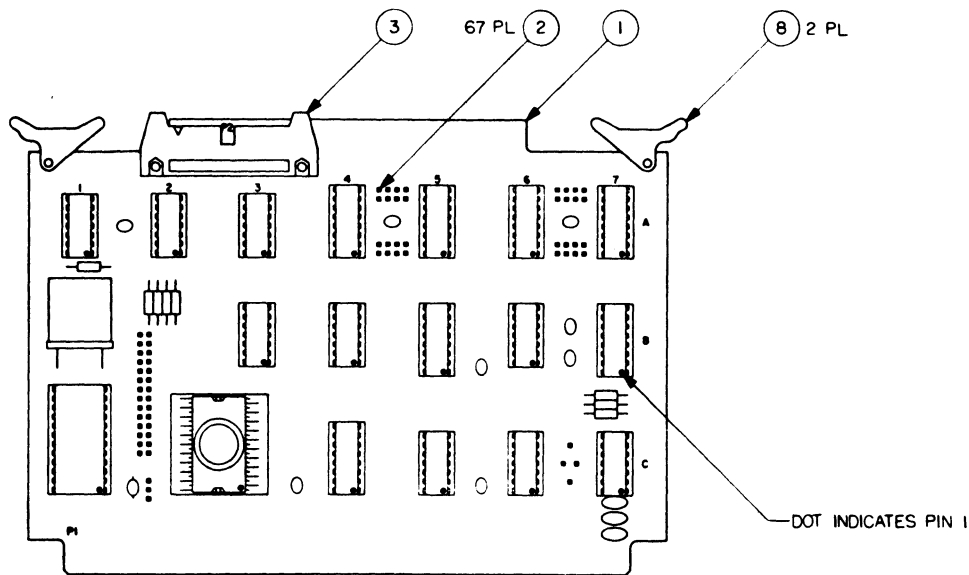
JC #	# OF PINS	V <sub>CC</sub>	V <sub>BA</sub>	GND
1	24	24	12	12
2	42	1	12	—
3	16	16	8	8
4	14	14	7	7
5	14	14	7	7
6	16	16	8	8
7	2	—	—	—
8	14	14	7	7
9	14	14	7	7
10	16	16	8	8
11	16	16	8	8
12	14	14	7	7
13	14	14	7	7
14	16	16	8	8
15	14	14	7	7
16	16	16	8	8
17	14	14	7	7
18	16	16	8	8
19	14	14	7	7

1. V<sub>CC</sub> AND GND (—) SYMBOL ATTACHED TO THE BLOCKS ON THE SCHEMATIC, SHOULD BE TIED TO THE RESPECTIVE PINS OF THE SAME IC.
2. ALL RESISTORS ARE 1/8 W. 5%.
3. BOARD GRID LOCATIONS ARE SHOWN ON IC'S



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS INCHES FRACTIONS MATERIAL HEAT TREAT		AUTHORIZATION NO. CHK BY DATE APPRO BY DATE		PART NO. ROCKWELL INTERNATIONAL CORPORATION 3525 BIRLAHARA AVE. AMARSELA, CA 94501 SCHEMATIC DIAGRAM - PPS-8/CRT DRIVER SUN CODE ONLY DRAWING NO. D 34376 SCALE: 1/8"=1"	
-001 PC00-010		732-080		PC00-XIII	
DASH NO.		NEXT ASST		USED ON	
APPLICATION		FINISH		SHEET	





REVISIONS			
ZONE/LTR	DESCRIPTION	DATE	APPROVED

COMPONENT PLACEMENT CHART

PL ITEM NO.	COMPONENT TYPE	LOCATION OR REF DESIG
4	SOCKET	C3
5		C1
6		A4 A5 A6 A7 B5 B7 C4
7	SOCKET	A1 A2 A3 B3 B4 B6 C5 C6 C7
10	IC	C3
11		C1
12		A3
13		A1
14		A4 A5 A6 A7 B5 C4
15		B7
16		C7
17		B3 B4 B6
18		C6
19	IC	A2 C5
21	CAPACITOR	C2
22		C9
23		C1 C6 C7 C8 C10 C11 C12
24	CAPACITOR	C3 C4 C5
26	RESISTOR	R1 R8
27		R2 R3 R4
28		R5
29		R6
30	RESISTOR	R7
32	CRYSTAL	Y1

- NOTE UNLESS OTHERWISE SPECIFIED  
 1. ASSEMBLE PER SPECIFICATION 19073A11  
 2. REF SCHEMATIC PC00-XIII  
 3. INSTALL IC SOCKETS WITH ORIENTATION SLOT DOWN

SEE SEPARATE PARTS LIST PC00-L110		PART NO. PC00-D110-001	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS XX = ± .03 XXX = ± .010		AUTHORIZATION NO. DR BY FM CASTER CHK BY APPD BY HEAT TREAT FINISH	
MATERIAL:		ROCKWELL INTERNATIONAL CORPORATION MICROELECTRONICS GROUP 3310 MIRALOMA AVE., ANAHEIM, CA 92803	
SIZE		PPS-8/CRT DRIVER	
DASH NO.		CODE IDENT NO. C 34576	
NEXT ASSY		DRAWING NO. PC00-D110	
USED ON		SCALE NONE SHEET	
APPLICATION		732-080	

PC00-D110

7/12

ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)

( 1 )

ROM	..CODE..	ARG	STMT	SOURCE STATEMENTS
ADDR	11 12 13		NUMBER	

```

4 .....
5 .
6 .
7 .
8 .
9 .      R O C K W E L L
10 .
11 .     P A R A L L E L   P R O C E S S I N G   S Y S T E M   ( P P S )
12 .
13 .
14 .     C R T / F D C   D E M O N S T R A T O R
15 .
16 .
17 .
18 .     P P S - 8   P R O G R A M   L I S T I N G
19 .
20 .     C O R R E S P O N D I N G   T O   T H E   R O M S
21 .
22 .     A 6 6 1 1           4 K   B Y T E   R O M
23 .
24 .
25 .           A N D
26 .
27 .     A 5 2 H 0           2 K   B Y T E   R O M
28 .
29 .     A 5 2 H 1           2 K   B Y T E   R O M
30 .
31 .
32 .     R O C K W E L L   I N T E R N A T I O N A L
33 .     M I C R O E L E C T R O N I C   D E V I C E   D I V I S I O N
34 .     A U G U S T   1 9 ,   1 9 7 6
35 .
36 .....

```

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ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)

( 2 )

ROM	..CODE..	ARG	STMT	SOURCE STATEMENTS
ADDR	11 12 13		NUMBER	

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ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 3 )

ROM	..CODE..	ARG	STMT	SOURCE STATEMENTS
ADDR	I1 I2 I3		NUMBER	

```

40 .....
41 .....
42 .....
43 .....
44 .....
45 .....
46 .....
47 .....
48 .....
49 .....
50 .....
51 .....
52 .....
53 .....
54 .....
55 .....
56 .....
57 .....
58 .....
59 .....
60 .....
61 .....
62 .....
63 .....
64 .....
65 .....
66 .....
67 .....
68 .....
69 .....

```

SECTION 1

POOL/EQUATES/RAM

THE FOLLOWING PAGES CONTAIN THE POOL DEFINITIONS, EQUATE STATEMENTS ASSIGNING VALUES TO VARIOUS PROGRAM SYMBOLS, AND ASSIGNMENTS OF RAM LOCATIONS TO THEIR SYMBOLIC NAMES.

THESE DEFINITIONS ARE USED BY BOTH THE CRT AND THE FLOPPY DISK ROUTINES.

ROCKWELL INTERNATIONAL  
MICROELECTRONIC DEVICE DIVISION  
AUGUST 19, 1976

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ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 4 )

ROM	..CODE..	ARG	STMT	SOURCE STATEMENTS
ADDR	I1 I2 I3		NUMBER	

94(04)	0001	71	POOL
85(05)	0002	72	SB 1
88(08)	0003	73	SB 2
89(09)	0004	74	SB 3
8C(0C)	0005	75	SB 4
9D(0D)	0006	76	SB 5
90(10)	0007	77	SB 6
91(11)	0008	78	SB 7
94(14)	0001	79	SB 8
95(15)	0002	80	RB 1
98(18)	0003	81	RB 2
99(19)	0004	82	RB 3
9C(1C)	0005	83	RB 4
9D(1D)	0006	84	RB 5
A0(20)	0007	85	RB 6
A1(21)	0008	86	RB 7
86(06)		87	RB 8
87(07)		88	LAI
8A(0A)		89	LAI\$
8B(0B)		90	LXI
8E(0E)		91	LXI\$
8F(0F)		92	LYI
92(12)		93	LYI\$
93(13)		94	LZI
97(17)		95	LZI\$
98(18)		96	PSHA
9F(1F)		97	PSHX
A3(23)		98	PSHY
96(16)		99	PSHZ
9A(1A)		100	PUPA
9E(1E)		101	PUPA\$
A2(22)		102	POPX
A6(26)		103	POPX\$
AA(2A)		104	POPY
AE(2E)		105	POPY\$
B2(32)		106	POPZ
A4(24)		107	POPZ\$
		108	ANI

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ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 5)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
	A5(25)		109	AISK
	A7(27)		110	AISKs
	A8(28)		111	LAL
	A9(29)		112	LXL
	AA(2H)		113	LYL
	AC(2C)		114	LZL
	AD(2D 70)	0000	115	LAI #00
	AF(2F 71)	00FF	116	LAI #FF
	00(30 40)	0080	117	LXI #80
	31(31 41)	0029	118	LXI CURS+1
	33(33 42)	0021	119	LXI FLAG
	44(34 43)	0020	120	LXI KEY
	45(35 44)	002A	121	LXI LINE
	46(36 45)	0030	122	LXI TRK
	47(37 60)	0001	123	LZI 1
	48(38 72)	0020	124	ANI #20
	49(39 61)	0001	125	AISK #01
	4A(3A 62)	0040	126	AISK 128
	4B(3B 63)	FFFF	127	AISK -1
	E0(80 A0)	1000	128	BL INT0
	F1(41 A1)	0150	129	BL INT1
	E2(82 A2)	0480	130	BL INT2
	E3(83 A3)	0300	131	BL INCZ
	E4(84 A4)	031F	132	RL DECZ
	E5(85 A5)	032E	133	RL IN80
	E6(86 A6)	0339	134	RL DE80
	E7(87 A7)	0380	135	RL INCL
	E8(88 A8)	03bC	136	BL DECL
	E9(89 A9)	030A	137	BL INZS
	EA(8A AA)	032A	138	BL DEZS
	EB(8B AB)	0392	139	RL CLIN
	EC(8C AC)	034E	140	RL LLIN
	ED(8D AD)	03A6	141	BL CLST
	EE(8E AE)	0384	142	RL RLC
	EF(8F AF)	03C0	143	RL DPC
	F0(90 B0)	03C7	144	RL RLKS
	F1(91 B1)	03DC	145	RL RLK1
	F2(92 B2)	03DF	146	RL RLK1

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ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 6)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
	F3(93 B3)	0003	147	BL ENBL
	F4(94 B4)	0382	148	BL LDC
	F5(95 B5)	0287	149	RL .CL
	F6(96 B6)	0316	150	BL DLY
	F7(97 B7)	030E	151	BL .INZ
	FA(98 B8)	01EE	152	BL MOD2
	F9(99 B9)	042E	153	RL SET
	FA(9A BA)	07DC	154	BL SNE
	FB(9B BB)	0404	155	RL STEP
	FC(9C BC)	0537	156	RL VDEL
	FD(9D BD)	02F1	157	BL EXIP
	FE(9E BE)	01A5	158	RL HTBL
	FF(9F BF)	0492	159	RL WFDU
			160	PEND
		1000	161	INT0 EQU #1000 USE INT0 TO GET TO FIRST LOC OF 2ND 4K

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 7 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
			163	**** DEVICE ASSIGNMENTS
0007	165	D1	EQU #07	PDC - CRT REFRESH
0008	166	D2	EQU #08	PDC - KEYBOARD
0004	167	PDCF	EQU #04	PDC - DISK DRIVE SELECT/CONTROL
0005	168	FDC	EQU #05	FLOPPY DISK CONTROLLER
000C	169	SDC	EQU #C	SERIAL DATA CONTROLLER
	170	*	D08	DATA TERMINAL READY
	171	*	D07	REQUEST TO SEND
	172	*	D14	CLEAR TO SEND
	173	*	D13	NOT USED
	174	*	D12	DATASET READY
	176			**** DMAC CHANNEL ASSIGNMENTS ****
0001	177	DCF	EQU #01	FDC FORMAT
0002	178	DCD	EQU #02	FDC DATA
0003	179	DCC	EQU #03	CRT
0007	180	DCR	EQU #07	FDC REFRESH
	182			**** FDC COMMANDS ****
0001	183	FST	EQU #01	FDC START
0002	184	FLD	EQU #02	FDC LOAD
0003	185	FCL	EQU #03	FDC CLEAR
0004	186	FRS	EQU #04	FDC READ STATUS
	188			**** FDC COMMAND BYTES
0010	189	%I	EQU #10	IDLE
0002	190	%RS	EQU #02	READ SECTOR
0004	191	%WS	EQU #04	WRITE SECTOR
0006	192	%RC	EQU #06	READ COMPARE
0014	193	%FW	EQU #18	FORMAT WHITE
000A	194	%RID	EQU #0A	READ ID
000E	195	%CRC	EQU #0E	READ CRC
	197			** COMMAND CODES **
0003	198	RSET	EQU 0	
0007	199	CLK0	EQU 7	
0003	200	CLK1	EQU 3	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 8 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
00C0	201	HOUT	EQU #C6	HANDSHAKE OUT,DMA,EOH
0001	202	SIN	EQU 0	PDC-STATIC IN
0004	203	SOUT	EQU 4	
0001	204	SIO	EQU 1	
0005	205	LAHL	EQU 5	
0006	206	LARU	EQU 6	
0007	207	LRLR	EQU 7	
0007	208	RHR	EQU #07	
0007	209	LFA	EQU 2	
0003	210	LFB	EQU 3	
0009	211	RBA	EQU 9	
000A	212	RBH	EQU 10	
0003	213	LBA	EQU 0	
0001	214	LHB	EQU 1	
0003	215	RSR	EQU 3	PDC-READ STATUS REGISTER
0001	216	LTH	EQU 1	
0002	217	LC	EQU 2	
0003	218	LF1	EQU 3	
0004	219	LF2	EQU 4	
0000	220	RRH	EQU 0	
0006	221	RS12	EQU 6	
0007	222	SIDL1	EQU #07	
0000	223	SIDL2	EQU 0	
0040	224	R0ST	EQU #40	SDC-REQUEST TO SEND
0080	225	NRDY	EQU #80	SDC-RESET RTS AND READY
00C0	226	NRDX	EQU #C0	SDC-SET RTS , RESET READY
0005	227	R0S3	EQU 5	SDC-READ QUALITY REGISTER AND STATUS
00C4	228	R0SX	EQU #C4	SDC-SET RTS AND ENABLE TRANSMITTER
	230			** CONSTANTS
000A	231	.LF.	EQU #A	
0000	232	.CR.	EQU #0	
0020	233	BLNK	EQU #20	ASCII BLANK
0041	234	.A.	EQU #41	
0043	235	.C.	EQU #43	
0044	236	.D.	EQU #44	
0045	237	.E.	EQU #45	
0046	238	.F.	EQU #46	

REG.3

DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 9)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
0047			239	.G. EQU #47	
0048			240	.H. EQU #48	ASCII M
0049			241	.I. EQU #49	
004A			242	.J. EQU #4A	
004B			243	.K. EQU #4B	
004C			244	.L. EQU #4C	
004D			245	.M. EQU #4D	
004E			246	.N. EQU #4E	DES
004F			247	.O. EQU #4F	
0050			248	.P. EQU #50	
0051			249	.Q. EQU #51	
0052			250	.R. EQU #52	
0053			251	.S. EQU #53	
0054			252	.T. EQU #54	
0056			253	.V. EQU #56	
0057			254	.W. EQU #57	
0058			255	.X. EQU #58	
00C4			256	IDLY EQU #C4	INITIAL REPEAT DELAY (UNITS=16.7 MS)
00F9			257	RDLY EQU #F9	REPEAT DELAY
00F1			258	RDLY EQU #F1	CURSOR BLINK DELAY
0003			259	RTRY EQU #03	TOTAL NO. OF TRIES
					DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 10)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
			261	**** RAM ASSIGNMENTS ****	
0020			262	ORAM 32	
0020			263	KEY RRAM 1	
0021			264	FLAG RRAM 1	INITIALLY 0
			265	.	8 CLOCK
			266	.	7 FAST TRANSFER FLAG
			267	.	6 ASCII MODE
			268	.	5 .D. DOUBLE ENTRY FLAG
			269	.	4 NUMBER ENTRY MADE
			270	.	3 INT2 YET TO BE PROCESSED
			271	.	2 SEEK TRACK 0 BYPASSED INITIALLY
			272	.	1 INSERT MODE
0022			273	IRPT RRAM 1	INITIALLY 0
0023			274	RPT RRAM 1	INITIALLY 0
0024			275	BCNT RRAM 1	INITIALLY 0
0025			276	LCNT RRAM 1	INITIALLY 0
0026			277	K80 RRAM 1	INITIALLY -80
0027			278	PDC RRAM 1	INITIALLY #C7
0028			279	CURS RRAM 2	CURSOR POSITION
002A			280	LINE RRAM 2	START OF NEXT LINE
002C			281	SCPD RRAM 1	VERY SHORT TERM SCRATCH PAD
002U			282	TEMP RRAM 1	TEMP STORAGE FOR .C.
002C			283	T20 RRAM 1	TEMP STORAGE FOR FINAL TRACK (.C. COMMAND)
002F			284	CTRK RRAM 1	CURRENT TRACK
0030			285	TRK RRAM 1	CURRENT DESIRED TRACK
0031			286	SCTR RRAM 1	CURRENT DESIRED SECTOR
0032			287	DHL RRAM 1	DIGIT BUFFER -- LOWER DIGIT
0033			288	URU RRAM 1	DIGIT BUFFER -- UPPER DIGIT
0034			289	STC RRAM 1	STEP COUNTER
0035			290	FIS RRAM 1	FDC INTERRUPT STATUS
0036			291	FNS RRAM 1	FDC NORMAL STATUS
0037			292	ERRC RRAM 1	ERROR COUNTER
0038			293	ERRS RRAM 1	NUMBER OF RETRIES MADE
00E9			296	ORAM #E9	
00E9			297	**** PRE FORMAT BLOCK FOR WRITE FORMAT	
00E9			298	FC=D RRAM 1	COMMAND(FORMAT WRITE)
					DES
					DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 11 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
00EA	299	FIGC	RRAM 1	PRE-INDEX GAP CHARACTER	
00EB	300	PIGS	RRAM 1	PRE-INDEX GAP SIZE	
00EC	301		RRAM 1	ARBITRARY (IGNORED BY FDC)	
00ED	302		RRAM 1	POST INDEX MARK GAP SIZE (FIRST HALF)	
00EE	303	IMC	RRAM 1	INDEX MARK CHARACTER	
00EF	304		RRAM 1	POST INDEX MARK GAP CHARACTER (FIRST HALF)	
00F0	306		ORAM #F0		
00F1	307	**** FDC	FORMAT BLOCK		
00F0	308	CWD	RRAM 1	FDC COMMAND BYTE	
00F1	309	GCA	RRAM 1	GAP CHARACTER A	
00F2	310	GSA	RRAM 1	GAP SIZE A	
00F3	311	RSA	RRAM 1	RECORD SIZE A	
00F4	312	GSD	RRAM 1	GAP SIZE H	
00F5	313	AMC	RRAM 1	MARK CHARACTER (ADDRESS MARK CODE)	
00F6	314	TA	RRAM 1	TRACK ADDRESS	
00F7	315		RRAM 1		
00F8	316	SA	RRAM 1	SECTOR ADDRESS	
00F9	317		RRAM 1		
00FA	318	GCB	RRAM 1	GAP CHARACTER B	
00FB	319	GCC	RRAM 1	GAP CHARACTER C	
00FC	320	GSC	RRAM 1	GAP SIZE C	
00FD	321	RSD	RRAM 1	RECORD SIZE B	
00FE	322	GSD	RRAM 1	GAP SIZE D	
00FF	323	SMC	RRAM 1	MARK CHARACTER (DATA SYNC MARK CODE)	
0100	326		ORAM #100		
0100	327	**** READ/	WRITE BUFFER ****		
0100	328	BUFR	RRAM 256		
0000	329	BAAL	EQU #00	LOWER BUFFER ADDRESS	
00C1	330	BAUR	EQU #C1	UPPER BUFFER ADDRESS + READ BIT	
0041	331	BAUW	EQU #41	UPPER BUFFER ADDRESS + WRITE BIT	
	334	****	SCREEN IMAGE ****		
0280	335		ORAM #880		
0280	336	DATA	RRAM 1		

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - POOL/EQUATES/RAM

( 12 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
0880	337	L1	EQU DATA		
08D0	338	L2	EQU DATA+80		
0F60	339	L23	EQU DATA+1760		
0F80	340	L24	EQU DATA+1840		
0FFF	341	OTOP	EQU DATA+1919		
00F0	342	KTOP	EQU #E0	= (TOP PAGE + 1)	
00EF	343	KBOT	EQU #EF	= BOTTOM PAGE	
00D0	344	DL2L	EQU #D0	LOWER 8 BITS OF L2	
0040	345	DL2U	EQU #40	UPPER 6 BITS + WRITE BIT FOR L2	
0080	346	DIAL	EQU #80	LOWER 8 BITS FOR DATA	
0048	347	DMAU	EQU #48	UPPER 6 BITS OF DATA + WRITE BIT	
00C0	348	DAUR	EQU #C8	UPPER 6 BITS OF DATA + READ BIT	



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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 13 )

ROM    ..CODE..    ARG    STMT  
ADDR   11 12 13       NUMBER

## SOURCE STATEMENTS

```

351 .....
352 *
353 *           SECTION 2
354 *
355 *           CRT  ROUTINES
356 *
357 *
358 *   THE CRT ROUTINES THAT FOLLOW RESIDE IN
359 *   THE LOWER 1K BYTES OF PROGRAM MEMORY
360 *   THE ROUTINES IN THIS SECTION PERFORM ALL
361 *   OF THE FUNCTIONS RELATED TO THE CRT AND
362 *   KEYBOARD.  THERE ARE LINKAGES TO THE
363 *   FLOPPY DISK ROUTINES IN THIS SECTION AND
364 *   SOME OF THE SUBROUTINES MAY BE CALLED BY
365 *   THE FLOPPY DISK ROUTINES.  THE SECTION
366 *   IS GENERALLY ORGANIZED AS FOLLOWS
367 *
368 *       1)  INITIALIZATION
369 *       2)  BACKGROUND LOOP KEYBOARD SAMPLING
370 *       3)  INTERRUPT 1 REFRESH OF CRT
371 *       4)  PROCESSING KEYBOARD ALPHANUMERICS
372 *       5)  HS232 INTERFACE
373 *       6)  PROCESSING SCREEN EDITOR KEYS
374 *       7)  MISCELLANEOUS SUBROUTINES
375 *
376 *           ROCKWELL INTERNATIONAL
377 *           MICROELECTRONIC DEVICE DIVISION
378 *           AUGUST 19, 1976
379 *
380 .....

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 14 )

ROM    ..CODE..    ARG    STMT  
ADDR   11 12 13       NUMBER

## SOURCE STATEMENTS

```

382            ORG    #00
383 *    POWER ON
384            NOP
385            R        POWR

387 ***** SUBROUTINE ENABLE INTERRUPTS *****

0003 58            389 ENBL        RT1

```

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 15)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
			390	ORG	#C0	
			392	* POWER ON OR RESET INITIALIZATION		
00C0	C1 76	00C0	394	POWR	EQU *	
00C2	AD(20 70)	00F6	395	RL	ISTK	INITIALIZE STACK POINTER
00C3	4E 73	0000	396	LAI	#00	
00C5	4E 32	82	398	OUT	LFB,D1	PDC 1, CH B = STATIC IN
00C7	86(06)FC	0003	399	OUT	LFA,D2	PDC2, CH, A = STATIC INPUT
00C9	4E H3	83	400	LAI	CLKI	
00CH	86(06)F9	0004	401	OUT	LFB,D2	PDC 2, CHAN, B = CLOCKED IN,
00CD	4E 42	42	402	LAI	SOUT	PDC F CHAN A <= STATIC OUT
00CF	86(06)FE	0001	403	OUT	LFA,PDCF	
00D1	4E 43	43	404	LAI	SIO	PDC F CHAN B <= STATIC I/O
00D3	86(06)FA	0007	405	OUT	LFB,PDCF	
00D5	4E C3	C3	406	LAI	#07	
00D7	FB(48 H8)	01EE	407	OUT	LF1,SDC	
00D9	BF	0040	408	BL	MOD2	
			409	OR	#40	
			410	* INITIALIZE FLAGS		
			411	* CLEAR PAGE 0		
00D9	AD(20 70)	0000	412	LAI	#00	
00DA	3A(0A)DF	0020	413	LXI	#20	
00DC	37		414	SN		
00DE	DC	00DC	415	H	*-1	
00E0	8A(0A)D9	0026	416	LXI	K80	
00E2	36(06)4F	FFH0	417	LAI	-80	
00E4	77		418	SN		
00E6	86(06)38	00C7	419	LAI	#C7	
00E8	75		420	S		
00EA	8A(0A)7F	0100	421	LXI	BUFR	
00EC	92(12)FD	0100	422	LZI	RUFH	FILL BUFFER WITH ERCDIC 7'S
00EE	86(06)90	006F	423	LAI	#6F	
00F0	37		424	SV		
00F2	EC	00FC	425	H	*-1	
00F4	37		426	SN		
00F6	FE	00EE	427	B	*-1	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 16)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
00F0	F3(93 B3)	0003	428	BL	ENBL	ENABLE INTERRUPTS
00F1	CA 00	0500	429	HL	SKT0	
00F3	21		430	NOP		
00F4	00 85	0280	431	H	.CLR	
00F6	9A(1A)		434	ISTK	PUPA	
00F7	FG	00F6	435	H	ISTK	
00F8	97(17)		436	PSHA		SET STACK POINTER TO ZERO
00F9	97(17)		437	PSHA		
00FA	97(17)		438	PSHA		PUSH 2 EXTRA SINCE RT WILL POP 2
00FB	SE		439	RT		

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 17)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
			441	ORG		
			443	****	BACKGROUND LOOP	****
0100	4E 89	81	445	BACK	IN RBA,D2	LINE/LOCAL
0102	47		446		RAR	
0103	27 5D 83	010D	447		BC RCVR	LINE
0106	4E 8B	83	448	DAKG	IN RSR,D2	NEW KEY?
0108	88(38 72)	0020	449		ANI #20	
0109	22 00 83	0160	450		BNZ NKEY	BIT 6 = RUFFER FULL
010C	93(33 42)	0021	451		LXI FLAG	
010D	08 80	0100	452		BBF 8,BACK	CLOCK ON ?
010F	A1(21)	0008	453		RB 8	YES, RESET IT
0110	3A(0A)DB	0024	454		LXI RCNT	INCREMENT BLINK COUNTER
0112	7D		455		L	
0113	42		456		INCA	
0114	75		457		S	
0115	25 9F	011F	458		BN B3	TEST BLINK COUNTER
0117	86(06)0E	00F1	459		LAI BDLY	DONE, RESET COUNTER
0119	75		460		S	
011A	F4(94 84)	03H2	461		HL LOC	
011H	86(06)7F	0080	462		LAI #80	
011D	69		463		EOR	
011E	75		464		S	
011F	8A(0A)DD	0022	465	B3	LXI IRPT	
0121	08 AE	012E	466		BBF 8,B0	INITIAL DELAY FOR REPEAT?
0123	7D		467		L	YES
0124	42		468		INCA	
0125	75		469		S	
0126	22 80	0100	470		BNZ BACK	DELAY FINISHED?
0128	4E 89	81	471		IN RBA,D2	SEE IF STROBE STILL ON
012A	25 C2	0142	472		BN B2	YES -- PERFORM KEY FUNCTION AGAIN
012C	21		473		NOP	
012D	H0	0100	474		R BACK	
012F	8A(0A)DC	0023	476	B0	LXI RPT	REPEAT IN PROGRESS?
0130	08 80	0100	477		BBF 8,BACK	
0132	4E 89	81	478		IN RBA,D2	YES,SAMPLE KEY STROBE

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 18)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
0134	25 89	0139	479	BN	B1	IS KEY STILL DEPRESSED?
0136	80 18	0038	480	RB	8	NO, RESET REPEAT FLAG
0138	90	0100	481	B	HACK	
0139	EE(8E AF)	03H4	483	B1	HL BLC	YES, FORCE CURSOR ON DURING REPEAT
013A	71(11)	0008	484		SB 8	
013H	8A(0A)DC	0023	485		LXI RPT	
013D	7D		486		L	TEST REPEAT COUNTER
013E	42		487		INCA	
013F	75		488		S	
0140	22 80	0100	489		BNZ BACK	REPEAT TIMER = 0 ?
0142	8A(0A)DC	0023	490	B2	LXI RPT	YES, RESET IT
0144	06(06)06	00F9	491		LAI RDLY	
0146	75		492		S	
0147	4E 89	81	493	****	SEE IF LINE OR LOCAL -- DISPLAY OR TRANSMIT REPEATED KEY	
0149	47		494		IN RBA,D2	
014A	27 3F 83	018F	496		RAR	
014D	21		497		BC TKEY	LINE SO TRANSMIT KEY
014E	15 83	0195	498		NOP B	NK.

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 19 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
			500	**** DATA REQUEST INTERRUPT ****
0150	97(17)		502	INT1 PSHA
0151	98(18)		503	PSHX
0152	8A(0A)DA	0025	504	LXI LCNT INCREMENT LINE COUNT
0154	4E 7A	72	505	IN RBB,D1 TEST FOR FRAME START
0156	46		506	RAL
0157	24 DC	015C	507	RP IN11 BIT 7 = FRAME START
0159	87(07)16	FFE9	508	LAI -23 YES, RESET LINE COUNT
015R	E1	0161	509	B IN12
015C	7D		510	L
015D	23 45 86	0345	511	HZ MRS LINE COUNT = ZERO, IGNORE LINE BUFFER DES
			512	*
			513	INCA
0160	42		514	IN12 SN
0161	77		515	BNZ I1
0162	22 F2	0172	516	* END OF FRAME, RESET DMA AND SET PSEUDO CLOCK
0164	36(06)7F	0080	517	LAI DMAL
0166	4E 35	35	518	OUT LARL,DCC
0168	61		519	NOP
0169	86(06)B7	0048	520	LAI DMAU
016R	4E 36	36	521	OUT LARU,DCC
016D	61		522	NOP
016E	83(33 42)	0021	523	LXI FLAG SET CLOCK FLAG
016F	91(11)	0008	524	SB 8
0170	8A(0A)D9	0026	525	LXI K80 LEAVE LINE COUNTER AT 0
			526	* RESET RECORD LENGTH COUNTER AND PDC
0172	7F		527	I1 LN -80
0173	4E 37	37	528	OUT LRLR,DCC
0175	61		529	NOP
0176	7F		530	LN
0177	4E 72	72	531	OUT LFA,D1
0179	61		532	NOP
017A	9E(1E)		533	12 POPX
017B	96(16)		534	POPA
017C	58		535	HTI

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 20 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
			536	ORG
			538	**** KEY PROCESSING ****
0180	4E 8A	82	539	NKEY IN RBB,D2 GET KEY CODE
0182	84(34 43)	0020	540	LXI KEY
0183	75		541	S
0184	A1(21)	0008	542	RB 8 CLEAR PARITY
0185	4E 89	81	543	IN RHA,D2
0187	88(38 72)	0020	544	ANI #20
0188	22 37 88	0587	545	RNZ FLPY NOT CONTROL KEY SO DISPLAY OR TRANSMIT IT
018R	4F 89	81	546	NK10 IN RBA,D2 LINE OR LOCAL? TRANSMIT OR DISPLAY
018D	47		547	RAR
018F	27 BF	018F	548	RC TKEY LINE SO TRANSMIT KEY ENTERED FROM KRD
0190	8A(0A)DD	0022	549	NK0 IN RPT SET INITIAL DELAY FOR REPEAT
0192	86(06)3H	00C4	550	LAI IDLY
0194	75		551	S
0195	FE(9E BE)	01A5	552	NK. HL BTBL WAS IT A SCREEN EDITOR KEY ?
0196	00 84	0200	553	DW0 KEYS
0198	09	0209	554	DW KTAB,LO
			556	* NORMAL KEY (NOT SCREEN EDITOR KEY)
0199	83(33 42)	0021	557	LXI FLAG
019A	0F 9F	019F	558	RHF 1,NK3 INSERT MODE
019C	EE(8E AF)	0384	559	HL RLC YES, MOVE CHARS. ON LINE
019D	C4 74	0274	560	RL INSC
019F	84(34 43)	0020	562	NK3 LXI KEY
01A0	7D		563	L
01A1	EF(8E AE)	0384	564	BL RLC DISPLAY CHARACTER
01A2	35		565	S
01A3	25 84	0225	566	B .CRT MOVE CURSOR

569 \*\*\* SUBROUTINE TO SEARCH CODE TABLE AND BRANCH TO CORRESPONDING RTN.

01A5 A9(29) 571 BTBL LXL GET ADDRESS OF CODE TABLE

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 21 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
01A6	AC(2C)		572	LZL	
01A7	5H		573	PSML	SAVE ADDRESS OF THIRD PARAMETER
01A8	59		574	XL	
01A9	B4(34 43)	0020	575	LXI	KEY
01AA	A8(28)		576	LAL	PICK UP CODES
01AH	25 RC	01BC	577	BTB2	NOT IN TABLE
01AN	28 AA	01AA	578	BTB1	KEEP LOOKING
01AF	59		579	XL	
01B0	54		580	XAX	CODE FOUND GO TO APPROPRIATE ROUTINE
01B1	5D		581	RC	
01B2	46		582	RAL	TIMES 2
01B3	8A(0A)D2	002D	583	LXI	TEMP
01B5	75		584	S	
01B6	5A		585	POPL	GET THIRD PARAMETER
01B7	A8(28)		586	LAL	
01B8	6F		587	A	
01B9	54		588	XAX	
01BA	59		589	XL	
01BP	1E		590	RTS	GO TO SELECTED ROUTINE
01BC	5A		592	BTB2	POPL
01BD	A8(28)		593	LAL	INCREMENT RETURN
01BE	3E		594	RT	RETURN IF CODE NOT FOUND

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 22 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
597 * SERIAL DATA CONTROLLER INTERFACE TO TERMINAL					
01BF	4E CD	C5	599	KEY	IN RQS3,SDC DATA SET HEADY?
01C1	B8(38 72)	0020	600	ANI	#20
01C2	23 C6	01C6	601	RZ	ONLN
01C4	21		602	NOP	
01C5	C4	01C4	603	R	*-1
01C6	FA(96 88)	01EE	605	ONLN	BL MOD2
01C7	FF	0000	606	DN	#00
01C8	4E CE	C6	607	IN	RS12,SDC DATA TERM RDY,REQUEST TO SEND
01CA	45		608	MDL	CLEAR TO SEND?
01CH	25 C6	01C6	609	RN	ONLN
01CD	F8(98 88)	01EE	610	SL	MOD2
01CE	FB	0004	611	DW	#04
01CF	B4(34 43)	0020	612	LXI	KEY
01D0	7D		613	L	
01D1	4F C1	C1	614	OUT	LTR,SDC
01D3	4E CE	C6	615	IN	RS12,SDC TRANSMIT BUFFER EMPTY?
01D5	46		616	RAL	
01D6	24 D3	01D3	617	BP	ABCK
01D8	FA(98 88)	01EE	618	HL	MOD2
01D9	8A	0044	619	DW	#44
01DA	21		620	NOP	
01DB	00 82	01D0	621	B	BACK
623 *** ONLINE RECEIVE ***					
01D0	4E CE	C6	625	RCVR	IN RS12,SDC
01DF	25 E7	01E7	626	HN	DISP
01E1	47		627	RAR	
01E2	26 06 82	01D6	628	RNC	BANK
01E5	21		629	NOP	
01E6	00	01D0	630	B	RCVR
RECEIVE BUFFER FULL					
RECEIVER NOT BUSY SO RETURN TO BACKG LOOP					
RECEIVER BUSY SO WAIT					

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## ROCKWELL CRT/FOC DEMONSTRATOR L6611 - CRT ROUTINES

( 23 )

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS		
01E7	4E C8	C0	632	DISP	IN	RRB,SDC
01E9	84(34 43)	0020	633		LXI	KEY
01EA	75		634		S	
01EB	80 18	0008	635		RB	8
01ED	90	0190	636		B	NK0
						CLEAR PARITY??????
			638	**** SUBROUTINE SDC MODE CONTROL ****		
01EE	A8(28)		640	MOD2	LAL	
01EF	4E C4	C4	641		OUT	LF2,SDC
01F1	5E		642		RT	

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## ROCKWELL CRT/FOC DEMONSTRATOR L6611 - CRT ROUTINES

( 24 )

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS		
			645	ORG		
			646	**** TABLES FOR PROCESSING SCREEN EDITOR KEYS		
			648	* NOTE....THE FOLLING TABLE MUST BE ALIGNED AT LOC. 0*MOD 64		
0200	E3	001C	649	KEYS	DW	#1C 1 CLEAR
0201	E7	0018	650		DW	#18 21 RESET
0202	F2	0000	651		DW	#0 35 CARRIAGE RETURN
0203	F5	000A	652		DW	#A 55 NEW LINE
0204	F7	0008	653		DW	#8 76,15 CURSOR LEFT OR BACKSPACE
0205	E0	001F	654		DW	#1F 77 CURSOR RIGHT
0206	E1	001E	655		DW	#1E 56 CURSOR UP
0207	F4	0008	656		DW	#8 57 CURSOR DOWN
0208	E2	001D	657		DW	#1D 17 DELETE LINE
0209	F3	000C	658		DW	#C 16 INSERT LINE
020A	A0	007F	659		DW	#7F 37 DELETE CHARACTER
020B	E5	001A	660		DW	#1A 36 INSERT CHARACTER
020C	7F	0080	661		DW	#80 - = END OF TABLE
			662	*** BRANCH TABLE		
		0209	663	KTAB	EQU	*-4
020D	00 A5	0280	664		DW0	.CLR CLEAR
020F	6F A4	026F	665		DW0	.RST RESET
0211	45 A4	0245	666		DW0	.CR CARRIAGE RETURN
0213	45 A4	0245	667		DW0	.CR NEW LINE
0215	2F A4	022F	668		DW0	.CLF CURSOR LEFT
0217	25 A4	0225	669		DW0	.CRT CURSOR RIGHT
0219	3D A4	023D	670		DW0	.CUP CURSOR UP
021A	41 A4	0241	671		DW0	.CDN CURSOR DOWN
021D	4A A5	02CA	672		DW0	.DEL DELETE LINE
021F	15 A5	0295	673		DW0	.INL INSERT LINE
0221	55 A5	0205	674		DW0	.DLC DELETE CHARACTER
0223	6A A4	026A	675		DW0	.INC INSERT CHARACTER
			677	**** CURSOR MOVEMENT		
			679	* RIGHT		
0225	EF(8E AF) 03B4		680	.CRT	BL	BLC BLANK CURSOR AND GET ADDRESS
0226	13		681	CRT	INCX	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 25)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS		
0227	AA	022A	682	B	CR1	NO PAGE BOUNDARY
0228	E3(83 A3)	0300	683	BL	INCZ	PAGE BOUND., INC. PAGE AND TEST WRAP
0229	AD	022D	684	R	CR2	WRAP-AROUND BOTTOM OF SCREEN
022A	EB(84 AR)	0392	685	BL	CLIN	NEW LINE?
022B	72 85	02F2	686	R	EXIT	NO, DONE
022D	E7(87 A7)	0380	687	BL	INCL	YES, INCREMENT LINE
022E	FD(9D HD)	02F1	688	BL	EXIP	
690 * LEFT						
022F	EC(8C AC)	039E	691	.CLF	BL	LLIN GET ADDRESS OF START OF LINE
0230	E6(86 A6)	0339	692		BL	DE80
0231	54		693		XAX	
0232	51(31 41)	0029	694		LXI	CURS+1
0233	28 86	0236	695		RNF	CL1
0235	E8(88 AB)	038C	696		HL	DECL
0236	EE(8E AE)	0384	697	CL1	BL	RLC
0237	11		698		DECX	DECREMENT CURSOR
0238	72 85	02F2	699	R	EXIT	NO PAGE CROSSING
023A	E4(84 A4)	031F	700	RL	DECZ	PAGE CROSS
023B	8C	023C	701	R	*+1	
023C	FD(9D HD)	02F1	702	HL	EXIP	
704 * UP						
023D	EE(8E AE)	0384	705	.CUP	BL	RLC
023E	E6(86 A6)	0339	706		RL	DE80
023F	E8(88 AB)	038C	707		RL	DECL
0240	FD(9D HD)	02F1	708		BL	EXIP
710 * DOWN						
0241	EE(8E AE)	0384	711	.CDN	RL	RLC
0242	E5(85 A5)	032E	712		RL	IN80
0243	E7(87 A7)	0380	713		BL	INCL
0244	FD(9D HD)	02F1	714		BL	EXIP
716 * NEW LINE (CARRIAGE RETURN)						
0245	EE(8E AE)	0384	718	.CR	BL	RLC
0246	ED(8D AD)	03AB	719		RL	CLST

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 26)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS		
0247	CA	024A	720	B	CRR1	NO
0248	21		721	NOP		YES, SCROLL
0249	CD	024D	722	R	SCOL	
024A	EC(8C AC)	039E	723	CRR1	BL	LLIN
024B	E7(87 A7)	0380	724		BL	INCL
024C	FD(9D HD)	02F1	725		BL	EXIP
727 **** SCROLL SCREEN ****						
024D	8A(0A)7F	0880	729	SCOL	LXI	L1
024F	92(12)EE	0880	730		LZI	L1
0251	59		731		XL	
0252	8A(0A)2F	08D0	732		LXI	L2
0254	92(12)EE	08D0	733		LZI	L2
0256	5F		734		SC	SET SCROLL FLAG
735 * MOVE SCREEN UP BY 1 LINE						
0257	3R		736	SC0.	LNXL	
0258	00	025D	737		R	SC1
0259	73		738		SNXL	
025A	E3(83 A3)	0300	739		HL	INCZ
025B	E3	0263	740		H	SC2
025C	78		741		LNXL	DONE, GO STORE BLANKS IN LAST LINE
025D	33		742	SC1	SNXL	
025E	07	0257	743		B	SC0.
025F	57		744		XAL	
0260	42		745		INCA	
0261	17		746		XAL	
0262	07	0257	747		R	SC0.
748 * STORE BLANKS IN LAST LINE						
0263	27 17 85	0297	749	SC2	RC	IN.
0266	F2(92 R2)	030F	750		BL	BLKL
0267	EC(8C AC)	039E	751		BL	LLIN
0268	E6(86 A6)	0339	752		BL	DE80
0269	FD(9D HD)	02F1	753		BL	EXIP
754 **** INSERT CHARACTER ****						
026A	H3(33 42)	0021	756	.INC	LXI	FLAG

SET INSERT MODE

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
0269	80 17	0001	757	SB 1
026D	00 82	0100	758	B BACK
026F	83(33 42)	0021	759	.RST LXI FLAG RESET KEY, CLEAR INSERT MODE
0270	94(14)	0001	760	RB 1
0271	21		761	NOP
0272	00 82	0100	762	B BACK
764 ***** SUBROUTINE INSERT CHARACTER *****				
* MOVE CHARS. 1 POSITION RIGHT STARTING AT CURSOR, ENDING AT END OF LINE				
0274	86(06)DF	0020	766	INSC LAI BLNK
0276	7D 37		767	INS0 XN
0278	FA	027A	769	R INS1
0279	E9(89 A9)	030A	770	HL INZS
027A	E8(8B AB)	0392	771	INS1 BL CLIN
027P	F6	0276	772	B INS0
027C	5F		773	RT

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
775				ORG
777 ***** CLEAR SCREEN *****				
0280	8A(0A)7F	0880	779	.CLR LXI DATA
0282	92(12)EE	0880	780	LZI DATA
0284	F0(9D 8D)	03C7	781	BL BLKS
0285	17	FFE8	782	DW -24
0286	5D		783	.CL RC
784				BYPASS CLRNG SCRN, HOME CURSOR
785				*((( THE FOLLOWING CODE IS USED AS A SUBROUTINE OR IN-LINE )))
0287	B5(35 44)	002A	785	..CL LXI LINE
0288	9A(06)EF	08D0	786	LAI L2+U
028A	77		787	SN
028B	86(06)2F	08D0	788	LAI L2
028D	75		789	S
028E	8A(0A)7F	0880	790	LXI DATA
0290	92(12)EE	0880	791	LZI DATA
0292	66		792	SKC
0293	F0(9D 8D)	02F1	793	RL EXIP
0294	5E		794	RT
796 ***** INSERT LINE *****				
0295	ED(8D AD)	03A6	798	.INL HL CLST
0296	9D	029D	799	R INI
0297	F2(92 B2)	030F	800	IN. BL BLKL
0298	8A(0A)4F	0FB0	801	LXI L24
029A	93(13)E0	0FB0	802	LZI L24
029C	F2	02F2	803	H EXIT
804				* MOVE DATA DOWN 1 LINE STARTING AT CURRENT LINE
029D	EE(8E AE)	0384	805	INI RL PLC
029F	8A(0A)00	0FFF	806	LXI DTOP
02A0	92(12)E0	0FFF	807	LZI DTOP
02A2	59		808	XL
02A3	8A(0A)D4	002R	809	LXI LINE+1
02A5	80 RC		810	LA



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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 29 )

ROM ADDR	..CODE.. I1 I2 I3	ANG	STMT NUMBER	SOURCE STATEMENTS		
02A7	50		811	DEXY		LINE NO. INTO Y
02A8	61		812	NOP		
02A9	8A(0A)50	0FAF	813	LXI	L24-1	
02AB	92(12)E0	0FB0	814	LZI	L24	
02AD	39		815	INO	LDXL	
02AE	83	02B3	816	B	IN2	
02AF	57		817	XAL		
02B0	4H(3B 63)	FFFF	818	AISK	-1	
02B1	61		819	NOP		
02B2	57		820	XAL		
02B3	70		821	INO	SDCX	
02B4	AD	02AD	822	B	INO	
02B5	59		823	XL		
02B6	54		824	XAX		
02B7	56		825	XAZ		
02B8	85(35 44)	002A	826	LXI	LINE	
02B9	28 BF	02BF	827	RNE	IN3	
02BA	EC(8C AC)	039E	828	BL	LLIN	STORE BLANKS AT CURRENT LINE
02BC	E6(86 A6)	0339	829	RL	DE80	
02BD	F1(91 B1)	030C	830	BL	BLK1	
02BE	FD(90 BD)	02F1	831	BL	EXIP	
02BF	56		832	INO	XAZ	
02C0	48		833		LXA	
02C1	59		834	XL		
02C2	42		835	INCA		
02C3	22 AD	02AD	836	RNZ	INO	PAGE BOUNDARY?
02C5	57		837	XAL		YES
02C6	8B(3B 63)	FFFF	838	AISK	-1	
02C7	61		839	NOP		
02C8	17		840	XAL		
02C9	AD	02AD	841	B	INO	
			843	****	DELETE LINE	****
02CA	ED(8D AD)	03A6	845	DEL	HL CLST	CURSOR ON LAST LINE?
02CB	CE	02CE	846	B	DE1	NO
02CC	21		847	NOP		YES, BLANK LAST LINE

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 30 )

ROM ADDR	..CODE.. I1 I2 I3	APG	STMT NUMBER	SOURCE STATEMENTS		
02CD	97	0297	848	B	IN.	
02CE	EC(8C AC)	039E	849	BL	LLIN	SET-UP TO MOVE SCREEN UP BY ONE
02CF	E6(86 A6)	0339	850	BL	DE80	LINE STARTING AT CURRENT LINE
02D0	59		851	XL		
02D1	EC(8C AC)	039E	852	BL	LLIN	
02D2	10		853	RC		SET DELETE LINE FLAG
02D3	57 84	0257	854	B	SC0.	
			856	****	DELETE CHARACTER	****
02D5	ED(8D AD)	03A6	858	DL0	CLST	LAST LINE?
02D6	DC	02DC	859	B	DL0	NO
02D7	8A(0A)00	0FFF	860	LXI	OTOP	YES
02D9	93(13)E0	0FFF	861	LZI	OTOP	
02DB	E0	02E0	862	B	DL1	
02DC	EC(8C AC)	039E	863	BL	LLIN	GET ADDRESS OF END OF LINE
02DD	11		864		DECK	
02DE	E0	02E0	865	B	DL1	
02DF	EA(8A AA)	032A	866	RL	DEZS	PAGE BOUNDARY
02E0	86(06)DF	0020	867	DL1	BLNK	
02E2	7D 75		868	DL4	X	STORE BLANK AT END OF LINE, SAVE CHARACTERS
02E4	49		869		LYA	SAVE A
02E5	54		870	XAX		
02E6	31(31 41)	0029	871	LXI	CURS+1	
02E7	28 E8	02E8	872	RNE	DL3	TEST FOR END
02E9	14		873	XAX		END, GO DISPLAY CURSOR
02EA	F2	02F2	874	B	EXIT	
02EB	54		875	DL3	XAX	
02EC	11		876		DECK	
02ED	EF	02EF	877	B	DL2	MOVE CHARS 1 POSITION LEFT
02EE	EA(8A AA)	032A	878	BL	DEZS	STARTING AT END OF LINE AND
02EF	15		879	XAY		ENDING AT CURSOR POSITION
02F0	E2	02E2	880	B	DL4	NEXT CHAR IN A
			882	*****	COMMON EXIT	*****
02F1	5A		883	EXIP	POPL	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 31)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
02F2	EF (BF AF)	03C0	884	EXIT HL DPC
02F3	21		885	NOP
02F4	00 82	0100	886	B RACK

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 32)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
			888	ORG
			890	***** SUBROUTINE INCREMENT Z *****
0300	56		892	INCZ XAZ
0301	42		893	INCA
0302	44		894	LZA
0303	A5(25)1F	00E0	895	AISK KTOP
0305	1C		896	HSK\$
0306	87	0307	897	R *+1
0307	92(12)EE	0080	898	LZI DATA
0309	1E		899	RT\$
			901	***** SUBROUTINE INCREMENT Z SHORT *****
030A	56		903	INZS XAZ
030H	42		904	INCA
030C	56		905	INZ. XAZ
030D	5E		906	RT
			908	***** SUBROUTINE TO INCR. Z AND TEST FOR END OF SCREEN *****
030F	E3(83 A3)	0300	910	.IN7 BL INCZ
030F	91	0311	911	R .IN1
0310	1E		912	RT\$
0311	F6(76 D6)	0316	913	.IN1 BL DLY
0312	01	FFFE	914	Dw -2
0313	21		915	NOP
0314	00 82	0100	916	R RACK
			919	***** SUBROUTINE DELAY *****
0316	A8(28)		921	DLY LAL

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 33)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
0317	B3(33 42)	0021	922	DD1 LXI FLAG
0318	08 97	0317	923	BHF B+DD1
031A	A1(21)	0008	924	RH 8
031H	42		925	INCA
031C	22 97	0317	926	BNZ DD1
031E	5E		927	RT
			929	***** SUBROUTINE DECREMENT Z *****
031F	56		931	DECZ XAZ
0320	B8(38 63)	FFFF	932	AISK -1
0321	61		933	NOP
0322	4A		934	LZA
0323	A7(27)10	00EF	935	AISK K80T
0325	A7	0327	936	B DE11
0326	1C		937	RSKS
0327	92(12)E0	0FFF	938	DE11 LZI DTOP
0329	1E		939	RTS
			941	***** SUBROUTINE DECREMENT Z SHORT *****
032A	56		943	DEZS XAZ
032F	B8(38 63)	FFFF	944	AISK -1
032C	21		945	NOP
032E	8C	030C	946	B INZ.
			948	***** SUBROUTINE INCREMENT BY 80 *****
032E	56		950	IN80 XAX
032F	A7(27)AF	0050	951	AISK 80
0331	87	0337	952	B IN81
0332	HA(3A 62)	0080	953	AISK 128
0333	48		954	LXA
0334	E3(A3 A3)	0300	955	RL INCZ
0335	36	0336	956	B *-1
0336	5E		957	RT

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 34)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
0337	48		958	IN81 LXA
0338	5E		959	RT
			961	***** SUBROUTINE DECREMENT BY 80 *****
0339	56		963	DE80 XAX
033A	A5(25)4F	FF80	964	AISK -80
033C	61		965	NOP
033D	48		966	LXA
033E	25 C4	0344	967	BNZ DE81
0340	HA(3A 62)	0080	968	AISK 128
0341	48		969	LXA
0342	E4(84 A4)	031F	970	RL DECZ
0343	C4	0344	971	B *-1
0344	5E		972	DE81 RT

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 35)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
			976	*	MASTER RESET ROUTINE - OPERATES AS LONG AS INTERRUPT 1 IS SERVICED	DES
			977	*	RESET 1 - MINOR - MASTER RESET BUTTON ONLY	DES
			978	*	RESET 2 - MAJOR - CONTROL BUTTON AND MASTER RESET BUTTON	DES
			979	*	RESET 3 - ????? - CONTROL, ANY KEY, AND MASTER RESET BUTTONS	DES
0345	4E 89	81	981	MRS	IN RBA.D2	
0347	48		982		LXA	DES
0348	A4(24)FH	0004	983	ANI	#04	DES
034A	23 7A 02	017A	984	BZ	12	DES
034C	54		985	XAX		DES
034E	48		986	LXA		DES
034F	98(38 72)	0020	987	ANI	#20	DES
0350	23 08	0358	988	BZ	MRS1	DES
0352	54		989	XAX		DES
0353	24 40 81	00C0	990	OP	POWR	DES
0356	21		991	NOP		DES
0357	06	0358	992	MRS3	B MRS1	DES
						MSTR RESET 3 SAME AS 1 NOW
0358	EE(8E AF)	0384	994	MRS1	BL	DES
0359	C1 76	00F6	995	HL	ISTK	DES
035B	83(33 42)	0021	996	LXI	FLAG	
035C	9D(1D)	0006	997	RB	6	
035D	A0(20)	0077	998	RB	7	
						TURN CURSOR OFF REINITIALIZE STACK
035E	F3(93 B3)	0003	1000	* MSR1	MASTER RESET 1	DES
035F	21		1001	POW3	BL ENBL	DES
0360	06 85	0286	1002	NOP		DES
			1003	R	.CL	DES
						DONT CLEAR SCREEN

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 36)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
			1005		ORG	
			1007	*****	SUBROUTINE INCREMENT LINE	*****
0380	A3(23)		1009	INCL	PSHZ	
0381	98(18)		1010		PSHX	
0382	EC(9C AC)	039E	1011	BL	LLIN	
0383	E5(85 A5)	032E	1012	HL	INR0	
0384	60		1013	INL.	XY	UPDATE LINE NO.
0385	56		1014		XAZ	
0386	77		1015		SH	
0387	55		1016		XAY	
0388	75		1017		S	
0389	9E(1E)		1018		POPX	
038A	AE(2E)		1019		POPZ	
038B	5E		1020		RT	
			1022	*****	SUBROUTINE DECREMENT LINE	*****
038C	A3(23)		1024	DECL	PSHZ	
038D	98(18)		1025		PSHX	
038E	EC(9C AC)	039E	1026	BL	LLIN	
038F	E6(86 A6)	0339	1027	BL	DEB0	
0390	21		1028		NOP	
0391	84	0384	1029	R	INL.	
			1031	*****	SUBROUTINE COMPARE LINE	*****
0392	97(17)		1033	CLIN	PSHA	
0393	54		1034		XAX	
0394	8A(0A)D4	0028	1035	LXI	LINE+1	
0396	28 9d	039B	1036	RNE	CLII	
0398	54		1037		XAX	
0399	96(16)		1038		POPA	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 37)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
039A	1C		1039	RSKS	
039B	54		1040	CL11	XAX
039C	96(16)		1041		POPA
039D	1E		1042		RTS
1044 ***** SURROUTINE LOAD LINE *****					
039E	85(35 44)	002A	1046	LLIN	LXI LINE
039F	80 8E		1047		LZ
03A1	53		1048		INCX
03A2	80 8D		1049		LY
03A4	50		1050		DEXY
03A5	5E		1051		RT
1053 ***** SUBROUTINE COMPARE FOR LAST LINE *****					
03A6	85(35 44)	002A	1055	CLST	LXI LINE
03A7	86(06)EE	0080	1056		LAI DATA,U
03A9	28 AF	03AF	1057		BNE CLS1
03AH	53		1058		INCX
03AC	06(06)7F	0080	1059		LAI 128
03AE	6A		1060		SKE
03AF	1E		1061	CLS1	RTS
03B0	81	03B1	1062		B **1
03B1	1C		1063		RSKS
1065 ***** SUBROUTINE LOAD CURSOR *****					
03B2	1F		1067	LDC	SC
03B3	85	03B5	1068		H RLC.
1070 ***** SUBROUTINE BLANK CURSOR *****					
03B4	5D		1072	BLC	RC

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - CRT ROUTINES

( 38)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
03B5	8A(0A)D7	0028	1073	BLC.	LXI CURS
03B7	30 8E		1074		LZ
03B9	53		1075		INCX
03BA	80 8D		1076		LY
03BC	50		1077		DEXY
03BD	66		1078		SKC
03BE	A1(21)	0068	1079		RB 8
03BF	5E		1080		RT
1082 ***** SUBROUTINE DISPLAY CURSOR *****					
03C0	91(11)	0008	1084	DPC	SB 8
03C1	54		1085		XAX
03C2	81(31 41)	0029	1086		LXI CURS*1
03C3	74		1087		SD
03C4	56		1088		XAZ
03C5	75		1089		S
03C6	5E		1090		RT
1092 ***** SUBROUTINE STORE BLANKS *****					
03C7	A8(28)		1094	BLKS	LAL
03C8	98(18)		1095	BL1	PSHX
03C9	A3(23)		1096		PSH2
03CA	97(17)		1097	BL11	PSHA
03CB	66(66)DF	0020	1098		LAI BLNK
03CD	8E(0E)B0	004F	1099		LYI 79
03CF	37		1100	BL12	SN
03D0	D2	03D2	1101		R BL13
03D1	E9(89 A9)	030A	1102		BL INZS
03D2	60 10		1103	BL13	DECY
03D4	CF	03CF	1104		R BL12
03D5	96(16)		1105		POPA
03D6	42		1106		INCA
03D7	22 CA	03CA	1107		BNZ BL11
03D9	AE(2E)		1108		POPZ

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
030A	9E(1E)		1109	POPX
030B	5E		1110	RT
			1112	***** SUBROUTINE STORE 1 BLANK LINE *****
030C	80 71(71)	00FF	1114	BLK1 LAI #FF
030E	CA	03CH	1115	R R RLI
			1117	***** SUBROUTINE STORE BLANKS IN LAST LINE *****
030F	8A(0A)4F	0FB0	1119	BLKL LXI L24
03E1	93(13)E0	0FH0	1120	LZI L24
03E3	0C	03DC	1121	B BLK1

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
1126				*****
1127				*
1128				SECTION 3
1129				*
1130				FDC ROUTINES
1131				*
1132				*
1133				THE FDC ROUTINES THAT FOLLOW RESIDE IN
1134				THE SECOND AND THIRD 1K BYTE SECTIONS OF
1135				PROGRAM MEMORY (1.6K BYTES ARE REQUIRED).
1136				THESE ROUTINES, COMPLEMENTED BY SOME OF
1137				THE CRT SUBROUTINES, PERFORM THE FUNCTIONS
1138				RELATED TO CONTROLLING AND TRANSFERRING
1139				FLOPPY DISK DATA AS WELL AS INTERPRETATION
1140				AND EXECUTION OF OPERATOR COMMANDS. THIS
1141				SECTION IS GENERALLY ORGANIZED AS FOLLOWS
1142				*
1143				1) ROUTINES FOR CONTROL OF THE FLOPPY
1144				DISK DRIVE AND FDC I/O ROUTINES
1145				2) PROCESSING OPERATOR COMMANDS
1146				3) MISCELLANEOUS SUBROUTINES
1147				4) ASCII TO/FROM EBCDIC TABLES
1148				5) WRITE FORMAT ROUTINES (THE FORMAT
1149				WRITE ROUTINES ARE NOT COMPLETE AND
1150				SHOULD NOT BE USED. THEY ARE ONLY
1151				INDICATIVE OF WHAT WILL BE REQUIRED)
1152				*
1153				ROCKWELL INTERNATIONAL
1154				MICROELECTRONIC DEVICE DIVISION
1155				AUGUST 19, 1976
1156				*
1157				*****

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 41)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
			1159	ORG
			1162	**** SUBROUTINE STEP ****
			1163	**STEP NUMBER OF TRACKS SPECIFIED BY STC THEN LOWER HEAD AND
			1164	**WAIT TO SETTLE ON LAST TRACK
0400	8A(0A)CB	0034	1166	STPI LXI STC
0402	A8(28)		1167	LAL
0403	75		1168	S
				LOAD NUMBER OF STEPS
0404	CA 29	0529	1170	STEP BL RDY?
			1171	*** SEE IF STEP COUNTER = 0 -- DINE
0406	8A(0A)CB	0034	1172	LXI STC
0408	7D		1173	L
0409	23 A8	0428	1174	HZ STE1
			1175	**** STEP COUNTER # 0 SO DRIVE MUST BE STEPPED
040B	64		1176	SKN
040C	A5(25)00	00FF	1177	AISK #FF
040E	42		1178	INCA
040F	7D 75		1179	X
0411	46		1180	RAL
0412	86(06)F3	000C	1181	LAI #0C
0414	66		1182	SKC
0415	86(06)F1	000E	1183	LAI #0E
0417	4E 41	41	1184	OUT LBB,PDCF
0419	86(06)F7	0008	1185	LAI #08
041R	66		1186	SKC
041C	86(06)F5	000A	1187	LAI #0A
041E	4E 41	41	1188	OUT LBB,PDCF
0420	A5(25)F8	0004	1189	AISK #04
0422	4E 41	41	1190	OUT LBB,PDCF
			1191	*WAIT FOR THE DELAY
0424	FC(9C)BC	0537	1192	RL VDEL
0425	FD	0002	1193	D# 2
0426	21		1194	NOP
0427	84	0404	1195	H STEP

DES  
DES.  
DES  
DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 42)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
			1197	**** AT DESIRED TRACK SO WAIT FOR HEAD TO SETTLE AT THIS TRACK
0428	86(35)45	0030	1198	STE1 LXI TRK
0429	7C		1199	LD
042A	75		1200	S
042B	FC(9C)BC	0537	1201	RL VDEL
042C	F9	0006	1202	DW #6
042D	5E		1203	RT
			1206	**** SUBROUTINE SET -- SET UP DMAC FOR FDC OPERATION ****
			1207	**** ALSO START THE FDC
			1208	**** CALLING SEQUENCE:
			1209	**** BL SET
			1210	**** DW <CONTENTS OF LOWER ADDRESS REGISTER>
			1211	**** DW <CONTENTS OF UPPER ADDRESS REGISTER>
			1212	**** DW <COMMAND TO BE PLACED IN FDC FORMAT BLOCK>
042E	97(17)		1214	SET PSHA
042F	98(18)		1215	PSHX
0430	A3(23)		1216	PSMZ
0431	CA 29	0529	1217	HL RDY?
0433	A8(28)		1218	LAL
0434	97(17)		1219	PSHA
0435	48(28)		1220	LAL
0436	97(17)		1221	PSHA
0437	46		1222	HAL
0438	H7(37)60	0001	1223	LZI 1
0439	8A(0A)0F	00F0	1224	LXI CWD
043R	A8(28)		1225	LAL
043C	75		1226	S
043D	8A(0A)D0	002F	1227	LXI CTRK
043F	7E		1228	LNXY
0440	8A(0A)09	00F6	1229	LXI TA
0442	97(17)		1230	PSHA
0443	77		1231	SN
0444	52		1232	INXY
0445	53		1233	INX
0446	7E		1234	LNXY
				LOAD SECTOR FROM SCTR

DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 43)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
0447	75		1235	S
0448	96(16)		1236	POPA RETRIEVE TRACK NUMBER
0449	A7(27)2H	FF04	1237	AI SK -44
044B	CF	044F	1238	B SET1 < TRACK 43 SO NOT LOW CURRENT
044C	A7(07)2D	0004	1239	LAI #04 LOW CURRENT
044E	01	0451	1240	B SET2
044F	86(06)0B	00F4	1241	LAI #F4 NOT LOW CURRENT
0451	47		1242	SET1 RAR DAB TO INDICATE READ OR WRITE
0452	4E 40	40	1243	OUT LBA,PDCF
0454	9A(1A)		1244	POPA UPPER BYTE OF BUFFER ADDRESS
0455	57 08	0457	1245	H01 SET3 DISABE INTERRUPTS
		0457	1246	SET3 EQU *
0457	4F 26	26	1247	OUT LARU,DCD
0459	96(16)		1248	POPA LOWER BYTE OF BUFFER ADDRESS
045A	4E 25	25	1249	OUT LARL,DCD
045C	AD(20 70)	0000	1250	LAI #00
045D	4E 27	27	1251	OUT LRLH,DCD
045F	86(06)0F	00F0	1252	SET4 LAI #F0 FORMAT BLOCK
0461	4E 15	15	1253	OUT LARL,DCF
0463	4E 75	75	1254	OUT LARL,DCR
0465	AD(20 70)	0000	1255	LAI #00 READ,RECORD CYCLE
0466	4E 16	16	1256	OUT LARU,DCF
0469	4E 76	76	1257	OUT LARU,DCR
046A	4E 17	17	1258	OUT LRLH,DCF
046C	4E 77	77	1259	OUT LRLH,DCR
046E	H3(33 42)	0021	1260	LXI FLAG SET FLAG FOR PENDING FDC OPERATION
046F	H9(09)	0003	1261	SH 3
0470	4F 53	53	1262	OUT FCL,FDC
0472	4E 51	51	1263	OUT FST,FDC START THE FDC
0474	61		1264	NOP
0475	AE(2E)		1265	POPZ
047C	9E(1E)		1266	POPX
0477	96(16)		1267	POPA
0478	58		1268	RTI RETURN AND REENABLE INTERRUPTS

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 44)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
			1269	ORG
			1272	**** INTERRUPT 2 PROCESSING ROUTINE -- ONLY FDC CAUSES INT2
0483	97(17)		1274	INT2 PSHA
0481	98(18)		1275	PSHX
0482	8A(0A)CA	0035	1276	LXI FIS SAVE THE STATUS BYTES
0484	4E 08	00	1277	RIS
0486	77		1278	SN
0487	4E 5C	54	1279	IN FHS,FDC
0489	74		1280	SD
048A	4E 53	53	1281	OUT FCL,FDC
048C	61		1282	NOP
048D	53(33 42)	0021	1283	LXI FLAG
048E	98(18)	0003	1284	SH 3
048F	9E(1E)		1285	IN21 POPX
0490	96(16)		1286	POPA
0491	58		1287	RTI
			1289	**** SUBROUTINE WFDD -- WAIT UNTIL FDC OPERATION IS DONE ****
			1290	***** DETERMINED BY OCCURANCE OF AN INTERRUPT
			1291	*** CALLING SEQUENCE:
			1292	**** BL WFDD
			1293	**** B <OPERATION NOT COMPLETED>
0492	97(17)		1295	WFDD PSHA
0493	98(18)		1296	PSHX
			1298	**** INTERRUPT MODE SO WAIT UNTIL FLAG(3) IS RESET BY INTERRUPT
0494	H3(33 42)	0021	1299	LXI FLAG
		0495	1300	WFDD EQU *
0495	05 95	0495	1301	HRT 3,WFDD WAIT UNTIL INTERRUPT IS SERVICED
		0497	1302	WFDD EQU *
0497	8A(0A)C9	0036	1303	LXI FNS NORMAL STATUS
0499	04 A2	04A2	1304	HRT 4,WFDD DATA MARK NOT EQUAL
049B	07 A2	04A2	1305	OUT 1,WFDD DATA OVERRUN?

DES  
DES  
DES



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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 45 )

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS		
049D	51		1306	DECH		POINT TO INTERRUPT STATUS
049E	01 A2	04A2	1307	BBT	7,WFD8	TIMEOUT
04A0	03 AD	04AD	1308	BBT	5,WFD7	OPERATION COMPLETED
04A2	8A(0A)C8	0037	1310	WFD8	LXI ERRC	INCR RETRY COUNTER
04A4	7D		1311		L	
04A5	42		1312		INCA	
04A6	75		1313		S	
04A7	86(06)FC	0003	1314		LAI RTRY	
04A9	28 B6	04B6	1315		BNE WFD6	
04AB	00 38	0838	1316		BL DST	
04AD	8A(0A)C8	0037	1318	WFD7	LXI ERRC	COMPLETED SO RESET RETRY COUNTER
04AF	AD(2D 70)	0000	1319		LAI #00	
04B0	7D 77		1320		XN	RESET RETRY COUNTER
04B2	75		1321		S	SAVE COUNT IN ERRS
04B3	9E(1E)		1322		POPX	
04B4	96(16)		1323		POPA	
04B5	1C		1324		RSKS	
04B6	9E(1E)		1326	WFD6	POPX	
04B7	96(16)		1327		POPA	
04B8	1E		1328		RTS	

1331 \*\*\*\* SUBROUTINE TO PASS FORMAT PARAMETERS TO INITIALIZE RAM

04B9	C9 48	04CB	1333	IFFH	BL	ICB	
04BB	FF	0000	1334		DW	#00	GAP CHARACTER A
04BC	05	00FA	1335		DW	#FA	GAP SIZE A
04BD	03	00FC	1336		DW	#FC	RECORD SIZE A (ID RECORD SIZE)
04BE	0A	00F5	1337		DW	#F5	GAP SIZE B
04BF	01	00FE	1338		DW	#FE	MARK CHARACTER (ADDRESS MARK CODE)
04C0	FF	0000	1339		DW	#00	TRACK
04C1	FF	0000	1340		DW	#00	
04C2	FE	0001	1341		DW	#01	SECTOR

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 46 )

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS			
04C3	FF	0000	1342		DW	#00	
04C4	00	00FF	1343		DW	#FF	GAP CHARACTER B
04C5	FF	0000	1344		DW	#00	GAP CHARACTER C
04C6	05	00FA	1345		DW	#FA	GAP SIZE C
04C7	7F	0080	1346		DW	#80	RECORD SIZE B (DATA BLOCK)
04C8	01	00FE	1347		DW	#FE	GAP SIZE D *****<#ES>*****
04C9	04	00FB	1348		DW	#FB	DATA MARK CHARACTER
04CA	5E		1349		RT		

1351 \*\*\*\* SUBROUTINE ICB -- INITIALIZE FORMAT BLOCK

04CB	8A(0A)0E	00F1	1353	ICB	LXI	GCA	
04CD	87(37 60)	0001	1354	ICMP	LZI	1	
04CE	A8(28)		1355	ICM1	LAL		
04CF	J7		1356		SN		
04D0	CE	04CE	1357		H	ICB1	
04D1	5E		1358		RT		

1360 \*\*\*\* SUBROUTINE TDIF -- COMPUTE # OF STEPS TO BE MADE \*\*\*\*

04D2	03(33 42)	0021	1362	TDIF	LXI	FLAG	
04D3	06 07	04D7	1363		BRT	2,TD	HAS TRACK ZERO BEEN FOUND INITIALLY ?
04D5	CA 00	0500	1364		HL	SKT0	NO, GO DO IT
04D7	06(36 45)	0030	1365	TD	LXI	TRK	ADDRESS DESIRED TRACK
04D8	7C		1366		LD		
04D9	40		1367		COM		
04DA	*2		1368		INCA		- DESIRED TRACK
04DH	6F		1369		A		CURRENT TRACK - DESIRED TRACK
04DC	8A(0A)C8	0034	1370		LXI	STC	
04DE	75		1371		S		
04DF	5E		1372		RT		

1374 \*\*\*\* SUBROUTINE DEL3 -- 3MSEC DELAY

04E0	97(17)		1375	DEL3	PSHA		
04E1	86(06)BB	0044	1376		LAI	#44	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 47)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
04E3	80 21(61)	0001	1377	DL31 AISK #01
04E5	E3	04E3	1378	H DL31
04E6	96(16)		1379	POPA
04E7	5E		1380	RT
04E8	4E 4A	04E8	1383	FST2 EQU *
04EA	24 E8	42	1384	IN RRR,PDCF
		04E8	1385	BP FST2
		04EC	1386	FST1 EQU *
04EC	4E 4A	42	1387	IN RRR,PDCF
04EE	25 EC	04EC	1388	BN FST1
04F0	FC(9C BC)	0537	1389	BL VDEL
04F1	FF	0000	1390	DW #00
04F2	86(06)00	00FF	1391	LAI 255
04F4	80 21(61)	0001	1392	FST3 AISK #01
04F6	F4	04F4	1393	R FST3
04F7	5E		1394	RT

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 48)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
			1395	ORG	
			1397	*RESET DRIVE	
0500	AD(20 70)	0000	1398	SKT0 LAI #00	DES
0501	4E 40	40	1399	OUT LBA,PDCF	
0503	AF(2F 71)	00FF	1400	LAI #FF	
0504	4E 40	40	1401	OUT LBA,PDCF	
			1402	**** SEEK TRACK 00	
0506	CA 00	0400	1403	BL STPI	STEP IN SECEAL TRACKS
0508	03	00FC	1404	DW #FC	
			1406	**** STEP OUT UNTIL TRACK 00 ENCOUNTERED	
0509	4E 4A	42	1407	POW1 IN RRR,PDCF	SEE IF AT TRACK 00
050B	A4(24)EF	0010	1408	ANI #10	
050D	22 94	0514	1409	BNZ POW2	
050F	C8 00	0400	1410	BL STPI	NO -- TAKE ONE MORE STEP OUT
0511	FE	0001	1411	DW #01	
0512	21		1412	NOP	
0513	89	0509	1413	R POW1	
			1415	**** INITIALIZE FORMAT BLOCK	
0514	C9 39	0489	1416	POW2 BL IFFB	
0516	8A(0A)00	002F	1417	LXI CTRK	DES
0518	AD(20 70)	0000	1418	LAI #00	
0519	75		1419	S	SET CURRENT TRACK VALUE TO ZERO
051A	83(13 42)	0021	1420	LXI FLAG	DES
0514	45(05)	0002	1421	SH 2	DES
051C	5E		1422	RT	DES
			1424	**** SUBROUTINE HLD -- LOAD HEAD ****	
		0510	1425	HLD EQU *	
			1426	*LOWER HEAD AND WAIT FOR HEAD LOADING	
051D	86(06)05	00FA	1427	LAI #FA	
051F	4E 40	40	1428	OUT LBA,PDCF	
0521	FC(9C BC)	0537	1429	BL VDEL	
0522	EE	0011	1430	DW 17	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 49)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
0523	5E		1431	RT
			1433	**** SUBROUTINE UNLD -- UNLOAD HEAD
0524	86(06)01	00FE	1434	UNLD LAI #FE
0526	4E 40	40	1435	OUT LBA,PDCF
0528	5E		1436	RT
			1439	**** SUBROUTINE RDY? -- DETERMINE IF DRIVE IS READY
0529	4E 4A	42	1440	RDY? IN RBB,PDCF
052B	AA(24)BF	0040	1441	ANI #40
052D	52		1442	SKZ
052E	5E		1443	RT
			1444	**** ATTEMPT TO RESET F0
052F	AD(2D 70)	0000	1445	LAI #00 OUTPUT RESET PULSE
0530	4E 40	40	1446	OUT LBA,PDCF
0532	AF(2F 71)	00FF	1447	LAI #FF
0533	4E 40	40	1448	OUT LBA,PDCF
0535	21		1449	NOP
0536	A9	0529	1450	B RDY?
			1453	**** SUBROUTINE VDEL -- DELAY IN MULTIPLES OF 3 MSEC ****
			1454	**** CALL *IG SEQUENCE*
			1455	**** BL VDEL
			1456	**** DW <# OF TIMES - 1 DEL3 TO BE CALLED>
0537	9F(1F)		1457	VDEL PSHY
0538	H0 05		1458	LYL
053A	H0	053D	1459	B VDEL2
053B	C9 60	04E0	1460	VDEL1 RL DEL3
053C	60 10		1461	VDEL2 DECY
053F	HR	053B	1462	R VDEL1
0540	A6(26)		1463	POPY
0541	5E		1464	RT
			1467	**** SUBROUTINE USED TO READ NEXT SECTOR INTO SUCCESSIVE RAM LOCS.
			1468	**** SUBROUTINE SET MUST BE CALLED FOR THE FIRST SECTOR

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 50)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
			0542	SETC EQU *
0542	97(17)		1470	PSMA
0543	98(18)		1471	PSMX
0544	A3(23)		1472	PSMZ
0545	8A(0A)CE	0031	1473	LXI SCTR
0547	70		1474	L
0548	B7(37 60)	0001	1475	LZI 1
0549	8A(0A)07	00F8	1476	LXI SA
054B	35		1477	S
054C	5F 0A	045F	1478	BDI SET4
				STORE SECTOR NO. IN FORMAT BLOCK
				GO SET FORMAT CHANNELS BUT NOT DATA CHANNEL

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 51)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS				
1480 **** SUBROUTINE TO LOAD 24 SECTIONS FROM FLOPPY & DISPLAY ON SCREEN								
054E	CE 26	0726	1482	.L	RL	SU2	SET UP	DES
0550	F7	0008	1403		DL	#08	START WITH SECTOR 8	
0551	F9(99 U9)	042C	1484	DS4	RL	SET	START THE READ	
0552	FF	0000	1485		DL	HAL		
0553	3E	00C1	1486		DL	HAUR		
0554	FD	0002	1487		DL	ARS		
0555	FF(9F BF)	0492	1489	DS3	RL	WFDD	WAIT UNTIL THE COMPLETION OF THE READ FROM THE	
0556	D1	0551	1490		B	DS4	ERROR SO RETRY	
0557	60		1491		XY			
0558	00 00	0800	1492		BL	LSN	INCREMENT SECTOR NO.	DES
055A	F8	0007	1493		DL	#07	INCREMENT SECTOR # BY 7	
055B	ER	0014	1494		Dd	#14	EXIT SECTOR NO. 20	
055C	ES	0565	1495		B	DS2	NOT TO LINE 24 YET	DES
1497 **** END								
055D	60		1498		XY			
055E	CF 07	0787	1499		BL	RBUF	READ LAST BUFFER HEAD	
0560	4F	0080	1500		DL	#80	-80	
0561	CE 36	0736	1501		BL	CU2	CLEAN UP	
0563	E4	0564	1502		B	**1		
0564	5E		1503		RT			DES
0565	60		1505	DS2	XY			
0566	CF 07	0787	1506		RL	RBUF	TRANSFER LAST BUFFER READ TO SCREEN AREA	
0568	4F	0080	1507		Dd	#80	-80	
0569	21		1508		NOP			
056A	D1	0551	1509		B	DS4		
1512 * WAIT ROUTINE USED TO KILL LOTS OF TIME								
1513 * TIMES ARE APPROX DOUBLED BY CRT REFRESH								
056B	97(17)		1515	WT	PSHA		SAVE A	DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 52)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS				
056C	80 F2(72)	0020	1516		LAI	#20	OUTER LOOP (4.8 SEC)	
056E	97(17)		1517	WT1	PSHA		SAVE COARSE COUNTER	DES
056F	A0(20 70)	0000	1518		LAI	#00	INNER LOOP (12.288 MS )	DES
0570	80 21(61)	0001	1519	WT2	AISK	#01	INNER LOOP INCREMENT )	DES
0572	F9	0579	1520		B	WT3		DES
0573	96(16)		1521		POPA		COARSE COUNT	
0574	A0 21(61)	0001	1522		AISK	#01	OUTER LOOP INCREMENT	DES
0576	EF	056E	1523		B	WT1		DES
0577	96(16)		1524		POPA		RECOVER A	DES
0578	5E		1525	WTE	RT			DES
0579	CA 74	0578	1527	WT3	RL	WTE	KILL TIME	DES
057A	21		1528		NOP			DES
057C	F0	0570	1529		B	WT2		DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 53)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
			1531	ORG
			1533	**** COMMANDS FOR USE WITH THE FD ADDITION
			1534	**** ALL CMDS ARE ENTERED WITH THE CMNTROL KEY DEPRESSED
			1535	****
			1536	**** A ASCII MODE FOR R,W,C,AND L AND DD
			1537	**** X ATRA FAST COMMAND
			1539	**** S SET SECTOR
			1540	**** T SET TRACK
			1541	****
			1542	**** R READ SECTOR FROM DISK INTO CURRENT LINE
			1543	**** W WRITE CUPRENT LINE OUT TO DISK
			1544	****
			1545	**** L LOAD SCREEN FROM SPECIFIED TRACK - EBCDIC, 7 SCTR INCRMNTS
			1546	**** DD DUMP SCREEN TO SPECIFIED TRACK - 7 SECTOR INCRMNTS
			1547	**** M MODIFIED LOAD SCREEN- ASCII, 1 SCTR INCRMNTS
			1548	**** DM MODIFIED DUMP SCREEN - ASCII, 1 SCTR INCRMNTS
			1549	****
			1550	**** F WRITE FOPMAT FOR CURRENT TRACK
			1551	****
			1552	**** N NORMAL DATA MARK TO BE USED (#FB)
			1553	**** K DELETED SECTOR DATA MARK TO BE USED(#FB)
			1554	****
			1555	**** I READ IBM FORMAT, 128 BYTE EBCDIC
			1556	**** J WRITE IBM FORMAT, 128 EBCDIC
			1557	**** C CONTINUOUS SHOWING, CONSECUTIVE TRACKS
			1558	**** Q QUESTION CHC - READ CRC CMND
			1559	**** V VERIFY, READ COMPARE COMMAND
			1561	*** TABLES FOR FLOPPY DISK FUNCTION KEYS
			1562	*** THIS TABLE MUST BE ALIGNED AT LOC.0, MOD 64

0580	BE	0041	1564	FDCX	DW	.A.	KEY NO. 43
0581	3C	0043	1565		DW	.C.	KEY NO. 65
0582	98	0044	1566		DW	.D.	KEY NO. 45
0583	89	0046	1567		DW	.F.	KEY NO. 46

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 54)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
0584	87	0048	1568	DW .H. KEY NO. 48
0585	86	0049	1569	DW .I. KEY NO. 30
0586	85	004A	1570	DW .J. KEY NO. 49
0587	84	004B	1571	DW .K. KEY NO. 50
0588	83	004C	1572	DW .L. KEY NO. 51
0589	82	004D	1573	DW .M. KEY NO. 49
058A	81	004E	1574	DW .N. KEY NO. 68
058B	80	0051	1575	DW .O. KEY NO. 23
058C	80	0052	1576	DW .R. KEY NO. 26
058D	AC	0053	1577	DW .S. KEY NO. 44
058E	80	0054	1578	DW .T. KEY NO. 27
058F	A9	0056	1579	DW .V. KEY NO. 66
0590	80	0057	1580	DW .W. KEY NO. 24
0591	47	0058	1581	DW .X. KEY NO. 64
0592	7F	0080	1582	DW #80 - = END OF TABLE

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
			1584	*** ROUTINE ADDRESSES
			1585	RTNA EQU *-4
0593	00 8C	0600	1586	DW0 ASCII .A.
0595	3C 8D	060C	1587	DW0 CTN .C.
0597	08 8C	0608	1588	DW0 WS .D.
0599	00 96	0600	1589	DW0 FMT .F.
059A	44 8H	05C4	1590	DW0 HDR .H. (READ ID)
059D	62 8H	05E2	1591	DW0 RIBM .I.
059F	70 8B	05F0	1592	DW0 WIBM .J.
05A1	34 8D	06H4	1593	DW0 ODMK .K.
05A3	26 8C	0626	1594	DW0 LS .L.
05A5	00 91	0880	1595	DW0 MTX .M.
05A7	31 8D	06H1	1596	DW0 NDMK .N.
05A9	00 8D	0680	1597	DW0 QCRC .Q.
05AB	2A 8C	062A	1598	DW0 RD .R.
05AD	50 8C	0650	1599	DW0 SSC .S.
05AF	57 8C	0657	1600	DW0 STR .T.
05B1	3C 8C	063E	1601	DW0 HCMP .V.
05B3	34 8C	0634	1602	DW0 ART .W.
05B5	04 8C	0604	1603	DW0 XFST .X.

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 55)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
			1605	**** NOT NORMAL KEY SO SEE IF CONTROL KEY		
0587	09 HU	058D	1607	FLPY	BHF	7,FLPI NOT ALPHABETIC
0589	7D		1608		L	ALPHABETIC SO FORCE TO UPPERCASE
058A	A4(24)A0	005F	1609		ANI	#5F
058C	75		1610		S	
058D	FE(9E BE)	01A5	1611	FLPI	BL	BTBL CHECK FLOPPY FUNCTION TABLE
058E	00 8B	0580	1612		DWO	FDCK
05C0	0F	058F	1613		DW	RTNA,LO
05C1	21		1614		NOP	
05C2	3C 2E	073C	1615		R	NK9
			1617	* READ ID ROUTINE		
			1618	**** FORMAT IH READ FROM CURRENT TRACK		
			1619	**** NIH READ FROM SPECIFIED TRACK		
		05C4	1621	HDR	EQU	*
05C4	47(37 60)	0001	1622		LZI	1
05C5	8A(0A)0C	00F3	1623		LXI	RSA
05C7	86(06)8B	FF44	1624		LAI	-188
05C9	75		1625		S	
05CA	CE 26	0726	1626		HL	SU2
05CC	FF	0000	1627		DW	#00
05CD	F9(99 89)	042E	1628	HDR1	BL	SET
05CE	FF	0000	1629		DW	HAL
05CF	3E	00C1	1630		DW	BAUR
05D0	F5	000A	1631		DW	%RID
05D1	FF(9F BF)	0497	1632		HL	WFDD
05D2	C0	05C0	1633		H	HDR1
05D3	02 00	0900	1634		BL	RID
05D5	4B	FF44	1635		DW	-188
05D6	E8(88 AB)	038C	1636		HL	DECL
05D7	CE 20	0720	1637		BL	CUI
05D9	0A	05DA	1638		B	*+1
05DA	47(37 60)	0001	1639		LZI	1
05DB	8A(0A)0C	00F3	1640		LXI	RSA
05DD	86(06)03	FFFC	1641		LAI	-4
						IBM FORMAT 188 BYTES PER REDORD CHANGE RECORD SIZE A
						SET UP READ ID CMND
						PETRY IF REQUIRED CONVERT DATA TO READABLE , PUT ON SCRIN
						LEAVE CURSOR AT BEGIN OF ORIGINAL LINE

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 56)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
05DF	35		1642	S		RESTORE RECORD SIZE A
05E0	5F 8C	065F	1643	R	EX1	
			1645	* READ IHM FORMAT - 128 BYTES OF EBCDIC DATA		
		05E2	1646	RIRM	EQU	*
05E2	CE 14	0714	1647		RL	SU1 STEP LOAD HEAD , GET SCREEN ADDRESS
05E4	CF 00	0780	1648		HL	READ
05E6	E7(87 A7)	0380	1649	RIB1	RL	INCL INCREMENT NEXT LINE POINTER FOR BLL
05E7	CF 07	0787	1650		RL	RBUF TRANSFER 128 BYTES OF BUFK TO SCREEN
05E9	7F	FF80	1651		DW	-128
05EA	CE 00	0700	1652		BL	RLL STORE BLANKS TO END OF LINE
05EC	CE 20	0720	1653		RL	CUI UNLOAD HEAD , STRT CURSOR
05EF	5F 8C	065F	1654		R	EX1
			1656	* WRITE IRM FORMAT - 128 BYTES OF EBCDIC DATA		
		05F0	1657	WIRM	EQU	*
05F0	CE 14	0714	1658		HL	SU1 STEP, LOAD, GET SCREEN ADDRESS
05F2	CF 38	0788	1659		RL	WHUF LOAD BUFK WITH 128 BYTES FROM SCREEN AREA
05F4	7F	FF80	1660		DW	-128
05F5	CF 31	0791	1661		BL	WRIT
05F7	E7(87 A7)	0380	1662		RL	INCL ADVANCE NEXT LINE POINTER
05F8	CF 20	0720	1663		RL	CUI UNLOAD HEAD, START CURSOR
05FA	5F 8C	065F	1664		B	EX1

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 57)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS			
			1666	ORG			
			1667	• ROUTINE TO SET ASCII MODE FLAG			
			1668	• CURRENTLY USED IN .C., .P., AND .W. CMNDS			
0600	B3(33 42)	0600	1670	ASCII	EQU	•	
0601	80 12	0021	1671	LXI	FLAG		
0603	DF	0006	1672	SB	6		SET ASCII MODE FLAG
		065F	1673	B	EX1		
			1675	• ROUTINE TO DECREASE DELAY BETWEEN FRAMES TO APPROX 250 MS			
0604	B3(33 42)	0604	1677	XFST	EQU	•	
0605	H0 11	0021	1678	LXI	FLAG		
0607	DF	0007	1679	SB	7		
		065F	1680	B	EX1		
			1682	**** DUMP THE SCREEN CONTENTS TO THE DISK			
			1683	**** FORMAT: ID	DUMP TO THE CURRENT TRACK		
			1684	****	NID	DUMP TO THE SPECIFIED TRACK	
0608	B3(33 42)	0021	1685	WS	LXI	FLAG	DES
0609	03 8F	060F	1686	HBT	5,WS1	IS THIS SECOND .D. ?	DES
0608	80 13	0035	1687	SB	5	SET FIRST .D. FLAG	DES
060C	00 82	0100	1688	H	PACK		
060F	CE 26	0726	1689	WS1	BL	SUZ	DES
0611	F7	3008	1690	DW	#08	START WITH SECTOR 8	
0612	60		1691	XY			
0613	60		1692	WS2	XY		
0614	CF 38	0788	1693	9L	WBUF	COPY THE CURRENT LINE TO THE BUFFER	
061A	4F	0080	1694	DW	#80	-80	
0617	F9(99 89)	042E	1695	WS3	BL	SET	SET UP DMAC TO TRANSFER BUFFER TO DISK
0614	FF	0000	1696	DW	BAL		
0619	3F	0041	1697	DW	BAUW		
061A	FA	0004	1698	DW	%WS		
061H	FF(9F BF)	0492	1699	BL	WFDD	WAIT UNTIL THE WRITE TO THE DISK IS COMPLETED	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 58)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS			
061C	97	0617	1700	B	WS3	ERROR SO RETRY	
061D	60		1701	XY			
061E	00 00	0800	1702	BL	LSN	INCREMENT SECTOR NO.	DES
0620	FA	0007	1703	DW	#07	INCREMENT SCIRS BY 7	
0621	EA	0014	1704	DW	#14	EXIT SECTOR NO. 20	
0622	93	0613	1705	B	WS2		DES
0623	CE 36	0736	1706	BL	CU2	CLEAN UP	
0625	DF	065F	1707	B	EX1		
			1709	**** LOAD SCREEN FROM DISK			
			1710	**** FORMAT: IL	LOAD SCREEN FROM CURRENT TRACK		
			1711	****	NIL	LOAD SCREEN FROM SPECIFIED TRACK	
0626	CA 4E	054E	1712	LS	EQU	•	DES
062H	21		1713	HL	.L		DES
0624	DF	065F	1714	NOP			DES
			1715	B	EX1		
			1717	**** LOAD SECTOR INTO CURRENT LINE			
			1718	**** FORMAT: IR	READ CURRENT TRACK, SECTOR		
			1719	****	NIR	HEAD CURRENT TRACK, SPECIFIED SECTOR	
062A	CF 14	062A	1720	HD	EQU	•	
062C	CF 00	0714	1721	BL	SU1	SET UP TRACK, SECTOR, LOAD HEAD	
		0780	1722	RL	READ	READ SECTOR INTO SCREEN AREA	
			1723	• Z-X ADDRESS	START OF SCREEN LINE ON ENTRY TO RBUF		
062E	CF 07	0787	1724	3L	RBUF	TRANSFER DATA TO SCREEN AREA	
0630	4F	FF80	1725	DW	-80		
0631	CE 20	0720	1726	RL	CU1	UNLOAD HEAD, TURN CURSOR ON	
0633	DF	065F	1727	B	EX1		
			1730	**** WRITE CURRENT LINE TO DISK			
			1731	**** FORMAT: IW	WRITE INTO CURRENT SECTOR, TRACK		
			1732	****	NIW	WRITE INTO SPECIFIED SECTOR, CURRENT TRACK	
0634	CE 14	0634	1733	WRT	EQU	•	
0636	CF 3H	0788	1734	BL	SU1		
0638	4F	FF80	1735	RL	WBUF	FILL BUFR FROM SCREEN	
0639	CF 31	0781	1736	DW	-80		
			1737	RL	WRT		

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 59)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
063E	CE 20	0720	1738	RL	CU1
063D	DF	065F	1739	R	EX1
1742 * COMPARE RECORD ON DISK WITH READ/WRITE BUFFER (BUFR)					
063E	CE 14	063E	1744	RCMP	EQU *
0640	F9(99 B9)	0714	1745	BL	SUI
0641	FF	042E	1746	RCM1	BL SET
0642	9E	0000	1747	DM	BAL
0643	F9	0041	1748	DM	BAUW
0644	FF(9F BF)	0006	1749	DM	WNC
0645	C0	0492	1750	BL	WDD
0646	9H(1H)	0647	1751	R	RCM1
0647	8A(0A)C9	0036	1752	PSHX	
0648	0D CD	0036	1753	LXI	FNS
0649	0D 3B	0640	1754	HBF	3,RCM2
064A	A2(22)	0638	1755	HL	OST
064E	66 8E	05E6	1756	RCM2	POPX
			1757	R	RIB1
			1759	**** SET SECTOR TO SPECIFIED VALUE	
			1760	**** FORMAT: IS INCREMENT CURRENT SECTOR VALUE	
			1761	**** NIS SET SECTOR TO SPECIFIED VALUE	
0650	FA(9A BA)	0650	1762	SSC	EQU *
0651	CE	07DC	1763	BL	SNE
0652	DF	0031	1764	DM	SCTR
0653	00 12	065F	1765	R	EX1
0655	21	0812	1766	HL	INCS
0656	UF	065F	1767	NOP	
			1768	R	EX1
			1771	**** SET TRACK TO SPECIFIED VALUE	
			1772	**** FORMAT: IT INCREMENT CURRENT TRACK NUMBER	
			1773	**** NIT SET TRACK TO SPECIFIED VALUE	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 60)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
0657	FA(9A BA)	0657	1774	STR	EQU *
0658	CF	070C	1775	RL	SNE
0659	DF	0030	1776	DM	TRK
065A	86(36 45)	065F	1777	R	EX1
065B	7D	0030	1778	LXI	TRK
065C	42		1779	L	
065D	35		1780	INCA	
065E	DF		1781	S	
		065F	1782	R	EX1
			1785	**** COMMON RETURN FOR FD COMMANDS	
065F	B3(33 42)	0021	1786	EX1	LXI FLAG
0660	9C(1C)	0005	1787	RB	5
0661	80 1C	0004	1788	RB	4
0663	00 82	0100	1789	R	BACK

DES



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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 61)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
			1790	ORG	
			1791	* HEAD SECTOR AND CHECK CRC. NO DATA TRANSFERED	
0680	CE 14	0680	1793	QCRC	EQU *
0682	F9(99 B9)	0714	1794	RL	SU1
0683	FF	042E	1795	RL	SET
0684	3E	0000	1796	DW	BAL DUMMY PARAM.
0685	F1	00C1	1797	DW	RAUR DUMMY PARAM.
0686	FF(9F HF)	000E	1798	DW	QCRC CHECK CRC COMMAND
0687	82	0492	1799	RL	#FDD
0688	98(1H)	0682	1800	B	QCR1 ERROR, SO RETRY
0689	AA(0A)C9	1801	1801	PSHX	SAVE LOWER SCREEN ADDRESS
068B	06 A6	0036	1802	LXI	FNS
068D	9E(1E)	06A6	1803	HRT	2,QCR3 BRANCH IF CRC ERROR
068E	86(06)H8	1804	1804	POPX	RESTORE SCREEN ADDRESS
0690	77	0047	1805	QCR2	LAI .G. OUTPUT MESSAGE
0691	86(06)5C	1806	1806	SN	
0693	77	004F	1807	LAI	.O.
0694	86(06)DF	1808	1808	SN	
0696	77	0020	1809	LAI	BLNK
0697	86(06)BC	1810	1810	SN	
0699	77	0043	1811	LAI	.C.
069A	86(06)AD	1812	1812	SN	
069C	77	0052	1813	LAI	.R.
069D	86(06)HC	1814	1814	SN	
069F	77	0043	1815	LAI	.C.
06A0	CE 00	1816	1816	SN	
06A2	CE 20	0700	1817	BL	BLL
06A4	5F 8C	0720	1818	BL	CU1
		065F	1819	B	EX1
06A6	9E(1E)		1821	QCR3	POPX
06A7	86(06)B1	004E	1822	LAI	.N.
06A9	77		1823	SN	
06AA	86(06)B0	004F	1824	LAI	.O.
06AC	77		1825	SN	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 62)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
06AD	86(06)DF	0020	1826	LAI	BLNK
06AF	37		1827	SN	
06B0	8E	068E	1828	B	QCR2
			1830	**** N COMMAND -- SET DATA MARK TO #FB (NORMAL VALUE)	
06B1	87(07)04	06B1	1832	NDMK	EQU *
06B3	85	00FB	1833	LAI	#FB
		06B6	1834	B	DMK
			1836	**** K COMMAND -- SET DATA MARK TO #FB (DELETED SECTOR DATA MARK)	
06B4	86(06)07	06B4	1837	DDMK	EQU *
06B6	8A(0A)00	00FA	1838	LAI	#FB
06B8	87(37 80)	00F1	1839	DMK	LXI SMC
06B9	35	0001	1840	LXI	1
06BA	00 82	0100	1841	S	
			1842	B	BACK
			1846	* NC COMMAND FOR CONTINUOUS READ	
			1847	* STARTS WITH CURRENT TRACK NUMBER	
			1848	* ENDS WITH TRACK NO. (N-1) WHERE N WAS INPUT PRIOR TO C CMND	
			1849	* LOOPS BACK TO BEGINNING TRACK - EXITS WHEN A KEY IS ENTERED	
			1850	* NOTE! START TRACK NO. MUST BE LESS THAN ENDING TRACK NO.	
06BC	8A(9A 8A)	070C	1852	CTN	RL SNE
06BD	01	002E	1853	DW	T20
06BF	C4	06C4	1854	H	CTN3
06B8	86(06)H2	0040	1855	CTN2	LAI 77
06C1	8A(0A)01	002E	1856	LXI	T20
06C3	75		1857	S	STOP TRACK
06C4	86(36 45)	0030	1859	CTN3	LXI TRK
06C5	70		1860	L	
06C6	8A(0A)02	0020	1861	LXI	TEMP
06C8	75		1862	CTN1	S
					SAVE ENDING TRACK NUMBER
					DEFAULT VALE FOR TRK 76
					STOP TRACK
					NO ENTRY. DEFAULT TO 77
					SAVE STARTING TRACK NUMBER

DES  
DES  
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DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 63)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	DES
06C9	00 20	0820	1863	PL M1	DES
06CB	8A(0A)D2	0020	1864	LXI TEMP	DES
06CD	7D		1865	L	DES
06CE	80 45(45)	0030	1866	LXI THK	DES
06D0	C8	06C8	1867	R CTN1	DES

RESET TO STARTING TRACK

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 64)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
			1869	ORG
			1870	* SUBROUTINE TO STORE BLANKS TO END OF CRT LINE
			1871	* USES 'LINE' TO DETERMINE END - MUST BE WITHIN 128 BYTES
0700	58		1873	BLL PSHL SAVE RETURN
0701	59		1874	XL SAVE SCREEN ADDRESS IN L
0702	EC(RC AC)	039E	1875	HL LLIN Z,X SET TO BEGIN ADDRESS OF NEXT LINE
0703	54		1876	XAX SAVE LOWER ADDRESS IN A
0704	8A(0A)D1	002E	1877	LXI T20
0706	75		1878	S SAVE IN TEMP FOR LATER COMPARISON
0707	59		1879	BLL1 XL GET SCREEN ADDRESS, SAVE TEMP ADDRESS
0708	H6(06)DF	0020	1880	LAI BLNK
070A	37		1881	SH STORE ONE BLANK, INCREMENT TO NEXT LOC
070B	AD	0700	1882	R
070C	L9(89 A9)	030A	1883	HL INZS PAGE BOUNDARY - INCREMENT Z
070D	54		1884	BLL2 XAX LOWER SCREEN ADDRESS IN A
070E	48		1885	LXA RESTORE X
070F	59		1886	XL SAVE SCREEN ADDRESS, GET TEMP ADDRESS
0710	28 A7	0707	1887	BNE BLL1 COMPARE ADDRESSES
0712	5A		1888	POPL GET RETURN
0713	5E		1889	HT
			1891	**** SETUP FOR READ, WRITE ONE SECTOR
0714	FA(9A 8A)	07DC	1892	SUI BL SNE IF NUMBER ENTERED STORE IT INTO SCTR
0715	CE	0031	1893	DW SCTR
0716	97	0717	1894	H *+1 NONE ENTERED SO NO CHANGE IN SECTOR
0717	C9 52	0402	1895	BL TDIF COMPUTE # OF STEPS TO BE TAKEN
0719	F8(9H 8H)	0404	1896	BL STEP STEP TO DESIRED TRACK
071A	CA 10	0510	1897	BL HLD LOAD HEAD
071C	EE(8E AE)	0384	1898	BL RLC BLANK CURSOR
071D	EC(8C AC)	037F	1899	BL LLIN LOAD ADDRESS OF START OF NEXT LINE
071E	F6(86 A6)	0379	1900	HL DER0 GET ADDRESS OF START OF CURRENT LINE
071F	5F		1901	HT

1904 \*\*\*\* CLEANUP OF READ, WRITE ONE SECTOR

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 65)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS			
0720	CA 24	0524	1905	CU1	BL	UNLD	UNLOAD HEAD
0722	EC(AC AC)	039F	1906		BL	LLIN	LOAD ADDRESS OF START OF NEXT LINE
0723	E7(87 A7)	0380	1907		BL	INCL	
0724	EF(8F AF)	03C0	1908		BL	DPC	TURN CURSOR ON AND POINT IT TO START OF LINE
0725	1E		1909		RTS		
			1911	**** SET UP FOR DUMP, LOAD ENTIRE SCREEN AREA			
0726	FA(9A BA)	070C	1912	SH2	HL	SNE	IF NUMBER ENTERED STORE INTO TRACK
0727	CF	0030	1913		DM	TRK	
0728	A9	0729	1914		R	**1	
0729	AB(28)		1915		LAL		SCRN AREA START SECTOR
072A	BA(0A)CE	0031	1916		LXI	SCTR	
072C	75		1917		S		
072D	C9 52	0402	1918		RL	TDIF	CALCULATE NUMBER TF TRACKS TO BE STPPED
072F	FA(93 44)	0404	1919		HL	STEP	STEP TO DESIRED TRACK
0730	CA 10	0510	1920		HL	HLD	LOAD HEAD
0732	EE(6E AE)	0384	1921		HL	BLC	BLANK CURSOR
0733	5F		1922		SC		
0734	F5(95 B5)	0287	1923		HL	**CL	ADDRESS STRT OF SCRNM, HOME CURSOR
0735	5E		1924		RT		
			1926	**** CLEAN UP FOLLOWING LOAD, DUMP ENTIRE SCREEN AREA			
0736	CA 24	0524	1927	CU2	BL	UNLD	UNLOAD HEAD
0738	5F		1928		SC		
0739	F5(95 B5)	0287	1929		HL	**CL	RESET LINE TO START FO SCREEN AREA
073A	EF(8F AF)	03C0	1930		BL	DPC	RESET CSH TO START AND TURN IT ON
073B	1E		1931		RTS		
			1934	* IF NOT ONE OF FLOPPY DISK FUNCTIONS ENTER HERE			
073C	86(06)2F	0000	1936	AK9	LAI	#D0	
073E	20		1937		ASK		
073F	00 82	0100	1938		B	BACK	
0741	A7(27)09	00F6	1939		AISK	#F6	
0743	C7	0747	1940		B	CNUM	NUMERIC ENTRY
0744	21		1941		NOP		
0745	00 82	0100	1942		B	BACK	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 66)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS			
			1943	**** NUMBER ENTRY			
0747	7D		1944	CNUM	L		LOAD THE DIGIT ENTERED
0748	A4(24)F0	000F	1945		ANI	#0F	
074A	8A(0A)CD	0032	1946		LXI	DBL	SHIFT INTO DIGIT BUFFER
074C	7D 77		1947		AN		
074E	75		1948		S		
074F	83(33 42)	0021	1949		LXI	FLAG	SET NUMBER ENTRY FLAG
0750	H0 14	0004	1950		SB	4	
0752	00 82	0100	1951		B	BACK	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 67)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
			1953	ORG	
			1955	**** SUBROUTINE READ -- READ CURRENT SECTOR INTO SCREEN AREA	
0780	F9(99 B9)	042E	1956	READ BL SET	SET UP DMAC
0781	FF	0000	1957	DW BAL	
0782	3E	00C1	1958	DW RAUR	
0783	FD	0002	1959	DW %RS	
0784	FF(9F BF)	0492	1960	HL WFDD	WAIT UNTIL THE READ FROM DISK TO BUFFER IS COMD
0785	80	0780	1961	B READ	OPERATION NOT COMPLETED SO RETRY
0786	5E		1962	RT	
			1965	**** SUBROUTINE RBUF -- TRANSFER BUFFER TO SCREEN AREA	
			1966	**** Z,X ADDRESS START OF LINE IN SCREEN AREA ON ENTRY	
			1967	**** Y = # OF BYTES TO BE TRANSFERED	
			1968	**** CALLING SEQUENCE:	
			1969	**** BL RBUF	
			1970	**** DW #NN WHERE #NN IS THE NEGATIVE OF THE NO. OF BYTES	
0787	AR(28)		1973	RBUF LAL	GET # OF BYTES TO BE READ
0788	5B		1974	PSHL	
0789	59		1975	XL	
078A	92(12)FD	0100	1976	LZI RUFH	ADDRESS START OF BUFFER
078C	AA(0A)7F	0100	1977	LXI RUFH	
078E	55		1978	RBU2 XAY	
078F	38		1979	LNXL	
0790	94	0794	1980	B RBU3	
0791	57		1981	XAL	INCREMENT L IF PAGE BNDRY CROSSED
0792	42		1982	INCA	
0793	57		1983	XAL	
		0794	1984	RBU3 EQU *	
0794	9B(1B)		1985	PSHX	SAVE
0795	B3(33 42)	0021	1986	LXI FLAG	
0796	02 AF	07AF	1987	RBT 6,RBU4	
0798	9E(1E)		1988	POPX	
0799	58		1989	PSHL	
079A	46		1990	RAL	C <- BIT SPECIFYING WHICH TABLE TO BE USED

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 68)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
079A	86(06)95	0A80	1991	LAI	ETAU,UO
079D	66		1992	SKC	
079E	86(06)94	0A00	1993	LAI	ETAL,UO
07A0	48		1994	LLA	
07A1	AB(28)		1995	LAL	LOAD CORRESPONDING BYTE FROM ATBLE
07A2	5A		1996	POPL	
07A3	33		1997	RBU5 SNXL	STORE INTO SCREEN AREA
07A4	A8	07A8	1998	B RBU1	
07A5	57		1999	XAL	
07A6	42		2000	INCA	
07A7	57		2001	XAL	
07A8	55		2002	RBU1 XAY	
07A9	42		2003	INCA	INCREMENT COUNT
07AA	22 8E	078E	2004	BNZ RBU2	NOT DONE YET
07AC	59		2005	XL	
07AD	5A		2006	POPL	
07AE	5E		2007	RT	
				*	
07AF	A2(22)		2009	RBU4 POPX	
07B0	A3	07A3	2010	B RBU5	
			2014	**** SUBROUTINE WRIT -- WRITE LINE TO SECTOR	
07B1	F9(99 B9)	042E	2015	WRIT BL SET	SET UP DMAC AND START FDC
07B2	FF	0000	2016	DW BAL	
07B3	BE	0041	2017	DW BAUM	
07B4	FR	0004	2018	DW %WS	
07B5	FF(9F BF)	0492	2019	BL WFDD	WAIT UNTIL TRANSFER FROM BUFFER TO DISK IS DO
07B6	B1	0761	2020	B WRIT	OPERATION NOT COMPLETED SO RETRY
07B7	5E		2021	RT	
			2024	**** SUBROUTINE WBUF -- TRANSFER LINE TO WRITE BUFFER	
			2025	**** Z,X ADDRESS START OF LINE IN SCREEN AREA ON ENTRY	
07B8	AB(28)		2026	WBUF LYL	GET # OF BYTES TO BE WRITTEN

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 69)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
07B9	86(06)7F	0100	2027	LAI	BUFR,L
07BH	86(06)FD	0100	2028	LAI	BUFR,U
07BD	58		2029	PSHL	
07BE	55		2030	XAY	
07BF	55		2032	WBU1	XAY
07C0	38		2033	LNXL	
07C1	C5	07C5	2034	H	WBU2
07C2	57		2035	XAL	
07C3	42		2036	INCA	
07C4	57		2037	XAL	
		07C5	2038	WBU2	EQU
07C5	9B(18)		2039	PSHX	SAVE
07C6	93(33 42)	0021	2040	LXI	FLAG
07C7	02 DA	07DA	2041	RBT	6,WBU4
07C9	9F(1E)		2042	POPX	
07CA	86(06)93	09H0	2043	LAI	ATE,U0
07CC	58		2044	PSHL	
07CD	A8(28)		2045	LAL	
07CE	5A		2046	POPL	
07CF	33		2047	WBU5	SNXL
07D0	04	07D4	2048	B	WBU3
07D1	57		2049	XAL	
07D2	42		2050	INCA	
07D3	57		2051	XAL	
07D4	55		2052	WBU3	XAY
07D5	42		2053	INCA	
07D6	22 HF	07BF	2054	HNZ	WBU1
07D8	5A		2055	FOPL	
07D9	5E		2056	RT	
07DA	A2(22)		2058	WBU4	POPX
07DB	CF	07CF	2059	B	WBU5

2062 \*\*\*\* SUBROUTINE SNE -- STORE NUMBER ENTRY INTO SPECIFIED LOCATION

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 70)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
			2063	**** NUMBER ENTERED INTO DIGIT BUFFER IS CONVERTED TO BINARY AND STORED	
			2064	**** INTO THE SPECIFIED LOCATION	
			2065	**** CALLING SEQUENCE:	
			2066	**** BL	SNE
			2067	**** DW	<LOCATION WHERE VALUE IS TO BE STORED>
			2068	**** B	<ENTRY MADE>
07DC	A8(28)		2069	SNE	LYL
07DD	93(33 42)	0021	2070	LXI	FLAG
07DE	0C F2	07F2	2071	RRF	4,SNE1
07E0	99(19)	0004	2072	RB	4
07E1	8A(0A)CC	0033	2073	LXI	DBU
07E3	7D		2074	L	
07E4	5D		2075	RC	
07E5	46		2076	RAL	MSD * 2
07E6	75		2077	S	
07E7	46		2078	RAL	MSD * 4
07E8	46		2079	RAL	MSD * 8
07E9	0F		2080	A	MSD * 10
07EA	51		2081	DECA	POINT TO LSD
07EB	0F		2082	A	MSD * 10 * LSD
07EC	60		2083	XY	
07ED	76		2084	SNXY	
07EE	AD(2D 70)	0000	2085	LAI	#00
07EF	77		2086	SN	
07F0	75		2087	S	
07F1	1E		2088	RTS	
07F2	1C		2089	SNE1	RSKS
					NO ENTRY MADE

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 71)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
			2091	ORG	
			2092	* ROUTINE TO INCREMENT SECTOR NOS. FOR L AND O COMMANDS	DES
			2093	* SECTOR INCREMENT AND SECTOR STOP READ MAY BE CHANGED	DES
			2094	* ALSO CHANGE SECTOR START IN ROUTINE SU2	DES
			2096	* CALLING SEQUENCE:	
			2097	* BL LSM	
			2098	* DW #07 INCREMENTING VALUE - MUST BE ODD # < 11	
			2099	* DW #XX EXIT WHEN THIS SECTOR IS ENCOUNTERED	
0800	A8(28)		2101	LSN LAL	
0801	8A(0A)CE	0031	2102	LXI SCTR	
0803	6F		2103	A	INCREMENT SCTR NO.
0804	75		2104	S	
0805	86(06)1A	FFES	2105	LAI -27	DES
0807	6F		2106	A	DES
0808	25 8D	080D	2107	BN LSN1	DES
080A	89(39 61)	0001	2108	AISK #01	IF NEG. PASSED SECTOR 26
080B	61		2109	NOP	
080C	75		2110	S	DES
080D	A8(28)		2111	LSN1 LAL	SECTOR NO. - 26 = NEW SECTOR
080F	28 91	0811	2112	HNE LSN2	PICK UP EXIT SECTOR NO.
0810	1C		2113	RSK\$	DES
0811	1C		2114	LSN2 RTS	TIME TO GET OUT
			2115	**** SURROUTINE INCS -- INCREMENT SECTOR IN SCTR	GO DO IT AGAIN, NOT DONE
0812	8A(0A)CE	0031	2116	INCS LXI SCTR	DES
0814	7D		2117	L	DES
0815	42		2118	INCA	
0816	75		2119	S	
0817	A5(25)1A	FFES	2120	AISK -27	
0819	5E		2121	RT	
			2122	**** END OF TRACK SO GO TO NEXT ONE	
081A	86(06)FE	0001	2123	LAI #01	SCTR <- 1
081C	74		2124	SD	
081D	6F		2125	A	INCREMENT TRACK
081E	75		2126	S	
081F	5E		2127	RT	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 72)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
0820	H3(33 42)	0021	2131	M1 LXI FLAG	
0821	02 B3	0833	2132	BBT 6,M3	BRANCH IF ASCII MODE
0823	CA 4E	054E	2133	BL ,L	
0825	33(33 42)	0021	2134	M2 LXI FLAG	
0826	01 B7	0837	2135	BBT 7,M4	
0828	CA 6B	056B	2136	BL WT	DELAY APPROX 5 SEC
082A	36(36 45)	0030	2137	M5 LXI TRK	
082B	7D		2138	L	
082C	42		2139	INCA	INCREMENT TO NEXT TRACK
082D	75		2140	S	DES
082E	8A(0A)D1	002E	2141	LXI T20	DES
0830	28 A0	0820	2142	HNE M1	HAVE 20 TRACKS BEEN READ
0832	5E		2143	RT	DES
0833	D1 05	0845	2145	M3 RL MTX0	
0835	21		2146	NOP	
0836	A5	0825	2147	B M2	
0837	FC(9C BC)	0537	2148	M4 BL VUEL	
0838	AF	0050	2149	DW #50	APPROX 250 MS
0839	21		2150	NOP	
083A	AA	082A	2151	B M5	
083B	5B		2153	DST PSHL	SAVE RETURN
083C	59		2154	XL	SAVE Z
083D	92(12)FD	0100	2155	LZI BUFR	READ/WRITE BUFFER
083F	8A(0A)7F	0100	2156	LXI BUFR	DES
0841	86(06)3A	00C5	2157	LAI #C5	DES
0843	77		2158	SN	E
0844	86(06)26	00D9	2159	LAI #D9	DES
0846	77		2160	SN	R
0847	77		2161	SN	R
0848	86(06)29	00D6	2162	LAI #D6	DES
084A	77		2163	SN	O
084B	86(06)26	00D9	2164	LAI #D9	DES
084D	77		2165	SN	R

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ROM ADDR	..CODE.. 11 12 13	ARG	SYMT NUMBER	SOURCE STATEMENTS			
			2205		ORG		
			2207	* SUBROUTINE TO MODIFY THE TRANSFER OF DATA TO ASCII CHARS.			
			2208	* THE TRANSFER IS DIRECTLY TO/FROM THE SCREEN IMAGE AREA			
			2209	* CHANGE RECORD SIZE R TO 80 BYTE RECORDS			
		0880	2211	MTX	EQU	*	
0880	01 05	0885	2213		BL	MTX0	
0882	21		2214		NOP		
0883	5F 8C	065F	2215		B	EX1	
			2217	* START AT BEGINNING OF SCREEN IMAGE AREA			
0885	CE 26	0726	2219	MTX0	RL	SU2	
0887	FD	0002	2220		DW	#02	START WITH SECTOR 2
0888	87(37 60)	0001	2221		LZI	1	
0889	83(33 42)	0021	2222		LXI	FLAG	
088A	93 A6	08A6	2223		BBT	5,MTXD	.D.-.M. REQUESTS MODIFIED SCREEN DUMP
088C	8A(0A)02	00FD	2224		LXI	RSB	
088E	86(06)4F	FFB0	2225		LAI	-80	2'S COMPLEMENT OF DESIRED RECORD SIZE
0890	75		2226		S		
0891	F9(99 B9)	042C	2228		BL	SET	.M. REQUESTS MODIFIED SCREEN LOAD
0892	7F	0080	2229		DW	DMAL	
0893	37	00C8	2230		DW	DAUR	
0894	FD	0002	2231		DW	%RS	
0895	FF(9F BF)	0492	2233	MTX3	BL	WFDD	WAIT FOR OPERATION TO COMPLETE
0896	84	08B4	2234		B	MTX2	ERROR SO RETRY
0897	00 00	0A00	2235		BL	LSN	INCREMENT SECTOR NUMBER

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 75)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMMER	SOURCE STATEMENTS		
0899	FE	0001	2236	DW	#01	INCREMENT SECTORS BY 1
089A	E5	001A	2237	DW	#1A	EXIT AT SECTOR 26
089B	B1	08B1	2238	R	MTX6	
2240 * RESTORE RECORD SIZE TO 128 BYTES						
089C	B7(37 60)	0001	2242	LZI	1	
089D	8A(0A)02	00FD	2243	LXI	RSB	
089F	86(06)7F	FFB0	2244	LAI	-128	2'S COMPLEMENT OF DESIRED RECORD LENGTH
08A1	75		2245	S		
08A2	CE 36	0736	2246	BL	CU2	CLEAN UP AND EXIT
08A4	A5	08A5	2247	B	*+1	
08A5	5E		2248	RT		
08A6	8A(0A)02	00FD	2250	MTXD	LXI	RSB
08A8	86(06)50	FFAF	2251	LAI	-81	2'S COMPLEMENT FOR WRITE RECORD SIZE
08AA	75		2252	S		
08AB	F9(99 89)	042E	2253	BL	SET	
08AC	7F	0080	2254	DW	DMAL	
08AD	B7	0048	2255	DW	DMAU	
08AE	FB	0004	2256	DW	%WS	
08AF	21		2257	NOP		
08B0	95	0895	2258	B	MTX3	
08B1	B3(33 42)	0021	2260	MTX6	LXI	FLAG
08B2	0B CC	08CC	2261	BBF	5,MTX1	DON'T LOAD ADDRESS REGS. IF READING
2263 * IF ERROR, RESET DMAD CHANNEL ADDRESSES TO START OF CRT LINE						
08B4	8A(0A)CE	0031	2265	MTX2	LXI	SCTR
08B6	7D		2266	L		CONVERT SECTOR # TO LINE #
08B7	D1 53	08D3	2267	BL	MPY5	

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 76)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS		
08B9	A5(25)81	007E	2268	AISK	#7E	SCREEN AREA OFFSET 88-5*STRT SCTR #
08BB	75		2269	S		
08BC	AD(2D 70)	0000	2270	LAI	#00	
08BD	44		2271	MOR		
08BE	4E 25	25	2272	OUT	LARL,DCD	LOWER 8 BITS OF ADDRESS
08C0	86(06)FB	0004	2273	LAI	#04	WRITE OPERATION
08C2	B3(33 42)	0021	2274	LXI	FLAG	
08C3	03 C7	08C7	2275	BBT	5,MTX4	
08C5	86(06)F3	000C	2276	LAI	#0C	READ OPERATION
08C7	8A(0A)D3	002C	2277	MTX4	LXI	SCPD
08C9	45		2278	MUL		
08CA	4E 26	26	2279	OUT	LARU,DCD	UPPER 6 BITS OF ADDRESS WITH CONTROL BITS
08CC	AD(2D 70)	0000	2281	MTX1	LAI	#00
08CD	4E 27	27	2282	OUT	LRLR,DCD	MAKE SURE DMA RL IS> RECORD SIZE 8
08CF	CA 42	0542	2283	RL	SETC	RESTART FDC OPERATION
08D1	21		2284	NOP		
08D2	95	0895	2285	B	MTX3	
2288 * MULTIPLY BY 5 SUBROUTINE						
2289 * ENTER WITH NO. IN A						
2290 * EXIT WITH RESULT IN A AND SCPD						
2291 * DATA ADDRESS IN X POINTING AT SCPD						
08D3	8A(0A)D3	002C	2293	MPY5	LXI	SCPD
08D5	75		2294	S		
08D6	5D		2295	RC		
08D7	46		2296	RAL		2*H
08D8	5D		2297	RC		OVERFLOW AT THIS POINT WILL BE THROWN AWAY
08D9	46		2298	HAL		4*H
08DA	0F		2299	A		5*H, OVERFLOW HERE WILL BE IN CARRY
08DB	75		2300	S		SAVE RESULT
08DC	5E		2301	RT		



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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 77)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
			2303	ORG	
			2305	* SUBROUTINE TO CONVERT DATA IN BUFFER TO ASCII-HEX FORMAT	
			2306	* AND TRANSFER IT TO THE CRT SCREEN AREA	
			2307	* CALLING SEQUENCE:	
			2308	BL RID	
			2309	DW -XX	WHERE XX IS THE NO. OF BYTES TO BE CNVRTD
0900	A8(28)		2311	RID	LAL COUNT IN A
0901	58		2312	PSHL	SAVE RETURN
0902	59		2313	XL	SAVE SCREEN POINTER
0903	92(12)FD	0100	2314	LZI BUFR	
0905	8A(0A)7F	0100	2315	LXI BUFR	
0907	55		2316	RID1 XAY	BYTE COUNT INTO Y
0908	02 28	0928	2317	BL LMXA	CONVERT LEFT HEX DIGIT
090A	59		2318	XL	POINT TO SCREEN AREA
090B	37		2319	SN	STORE LEFT ASCII-HEX DIGIT
090C	8E	090E	2320	R RID3	
090D	E9(89 A9)	030A	2321	RL INZS	
090E	59		2322	RID3 XL	
090F	02 25	0925	2323	HL PHXA	CONVERT RIGHT HEX DIGIT
0911	59		2324	XL	POINT AT SCREEN AREA
0912	37		2325	SN	STORE RIGHT ASCII-HEX DIGIT
0913	75	0915	2326	R RID4	
0914	E9(89 A9)	030A	2327	RL INZS	
0915	00 F2(72)	0020	2328	RID4 LAI #20	
0917	37		2329	SN	
0918	9A	091A	2330	R RID5	
0919	E9(89 A9)	030A	2331	RL INZS	
091A	59		2332	RID5 XL	
091B	13		2333	INCX	INCREMENT BUFR POINTER
091C	9E	091E	2334	R RID2	
091D	E9(89 A9)	030A	2335	HL INZS	PAGE BOUNDARY
091F	55		2336	RID2 XAY	
091F	42		2337	INCA	INCREMENT BYTE COUNTER
0920	22 87	0907	2338	RN2 RID1	NOT DONE , DO ANOTHER BYTE

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 78)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS	
0922	59		2339	XL	POINT TO SCREEN AREA
0923	5A		2340	POPL	GET RETURN
0924	5E		2341	RT	
			2343	* ROUTINE TO CONVERT BINARY TO ASCII-HEX FORMAT FOR READABILITY	
			2344	* IF TWO DIGITS DESIRED ALWAYS DO LEFT DIGIT FIRST	
			2345	* CALL ROUTINE WITH Z,X POINTING AT BYTE TO BE CONVERTED	
			2346	* EXIT WITH ASCII-HEX IN A	
0925	70		2348	RHXA L	
0926	45		2349	MDL	REPOSITION RIGHT DIGIT
0927	75		2350	S	OVERLAYS ORIGINAL BYTE .....
0928	86(06)FD	000F	2351	LHXA LAI #0F	
092A	45		2352	MDL	SET UP TO CAUSE OVERFLOW IF > 9
092B	A5(25)F9	0006	2353	AISK #06	SKIP IF N > 9
092D	A5(25)06	00F9	2354	AISK #F9	N <= 9
092F	61		2355	NOP	ALWAYS SKIPS
0930	A5(25)BE	0041	2356	AISK #41	30*N OR 40*(N-9)
0932	61		2357	NOP	
0933	5F		2358	RT	ASCII-HEX IN ACCUM

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 79)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS			
			2360	ORG			
			2361	**** ASCII TO EBCDIC TRANSLATION TABLE			
		0980	2362	ATE EQU *			
0980	8F	0040	2363	DW #40	DEL		
0981	8E	0071	2364	DW #71	CYCLES		DES
0982	8A	0075	2365	DW #75	RT BRACE		DES
0983	8C	0073	2366	DW #73	NBL VERTICAL BARS		DES
0984	88	0074	2367	DW #74	LFT BRACE		
0985	56	00A9	2368	DW #A9	Z		
0986	57	00A8	2369	DW #A8	Y		
0987	58	00A7	2370	DW #A7	X		
0988	59	00A6	2371	DW #A6	W		
0989	5A	00A5	2372	DW #A5	V		
098A	5B	00A4	2373	DW #A4	U		
098B	5C	00A3	2374	DW #A3	T		
098C	5D	00A2	2375	DW #A2	S		
098D	66	0099	2376	DW #99	R		
098E	67	0098	2377	DW #98	O		
098F	68	0097	2378	DW #97	P		
0990	69	0096	2379	DW #96	O		
0991	6A	0095	2380	DW #95	N		
0992	6B	0094	2381	DW #94	M		
0993	6C	0093	2382	DW #93	L		
0994	6D	0092	2383	DW #92	K		
0995	6E	0091	2384	DW #91	J		
0996	76	0089	2385	DW #89	I		
0997	77	0088	2386	DW #88	H		
0998	78	0087	2387	DW #87	G		
0999	79	0086	2388	DW #86	F		
099A	7A	0085	2389	DW #85	E		
099B	7B	0084	2390	DW #84	D		
099C	7C	0083	2391	DW #83	C		
099D	7D	0082	2392	DW #82	B		
099E	7E	0081	2393	DW #81	A		
099F	8F	0070	2394	DW #70	SHORT LFT SLASH		DES
09A0	92	005D	2395	DW #6D			
09A1	87	0078	2396	DW #78	UPSIDE DOWN V		DES
09A2	88	0077	2397	DW #77	RT BRACKET		DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 80)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS			
09A3	8D	0072	2398	DW #72	LFT SLASH		DES
09A4	89	0076	2399	DW #76	LFT BRACKET		DES
09A5	16	00E9	2400	DW #E9	Z		
09A6	17	00E8	2401	DW #E8	Y		
09A7	18	00E7	2402	DW #E7	X		
09A8	19	00E6	2403	DW #E6	W		
09A9	1A	00E5	2404	DW #E5	V		
09AA	1B	00E4	2405	DW #E4	U		
09AB	1C	00E3	2406	DW #E3	T		
09AC	1D	00E2	2407	DW #E2	S		
09AD	26	00D9	2408	DW #D9	R		
09AE	27	00D8	2409	DW #D8	O		
09AF	28	00D7	2410	DW #D7	P		
09B0	29	00D6	2411	DW #D6	O		
09B1	2A	00D5	2412	DW #D5	N		
09B2	2B	00D4	2413	DW #D4	M		
09B3	2C	00D3	2414	DW #D3	L		
09B4	2D	00D2	2415	DW #D2	K		
09B5	2E	00D1	2416	DW #D1	J		
09B6	36	00C9	2417	DW #C9	I		
09B7	37	00C8	2418	DW #C8	H		
09B8	38	00C7	2419	DW #C7	G		
09B9	39	00C6	2420	DW #C6	F		
09BA	3A	00C5	2421	DW #C5	E		
09BB	3B	00C4	2422	DW #C4	D		
09BC	3C	00C3	2423	DW #C3	C		
09BD	3D	00C2	2424	DW #C2	B		
09BE	3E	00C1	2425	DW #C1	A		
09BF	83	007C	2426	DW #7C			
09C0	90	006F	2427	DW #6F	?		
09C1	91	006E	2428	DW #6E	>		
09C2	91	007E	2429	DW #7E	=		
09C3	93	004C	2430	DW #4C	<		
09C4	A1	005E	2431	DW #5E	!		
09C5	95	007A	2432	DW #7A	!		
09C6	06	00F9	2433	DW #F9	9		
09C7	07	00F8	2434	DW #F8	8		
09C8	08	00F7	2435	DW #F7	7		

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 81)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
09C9	09	0016	2436	DW	#F6	6
09CA	0A	00F5	2437	DW	#F5	5
09CB	0B	00F4	2438	DW	#F4	4
09CC	0C	00F3	2439	DW	#F3	3
09CD	0D	00F2	2440	DW	#F2	2
09CE	0E	00F1	2441	DW	#F1	1
09CF	0F	00F0	2442	DW	#F0	0
09D0	0F	0061	2443	DW	#61	/
09D1	94	0043	2444	DW	#4B	.
09D2	9F	0060	2445	DW	#60	-
09D3	94	0069	2446	DW	#6B	.
09D4	B1	004E	2447	DW	#4E	+
09D5	A3	005C	2448	DW	#5C	*
09D6	A2	005D	2449	DW	#5D	)
09D7	B2	004D	2450	DW	#4D	(
09D8	B2	007D	2451	DW	#7D	'
09D9	AF	0050	2452	DW	#50	&
09DA	93	006C	2453	DW	#6C	%
09DB	A4	0054	2454	DW	#5B	\$
09DC	B4	007H	2455	DW	#7B	#
09DD	B0	007F	2456	DW	#7F	"
09DE	A5	005A	2457	DW	#5A	!
09DF	BF	0040	2458	DW	#40	SPACE
09E0	E0	001F	2459	DW	#1F	US
09E1	CA	0035	2460	DW	#35	RS
09E2	E2	0010	2461	DW	#10	GS
09E3	JD	0022	2462	DW	#22	FS
09E4	DA	0027	2463	DW	#27	ESC
09E5	C0	003F	2464	DW	#3F	SUB
09E6	E6	0019	2465	DW	#19	EM
09E7	E7	0018	2466	DW	#18	CAN
09E8	D3	0026	2467	DW	#26	FTB
09E9	C0	0032	2468	DW	#32	SYM
09EA	C2	003D	2469	DW	#3D	NAK
09EB	C3	003C	2470	DW	#3C	DC4
09EC	BF	0040	2471	DW	#40	DC3
09ED	ED	0012	2472	DW	#12	DC2
09EE	EF	0011	2473	DW	#11	DC1

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 82)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS		
09EF	EF	0010	2474	DW	#10	DLE
09F0	F0	000F	2475	DW	#0F	SI
09F1	F1	000E	2476	DW	#0E	SO
09F2	F2	000D	2477	DW	#0D	CH
09F3	F3	000C	2478	DW	#0C	FF
09F4	F4	000B	2479	DW	#0B	VT
09F5	DA	0025	2480	DW	#25	LF
09F6	FA	0005	2481	DW	#05	HT
09F7	E9	0016	2482	DW	#16	RS
09F8	D0	002F	2483	DW	#2F	REL
09F9	D1	002E	2484	DW	#2E	ACK
09FA	D2	002D	2485	DW	#2D	ENQ
09FB	C8	0037	2486	DW	#37	EOT
09FC	FC	0003	2487	DW	#03	ETX
09FD	FD	0002	2488	DW	#02	STX
09FE	FF	0001	2489	DW	#01	SOM
09FF	FF	0000	2490	DW	#00	NUL

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 83)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
			2491	ORG	
			2492	**** LOWER TABLE FOR TRANSLATION FROM ERCDIC TO ASCII	
			2493	ETAL EQU *	
0A00	00	0022	2494	DW #22	"
0A01	C2	0030	2495	DW #30	=
0A02	08	0027	2496	DW #27	'
0A03	8F	0040	2497	DW #40	#
0A04	DC	0023	2498	DW #23	#
0A05	C5	003A	2499	DW #3A	!
0A06	0F	0020	2500	DW #20	'
0A07	A1	005F	2501	DW #5E	UPSIDE DOWN V
0A08	A2	0050	2502	DW #5D	RT BRACKET
0A09	A4	0058	2503	DW #5B	LFT BRACKET
0A0A	82	0070	2504	DW #70	RT BRACE
0A0B	84	0078	2505	DW #7B	LFT BRACE
0A0C	83	007C	2506	DW #7C	ORL VERTICAL BARS
0A0D	A3	005C	2507	DW #5C	LFT SLASH
0A0E	81	007E	2508	DW #7E	CYCLES
0A0F	9F	0060	2509	DW #60	SHORT LFT SLASH
0A10	C0	003F	2510	DW #3F	?
0A11	C1	003E	2511	DW #3E	>
0A12	A0	005F	2512	DW #5F	_
0A13	0A	0025	2513	DW #25	%
0A14	03	002C	2514	DW #2C	'
0A15	0F	0020	2515	DW #20	
0A16	0F	0020	2516	DW #20	
0A17	0F	0020	2517	DW #20	
0A18	0F	0020	2518	DW #20	
0A19	0F	0020	2519	DW #20	
0A1A	0F	0020	2520	DW #20	
0A1B	0F	0020	2521	DW #20	
0A1C	0F	0020	2522	DW #20	
0A1D	0F	0020	2523	DW #20	
0A1E	00	002F	2524	DW #2F	/
0A1F	02	0020	2525	DW #20	-
0A20	0F	0020	2526	DW #20	
0A21	C4	003B	2527	DW #3B	!
0A22	06	0029	2528	DW #29	)

DES  
DES  
DES  
DES  
DES  
DES  
DES  
DES  
DES  
DES

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 84)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
0A23	05	002A	2529	DW #2A	*
0A24	0H	0024	2530	DW #24	\$
0A25	0F	0021	2531	DW #21	!
0A26	0F	0020	2532	DW #20	
0A27	0F	0020	2533	DW #20	
0A28	0F	0020	2534	DW #20	
0A29	0F	0020	2535	DW #20	
0A2A	0F	0020	2536	DW #20	
0A2B	0F	0020	2537	DW #20	
0A2C	0F	0020	2538	DW #20	
0A2D	0F	0020	2539	DW #20	
0A2E	0F	0020	2540	DW #20	
0A2F	09	0026	2541	DW #26	&
0A30	81	007E	2542	DW #7E	
0A31	04	002B	2543	DW #2B	*
0A32	07	0028	2544	DW #28	(
0A33	C3	003C	2545	DW #3C	<
0A34	01	002E	2546	DW #2E	.
0A35	0F	0020	2547	DW #20	
0A36	0F	0020	2548	DW #20	
0A37	0F	0020	2549	DW #20	
0A38	0F	0020	2550	DW #20	
0A39	0F	0020	2551	DW #20	
0A3A	0F	0020	2552	DW #20	
0A3B	0F	0020	2553	DW #20	
0A3C	0F	0020	2554	DW #20	
0A3D	0F	0020	2555	DW #20	
0A3E	0F	0020	2556	DW #20	
0A3F	0F	0020	2557	DW #20	SPACE
0A40	0F	0020	2558	DW #20	SUB
0A41	0F	0020	2559	DW #20	
0A42	EA	0015	2560	DW #15	NAK
0A43	ER	0014	2561	DW #14	DC4
0A44	0F	0020	2562	DW #20	CU3
0A45	0F	0020	2563	DW #20	
0A46	0F	0020	2564	DW #20	
0A47	0F	0020	2565	DW #20	
0A48	FR	0004	2566	DW #04	EOT

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 85)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
0A49	DF	0020	2567	DW	#20 UC
0A4A	E1	001E	2568	DW	#1E RS
0A4B	DF	0020	2569	DW	#20 PN
0A4C	DF	0020	2570	DW	#20
0A4D	F9	0016	2571	DW	#16 SYN
0A4E	DF	0020	2572	DW	#20
0A4F	DF	0020	2573	DW	#20
0A50	F8	0007	2574	DW	#07 BEL
0A51	F9	0006	2575	DW	#06 ACK
0A52	FA	0005	2576	DW	#05 ENQ
0A53	DF	0020	2577	DW	#20
0A54	DF	0020	2578	DW	#20 CUP
0A55	DF	0020	2579	DW	#20 SM
0A56	DF	0020	2580	DW	#20
0A57	DF	0020	2581	DW	#20
0A58	E4	0018	2582	DW	#18 ESC
0A59	E8	0017	2583	DW	#17 ETH
0A5A	F5	000A	2584	DW	#0A LF
0A5B	DF	0020	2585	DW	#20 BYP
0A5C	DF	0020	2586	DW	#20
0A5D	E3	001C	2587	DW	#1C FS
0A5E	DF	0020	2588	DW	#20 SOS
0A5F	DF	0020	2589	DW	#20 DS
0A60	E0	001F	2590	DW	#1F IUS
0A61	E1	001E	2591	DW	#1E IRS
0A62	E2	001D	2592	DW	#1D UGS
0A63	E3	001C	2593	DW	#1C IFS
0A64	DF	0020	2594	DW	#20 CUI
0A65	DF	0020	2595	DW	#20 CC
0A66	E6	0019	2596	DW	#19 EM
0A67	E7	0018	2597	DW	#18 CAN
0A68	DF	0020	2598	DW	#20 IL
0A69	F7	0008	2599	DW	#08 BS
0A6A	DF	0020	2600	DW	#20 NL
0A6B	DF	0020	2601	DW	#20 RES
0A6C	DF	0020	2602	DW	#20 TM
0A6D	ED	0012	2603	DW	#12 DC2
0A6E	EE	0011	2604	DW	#11 DC1

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 86)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS	
0A6F	EF	0010	2605	DW	#10 DLE
0A70	F0	000F	2606	DW	#0F SI
0A71	F1	000E	2607	DW	#0E SO
0A72	F2	000D	2608	DW	#0D CH
0A73	F3	000C	2609	DW	#0C FI
0A74	F4	000B	2610	DW	#0B VI
0A75	DF	0020	2611	DW	#20 SYN
0A76	DF	0020	2612	DW	#20
0A77	DF	0020	2613	DW	#20
0A78	80	007F	2614	DW	#7F DEL
0A79	DF	0020	2615	DW	#20 LC
0A7A	F6	0009	2616	DW	#09 HT
0A7B	DF	0020	2617	DW	#20 PF
0A7C	FC	0003	2618	DW	#03 ETX
0A7D	FD	0002	2619	DW	#02 STX
0A7E	FE	0001	2620	DW	#01 SOH
0A7F	FF	0000	2621	DW	#00 NUL

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 87)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
			2622	ORG
			2623	**** UPPER TABLE FOR TRANSLATION FROM ERCDIC TO ASCII
		0A80	2624	ETAU EQU *
0A80	0F	0020	2625	DW #20
0A81	0F	0020	2626	DW #20
0A82	0F	0020	2627	DW #20
0A83	0F	0020	2628	DW #20
0A84	0F	0020	2629	DW #20
0A85	0F	0020	2630	DW #20
0A86	C6	0039	2631	DW #39 9
0A87	C7	0038	2632	DW #38 8
0A88	C8	0037	2633	DW #37 7
0A89	C9	0036	2634	DW #36 6
0A8A	CA	0035	2635	DW #35 5
0A8B	CB	0034	2636	DW #34 4
0A8C	CC	0033	2637	DW #33 3
0A8D	CD	0032	2638	DW #32 2
0A8E	CE	0031	2639	DW #31 1
0A8F	CF	0030	2640	DW #30 0
0A90	0F	0020	2641	DW #20
0A91	0F	0020	2642	DW #20
0A92	0F	0020	2643	DW #20
0A93	0F	0020	2644	DW #20
0A94	0F	0020	2645	DW #20
0A95	0F	0020	2646	DW #20
0A96	A5	005A	2647	DW #5A Z
0A97	A6	0059	2648	DW #59 Y
0A98	A7	0058	2649	DW #58 X
0A99	A8	0057	2650	DW #57 W
0A9A	A9	0056	2651	DW #56 V
0A9B	AA	0055	2652	DW #55 U
0A9C	AB	0054	2653	DW #54 T
0A9D	AC	0053	2654	DW #53 S
0A9E	0F	0020	2655	DW #20
0A9F	0F	0020	2656	DW #20
0AA0	0F	0020	2657	DW #20
0AA1	0F	0020	2658	DW #20
0AA2	0F	0020	2659	DW #20

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 88)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
0AA3	0F	0020	2660	DW #20
0AA4	0F	0020	2661	DW #20
0AA5	0F	0020	2662	DW #20
0AA6	AD	0052	2663	DW #52 R
0AA7	AE	0051	2664	DW #51 Q
0AA8	AF	0050	2665	DW #50 P
0AA9	00	004F	2666	DW #4F O
0AAA	B1	004E	2667	DW #4E N
0AA9	B2	004D	2668	DW #4D M
0AAC	B3	004C	2669	DW #4C L
0AAD	B4	004B	2670	DW #4B K
0AAE	B5	004A	2671	DW #4A J
0AAF	0F	0020	2672	DW #20
0AB0	0F	0020	2673	DW #20
0AB1	0F	0020	2674	DW #20
0AB2	0F	0020	2675	DW #20
0AB3	0F	0020	2676	DW #20
0AB4	0F	0020	2677	DW #20
0AB5	0F	0020	2678	DW #20
0AB6	B6	0049	2679	DW #49 I
0AB7	B7	0048	2680	DW #48 H
0AB8	B8	0047	2681	DW #47 G
0AB9	B9	0046	2682	DW #46 F
0ABA	BA	0045	2683	DW #45 E
0AB9	BB	0044	2684	DW #44 D
0ABC	BC	0043	2685	DW #43 C
0ABD	BD	0042	2686	DW #42 B
0ABE	BE	0041	2687	DW #41 A
0ABF	0F	0020	2688	DW #20
0AC0	0F	0020	2689	DW #20
0AC1	0F	0020	2690	DW #20
0AC2	0F	0020	2691	DW #20
0AC3	0F	0020	2692	DW #20
0AC4	0F	0020	2693	DW #20
0AC5	0F	0020	2694	DW #20
0AC6	0F	0020	2695	DW #20
0AC7	0F	0020	2696	DW #20
0AC8	0F	0020	2697	DW #20

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 89)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
0AC9	0F	0020	2698	DW #20
0ACA	0F	0020	2699	DW #20
0ACH	0F	0020	2700	DW #20
0ACC	0F	0020	2701	DW #20
0ACD	0F	0020	2702	DW #20
0ACE	0F	0020	2703	DW #20
0ACF	0F	0020	2704	DW #20
0AD0	0F	0020	2705	DW #20
0AD1	0F	0020	2706	DW #20
0AD2	0F	0020	2707	DW #20
0AD3	0F	0020	2708	DW #20
0AD4	0F	0020	2709	DW #20
0AD5	0F	0020	2710	DW #20
0AD6	85	007A	2711	DW #7A Z
0AD7	86	0079	2712	DW #79 Y
0AD8	87	0078	2713	DW #78 X
0AD9	88	0077	2714	DW #77 W
0ADA	89	0076	2715	DW #76 V
0ADH	8A	0075	2716	DW #75 U
0ADC	8B	0074	2717	DW #74 T
0ADD	8C	0073	2718	DW #73 S
0ADE	0F	0020	2719	DW #20
0ADF	0F	0020	2720	DW #20
0AE0	0F	0020	2721	DW #20
0AE1	0F	0020	2722	DW #20
0AE2	0F	0020	2723	DW #20
0AE3	0F	0020	2724	DW #20
0AE4	0F	0020	2725	DW #20
0AE5	0F	0020	2726	DW #20
0AE6	8D	0072	2727	DW #72 R
0AE7	8E	0071	2728	DW #71 Q
0AE8	8F	0070	2729	DW #70 P
0AE9	90	006F	2730	DW #6F O
0AEA	91	006E	2731	DW #6E N
0AEB	92	006D	2732	DW #6D M
0AEC	93	006C	2733	DW #6C L
0AED	94	006B	2734	DW #6B K
0AEE	95	006A	2735	DW #6A J

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 90)

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
0AEF	0F	0020	2736	DW #20
0AF0	0F	0020	2737	DW #20
0AF1	0F	0020	2738	DW #20
0AF2	0F	0020	2739	DW #20
0AF3	0F	0020	2740	DW #20
0AF4	0F	0020	2741	DW #20
0AF5	0F	0020	2742	DW #20
0AF6	96	0069	2743	DW #69 I
0AF7	97	0068	2744	DW #68 H
0AF8	98	0067	2745	DW #67 G
0AF9	99	0066	2746	DW #66 F
0AFA	9A	0065	2747	DW #65 E
0AFB	9B	0064	2748	DW #64 D
0AFC	9C	0063	2749	DW #63 C
0AFD	9D	0062	2750	DW #62 B
0AFE	9E	0061	2751	DW #61 A
0AFF	0F	0020	2752	DW #20

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ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 91)

ROM	..CODE..	ARG	STMT	SOURCE STATEMENTS
ADDR	I1 I2 I3		NUMBER	

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ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 92)

ROM	..CODE..	ARG	STMT	SOURCE STATEMENTS
ADDR	I1 I2 I3		NUMBER	
			2755	ORG
			2756	**** WRITE FORMAT ON CURRENT TRACK
0800	CE 25	0800	2757	FMT EQU *
0802	FF	0000	2758	RL SU2 SET TO ENTERED TRACK AND LOWER HEAD
			2759	DW #00 NO PARAMETER USED
			2760	**** INITIALIZE FORMAT BLOCKS
0803	8A(0A)16	00E9	2761	LXI FCWD
0805	C9 40	04CD	2762	RL ICBP
0807	E7	0018	2763	DW #FW FORMAT WRITE -- NO INTERRUPT
0808	FF	0000	2764	DW #00 PRE INDEX MARK GAP CHARACTER
0809	2D	00D2	2765	DW #D2 PRE INDEX MARK GAP SIZE = 46
080A	FF	0000	2766	DW #00 ARBITRARY
080B	1A	00E5	2767	DW #E5 POST INDEX MARK GAP SIZE(FIRST HALF)
080C	03	00FC	2768	DW #FC INDEX MARK CHARACTER
080D	FF	0000	2769	DW #00 POST INDEX MARK GAP CHARACTER(FIRST HALF)
080E	E7	0018	2770	DW #FW FORMAT WRITE COMMAND FOR FORMAT BLOCK
080F	FF	0000	2771	DW #00 GCA
0810	05	00FA	2772	DW #FA GSA
0811	03	00FC	2773	DW #FC ID FIELD SIZE
0812	0A	00F5	2774	DW #F5 GSH
0813	01	00FE	2775	DW #FE ID MARK
0814	FF	0000	2776	DW #00 TRACK
0815	FF	0000	2777	DW #00
0816	FF	0001	2778	DW #01 SECTOR
0817	FF	0000	2779	DW #00
0818	00	00FF	2780	DW #FF GCB
0819	FF	0000	2781	DW #00 GCC
081A	05	00FA	2782	DW #FA GSC
081B	7F	0080	2783	DW #80 RECORD SIZE
081C	1A	00E5	2784	DW #E5 GSD
081D	04	00F8	2785	DW #F8 DATA MARK
			2787	**** SET UP DCF TO POINT TO PREFORMAT BLOCK AND DCR TO POINT TO
			2788	**** NORMAL FORMAT BLOCK
081E	AD(2D 70)	0000	2789	LAI #00
081F	4F 16	16	2790	OUT LARU,DCF
0821	4E 76	76	2791	OUT LARU,DCR
0823	4E 77	77	2792	OUT LRLR,DCR



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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 93 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
0B25	R6(06)0F	00F0	2794	LAI #F0
0B27	4E 75	75	2795	OUT LARL,DCF
0B29	21		2796	NOP
0B2A	8E	0B3E	2797	R FMT0
0B2B	86(06)16	00E9	2800	**** WAIT FOR LEADING EDGE OF INDEX AND START OPERATION
0B2D	4E 15	15	2801	LAI #C9 POINT TO START OF PREFORMAT BLOCK
0B2F	AD(2D 70)	0000	2802	OUT LARL,DCF
0B30	4E 17	17	2803	LAI #00
0B32	4E 4A	42	2804	OUT LRLR,DCF
0B34	25 02	0B32	2805	IN RBB,PDCF
0B36	4E 4A	42	2806	BN FMT5
0B38	24 86	0B36	2807	IN RBB,PDCF
0B3A	4E 51	51	2808	RP FMT6
0B3C	21		2809	OUT FST,FDC
0B3D	CR	0B4B	2810	NOP
			2811	R FMT7
			2814	**** SET PTRS AND START INDEX PORTION OF FORMAT WRITE
			2815	**** IF INDEX NOT DETECTED THEN RESTART
0B3E	86(06)16	00E9	2816	FMT0 LAI #E9 POINT TO START OF PREFORMAT BLOCK
0B40	4E 15	15	2817	OUT LARL,DCF
0B42	AD(2D 70)	0000	2818	LAI #00
0B43	4E 17	17	2819	OUT LRLR,DCF SET TO MAX SO NO PROBLEMS
			2820	**** START FDC IN INDEX PORTION OF FORMAT WRITE
0B45	4E 51	51	2821	OUT FST,FDC
			2822	**** SEE IF INDEX IS DETECTED
0B47	4E 4A	42	2823	IN RBB,PDCF
0B49	25 8E	0B3E	2824	BN FMT0 DETECTED SO TOO LATE
		0B4B	2825	FMT7 EQU *
0B4A	61		2826	NOP NO BUT WAIT A BIT
0B4C	61		2827	NOP
0B4D	61		2828	NOP
0B4E	61		2829	NOP
0B4F	61		2830	NOP
0B50	61		2831	NOP

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 94 )

ROM ADDR	..CODE.. 11 12 13	ARG	STMT NUMBER	SOURCE STATEMENTS
0H51	H7(37 60)	0001	2833	FMT1 LZI 1
0H52	8A(0A)07	00F8	2834	LXI SA ADDRESS SECTOR VALUE
0H54	8E(0E)E6	0019	2835	LYI 25 COUNTER TO DETERMINE END
0H56	4E 4A	42	2836	IN RBB,PDCF
0H58	24 8E	0B3E	2837	RP FMT0
0H5A	4E 51	51	2839	**** INDEX DETECTED SO SET UP PTRS AND COUNTERS FOR SECTORS
0H5C	FC(9C BC)	0537	2840	OUT FST,FDC START SECOND PORTION FO FORMAT WRITE(POST IND
0H5D	FE	0001	2841	BL VDEL DELAY PAST FIRST ID
0H5E	86(06)FE	0001	2842	DW #01
			2843	LAI #01 SECTOR VALUE BEING OUTPUT
0B60	42		2845	**** LAST ID READ OUT SO UPDATE SECTOR IN FORMAT BLOCK
0B61	75		2846	FMT4 INCA INCR SECTOR
0B62	60 10		2847	S STORE INTO SA
0B64	F8	0B7B	2848	DECY DECR SECTOR COUNTER
			2849	H FMT2 NOT DONE YET
0B65	AD(2D 70)	0000	2851	**** LAST SECTOR SO SET GAP SIZE D TO MAX
0B66	8A(0A)01	00FE	2852	LAI #00
0B68	75		2853	LXI GSD
			2854	S
0B69	4E 4A	42	2856	**** WAIT FOR THE INDEX
0B6B	24 E9	0B69	2857	FMT3 IN RBB,PDCF
			2858	RP FMT3
0B6D	86(06)EF	0010	2860	**** TRACK FORMATTED SO IDLE FDC
0B6F	4E 51	51	2861	LAI #1
0B71	4E 52	52	2862	OUT FST,FDC
0B73	CE 36	0736	2863	OUT FLD,FDC
0B75	21		2864	BL CU2 UNLOAD HEAD
0B76	5F 8C	065F	2865	NOP
			2866	B EX1
0B78	FC(9C BC)	0537	2869	**** NOT END OF TRACK SO DELAY TO MIDDLE OF NEXT SECTOR
			2870	FMT2 BL VDEL

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 95)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
0879	FD	0002	2871	DW #02
087A	21		2872	NOP
087B	E0	0960	2873	B FMT4

```

2879 .....
2880 *
2881 *           SECTION 4
2882 *
2883 *           POST ASSEMBLY INFORMATION
2884 *
2885 *
2886 * THE BATCH CROSS ASSEMBLER PROVIDES THE
2887 * INFORMATION IN THIS SECTION. CONTROL
2888 * CARDS MAY BE USED TO REQUEST ADDITIONAL
2889 * INFORMATION. THE INFORMATION IN THIS
2890 * LISTING IS
2891 *
2892 * 1) POOL ROM MAP
2893 * 2) SYMBOL CROSS REFERENCE TABLE
2894 * 3) DIAGNOSTIC MESSAGES
2895 * 4) ROM UTILIZATION
2896 *
2897 *
2898 *
2899 *
2900 *
2901 *
2902 *
2903 *
2904 *           ROCKWELL INTERNATIONAL
2905 *           MICROELECTRONIC DEVICE DIVISION
2906 *           AUGUST 19, 1976

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 96)

ROM ADDR	..CODE.. I1 I2 I3	ARG	STMT NUMBER	SOURCE STATEMENTS
2907				*
2908				.....

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## ROCKWELL CRT/FDC DEMONSTRATOR L6611 - FDC ROUTINES

( 97)

ROM	..CODE..	ARG	STMT	SOURCE STATEMENTS
ADDR	11 12 13		NUMHER	
			2910	END

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## ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 &amp; A52H1)

( 98)

	POOL POM MAP															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	21	40	81	58	97	96	FF	7F	95	94	CF	4F	93	92	DF	5F
0010	91	90	EF	6F	9F	9E	83	83	9D	9C	03	80	9B	9A	80	81
0020	99	98	00	82	8F	AF	A1	2F	87	84	01	85	86	F0	82	F1
0030	C0	C1	02	C2	C3	C4	C5	CU	B2	A1	A2	A3	00	00	00	00
0040	7F	D6	DE	DF	D5	CF	00	00	00	00	00	00	00	00	00	00
0050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0060	FE	FE	7F	00	00	00	00	00	00	00	00	00	00	00	00	00
0070	FF	00	DF	00	00	00	00	00	00	00	00	00	00	00	00	00
0080	80	D0	80	80	9F	AE	89	80	8C	8A	AA	92	9E	A6	84	C0
0090	C7	UC	DF	A3	82	87	96	8E	EE	AE	DC	84	87	F1	A5	92
00A0	A0	82	A9	86	86	86	A6	87	87	86	86	87	87	87	87	87
00B0	87	87	A7	80	87	A5	86	86	83	88	8F	88	8A	85	63	89

7/12 SYMBOL	DEFINED	ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)	REFERENCED	( 99)
.CL	785	1929	1923 149	
.A.	234	1564		
.C.	235	1915	1811 1565	
.CDN	711	671		
.CL	783	1003		
.CLF	691	568		
.CLR	779	564	431	
.CR	718	667	666	
.CR.	232			
.CRT	680	669	556	
.CUP	705	670		
.D.	236	1566		
.DEL	845	672		
.DLC	858	674		
.E.	237			
.F.	238	1567		
.G.	239	1805		
.H.	240	1568		
.I.	241	1569		
.INC	756	675		
.INL	798	673		
.INZ	910	151		
.INI	913	911		
.J.	242	1570		
.K.	243	1571		
.L	1482	2133	1713	
.L.	244	1572		
.LF.	231			
.M.	245	1573		
.N.	246	1822	1574	
.O.	247	1824	1807	
.P.	248			
.Q.	249	1575		
.R.	250	1813	1576	
.RST	759	665		
.S.	251	1577		
.T.	252	1578		
.V.	253	1579		

7/12 SYMBOL	DEFINED	POCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)	REFERENCED	(100)
.W.	254	1580		
.X.	255	1581		
%CRC	195	1798		
%FW	193	2770	2763	
%I	189	2461		
%RC	192	1749		
%RID	174	1631		
%RS	190	2231	1959 1437	
%WS	191	2256	2018 1698	
AMC	313			
ASCI	1670	1586		
ATE	2362	2043		
BACK	445	1951	1942 1938 1842 1789 1688 916 886 762 758 621 489 481 477	
		474 470 452		
BAKG	448	628		
BAL	329	2016	1957 1796 1747 1696 1629 1485	
BAUR	330	1958	1797 1630 1486	
BAUW	331	2017	1748 1697	
BCNT	275	454		
BDLY	256	459		
BIN	2194	2184		
HLC	1072	1921	1898 994 805 718 711 705 697 680 564 559 483 142	
HLC.	1073	1068		
HLKL	1119	900	750 146	
HLKS	1094	781	144	
HLK1	1114	1121	830 145	
HLL	1873	1817	1652	
HLL1	1879	1807		
HLL2	1884	1882		
HLNK	233	1880	1826 1809 1098 867 767	
HL1	1095	1115		
HL11	1097	1107		
HL12	1100	1104		
HL13	1103	1101		
HTAL	571	1611	552 158	
ETU1	576	578		
UTB2	592	577		
HUFR	328	2315	2314 2156 2155 2028 2027 1977 1976 422 421	

7/12 SYMBOL	DEFINED	ROCKWELL CRT/FDC REFERENCED	DEMONSTRATOR (A6611 AND A52H0 & A52H1)												(101)
B0	476	466													
B1	483	479													
B2	490	472													
B3	465	458													
CLIN	1033	771	685	139											
CLII	1040	1036													
CLKI	200	399													
CLKO	199														
CLST	1055	858	845	798	719	141									
CLS1	1061	1057													
CL1	697	695													
CNUM	1944	1940													
CRR1	723	720													
CRT	681														
CR1	685	692													
CR2	687	684													
CTN	1852	1567													
CTN1	1862	1867													
CTN2	1855														
CTN3	1859	1854													
CTRK	284	1417	1227												
CURS	279	1066	1073	871	694	118									
CU1	1905	1618	1738	1726	1663	1653	1637								
CU2	1927	2864	2246	1706	1501										
CWD	308	1224													
DATA	336	1056	898	791	790	780	779	341	340	339	338	337			
DAUR	348	2230													
DBL	287	1946													
DBU	288	2073													
DCC	179	526	521	518											
DCU	178	2282	2279	2272	1251	1249	1247								
DCF	177	2819	2817	2804	2802	2790	1258	1256	1253						
DCK	180	2795	2792	2791	1259	1257	1254								
DDMK	1837	1593													
DD1	922	926	923												
DECL	1024	1635	707	696	136										
DECZ	931	970	700	132											
DEL3	1375	1460													

7/12 SYMBOL	DEFINED	ROCKWELL CRT/FDC REFERENCED	DEMONSTRATOR (A6611 AND A52H0 & A52H1)												(102)
DEZS	943	878	866	138											
DE1	849	846													
DE11	938	936													
DE80	963	1900	1027	850	829	752	706	692	134						
DE81	972	967													
DISP	632	626													
DLY	921	913	150												
DL0	853	859													
DL1	867	865	862												
DL2	879	877													
DL2L	344														
DL2U	345														
DL3	875	872													
DL31	1377	1378													
DL4	868	880													
DMAL	346	2254	2229	517											
DMAU	347	2255	520												
DMK	1839	1834													
DPC	1084	1930	1908	884	143										
DST	2153	1755	1316												
DSTX	2192	2188													
DST1	2177	2178													
DST2	2183	2175	2170												
DST3	2184	2191													
DS2	1505	1495													
DS3	1489														
DS4	1484	1509	1490												
OTOP	341	938	861	860	807	806									
D1	165	531	505	397											
D2	166	981	546	543	539	494	478	471	448	445	400	398			
ENBL	389	1001	428	147											
ERRC	292	1318	1310												
ERRS	293														
ETAL	2493	1993													
ETAU	2624	1991													
EXIP	883	831	793	753	725	714	708	702	688	157					
EXIT	884	874	803	699	686										
EX1	1786	2866	2215	1819	1782	1777	1768	1765	1739	1727	1715	1707	1680	1673	1664

7/12 SYMBOL	DEFINED	ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)	REFERENCED	(103)
FCL	185	1654	1643	
FC#0	298	1781	1762	
FDC	168	2761		
FDCX	1564	2863	2862 2840 2821 2809 1281 1279 1263 1262	
FIS	290	1612		
FLAG	264	2173	1276	
		2274	2260 2222 2134 2131 2070 2040 1986 1949 1786 1685 1678 1671 1420	
		1362	1299 1283 1260 996 922 759 756 557 523 451 119	
FLD	184	2863		
FLPI	1611	1607		
FLPY	1607	545		
FMT	2757	1589		
FMT0	2816	2837	2824 2797	
FMT1	2833			
FMT2	2870	2849		
FMT3	2857	2858		
FMT4	2846	2873		
FMT5	2805	2806		
FMT6	2807	2808		
FMT7	2825	2811		
FNS	291	2168	1802 1753 1303	
FRS	186	1279		
FST	183	2862	2840 2821 2809 1263	
FST1	1386	1388		
FST2	1383	1385		
FST3	1392	1393		
GCA	309	1353		
GCB	318			
GCC	319			
GSA	310			
GSB	312			
GSC	320			
GSD	322	2853		
HDR	1621	1590		
HDR1	1628	1633		
MLD	1425	1920	1897	
HOUT	201			
ICB	1353	1333		

7/12 SYMBOL	DEFINED	ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)	REFERENCED	(104)
ICBP	1354	2762		
ICB1	1355	1357		
IDLY	256	550		
IFFR	1333	1416		
IMC	303			
IN.	800	848	749	
IN11	510	507		
IN12	514	509		
INCL	1009	1907	1662 1649 724 713 687 135	
INCS	2116	1766		
INC7	692	955	910 739 683 131	
INL.	1013	1029		
INSC	767	560		
INS0	769	172		
INS1	771	769		
INT0	161	128		
INT1	502	129		
INT2	1274	130		
INZ.	905	946		
INZ5	903	2335	2331 2327 2321 1883 1102 770 137	
INO	815	841	836 822	
IN1	805	799		
IN2	821	816		
IN21	1285			
IN3	832	827		
IN80	950	1012	712 133	
IN81	958	952		
IRPT	273	549	465	
ISTK	434	995	435 395	
I1	527	515		
I2	533	984		
KBOT	343	935		
KEY	263	633	612 575 562 540 120	
KEYS	649	553		
KTAH	663	554		
KTOP	342	895		
K80	277	525	416	
LARL	205	2617	2802 2795 2272 1254 1253 1249 518	



7/12 SYMBOL	DEFINED	ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)	REFERENCED	(107)
RD	1720	1598		
RDLY	257	491		
RDY7	1440	1450	1217 1170	
READ	1956	1961	1722 1648	
RHR	208			
RHXA	2348	2323		
RIBM	1646	1591		
RIB1	1649	1757		
RID	2311	1634		
RID1	2316	2338		
RID2	2336	2334		
RID3	2322	2320		
RID4	2328	2326		
RID5	2332	2330		
RPT	274	490	485 476	
RQST	224			
RQSK	228			
RQ53	227	599		
RRB	220	632		
RSA	311	1640	1623	
RSB	321	2250	2243 2224	
RSET	198			
RSR	215	448		
RS12	221	625	615 607	
RTNA	1585	1613		
RTRY	259	1314		
SA	316	2834	1476	
SCOL	729	722		
SCPD	281	2293	2277	
SCTR	286	2265	2116 2102 1916 1893 1764 1473	
SC0.	736	854	747 743	
SC1	742	737		
SC2	749	740		
SDC	169	641	632 625 615 614 607 599 406	
SET	1214	2253	2223 2015 1956 1795 1745 1695 1628 1484 153	
SETC	1469	2283		
SET1	1241	1238		
SET2	1242	1240		

7/12 SYMBOL	DEFINED	ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)	REFERENCED	(108)
SET3	1246	1245		
SET4	1252	1478		
SIOL1	222			
SIOL2	223			
SIN	202			
SIO	204	403		
SKT0	1398	1364	429	
SMC	323	1839		
SNE	2069	1912	1892 1852 1775 1763 154	
SNE1	2089	2071		
SOUT	203	401		
SSC	1762	1599		
STC	289	1170	1172 1166	
STEP	1170	1919	1896 1195 155	
STE1	1198	1174		
STPI	1166	1410	1403	
STR	1774	1400		
SU1	1892	1794	1745 1734 1721 1658 1647	
SU2	1912	2758	2219 1689 1626 1482	
TA	314	1229		
TD	1365	1363		
TDIF	1362	1918	1895	
TEMP	242	1664	1861 583	
THEY	599	548	496	
TRK	285	2137	1913 1866 1859 1778 1776 1365 1198 122	
T20	283	2141	1977 1856 1853	
UNLD	1434	1927	1905	
VDEL	1457	2070	2841 2148 1429 1389 1201 1192 156	
VDE1	1460	1462		
VDE2	1461	1459		
WBUF	2026	1735	1643 1659	
WBU1	2032	2054		
WBU2	2038	2034		
WBU3	2052	2048		
WBU4	2058	2041		
WBU5	2047	2059		
WFD0	1295	2233	2019 1960 1799 1750 1699 1632 1489 159	
WFD1	1302			



7/12 SYMBOL	DEFINED	ROCKWELL REFERENCED	CRT/FDC	DEMONSTRATOR (A6611 AND A52H0 & A52H1)
WFD2	1300	1301		
WFD6	1326	1315		
WFD7	1318	1308		
WFD8	1310	1307	1305	1304
WIBM	1657	1592		
WRIT	2015	2020	1737	1661
WRT	1733	1602		
WS	1685	1588		
WS1	1689	1686		
WS2	1692	1705		
WS3	1695	1700		
WT	1515	2136		
WTE	1525	1527		
WT1	1517	1523		
WT2	1519	1529		
WT3	1527	1520		
XBCK	615	617		
XFST	1677	1603		

(109)

7/12  
NO DIAGNOSTICS

ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)

(110)

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ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)

(111)

UNUSED ROM

PAGE ADDRESS	0000	0080	0100	0180	0200	0280	0300	0380	
UNUSED LOCATIONS	54	4	3	14	3	10	30	28	147

PAGE ADDRESS	0400	0480	0500	0580	0600	0680	0700	0780	
UNUSED LOCATIONS	7	8	3	4	27	47	44	13	153

PAGE ADDRESS	0800	0880	0900	0980	0A00	0A80	0B00	0B80	
UNUSED LOCATIONS	2	35	76	0	0	0	4	128	245

TOTAL UNUSED = 553

15993 WORDS OF UNUSED SPACE

FILE TITLE: ROCKWELL CRT/FDC DEMONSTRATOR (A6611 AND A52H0 & A52H1)  
ROMTOP : 087F  
ERRORS : 0  
TYPE : 3  
START : 0000  
END : 0B7F