NXP Semiconductors
Reference Manual

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QorIQ LS1028A Reference Design Board Reference Manual

Contents

Chapter 1
LS1028ARDB Overview

The QorIQ® LS1028A reference design board (LS1028ARDB) is a computing, evaluation, development, and test platform supporting the QorIQ LS1028A processor, which is a dual-core Arm® Cortex®-v8 A72 processor with frequency up to 1.3 GHz. The LS1028ARDB is optimized to support SGMII (1 Gbit/s), QSGMII (5 Gbit/s), PCIe x1 (8 Gbit/s), and SATA (6 Gbit/s) over high-speed SerDes ports, USB 3.0, DisplayPort, and also a high-bandwidth DDR4 memory.

The LS1028ARDB can be used to develop and demonstrate human machine interface systems, industrial control systems such as robotics controllers and motion controllers, and PLCs. The reference design also provides the functionality needed for Industrial IoT gateways, edge computing, industrial PCs, and wireless or wired networking gateways.

The board is lead-free and RoHS-compliant.

NOTE

The LS1043A processor is used in the LS1028ARDB for early evaluation of board. Throughout this document, description of LS1028ARDB features also applies to the board with the LS1043A interposer, unless otherwise noted.

Developers using the LS1028ARDB can perform standard debugging tasks, such as:

- Upload and run code
- Set breakpoints
- Display memory and registers
- Connect and incorporate proprietary hardware into target systems using the LS1028A as a host processor
- Use the LS1028ARDB as a demonstration tool

The board support package (BSP) is developed using the Linux operating system. The onboard CPLD provides startup configuration information for the U-Boot and Linux.

1.1 Acronyms and abbreviations

The table below lists and explains the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Term	Description
CAN	Controller area network
CCI	Cache coherency interconnect
CPLD	Complex programmable logic device
CTS	Clear to send
DCM	Development system control monitor
DDR SDRAM	Double data rate synchronous dynamic random-access memory
DIP	Dual inline package
DPAA	Data path acceleration architecture
DQS	Data strobe

Table continues on the next page...

Table 1. Acronyms and abbreviations (continued)

Term	Description
DUART	Dual universal asynchronous receiver/transmitter
DUT	Device under test
EC	Ethernet controller
ECC	Error correcting code
eDP	Embedded DisplayPort
EMI	Ethernet management interface
ENETC	Ethernet controller
eMMC	Embedded multimedia card
eSDHC	Enhanced secure digital host controller
FET	Field-effect transistor
FPGA	Field-programmable gate array
GbE	Gigabit Ethernet
GPIO	General purpose input/output
GT/s	GigaTransfers/second
HDLC	High-level data link control
HSSI	High-speed serial interface
I2C	Inter-integrated circuit
JTAG	Joint Test Action Group (IEEE® Standard 1149.1™)
LOS	Loss of signal
OCM	Offline configuration manager
OTG	On-The-Go
PBL	Pre-boot loader
PLL	Phase-locked loop
PMIC	Power management multi-channel IC
POR	Power-on reset
PSU	Power supply unit
PTP	Precision time protocol
PWM	Pulse width modulation
QSGMII	Quad serial gigabit media independent interface
QSPI	Quad serial peripheral interface
RCW	Reset configuration word
RTC	Real time clock

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Table 1. Acronyms and abbreviations (continued)

Term	Description
RTS	Request to send
SATA	Serial advanced technology attachment
SDRAM	Synchronous dynamic random-access memory
SerDes	Serializer/deserializer
SGMII	Serial gigabit media independent interface
SPD	Serial presence detect
SPI	Serial peripheral interface
SS	Spread spectrum
SSC	Spread spectrum clocking
TCXO	Temperature compensated crystal (Xtal) oscillator
UART	Universal asynchronous receiver/transmitter
UDIMM	Unbuffered dual inline memory module
UFT	Universal frequency translator
USB	Universal serial bus
XSPI	Octal serial peripheral interface

1.2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on the LS1028ARDB.

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 2. Related documentation

Document	Description	Link/how to access
QorIQ LS1028A Product Brief	Provides a brief overview of the LS1028A processor	Contact FAE / sales representative
QorIQ LS1028A Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	Contact FAE / sales representative
QorIQ LS1028A Reference Manual	Provides a detailed description about the LS1028A QorIQ multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information	Contact FAE / sales representative
QorIQ LS1028A Chip Errata	Lists the details of all known silicon errata for the LS1028A	Contact FAE / sales representative

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Table 2. Related documentation (continued)

Document	Description	Link/how to access
QorIQ LS1028A Reference Design Board Getting Started Guide	Explains the LS1028ARDB settings and physical connections needed to boot the board	Contact FAE / sales representative
QorIQ LS1028A Design Checklist, AN12028	This document provides recommendations for new designs based on the LS1028A SoC. This document can also be used to debug newly designed systems by highlighting those aspects of a design that merit special attention during initial system start-up	Contact FAE / sales representative
Layerscape LS1028A BSP	This document explains how to use the QorIQ LS1028A BSP, which is a Linux-based development kit, to evaluate and explore the features of the LS1028A SoC	Contact FAE / sales representative
CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual	This manual explains how to use the CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA product	CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual
CodeWarrior TAP Probe User Guide	Provides details of CodeWarrior® TAP, which enables target system debugging through a standard debug port (usually JTAG) while connected to a developer workstation through Ethernet or USB	CodeWarrior TAP Probe User Guide

1.3 Block diagrams

This section provides block diagrams showing major functional units of the LS1028A processor and LS1028ARDB.

The figure below shows the LS1028A processor block diagram.

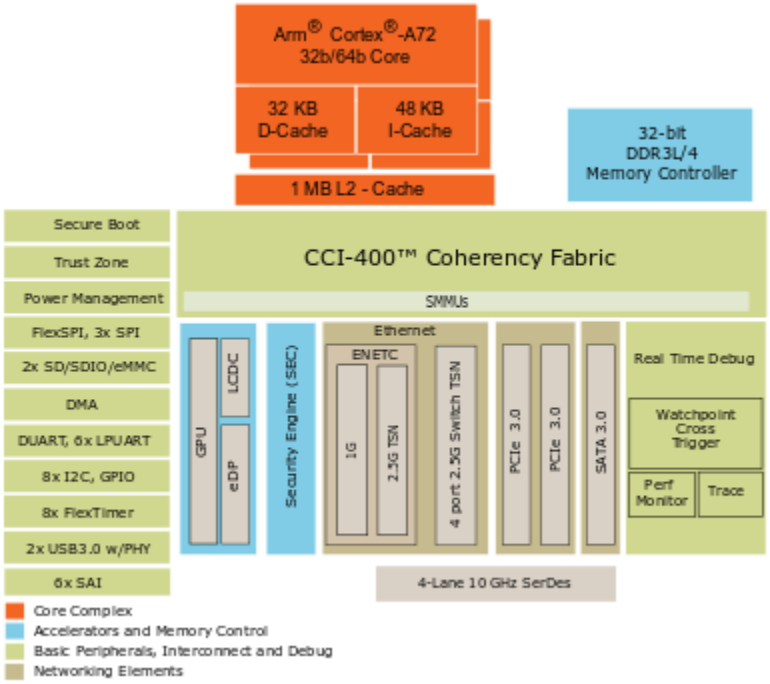

Figure 1. LS1028A block diagram

The figure below shows the LS1028ARDB block diagram.

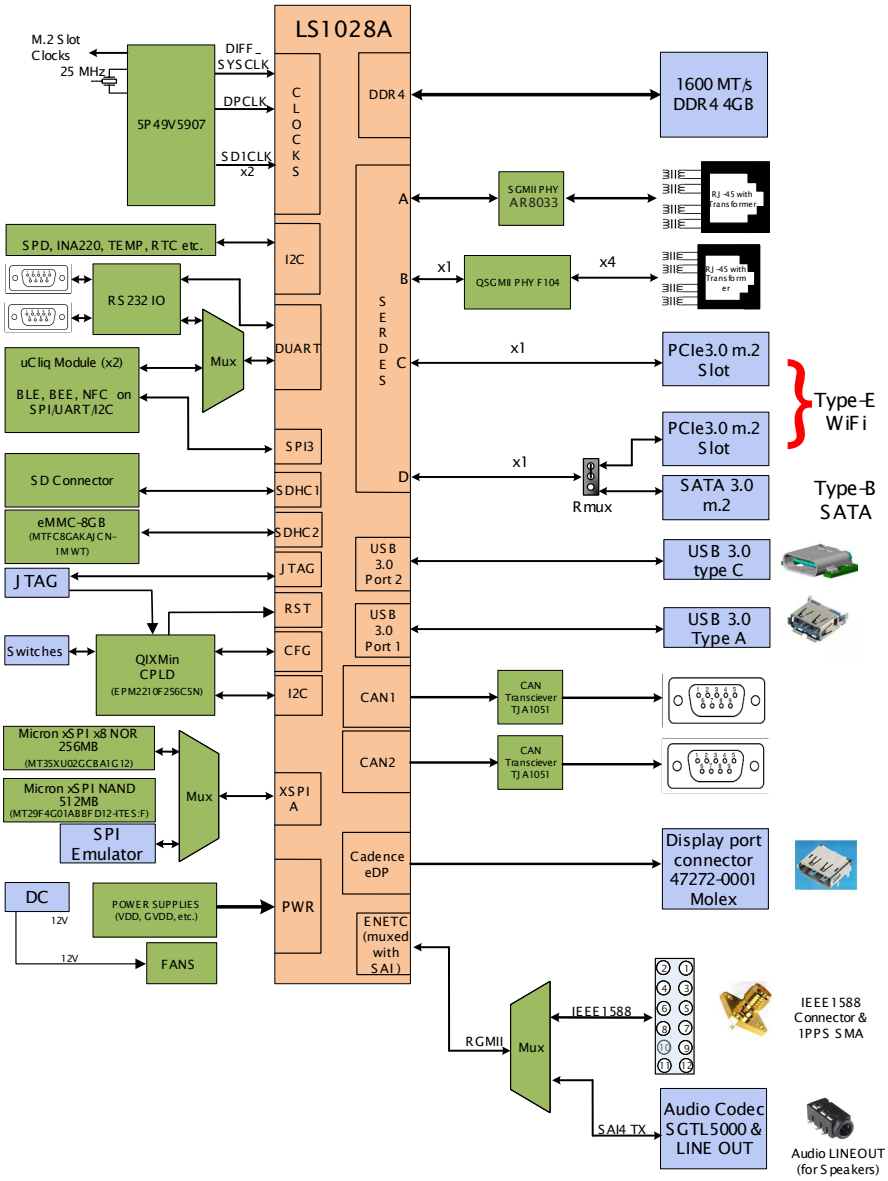

Figure 2. LS1028ARDB block diagram

1.4 Board features

The table below lists the features of the LS1028ARDB.

Table 3. LS1028ARDB features

LS1028ARDB feature	Specification	Description
Processor	Two-core processor	Two Arm® Cortex®- A72 processor cores: • Based on 64-bit ARMv8 architecture • Up to 1.3 GHz operation • Single-threaded cores with 48 KB L1 instruction cache and 32 KB L1 data cache • Arranged as a single cluster of two cores sharing a single 1 MB L2 cache **NOTE** For more details on the LS1028A processor, see *QorIQ LS1028A Family Reference Manual*.
DDR memory	DDR4	• Five onboard 1G x8 discrete memory modules (Four data byte lanes + ECC) • 32-bit data and 4-bit ECC • One chip select • Data transfer rates of up to 1.6 GT/s • Single-bit error correction and double-bit error detection ECC (4-bit check word across 32-bit data)
High-speed serial ports (SerDes)	One four-lane SerDes	• Lane 0: Supports one 1 GbE RJ45 SGMII, connected through the Qualcomm AR8033 PHY • Lane 1: Supports four 1.25 GbE RJ45 QSGMII, each connected through the NXP F104S8A PHY • Lane 2: Connects to one PCIe M.2 Key-E slot to support PCIe Gen3 (8 Gbit/s) cards • Lane 3: Connects to one PCIe M.2 Key-E slot or one SATA M.2 Key-B slot through a register mux to support either PCIe Gen 3 (8 Gbit/s) or SATA Gen 3 cards (6 Gbit/s) at a time
eSDHC	eSDHC1	Supports a secure digital (SD) connector for connecting an external SD 3.0 card
	eSDHC2	• Onboard 8 GB eMMC memory (MTFC8GAKAJCN) supporting — x1, x4, and x8 I/Os — SDR/DDR modes up to 52 MHz clock speed — HS200/HS400 modes
SPI	SPI3	Connects to two mikroBUS™ sockets to support mikro-click modules, such as Bluetooth 4.0, 2.4 GHz IEEE 802.15.4 radio transceiver, near field communications (NFC) controller

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Table 3. LS1028ARDB features (continued)

LS1028ARDB feature	Specification	Description
Octal SPI (XSPI)	One XSPI (XSPI A)	• One 256 MB onboard XSPI serial NOR flash memory • One 512 MB onboard XSPI serial NAND flash memory • Supports a QSPI emulator for offboard QSPI emulation
I2C	Six I2C interfaces	• All system devices are accessed via I2C1, which is multiplexed on I2C multiplexer PCA9848 to isolate address conflicts and reduce capacitive load • I2C1 is used for EEPROMs, RTC, INA220 current-power sensor, thermal monitor, PCIe/SATA M.2 connectors and mikro-click modules 1 and 2
Serial ports	Two UART ports (UART1 and UART2)	• UART1 supports RS-232 levels of up to 1 Mbit/s data rate on a DB9 male connector. LTC8204 RS232 transceiver is used for interface conversion. Hardware handshaking is not supported. • UART2 can be used to interface with either mikro-click modules or RS-232 transceiver LTC2804 (similar to UART1). The selection can be controlled from FPGA.
CAN	Two CAN ports (CAN1 and CAN2)	The two CAN DB9 ports can support CAN FD fast phase at data rates of up to 5 Mbit/s.
Ethernet	SGMII (1 GB Ethernet port) QSGMII (four 1 GB Ethernet ports) IEEE 1588™	• Five 1G/100M/10BaseT Ethernet ports supported. One port is supported on SGMII ENET MAC and the other four through the TSN switch. • Five RJ45 connectors with link and activity status are used with the SGMII and QSGMII interfaces • IEEE 1588 precision time protocol (PTP) is supported through an onboard header (J11) and SMA connector (J12) on the PULSE_OUT1 signal for 1PPS timing signal generation
USB 3.0	Two high-speed USB 3.0 ports with integrated PHYs	• Supports super-speed (5 Gbit/s) operations • USB 3.0 port 1 is configured as host with a Type A connector • USB 3.0 port 2 is configured as downstream facing port (DFP) or upstream facing port (UFP) with a Type C connector
Serial audio interface (SAI)	Audio transceiver (used only on TX signals) (not supported by the LS1043A processor)	• Audio codec SGTL5000 provides headphone and audio LINEOUT for stereo speakers • IEEE1588 interface to support audio on SAI4
Display	DisplayPort (not supported by the LS1043A processor)	• Supports display resolution of up to 4Kp60 • Supports link transfer rates of up to HBR2 (5.4 Gbit/s)
Clocks	Differential system clock (DIFF_SYSCLK)	100 MHz

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Table 3. LS1028ARDB features (continued)

LS1028ARDB feature	Specification	Description
	SerDes clocks	REF_CLK1 and REF_CLK2 of 100 MHz
	Ethernet clocks	125 MHz clock to Ethernet controller either from the IEEE 1588 port or an onboard oscillator
	Display Port clock (DP_REFCLK)	27 MHz
	FPGA CLK	25 MHz clock to CPLD
Power supplies		• 12 V input power from DC input adaptor • 5.0 V for USB1, USB2, CAN1, CAN2, and mikro-click modules • 1.0 V (VDD) for core and platforms • Filtered 1.0 V / 0.9 V USB_SDVDD, USB_SVDD, DP_SVDD, SVDD • 3.3 V for board components (SGMII PHY, M.2 connectors, SD card, eMMC, CAN transceivers, mikroBUS connectors, LEDs, DP port, CPLD IO and VDD, clockgen VDDO) • Filtered 3.3 V for USB_HVDD • 1.8 V for board components (UART transceivers, XSPI memories, eMMC memory IO VDD, CPLD IO bank3) • 1.8 V clockgen VDD and VDDA • 1.8 V OVDD, TH_VDD • Filtered 1.35 V X1VDD, AVDD_SD1_PLL1, AVDD_SD1_PLL2 • 2.5 V QSGMII PHY VDD25, VDD25A, and DDR4 memory VPP • 1.0 V QSGMII PHY VDD, VDDA • 1.2 V DRAM VDD • 0.6 V DRAM VTT, VREF • 3.3 V / 1.8 V EVDD for eSDHC • 0.9 V / 1.0 V TA_BB_VDD
Debug interface		• Arm Cortex 10-pin JTAG connector • CPLD programming header
Package		• Package type is Flip Chip, Plastic-ball, Grid Array (FC-PBGA), 17 mm x 17 mm • Socket and heat sink are included

Table continues on the next page...

Table 3. LS1028ARDB features (continued)

LS1028ARDB feature	Specification	Description
System logic	CPLD	• Manages the following: — System reset sequencing — SoC POR configuration at reset • Implements registers for system control and monitoring • General fault monitoring and logging

Chapter 2
LS1028ARDB Functional Description

This chapter explains all major functional components of the LS1028ARDB. The chapter is divided into the following sections:

2.1 Processor

The LS1028ARDB board is based on the QorIQ LS1028A processor having two Arm® Cortex®- A72 processor cores. The LS1028ARDB board supports as many features of the LS1028A as possible. In addition, the LS1028ARDB board supports an LS1043A interposer that allows early evaluation of the board with limited features and restrictions.

As a restriction, the following interfaces cannot be tested using the LS1043A interposer:

- DisplayPort
- SDHC2
- Octal SPI (XSPI)
- CAN
- SPI3

2.2 Power supplies

The LS1028ARDB generates all the voltages necessary for the correct operation of the LS1028A processor, DDR4, PHYs, and numerous other peripherals. All power is derived from an external 12 V DC power supply.

The following figures show the block diagram of LS1028ARDB power supplies:

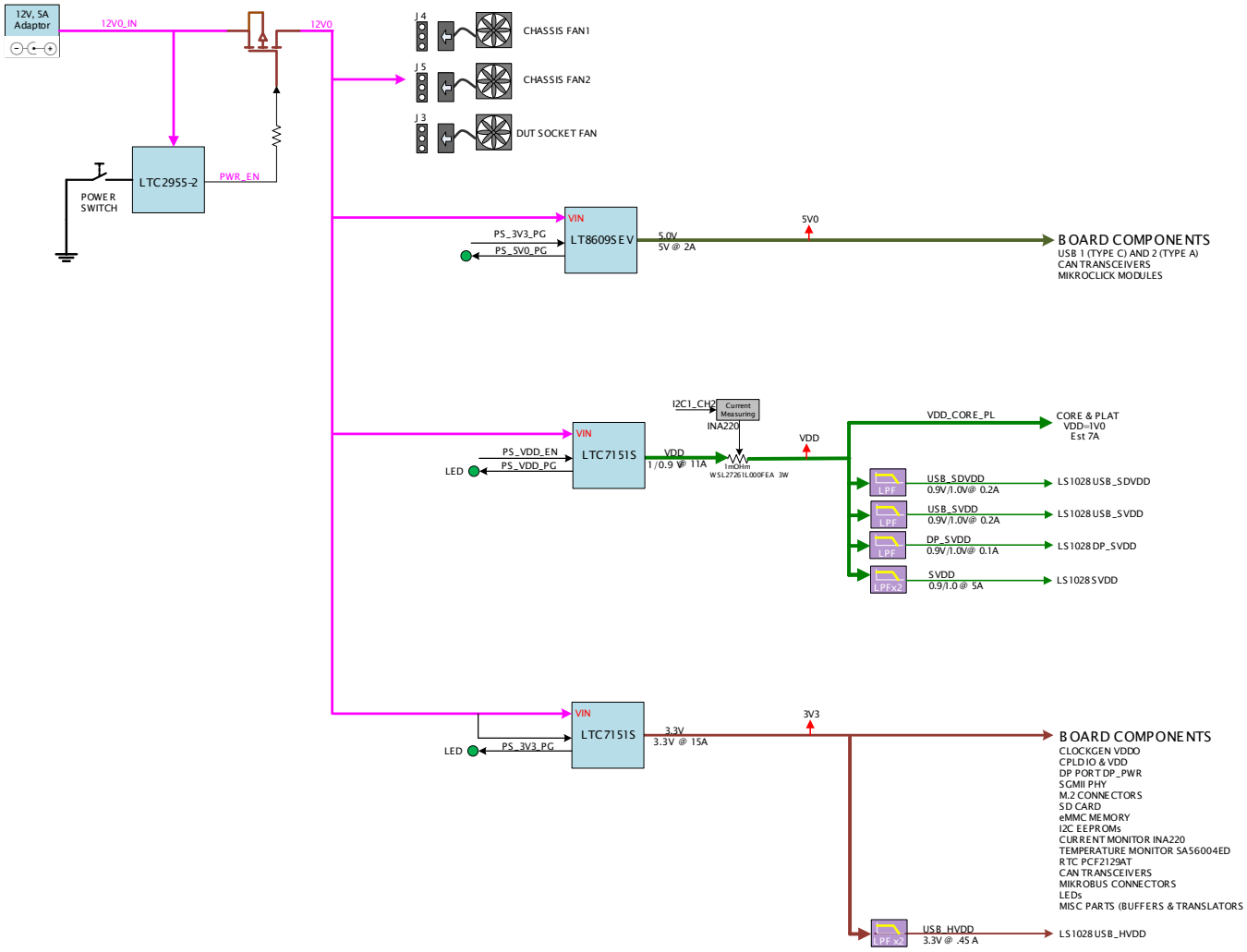


Figure 3. Power supplies - Part 1

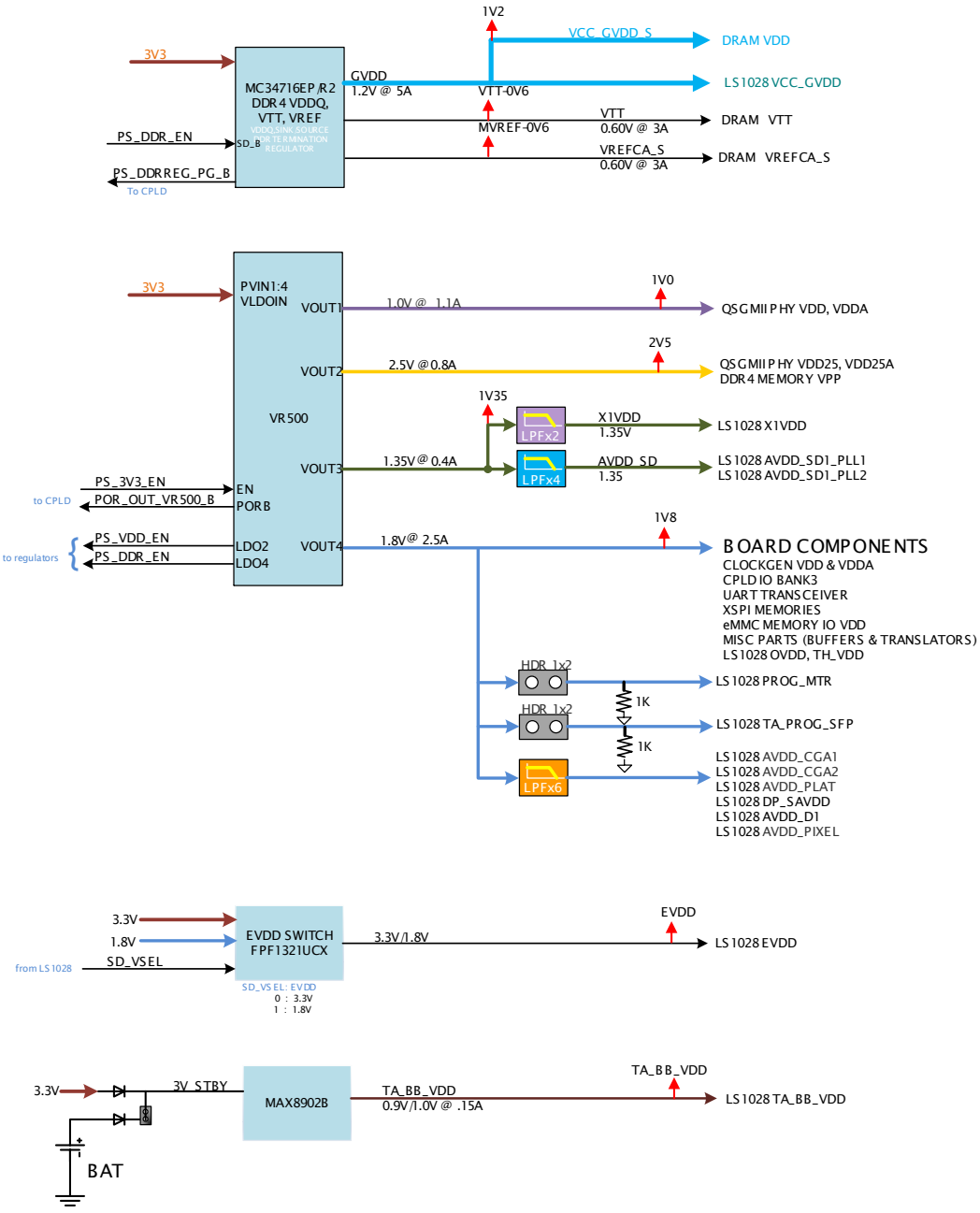


Figure 4. Power supplies - Part 2

Note that several power supplies have onboard low-pass filters, to prevent board switching noise from coupling into sensitive analog supplies. The figure below shows the filters used.

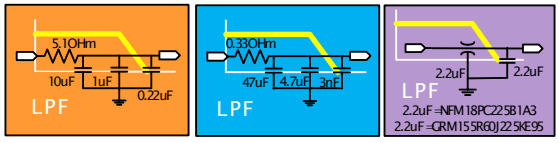


Figure 5. Passive low pass filters

2.2.1 Primary power supply

The LS1028ARDB is powered up through an external 12 V DC power adapter. The specifications of the DC adapter are as follows:

- Input: 100 - 240 VAC, 50 - 60 Hz
- Output: 12 V, 0 - 5 A DC power supply adapter (160 W) - Standard
- DC Jack (2 pin, 2.5 mm x 5.5 mm x 11 mm)

2.2.2 Secondary power supplies

The following table lists different power supply components used to generate various LS1028ARDB power supplies.

Table 4. Secondary power supplies

Part identifier	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
U1	LT8609SEV	Linear Technology	5V0	5 V at 2 A	Supplies power to the board components: • USB 1 and USB 2 connectors • CAN transceivers • Mikro-click modules
U2	LTC7151S	Linear Technology	VDD	1.0 V / 0.9 V at 20 A[1]	Supplies power to the LS1028A core supplies. **NOTE** Filtered VDD also powers USB (USB_SDVDD, USB_SVDD), Display Port (DP_SVDD), and SerDes (SVDD) power supplies of LS1028A.
U3	LTC7151S	Linear Technology	3V3	3.3 V at 15 A	Supplies power to board components: CPLD IO and VDD, Display Port, SGMII PHY, M.2 connectors, SD card, eMMC memory, I2C EEPROMs, current monitor (INA220), Temperature monitor (SA56004ED), CAN transceivers, mikroBUS connectors, misc components (buffers and translators). **NOTE** Filtered 3V3 also powers USB (USB_HVDD of LS1028A).
U4	MC34716EP	NXP Semiconductors	1V2	1.2 V at 4 A	DDR4 DRAM memories LS1028A DRAM controller core and I/O
			VTT_0V6	0.6 V at 3 A	Address and control bus termination supply

Table continues on the next page...

Table 4. Secondary power supplies (continued)

Part identifier	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
			MVREF	0.6 V at 3 A	Reference voltage for DDR4 DRAM memories
U6	MC34VR500V9ES	NXP Semiconductors	1V0, 2V5, 1V35, 1V8	• 1.0 V at 1.1 A • 2.5 V at 0.8 A • 1.35 V at 0.4 A • 1.8 V at 2.5 A	Multi-output DC/DC regulator with four switched outputs, two LDO outputs (VDD and DDR enable), and one reset control output to CPLD (RST_OUT). Four switched outputs are: • SW1LX: 1.0 V for the QSGMII PHY VDD and VDDA • SW2LX: 2.5 V for QSGMII PHY VDD25, VDD25A, and DDR4 memory VPP • SW3LX: 1.35 V; Filtered 1.35 V is supplied to LS1028A X1VDD, AVDD_SD1_PLL1, and AVDD_SD1_PLL2 • SW4LX: 1.8 V for board components: UART transceiver, XSPI memories, eMMC memory IO, CPLD IO bank3, clockgen VDD and VDDA **NOTE** Filtered 1V8 also powers LS1028A power supplies: AVDD_CGA1, AVDD_CGA2, AVDD_PLAT, DP_SAVDD, AVDD_D1, and AVDD_PIXEL. **NOTE** Jumper-enabled 1V8 also powers PROG_MTR and PROG_SFP.

Table continues on the next page...

Table 4. Secondary power supplies (continued)

Part identifier	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
U7	FPF1321UCX	ON Semiconductor	EVDD	3.3 V 1.8 V	eSDHC IO Power. **NOTE** EVDD boots up to 3.3 V and can be changed to 1.8 V depending upon the SD_VSEL pin state that is controlled from the LS1028A SDHC IP block. **NOTE** The FPF1321UCX is a power switch, not a power supply. .
U8	MAX8902B	Maxim Integrated	TA_BB_VDD	0.9 V / 1.0 V at 0.15 A	Power supply for TA_BB_VDD.

1. VDD is 1.0 V or 0.9 V depending upon the state of GPIO1_DAT24 GPIO pin of LS1028A.

2.2.3 Power supply sequence

The LS1028ARDB board is configured to switch ON automatically when the 12 V power supply is switched ON and is connected to jack (J1) on the board.

The 12 V input can be subsequently power cycled using the following events:

- The power switch (push button) is pressed
- The register bit, PWR_CTL2[PWR], is set to '1' using the I2C or JTAG/CCS communication paths

On the availability of 12 V supply to the power regulators, the orderly enable of all power supplies are sequenced using powergood of the regulators, as shown in the following figure.

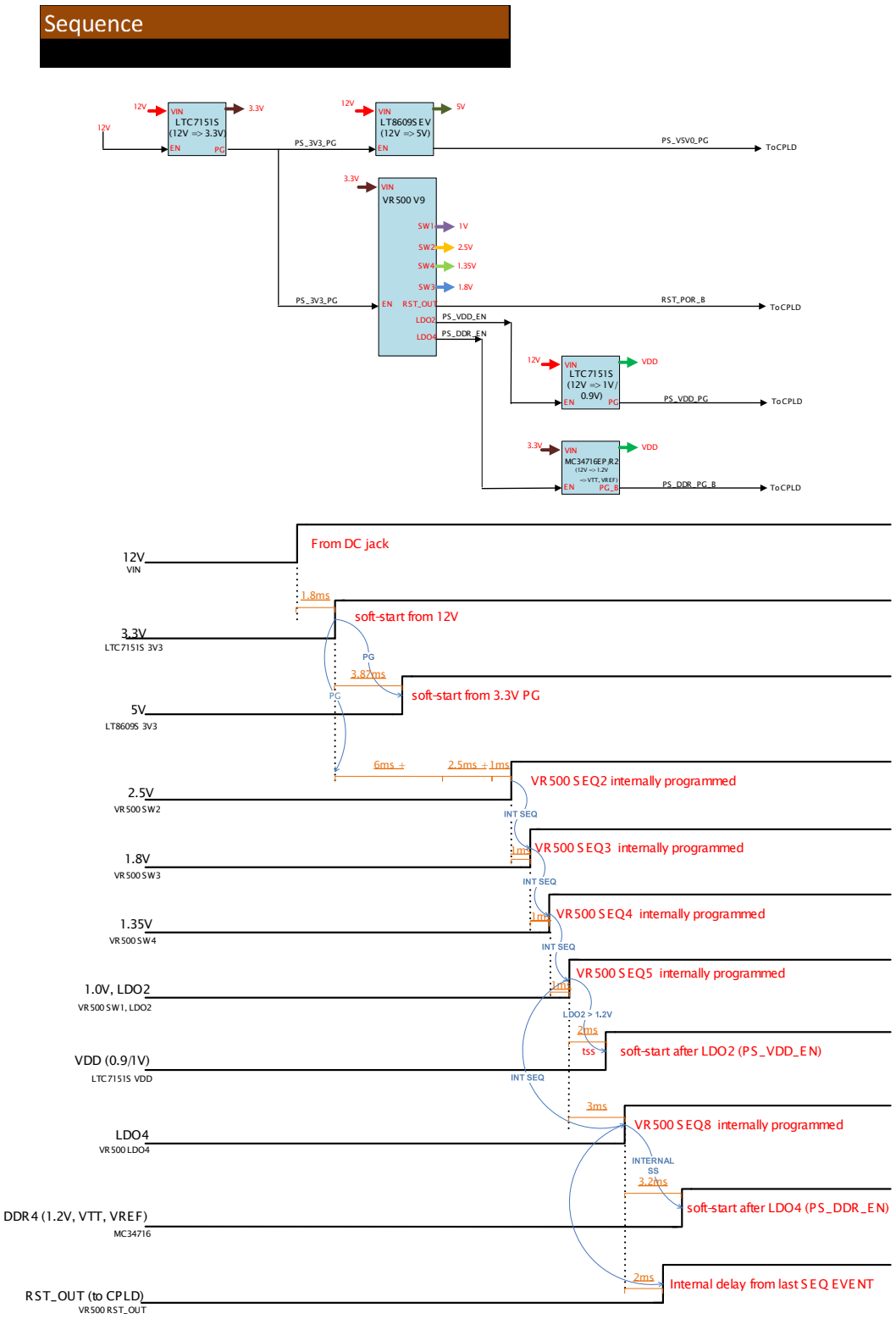


Figure 6. Power up voltage sequence

NOTE

The LS1028ARDB follows the power supply sequencing requirements as detailed in *QorIQ LS1028A Data Sheet*.

2.2.4 Current and power measurement

The LS1028ARDB implements onboard current and power measurements only for the VDD supply. The table below lists all measurable supplies.

Table 5. Power monitoring

Power	Measurement device	Shunt resistor value	Notes
VDD	INA220	0.001	The VDD supply powers the LS1028A core (0.9 V / 1 V), USB (USB_SDVDD, USB_SVDD), DisplayPort (DP_SVDD) and SerDes (SVDD) power supplies.

Power supplies not listed in the above table are considered as low-current/incidental supplies and are not instrumented for power measurement.

2.3 Clocks

The LS1028ARDB provides all the clocks required for the processor and peripheral interfaces. The figure below shows the LS1028ARDB clock architecture.

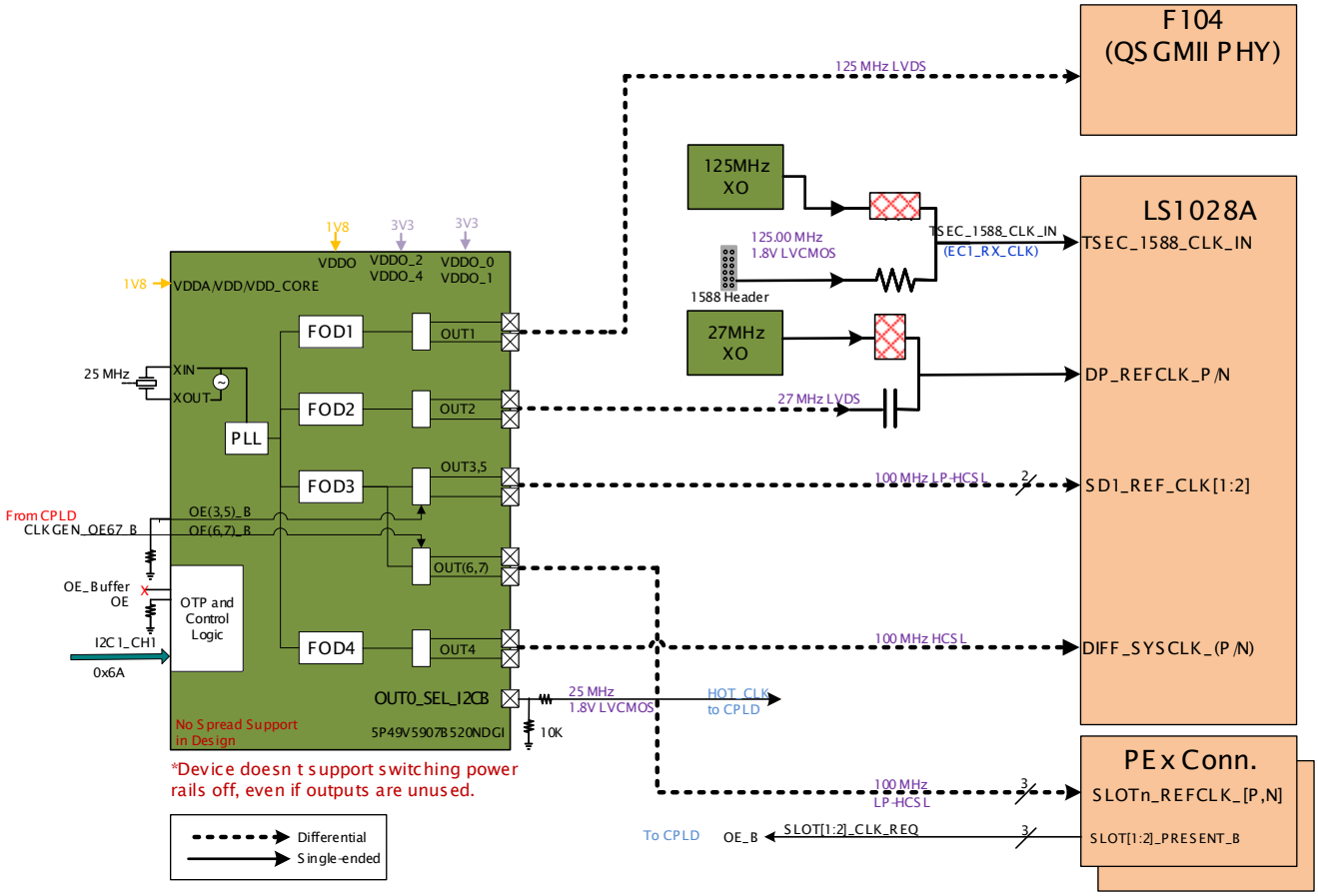


Figure 7. LS1028ARDB clock architecture

The 5P49V5907B520NDGI is a programmable clock generator that generates most of the clocks. Clock configurations are stored in its one-time programmable (OTP) memory. The configuration in volatile memory can be changed through the I2C1_CH1 interface. The device is accessible at 0x6A I2C 7-bit address. The frequencies are generated from a 25 MHz crystal (603-25-261 from FOX Electronics). The following table summarizes the specifications of each clock.

Table 6. LS1028ARDB clocks

Part identifier	Clock generator	Clock	Specifications	Destination
U9	IDT 5P49V5907B520NDGI	VDD0: FPGA_CLK_25MHz	• Frequency: 25 MHz • Output type: LVCMOS • Operating voltage: 3.3 V	CPLD
		OUT3,5: SD1_REF_CLK1_[P, N] SD1_REF_CLK2_[P,N]	• Frequency: 100 MHz • Output type: LP-HCSL • Operating voltage: 1.8 V	SerDes1 controller
		OUT6, 7[1]: PEXM2_1_REFCLK_[P,N] PEXM2_2_REFCLK_[P,N]	• Frequency: 100 MHz • Output type: LP-HCSL • Operating voltage: 1.8 V	M.2 connectors 1 and 2
		OUT4: DIFF_SYSCLK[P, N]	• Frequency: 100 MHz • Output type: HCSL • Operating voltage: 3.3 V	DIFF_SYSCLK
		OUT2: DP_REFCLK_[P, N]	• Frequency: 27 MHz • Output type: LVDS • Operating voltage: 3.3 V	Display Port
		OUT1: 125M0_LVDS_REF_CLK_[P,N]	• Frequency: 125 MHz • Output type: LVDS • Operating voltage: 3.3 V	QSGMII PHY
Y2[2]	125 MHz crystal oscillator (KC5032A125.000C1GE00)	EC1_125MHz_CLK (EC1_RX_CLK)	• Frequency: 125 MHz • Output type: LVCMOS • Operating voltage: 1.8 V	Ethernet controller / IEEE 1588 port

Table continues on the next page...

Table 6. LS1028ARDB clocks (continued)

Part identifier	Clock generator	Clock	Specifications	Destination
U91[3]	27 MHz crystal	DP_REFCLK_P DP_REFCLK_N	Frequency: 27 MHz	Display port
Y3	25 MHz crystal	ETH_XTALIN ETH_XTALOUT	Frequency: 25 MHz	SGMII PHY

1. The enable/disable for 100 MHz clocks to the M.2 connectors (J16 and J18/J20) is controlled by CPLD. The CPLD detects the CARD presence on the M.2 slots and enables the OUT 6 and 7 of the clock generator accordingly. Since, both the outputs are controlled from the same OE, 100 MHz clocks to the M.2 slots are enabled even if only one of the M.2 slots is populated.
2. The Y2 oscillator provides an option for stable 125 MHz CLK_IN to the 1588 block. The option can be enabled by mounting R388 and removing R387 that is mounted on the board by default.
3. The U91 oscillator provides an option for a low jitter clock input for Display interface. Clock from U91 can be enabled by removing C646, C647 and mounting C705, C706. The C646 and C647 capacitors are mounted by default.

2.4 DDR interface

The LS1028ARDB board supports four 1G x8 DDR4 SDRAM memory chips supporting data transfer rates of up to 1.6 GT/s and one 1G x8 DDR4 SDRAM memory chip for supporting ECC.

The address and control/command signals to the DDR4 SDRAM memory chips are routed in as per the Fly-by topology and are terminated to VTT (0.6 V). The data bus and associated signals, such as DM and DQS/DQS_B have one-to-one byte wise connections to the individual x8 DDR4 memories. The ECC nibble goes to the fifth DDR4 memory. The part number of the SDRAM memory chips is MT40A1G8SA-075:E (from Micron Technology).

Following are the characteristics of the LS1028A DDR4 memory controller:

- Up to 1.6 GT/s
- Supports 32-bit operation (with ECC support)
- Supports x8 devices
- Supports two chip selects, D1_MCS0_B and D1_MCS1_B; however, on board only D1_MCS0_B chip select is supported
- IOs powered by 1.2 V power supply from MC34716EP switch regulator

The MC34716EP switch regulator generates the following different power supplies for the DDR4 controller IO, memory devices, and terminations: VCC_GVDD_S (1.2 V), VTT (0.6 V) and VREFCA (0.6 V). The memory interface including all the necessary termination and I/O power are routed, as shown in the following figure.

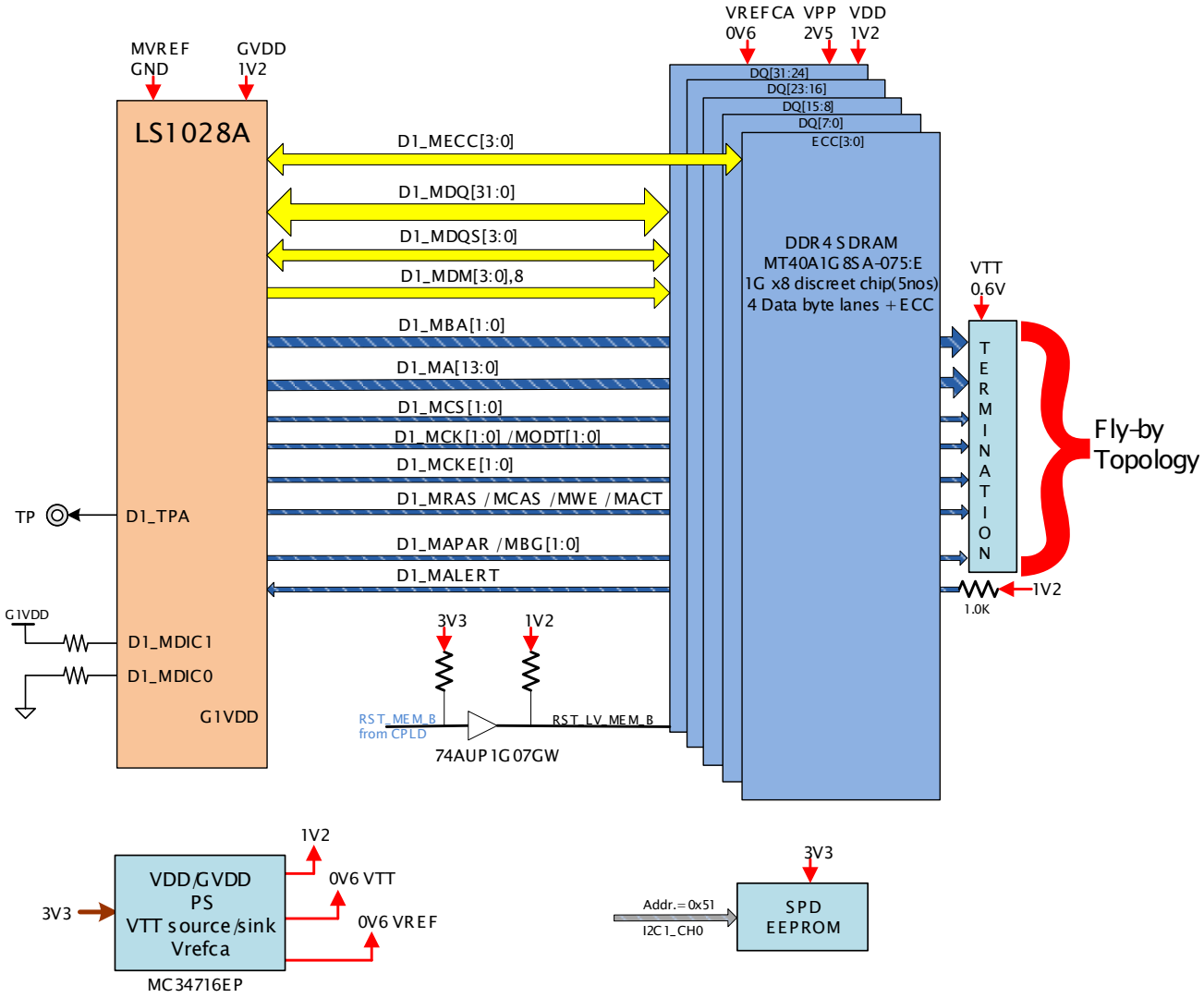


Figure 8. DDR4 interface

2.5 USB interface

The LS1028ARDB supports two USB 3.0 ports. The USB 1 port is connected to a Type A connector and is configured as host. Type A connector is always host only. The USB2 port is connected to a Type C connector and is configured as downstream facing port (DFP) or upstream facing port (UFP). Based on the configuration detected on the Type C port, the USB2 PHY can operate either in host or device mode. The following figure shows the architecture of the USB 3.0 interface.

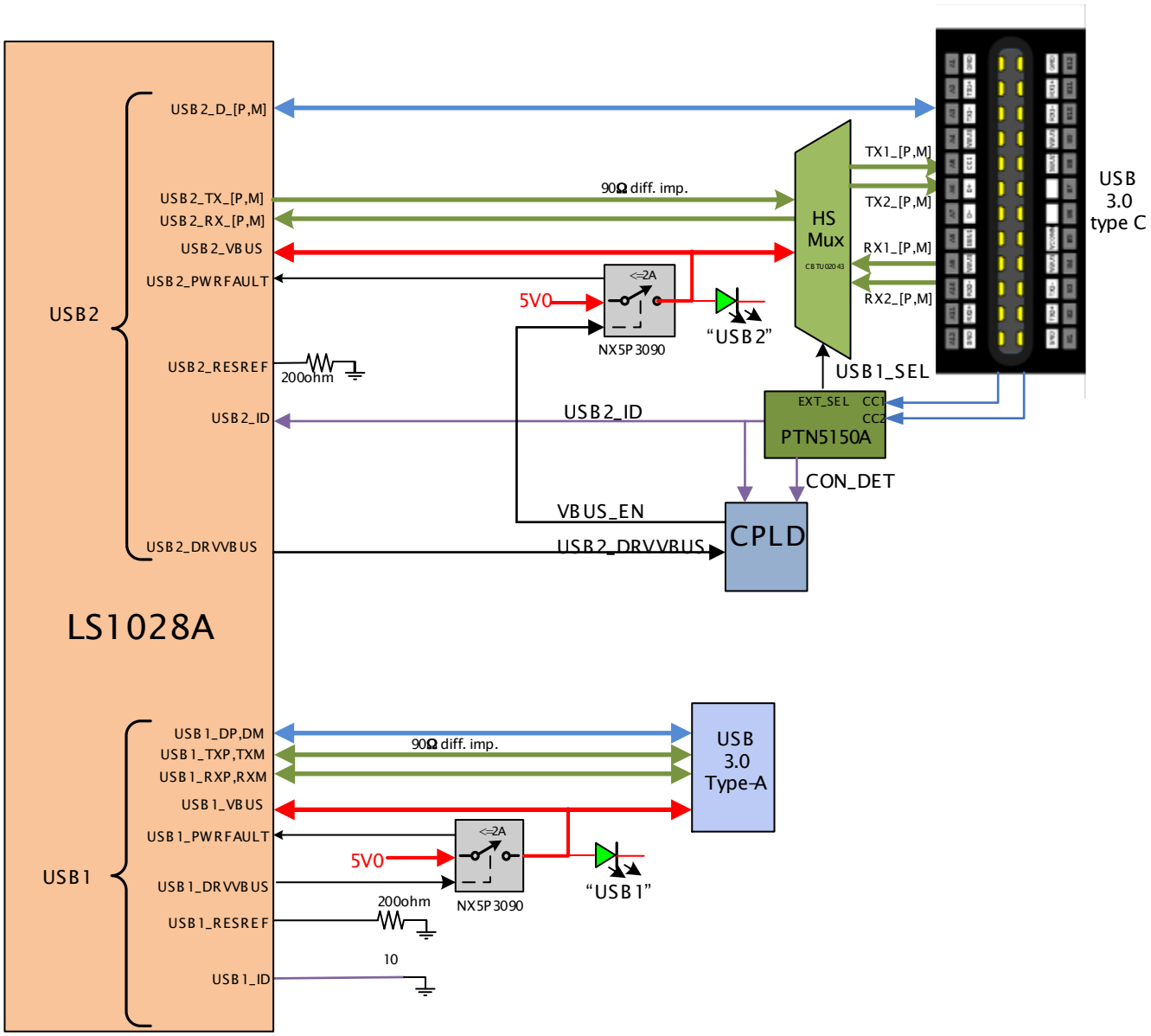


Figure 9. USB architecture

The PTN5150A (from NXP) is a small low-power configuration channel logic chip that detects (through CC1 and CC2 pins) and indicates to the USB controller (through USB2_ID signal) if the USB2 Type C connector is configured as a device or host. The PTN5150A is configured to operate the USB3 Type C port in DFP mode with default USB current capability (0.5 A / 0.9 A). To support higher current on the Type C (USB2) port, the hardware configuration of PTN5150 and NX5P3090UK VBUS switch should be changed. Refer to the device datasheet for more information.

The USBx_DRVVBUS and USBx_PWRFAULT pins of each USB controller are connected to a programmable-current USB switch, NX5P3090UK (from NXP), for individual port management. The USB switch is powered from +5 V USB power supply. To indicate power fault conditions, the USB switch sends PWRFAULT signals to the USB controller. For USB2 port, the USB switch drives USB2 VBUS (USB2_VBUS) when USB2_DRVVBUS=1, USB1_ID = 0, and USB2_CON_DET=1, this logic is controlled by CPLD. For USB1 port, the USB switch drives USB1 VBUS (USB1_VBUS) when USB1_DRVVBUS=1.

The maximum allowed current consumption of a USB connected device is 900 mA per channel.

Both, USB1 and USB2 connectors have an LED nearby, USB1_5V and USB2_5V, respectively, which are active when the +5 V USB power supply is enabled to the connectors.

2.6 DisplayPort

The LS1028A processor supports and embedded DisplayPort (eDP) TX controller that connects to the DisplayPort connector on the board for digital display.

The controller supports the following:

- Supports DisplayPort 1.3 and eDP 1.4
- Supports link transfer rates of up to HBR2 (5.4 Gbit/s) and display resolution up to 4Kp60

The CONFIG1 and CONFIG2 pins of the DisplayPort are pulled down with 1 MΩ resistors to avoid any power driven on the DP_PWR pin from a downstream device.

The DP_PWR pin can provide 3.3 V up to 3 A inrush current through a power switch NX5P3090UK (controlled through the CPLD register).

2.7 SerDes interface

The LS1028A processor supports one SerDes LYNX36 module with four high-speed serial communication lanes to support various protocols, such as SGMII, QSGMII, PCIe, and SATA.

The figure below shows the LS1028ARDB SerDes architecture.

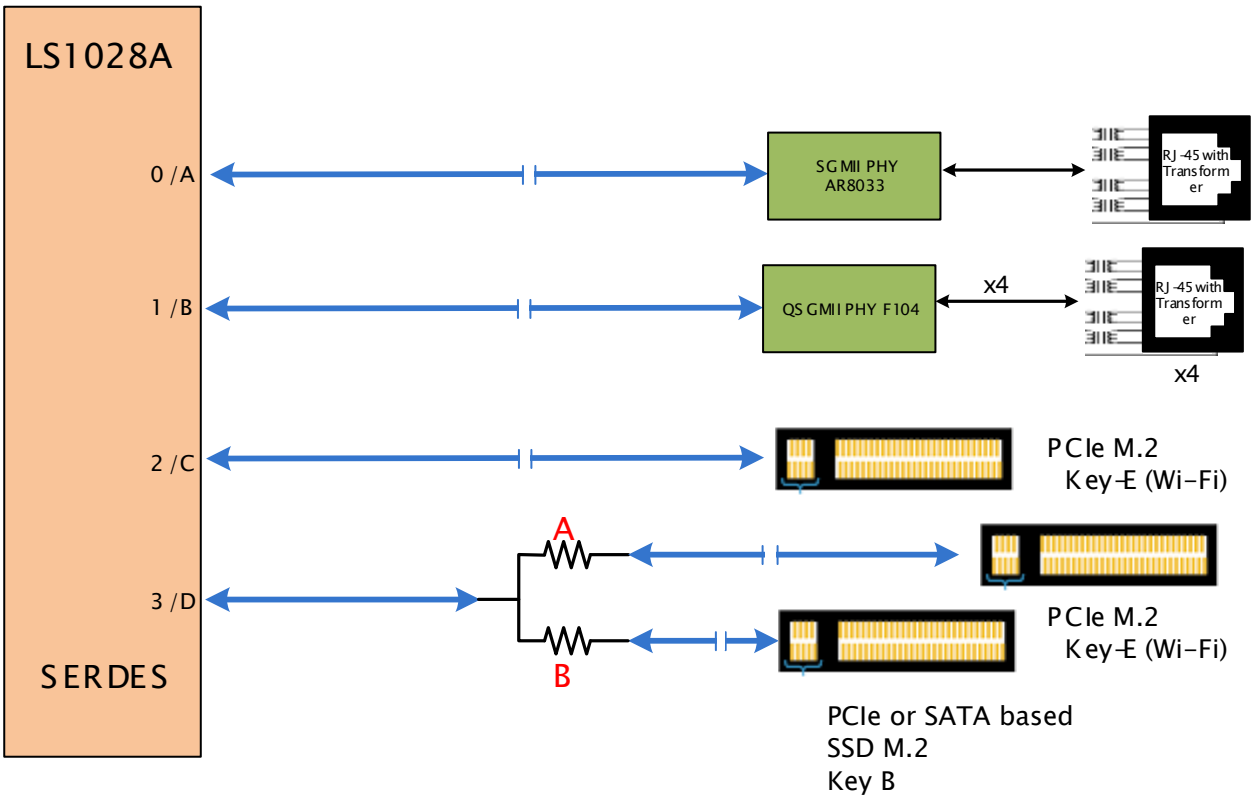


Figure 10. SerDes architecture

The LS1028A SerDes module support several protocols, which are assigned to dedicated functions on the LS1028ARDB, as shown in the table below.

Table 7. SerDes assignments

SerDes module	Lane	Connectivity	Port
1	0 / A	Qualcomm AR8033 1 GbE PHY	1 x 1GbE RJ45 on SGMII MAC interface
	1 / B	NXP F104S8A QSGMII Quad 1 GbE PHY	4 x 1GbE RJ45 on QSGMII MAC interface
	2 / C	PCIe Gen 3 (8 Gbit/s)	M.2 Key E slot for Wi-Fi cards
	3 / D	PCIe Gen 3 (8 Gbit/s) or SATA 3.0 (6 Gbit/s)	M.2 Key E slot for Wi-Fi cards or M.2 Key B slot for SATA based SSD cards

2.8 Ethernet controller interface

The LS1028A processor supports one Ethernet controller (ENETC), which connects either to an onboard 1588 access header or to an audio transceiver (through TX signals only) and an SGMII port (over LYNX36 SerDes Lane A). The controller also supports QSGMII connectivity through the TSN switch and it is available over LYNX36 SerDes interface (Lane B).

The EMI1 MDIO/MDC signals control the SGMII and QSGMII PHY transceivers. EMI1 operates at OVDD (1.8 V) levels. The signals are bi-directionally shifted to 2.5 V for compatibility with both AR8033 (one-port SGMII) and F104S8A PHY (Four-port QSGMII).

2.8.1 SGMII Ethernet

The onboard Ethernet PHY, Qualcomm AR8033 PHY (U23) connects to the ENETC of the LS1028A processor using SGMII protocol over LYNX36 SerDes lane A.

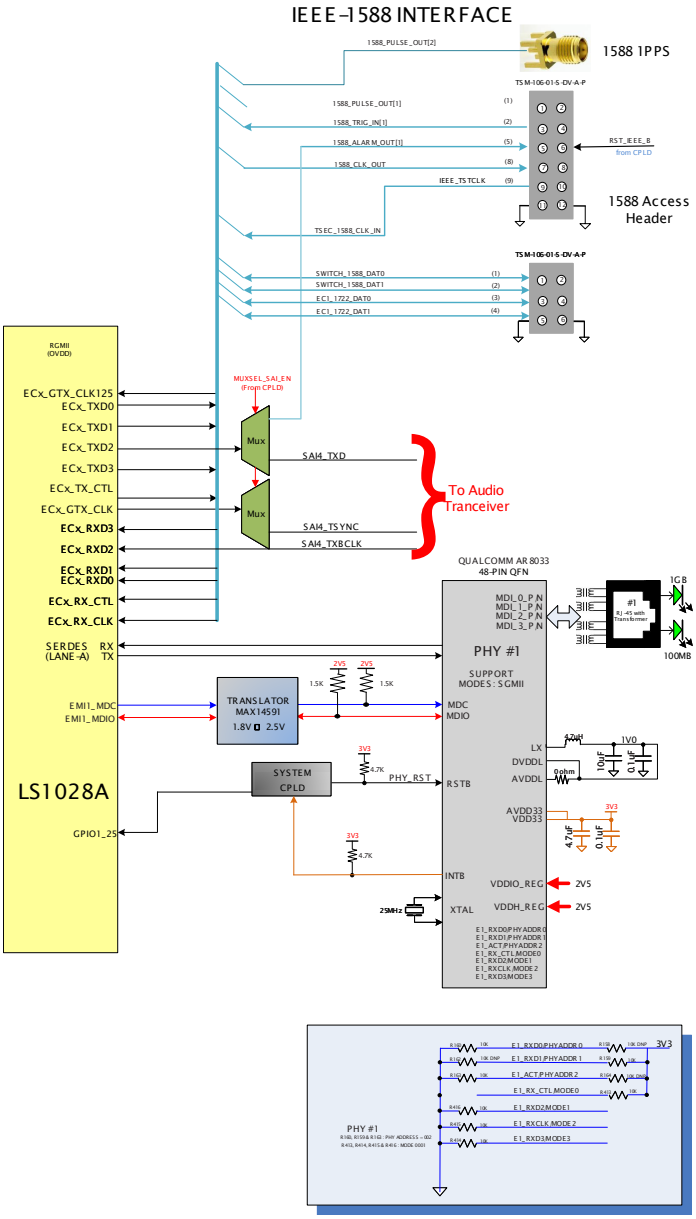


Figure 11. SGMII and IEEE 1588

Table 8. Hardware bootstrap settings for SGMII PHY

Setting	Description
PHY_AD[2:0]	PHY address = 0b00010
MODE[3:0]=0001	SGMII<=>UTP

2.8.2 QSGMII Ethernet

The onboard Ethernet PHY, NXP F104S8A PHY (U24), connects to the TSN switch of the LS1028 processor using QSGMII protocol over SerDes lane B.

The following figure shows the QSGMII interface.

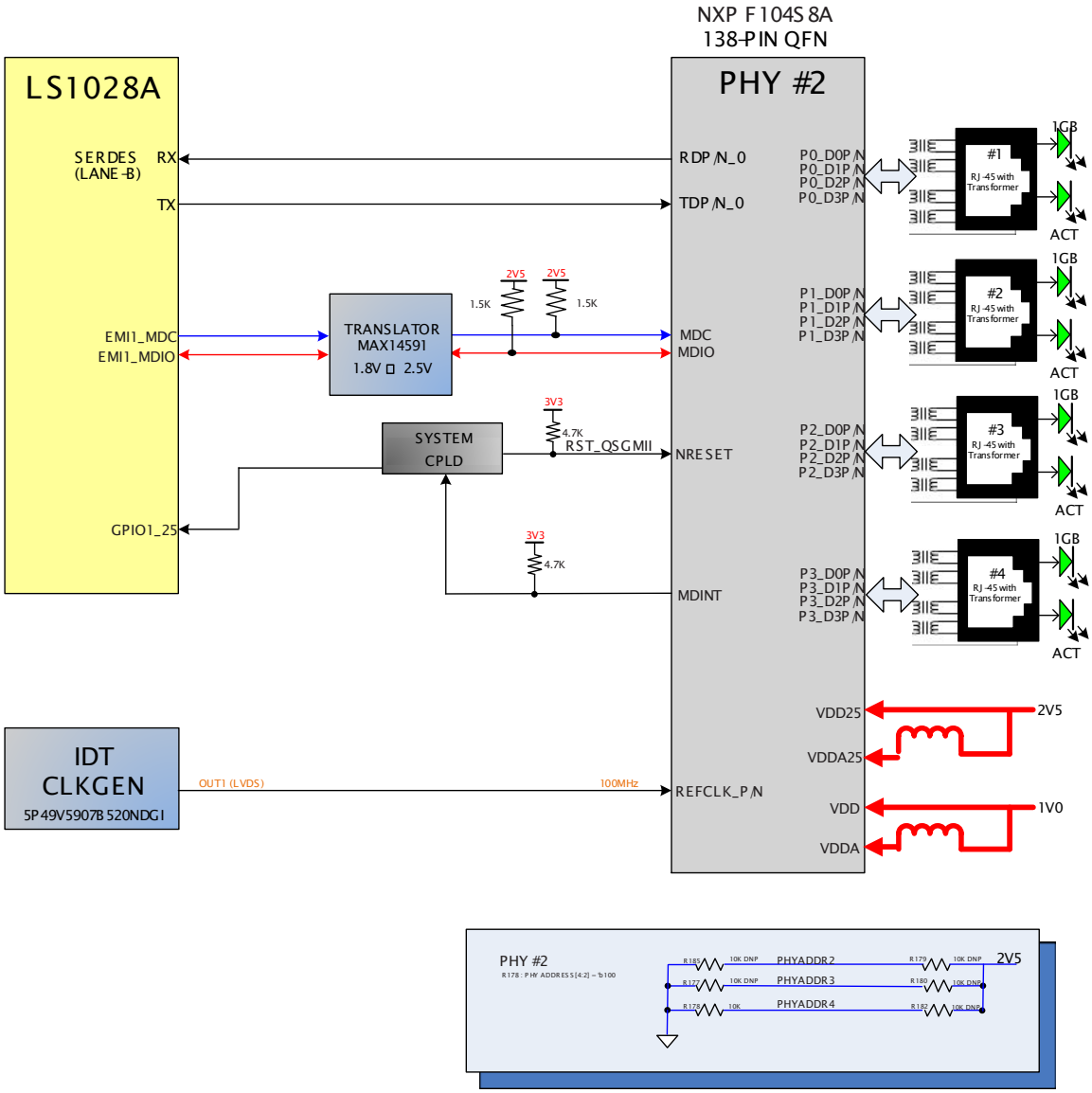


Figure 12. QSGMII port

Table 9. Hardware bootstrap settings for QSGMII PHY

Setting	Description
PHY_AD[4:2]	PHY address = 0b100
MODE	• REFCLK_SEL[1:0] = 00: 125 MHz is used as REFCLK. • COMA_MODE = 0: PHY comes out of reset as soon as reset is de-asserted.

2.8.3 IEEE 1588 interface

The LS1028A processor provides support for the IEEE 1588™ precision time protocol (PTP), which works in tandem with ENETC to time-stamp the incoming packets. A 12-pin header (J11) is provided on the board to allow support for 1588 protocol. The SMA connector (J12) is used to analyze time synchronization by measuring the pulse per second (PPS) signal. A 6-pin header (J13) is used to access TSN switch 1588 pins and IEEE 1722 pins.

The IEEE signals are multiplexed with the SAI4 signals (see Figure 11. on page 28) and LS1028ARDB uses the multiplexer 74LVC2G3157DPJ (U92, from Nexperia) to demux. The IEEE signals available on header J11 and J13 depend upon the RCW settings and the appropriate signal through the CPLD. For more information on the RCW settings, see *QorIQ LS1028A Reference Manual*.

Figure 11. on page 28 shows the architecture of the IEEE 1588 system.

The table below lists the testing options provided by the IEEE 1588 test header.

Table 10. IEEE 1588 port

IEEE 1588 feature	Specifications	Description
Clocks	Input clock	ETH reference clock (to processor) is driven from an onboard 125 MHz oscillator source. Under software configuration, it may be clocked from the IEEE 1588 header instead.
Signals	Other related signals	All remaining IEEE 1588 signals are connected to the dedicated header pins

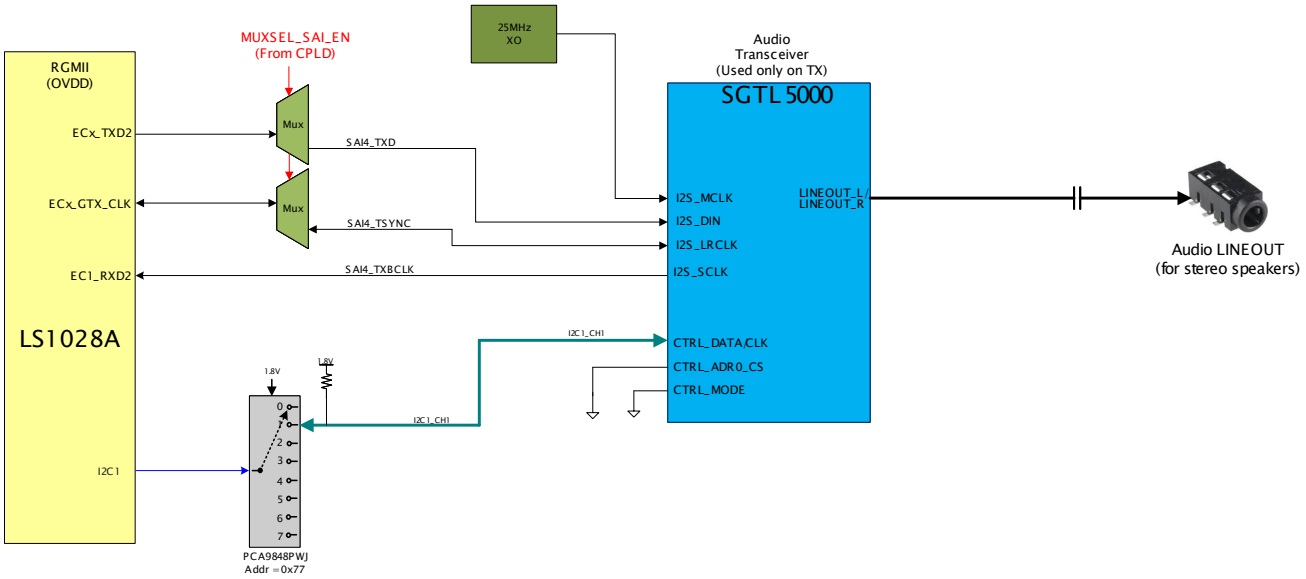
Table 11. IEEE1588 and IEEE1722 signals

Signal name	Connector name and Designator	Description	Availability with Audio
1588_PULSE_OUT2	1PPS(IEEE1588) (J12)	SMA connector	Yes
1588_CLK_OUT	IEEE1588 (J11)	IEEE1588 header	Yes
1588_ALARM_OUT[1]	IEEE1588 (J11)	IEEE1588 header	No
1588_PULSE_OUT1[1]	IEEE1588 (J11)	IEEE1588 header	No
SWITCH_1588_DAT1[1]	TSN Switch IEEE1588 & IEEE1722 (J13)	IEEE1588 signals from TSN switch	No
SWITCH_1588_DAT0[1]	TSN Switch IEEE1588 & IEEE1722 (J13)	IEEE1588 signals from TSN switch	No
EC1_1722_DAT0[1]	TSN Switch IEEE1588 & IEEE1722 (J13)	IEEE1722 synchronization signal for audio	Yes
EC1_1722_DAT1[1]	TSN Switch IEEE1588 & IEEE1722 (J13)	IEEE1722 synchronization signal for audio	No
1588_TRIG_IN1	IEEE1588 (J11)	IEEE1588 header	Yes
1588_CLK_IN[1]	IEEE1588 (J11)	IEEE1588 header	Yes

1. This signal is available only when RCW field EC1_SAI4_5_PMUX is set to 3'b101 (IEEE1588).

2.9 Synchronous audio interface (SAI)

The LS1028ARDB board supports audio through NXP SGTL5000-32QFN audio codec (U93). The board supports one audio LINEOUT (J34) for headphone and stereo speakers. The figure below shows the LS1028ARDB audio interface architecture.



The SGTL5000 has 25 MHz as MCLK input to generate the required SAI and internal clocks. The device can provide or take as input the TSYNC based on desired configuration.

The SAI4 signals are multiplexed with the IEEE signals (see Figure 11. on page 28) and LS1028ARDB uses the multiplexer 74LVC2G3157DPJ (U92, from Nexperia) to demux. Software must configure the appropriate signal through FPGA, to select the appropriate controller and interface.

Table 12. SAI4 configuration and setup

Configuration signal	Controlled by	Description
MUXSEL_SAI_EN	BRDCFG3[2]	• 0: IEEE signals connect to the IEEE header • 1: IEEE signals connect to the SAI4 CODEC

2.10 M.2 connectors

The LS1028ARDB supports M.2 connectors (Key E and Key B) that are supported through SerDes lanes 2 and 3.

One M.2 Key E connector (J16) is connected through the LYNX36 SerDes lane 2. This connector supports only 1630 and 2230 PCIe Gen3 card types to provide wireless connectivity including Wi-Fi, Bluetooth, and NFC.

The other M.2 Key E connector (J18) is connected through the LYNX36 SerDes lane 3. However, lane 3 can also connect to the M.2 Key B connector (J20) as per the register settings mentioned in Table 13. Register configuration on page 31 to support solid state storage devices (SSD) (SATA 3.0). The M.2 Key B connector supports 2230 and 2242 module card types.

The following table describes the three-pad arrangement that is required to select either Type E connector or Type B connector on the LYNX36 SerDes lane 3.

Table 13. Register configuration

M.2 connector select	Signal name	Mount register/capacitor	Values
Type E[1]	PEXM2_2_REFCLK_P	R214	0 Ω

Table continues on the next page...

Table 13. Register configuration (continued)

M.2 connector select	Signal name	Mount register/capacitor	Values
	PEXM2_2_REFCLK_N	R213	0 Ω
	PEXM2_2_PET_P	C409	0.22 µF ±10%
	PEXM2_2_PET_N	C410	0.22 µF ±10%
	PEXM2_2_PER_P	R216	0 Ω
	PEXM2_2_PER_N	R215	0 Ω
Type B	PEXM2_2_REFCLK_P	R223	0 Ω
	PEXM2_2_REFCLK_N	R222	0 Ω
	PEXM2_2_PET_P	C423	0.01 µF ±10%
	PEXM2_2_PET_N	C422	0.01 µF ±10%
	PEXM2_2_PER_P	C420	0.01 µF ±10%
	PEXM2_2_PER_N	C421	0.01 µF ±10%

1. By default, registers and capacitors are mounted for the M.2 Key E connector (J18).

The M.2 Key E connectors J16 and J18 have 1x4-pin headers J17 and J19, respectively, for coexistence signals. Since, co-existence signal assignments on M.2 connectors is vendor dependant, refer to the vendor-specific documentation of M.2 modules for details.

2.10.1 Adapters

You can use adapters to convert M.2 connector to a PCIe slot for PCIe Gen 1 and Gen 2 compliant endpoints. For more detail on these adapters, click the following links.

- P11S-P11F - M.2 (NGFF) to PCI-E Extender Board
- P11S-P11F - Duo PCI-E to M.2 (NGFF) Extender Board

2.11 DUART interface

The LS1028A device provides one instance of the DUART block, which support two 2-wire serial ports with no hardware flow control. On the LS1028ARDB board, the DUART ports connect to an RS-232 transceiver (Linear Technology LTC2804-1), which translates the UART1 and UART2 signals to RS-232 levels. The RS-232 signals of UART1 and UART2 are provided on dual DB9 male connector (DTE configuration) to provide convenient communication channels to both terminal and host computers.

It is recommended to use UART1 as a debug port. The LTC2804-1 transceiver can support 1 Mbit/s data rate on each of the serial ports.

The figure below shows the LS1028ARDB DUART connections.

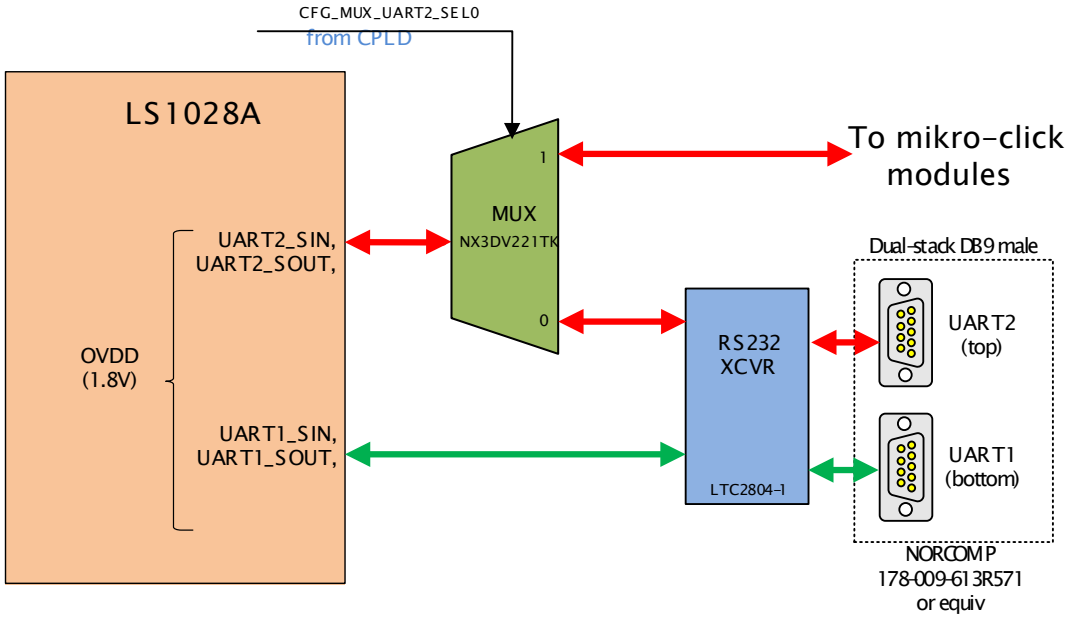


Figure 14. DUART architecture

The UART2 signals can be used either to communicate with mikro-click modules or with RS232-compliant devices using the LTC2804-1 transceiver. The selection is done through a mux which is controlled through the CFG_MUX_UART2_SEL0 signal by CPLD.

Table 14. UART configuration and setup

Configuration signal	Config register	DIP switch	Description
CFG_MUX_UART2_SEL0	BRDCFG3[5:4]	SW2[5:6]	• 0x: UART2 on DB9 connector (default value) • 10: UART2 on mikro-click module 1 • 11: UART2 on mikro-click module 2

2.12 CAN interface

The LS1028A processor supports two controller area network (CAN) modules, CAN1 and CAN2. On the LS1028ARDB, the CAN ports are available for external connection through a dual-port stacked DB9 male connector. Two high-speed CAN transceivers TJA1051T/3 from NXP (U54 and U56) provide an interface for the CAN ports to send and receive CAN signals to and from the processor. The TJA1052T/3 transceivers can support data rate of up to 5 Mbit/s in CAN with Flexible Data-Rate (CAN FD) phase.

The figure below shows the CAN architecture.

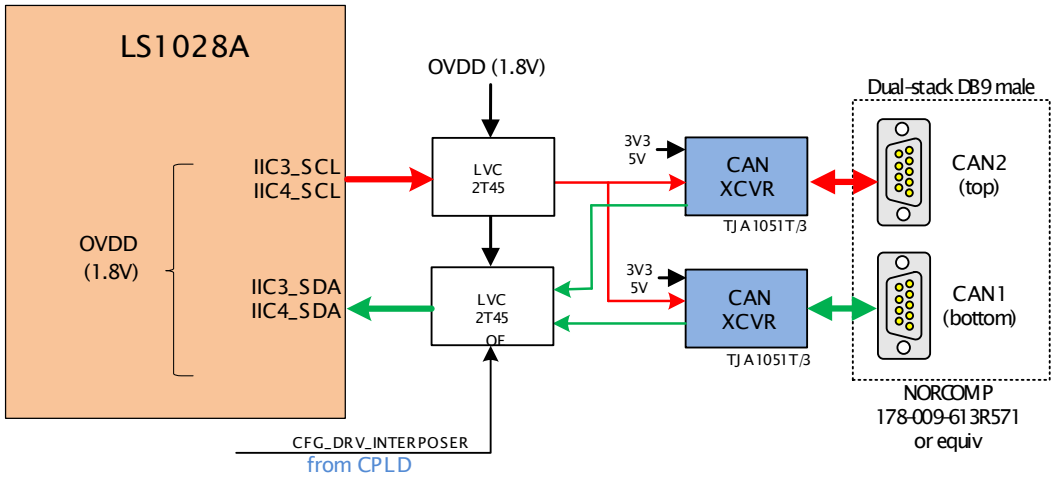


Figure 15. CAN architecture

2.13 I2C interface

The LS1028A processor supports up to six I2C buses. The I2C1 port is used for system setup and monitoring and the other ports should be programmed to be used for SDHC1 CD and WP, CAN 1 and 2 interfaces, GPIO, and USB2 PWRFAULT & DRVVBUS. These secondary functionalities should be enabled in the RCW field.

The I2C1 port is connected to a PCA9847PWJ I2C multiplexer to isolate address conflicts and to effectively manage the large number of I2C devices. The I2C1 port is connected to the level shifter device NTSX2102GU8H (from NXP) to enable bidirectional voltage level translation (1.8 V to 3.3 V and 3.3 V to 1.8 V) for CPLD and external I2C devices.

The figure below shows the I2C bus architecture.

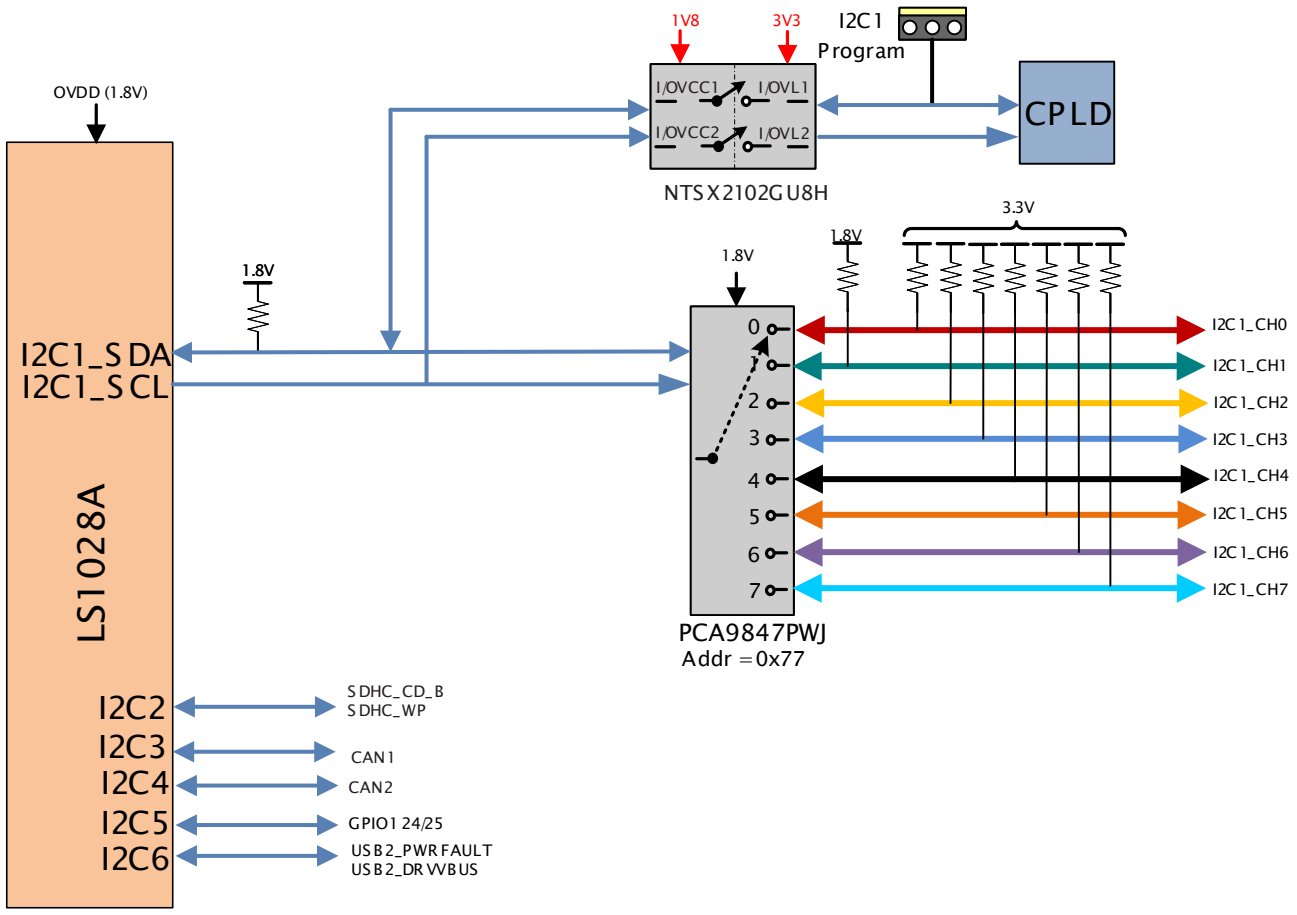


Figure 16. I2C bus architecture

The multiplexer used for the I2C1 bus partitions the bus into eight sub-buses, called "channels." Software must program the multiplexer to access one of the eight I2C1 channels. All boot-software-dependant devices are placed on channel 0, or "I2C1_CH0" as it is named. Channel 0 is the default selection upon reset so that software has immediate access to critical resources.

All channels on I2C1 are translated to 3V3 except channel 1, which operates at 1V8 (OVDD) power supply.

The I2C devices available on the I2C1 bus are shown in the figure below.

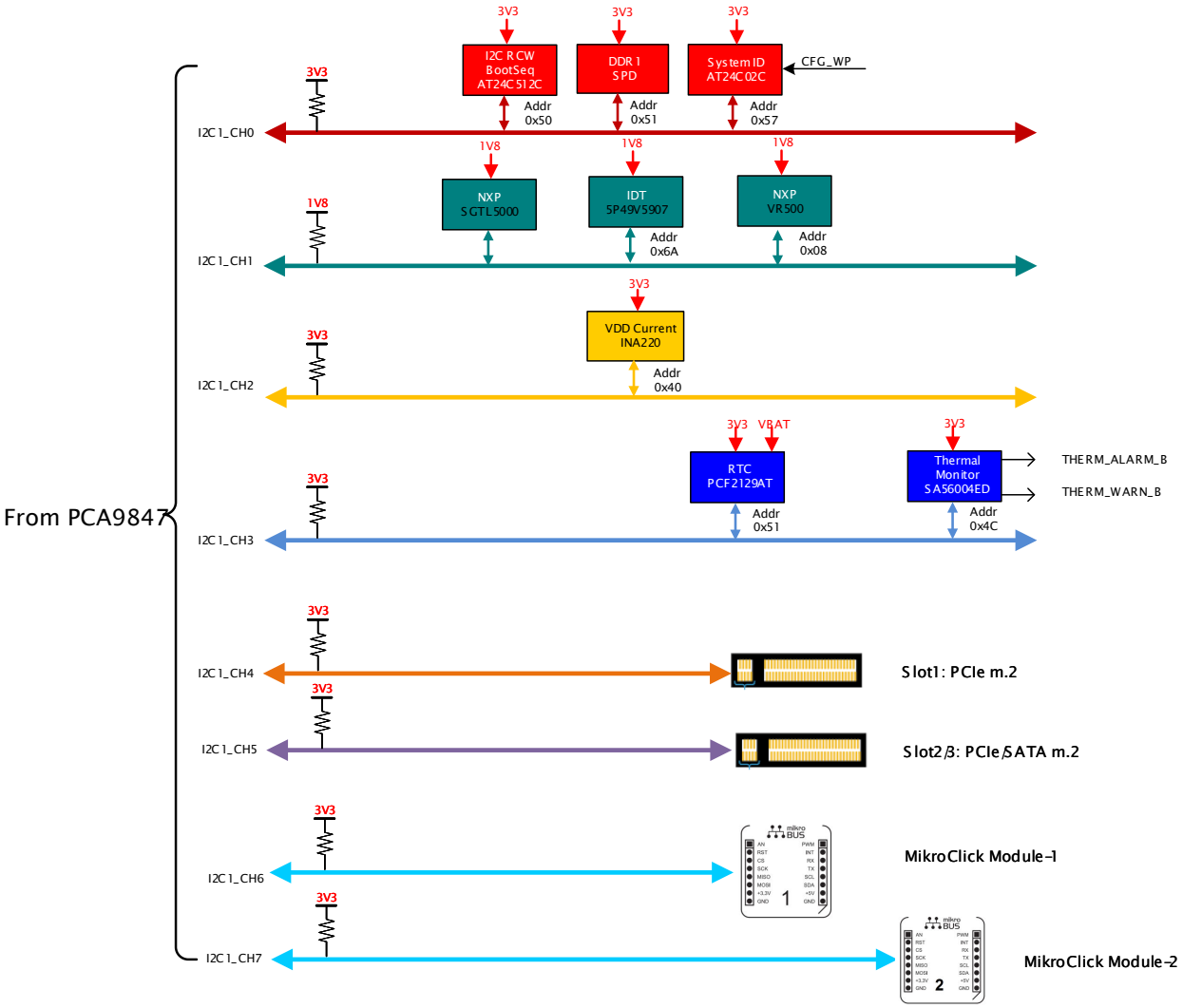


Figure 17. I2C1 channels

The following table describes the devices available on each of the eight I2C1 channels.

Table 15. I2C1 bus device map

I2C bus	7-bit address	Device	Description	Notes
(All)	-	I2C master	LS1028ARDB	
	0x66	I2C slave	CPLD	I2C access to CPLD BCSRs (registers).
	0x77	NXP PCA9847PWJ	I2C bus multiplexer (primary)	Converts I2C1 bus into eight channels
I2C1_CH0	0x50	Atmel AT24C512C-XHD-B: 64 KB EEPROM	UEFI/ boot memory	Provides I2C booting option. Write protectable.

Table continues on the next page...

Table 15. I2C1 bus device map (continued)

I2C bus	7-bit address	Device	Description	Notes
	0x51	AT24C04C 512-byte DDR4 SPD EEPROM	SPD data	Stores SPD and temperature data for DDR4 SDRAM memory. Write protectable.
	0x57	Atmel AT24C02C-XHM-B: 256-byte EEPROM	System ID	Stores board-specific data, such as MAC addresses and serial number/errata. Write protectable.
I2C1_CH1	0x0A	SGTL5000 32QFN	Low-power stereo codec	Audio transceiver providing audio LINEOUT for stereo speakers
	0x6A	IDT 5P49V5907	Programmable clock generator	Generates differential sysclk and reference clocks for DP, LYNX36 SerDes and PEX M.2 connectors
	0x08	NXP MC34VR500V9ES	PMIC switched outputs	Generates 1.8 V, 1.35 V, 1.0 V, and 2.5 V
I2C1_CH2	0x40	Texas Instruments INA220	VDD voltage/current/ power monitor	Reports voltage, current, and power data for VDD
I2C1_CH3	0x4C	NXP SA56004ED	Thermal monitor	Monitors processor thermal diode
	0x51	NXP PCF2129AT	Battery-backed clock	Provides time and date functionality with battery backup option
I2C1_CH4	I2C address is defined by the plugged-in PCIe card	PCIe M.2	Key E connector	I2C path for the M.2 connector (J16), which supports Wi-Fi cards on lane 2 of LYNX36 SerDes.
I2C1_CH5	I2C address is defined by the plugged-in PCIe/ SATA card	PCIe M.2	Key E / Key B connector	I2C path for the J18 or J20 M.2 connector which supports Wi-Fi or SATA SSD cards, respectively, on lane 3 of LYNX36 SerDes.
I2C1_CH6	I2C address is defined by the plugged-in mikro-click module	MIKROE 1597	BLE / BEE / NFC	Provides I2C connectivity to mikro-click modules on connectors J29 and J30.

Table continues on the next page...

Table 15. I2C1 bus device map (continued)

I2C bus	7-bit address	Device	Description	Notes
I2C1_CH7	I2C address is defined by the plugged-in mikro-click module	MIKROE 2395	BLE / BEE / NFC	Provides I2C connectivity to mikro-click modules on connectors J31 and J32.

NOTE

A 7-bit address does not include the read/write (R/W) bit as an address member, though some datasheets might do so. For consistency, all I2C addresses above are of 7 bits only.

2.14 XSPI interface

The LS1028ARDB octal serial peripheral interface (XSPI) supports two onboard XSPI serial flash memories (NOR flash and NAND flash) for boot image and one QSPI emulator for offboard QSPI emulation. The XSPI chip-select signals from the processor are driven to the XSPI memories or to the QSPI emulator through two high-speed multiplexers.

The XSPI memories and QSPI emulator supports single mode data transfer at boot; additionally, NOR flash memory supports octal mode, NAND flash memory supports qual mode, and QSPI emulator supports quad mode data transfer.

The figure below shows the LS1028ARDB XSPI connections.

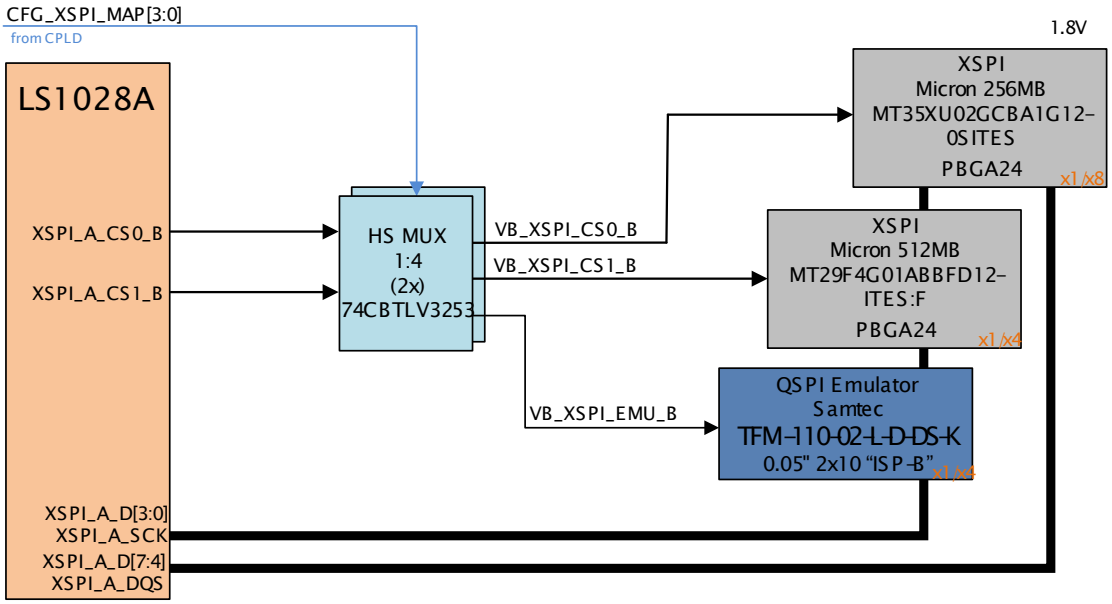


Figure 18. XSPI architecture

The table below shows the devices attached to the LS1028ARDB XSPI interface.

Table 16. Devices attached to XSPI interface

Part identifier	Part number	Manufacturer	Description
U32	MT35XU02GCBA1G12-0SIT ES	Micron	• 256 MB, PBGA24 x1/x8 SPI serial NOR flash memory • Supports 166 MHz SDR speed and 200 MHz DDR speed • Powers up in x1 mode
U35	MT29F4G01ABBFD12-ITES:F	Micron	• 512 MB, PBGA24 x1/x4 SPI NAND flash memory • Supports 166 MHz SDR speed • Powers up in x1 mode
J23	TFM-110-02-S-D-SN-K-TR	Samtec	A 2x10-pin connector that connects to an external QSPI flash emulator (DediProg EM100Pro) through an ISP-ADP-intel-B cable adapter. The EM100Pro emulator uses 1.8 V as the input/output voltage.

The table below describes the XSPI routing configuration.

Table 17. XSPI configuration

Configuration signal	DIP switch	CPLD register	Description
CFG_XSPI_MAP	SW1[8]	BRDCFG0[7:5]	**Table 18.**

Table 18.

Bit value	XSPI_A_CS 0	XSPI_A_CS 1	Description
000	sNOR	sNAND	Normal NOR
001	sNAND	sNOR	Normal NAND
010	Emulator	sNOR	Programmable NOR
011	Emulator	sNAND	Programmable NAND
100	sNOR	Emulator	Boot from sNOR and program emulator

The NAND and NOR device selection is based on the RCW_BOOT_SRC settings. Refer to System configuration on page 46 for more details.

2.15 JTAG port

The JTAG port provides access to the processor using a standard 10-pin Arm Cortex JTAG connector for debugging purposes. The following figure shows the LS1028ARDB JTAG architecture.

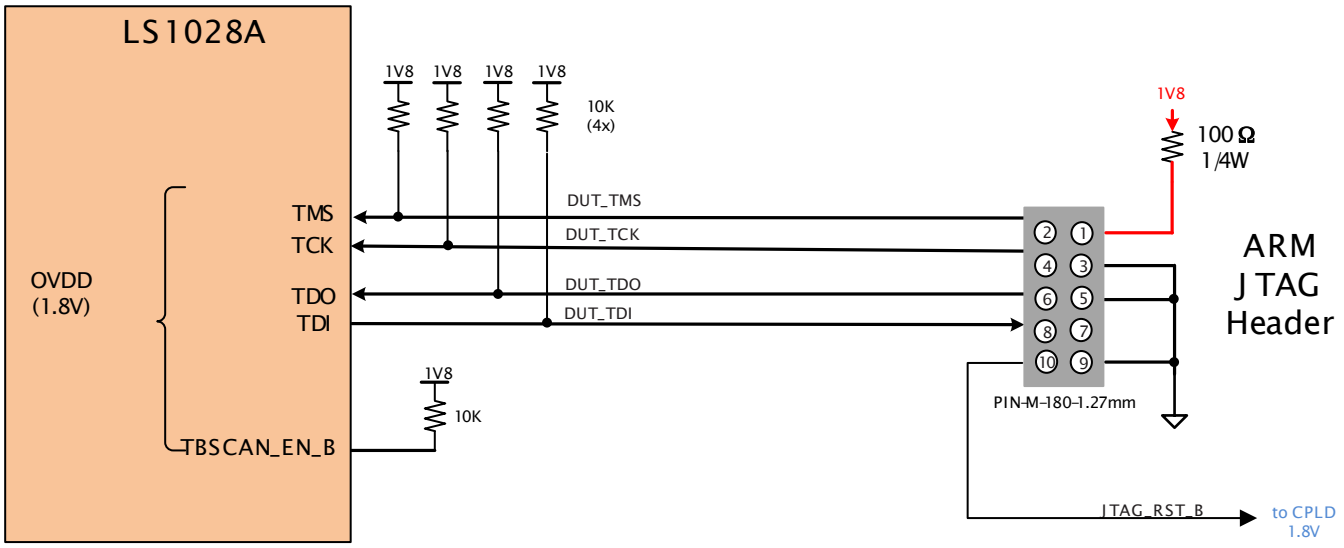


Figure 19. JTAG architecture

2.16 eSDHC interface

The LS1028A processor supports two enhanced secured digital host controllers (eSDHC): eSDHC1 and eSDHC2. The LS1043 interposer can support only one SDHC controller and it is connected to SDHC1.

The figure below shows the eSDHC1 and eSDHC2 connections in the LS1028ARDB.

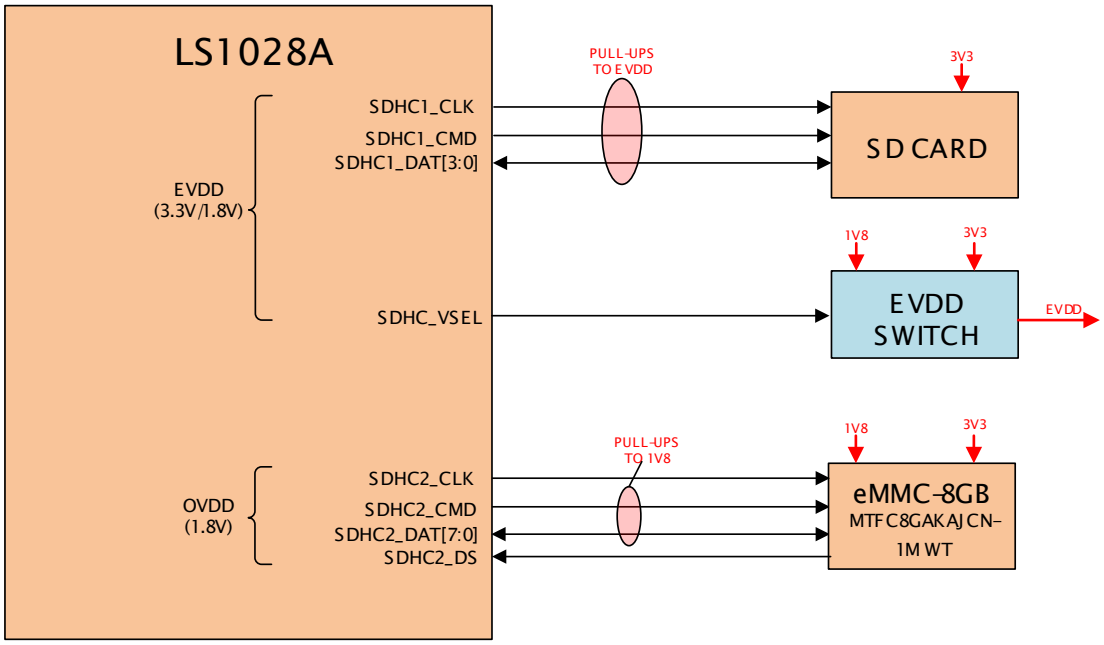


Figure 20. eSDHC architecture

The LS1028ARDB eSDHC1 interface is connected to a secure digital (SD) connector (P2) on board to support an SD card. For default- or high-speed of SD card, the eSDHC1 controller and the SD card operate at EVDD (3.3 V) power. However, in case the eSDHC1 controller requires the ultra-high speed (UHS) of the SD card, the card and the controller operates at 1.8 V. The EVDD switch (FPF1321UCX) changes the 3.3 V supply to 1.8 V for the controller depending upon the value of SDHC_VSEL signal.

The following table describes EVDD switch output voltage depending upon the SD card speed and SDHC_VSEL value.

Table 19. EVDD switch output voltage

SD card speed	SDHC_VSEL	EVDD switch voltage
Default or high speed	0	3.3 V
Ultra-high speed (UHS)	1	1.8 V

NOTE

To move from UHS state to default- or high-speed state of SD card, a power reset is required.

I2C2 must be programmed in the RCW to serve as the card detect (CD_B) and write protect (WP) pins for the eSDHC1 interface. This happens automatically when the SD card slot is selected as the boot device.

The LS1028ARDB eSDHC2 interface is connected to an 8 GB eMMC device, MTFC8GAKAJCN (from Micron) on the board. The eMMC memory can support x1, x4 and x8 data width and data rate of HS400 mode. The eSDHC2 controller and the on-board embedded eMMC memory operate at 1.8 V IO.

2.17 Mikro-click modules

The LS1028ARDB board provides two mikroBUS™ connectors, mikroBUS1 (J29 and J30) and mikroBUS2 (J31 and J32). These mikroBUS connectors support different types of mikro-click modules that can be accessed through SPI3, UART2, PWM, or I2C interface. Since SPI and UART buses to the mikroBUS sockets are shared, modules using the same communication interface (both SPI or both UART) cannot be used. However, a combination can be supported. For example, a UART based module and

an SPI based module can be supported simultaneously on mikroBUS 1 and 2 sockets, or vice-versa. I2C on both the modules can be accessed instantaneously from the I2C mux. For more information on I2C mux selection, refer I2C interface on page 34.

The following figure shows the mikroBUS architecture.

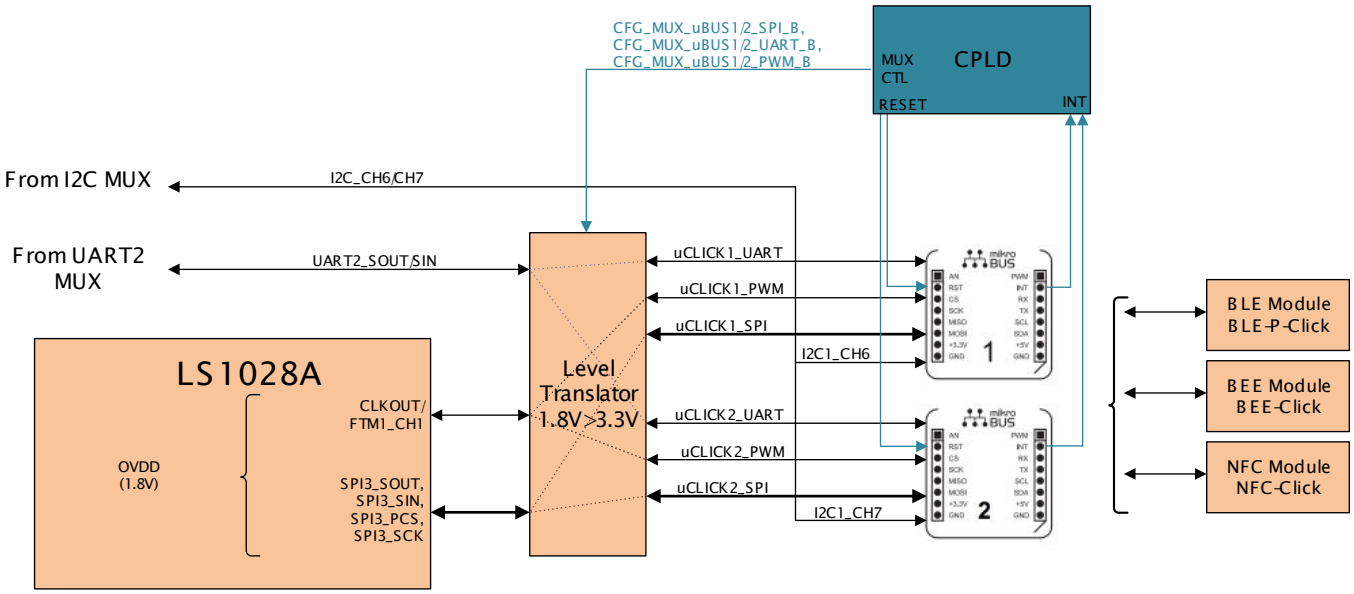


Figure 21. mikroBUS architecture

The following table describes some of the mikro-click modules (boards) that can be used on the mikroBUS sockets.

Table 20. Mikro-click modules

Module	Communication interface	Part number	Description
BLE module BLE P Click	SPI	MIKROE-1597	Module supports Bluetooth 4.0 on the board. This module communicates with LS1028ARDB through SPI (CS, SCK, MISO, MOSI), INT (RDY) and AN (ACT) lines on mikroBUS socket.
BEE module BEE click	SPI	MIKROE-987	Module features a 2.4 GHz IEEE 802.15.4 radio transceiver module to support wireless communication applications.
NFC module NFC click	I2C, GPIO	MIKROE-2395	It is a near field communications (NFC) controller from NXP.

The LS1028A processor supports serial peripheral interface (SPI3) controller. The SPI3 pins are used to access the two mikroBUS sockets connected on the board. However, only one mikroBUS connector can be used at a time as SPI3 supports only one chip select.

The UART2 interface can be used to communicate either with mikro-click modules or with RS232 compliant devices using the LTC2804-1 transceiver. The selection is done through a mux which is controlled through the CFG_MUX_UART2_SEL0 signal by CPLD.

Since the mikro-click modules operate at 3.3 V power supply, the CPLD enables the level translator, SN74AVC2T245 (from Texas) to translate 1.8 V to 3.3 V voltage for the selected module.

The following table describes configuration for accessing mikro-click modules on mikroBUS1 or mikroBUS2 through SPI3/UART2/PWM interface.

Table 21. SPI3/UART2/PWM selection on mikro-click modules

CPLD signals	Registers	Configuration
CFG_MUX_uBUS1_SPI_B CFG_MUX_uBUS2_SPI_B	BRDCFG3[6]	0: SPI3 routed to mikroBUS1 module. 1: SPI3 routed to mikroBUS2 module.
CFG_MUX_UART2_SEL0 CFG_MUX_uBUS1_UART_B CFG_MUX_uBUS2_UART_B	BRDCFG3[5:4]	0X: UART2 routed to RS232 transceiver and DB9 connector P1A (default). 10: UART2 routed to mikroBUS1 module. 11: UART2 routed to mikroBUS2 module.
CFG_MUX_uBUS1_PWM_B CFG_MUX_uBUS2_PWM_B	BRDCFG3[7]	0: PWM (FTM1_CH1) routed to mikroBUS1 module. 1: PWM (FTM1_CH1) routed to mikroBUS2 module.

Also, the mikro-click modules on mikroBUS1 or mikroBUS2 can be accessed directly through I2C1 channel 6 or channel 7, respectively.

2.18 GPIOs

The GPIOs used on the LS1028ARDB are GPIO1_DAT[24], GPIO1_DAT[25], and GPIO3_DAT[2:4]. Apart from these GPIOs, all signals (UART, SPI, PWM) coming on connectors (mikro-click module) can also act as GPIO signals.

GPIO1_DAT24 controls output voltage of the VDD and TA_BB_VDD regulators. It is used to change the VDD/TA_BB_VDD value from 1.0 V to 0.9 V as described in the following table.

Table 22. GPIO1_DAT[24] setting

GPIO	Setting	VDD/TA_BB_VDD
GPIO1_DAT24	High (default)	1.0 V
GPIO1_DAT24	Low	0.9 V

GPIO3_DAT[2:4] connects to the CPLD and the CPLD has provision to control/monitor the GPIO through registers. For more information, see BRDCFG3 register detail in Qixis Programming Model on page 58.

The CPLD combines all the interrupts received from the board devices and sends out the interrupt signals to the LS1028A processor using GPIO1_DAT25.

2.19 Interrupt handling

All interrupts coming from all devices on LS1028ARDB are communicated to the LS1028A processor through GPIO1_DAT25. The following are the interrupt assignments:

Table 23. Interrupt assignments

GPIO	Interrupt signal	Description
GPIO1_DAT25	IRQ_RTC_B	RTC interrupt
	IRQ_QSGMII_B	5 Gbit QSGMII PHY interrupt
	uBUS1_INT	mikroBUS1 module interrupt
	uBUS2_INT	mikroBUS2 module interrupt
	IRQ_ETH_B	1 Gbit SGMII PHY interrupt

2.20 Temperature measurement

The LS1028A has a thermal monitoring diode which can be measured by NXP SA56004ED thermal monitor device (U52). Software can perform direct die temperature readings with an accuracy of ±1°C. See the I2C section for addressing information.

In addition to monitoring, the SA56004ED monitor can also trigger alarms upon detecting thermal problems. The SA56004ED THERM_WARN and THERM_ALERT signals are connected to the system controller (CPLD), as well as to status LEDs. The CPLD uses these signals to power down the system, to protect the processor from over-temperature damage.

Temperature measurement requires no programming; however, to change the default thermal limit, which is 70°C for high temperature and 0°C for low temperature, issue the I2C writes as described in the following table.

Table 24. Thermal monitor configuration

I2C write	Description
0x77 0x0B 0x0B	Program primary I2C bus multiplexer (PCA9848PWJ) to get access to I2C1_CH3 (I2C sub-channel for SA56004ED)
0x4C 0xOD <TLIMITH>	Program the high set point of SA56004ED remote measurement (the processor). <TLIMITH> can be any user defined value in 2's complement form. For example, for +85°C, TLIMITH should be 0x55.
0x4C 0x0E <TLIMITL>	Program the low set point of SA56004ED remote measurement (the processor). <TLIMITL> can be any user defined value in 2's complement form. For example, -25°C can be programmed as 0xE7.

NOTE

The SW_BYPASS_B switch (SW3[3]) disables thermal monitoring. This may be necessary if operating the board without a processor installed, as an open thermal diode connection measures as 127 °C.

2.21 System controller

The LS1028ARDB system controller (or “CPLD” for short) controls the operation of the system, including:

- Reset assertion to processor and devices
- Processor and system configuration
- Interrupt management
- System alert monitoring and status display
- Remapping of system boot devices

- Handling of board control and status registers

The following figures show the system controller architectural details.

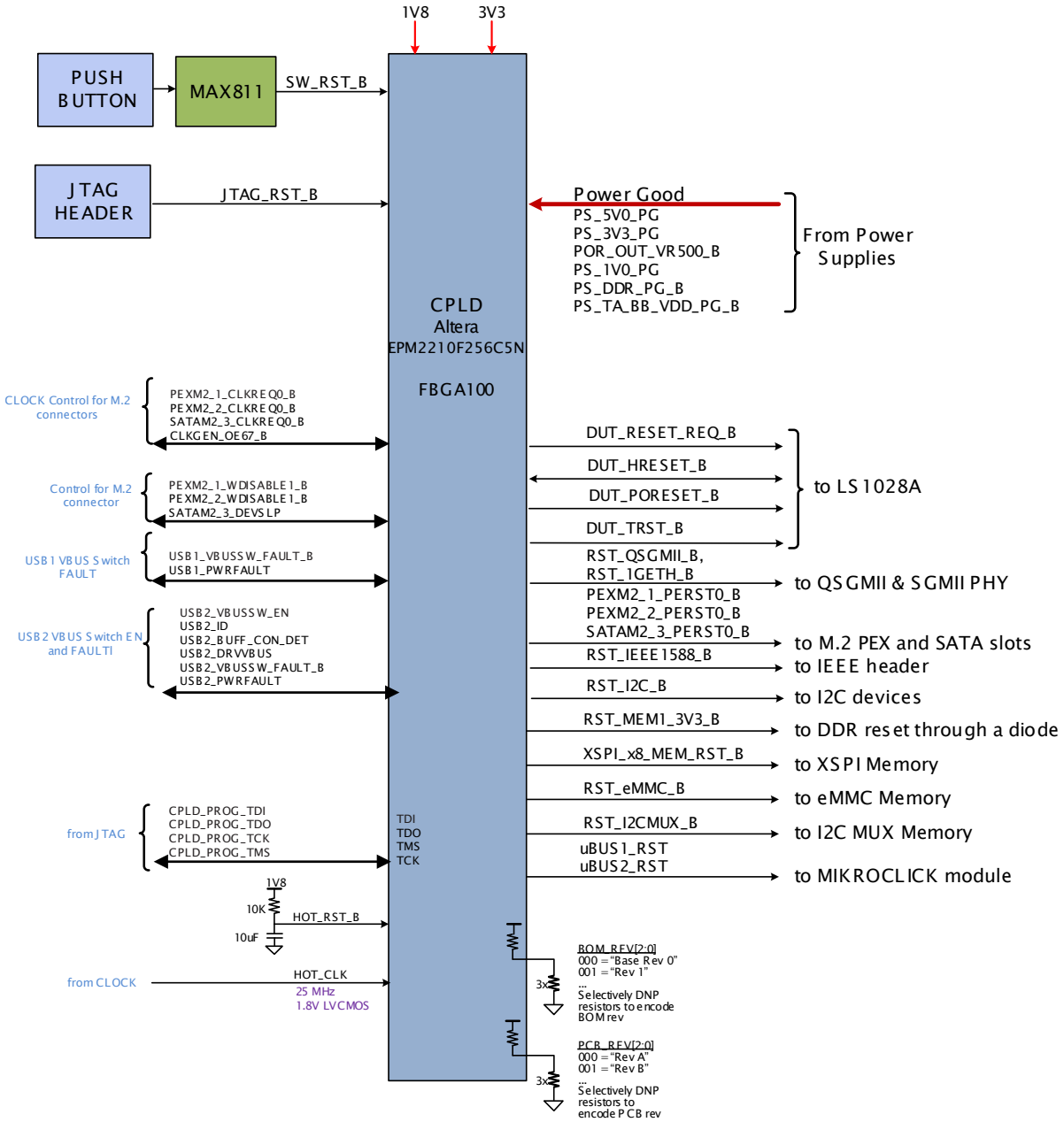


Figure 22. System controller architecture

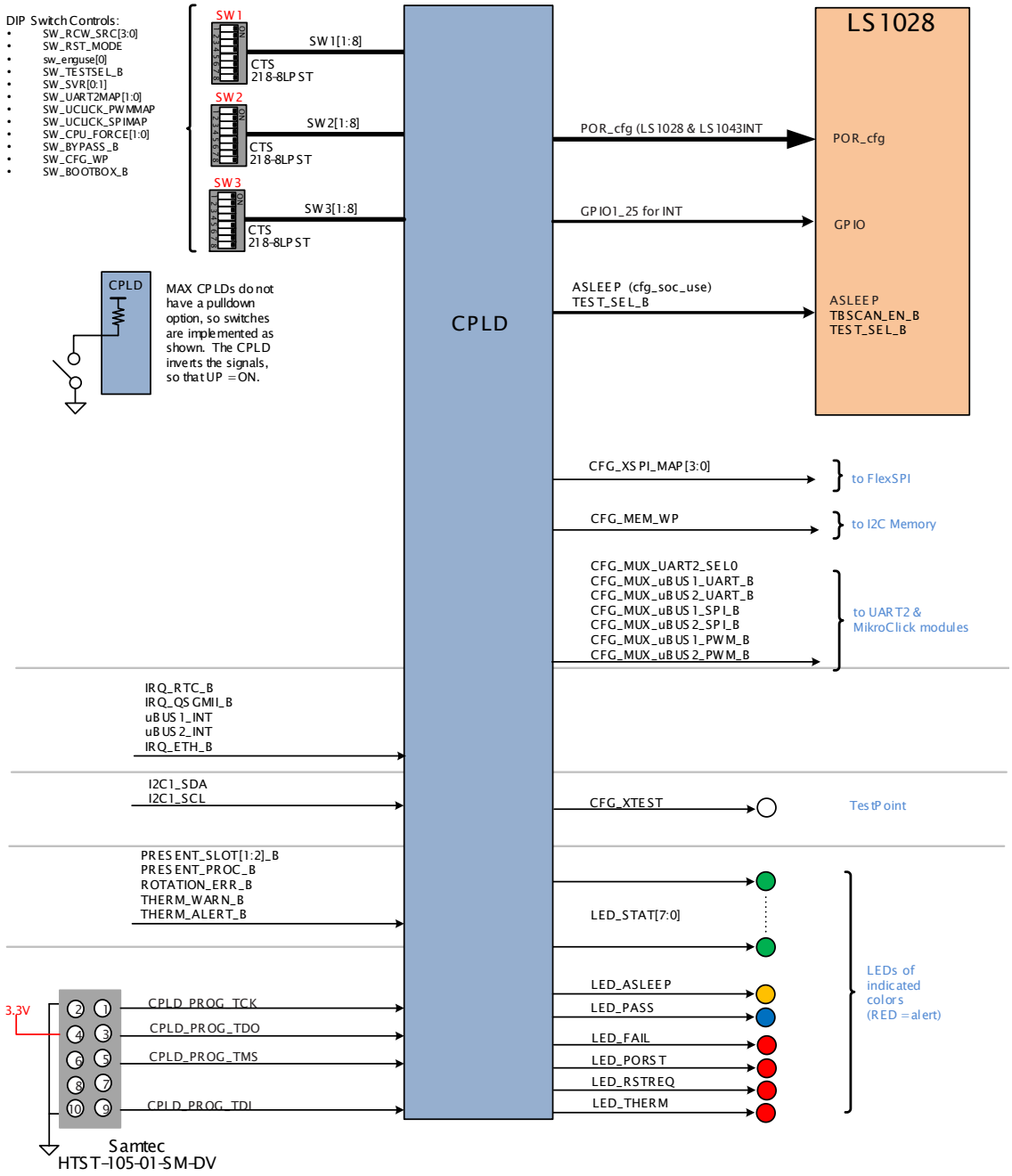


Figure 23. System controller architecture (continued)

The system controller is implemented in a 100-ball FBGA Altera CPLD, EPM2210F256C5N.

The system controller is powered using the 3.3 V and 1.8 V regulators. The CPLD controls the reset of the board peripherals including the LS10128A processor. However, the CPLD does not control power sequencing.

2.21.1 System configuration

The system controller uses switches to configure the target system into various modes. Switches are sampled and stored in BRDCFG and DUTCFG registers. BRDCFG registers are always active, and software may change them to result in immediate changes to the system configuration. DUTCFG registers are used to control processor configuration pins that are only sampled

during PORESET_B, such as RCW_SRC in DUTCFG0. Changes to DUTCFG registers only take effect on the next reset or reconfiguration event. The following figure shows the configuration hardware arrangement.

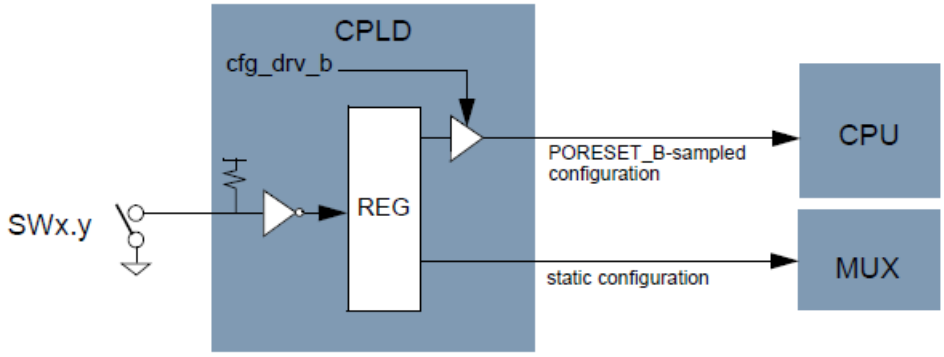


Figure 24. Configuration sampling

Note that switches cause a short to ground when closed. To make it easier to set and read switches, values are inverted in the CPLD, so that when a switch is on, the value used is 1.

All switches can be read from software to easily determine the system configuration for reporting purposes (see the "Core Management Space Registers" section of the "CPLD Programming Model" chapter).

The table below describes the LS1028A configuration signals.

Table 25. Processor configuration settings

Configuration signal	LS1028A primary signal	DIP switch	CPLD register	Description
CFG_RCW_SRC0	UART2_SOUT	SW1[1:4]	DUTCFG0[3:0]	Specifies RCW fetch location
CFG_RCW_SRC1	UART1_SOUT			
CFG_RCW_SRC2	ASLEEP			
CFG_RCW_SRC3	CLK_OUT			
TEST_SEL_B[1]	TEST_SEL	SW3[1]	DUTCFG2[0]	Silicon variations
CFG_SVR[0:1]	XSPI_CS0_B XSPI0_CS1_B	-	DUTCFG2[2:1]	-
CFG_ENG_USE0	XSPI_SCK	-	DUTCFG11[7]	Configures processor to use differential SYSCLK.

1. TEST_SEL_B is a static signal (constantly driven), unlike most other processor configuration signals.

All other configuration signals are static and unrelated to the processor. The following table summarizes these configuration signals.

Table 26. Non-processor configuration settings

Configuration signal	DIP switch	CPLD register	Description
CFG_XSPI_MAP	SW1[8]	BRDCFG0[6]	Controls how XSPI_A chip-select 0 is connected to devices/peripherals.
CFG_MEM_WP	SW3[4]	CTL[3]	Allows/prevents write to SYSTEM ID, UEFI flash, and DDR4 SPD.

Table continues on the next page...

Table 26. Non-processor configuration settings (continued)

Configuration signal	DIP switch	CPLD register	Description
CFG_MUX_UART2_SEL0, CFG_MUX_uBUS1_UART_B , CFG_MUX_uBUS2_UART_B	SW2[6:5]	BRDCFG3[5:4]	Controls UART2 routing to RS232 transceiver (DB9 connector P1A), mikroBUS1, or mikroBUS2 module.
CFG_MUX_uBUS1_SPI_B, CFG_MUX_uBUS2_SPI_B	SW2[8]	BRDCFG3[6]	Controls routing of SPI3 to mikroBUS1 or mikroBUS2 module
CFG_MUX_uBUS1_PWM_B , CFG_MUX_uBUS2_PWM_B	SW2[7]	BRDCFG3[7]	Controls routing of PWM to mikroBUS1 or mikroBUS2 module

DIP switches that are not listed in the above tables do not directly control board signals, rather they alter the behavior of the system controller. See Switch configuration on page 51 for complete details about DIP switches.

2.21.2 Reset sequencing

The system controller manages the reset sequencing during the system startup. After successful power sequencing (all "power good" are reported from power supplies), reset sequencer asserts the PORESET_B signal.

The reset sequencing (including device configuration) is described in the following table.

Table 27. Reset sequence

Controller	Step	Action	Description
Reset sequencer	1	Assert all resets.	LS1028A PORESET_B is asserted if not already asserted. Device resets are asserted: • RST_QSGMII_B • RST_1GETH_B • PEXM2_1_PERST0_B • PEXM2_2_PERST0_B • SATAM2_3_PERST0_B • RST_IEEE1588_B • RST_I2C_B • RST_MEM1_3V3_B • XSPI_x8_MEM_RST_B • RST_eMMC_B • RST_I2CMUX_B • uBUS1_RST • uBUS2_RST The LS1028A processor asserts ASLEEP and HRESET_B in response. ASLEEP is monitored with an LED, otherwise the signals are ignored.

Table continues on the next page...

Table 27. Reset sequence (continued)

Controller	Step	Action	Description
	2	Wait for reset clear.	Wait for reset assertion to be released. The reset sequencer will stall as long as any of the following reset inputs is asserted: • CWJTAG_RST_B • SW_RST_B
	3	Sample switches.	Internal registers are reset to default values. Registers that default to switch values are set now.
	4	Drive configuration values.	Reset-sampled configuration signals are driven: • CFG_RCW_SRC[3:0] • CFG_SVR[0:1] • CFG_ENG_USE[0] Static (constant) configuration signals are driven: • CFG_XSPI_MAP[0:3] • CFG_MUX_I2C2 • CFG_MUX_I2C3 • CFG_MEM_WP • CFG_MUX_UART2_SEL0 • CFG_MUX_uBUS1_UART_B • CFG_MUX_uBUS2_UART_B • CFG_MUX_uBUS1_SPI_B • CFG_MUX_uBUS2_SPI_B • CFG_MUX_uBUS1_PWM_B • CFG_MUX_uBUS2_PWM_B
	5	Release resets.	Release all resets shown in reset sequencer step 1. The processor samples reset pins at this time.
	6	Tristate reset-sampled pins.	A fixed time period after step 5: Tristate configuration signals drive outputs. This ensures proper configuration hold time. The CPLD is no longer involved in reset activity.

Table continues on the next page...

Table 27. Reset sequence (continued)

Controller	Step	Action	Description
	7	Processor reset.	The LS1028A processor begins loading RCW data from the specified RCW source location. When RCW loading is complete, the LS1028A processor de-asserts HRESET_B and ASLEEP. If RCW data is correct, then the system starts running the code. If there is an error, then RESET_REQ_B is asserted and the system halts.
	8	Reset sequence complete.	The CPLD has finished reset management. The reset sequencer watches for reset switch events and will restart at reset sequencer step 1 if any are detected.

Chapter 3
Board Configuration and Debug Support

This chapter contains the following sections:

3.1 Switch configuration

The LS1028ARDB provides dual inline package (DIP) switches to allow easy configuration of the system for the most popular board options. The CPLD stores the DIP switch values in the BRDCFG and DUTCFG registers and that allows the software (either local or remote) to reconfigure the system as required.

For each DIP switch:

- If the switch is up (on), the value is 1
- If the switch is down (off), the value is 0

Table 28. Switch settings

Switch	Supported function	Description
SW2[1:4]	RCW fetch location CFG_RCW_SRC[3:0]	SW_RCW_SRC[3:0] • 0000: Hard-coded RCW • 1000: SDHC1: SD card • 1001: SDHC2: eMMC • 1010: UEFI/I2C Boot EEPROM • 1101: XSPI serial NAND, 4K pages • 1111: XSPI serial NOR, 24-bit address (default value) **NOTE** The RCW source settings are mapped to 9-bit values when an LS1043A processor is installed.
SW2[5]	Reset mode RESET_REQ_B	SW_RST_MODE • 0: Ignore RESET_REQ_B • 1: Trigger system reset on RESET_REQ_B (default value)

Table 28. Switch settings (continued)

<table>
<tr><th>Switch</th><th>Supported function</th><th>Description</th></tr>
<tr><td>SW2[6:8]</td><td>XSPI_A device mapping
CFG_XSPI_MAP</td><td>SW_XSPIMAP[2:0]: Controls how XSPI_A chip-selects are connected to devices/peripherals.
Table 29.
<table>
<tr><th>Bit value</th><th>XSPI_A_CS0</th><th>XSPI_A_CS1</th><th>Description</th></tr>
<tr><td>000</td><td>sNOR</td><td>sNAND</td><td>Normal NOR</td></tr>
<tr><td>001</td><td>sNAND</td><td>sNOR</td><td>Normal NAND</td></tr>
<tr><td>010</td><td>Emulator</td><td>sNOR</td><td>Programmable NOR</td></tr>
<tr><td>011</td><td>Emulator</td><td>sNAND</td><td>Programmable NAND</td></tr>
<tr><td>100</td><td>sNOR</td><td>Emulator</td><td>Boot from sNOR and program emulator</td></tr>
</table></td></tr>
<tr><td>SW3[1]</td><td>CFG_ENG_USE0</td><td>SW_enguse[0]
• 0: Reserved
• 1: Use differential clock (default value)</td></tr>
<tr><td>SW3[2:4]</td><td>Device type selection
TEST_SEL_B, CFG_SVR[0:1]</td><td>SW_TESTSEL_B + SW_SVR[0:1]
• 011: LS1018AN/E
• 111: LS1028AN/E (default value)</td></tr>
<tr><td>SW3[5:6]</td><td>UART2 configuration
CFG_MUX_UART2_SEL0</td><td>SW_UART2MAP[1:0]
• 0x: UART2 on DB9 connector (default value)
• 10: UART2 on mikro-click module 1
• 11: UART2 on mikro-click module 2</td></tr>
<tr><td>SW3[7]</td><td>PWM configuration
CFG_MUX_PWM2uBUS1_B
CFG_MUX_PWM2uBUS2_B</td><td>SW_UCLICK_PWMMAP
• 0: PWM signal routed to mikro-click module 1 (default value)
• 1: PWM signal routed to mikro-click module 2</td></tr>
<tr><td>SW3[8]</td><td>SPI configuration
CFG_MUX_SPI2uBUS1_B
CFG_MUX_SPI2uBUS2_B</td><td>SW_UCLICK_SPIMAP
• 0: SPI signal routed to mikro-click module 1 (default value)
• 1: SPI signal routed to mikro-click module 2</td></tr>
</table>

Table continues on the next page...

Table 28. Switch settings (continued)

Switch	Supported function	Description
SW5[1:2]	SoC use	SW_CPU_FORCE[1:0] • 0x: Normal mode (default value) • 10: Force LS1043 interposer • 11: Force LS1028 **NOTE** Do not change the default setting of this switch.
SW5[3]	Bypass mode	SW_BYPASS_B • 0: Disable thermal monitors and other alarms • 1: Normal operation (default value)
SW5[4]	Write protect	SW_CFG_WP • 0: Allow write to SYSID and UEFI flash • 1: Write-protect SYSID and UEFI flash (default value)
SW5[5]	Boot Box mode	SW_BOOTBOX_B • 0: Enable boot-box mode • 1: Normal operating mode (default mode)
SW5[6:7]	Unused	Reserved Default value is 0.
SW5[8]	IEEE/SAI	• 0: Signals routed to IEEE1588 connector • 1: Signals routed to TX-only SAI transceiver

The table below summarizes the default switch settings of the LS1028ARDB DIP switches.

Table 30. Default switch settings

DIP switch	Value
SW2	1111_1000
SW3	1111_0X00
SW5	0X11_1000

3.2 LEDs

The LS1028ARDB has numerous onboard light-emitting diodes (LEDs), which can be used to monitor various system functions, such as power-on, reset, board faults, and so on. The information collected from LEDs can be used for debugging purposes.

The following table lists all the LEDs available on the top-side of the LS1028ARDB board.

Table 31. LEDs available on top-side of LS1028ARDB

Reference designator	LED color	LED name	Description (when LED is ON)
D2	Green	12V_IN	Indicates 12 V input power supply is operating.
D14	Green	M.2 LED1	The M.2 card on J16 is powered properly and its transmitter is ready to transmit.
D15	Green	M.2 LED1	The M.2 card on J18 is powered properly and its transmitter is ready to transmit.
D16	Green	M.2 DAS	The SSD M.2 card on J20 is powered properly and drive is active. DAS stands for Drive Activity Signal.
D19	Green	USB2 5V	5 V power is supplied to the USB 2 connector for external devices
D17	Green	USB1 5V	5 V power is supplied to the USB 1 connector for external devices
D25	Yellow	ASLEEP	The processor has not exited Sleep mode, which generally indicates: • Improper RCW source selection • Boot memory does not contain a valid RCW/PBL • PLL multipliers in the RCW data are not compatible with the fixed SYSCLK, DDRCLK, or SDCLK values
D26	Red	FAIL	Indicates one of the following has happened: • A thermal over-temperature fault has occurred • One or more power supplies have not started • Software has set the CTL.FAIL bit to indicate a software fault
D28	Red	RST_REQ	The processor is asserting RESET_REQ_B. This is typically due to the reasons described for the ASLEEP LED.
D29	Red	THERM	Thermal monitors have detected a thermal fault and have shut down the system. **NOTE** Unless reprogrammed by user software, the thermal trip point is 85 °C. .
D35	Green	M3	General status. See Multi-status LEDs for details.
D36	Green	M2	
D37	Green	M1	

Table continues on the next page...

Table 31. LEDs available on top-side of LS1028ARDB (continued)

Reference designator	LED color	LED name	Description (when LED is ON)
D38	Green	M0	
D39	Green	5.0V	5V0 power supply is operating correctly
D40	Green	3.3V	3V3 power supply is operating correctly
D41	Green	1.0V	1V0 power supply is operating correctly
D42	Green	PS_DDR	DDR power supply is operating correctly
D43	Green	VR500	VR500 output supplies (2V5/1V8/1V35) are operating correctly
D44	Green	TA_BB_VDD	Low power security monitor supply is operating correctly
D45	Green	SocInSocket	Indicates that the LS1028A processor is in socket

The following table lists all the LEDs available on the front-panel of the LS1028ARDB board chassis.

Table 32. LEDs available on front-panel of board chassis

Reference designator	LED color	LED name	Description (when LED is ON)
D27	Red	RESET	RESET is 'ON' when reset to DUT is asserted due to: • Power cycle • Debugger reset • Reset from SoC (RESET_REQ_B if enabled in CPLD) • RESET switch
	Green	SYSTEM READY	SYSTEM READY is 'On', when power-on reset sequencing is done SYSTEM READY is 'Off' for: • Power sequencing fault • Any alarm, such as over-temperature • Explicit software enable (reg CTL.FAIL) • Other fault signals
SW1	Green/Yellow	POWER	• OFF: off • YELLOW: power cycle in progress/fault • GREEN: System ready
D47	Green/Yellow	SWP0	• GREEN : Link is active • YELLOW: Link is 1000BaseT
D48	Green/Yellow	SWP1	

Table continues on the next page...

Table 32. LEDs available on front-panel of board chassis (continued)

Reference designator	LED color	LED name	Description (when LED is ON)
D49	Green/Yellow	SWP2	Available on the chassis front panel.
D50	Green/Yellow	SWP3	
D51	Green/Yellow	MAC1	

3.2.1 Multi-status LEDs

The board includes four multi-status LEDs that indicate hardware activity; however, software can override these LEDs to use them for debugging purposes. The table below describes the functions of the multi-status LED arrays.

Table 33. LED array functions

LED	Reset sequencer state	Normal (after 2 seconds)	User-defined (if register CTL[1] (LED) = 1)
M3	(see Table 34. Reset sequencer state on page 56)	Not applicable	M[3:0] reflect contents of the LED register
M2		Not applicable	
M1		Not applicable	
M0		Heartbeat: Clock monitor	

Table 34. Reset sequencer state

State	LED: M[3:0]	Description
IDLE	0000 = 0x0	Waiting for initial reset events
SAMPLE	0001 = 0x1	Sample configuration switches
RECONFIG	0010 = 0x2	Update configuration from registers
Reserved	0011 = 0x3	Reserved
Reserved	0100 = 0x4	Reserved
CLOCK_LOCK	0101 = 0x5	Wait for clock PLLs to stabilize
RELEASE_ALL	0110 = 0x6	Release all hardware resets except DUT
RELEASE_DUT	0111 = 0x7	Release DUT from reset
STABLE	1000 = 0x8	Reset sequencing complete. Wait for reset events.
RESET_REQ	1001 = 0x9	Start reset due to (cause): DUT HRESET_REQ_B
PORESET	1010 = 0xA	Start reset due to (cause): JTAG HRESET_B (PORESET_B)
RST_WATCH	1011 = 0xB	Start reset due to (cause): Watchdog timeout

Table continues on the next page...

Table 34. Reset sequencer state (continued)

State	LED: M[3:0]	Description
RST_BY_REG	1100 = 0xC	Start reset due to (cause): Register bit set
RST_BY_SW	1101 = 0xD	Start reset due to (cause): Pushbutton switch
RECONFIG	1110 = 0xE	Start reset due to (cause): Reconfig request
POST_RST	1111 = 0xF	Recover from requester reset

Chapter 4
Qixis Programming Model

This chapter describes the contents of the register block (the BCSR - Board Control / Status Registers). These are contained within the system controller FPGA or CPLD, and may be used to control and monitor the target system. These registers are accessible over one or more system-specific interfaces, typically I2C, JTAG or an embedded processor. Refer to the system reference manual for these connection details. In all cases, each interface will use the 12-bit base address supplied in the definitions below.

This table shows the register memory map for Qixis.

Table 35. Qixis Register Memory Map

Offset	Register	Width (In bits)	Access	Reset value
000h	Identification (ID)	8	RO	01000111b
001h	Board Version (VER)	8	RO	00010001b
002h	Qixis Version (QVER)	8	RO	00000001b
003h	Programming Model (MODEL)	8	RO	01000000b
004h	Minor Revision (MINOR)	8	RW	00000101b
005h	General Control (CTL)	8	RW	00000000b
006h	Auxiliary (AUX)	8	RW	00000000b
009h	System Status (STAT_SYS)	8	RO	00000000b
00Ah	Alarm (ALARM)	8	RO	00000000b
00Bh	Presence Detect 1 (STAT_PRES1)	8	RO	0110xxxxb
00Ch	Presence Detect 2 (STAT_PRES2)	8	RO	xxxx1111b
00Eh	LED Control (LED)	8	RW	00000000b
010h	Reconfiguration Control (RCFG)	8	RW	0001x00xb
01Dh	USB Control (USB_STAT)	8	RW	00000001b
01Eh	USB Control (USB_CTL)	8	RW	00xx0000b
01Fh	Watchdog (WATCH)	8	RW	xxxxxxxb
021h	Power Control 2 (PWR_CTL2)	8	RW	00000000b
024h	Power Status 0 (PWR_MSTAT)	8	RO	110010xxb

Table continues on the next page...

Table 35. Qixis Register Memory Map (continued)

Offset	Register	Width (In bits)	Access	Reset value
025h	Power Status 1 (PWR_STAT1)	8	RO	1xx11111b
030h	Clock Speed 1 (CLK_SPD1)	8	RO	0000xxxxb
033h	Clock ID/Status (CLK_ID)	8	RO	00000000b
040h	Reset Control (RST_CTL)	8	RW	00xxx000b
041h	Reset Status (RST_STAT)	8	RO	00000000b
042h	Reset Event Trace (RST_REASON)	8	RO	xxxx0000b
043h	Reset Force 1 (RST_FORCE1)	8	RW	00000000b
044h	Reset Force 2 (RST_FORCE2)	8	RW	00000000b
045h	Reset Force 3 (RST_FORCE3)	8	RW	00000000b
04Bh	Reset Mask 1 (RST_MASK1)	8	RW	00000000b
04Ch	Reset Mask 2 (RST_MASK2)	8	RW	00000000b
04Dh	Reset Mask 2 (RST_MASK3)	8	RW	00000000b
050h	Board Configuration 0 (BRDCFG0)	8	RW	xxx00000b
051h	Board Configuration 1 (BRDCFG1)	8	RO	0000xxxxb
052h	Board Configuration 2 (BRDCFG2)	8	RO	00000000b
053h	Board Configuration 3 (BRDCFG3)	8	RO	xxxx0100b
054h	Board Configuration 4 (BRDCFG4)	8	RW	00001000b
055h	Board Configuration 5 (BRDCFG5)	8	RW	xxx00000b
056h	Board Configuration 6 (BRDCFG6)	8	RW	xxx00000b
060h	DUT Configuration 0 (DUTCFG0)	8	RW	xxxxxxxxb
061h	DUT Configuration 1 (DUTCFG1)	8	RW	0xxxxxxxb
062h	DUT Configuration 2 (DUTCFG2)	8	RW	xxxxxxx1b
06Bh	DUT Configuration 11 (DUTCFG11)	8	RW	xxxxxxxxb
080h	GPIO I/O (GPIO_IO)	8	RW	xxx111xxb
084h	GPIO Direction (GPIO_DIR)	8	RW	00000000b

Table continues on the next page...

Table 35. Qixis Register Memory Map (continued)

Offset	Register	Width (In bits)	Access	Reset value
090h	Interrupt Status 0 (IRQSTAT0)	8	RO	11xx1111b
091h	Interrupt Status 1 (IRQSTAT1)	8	RO	xxxxx1xxb
092h	Interrupt Status 2 (IRQSTAT2)	8	RO	xxxxxxxb
09Dh	Interrupt Drive 5 (IRQDRV5)	8	RW	00000000b
0D8h	Core Management Address (CMSA)	8	RW	00000000b
0D9h	Core Management Data (CMSD)	8	RW	00000000b

4.1 Register Conventions

An undefined register address does not have any defined register value. Reads and writes to such addresses should be avoided. If you attempt to read such addresses, undefined data is returned. Undefined register addresses may be defined in the future.

For registers which do not define all bits, reserved bits behave as follows:

Reserved Bits

Register	Recommended Actions
DUTCFG	Read as 1. Write ones to unused bits.
others	Read as 0. Write zeroes to unused bits.

Future definitions of reserved bits will maintain backward compatibility with the above rules.

4.2 Resets

The reset values for registers are defined as follows:

Reset Actions

Term	Reset Action
NONE	Register cannot be reset. Applies to read-only registers.
ARST	Auxiliary Reset: registers are reset when the system powers up with standby power, and is never altered by hardware again. Software writes are preserved.
CRST	Control Reset: registers are not reset except under exceptional situations, such as power cycles or watchdog timeout.

Table continues on the next page...

Table continued from the previous page...

Term	Reset Action
RRST	Reconfig Reset: configuration registers are reset as with CRST unless a reconfiguration reset has been requested.
GRST	General Reset: always reset, for any reason.

Generally, a register is wholly affected by only one reset source, however there are exceptions and these are shown with separate reset lines for each reset source.

4.3 Identification Registers

The ID block of registers contain values which identify the board, including major revisions to the board and/or system controller FPGA or CPLD.

4.4 Identification (ID)

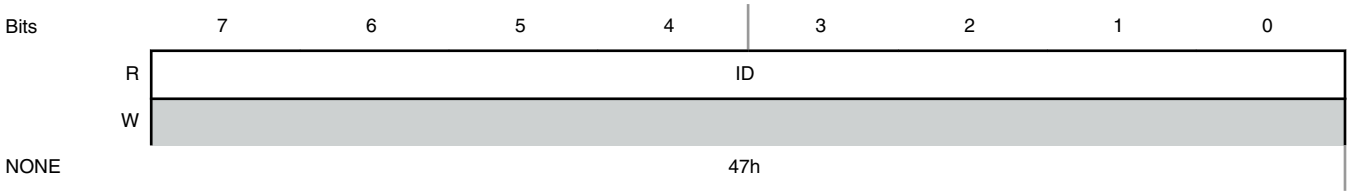
Address

Register	Offset
ID	000h

Function

The ID register contains a unique classification number. This ID number is used by system software to identify board types. The ID number remains same for all board revisions.

Diagram



Fields

Field	Function
7-0 ID	The board-specific identifier for the system. 47h= LS1028ARDB

4.5 Board Version (VER)

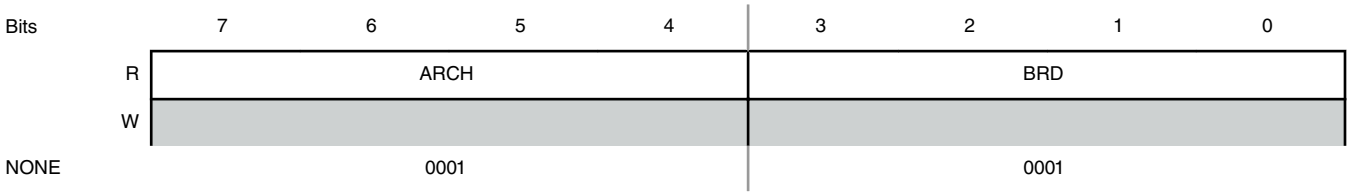
Address

Register	Offset
VER	001h

Function

The VER register records version information for the PCB board as well the board architecture. The PCB board version can change without impacting the board architecture version, and vice versa.

Diagram



Fields

Field	Function
7-4 ARCH	Board architecture version: 1= V1 2= V2 (etc.)
3-0 BRD	PCB board version: 1= Rev A (or pre-release) 2= Rev B (etc.)

The ARCH field is used by QIXIS and software to handle architecture changes. The ARCH field allows the use of a common QIXIS image across multiple board revisions, if supported by the device.

The BRD field lets end users determine the version of the board. Software can use this field to print board version identification. For example:

```
printf("Board Version: %c", (get_pixis( VER ) & 0Fh) + 'A' - 1 );
```

4.6 Qixis Version (QVER)

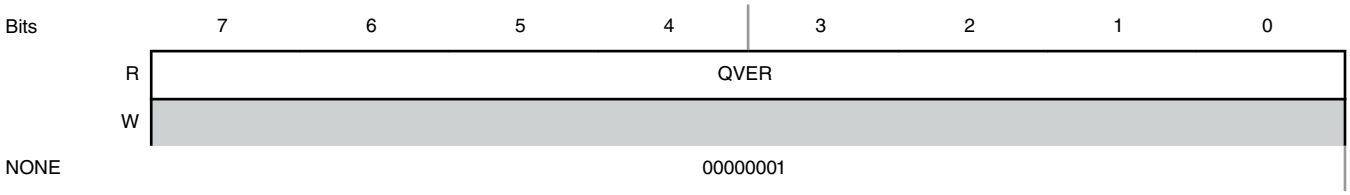
Address

Register	Offset
QVER	002h

Function

The QVER register contains the major version information of the Qixis system controller. Minor revision information may be found in the MINOR register.

Diagram



Fields

Field	Function
7-0 QVER	Qixis version as a decimal value: 1= Version 1 2= Version 2

4.7 Programming Model (MODEL)

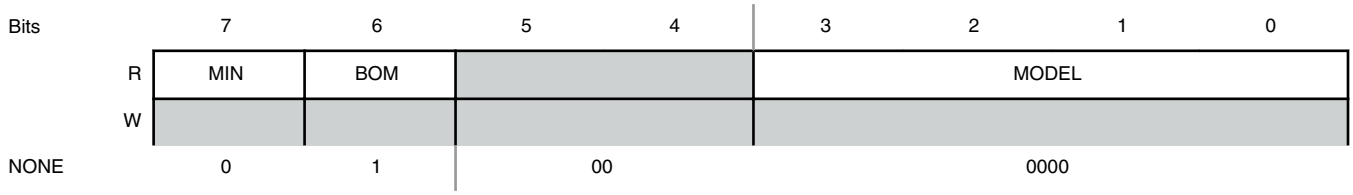
Address

Register	Offset
MODEL	003h

Function

The MODEL register contains information about the software programming model version and PCB Bill Of Materials (BOM) information.

Diagram



Fields

Field	Function
7 MIN	Programming Model Type: 0= Normal Qixis register set. 1= Subset Qixis register set (QixMin).
6 BOM	Model Register Encoding: 0= Lower 4 bits contain programming model revision (MODEL). 1= Lower 4 bits contain PCB BOM (Bill of Materials) version.
5-4 -	Reserved.
3-0 MODEL	Model (BOM Version) Information: 0000= No revision: PCB version is A, B, etc. 0001= Revision 1 : PCB version is A1, B1, etc. 0010= Revision 2 : PCB version is A2, B2, etc. and so forth. Note that this field should be appended to the VER.PCB information only if non-zero.

4.8 Minor Revision (MINOR)

Address

Register	Offset
MINOR	004h

Function

The MINOR (or MINTAG) register can be used to obtain CPLD build information from software. The register returns a subset of the Qixis QTAG facility but more than the limited MINOR facility on other RDBs.

Writes to MINOR select various pieces of information for subsequent read. On reset, the 'minor revision' field is returned, for backward-compatiblity.

Concatenated with the QVER register, it forms the full revision information for the CPLD device. This is typically reported as:

```
qver = get_pixis( QVER );

minor = get_pixis( MINOR );

printf("FPGA: V%d", qver );

if (minor != 0) {

  printf(".%d", minor );

}
```

Note: setting the MINOR/MINTAG register to 5h before reading is optional, as on every reset 05h is the default.

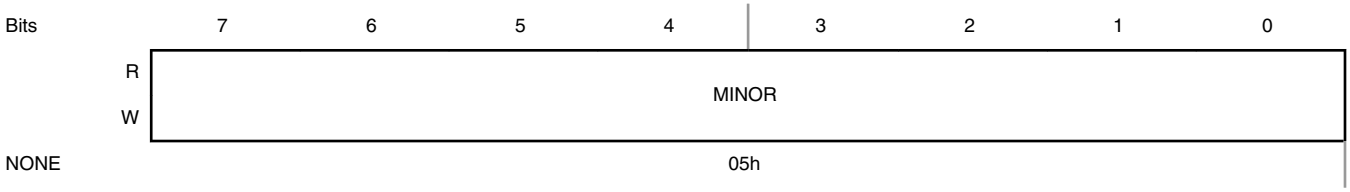
Note: for harmonization with QDS-supporting code (e.g. uboot), if MINOR is zero, do not print it.

Other information can be obtained by writing the corresponding address and reading the register. Reserved fields are found only in QDS QTAG but are present for compatibility. Contents are as follows:

MINTAG Definition

Address Range	Name	Definition
0x00-0x03	TAG	not implemented.
0x05-0x06	MINOR	Minor build version: u16 value in little-endian order.
0x08-0x0B	DATE	Date/time stamp: u32 Unix GMT time value in big-endian order.
0x0C	RELEASE	Released flag: 0=unreleased, non-zero=released.
0x10-0x2F	NAME	not implemented.
0x30-7F	reserved	reserved

Diagram



Fields

Field	Function
7-0 MINOR	Read: Data to read from MINOR/MINTAG. Write: Address of data to read.

4.9 Control and Status Registers

This block of registers control the operation of Qixis itself (or other operations which do not constitute controlling the board or the DUT, which are managed with BRDCFG/DUTCFG registers) or monitor the status of various things.

4.10 General Control (CTL)

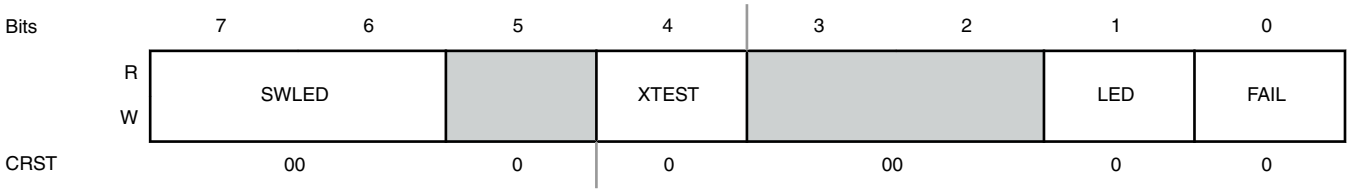
Address

Register	Offset
CTL	005h

Function

The CTL register is used to control various aspects of the target system.

Diagram



Fields

Field	Function
7-6 SWLED	Controls front-panel power-switch LEDs: when CTL.LED is set
5 -	Reserved.
4 XTEST	This bit directly drives the XTEST signal, typically driving an SMA connector. The function is user-defined.
3-2 -	Reserved.
1 LED	Software Diagnostic LED Enable: 0= Diagnostic LEDs operate normally. 1= Software can directly control the M3:M0 monitoring LEDs using the LED register.

Table continues on the next page...

Table continued from the previous page...

Field	Function
0 FAIL	Software Failure Diagnostic LED: 0= FAIL LED is not asserted due to software (it might still be on due to hardware failures). 1= FAIL LED is forced on. Generally, this indicates a software-diagnosed error.

4.11 Auxiliary (AUX)

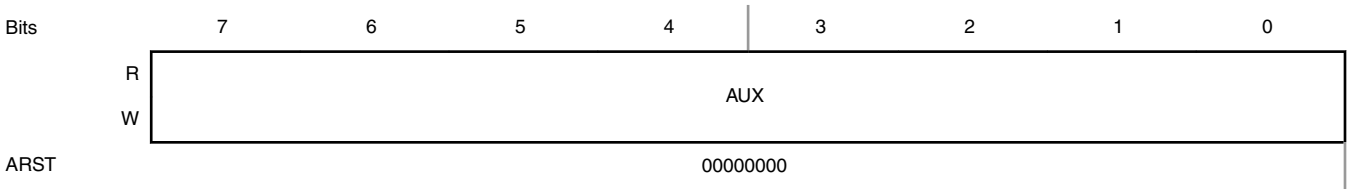
Address

Register	Offset
AUX	006h

Function

The AUX register may be used by software to store information. The AUX register is initialized to zero when the system is powered-up, and never altered by hardware again.

Diagram



Fields

Field	Function
7-0 AUX	User-defined value.

4.12 System Status (STAT_SYS)

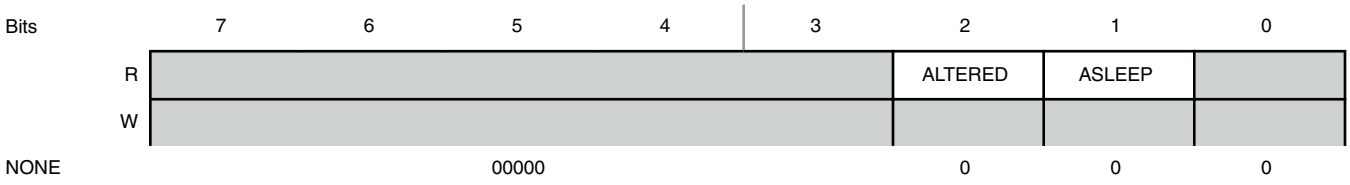
Address

Register	Offset
STAT_SYS	009h

Function

The STAT_SYS register reports general system status.

Diagram



Fields

Field	Function
7-3 -	Reserved.
2 ALTERED	Reconfiguration Active: 0= The system has been configured as normal. 1= The system has been reconfigured by software.
1 ASLEEP	ASLEEP Reporting: 0= At least one core is actively operating. 1= All cores are in sleep mode.
0 -	Reserved.

4.13 Alarm (ALARM)

Address

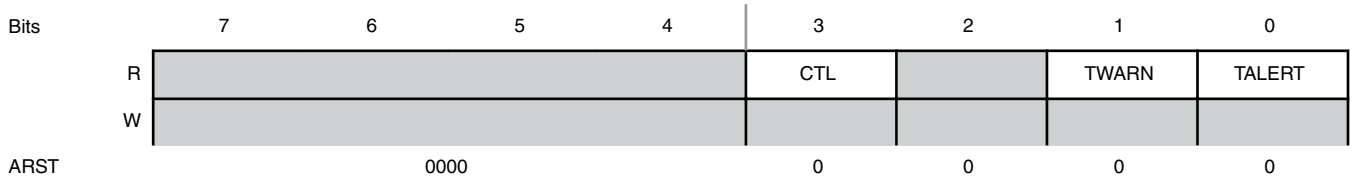
Register	Offset
ALARM	00Ah

Function

The ALARM register detects and reports any alarms raised in the QIXIS system.

Write 1 to an ALARM register bit to prevent Qixis from recognizing that alarm condition. By default, all alarms are handled.

Diagram



Fields

Field	Function
7-4 -	Reserved.
3 CTL	Software Fault (CTL[FAIL] was set).
2 -	Reserved.
1 TWARN	Temperature Fault: 0= The temperature is within normal limits. 1= The temperature has exceeded warning limits. NOTE: This signal may be asserted by either SA56004 thermal monitor. The temperature limits depend upon software programming.
0 TALERT	Temperature Alert: 0= The temperature is within normal limits. 1= The temperature has exceeded fault limits. NOTE: This signal may be asserted by either SA56004 thermal monitor. The temperature limits depend upon software programming.

4.14 Presence Detect 1 (STAT_PRES1)

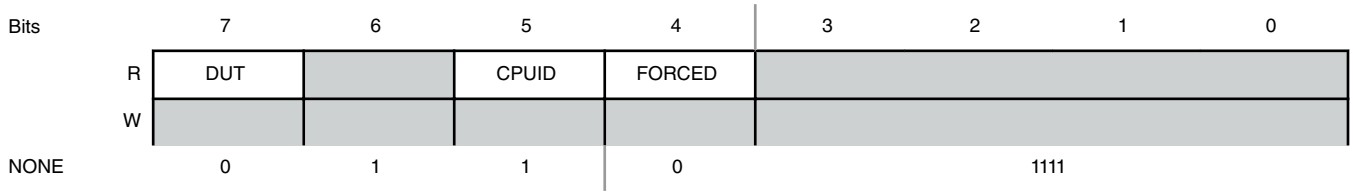
Address

Register	Offset
STAT_PRES1	00Bh

Function

The STAT_PRES1 register detects the presence and type of processor installed.

Diagram



Fields

Field	Function
7 DUT	Processor Present: 0= A processor is detected (soldered-in or socketed). 1= No device detected.
6 -	Reserved.
5 CPUID	Processor ID: 0= LS1043A (interposer) installed. 1= LS1028A installed.
4 FORCED	Processor Override: 0= Processor type (CPUID) is based on device. 1= Processor type (CPUID) was overridden using SW_CPU_FORCE.
3-0 -	Reserved.

4.15 Presence Detect 2 (STAT_PRES2)

Address

Register	Offset
STAT_PRES2	00Ch

Function

The STAT_PRES2 register detects the installation of cards in various PCI Express or SGMII slots.

Diagram

Bits	7	6	5	4	3	2	1	0
R	CFG					M2_3	M2_2	M2_1
W								
NONE	XXXX				1	1	1	1

Fields

Field	Function
7-4 CFG	M.2 #3 (SATA) module config/ID values: 0001= SATA SSD 0010= PCIe SSD Values reported depend on the type of module installed.
3 -	Reserved.
2 M2_3	0= a module is detected in M.2 connector #3 (SATA). 1= no module is detected.
1 M2_2	0= a module is detected in M.2 connector #2 (PEX). 1= no module is detected.
0 M2_1	0= a module is detected in M.2 connector #1 (PEX). 1= no module is detected.

4.16 LED Control (LED)

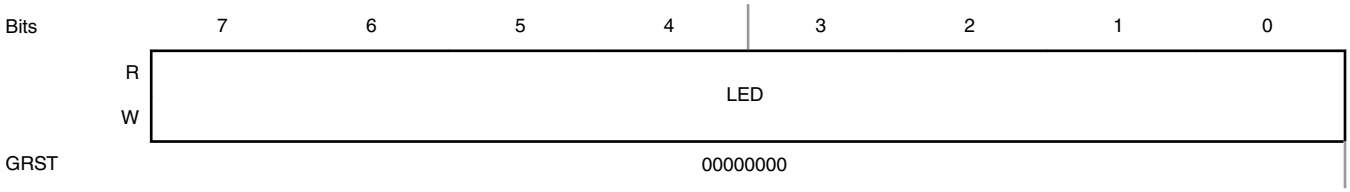
Address

Register	Offset
LED	00Eh

Function

The LED register can be used to directly control the monitoring LEDs (M3-M0) for software debugging or other purposes. Direct control of the LEDs is possible only when CTL[LED] is set to 1; otherwise they are used to display general system activity.

Diagram



Fields

Field	Function
7-0 LED	LED Status Control: 0= LED M[bitno] is off. 1= LED M[bitno] is on.

4.17 Reconfiguration Registers

This block of registers controls the operation of the reconfiguration system, which is used to alter the configuration of the board or processor into different voltages, SYSCLK frequencies, boot device selections, or any other configuration controlled by a BRDCFG or DUTCFG register.

4.18 Reconfiguration Control (RCFG)

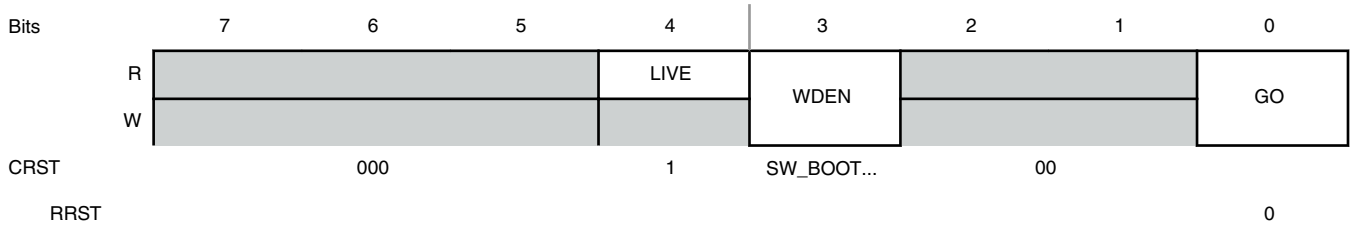
Address

Register	Offset
RCFG	010h

Function

The RCFG register is used to control the reconfiguration sequencer.

Diagram



Fields

Field	Function
7-5 -	Reserved.
4 LIVE	Immediate changes for BRDCFG registers: 1= BRDCFG registers outputs occur immediately. For QixMin, LIVE is always 1.
3 WDEN	Watchdog Enable: 0= The watchdog is not enabled during reconfiguration. 1= The watchdog is enabled during reconfiguration. If not disabled within 2^29 clock cycles (> 8 minutes), the system is reset. NOTE: This is not a highly-secure watchdog; software can reset this bit at any time and disable the watchdog.
2-1 -	Reserved.
0 GO	Reconfiguration Start: 0= Reconfiguration sequencer is idle. 1= On the 0-to-1 transition, the reconfiguration process begins.

4.19 USB Control (USB_STAT)

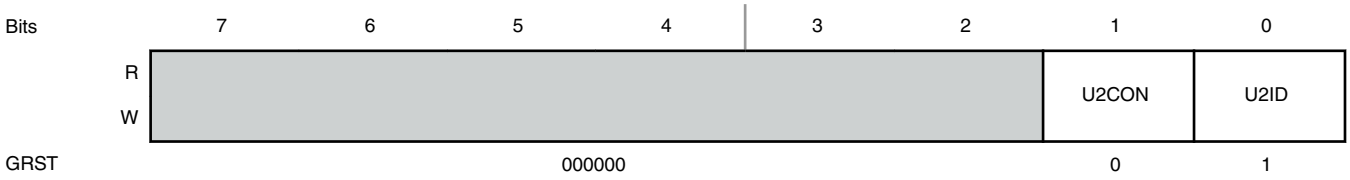
Address

Register	Offset
USB_STAT	01Dh

Function

The USB_STAT register reports USB 2 port status.

Diagram



Fields

Field	Function
7-2 -	Reserved.
1 U2CON	USB2 CON_DET Status: 0= No connection detected. 1= Connection detected.
0 U2ID	USB2 ID Status: 0= USB2 ID is low (DFP mode). 1= USB2 ID is high (UFP mode).

4.20 USB Control (USB_CTL)

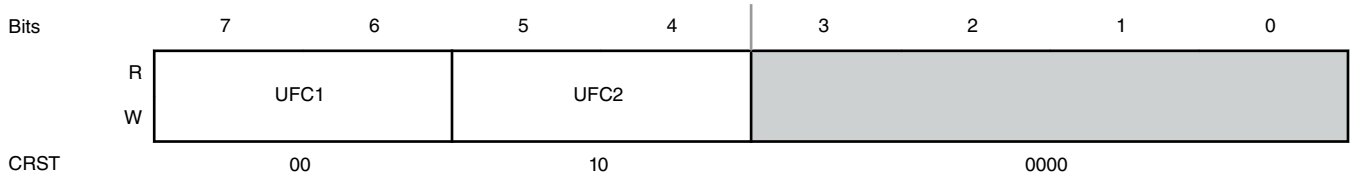
Address

Register	Offset
USB_CTL	01Eh

Function

The USB_CTL register manages USB features, principally USB fault control and/or status.

Diagram



Fields

Field	Function
7-6 UFC1	USB1 Fault Control: 0X= Normal operation. 10= Force USB1_PWRFAULT low (mask power-faults). 11= Force USB1_PWRFAULT high (trigger a power-fault condition).
5-4 UFC2	USB2 Fault Control: 10= Normal operation. 11= Force signal USB2_PWRFAULT high (trigger a power-fault condition).
3-0 -	Reserved.

4.21 Watchdog (WATCH)

Address

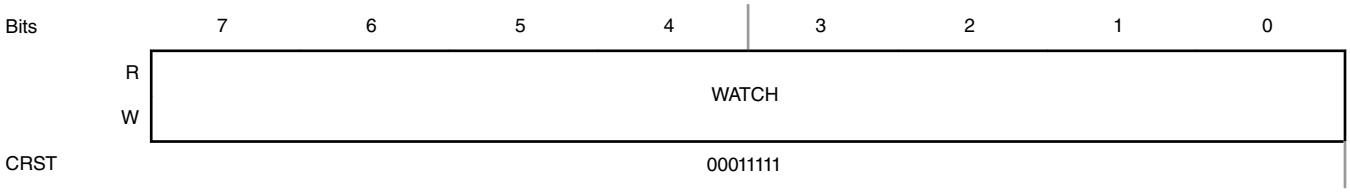
Register	Offset
WATCH	01Fh

Function

The WATCH register selects the watchdog timer value used during the reconfiguration processes. When RCFG[WDEN] enables the watchdog timer, a count down timer begins. If the DUT software does not disable or restart the watchdog timer within the specified limits, the system restarts.

Note that the watchdog timer is not dependent upon a reconfiguration sequence being active. While it is typically enabled along with RCFG[GO] as part of a reconfiguration sequence; in fact, it is independent and can be enabled for any reason.

Diagram



Fields

Field	Function

7-0
WATCH
	Watchdog timer value, as determined by the formula:
	`time-out = [ WATCH * (2.0sec) ] + 2.0sec`
	Examples:
	`11111111= 8 min`
	`00111111= 2 min`
	`00001111= 32 sec`
	`00000011= 8 sec`
	`00000000= 2 sec`

4.22 Power Control/Status Registers

The power registers provide the ability to monitor general power status, as well as individual power status (for those supplies that have reporting capability). Other registers provide limited power control features (most power control is through the PMBus/I2C interface).

4.23 Power Control 2 (PWR_CTL2)

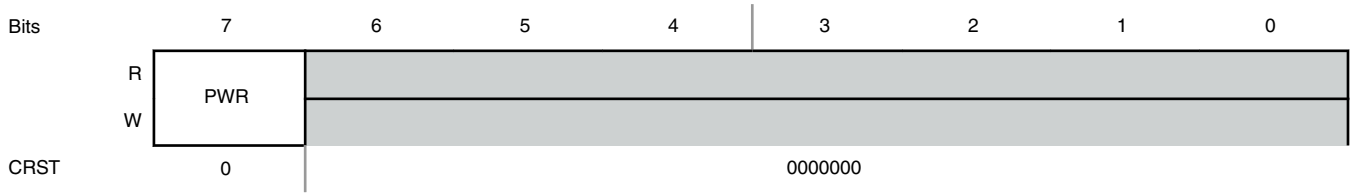
Address

Register	Offset
PWR_CTL2	021h

Function

The PWR_CTL2 register is used to control system power-on/power-off events.

Diagram



Fields

Field	Function
7 PWR	System Power Off: 0= No action. 1= On the 0-to-1 transition, power-off the system. The system must be externally powered up.
6-0 -	Reserved.

4.24 Power Status 0 (PWR_MSTAT)

Address

Register	Offset
PWR_MSTAT	024h

Function

The PWR_MSTAT register monitors the overall power status of the board, including that of the main (ATX or other) power supply used to power all other rails.

Diagram

Bits	7	6	5	4	3	2	1	0
R	ATXON	ATXGD		FAULT	PWROK		SSTATE	
W								
NONE	1	1	0	0	1	0	11	

Fields

Field	Function
7 ATXON	Main Power Supply Control Status: 0= Power supply is set to off. 1= Power supply is set to on.
6 ATXGD	Main Power Supply Status: 0= Power supply is off or not yet stable. 1= Power supply is on and stable.
5 -	Reserved.
4 FAULT	Faulted: 0= Power supply system operating normally. 1= Power supply system was shutdown for some reason. Check the ALARM register for details.
3 PWROK	General Power Status: 0= One or more power supplies are off or not yet stable. 1= All power supplies are on and stable.
2 -	Reserved.
1-0 SSTATE	Reports the current power savings level, for those devices which support it. 11= S3 - completely on Note: If a device does not support hardware (i.e external) power savings modes, S3 is always reported.

4.25 Power Status 1 (PWR_STAT1)

Address

Register	Offset
PWR_STAT1	025h

Function

The PWR_STAT1 registers is used to monitor the status of individual power supplies. If a bit is set to '1', the respective power supply is operating correctly.

Diagram

Bits	7	6	5	4	3	2	1	0
R	TA_BB			DPPWR	DDR	P5V	P3V3	VDD
W								
NONE	1	11		1	1	1	1	1

Fields

Field	Function
7 TA_BB	TA_BB Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
6-5 -	Reserved.
4 DPPWR	DP Power Fault: 0= DP_PWR is faulted (overcurrent). 1= DP_PWR is operating.
3 DDR	DDR Power Supplies (GVDD, VTT, MVREF) Status: 0= Power supplies are disabled or faulted. 1= Power supply are operating.
2 P5V	5V0 Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
1 P3V3	3V3 Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.
0 VDD	VDD Power Supply Status: 0= Power supply is disabled or faulted. 1= Power supply is operating.

4.26 Clock Control Registers

The clock control registers control programmable clock synthesizers used to supply clocks to the processor and associated peripherals.

4.27 Clock Speed 1 (CLK_SPD1)

Address

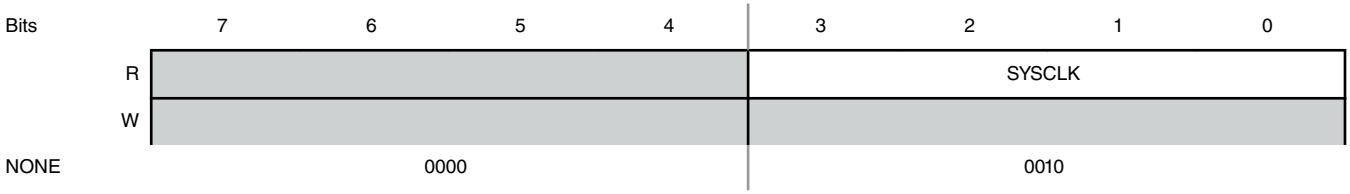
Register	Offset
CLK_SPD1	030h

Function

The CLK_SPD1 register is used to report the user-selectable speed settings (typically from switches) for the SYSCLK and DDRCLK clocks.

Values in the CLK_SPD1 register are used by boot software accurately initialize timing-dependent parameters, such as for UART baud rates, I2C clock rates, and DDR memory timing.

Diagram



Fields

Field	Function
7-4 -	Reserved.

3-0
SYSCLK
	SYSCLK Rate Selection:
	`0010= 100.00 MHz (fixed)`
	`Other values are Reserved.`

4.28 Clock ID/Status (CLK_ID)

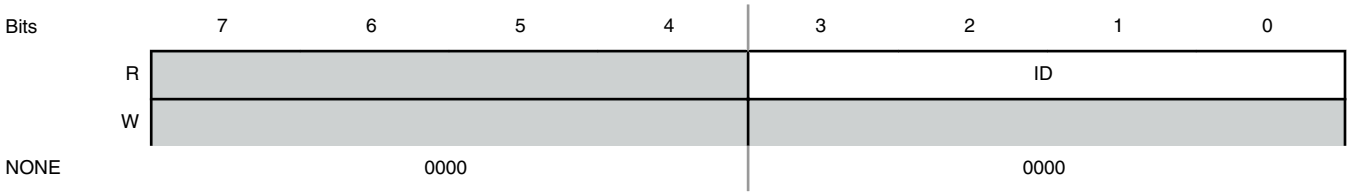
Address

Register	Offset
CLK_ID	033h

Function

The CLK_ID register is used to identify the arrangement of the clock control registers. Software should check CLK_ID register before attempting to interpret/control the clock control registers.

Diagram



Fields

Field	Function
7-4 -	Reserved.
3-0 ID	System Clock ID = 0000 (NONE) CLK0= SYSCLK is fixed on this system.

4.29 Reset Control Registers

The reset control register group handles reset behavior configuration and general monitoring of resets.

4.30 Reset Control (RST_CTL)

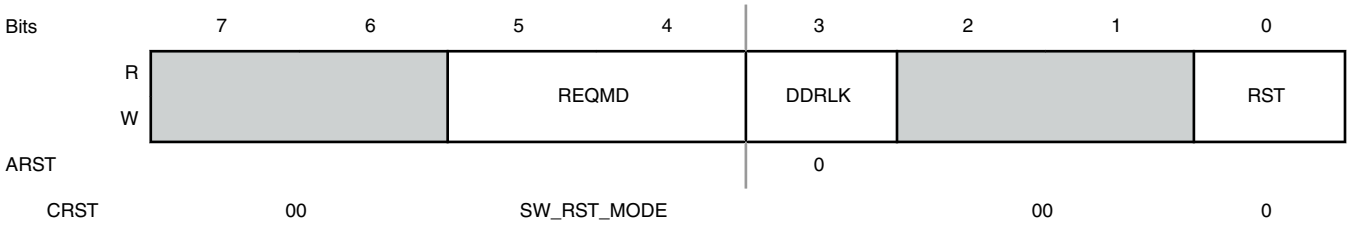
Address

Register	Offset
RST_CTL	040h

Function

The RST_CTL register is used configure or trigger reset actions.

Diagram



Fields

Field	Function
7-6 -	Reserved.
5-4 REQMD	Reset Request (RESET_REQ_B) handling: 00= Disabled - do nothing. 11= Normal - assert PORESET_B to DUT to begin normal reset sequence.
3 DDRLK	DDR Reset Lock: 0= Reset is asserted to the DDR DIMMs/devices normally. 1= Reset will not be asserted to the DDR DIMMs/devices. With proper DDR controller setup and careful software setup DDR contents can survive resets. This bit is not cleared with a general reset, but is preserved, as long as power is available. It is expected that software that sets this bit is also responsible for clearing it.
2-1 -	Reserved.
0 RST	Reset: 0= Reset sequencer operates normally. 1= Upon transition from 0 to 1, restart the reset sequence.

4.31 Reset Status (RST_STAT)

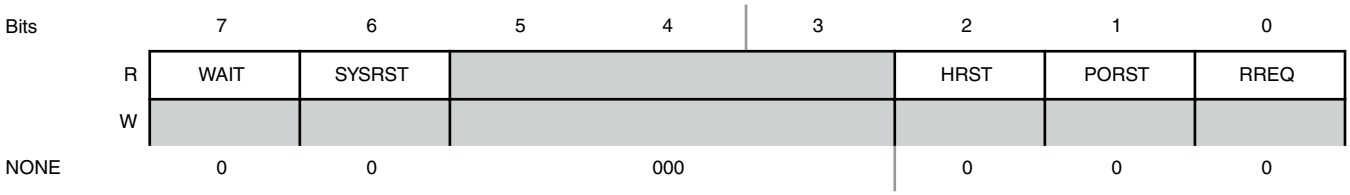
Address

Register	Offset
RST_STAT	041h

Function

The RST_STAT register reports the current status of various reset-related signals.

Diagram



Fields

Field	Function
7 WAIT	Reset Waiting: 0= Reset sequencer is operating normally. 1= Reset sequencer is in RMT-WAIT state, waiting for permission to proceed.
6 SYSRST	System Reset: 0= System is operating normally. 1= System is in reset.
5-3 -	Reserved.
2 HRST	HRESET_B status: 0= HRESET_B is not asserted. 1= HRESET_B is asserted.
1 PORST	PORESET_B status: 0= PORESET_B is not asserted. 1= PORESET_B is asserted.
0 RREQ	RESET_REQ_B status: 0= RESET_REQ_B is not asserted. 1= RESET_REQ_B is asserted.

4.32 Reset Event Trace (RST_REASON)

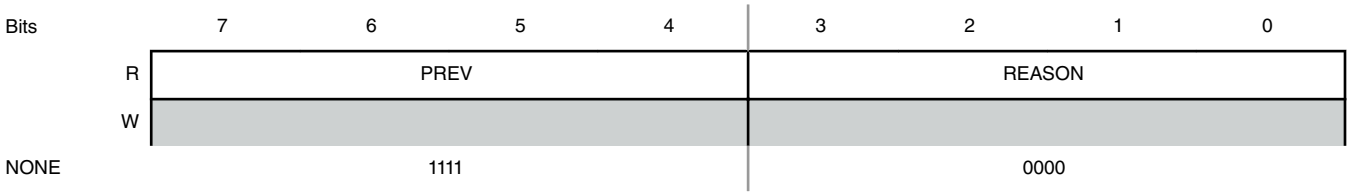
Address

Register	Offset
RST_REASON	042h

Function

The RST_REASON register is used to report the cause of the most-recent reset cycle.

Diagram



Fields

Field	Function
7-4 PREV	Previous reset reason: See REASON field codes.
3-0 REASON	Reset Reason: 0000= Power-on reset 0001= COP/JTAG HRESET_B was asserted 0010= (reserved) 0011= RST_CTL[RST] was set 0100= Reset switch (chassis or on-board) was pushed. 0101= RCFG[GO] (that is, reconfiguration reset) was asserted. 0110= RESET_REQ_B assertion (from processor) was asserted. 1111= No event recorded yet.

4.33 Reset Force 1 (RST_FORCE1)

Address

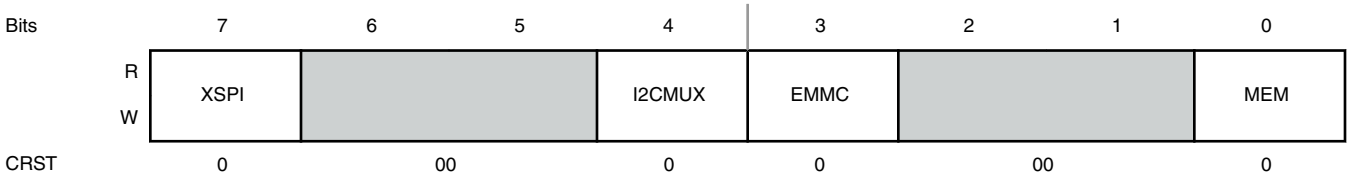
Register	Offset
RST_FORCE1	043h

Function

The RST_FORCEn registers are used to force reset to a particular device, independent of the general reset sequencer. As long as a bit is set to 1, the reset signal to grouped devices will be asserted.

Resetting a resource while in used by the bootloader or OS will typically cause crashes, etc. Use carefully.

Diagram



Fields

Field	Function
7 XSPI	1= Assert RST_XSPI_B.
6-5 -	Reserved.
4 I2CMUX	1= Assert RST_I2CMUX_B.
3 EMMC	1= Assert RST_EMMC _B
2-1 -	Reserved.
0 MEM	Reset DDR DIMM. 1= Assert RST_MEM_B

4.34 Reset Force 2 (RST_FORCE2)

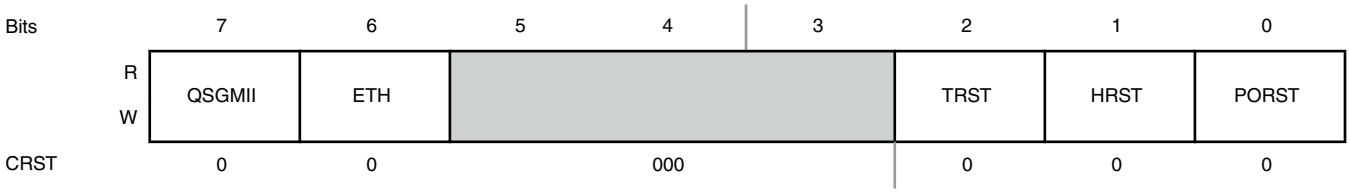
Address

Register	Offset
RST_FORCE2	044h

Function

Assert selected reset sources. See RST_FORCE1 for details.

Diagram



Fields

Field	Function
7 QSGMII	1= Assert RST_QSGMII_B for the NXP F104 PHY.
6 ETH	1= Assert RST_ETH_B for the Qualcomm AR8033 PHY.
5-3 -	Reserved.
2 TRST	1= Assert DUT_TRST_B.
1 HRST	1= Assert DUT_HRESET_B. NOTE: This bit only asserts the signal to the DUT; it is not intended to be used as a general system reset.
0 PORST	1= Assert DUT_PORESET_B. NOTE: This bit only asserts the signal to the DUT; it is not intended to be used as a general system reset.

4.35 Reset Force 3 (RST_FORCE3)

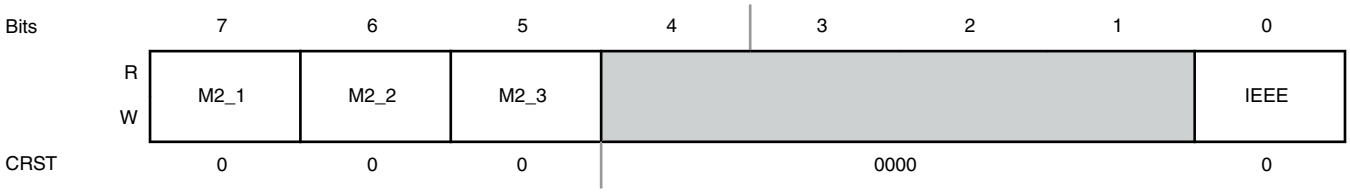
Address

Register	Offset
RST_FORCE3	045h

Function

Assert selected reset sources. See RST_FORCE1 for details.

Diagram



Fields

Field	Function
7 M2_1	1= Assert RST_PEXM2_1_B.
6 M2_2	1= Assert RST_PEXM2_2_B.
5 M2_3	1= Assert RST_SATAM2_3_B.
4-1 -	Reserved.
0 IEEE	1= Force RST_IEEE1588_B.

4.36 Reset Mask 1 (RST_MASK1)

Address

Register	Offset
RST_MASK1	04Bh

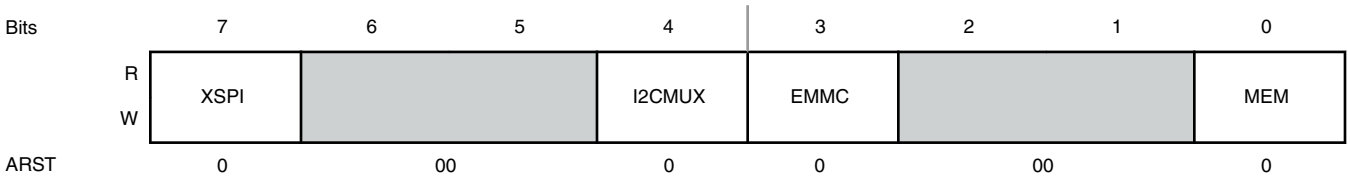
Function

The RST_MASKn registers are used to block reset to a particular device, independent of the general reset sequencer. As long as a bit is set to 1, the reset signal to that device or devices will be blocked.

RST_MASKn bits have the same bit definition as their counterparts in RST_FORCEn; refer to Table 5-53 for details.

Note that RST_MASK bits are cleared on AUX reset, and so are usually only cleared by software. This is very different from the RST_FORCE registers.

Diagram



Fields

Field	Function
7 XSPI	1= Mask RST_XSPI_B.
6-5 -	Reserved.
4 I2CMUX	1= Mask RST_I2CMUX_B.
3 EMMC	1= Mask RST_EMMC _B
2-1 -	Reserved.
0 MEM	Reset DDR DIMMs. 1= Mask RST_MEM_B

4.37 Reset Mask 2 (RST_MASK2)

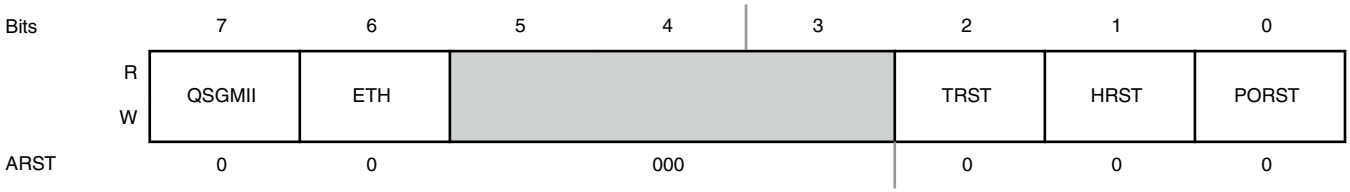
Address

Register	Offset
RST_MASK2	04Ch

Function

Mask selected reset sources. See RST_FORCE1 for details.

Diagram



Fields

Field	Function
7 QSGMII	1= Mask RST_QSGMII_B.
6 ETH	1= Mask RST_ETH_B for the RealTek PHY.
5-3 -	Reserved.
2 TRST	1= Mask DUT_TRST_B.
1 HRST	1= Mask DUT_HRESET_B.
0 PORST	1= Mask DUT_PORESET_B.

4.38 Reset Mask 2 (RST_MASK3)

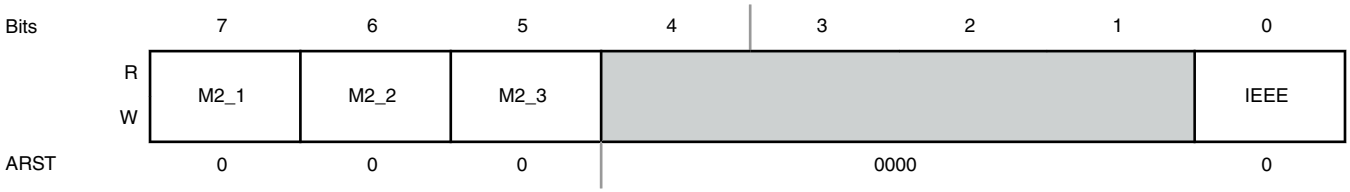
Address

Register	Offset
RST_MASK3	04Dh

Function

Mask selected reset sources. See RST_FORCE1 for details.

Diagram



Fields

Field	Function
7 M2_1	1= Mask RST_PEXM2_1_B.
6 M2_2	1= Mask RST_PEXM2_2_B.
5 M2_3	1= Mask RST_SATAM2_3_B.
4-1 -	Reserved.
0 IEEE	1= Mask RST_IEEE1588_B.

4.39 Board Configuration Registers

This block of registers control the configuration of the board. BRDCFG registers are always static, driven at all times power is available. There are up to 16 registers providing up to 128 control options; however, not every platform implements all the registers.

4.40 Board Configuration 0 (BRDCFG0)

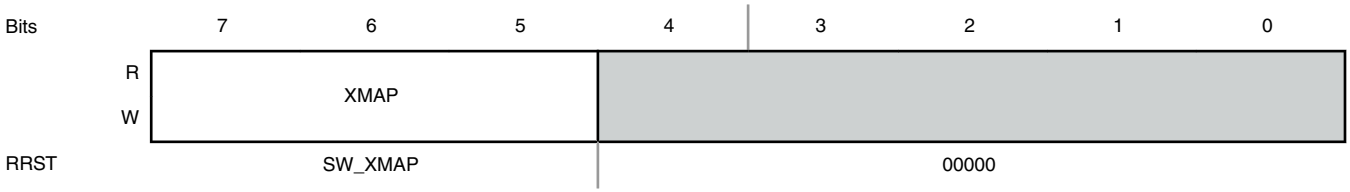
Address

Register	Offset
BRDCFG0	050h

Function

The BRDCFG0 register is commonly used to select IFC and QSPI boot devices.

Diagram



Fields

Field	Function

7-5
XMAP
	XMAP controls how XSPI_A chip-selects are connected to devices/peripherals.
	`XSPI_A_CS0 XSPI_A_CS1`
	`========== ==========`
	`000= sNOR sNAND`
	001= sNAND sNOR
	`010= EMU sNOR`
	011= EMU sNAND
	`100= sNOR EMU`

4-0 -	Reserved.

4.41 Board Configuration 1 (BRDCFG1)

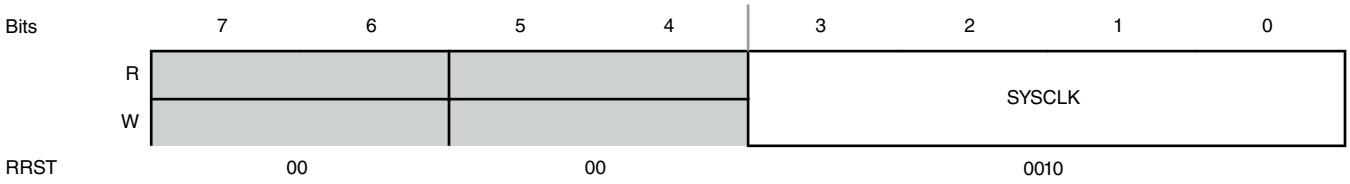
Address

Register	Offset
BRDCFG1	051h

Function

The BRDCFG1 register shows/controls SYSCLK and DDRCLK speeds.

Diagram



Fields

Field	Function
7-6 -	Reserved.
5-4 -	Reserved.
3-0 SYSCLK	SYSCLK Frequency Selection: 0010= 100.00 MHz (fixed) All other values are reserved.

4.42 Board Configuration 2 (BRDCFG2)

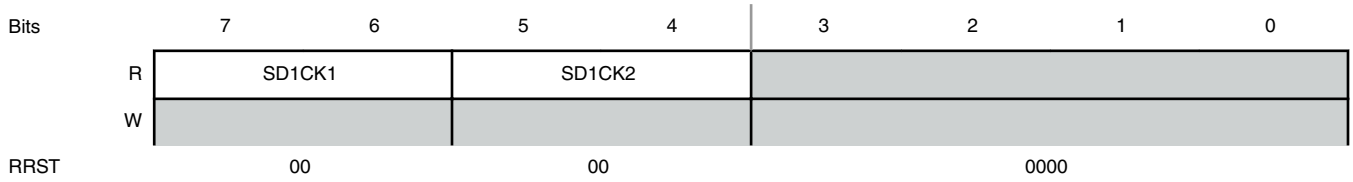
Address

Register	Offset
BRDCFG2	052h

Function

The BRDCFG2 register reporst SerDes clock speeds for SerDes blocks 1 and 2.

Diagram



Fields

Field	Function
7-6 SD1CK1	SerDes1 Clock #1 Rate: 00= 100.000 MHz (fixed)
5-4 SD1CK2	SerDes1 Clock #2 Rate: 00= 100.000 MHz (fixed)
3-0 -	Reserved.

4.43 Board Configuration 3 (BRDCFG3)

Address

Register	Offset
BRDCFG3	053h

Function

The BRDCFG3 register controls board routing.

Diagram

Bits	7	6	5	4	3	2	1	0
R	PWM2	SPI3	UART2		GTA			
W								
RRST	SW_UBUS...	SW_UBUS...	SW_UART2		0	1	00	

Fields

Field	Function
7 PWM2	Controls routing of PWM (FTM1_CH1) for uCLICK modules (nets CFG_MUX_PWM2*): 0= Routed to uBUS1 module. 1= Routed to uBUS2 module.
6 SPI3	Controls routing of SPI3 for uCLICK modules (nets CFG_MUX_SPI3*): 0= Routed to uBUS1 module. 1= Routed to uBUS2 module.
5-4 UART2	Controls routing of UART2 (nets CFG_MUX_UART2*): 00= Routed to RS232 transceiver and DB9 connector P1A (default). 01= reserved. 10= Routed to uBUS1 module. 11= Routed to uBUS2 module.
3 GTA	Controls whether GPIO3 can drive TA_TMP_DETECT_B: 0= Normal mode, GPIO3 is ignored. 1= Test, TA_TMP_DETECT_B is driven with the logical-OR of GPIO3\[4:2\].
2 -	Reserved. Controls the SAI/IEEE multiplexer (MUXSEL_SAI_EN): 0= IEEE signals connect to the IEEE header. 1= IEEE signals connect to the SAI4 CODEC.
1-0 -	Reserved.

4.44 Board Configuration 4 (BRDCFG4)

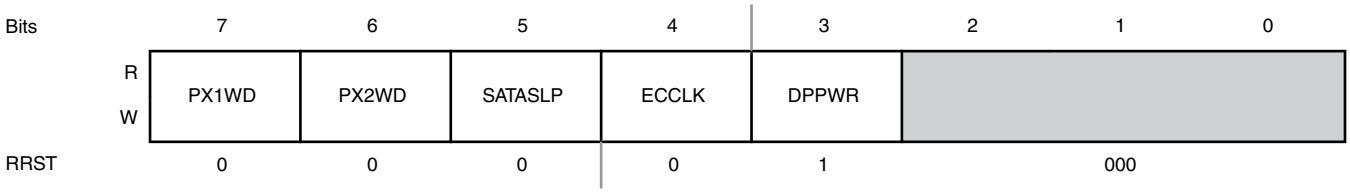
Address

Register	Offset
BRDCFG4	054h

Function

The BRDCFG4 register controls general board configuration.

Diagram



Fields

Field	Function
7 PX1WD	PCI Express M.2 Wireless disable (net CFG_PEX1_WDIS_B): 0= Board operates normally. 1= Board wireless shutdown requested.
6 PX2WD	PCI Express M.2 Wireless disable (net CFG_PEX2_WDIS_B): 0= Board operates normally. 1= Board wireless shutdown requested.
5 SATASLP	SATA DevSlp control (net SATAM2_3_DEVSLP): 0= SATA module operates normally. 1= SATA module enters sleep-mode.
4 ECCLK	EC1_CLK Enable (net EC1_125MHZ_EN): 0= Clock is enabled (default). 1= Clock is disabled.
3 DPPWR	DisplayPort Power Enable (net DP_PWR_EN): 0= DP_PWR is disabled. 1= DP_PWR is enabled (default).

Table continues on the next page...

Table continued from the previous page...

Field	Function
2-0 -	Reserved.

4.45 Board Configuration 5 (BRDCFG5)

Address

Register	Offset
BRDCFG5	055h

Function

The BRDCFG5 register manages uBUS1 connections and status.

Diagram

Bits	7	6	5	4	3	2	1	0
R	U1A	U1I	U1R		U1IRQ		U1RST	
W								
RRST	X	X	X	0	00		00	

Fields

Field	Function
7 U1A	U1A reports the current 3.3V LVTTL level on the AN analog output pin.
6 U1I	U1I reports the current 3.3V LVTTL level on the IRQ interrupt pin.
5 U1R	U1R reports the current 3.3V LVTTL level on the RST pin.
4 -	Reserved.

Table continues on the next page...

Table continued from the previous page...

Field	Function
3-2 U1IRQ	Manages the uBUS1 IRQ input pin: 00= IRQ pin treated as active-low interrupt input. 01= IRQ pin treated as active-high interrupt input. 10= IRQ pin treated as output, asserted low. 11= IRQ pin treated as output, asserted high.
1-0 U1RST	Manages the uBUS1 RST output pin: 00= RST pin tri-stated. 01= reserved. 10= RST pin treated as output, asserted low. 11= RST pin treated as output, asserted high.

4.46 Board Configuration 6 (BRDCFG6)

Address

Register	Offset
BRDCFG6	056h

Function

The BRDCFG6 register manages uBUS2 connections and status.

Diagram

Bits	7	6	5	4	3	2	1	0
R	U2A	U2I	U2R		U2IRQ		U2RST	
W								
RRST	X	X	X	0	00		00	

Fields

Field	Function
7 U2A	U2A reports the current 3.3V LVTTL level on the AN analog output pin.

Table continues on the next page...

Table continued from the previous page...

Field	Function
6 U2I	U2I reports the current 3.3V LVTTL level on the IRQ interrupt pin.
5 U2R	U2R reports the current 3.3V LVTTL level on the RST pin.
4 -	Reserved.
3-2 U2IRQ	Manages the uBUS2 IRQ input pin: 00= IRQ pin treated as active-low interrupt input. 01= IRQ pin treated as active-high interrupt input. 10= IRQ pin treated as output, asserted low. 11= IRQ pin treated as output, asserted high.
1-0 U2RST	Manages the uBUS2 RST output pin: 00= RST pin tri-stated. 01= reserved. 10= RST pin treated as output, asserted low. 11= RST pin treated as output, asserted high.

4.47 DUT Configuration Registers

This block of registers control the configuration of the DUT (Device Under Test). DUTCFG registers, unlike BRDCFG registers, are not always driven - they are driven only during the reset configuration sampling interval (PORESET_B assertion), and remain tri-stated thereafter. Refer to the device hardware specification for hardware pin-sampled timing parameters.

4.48 DUT Configuration 0 (DUTCFG0)

Address

Register	Offset
DUTCFG0	060h

Function

The DUTCFG0 register is used to the RCW location setting (cfg_rcw_src).

Diagram

Fields

Field	Function
7-4 -	Reserved.
3-0 RCWSRC	RCW Source Location: 0000 : Hard-coded RCW 1000 : SDHC1: SD Card 1001 : SDHC2: eMMC 1010 : UEFI/I2C Boot EEPROM 1100 : FlexSPI Serial NAND, 2kB pages 1101 : FlexSPI Serial NAND, 4kB pages 1111 : XSPI serial NOR, 24bit address Note that the RCW_SRC settings are mapped to equivalent 9-bit values when an LS1043A interposer is connected.

4.49 DUT Configuration 1 (DUTCFG1)

Address

Register	Offset
DUTCFG1	061h

Function

The DUTCFG1 register specifies the type of DDR memory attached, and the operating voltages for it.

Diagram

Fields

Field	Function
7 DRAM	Set DDR DRAM type Selection (configuration signal cfg_dram_type): 0= DDR4 (default). 1= DDR3L (not supported)
6-0 -	Reserved.

4.50 DUT Configuration 2 (DUTCFG2)

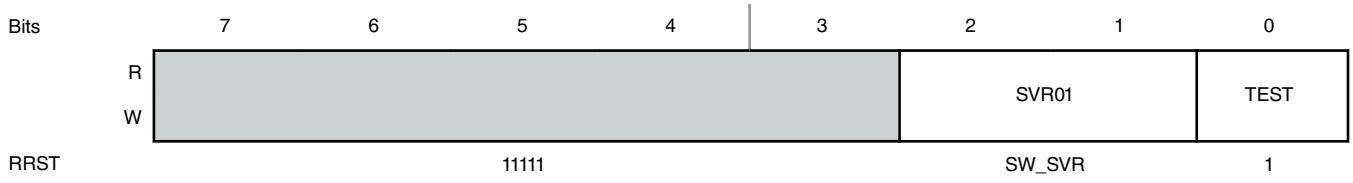
Address

Register	Offset
DUTCFG2	062h

Function

The DUTCFG2 register manages device selection (SVR) and internal-only device test features.

Diagram



Fields

Field	Function
7-3 -	Reserved.

Table continues on the next page...

Table continued from the previous page...

Field	Function
2-1 SVR01	Controls cfg_svr[0:1] (note the bit order).
0 TEST	Controls processor pin TESTSEL_B. NOTE: Unlike all other DUTCFG bits, TESTSEL is always driven.

4.51 DUT Configuration 11 (DUTCFG11)

Address

Register	Offset
DUTCFG11	06Bh

Function

The DUTCFG11 register is used to control the CFG_ENG_USE[7:0] signals. The function of these bits are defined by silicon engineers for special use.

Diagram

Fields

Field	Function
7 ENGUSE0	Controls (cfg_enguse0): 0= Processor uses differential SYSCLK_P/SYSCLK_N input (LS1043 only). 1= Reserved (default).
6-0 -	Reserved.

4.52 GPIO Registers

The GPIO registers provide an 8-bit general-purpose GPIO port. For the LS1028A RDB, the following connections are provided:

LS1028A GPIO3\[4:2\] =>

GPIO\[4:2\]

4.53 GPIO I/O (GPIO_IO)

Address

Register	Offset
GPIO_IO	080h

Function

GPIO_IO is the input/output registers of the 8-bit GPIO port.

Read operations return the current pin state, whether driven externally (input mode) or driven internally (output mode).

Write operations set the pin level when in output mode; writes while in input mode are ignored.

Undefined pins read as '0'.

Diagram

Bits	7	6	5	4	3	2	1	0
R				IO4	IO3	IO2		
W								
CRST	111			1	1	1	11	

Fields

Field	Function
7-5 -	Reserved.
4 IO4	IO port values (if corresponding DIR.n is 0): 0= input pin is at level 0. 1= input pin is at level 1. IO port values (if corresponding DIR.n is 1): 0= output pin driven to level 0. 1= output pin driven to level 1.
3 IO3	Same as IO4.

Table continues on the next page...

Table continued from the previous page...

Field	Function
2 IO2	Same as IO4.
1-0 -	Reserved.

4.54 GPIO Direction (GPIO_DIR)

Address

Register	Offset
GPIO_DIR	084h

Function

GPIO_DIR is the direction control registers of the 8-bit GPIO port.

If a GPIO_DIR register bit is 0, the corresponding GPIO port pin is in input mode, and can be accessed through the same GPIO1_IOn pin.

If a GPIO_DIR register bit is 1, the corresponding GPIO port pin is in output mode, and GPIO1 port pins are set to the corresponding value in GPIO_IOn.

Diagram

Bits	7	6	5	4	3	2	1	0
R				IO4	DIR3	DIR3		
W								
CRST	000			0	0	0	00	

Fields

Field	Function
7-5 -	Reserved.

Table continues on the next page...

Table continued from the previous page...

Field	Function
4 IO4	IO port values (if corresponding DIR.n is 0): 0= input pin is at level 0. 1= input pin is at level 1. IO port values (if corresponding DIR.n is 1): 0= output pin driven to level 0. 1= output pin driven to level 1.
3 DIR3	Same as DIR4.
2 DIR3	Same as DIR4.
1-0 -	Reserved.

4.55 IRQ Status Registers

The IRQSTATn registers show the current (live) states of various IRQ/EVT pins.

IRQ/EVT signals have programmable polarities, so no interpretation is made as to whether the signal is asserted or deasserted.

4.56 Interrupt Status 0 (IRQSTAT0)

Address

Register	Offset
IRQSTAT0	090h

Function

IRQ_STATn registers report the current level of various IRQ/EVT signals.

IRQ/EVT signals have programmable polarities, so no interpretation is made as to whether the signal is asserted or deasserted.

Diagram

Bits	7	6	5	4	3	2	1	0
R	ETH	QSGMII			RTC		UBUS2	UBUS1
W								
NONE	1	1	11		1	1	1	1

Fields

Field	Function
7 ETH	Interrupt input IRQ_ETH_B: 0: Interrupt is asserted.
6 QSGMII	Interrupt input IRQ_QSGMII_B: 0: Interrupt is asserted.
5-4 -	Reserved.
3 RTC	Interrupt input IRQ_RTC_B: 0: Interrupt is asserted.
2 -	Reserved.
1 UBUS2	Interrupt input IRQ_UBUS2_B: 0: Interrupt is asserted.
0 UBUS1	Interrupt input IRQ_UBUS1_B: 0: Interrupt is asserted.

4.57 Interrupt Status 1 (IRQSTAT1)

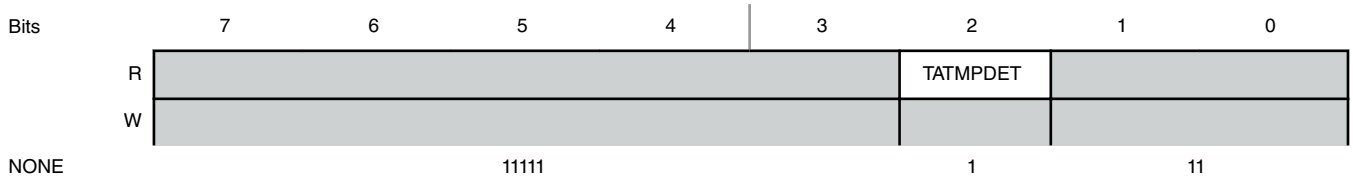
Address

Register	Offset
IRQSTAT1	091h

Function

Additional IRQ_STAT reporting; see IRQSTAT0 for details.

Diagram



Fields

Field	Function
7-3 -	Reserved.
2 TATMPDET	1: TMP_DETECT_B signal is high.
1-0 -	Reserved.

4.58 Interrupt Status 2 (IRQSTAT2)

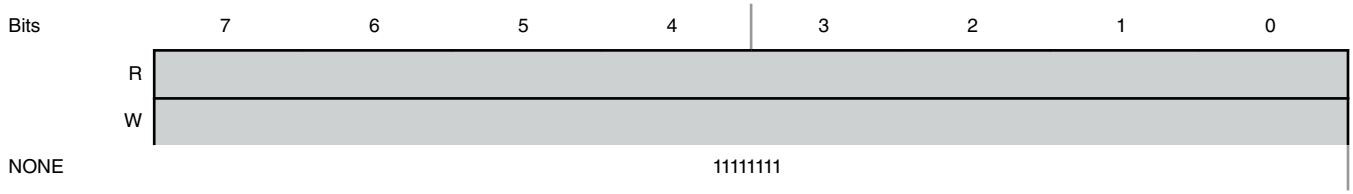
Address

Register	Offset
IRQSTAT2	092h

Function

Additional IRQ_STAT reporting; see IRQSTAT0 for details.

Diagram



Fields

Field	Function
7-0 -	Reserved.

4.59 Interrupt Drive 5 (IRQDRV5)

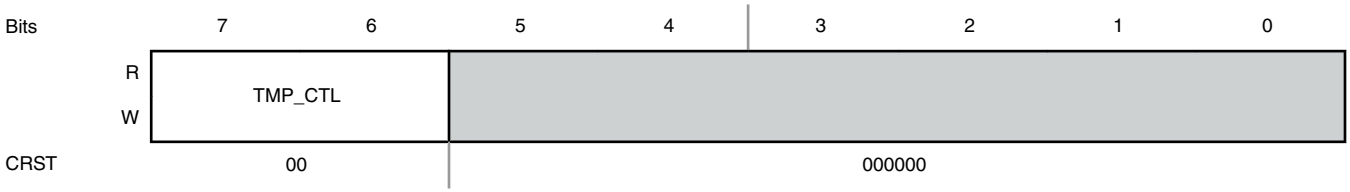
Address

Register	Offset
IRQDRV5	09Dh

Function

IRQDRV5 allows controlling misc. interrupts such as TA_TMP_DETECT, where possible.

Diagram



Fields

Field	Function
7-6 TMP_CTL	Allows control of the TMP_DETECT_B pin. 0X= Undriven (Z). 10= Drive TMP_DETECT_B low. 11= Drive TMP_DETECT_B high. The status of TMP_DETECT_B can be monitored with the IRQSTAT registers.
5-0 -	Reserved.

4.60 Core Management Space Registers

The core management address/data registers allow access to internal Qixis control registers, primarily the direct switch access registers which allow easy reporting of board configuration.

For RDB systems, only the following are defined:

CMS Registers

Address	Name	Definition
00	SW#	Number of configuration switches.
01..0F	SWn	Image of configuration switch #n.

Ranges not listed are reserved.

A standard use of the CMSA/CMSD port is to read the state of configuration switches, for example:

```
Qixis_Set_Reg( CMS_A, 00h );

nr = Qixis_Get_Reg( CMS_D );

for (i = 1; i <= nr; i++) {

   Qixis_Set_Reg( CMS_A, i );

   printf("SW%1d = %02X\\ n", i, Qixis_Get_Reg( CMS_D ));

}
```

4.61 Core Management Address (CMSA)

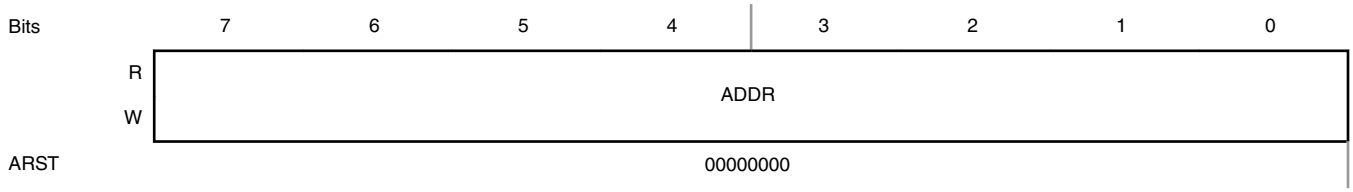
Address

Register	Offset
CMSA	0D8h

Function

The CMSA register selects one of the internal core management registers within Qixis for subsequent read- or write-access via the CMSD register.

Diagram



Fields

Field	Function
7-0 ADDR	Select internal CMS register for read/write via CMSD.

4.62 Core Management Data (CMSD)

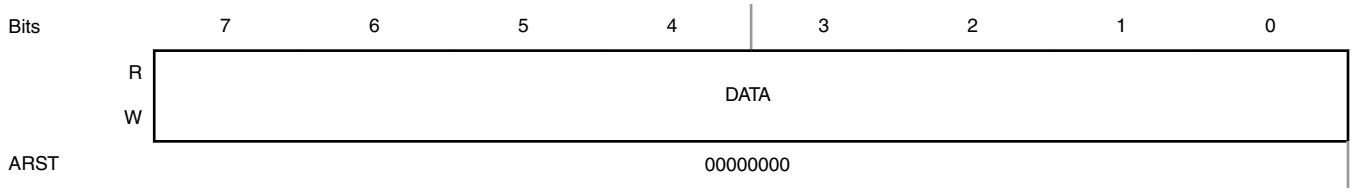
Address

Register	Offset
CMSD	0D9h

Function

CMSD contains the value of a CMS register selected by CMSA. See CMSA for details.

Diagram



Fields

Field	Function
7-0 DATA	Read/write internal CMS registers selected with CMSA.

Appendix A
Revision History

The table below summarizes the revisions to this document.

Table 36. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. B	11/2018	Synchronous audio interface (SAI) on page 30	Added section.
		Switch configuration on page 51	Updated SW1[8] description in Table 28. Switch settings on page 51.
		XSPI interface on page 38	Updated Table 17. XSPI configuration on page 39.
		Clocks on page 21	• Updated Table 6. LS1028ARDB clocks on page 22. • Updated Figure 7. on page 21.
		Ethernet controller interface on page 27	• Updated IEEE 1588 interface on page 29 section. • Updated Figure 11. on page 28.
		I2C interface on page 34	Updated Figure 17. on page 36.
		GPIOs on page 43	Added detail about GPIO1_DAT[24]
		Adapter	Added topic.
		Qixis Programming Model on page 58	Updated Interrupt Status 0 (IRQSTAT0), Power Status 1 (PWR_STAT1) registers.
Rev. A	02/2018	-	Initial NDA revision

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