*Application Report*
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# *Using the TPS5430 as an Inverting Buck-Boost Converter*

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## ABSTRACT

The wide input voltage range SWIFT™ (Switcher With Integrated FET) dc/dc converters are typically used as step-down converters where the derived output is a positive voltage less than the input voltage source. In some cases, it may be required to generate a negative voltage from the input voltage source. In such instances, it is possible to configure the TPS5430/20/10 devices in an inverting buck–boost topology, where the output voltage is negative with respect to ground.

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## 1 Basic Buck Topology

To understand the circuit operation, consider the basic topology of the buck converter as shown in Figure 1.

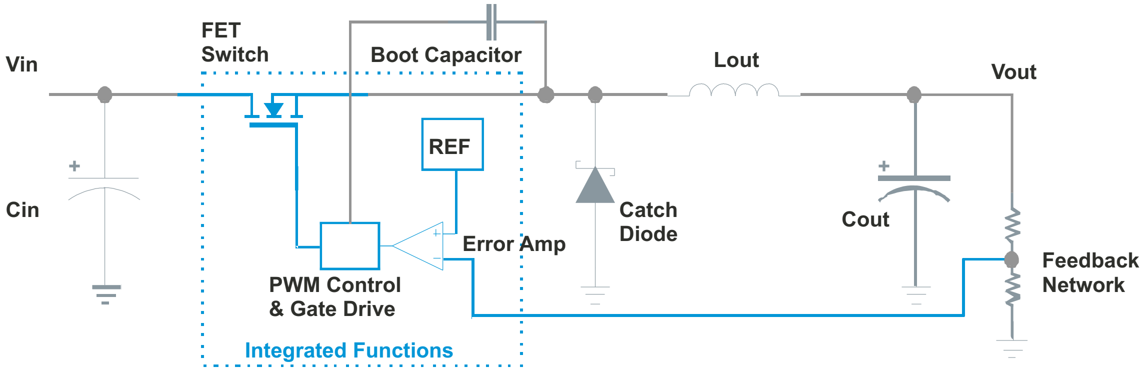

**Figure 1. Buck Topology**

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When the FET switch is on, the voltage across the inductor is Vin – Vout, and the current through the inductor increases at a rate of di/dt = (Vin – Vout) / L. When the switch is off, the inductor voltage reverses to keep the inductor current continuous. Assuming that the voltage drop across the diode is small, the inductor current ramps down at a rate of di/dt = (Vout) / L. The steady-state load current is always carried by the inductor during both the on and off times of the FET switch. The average inductor current is equal to the load current, and the peak-to-peak inductor ripple current is Il p-p = ((Vin – Vout) D) / (fsw × L). Where Vin is the input voltage, Vout is the output voltage, the duty cycle D= Vout / Vin, fsw is the switching frequency and L is the inductor value.

## 2 Inverting Buck-Boost Topology

Compare the above operation to that of the buck-boost topology shown in Figure 2.

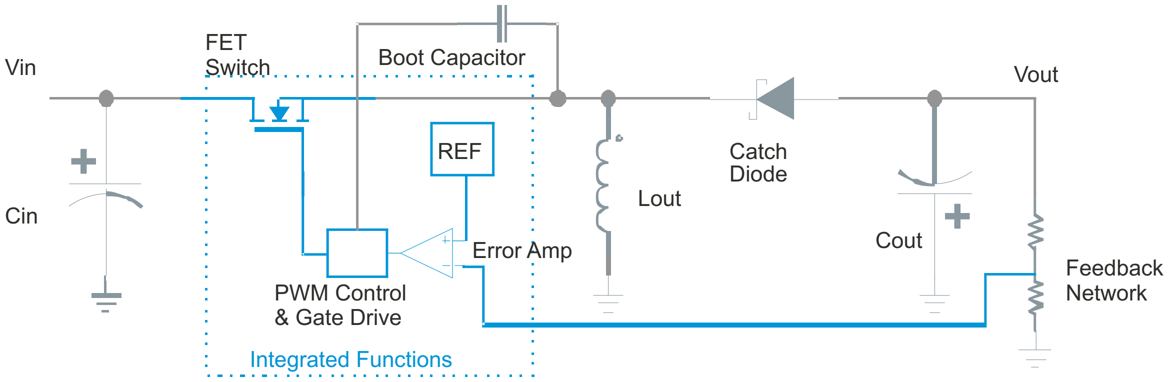


**Figure 2. Inverting Buck-Boost Topology**

The inductor and catch diode have switched places relative to the buck converter of Figure 1. Also, the output capacitor is reversed in polarity as the output voltage is negative. During operation, when the FET switch is on, the voltage across the inductor is Vin, and the current ramps up at a rate of di/dt = Vin / L. While the FET switch is on, all of the load current is supplied by energy stored in the output capacitor. When the FET switch turns off, the inductor reverses polarity to keep the inductor current continuous. The voltage across the inductor is approximately Vout and the inductor current decreases at a rate of di/dt = –Vout / L. During the off-time, the inductor supplies both the current to the load and also current to replenish the energy lost by the capacitor during the on-time. So, for the buck-boost circuit, the average inductor current is Il = Iout / (1 –D), and the peak-to-peak inductor current is Il p-p = (Vin × D)/(Fsw × L). The duty cycle D is approximately D = Vout / (Vout - Vin). These basic differences in circuit operation are important when using the TPS5430 as a buck-boost converter.

## 3 Design Considerations

Consider the circuit of Figure 3. In this design, the TPS5430 is designed as an inverting buck-boost converter with a 15-V input voltage and a –5-V output voltage. The design equations are presented in simplified form with the semiconductors idealized and other component losses neglected. To implement the buck-boost topology of Figure 2, connect the TPS5430 GND pin to Vout and connect the positive terminal of the output capacitor to the Vout return, which is the circuit ground.

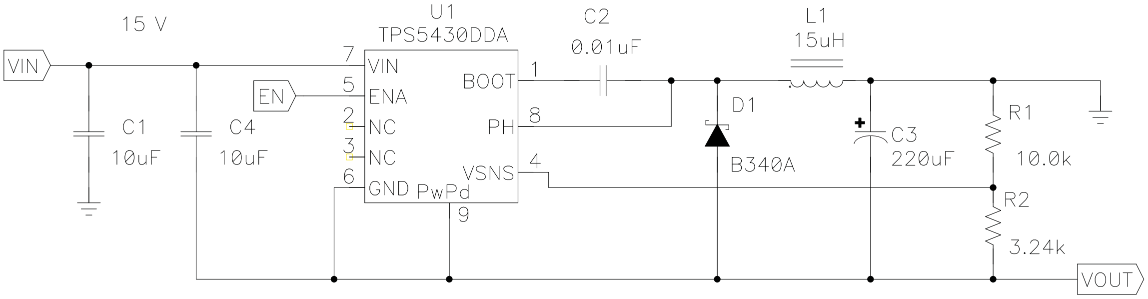


**Figure 3. TPS5430 Buck–Boost Application**

The input voltage across the device VIN pin to GND is now Vin – Vout, or 15 – (–5) = 20 V.

The operating duty cycle is:

D = Vout / (Vout – Vin) = –5 / (–5 – 15) = 0.25

The average inductor current is:

Il avg = Iout / (1-D)

The average output current cannot exceed the TPS5430 rated output of 3 A, so the available load current is reduced by a factor of 1 – D. For this design, the maximum available dc load current is:

3 × (1 – D) = 2.25 A

Also, the inductor ac ripple current should be kept small for several reasons. The peak inductor current is the average inductor current plus one-half the peak-to-peak ac current. This must be below the internal current limit of 4 A. The inductor ac ripple current also determines the dc output current below which the circuit begins to operate in the discontinuous conduction mode. This point is when the dc output current is equal to one-half the peak-to-peak ac current. This circuit is designed to operate in the continuous mode; therefore, the inductor ripple current should be less than 2 times the minimum output current. In general, this is a more severe restriction than the current limit. Additionally, the ripple current contributes significantly to the output voltage ripple. Lower inductor ripple currents provide cleaner output voltages.

For the inverting buck-boost converter, there are significant operating differences between discontinuous and continuous mode operation. Designs that are stable in the discontinuous mode of operation often will become unstable when increased load current causes them to operate in the continuous mode as the feedback loop now contains a right-half-plane zero. This example is designed to be stable in continuous conduction mode, and should be operated in that mode. The inductor value is chosen so that the converter will work in the continuous conduction mode at any output above 0.25 A. If the load current drops below 0.25 A the output will continue to regulate and remain stable in this design.

For this design, the inductor value is calculated based on maintaining continuous conduction with a minimum load of 250 mA. The maximum switch current is 3 + (0.500 / 2) = 3.25 A, which is below the 4-A minimum current limit of the TPS5430; the minimum inductor size is given by:

Lmin = (Vin × D) / ( Fsw × 2 × Iomin) = (15 × 0.25) / (500000 × 2 × 0.25) = 15 µH

Choose the inductor so that RMS and saturation current ratings are not exceeded. The peak current of 3.25 A should be lower than the saturation current. The RMS current is given by:

Ilrms = sqrt( Ilavg ^2 + (1/12 × (Ilp-p ^ 2)) = 3.003 A

Choose the output capacitor so that the circuit will work well with the internal compensation of the TPS5430. The internal compensation for the TPS5430 contains an integrator pole at the origin and two additional poles and zeros. These are located at the frequencies shown:

Fint = 2165 Hz

Fz1 = 2170 Hz

Fz2 = 2590 Hz

Fp1 = 24 kHz

Fp2 = 54 kHz

The capacitor value is chosen based on the output inductor so that the LC resonant frequency is situated near in frequency to the internal zeros of the internal compensation. The LC resonant frequency should be at or just above the Fz2 frequency. The ESR of the output capacitor then is chosen so that the ESR zero is located near (+/-10 kHz) to the first internal pole in the compensation network. For this circuit, the output capacitor is a 220-μF POSCAP with an ESR of 40 mΩ. The resultant LC resonant frequency and ESR zero are:

$$Flc = 1 / (2\times\pi\times \sqrt{(L\times C)}) = 2770\ \text{Hz}$$

$$Fesr = 1/ (2\times\pi\times C\times Resr) = 18\ \text{kHz}$$

This assures stable operation with an optimal closed-loop crossover frequency.

On the input, be sure to use both a bypass capacitor from Vin to ground (C1) and from Vin to Vout (C4). The bypass from Vin to Vout is across the device voltage input. These can be of equal value and should meet the ripple current and voltage rating of the circuit.

The buck-boost circuit shown in Figure 3 is available as an evaluation module. See the TPS5430 product folder or send an e-mail to tps5430buckboost@ti.com to request an evaluation module.

## 4 Circuit Performance

The performance characteristics of the circuit are depicted in Figure 4 through Figure 8. All performance data is for an ambient temperature of 25°C. The measured closed-loop response is shown in Figure 4. The closed-loop crossover frequency is approximately 20 kHz and the phase margin is 59 degrees.

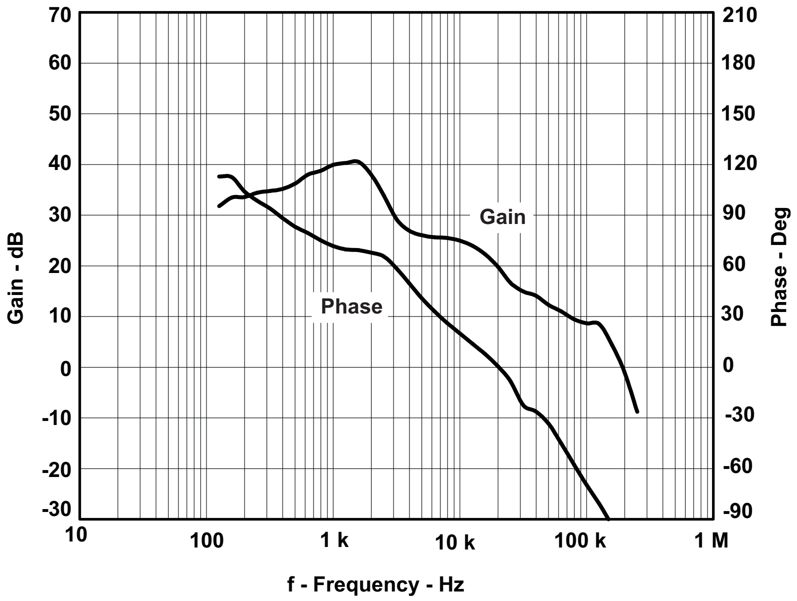
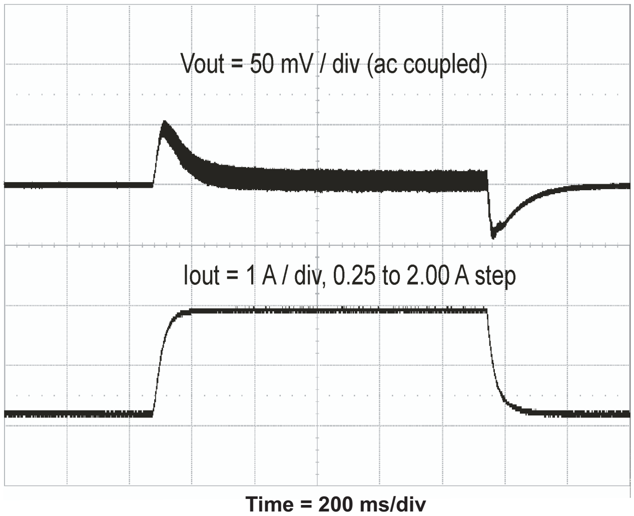


Figure 4. Closed Loop Response

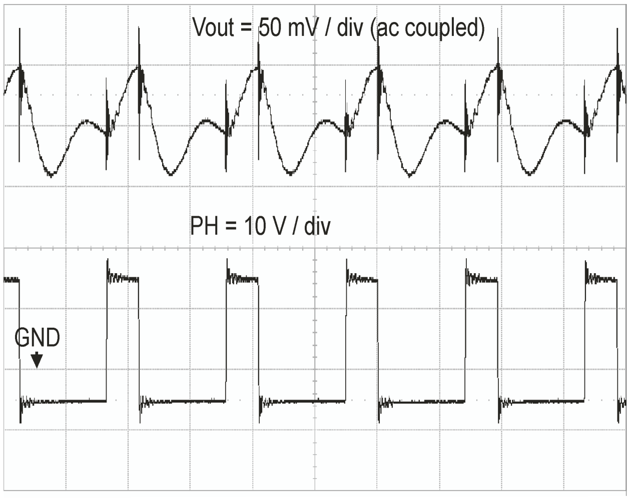
The output voltage response to a load transient is shown in Figure 5. The output current step is from the minimum current of 0.25 A to 2 A then back to 0.25 A. The peak-to-peak voltage deviation in response to the step load change is ±50 mV.



**Time = 200 ms/div**

**Figure 5. Transient Response**

Output voltage ripple and PH node waveform is shown in Figure 6. Note that the PH node switching waveform varies from Vin to Vout, or from 15 V to –5 V. The ground reference line is indicated in the figure. Also observe that the output voltage ripple does not show the linear ramp characteristic typical for the buck converter. In the buck converter, the average inductor current is delivered to the load while the ac portion is shunted to ground through the output filter capacitor. The primary component of the ripple voltage is the ac ripple current times the esr of the output capacitor, resulting in a waveform resembling a ramp that rises during the FET with on time and falls during the switch-off time. For the inverting buck-boost converter, the output capacitor supplies the load current during the switch-on time, and is recharged during the switch-off time. This charge and discharge cycle is superimposed with the ac ripple current to create a more complex ripple current as shown in Figure 6. Remember that the output voltage is negative; so, the positive portions of the waveform represent the output going less negative or the discharge portion of the cycle.



**Time = 1 μs/div**

**Figure 6. Output Voltage Ripple and PH Node Voltage**

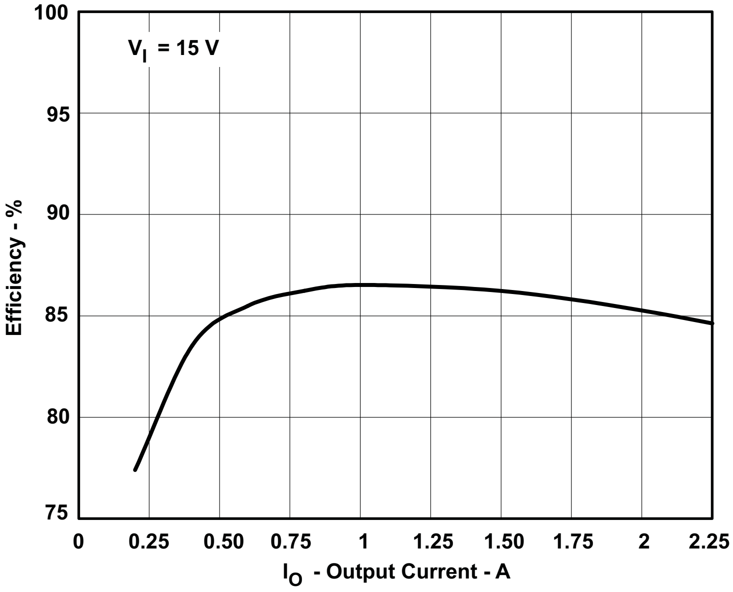


**Figure 7. Efficiency**

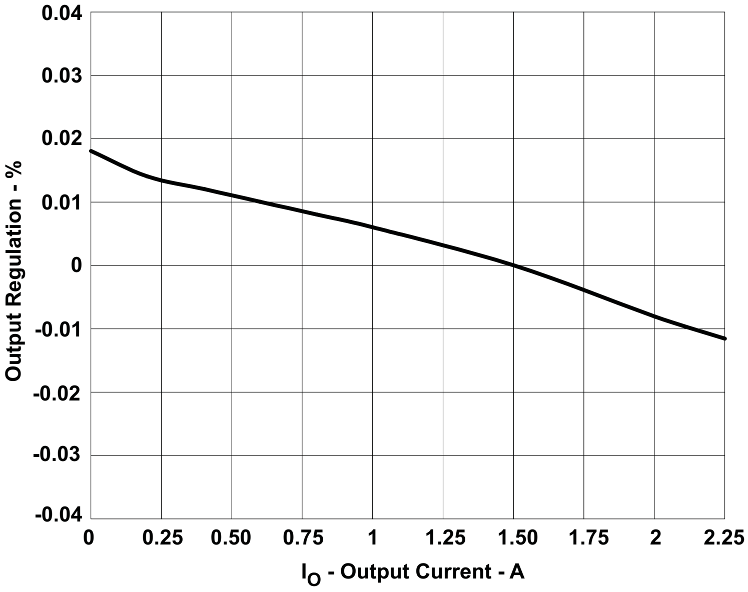


**Figure 8. Load Regulation**

The efficiency curve is shown in Figure 7. The low on-resistance of the internal FET switch makes high efficiency of 87 percent maximum possible for this design. The output voltage variation with respect to load current is shown in Figure 8. Note the tight voltage regulation across the entire load current range of which this circuit is capable.

## 5 Conclusion

The TPS5430 can be used to generate a negative output voltage from a positive input voltage by configuring the circuit as a buck-boost design. The circuit design is straight-forward, but remember these important points. The output current is less than the average inductor current by a factor of 1-D; thus, the available output current will be less than the device rating. The output voltage is negative and is available at the device ground pin; so, the effective voltage across the input of the device is Vin – Vout. This difference must not exceed the input voltage rating of the device. Make sure not to tie the ground of the device or the exposed PowerPAD™ package to the system ground.

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