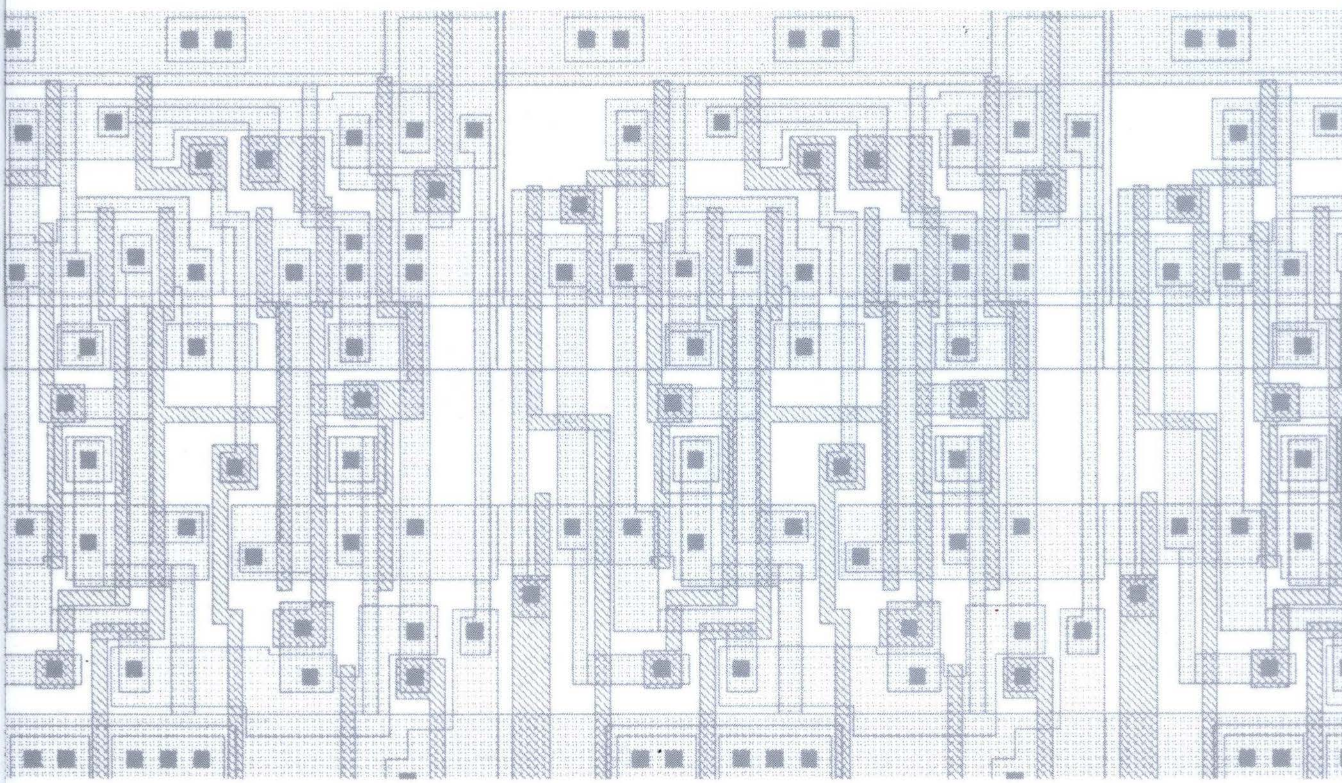
CATALYST
SEMICONDUCTOR, INC.

1988 DATA BOOK



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President's Message *January 1988*

Dear Customer,

Catalyst Semiconductor is a company founded in 1985, whose objective is to provide innovative solutions to integrated circuits utilizing non-volatile memory.

Our long term strategic alliances with major semiconductor manufacturers give us the credibility and stability to offer quality products at competitive prices in high volumes. We maintain strict quality controls over our foundries to guarantee the high quality and reliability of our products.

Our worldwide sales, marketing, and applications network is committed to support your requirements. Our pledge is to be partners in innovation with our customers. It is our charter to be leaders in new product design and introductions.

B.K. Marya

President & Chairman

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Catalyst Semiconductor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

LIMITED WARRANTY

Devices sold by Catalyst Semiconductor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Catalyst Semiconductor, Inc. makes no warranty, express, statutory, implied, or by description, regarding the information set forth herein or regarding the freedom of the described devices from patent infringement.

Catalyst Semiconductor, Inc. makes no warranty of merchantability or fitness for any purpose. Catalyst Semiconductor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice. Catalyst Semiconductor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Catalyst Semiconductor, Inc. product. No other circuits, patents, licenses are implied.

CATALYST SEMICONDUCTOR PRODUCT FAMILY

NVRAMs

Parallel

- CAT22C10 /I
- CAT22C12 /I

Serial

- CAT24C44 /I

EEPROMs

Serial

- CAT93C46
- CAT93C46I
- CAT59C11
- CAT59C11A
- CAT59C11I
- CAT35C102
- CAT35C202
- CAT35C104

Parallel

- CAT28C16A /I
- CAT28C17A /I
- CAT28C64A
- CAT28C256

EPROMs

OTPs

- CAT2764A
- CAT27128A
- CAT27256
- CAT27512

CMOS

- CAT27C210
- CAT27HC256

SRAMs

CMOS

- CAT71C88
- CAT71C256
- CAT71C256L

MICROCOMPUTERs

SMART CARD MICROCOMPUTERs

- CAT62C580
- CAT62C780

ASEED™

CUSTOM

- 8-BIT MICROs
- Parallel & Serial EE CORES
- EPROM ARRAYS
- SRAM CELLS
- RF/ANALOG
- LOGIC

ASEED™ indicates application-specific EE devices.

The ' /I ' indicates industrial temperature range parts.

TABLE OF CONTENTS

CATALYST RELIABILITY AND QUALITY ASSURANCE

A commitment to outstanding Quality and Reliability is an integral part of the Catalyst corporate policy. This is embodied in a comprehensive quality program which is extensively documented and structured to meet the highest standards of the most discriminating customer. This program assures quality at all phases of the production process and provides for the prevention and ready detection of discrepancies and for timely and positive corrective action. The quality and reliability programs utilized at Catalyst can be divided into the following areas:

1) Design-in quality and reliability

2) Document Control

3) Incoming inspection

4) Material Traceability

5) In-Line Inspection

6) Subcontractor Control

7) Comprehensive qualification programs

8) Ongoing monitors

9) Thorough production testing

10) Continued quality and reliability improvement

11) Customer Service

By definition, quality is conformance to specification, whether process or procedures, electrical or mechanical, customer or Catalyst Semiconductor, Inc. Similarly, reliability is continued conformance to specification. Therefore, it is necessary for the Quality and Reliability group to be involved in all phases of the design and manufacturing process.

1) Designed in Quality and Reliability

The Catalyst Q/R program begins at the process design as well as circuit design level.

For example:

- Parametric margins for device operations are above and beyond those necessary to simply meet specification.

- Special attention is paid to electrostatic discharge protection (ESD). Every pin is designed to withstand 2000V minimum (Human Body model).

- Attention is also paid to layout and process sensitive problems such as CMOS latch-up. Every device must meet rigid standards and test conditions well beyond those anticipated in normal operation.

- Reliability failure rate and process parameter requirements for qualification are clearly documented for all products at or prior to product conception thereby helping to assure the highest standards of quality and reliability. These standards must be demonstrated at qualification. The involvement of quality and reliability personnel as part of the development team assures that a product manufactured under state-of-the-art technology will continue to be a useful product well into the future.

2) Document Control

The document control group maintains control over all manufacturing specifications, lot travelers, procurement specification and drawings, reticle tapes, and test programs.

They also are charged with the generation and translation of customer specification requirements into Catalyst internal travelers, specifications, and procedures.

Any and all changes to specifications are subject to approval by Engineering and Manufacturing managers.

See Fig. 1 block diagrams on document control.

RELIABILITY AND QUALITY

3) Incoming Inspection

For all purchased materials the manufacturer is required to maintain a high product quality level. The manufacturer's facility must also meet the requirements of Catalyst QC and is subject to periodic audit to verify that the manufacturer is following the required quality procedures and keeping proper records. All manufacturers must be qualified before their aterials may be used in production.

Incoming inspection is performed on each lot of material, with the individual purchasing specification for that material as a standard to determine defective mataerial. Those lots that do not meet the standard are rejected and returned to the manufacturer. The manufacturer must then analyze and report on the failures, stating what corrective action is being performed to correct the problem. Those actions are reviewed by Catalyst and, upon approval, are accepted by Catalyst for implementation by the manufacturer.

4) Material Traceability

Catalyst maintains a complete history of production lots, from incoming to outgoing inspection. Incoming material is inspected and assigned a lot number that is referenced on production travelers thereby identifying that material throughout the production process. In addition, all assembled units are marked with a lot number which provides the neccessary traceability to determine any information about the history of the component or any material used to build that component.

5) In-Line Inspection

Manufacturing facilities used to build Catalyst products are carefully monitored and audited for adequate QC and QA procedures and methods.

Among the myriad of process and quality control procedures that must be in operation the following is a sample:

- Incoming inspection of all materials such as chemicals, wafers, masks, and piece parts.

- Vendor qualification and monitoring data.

- Calibration and maintenance procedures of fab and test equipment.

- Environmental controls over temperature, relative humidity, particle content in clean air facilities, wafer resistivity and bacteria content in deionized water.

- Training procedures for operators. - Process monitor procedures, frequency and sampling plans.

- $\overline{X}$ and R charts and evidence of corrective action response capability.

Experience has proven that such close control of operators, equipment, and environment is highly effective towards improved quality and increased yields.

Fig. 2 shows typical inprocess QC flows utilized by Catalyst vendors to control critical process steps in wafer fab, assembly, and test.

6) Subcontractor Control

All of Catalysts subcontractor facilities and procedures must be qualified before manufacturing is allowed to begin. Every product manufactured must meet Catalyst's quality standards. In preparation for manufacturing for Catalyst, the subcontractor is instructed to use only equipment, materials, conditions, and quality control procedures which are specified or approved by Catalyst. Based on Catalyst instructions, the subcontractor develops detailed manufacturing standards which are approved or qualified by Catalyst. During manufacturing, Catalyst provides the subcontractor with technical and quality control support. The subcontractor must submit process quality control reports periodically. In addition the subcontractors facility is subject to periodic audit by Catalyst, and the products are checked regularly against Catalyst quality standards.

A summary of the relationship between Catalyst and the subcontractor is shown in Fig. 3.

RELIABILITY AND QUALITY

7) Comprehensive Qualification Programs

Catalyst's extensive Qualification Program is the backbone of the quality program. Device, process, and package qualification programs are thoroughly documented and required failure rate criteria are established as part of the development cycle. Only engineering samples are allowed to be delivered without meeting the qualification criteria.The qualification programs have their basis and are in accordance with MIL-STD-883C.

Historically, memory products have been the test vehicle for bringing new technology to the marketplace. During qualification and subsequent reliability monitor program, the memory devices are thoroughly analyzed for failure mechanisms and the process technology altered to eliminate them. After completion of this process the technology is able to be transferred to other types of devices and products, i.e., the smart card micro.

For example, the following is a list of reliability tests necessary to be performed on the qualification of a new wafer fab technology for EEPROMs. Samples from the first 5 wafer lots must pass these tests:

1) 125° C operating life, 1000 hrs.
2) 150° C data retention storage,1000 hrs. after 10K cycles.
3) Endurance cycle/bake @ 150° C.
4) Temp. cycle, -65 /+150° C, 1000 cycles
5) High voltage lifetest, 1000 hrs.
6) E.S.D. (1.5K /100pf), 2000 volts all pins
7) Latch-up sensitivity, 100 mA/pin

It is from these tests that information on infant mortality, long term failure rates, and associated failure mechanisms is determined. The data from these tests are published in a reliability report and made available to our customers.

Similarly, samples of a new package technology or facility must undergo their own extensive qualification to assure the highest standards in mechanical integrity.

8) Ongoing Monitor Program

While initial qualification is a key step in product introduction, it would be meaningless if products were not monitored throughout their product life. Each quarter production lots are randomly sampled for the monitor program and submitted to many of the same comprehensive tests used for initial qualification. As in the qualification process, any device failures are carefully analyzed using bench testers, microscopes, and S.E.M. to determine failure mechanisms and their importance to the process and the device. In this way, Catalyst reliability engineers can develop extensive data on long term problems that will quickly and accurately determine why a product may have failed and generate the necessary feedback to the applicable engineering groups.

An example of the monitor program for EEPROM technology:

1) 125° C operating life, 1000 hrs.
2) 150° C data retention storage, 1000 hrs. after 10K cycles.
3) Endurance cycle/bake @ 150° C.
4) Temp cycles, 1000 cy, -65 /150° C.
5) H.A.S.T. test, 24 hrs., +5V, 94% R.H., 38 psi. *
6) Pressure Pot, 96 hrs. *

(* Plastic package only)

As in qualification, reliability failure rate goals are clearly documented and results are carefully scrutinized to ensure goals are met.

9) Thorough Production Testing

Every device manufactured by Catalyst must be thoroughly tested for electrical functionality prior to shipment. Test programs are validated prior to qualification to ensure the required limits, as deter-

RELIABILITY AND QUALITY

mined in the data sheet for each product, are being met. Not only are the operating specifications carefully scrutinized, but also any and all reliability requirements must be checked. See Fig. 4.

For example, one of the most important specifications for EEPROMS is the ability to perform 10,000 write/erase cycles and have 10 years data retention. Catalyst has taken the position that all outgoing products will meet specifications including long term reliability requirements. Therefore, 100 percent of all units are tested for reliability during the test flow. These tests are specifically designed to eliminate reliability rejects from reaching the customer as well as infant mortality type rejects.

10) Continued R/QA Improvement

In order to achieve its goal as an industry leader in reliability and quality, Catalyst is continually pushing improvements in design and process. Before any changes are implemented in a qualified technology, test chips are generated and again rigorously tested. If an improvement in process or design is to be implemented, it must again be qualified prior to shipment of any revenue parts. The same is true for any significant change in package related materials, facility, or methods.

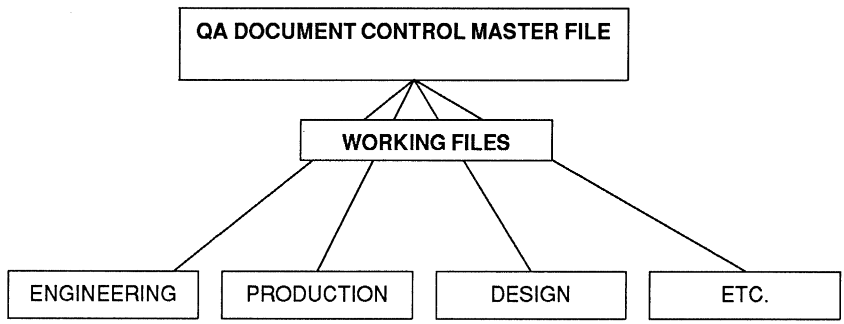
11) Customer Service

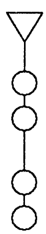
Customer feedback and problems are continually monitored and analyzed with failure analysis reports written and distributed to applicable engineering groups for immediate corrective action. Sometimes problems are related to the application, rather than the IC itself, and corrective measures can be suggested.

Customer service activities also include the collection, evaluation and feedback of quality-related data from customers. It is Catalyst's intent to be continual aware of how it can improve the quality and reliability of all Catalyst products.

At Catalyst, we believe in satisfied customers.

CATALYST DOCUMENT CONTROL SYSTEM Fig. 1





- Specification written or data collected for engineering change of existing specification
- ECN number issued by document control.
- ECN circulated and approved by manufacturing, engineering, and R/QA managers.
- Approved ECN returned to document control.
- Document control revises master file and generates new documents to pertinent working files.

IN-PROCESS QC FLOW CHART Fig. 2A

WAFER FABRICATION (3 µm SI Gate CMOS

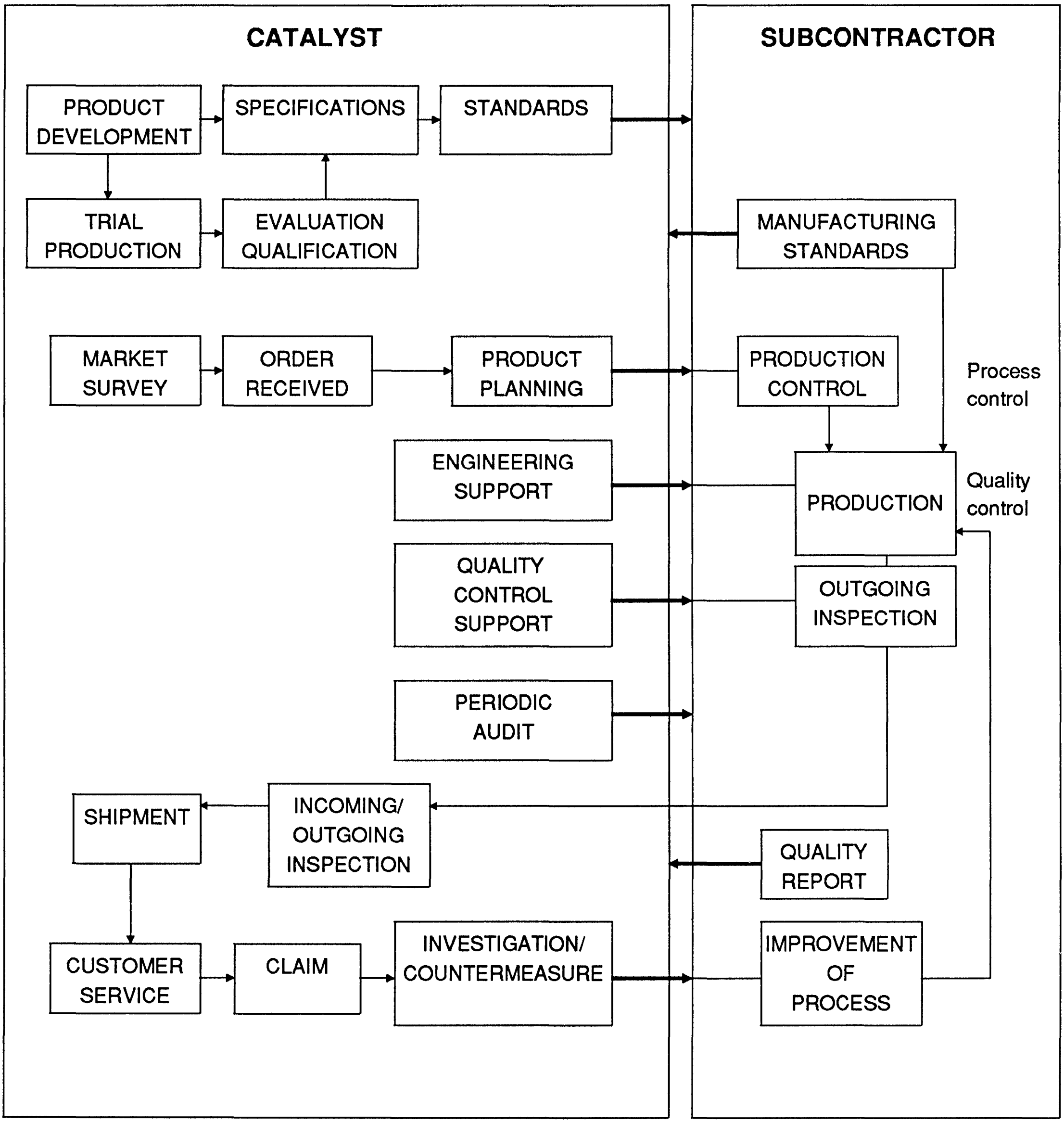
FLOW	PROCESS	QC ITEM	SAMPLING METHOD
▽	STARTING MATERIAL		
○	P-WELL FORMATION	THICKNESS RESISTIVITY	1 WAFER/LOT 1 WAFER/LOT
○	ACTIVE AREA FORMATION	CRITICAL DIMENSION	2 WAFERS/ LOT
○	FIELD FORMATION	THICKNESS	1 WAFER/CHARGE
○	GATE FORMATION	THICKNESS RESISTIVITY CRITICAL DIMENSION	1 WAFER/CHARGE 1 WAFER/CHARGE 2 WAFERS/LOT
○	S/D FORMATION	THICKNESS RESISTIVITY	1 WAFER/10 LOTS 1 WAFER/ 10 LOTS
○	INTERLAYER FORMATION	THICKNESS P-CONCENTRATION	1 WAFER/ LOT 1 WAFER/ LOT
○	METAL FORMATION	THICKNESS	2 WAFERS/ 10 LOTS
○	FINAL PASSIVATION FORMATION	THICKNESS	2 WAFERS/ CHARGE
○	PARAMETER CHECK	DEVICE PARAMETER	3 WAFERS/ LOT
○	ELECTRICAL TEST	ELECTRICAL CHARACTERISTICS	100%

IN-PROCESS QC FLOW CHART Fig. 2B

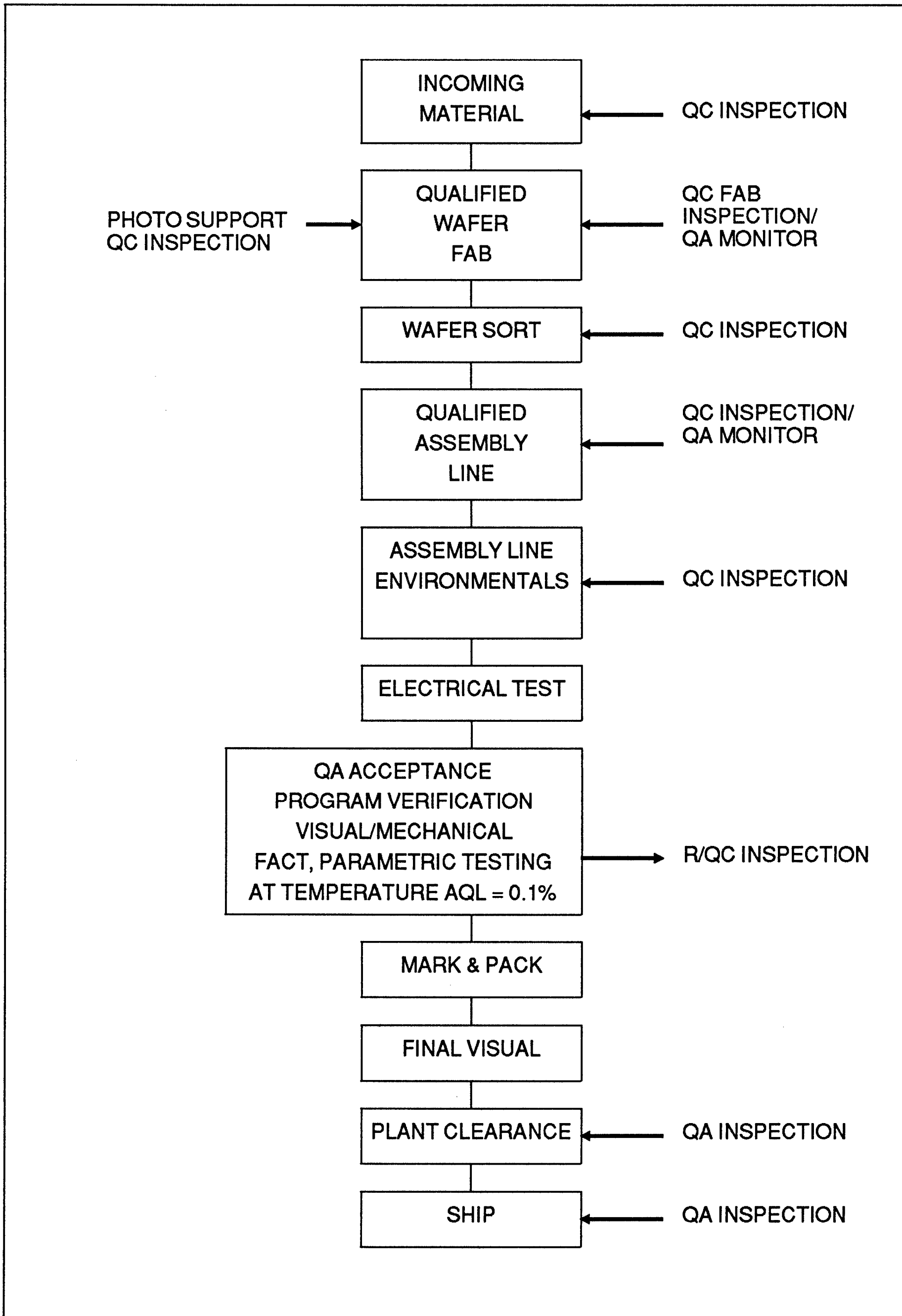
ASSEMBLY & TESTING PROCESS (PLASTIC DIP)

FLOW	PROCESS	QC ITEM	SAMPLING METHOD
○	SCRIBING		
○	CHIP VISUAL	VISUAL	100%
○	DIE BONDING	VISUAL	TWICE/SHIFT/MAC*
○	WIRE BONDING	BOND STRENGTH VISUAL	ONCE/SHIFT/MAC ONCE/SHIFT/MAC
○	VISUAL INSPECTION	VISUAL	100%
○	MOLDING		
○	VISUAL INSPECTION	VISUAL	100%
○	SOLDER PLATING	VISUAL	PER LOT
○	LEAD CUTTING/FORMING	VISUAL	PER LOT
○	MARKING	VISUAL	100%
○	ELECTRICAL TEST	ELECTRICAL CHARACTERISTICS	100%
			* MAC means machine
◇	OUTGOING INSPECTION		
○	PACKING/SHIPPING		

SUBCONTRACTOR CONTROL SYSTEM Fig. 3



QA FLOWCHART Fig. 4



NVRAMs

1

CAT22C10, CAT22C10 I [Industrial Temperature]
256-BIT (64X4) NON-VOLATILE CMOS STATIC RAM

DESCRIPTION

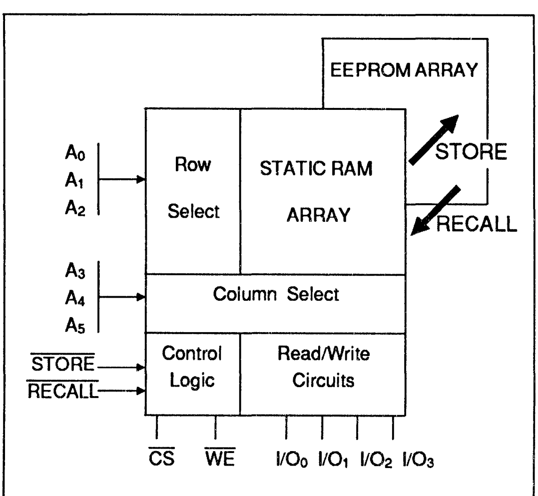
The Catalyst CAT22C10 Non-Volatile Random Access Memory (NVRAM) is a 256-bit device with a 64x4 organization. It features fully static CMOS circuitry for very low power consumption. The active current is 40mA. and the standby current is 30μA.

An internal EEPROM array provides bit-by-bit backup for the static RAM array. Store operations write data from the RAM array to the EEPROM array. Recall operations write data from the EEPROM array to the RAM array.

Data retention for each store cycle is specified for over 10 years, and over 10,000 store operations can be performed reliably. Unlimited recall operations, and read and write operations to the RAM are further specified.

The CAT22C10 has internal false store protection circuitry, which prohibits any store operation for V_{CC} less than 3.5 volts (typically) to ensure the integrity of the EEPROM data. Other internal circuitry performs an automatic recall operation upon V_{CC} power-up.

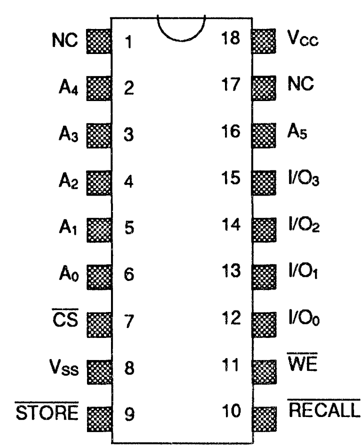
BLOCK DIAGRAM



FEATURES

- CMOS technology - completely static operation
- Low current consumption (standby 30μA max., operation 40mA. max.)
- Single power supply (+5V ±10%)
- RAM access time 200ns, and 300ns.
- Fully TTL and CMOS compatible
- JEDEC standard 18-pin 300-mil package
- Write protect circuit to preserve data on Power-up and Power-down
- Automatic recall on power-up
- 3-state output
- Short store pulse -200ns
- Short recall pulse -300ns
- False store protection below 3.5V operation level
- 10,000 non-volatile store cycles per bit

PIN CONFIGURATION



(TOP VIEW)

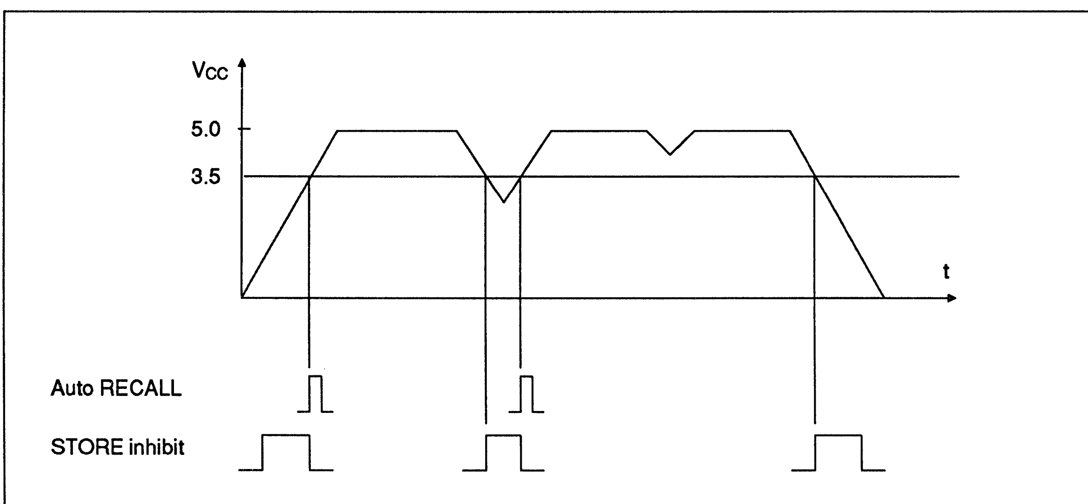
A_0-A_5	Address	$\overline{STORE}$	Store
I/O_0-I/O_3	Data in/out	V_{CC}	+5V
$\overline{WE}$	Write enable	V_{SS}	Ground
$\overline{CS}$	Chip select	NC	No connect
$\overline{RECALL}$	Recall		

MODES OF OPERATION

Input				Input/Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$		
H	-	H	H	Output high impedance	Standby
L	H	H	H	Output data	RAM Read
L	L	H	H	Input data	RAM Write
-	H	L	H	Output high impedence RECALL	(EEPROM→RAM)
H	-	L	H	Output high impedence RECALL	(EEPROM→RAM)
-	H	H	L	Output high impedence STORE	(RAM→EEPROM)
H	-	H	L	Output high impedence STORE	(RAM→EEPROM)

NOTES:

- $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time
- $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 1000ms



MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Temperature under bias	T_{bias}	-40°C to +85°C
Power supply	V_{CC}	-0.3 to +6V
Input voltage	V_{IN}	-0.3 to +6V
Output voltage	V_{OUT}	0.0 to +6V
Output current	I_{OUT}	5mA
Lead temperature (soldering for 10 seconds)		260°C

1

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT22C10 T_A = 0°C to +70°C, CAT22C10I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CCO}	Current consumption (operating)	All input=5.5V, T_A =0°C All outputs unloaded		15	40	mA
I_{CCS}	Current consumption (stand-by)				30	µA
I_{LI}	Input current	$0 \le V_{IN} \le 5.5V$		0.1	10	µA
I_{LO}	Output leakage current	$0 \le V_{OUT} \le 5.5V$		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.4	V
V_{DH}	RAM data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

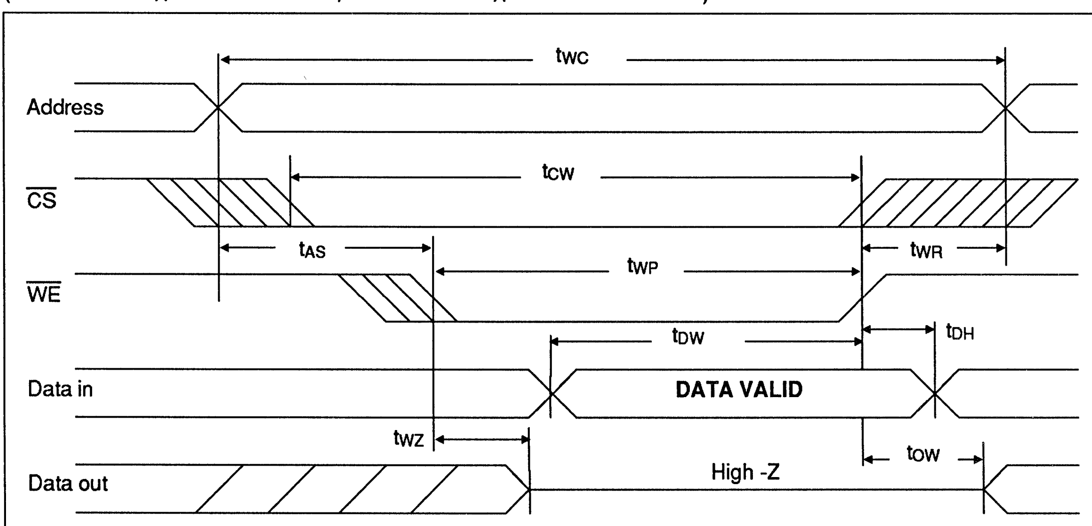
AC CHARACTERISTICS < Write Cycle>

(CAT22C10 T_A = 0°C to +70°C, CAT22C10I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	22C10-20 Min	22C10-20 Max	22C10-30 Min	22C10-30 Max	Units
t_{WC}	Write cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{CW}	CS write pulse width		150		150		ns
t_{AS}	Address set-up time		50		50		ns
t_{WP}	Write pulse width		150		150		ns
t_{WR}	Write recovery time		25		25		ns
t_{DW}	Data valid time		100		100		ns
t_{DH}	Data hold time		20		20		ns
t_{WZ}	Output disable time		10	100	10	100	ns
t_{OW}	Output enable time		10		10		ns

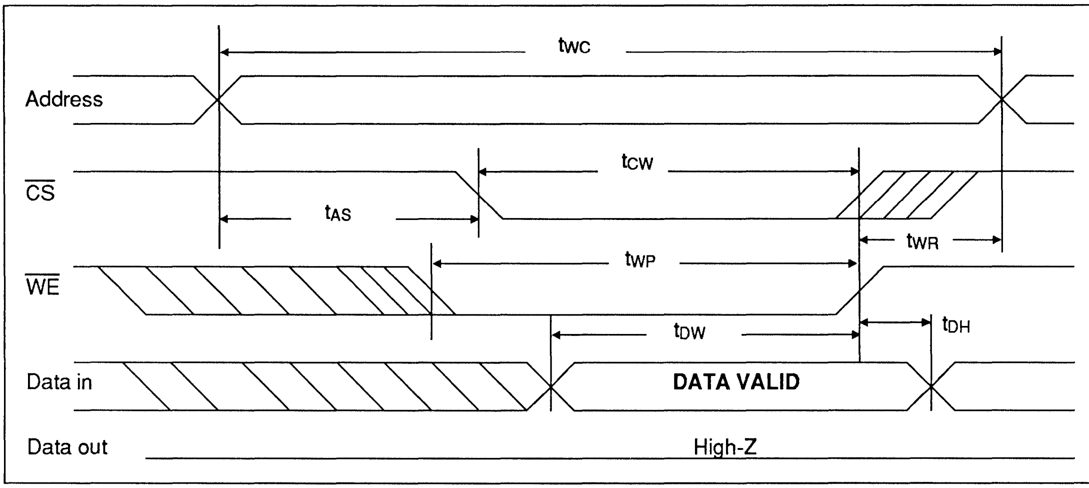
AC CHARACTERISTICS <Write Cycle>

(CAT22C10 T_A = 0°C to +70°C, CAT22C10I T_A = -40°C to +85°C)



AC CHARACTERISTICS <Early Write Cycle>

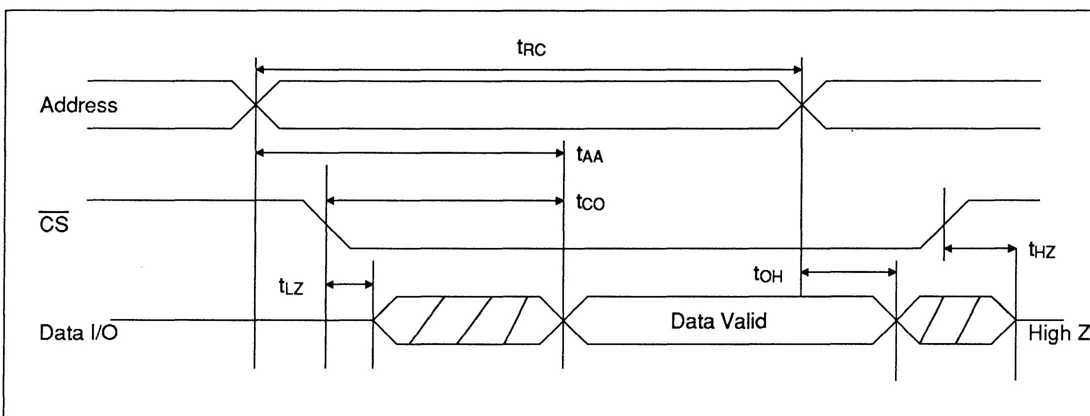
(CAT22C10 T_A = 0°C to +70°C, CAT22C10I T_A = -40°C to +85°C)



1

AC CHARACTERISTICS <Read Cycle>

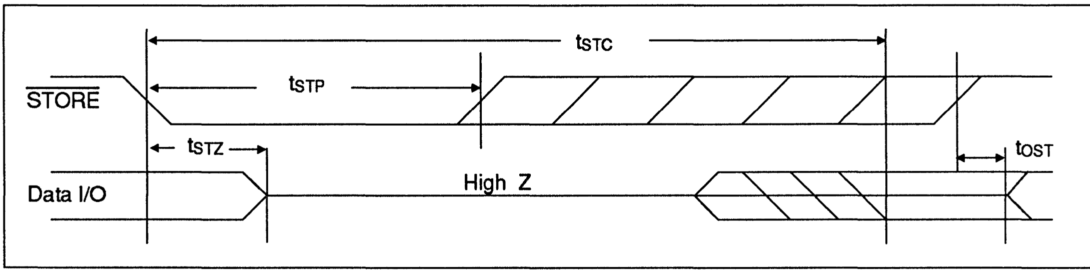
(CAT22C10 T_A = 0°C to +70°C, CAT22C10I T_A = -40°C to +85°C)



Symbol	Parameter	Conditions	22C10-20 Min	22C10-20 Max	22C10-30 Min	22C10-30 Max	Units
t_{RC}	Read cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{AA}	Address access time			200		300	ns
t_{CO}	CS access time			200		300	ns
t_{OH}	Output data hold time		50		50		ns
t_{LZ}	CS enable time		10		10		ns
t_{HZ}	CS disable time		10	100	10	100	ns

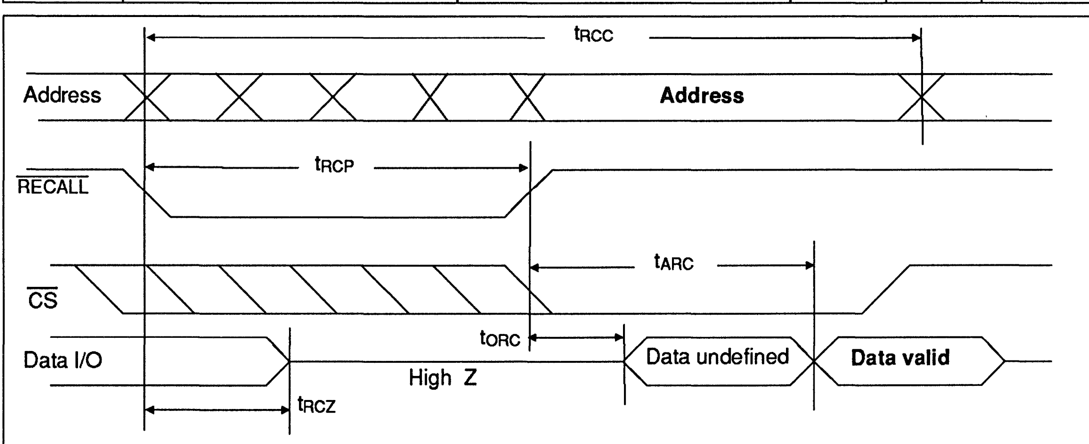
AC CHARACTERISTICS <Store Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{STC}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns
t_{OST}	Store enable time		10		ns



AC CHARACTERISTICS <Recall Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	1400		ns
t_{RCP}	Recall pulse width		300		ns
t_{RCZ}	Recall disable time			100	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1100	ns



DEVICE OPERATION

The configuration of the CAT22C10 allows a common address bus to be directly connected to the address inputs, and the Input/Output (I/O) pins to be connected directly to a common I/O bus if it has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) goes low, the chip is activated. When $\overline{CS}$ is forced high, the chip goes into the standby mode and consumes very little current. With the Non-Volatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0 - A_5), and that byte will be read or written to through the Input/Output pins (I/O_0 - I/O_3).

The Non-Volatile functions are inhibited by holding the $\overline{STORE}$ input and the $\overline{RECALL}$ high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire EEPROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the EEPROM array.

STANDBY MODE

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C10. When a high level is supplied to the $\overline{CS}$ pin, the chip goes into the standby mode. In the mode the chip consumes 99.9% less power and the outputs are put into a high impedance state. Because I_{CCS} is less than 100µA in standby mode, the designer has the flexibility to use this part in battery operated systems.

READ

When the chip is enabled ($\overline{CS}$ = low), the Non-Volatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). The Write Enable ($\overline{WE}$) can put the chip into the read mode when it is held high. In this mode, the data in the Static RAM array may be accessed by selecting an address on the input pins A_0 - A_5. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

WRITE

Like the read mode, with the chip enabled and the non-volatile functions inhibited, the Write Enable ($\overline{WE}$) will select the write mode when taken to a low level. In this mode, the address must be supplied for the byte to be written to. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0 - I/O_3. When these conditions, including the write pulse width time (t_{WP}), are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by setting $\overline{WE}$ = low, inhibiting the Non-Volatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

RECALL

At anytime, except during a store, taking the $\overline{RECALL}$ pin low will initiate a recall operation. This is independent of the state of $\overline{CS}$, $\overline{WE}$, or A_0-A_5. After the $\overline{RECALL}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire content of the EEPROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall (t_{ARC}). After this, any other bytes may be accessed by using the normal read mode.

If $\overline{RECALL}$ is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data. A recall operation is automatically performed upon power-up (low to high transition) of VCC.

The outputs I/O0-I/O3 will go into the high impedance state as long as the $\overline{RECALL}$ signal is held low.

STORE

At any time, except during a recall operation, taking the $\overline{STORE}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{CS}$, $\overline{WE}$ or A_0-A_5. The $\overline{STORE}$ pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{STORE}$ pin may be left low or taken high and the store operations will complete its transfer of the entire contents of the Static RAM array into the EEPROM array within the Store Cycle time (t_{STC}). However, if a store operation is initiated during the write mode, the contents of the addressed Static RAM byte and its corresponding byte in the EEPROM array will be unknown.

During the store operation, the outputs are in a High impedance state. At least 10,000 store operations can be performed reliably. The data which is written into the EEPROM array during a store operation has a data retention time greater than 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C10 has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.5V. This function eliminates the potential hazard of a spurious Store operation being initiated because the system signals are unstable at a low V_{CC}. This function does not affect the ability of external circuitry to intentionally do a Store operation when V_{CC} falls below 4.5V. In fact, it is still important to prevent a potential second initiation of a store operation.

CAT22C12, CAT22C12 I [Industrial Temperature]
1024-BIT (256X4) NON-VOLATILE CMOS STATIC RAM

DESCRIPTION

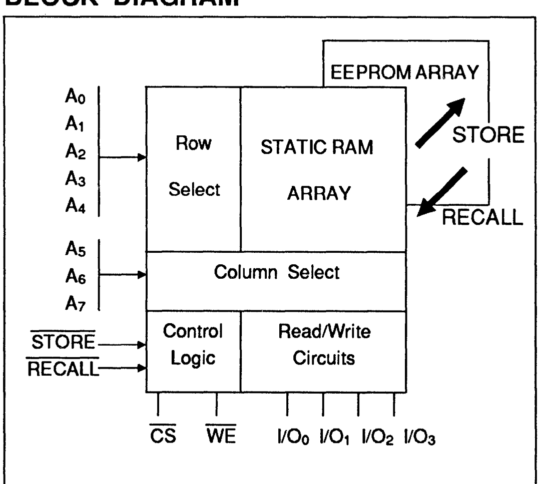
The Catalyst CAT22C12 Non-Volatile Random Access Memory (NVRAM) is a 1024-bit device with a 256x4 organization. It features fully static CMOS circuitry for very low power consumption. The active current is 50mA. and the standby current is 30μA.

An internal EEPROM array provides bit-by-bit back-up for the static RAM array. Store operations write data from the RAM array to the EEPROM array. Recall operations write data from the EEPROM array to the RAM array.

Data retention for each store cycle is specified for over 10 years, and over 10,000 store operations can be performed reliably. Unlimited recall operations, and read and write operations to the RAM are further specified.

The CAT22C12 has internal false store protection circuitry, which prohibits any store operation for V_{CC} less than 3.5 volts (typically) to ensure the integrity of the EEPROM data. Other internal circuitry performs an automatic recall operation upon V_{CC} power-up.

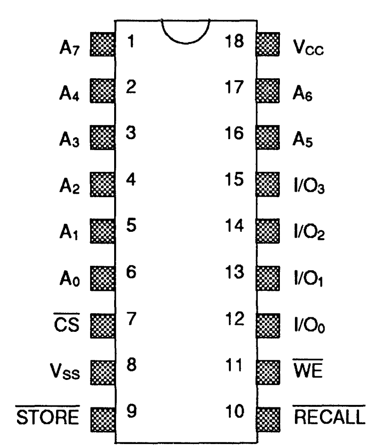
BLOCK DIAGRAM



FEATURES

- CMOS technology - completely static operation
- Low current consumption (standby 30μA max., operation 50mA. max.)
- Single power supply (+5V ±10%)
- RAM access time 200ns, and 300ns.
- Fully TTL and CMOS compatible
- JEDEC standard 18-pin 300-mil package
- Write protect circuit to preserve data on Power-up and Power-down
- Automatic recall on power-up
- 3-state output
- Short store pulse -200ns
- Short recall pulse -300ns
- False store protection below 3.5V operation level
- 10,000 non-volatile store cycles per bit

PIN CONFIGURATION



(TOP VIEW)

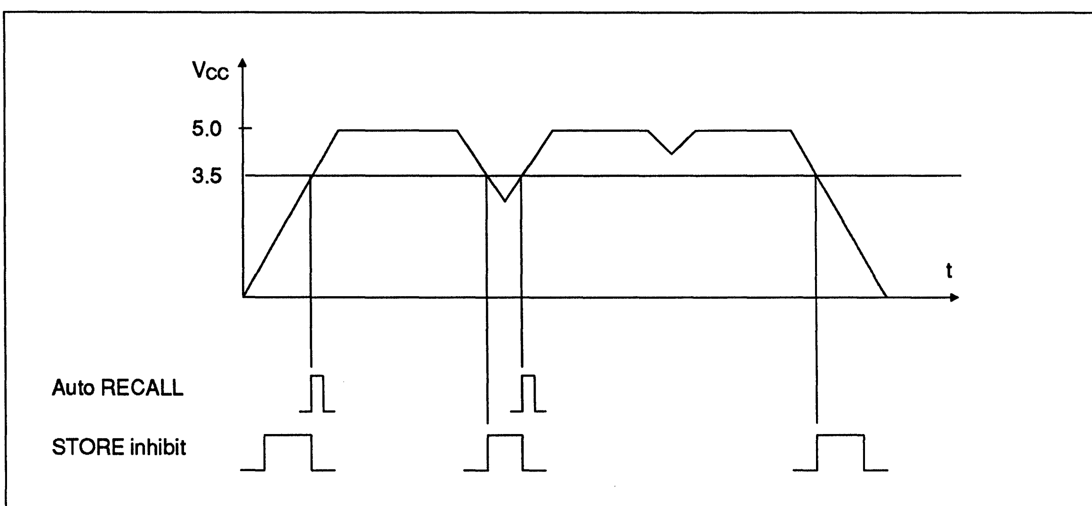
A_0-A_7	Address in	STORE	Store
I/O_0-I/O_3	Data in/out	V_{CC}	+5V
WE	Write enable	V_{SS}	Ground
CS	Chip select	NC	No connect
RECALL	Recall		

MODES OF OPERATION

Input				Input/Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$		
H	-	H	H	Output high impedance	Standby
L	H	H	H	Output data	RAM Read
L	L	H	H	Input data	RAM Write
-	H	L	H	Output high impedence RECALL	(EEPROM→RAM)
H	-	L	H	Output high impedence RECALL	(EEPROM→RAM)
-	H	H	L	Output high impedence STORE	(RAM→EEPROM)
H	-	H	L	Output high impedence STORE	(RAM→EEPROM)

NOTES:

- $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time
- $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 1000ms



MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Temperature under bias	T_{bias}	-40°C to +85°C
Power supply	V_{CC}	-0.3 to +6V
Input voltage	V_{IN}	-0.3 to +6V
Output voltage	V_{OUT}	0.0 to +6V
Output current	I_{OUT}	5mA
Lead temperature (soldering for 10 seconds)		260°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT22C12 T_A = 0°C to +70°C, CAT22C12I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CCO}	Current consumption (operating)	All input=5.5V, T_A =0°C All outputs unloaded		15	50	mA
I_{CCS}	Current consumption (stand-by)				30	µA
I_{LI}	Input current	$0 \le V_{IN} \le 5.5V$		0.1	10	µA
I_{LO}	Output leakage current	$0 \le V_{OUT} \le 5.5V$		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.4	V
V_{DH}	RAM data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

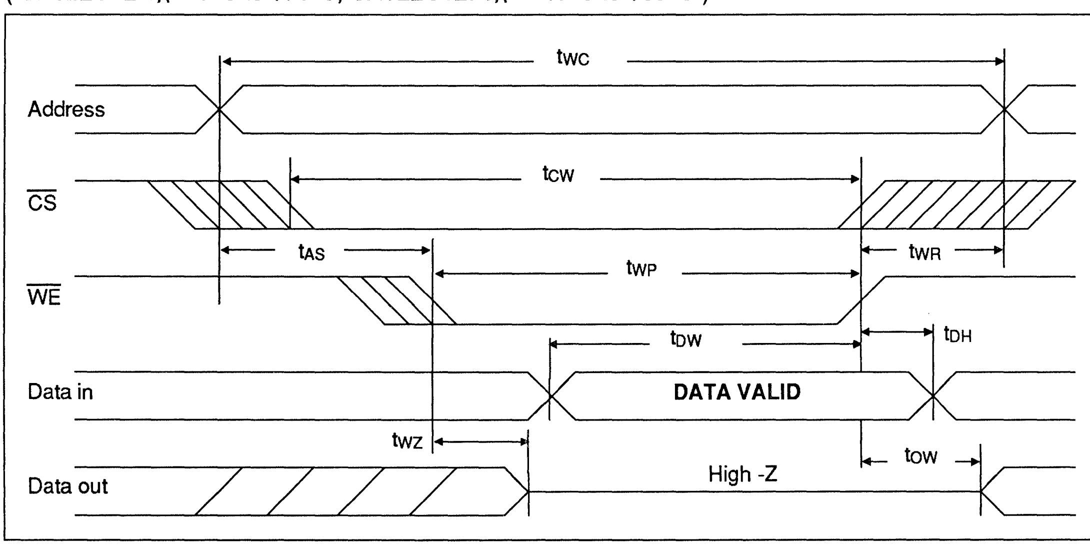
AC CHARACTERISTICS < Write Cycle>

(CAT22C12 T_A = 0°C to +70°C, CAT22C12I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	22C12-20 Min	22C12-20 Max	22C12-30 Min	22C12-30 Max	Units
t_{WC}	Write cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{CW}	CS write pulse width		150		150		ns
t_{AS}	Address set-up time		50		50		ns
t_{WP}	Write pulse width		150		150		ns
t_{WR}	Write recovery time		25		25		ns
t_{DW}	Data valid time		100		100		ns
t_{DH}	Data hold time		20		20		ns
t_{WZ}	Output disable time		10	100	10	100	ns
t_{OW}	Output enable time		10		10		ns

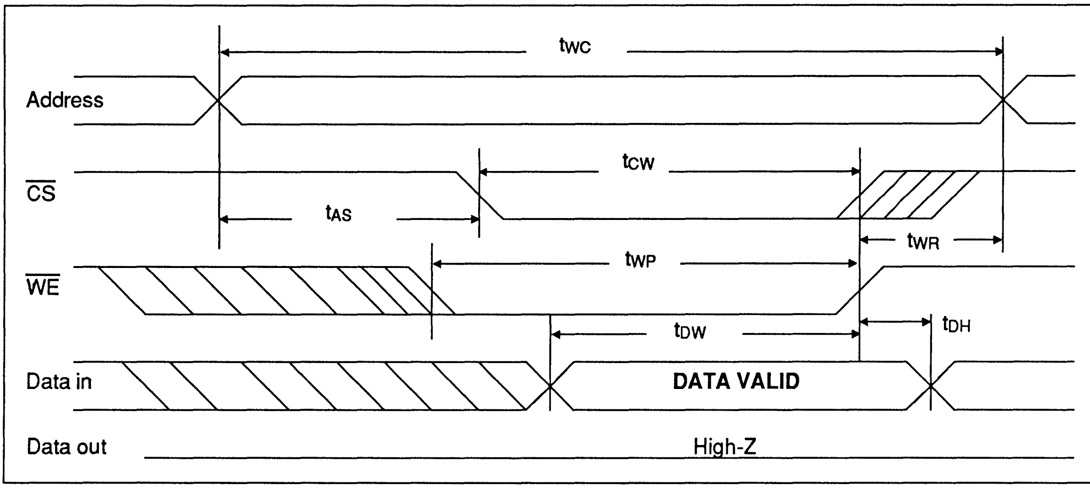
AC CHARACTERISTICS <Write Cycle>

(CAT22C12 T_A = 0°C to +70°C, CAT22C12I T_A = -40°C to +85°C)



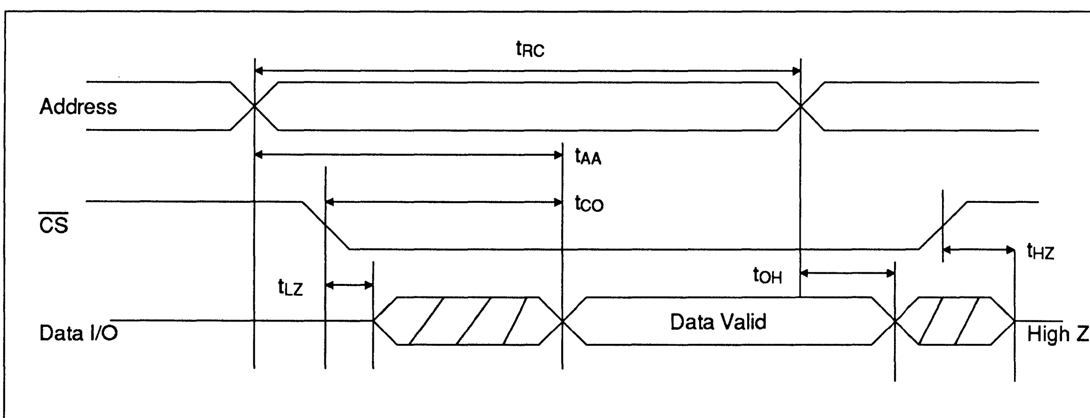
AC CHARACTERISTICS <Early Write Cycle>

(CAT22C12 T_A = 0°C to +70°C, CAT22C12I T_A = -40°C to +85°C)



AC CHARACTERISTICS <Read Cycle>

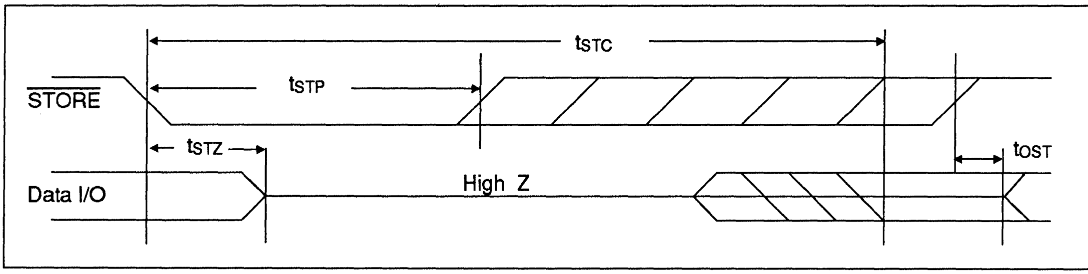
(CAT22C12 T_A = 0°C to +70°C, CAT22C12I T_A = -40°C to +85°C)



Symbol	Parameter	Conditions	22C12-20 Min	22C12-20 Max	22C12-30 Min	22C12-30 Max	Units
t_{RC}	Read cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{AA}	Address access time			200		300	ns
t_{CO}	CS access time			200		300	ns
t_{OH}	Output data hold time		50		50		ns
t_{LZ}	CS enable time		10		10		ns
t_{HZ}	CS disable time		10	100	10	100	ns

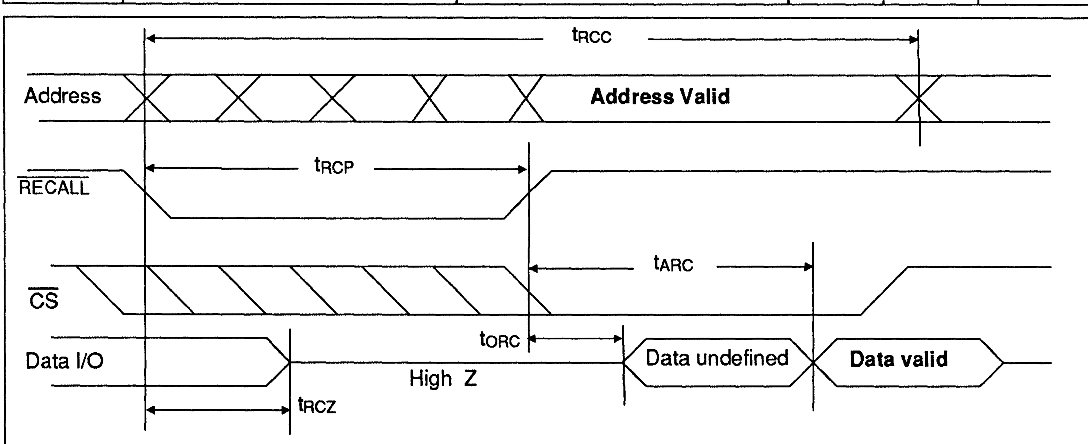
AC CHARACTERISTICS <Store Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{STC}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns
t_{OST}	Store enable time		10		ns



AC CHARACTERISTICS <Recall Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	1400		ns
t_{RCP}	Recall pulse width		300		ns
t_{RCZ}	Recall disable time			100	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1100	ns



DEVICE OPERATION

The configuration of the CAT22C12 allows a common address bus to be directly connected to the address inputs, and the Input/Output (I/O) pins to be connected directly to a common I/O bus if it has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) goes low, the chip is activated. When $\overline{CS}$ is forced high, the chip goes into the standby mode and consumes very little current. With the Non-Volatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0 - A_7), and that byte will be read or written to through the Input/Output pins (I/O_0 - I/O_3).

The Non-Volatile functions are inhibited by holding the $\overline{STORE}$ and the $\overline{RECALL}$ high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire EEPROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the EEPROM array.

STANDBY MODE

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C12. When a high level is supplied to the $\overline{CS}$ pin, the chip goes into the standby mode. In the mode the chip consumes 99.9% less power and the outputs are put into a high impedance state. Because I_{CCS} is less than 100μA in standby mode, the designer has the flexibility to use this part in battery operated systems.

READ

When the chip is enabled ($\overline{CS}$ = low), the Non-Volatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). The Write Enable ($\overline{WE}$) can put the chip into the read mode when it is held high. In this mode, the data in the Static RAM array may be accessed by selecting an address on the input pins A_0 - A_7. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

WRITE

Like the read mode, with the chip enabled and the non-volatile functions inhibited, the Write Enable ($\overline{WE}$) will select the write mode when taken to a low level. In this mode, the address must be supplied for the byte to be written to. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0 - I/O_3. When these conditions, including the write pulse width time (t_{WP}), are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by setting $\overline{WE}$ = low, inhibiting the Non-Volatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

RECALL

At anytime, except during a store, taking the $\overline{RECALL}$ pin low will initiate a recall operation. This is independent of the state of $\overline{CS}$, $\overline{WE}$, or A_0-A_7. After the $\overline{RECALL}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire content of the EEPROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from End of Recall (t_{ARC}). After this, any other bytes may be accessed by using the normal read mode.

If $\overline{RECALL}$ is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data. A recall operation is automatically performed upon power-up (low to high transition) of V_{CC}.

The outputs I/O_0-I/O_3 will go into the high impedance state as long as the $\overline{RECALL}$ signal is held low.

STORE

At any time, except during a recall operation, taking the $\overline{STORE}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{CS}$, $\overline{WE}$ or A_0-A_7. The $\overline{STORE}$ pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{STORE}$ pin may be left low or taken high and the store operations will complete its transfer of the entire contents of the Static RAM array into the EEPROM array within the Store Cycle time (t_{STC}). However, if a store operation is initiated during the write mode, the contents of the addressed Static RAM byte and its corresponding byte in the EEPROM array will be unknown.

During the store operation, the outputs are in a high impedance state. At least 10,000 store operations can be performed reliably. The data which is written into the EEPROM array during a store operation has a data retention time greater than 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C12 has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.5V. This function eliminates the potential hazard of a spurious store operation being initiated because the system signals are unstable at a low V_{CC}. This function does not affect the ability of external circuitry to intentionally do a store operation when V_{CC} falls below 4.5V. In fact, it is still important to prevent a potential second initiation of a store operation.

CAT24C44, CAT24C44 I [Industrial Temperature]
256-BIT (16X16) NON-VOLATILE CMOS SERIAL STATIC RAM

DESCRIPTION

The Catalyst CAT24C44 Non-Volatile RAM (NVRAM) is a 256-bit device with a 16 x 16 organization. It features fully static CMOS circuitry for very low power consumption. Active current is 10 mA and standby current is typically 5µA. An internal EEPROM array provides bit-by-bit backup for the static RAM array. Store operations write data from the RAM to the EEPROM array. Recall operations write data from the EEPROM array by either hardware inputs or software commands.

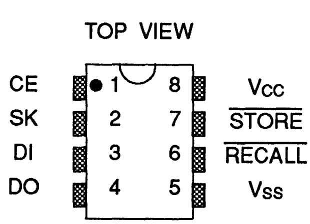
Data retention for each store cycle is specified for over 10 years and over 10,000 store operations can be performed reliably. There are unlimited recall operations from the EEPROM along with unlimited read and write operations to the RAM.

The CAT24C44 has internal false store protection circuitry to prohibit store operations when Vcc is less than 3.5V (typ.). This ensures EEPROM data integrety. Other internal circuitry performs an automatic recall upon power-up.

FEATURES

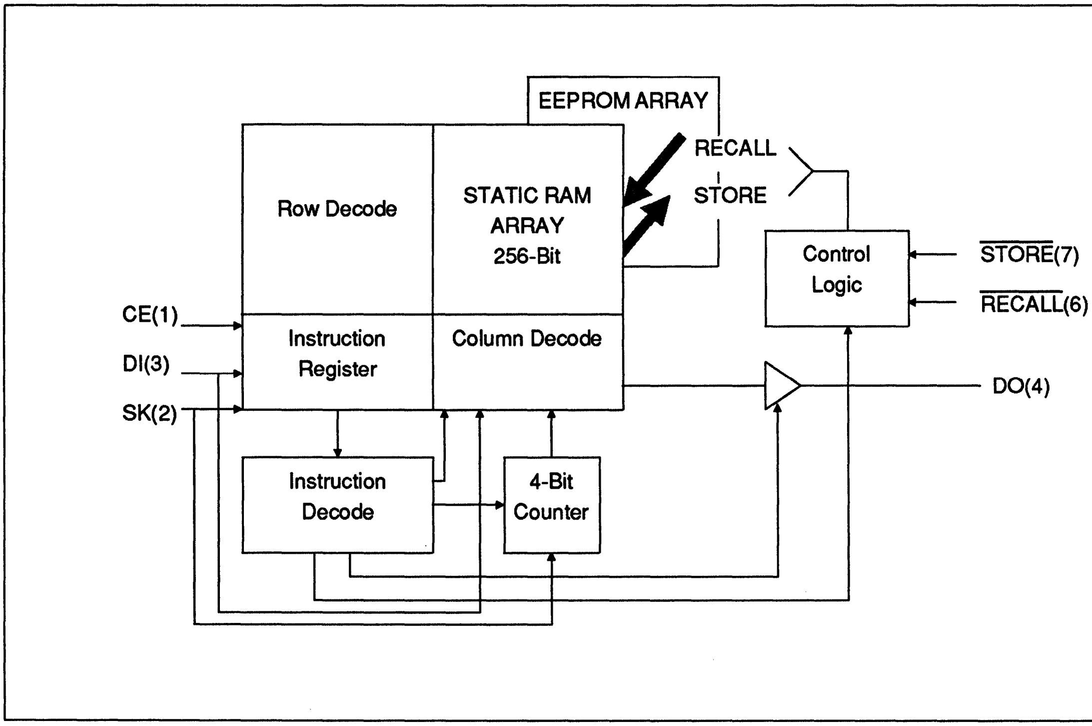
- CMOS technology, completely static operation
- Single 5-volt supply
- Low current consumption (standby-5µA typ., operation 10mA typ., sleep current 5µA typ.)
- Software/hardware control of non-volatile functions
- Fully TTL & CMOS compatible with high drive ability
- Write protection preserves data on power-up and power-down
- Auto-recall on power-up
- Serial port compatible (i.e. COPS™, 8051)
- 3-State output
- Short store pulse - 200ns
- Short recall pulse - 500ns
- False store protection below 3.5V operation level
- 10,000 non-volatile store cycles ber bit.
- 8 pin low cost 300-mil package

PIN CONFIGURATION



SK	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
Vcc	+5V
Vss	Ground

BLOCK DIAGRAM



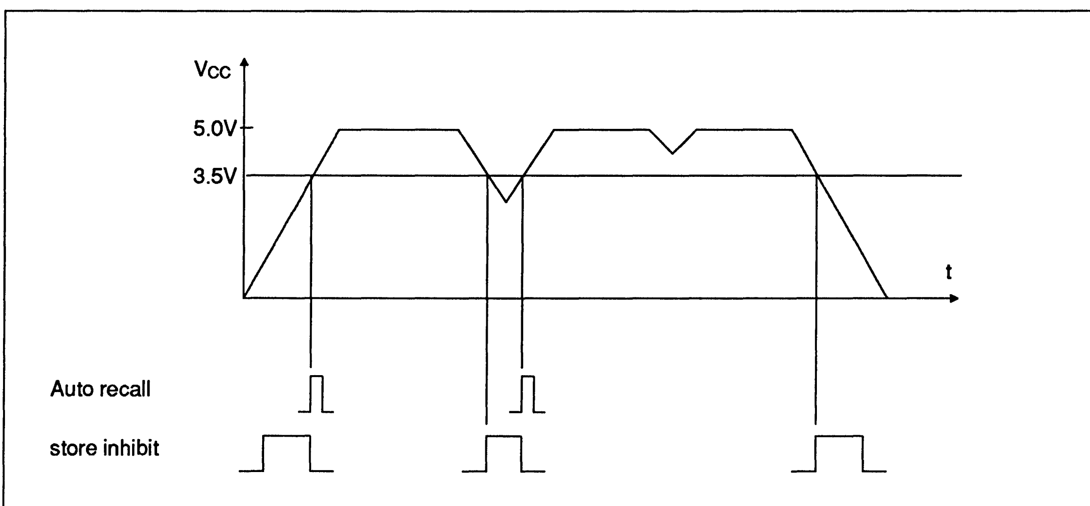
NON-VOLATILE MODES OF OPERATION

Operation	$\overline{STORE}$	$\overline{RECALL}$	Inst.	Write Enable Latch	Previous RECALL
Hardware recall	1	0		X	X
Software recall	1	1	RCL	X	X
Hardware store	0	1		SET	TRUE
Software store	1	1	STO	SET	TRUE

X = Don't care

NOTES:

- The store operation has priority over all the other operations
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 100ms



MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Temperature under bias	T_{bias}	-50° C to +125°C
Power supply	V_{CC}	-0.3 to +6V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3V
Output voltage	V_{OUT}	0.0 to $+V_{CC}$
Output current	I_{OUT}	5mA
Lead temperature (soldering for 10 seconds)		260°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT24C44 T_A = 0°C to +70°C, CAT24C44I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CCO}	Current consumption (operating)	$I_{I/O}$ = 0 mA, All inputs=V_{CC}, T_A =0°C		10	20	mA
I_{CCS}	Current consumption (stand-by)	Inputs=V_{CC} or V_{SS}		5	30	µA
I_{SL}	Sleep current	CE=V_{SS}		5	30	µA
I_{LI}	Input current	$0 \leq V_{IN} \leq 5.5V$		0.1	10	µA
I_{LO}	Output leakage current	$0 \leq V_{OUT} \leq 5.5V$		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.40	V
V_{DH}	Data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

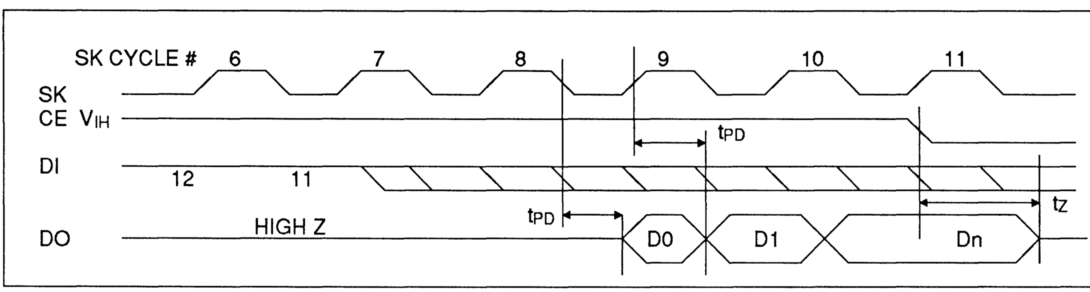
Note: These parameters are periodically sampled and are not 100% tested.

AC CHARACTERISTICS

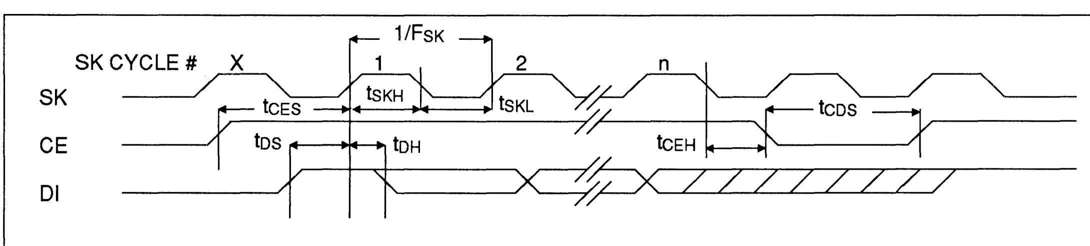
(CAT24C44 T_A = 0°C to +70°C, CAT24C44I T_A = -40°C to +85°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions	Min	Max	Units
F_{SK}	SK frequency	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V Input rise and fall times = 10ns.	DC	1.0	MHz
t_{SKH}	SK positive pulse width		400		ns
t_{SKL}	SK negative pulse width		400		ns
t_{DS}	Input data setup time		400		ns
t_{DH}	Input data hold time		80		ns
t_{PD}	SK data valid time			375	ns
t_Z	CE disable time			1.0	µs
t_{CES}	CE enable setup time		800		ns
t_{CEH}	CE enable hold time		400		ns
t_{CDS}	CE de-select time		800		ns

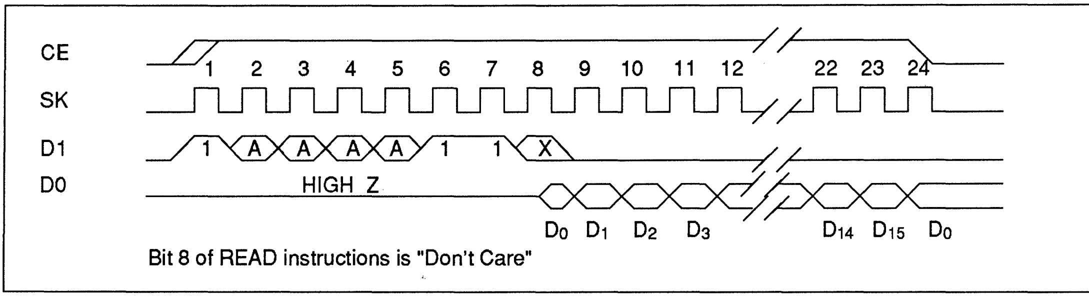
READ CYCLE



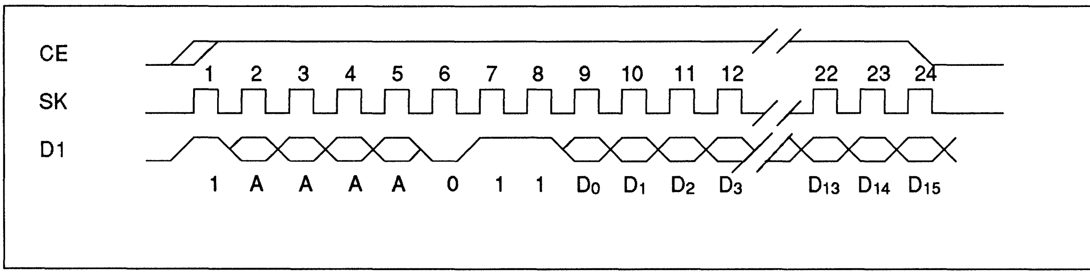
WRITE CYCLE



RAM READ



RAM WRITE

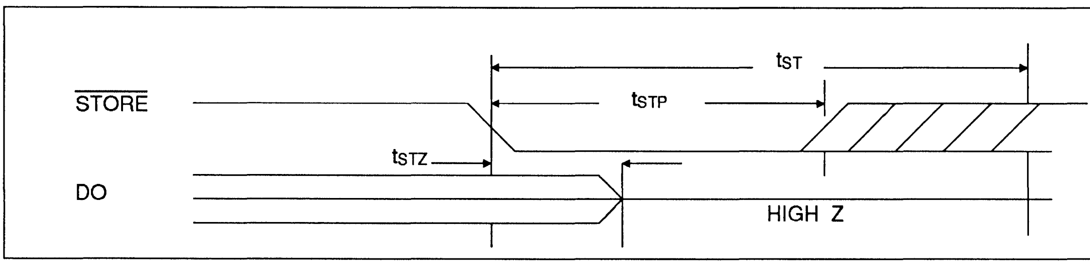


STORE CYCLE

Symbol	Parameter	Conditions	Min	Max	Units
t_{ST}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns

1

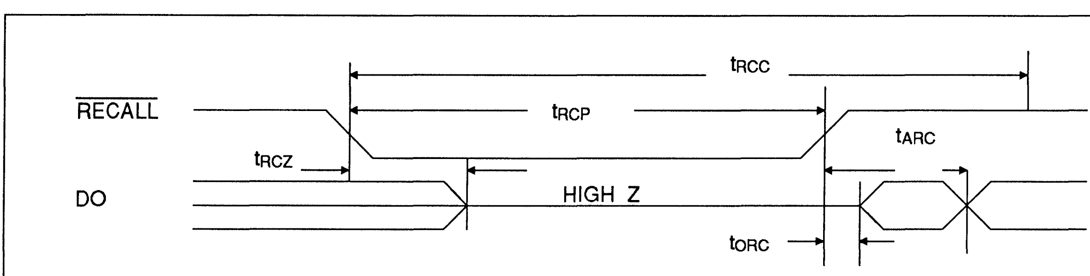
HARDWARE STORE



RECALL CYCLE

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	2500		ns
t_{RCP}	Recall pulse width		500		ns
t_{RCZ}	Recall disable time			500	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1500	ns

RECALL CYCLE



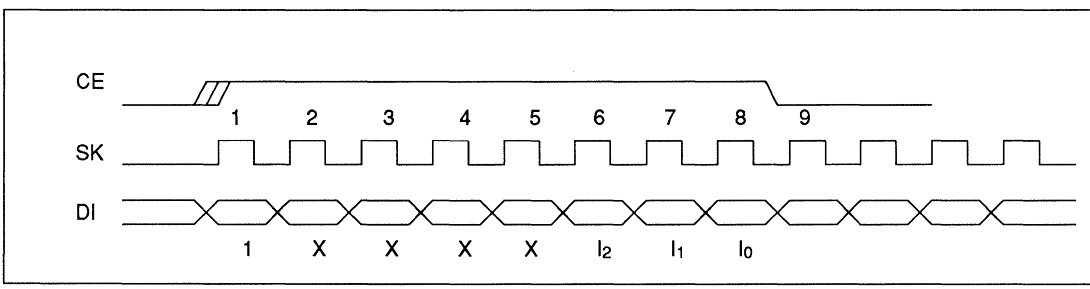
INSTRUCTION SET

Instruction	**Format, I_2, I_1, I_0**	**Operation**
WRDS	1XXXX000	Reset write enable latch
STO	1XXXX001	Store RAM data in EEPROM
SLEEP	1XXXX010	Enter SLEEP mode
WRITE	1AAAA011	Write data into RAM address AAAA
WREN	1XXXX100	Set write enable latch (enables writes and stores)
RCL	1XXXX101	Recall EEPROM data into RAM
READ	1AAAA11X	Read data from RAM address AAAA

X = Don't care

A = Address bit

NON-DATA OPERATIONS



DEVICE OPERATION

The CAT24C44 is a 256 bit non-volatile CMOS serial static RAM intended for use with the COPS™ family of microcontrollers, or other standard microprocessors such as the 8048 or 8051. The CAT24C44 is organized as 16 registers by 16 bits. Seven 8 bit instructions control the device's operating modes, the RAM reading and writing, and the EEPROM storing and recalling. It is also possible to control the EEPROM store and recall functions in hardware with the STORE and RECALL pins. The CAT24C44 operates on a single 5 Volt supply and will generate, on chip, the high voltage required during a RAM to EEPROM storing operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when outputting data from the device. The CE (chip enable) pin must remain selected (low) during the entire data transfer.

The format for all instructions sent to the CAT24C44 is one logical "1" start bit, 4 address bits (data read or write operations) or 4 "don't care" bits (device mode operations), and a 3 bit op code (See table above). For data write operations, the 8 bit instruction is followed by 16 bits of data. For data read instructions, DO will come out of the high impedance state and enable 16 bits of data to be clocked from the device. The 8th bit of the read instruction is a "don't care" bit. This is to eliminate any bus contention that would occur in applications where the DI and DO pins are tied together to form a common DI/O line. A word of caution while clocking data to or from the device. If the CE pin is prematurely deselected while shifting in an instruction, that instruction will not be executed and the shift register internal to the CAT24C44 will be cleared. If there are more than or less than 16 SK clocks during a memory data transfer, an improper data transfer will result.

WREN/WRDS

The CAT24C44 powers up in the program disable state (the "write enable latch" is reset). Any programming after power-up or after a WRDS (RAM write/EEPROM store disable) instruction must first be preceded by the WREN (RAM write/EEPROM store enable) instruction. Once writing/storing is enabled, it will remain enabled until power to the device is removed, the WRDS instruction is sent, or an EEPROM store has been executed (STO/STORE). The WRDS (write/store disable) can be used to disable all CAT24C44 programming functions, and will prevent any accidental writing to the RAM, or storing to the EEPROM. Data can be read normally from the CAT24C44 regardless of the "write enable latch" status.

SLEEP

The sleep mode places the CAT24C44 into a lower quiescent power mode. Internal RAM power is turned off, and any data that is written into the RAM area is lost. However, data from the last RAM to EEPROM store operation is retained in the EEPROM memory. The CAT24C44 will exit the sleep mode, and restore the RAM memory area by issuing either a hardware or software recall command.

RCL/RECALL

Data is transferred from the EEPROM data memory to RAM by either sending the RCL instruction, or by pulling the RECALL input pin low. Although the EEPROM data is automatically transferred to RAM at power up, a recall operation must be performed before the EEPROM store, or RAM write operations can be executed. Either recall operation will set the "previous recall latch" internal to the CAT24C44.

STO/STORE

Data in the RAM memory area is stored in the EEPROM memory either by sending the STO instruction or by pulling the STORE input pin low. To prevent any unwanted store operation, the following conditions must all be true before data can be transferred:

The "previous recall latch" must be set. (See RCL/RECALL)

The "write enable latch" must be set. (See WREN/WRDS)

A store operation must be executed.

During the store operation, all other CAT24C44 functions are inhibited. Upon completion of the store operation the "write enable latch" is reset. The device also provides false store protection for V_{CC} falling below a 3.5 volt level. If V_{CC} falls below this level, the store operation is disabled and "write enable latch" is reset.

READ

Upon receiving a start bit, 4 address bits, and the 3 bit read command (clocked into the DI pin), the DO pin of the CAT24C44 will come out of the high impedance state and the 16 bits of data, located at the address location specified in the instructions, will be clocked out of the device. When clocking data from the device, the first bit clocked out (D0) is timed from the falling edge of the 8th clock, all succeeding bits (D1 - D15) are timed from the rising edge of the clock. (See Read Cycle timing diagram.)

WRITE

After receiving a start bit, 4 address bits, and the 3 bit WRITE command, the 16 bit word is clocked into the device for storage into the RAM memory location specified.

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EEPROMs

2

CAT93C46
1K BIT SERIAL EEPROM

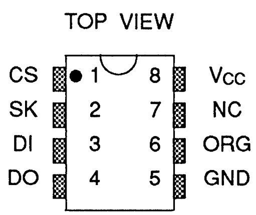
DESCRIPTION

The CAT93C46 is a 1K bit Serial EEPROM memory device organized in 64 registers of 16 bits (ORG pin at V_{CC}) or 128 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip or S.O. package. To be offered in a 3-volt version (CAT33C101).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with National Semiconductor NMC 9346
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range $0^{o}C$ to $70^{o}C$ [industrial temp range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

PIN CONFIGURATION

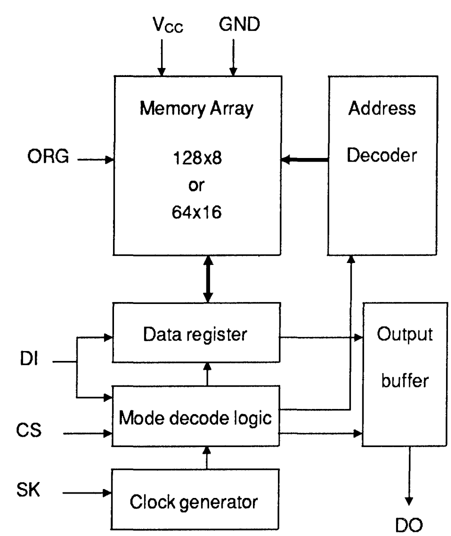


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: ORG, When the ORG pin is connected to +5V, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CC1}	Current consumption (operating)	V_{CC} =5V, CS = V_{IH} Outputs unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	μA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	μA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400μA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address 128 x 8	Address 64 x 16	Data 128 x 8	Data 64 x 16	Comments
READ	1	1 0	A6 - A0	A5 - A0			Read address AN - A0
ERASE	1	1 1	A6 - A0	A5 - A0			ERASE address AN - A0
WRITE	1	0 1	A6 - A0	A5 - A0	D7 - D0	D15 - D0	WRITE address AN - A0
EWEN	1	0 0	11XXXXX	11XXXX			Program enable
EWDS	1	0 0	00XXXXX	00XXXX			Program disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase all addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			µs
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{HZ}	Output delay to Hi-Z				0.4	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		1			µs
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minumun SK low time		1			µs
t_{SV}	Output delay to status valid	C_L = 100pF			1	µs
SK_{MAX}	Maximum frequency		DC		250	kHz

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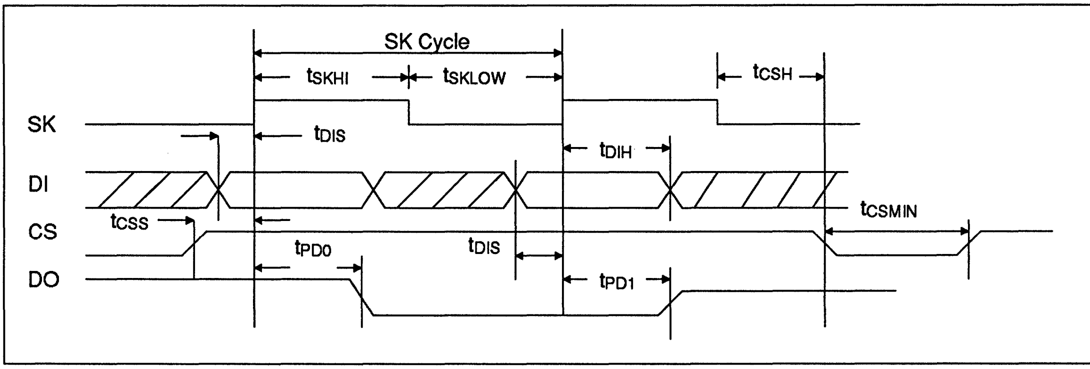
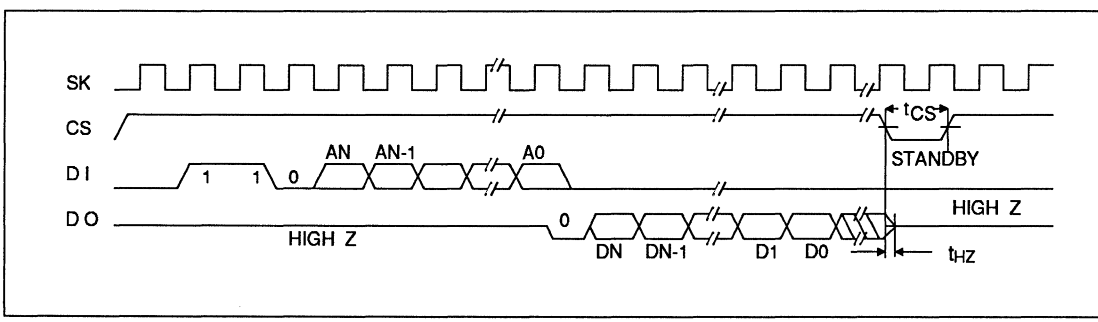
SYNCHRONOUS TIMINGS



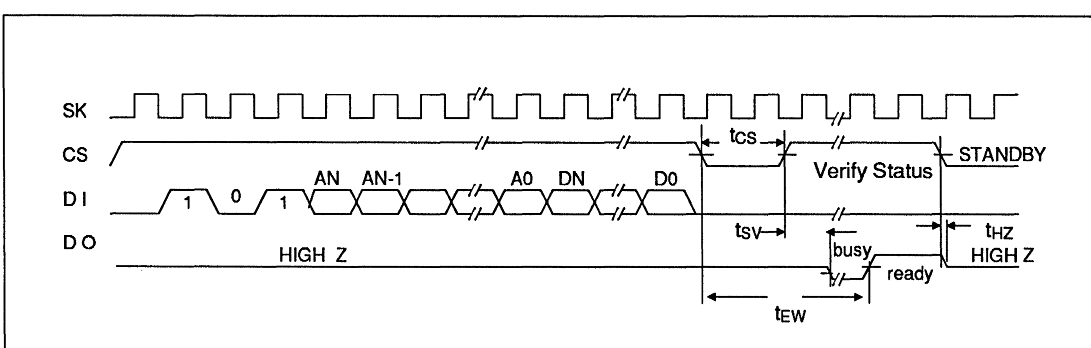
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

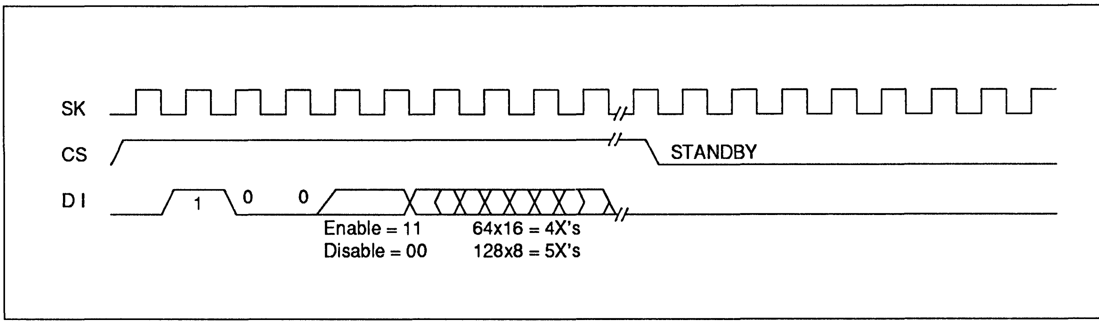
INSTRUCTION TIMING <READ>



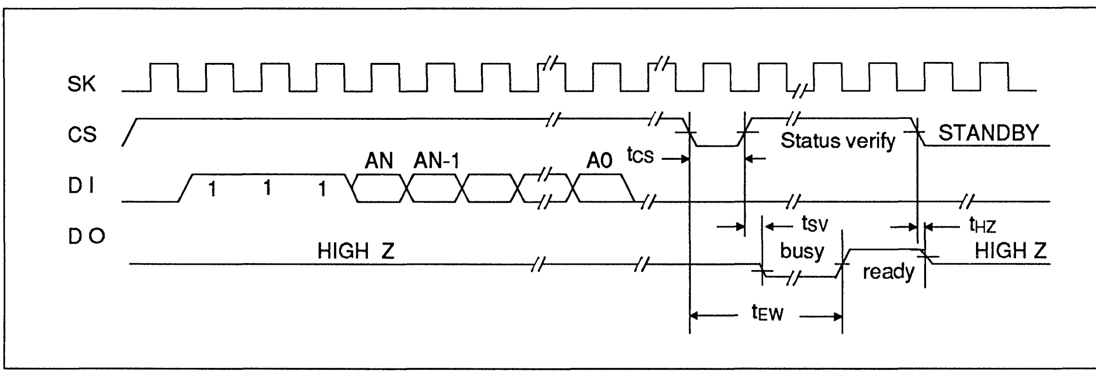
INSTRUCTION TIMING <WRITE>



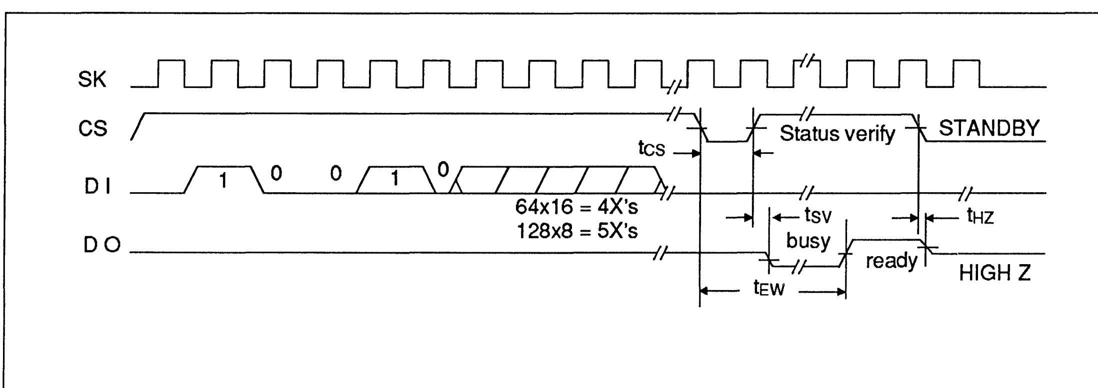
INSTRUCTION TIMING <EWENS, EWDS>



INSTRUCTION TIMING <ERASE>

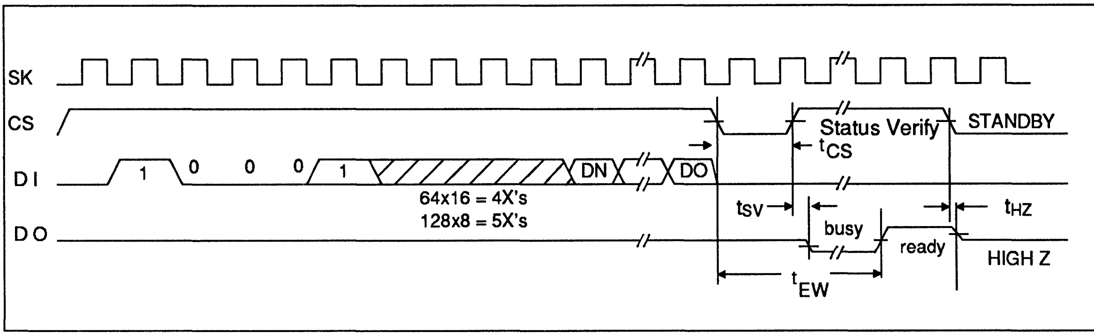


INSTRUCTION TIMING <ERAL>



2

INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46H is a 1024 bit non-volatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT93C46H can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven, 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT93C46H operates on a single 5 Volt supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the busy\ready status after a programming operation. The busy/ready status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46H is 1 logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT93C46H will come out of the high impedance state, after sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifting out. The data bits being shifted out will toggle on the rising edge of the SK clock and is stable after the specified time delay t_{PD0} or t_{PD1}.

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46H powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46H programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46H regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46H can be determined by selecting the device and polling the DO pin.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46H can be determined by selecting the device and polling the DO pin. With the CAT93C46H it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERASE ALL command, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46H can be determined by selecting the device and polling the DO pin.

WRITE ALL

Upon receiving a WRITE ALL command and data, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46H can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRITE ALL command is executed.

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CAT93C46I [Industrial Temperature]
1K BIT SERIAL EEPROM

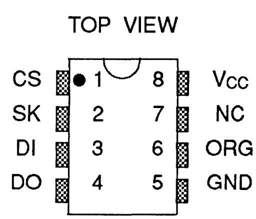
DESCRIPTION

The CAT93C46I is a 1K bit Serial EEPROM memory device organized in 64 registers of 16 bits (ORG pin at V_{CC}) or 128 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46I is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip or S.O. package. To be offered in a 3-volt version (CAT33C101 I).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with National Semiconductor NMC 9346
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range -40°C TO +85°C
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

PIN CONFIGURATION

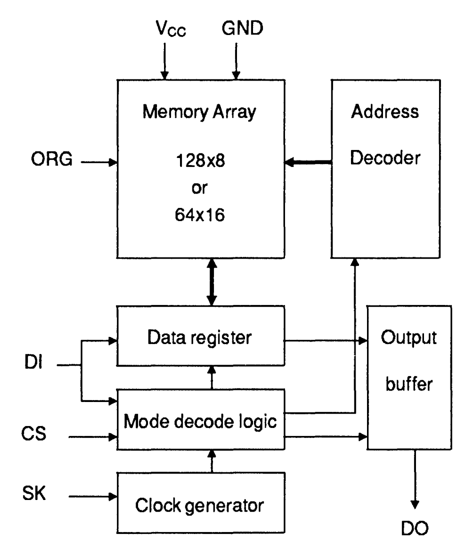


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: ORG, When the ORG pin is connected to +5V, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC1}	Current consumption (operating)	V_{CC} =5.0V, CS = V_{IH} Outputs unloaded			4	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

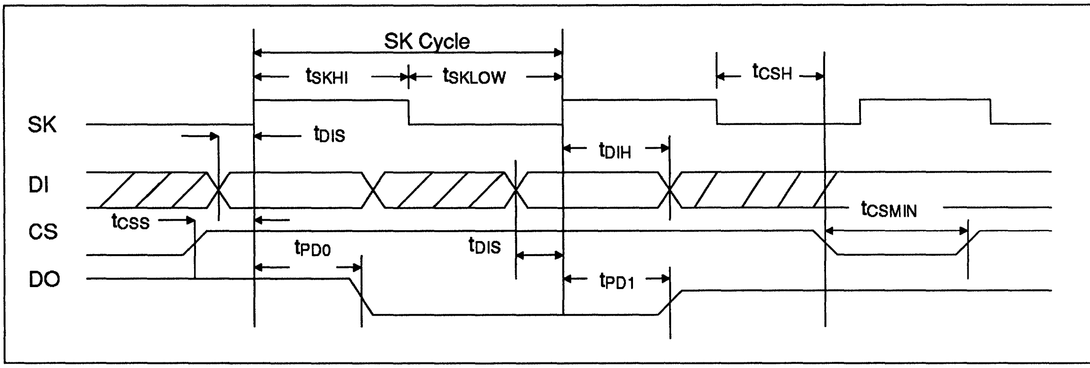
Instruction	Start Bit	Opcode	Address 128 x 8	Address 64 x 16	Data 128 x 8	Data 64 x 16	Comments
READ	1	1 0	A6 - A0	A5 - A0			Read address AN - A0
ERASE	1	1 1	A6 - A0	A5 - A0			ERASE address AN - A0
WRITE	1	0 1	A6 - A0	A5 - A0	D7 - D0	D15 - D0	WRITE address AN - A0
EWEN	1	0 0	11XXXXX	11XXXX			Program enable
EWDS	1	0 0	00XXXXX	00XXXX			Program disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase all addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			µs
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{HZ}	Output delay to Hi-Z				0.4	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		1			µs
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minimum SK low time		1			µs
t_{SV}	Output delay to status valid	C_L = 100pF			1	µs
SK_{MAX}	Maximum frequency		DC		250	kHz

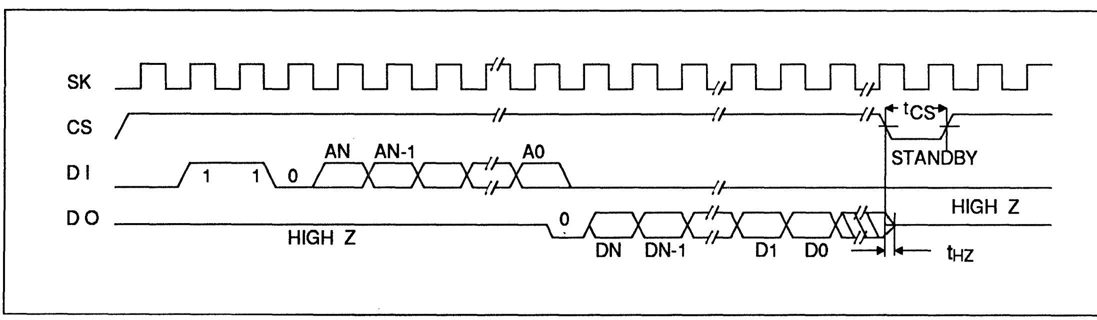
SYNCHRONOUS TIMINGS



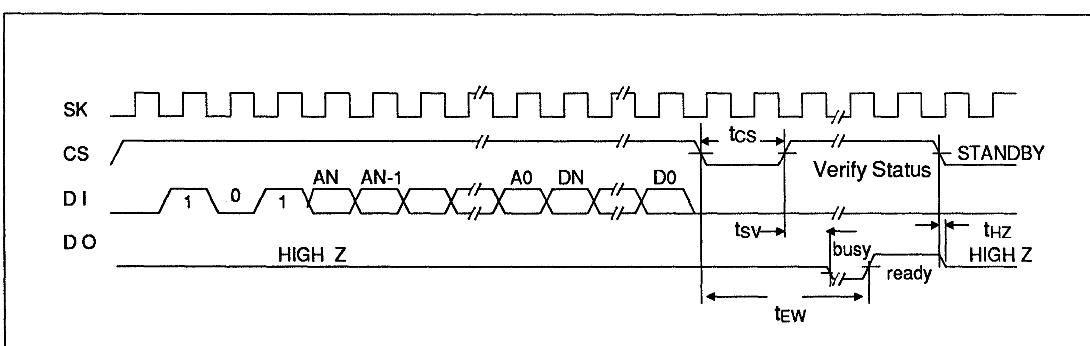
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

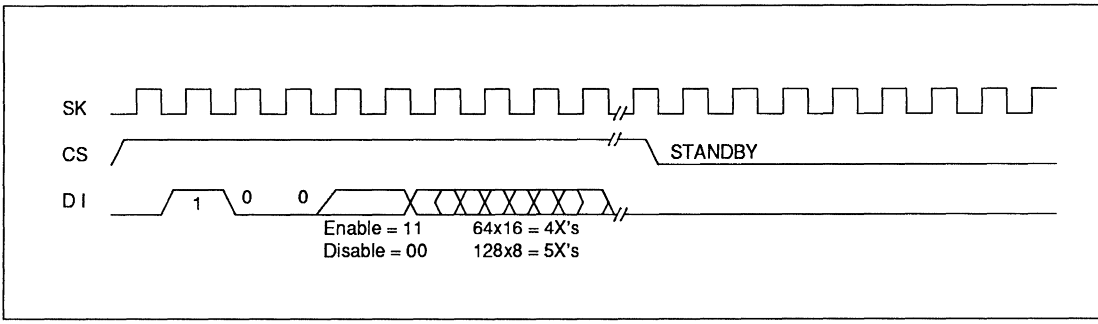
INSTRUCTION TIMING <READ>



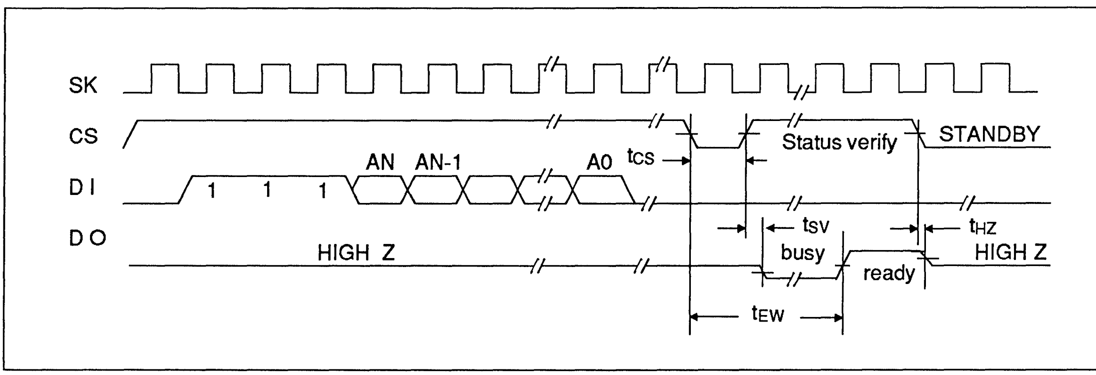
INSTRUCTION TIMING <WRITE>



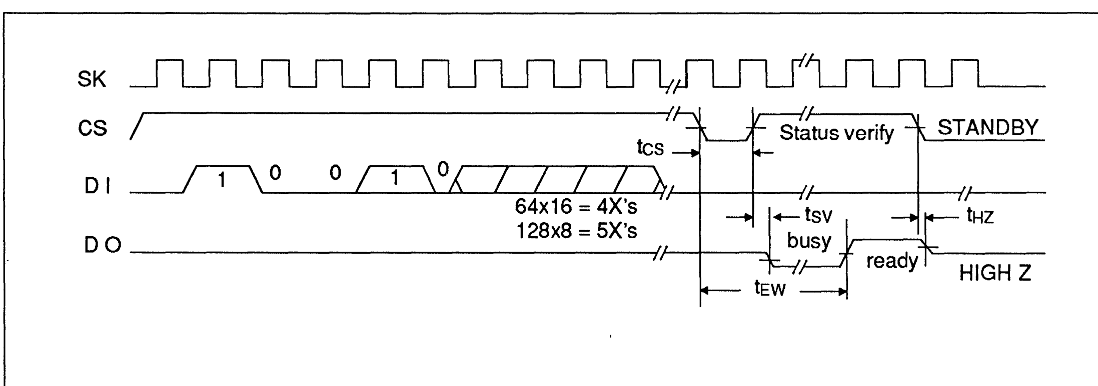
INSTRUCTION TIMING <EWENS, EWDS>



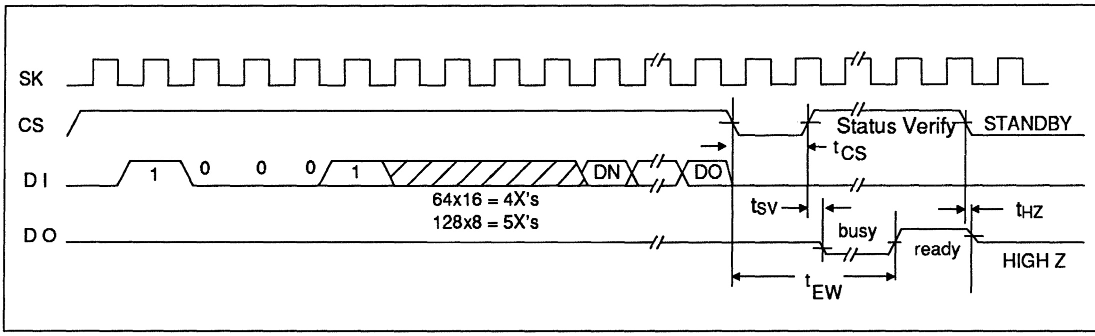
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46I is a 1024 bit non-volatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT93C46I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven, 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT93C46I operates on a single 5 Volt supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the busy\ready status after a programming operation. The busy/ready status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46I is 1 logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT93C46I will come out of the high impedance state, after sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifting out. The data bits being shifted out will toggle on the rising edge of the SK clock and is stable after the specified time delay t_{PD0} or t_{PD1}.

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46I powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46I programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46I regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46I can be determined by selecting the device and polling the DO pin.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46I can be determined by selecting the device and polling the DO pin. With the CAT93C46I it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERASE ALL command, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46I can be determined by selecting the device and polling the DO pin.

WRITE ALL

Upon receiving a WRITE ALL command and data, the CS (chip select) must be deselected for a minimum of 1 µs (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT93C46I can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRITE ALL command is executed.

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2

CAT59C11
1K BIT SERIAL EEPROM

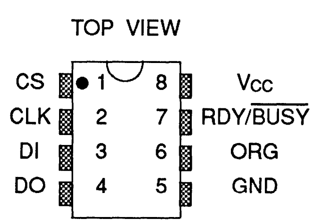
DESCRIPTION

The CAT59C11 is a 1K bit Serial EEPROM memory device organized in 64 registers of 16 bits (ORG pin at V_{CC}) or 128 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip and Small Outline packages. To be offered in a 3-volt package (CAT33C201).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

PIN CONFIGURATION

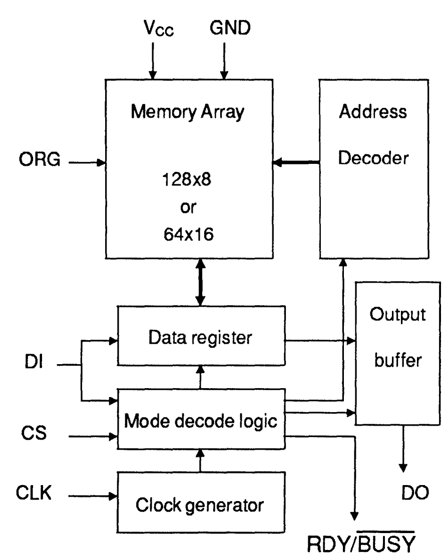


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/$\overline{\text{BUSY}}$	Status output
GND	Ground
ORG	Memory organization

Note: When the **ORG** pin is connected to +5V, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature T_{stg} . . . . -65°C to +150°C
Power supply V_{CC} . . . . +7 V
Voltage on any input pin . . . . -0.3 to +7V
Voltage on any output pin . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CC1}	Current consumption (operating)	V_{CC} =5.5V, CS = 1 DO unloaded			5	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address 128 x 8	Address 64 x 16	Data 128 x 8	Data 64 x 16	Comments
READ	1	1000	A_6 - A_0	A_5 - A_0			Read address A_N - A_0
PROGRAM	1	X100	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Program address A_N - A_0
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D_7 - D_0	D_{15} - D_0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	CL = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			µs
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				20	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minumun SK low time		1			µs
CK_{MAX}	Maximum frequency		DC		250	kHz

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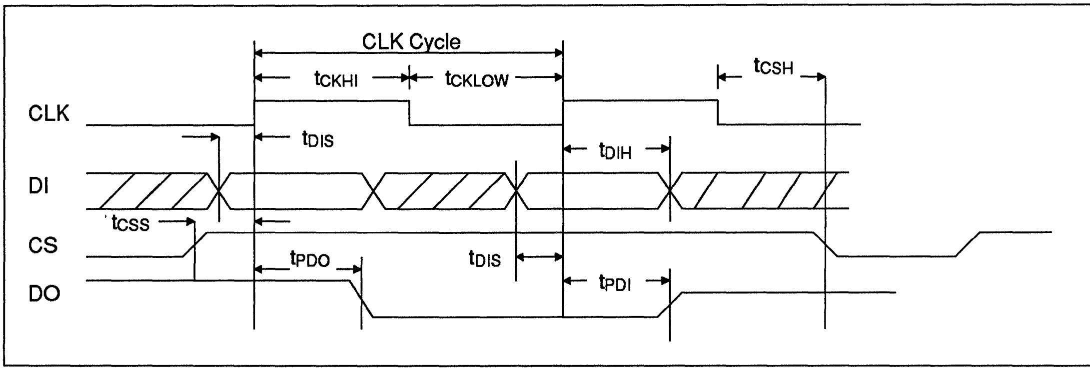
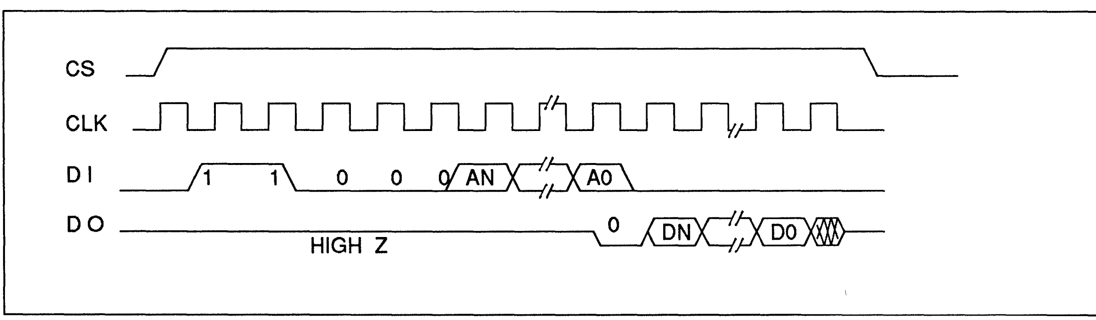
SYNCHRONOUS TIMINGS



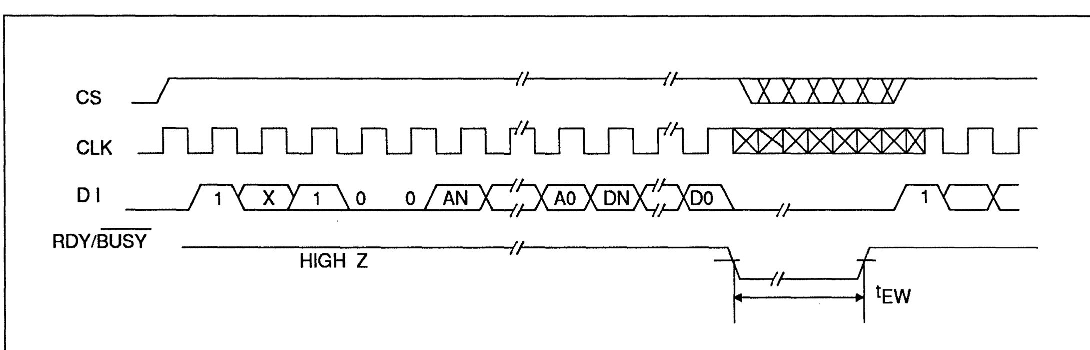
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

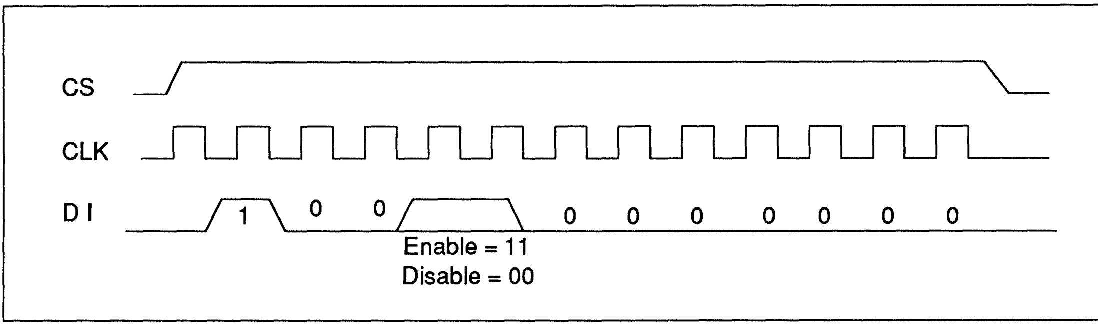
INSTRUCTION TIMING <READ>



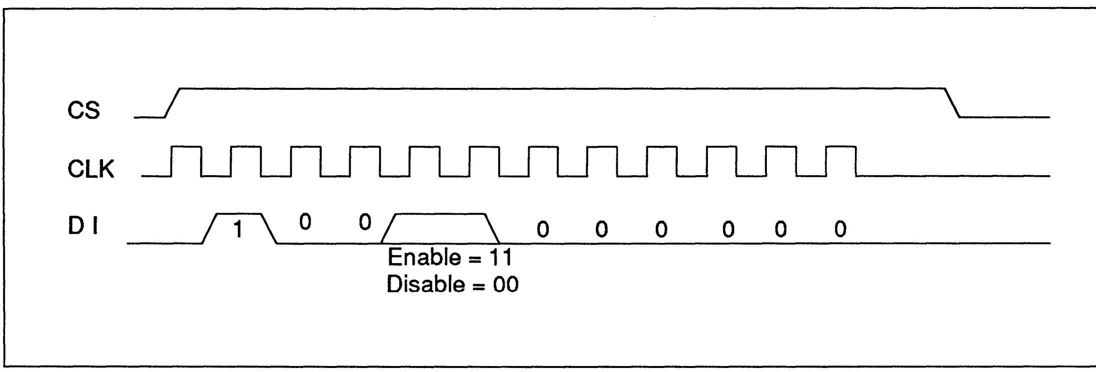
INSTRUCTION TIMING <PROGRAM>



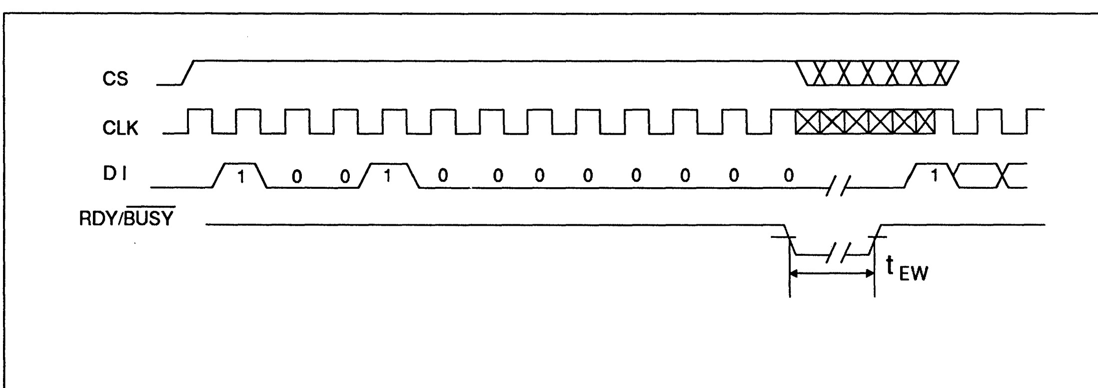
INSTRUCTION TIMING <PEN, PDS, for 128 x 8 organization>



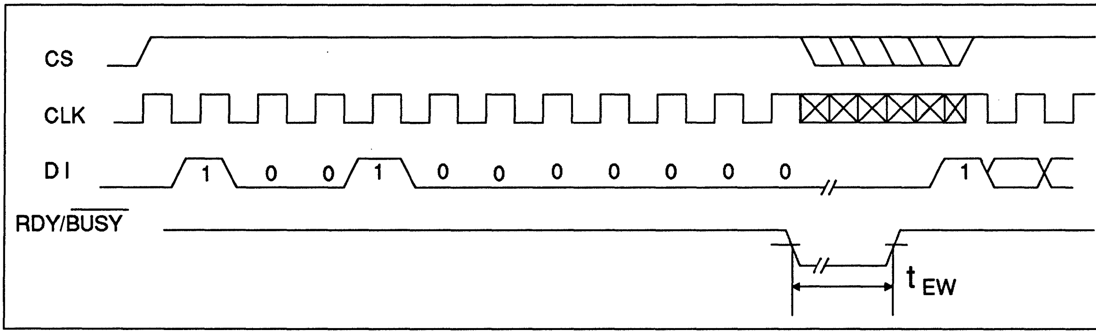
INSTRUCTION TIMING <PEN, PDS , for 64 x 16 organization>



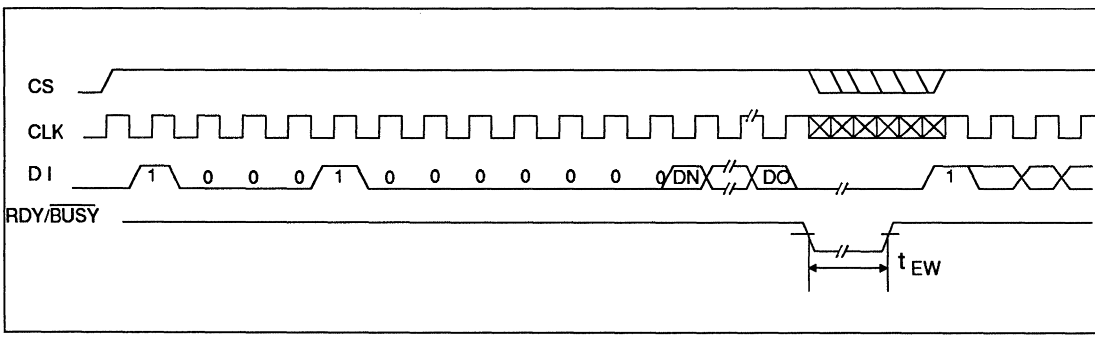
INSTRUCTION TIMING <ERAL, 128 x 8 organization>



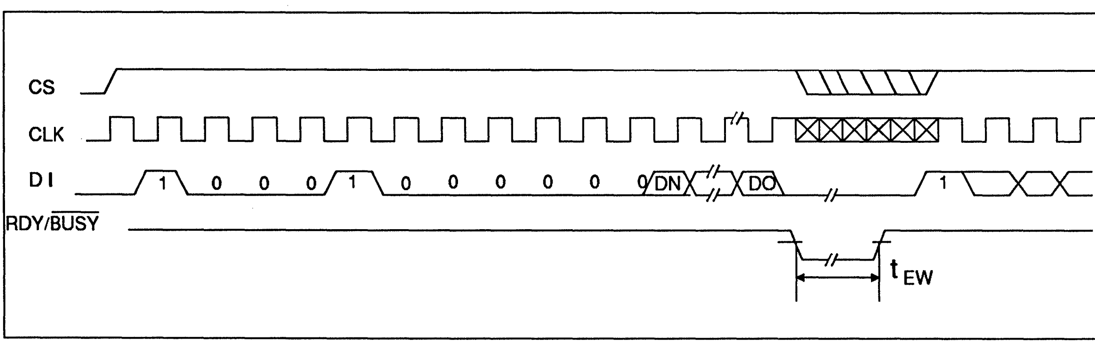
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11 is a 1024 bit non-volatile memory intended for use with all standard controllers. The CAT59C11 can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six, 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11 operates on a single 5 Volt supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{\text{BUSY}}$ pin.

The format for all instructions sent to the CAT59C11 is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11 will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11 powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11 regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{BUSY}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11 can be determined by polling the RDY/$\overline{BUSY}$ pin.

ERASE ALL

Upon receiving an WRAL command, the RDY/$\overline{BUSY}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11 can be determined by polling the RDY/$\overline{BUSY}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{BUSY}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11 can be determined by polling the RDY/$\overline{BUSY}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

2

CAT59C11A
1K BIT SERIAL EEPROM

DESCRIPTION

The CAT59C11A is a 1K bit Serial EEPROM memory device organized in 64 registers of 16 bits (ORG pin at V_{CC}) or 128 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11A is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip and Small Outline packages. To be offered in a 3-volt package (CAT33C201A).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

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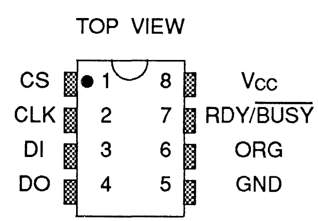
PIN CONFIGURATION

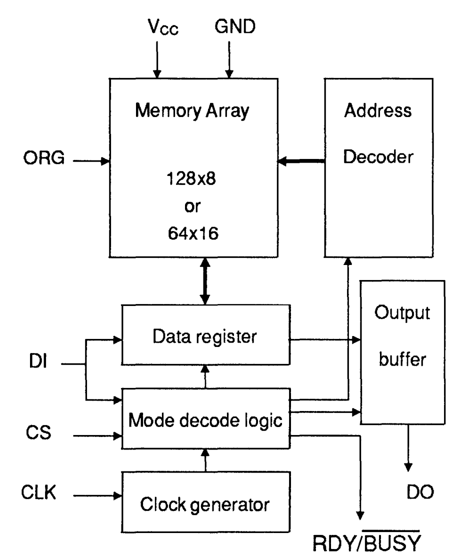


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the **ORG** pin is connected to +5V, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CC1}	Current consumption (operating)	V_{CC} =5.5V, CS = 1 DO unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address 128 x 8	Address 64 x 16	Data 128 x 8	Data 64 x 16	Comments
READ	1	1000	$A_6 - A_0$	$A_5 - A_0$			Read address $A_N - A_0$
PROGRAM	1	X100	$A_6 - A_0$	$A_5 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Program address $A_N - A_0$
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	$D_7 - D_0$	$D_{15} - D_0$	Write all addresses

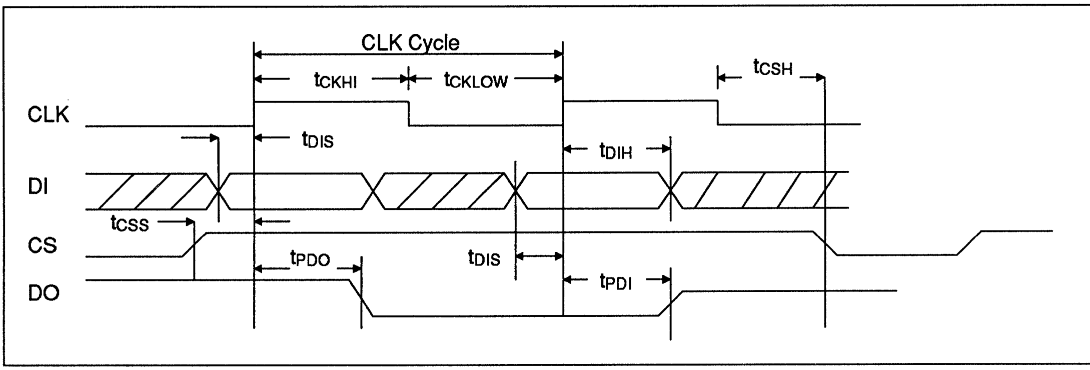
AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			µs
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minimum SK low time		1			µs
CK_{MAX}	Maximum frequency		DC		250	kHz

2

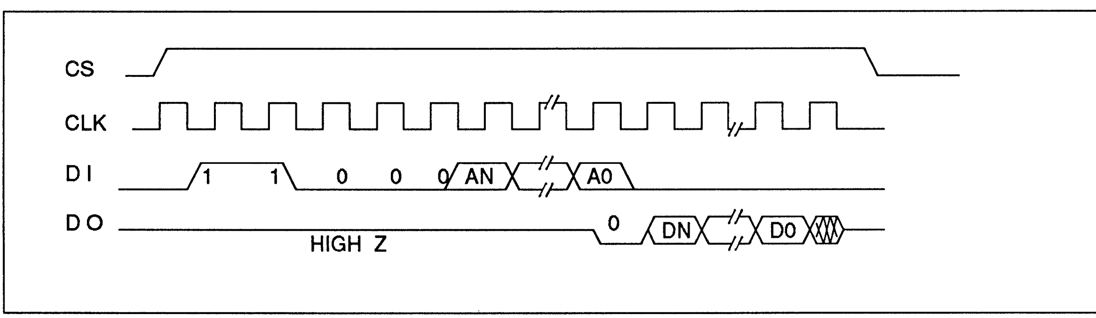
SYNCHRONOUS TIMINGS



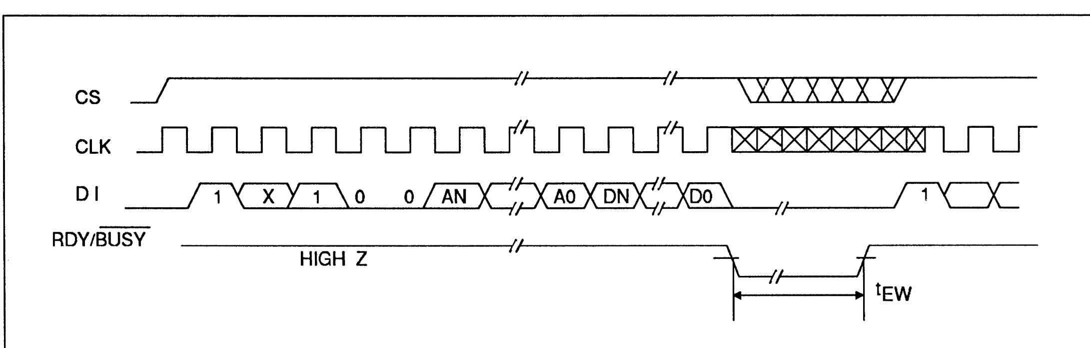
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

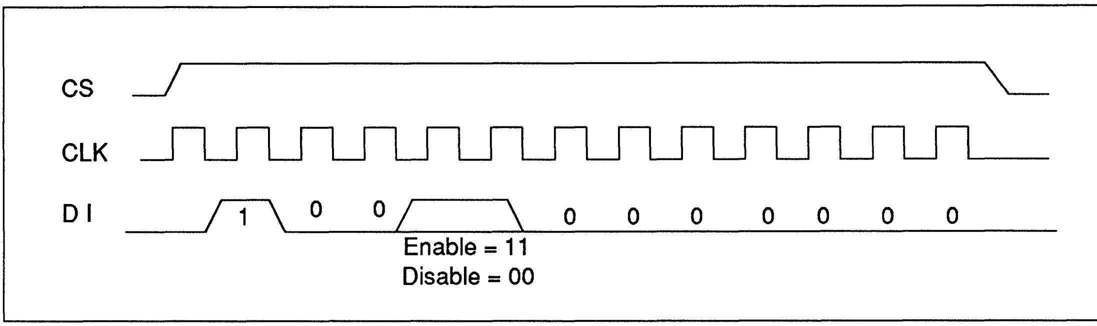
INSTRUCTION TIMING <READ>



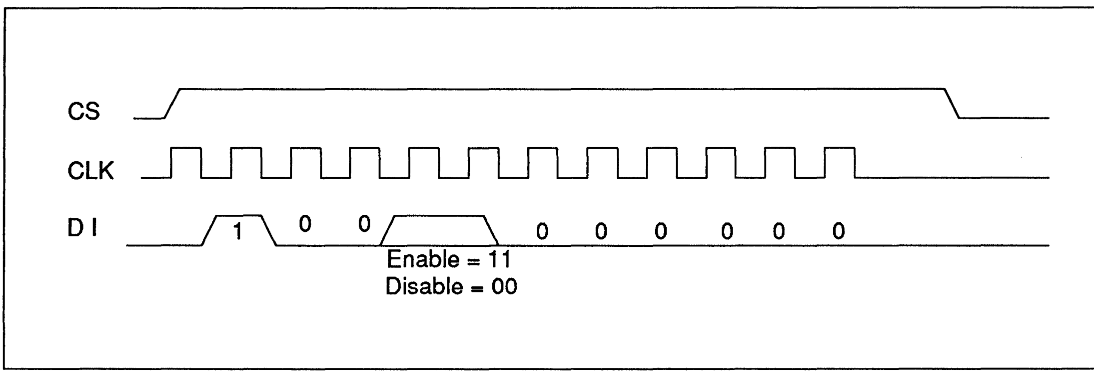
INSTRUCTION TIMING <PROGRAM>



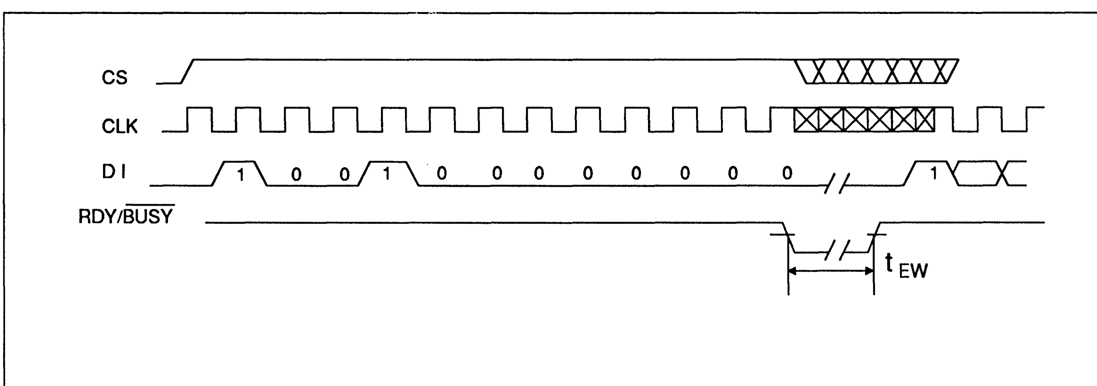
INSTRUCTION TIMING <PEN, PDS, for 128 x 8 organization>



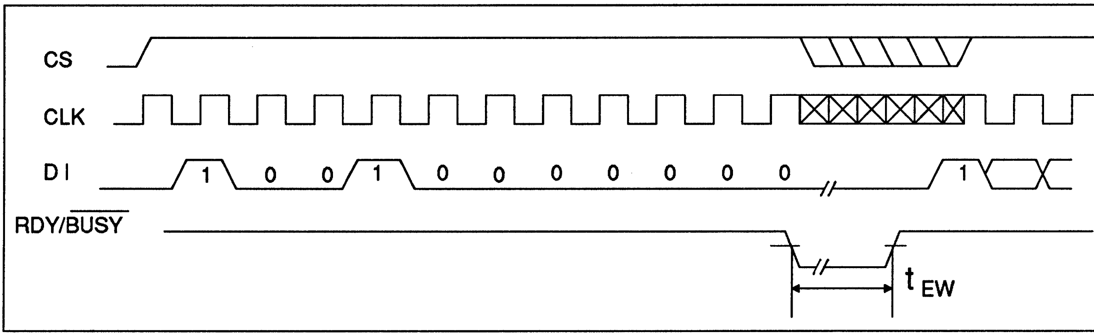
INSTRUCTION TIMING <PEN, PDS , for 64 x 16 organization>



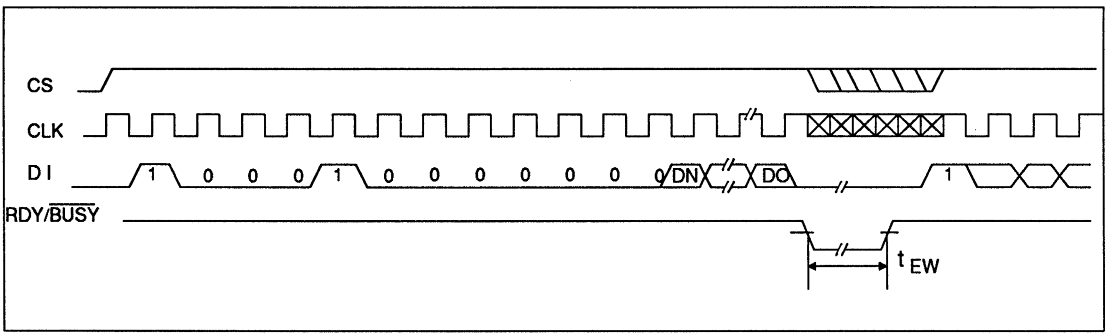
INSTRUCTION TIMING <ERAL, 128 x 8 organization>



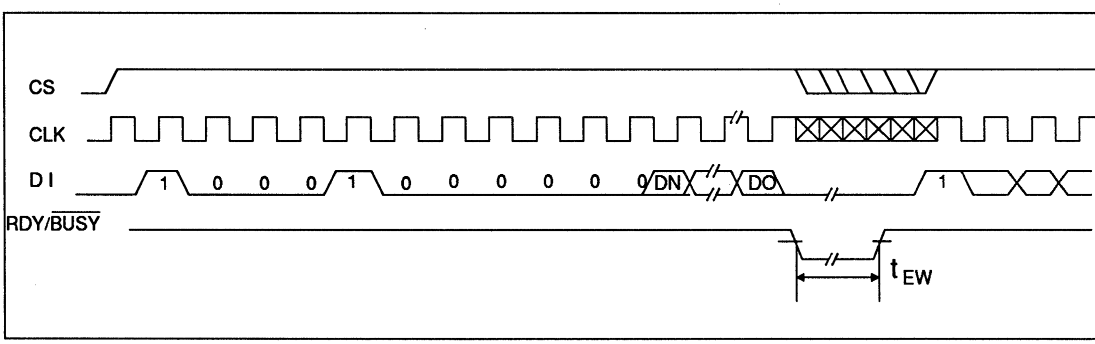
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11A is a 1024 bit non-volatile memory intended for use with all standard controllers. The CAT59C11A can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six, 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11A operates on a single 5 Volt supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{BUSY}$ pin.

The format for all instructions sent to the CAT59C11A is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11A will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11A powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11A's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11A regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an WRAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT59C11 I [Industrial Temperature]
1K BIT SERIAL EEPROM

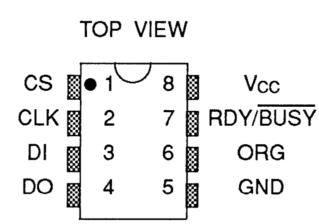
DESCRIPTION

The CAT59C11I is a 1K bit Serial EEPROM memory device organized in 64 registers of 16 bits (ORG pin at V_{CC}) or 128 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11I is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip and Small Outline packages. To be offered in a 3-volt version (CAT33C201 I).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range -40°C to +85°C
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

PIN CONFIGURATION

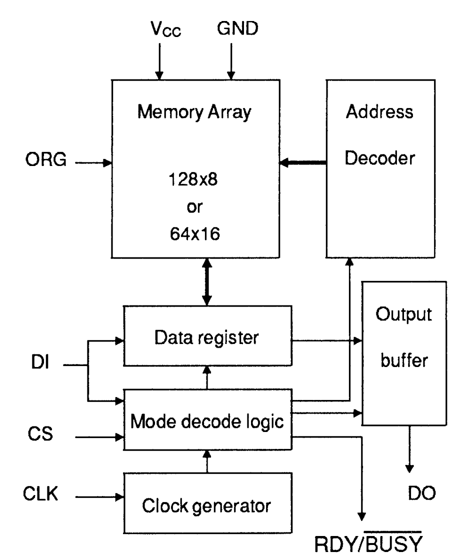


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/$\overline{BUSY}$	Status output
GND	Ground
ORG	Memory organization

Note: When the **ORG** pin is connected to +5V, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CC1}	Current consumption (operating)	V_{CC} =5.5V, CS = 1 DO unloaded			5	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address 128 x 8	Address 64 x 16	Data 128 x 8	Data 64 x 16	Comments
READ	1	1000	A_6 - A_0	A_5 - A_0			Read address A_N - A_0
PROGRAM	1	X100	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Program address A_N - A_0
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D_7 - D_0	D_{15} - D_0	Write all addresses

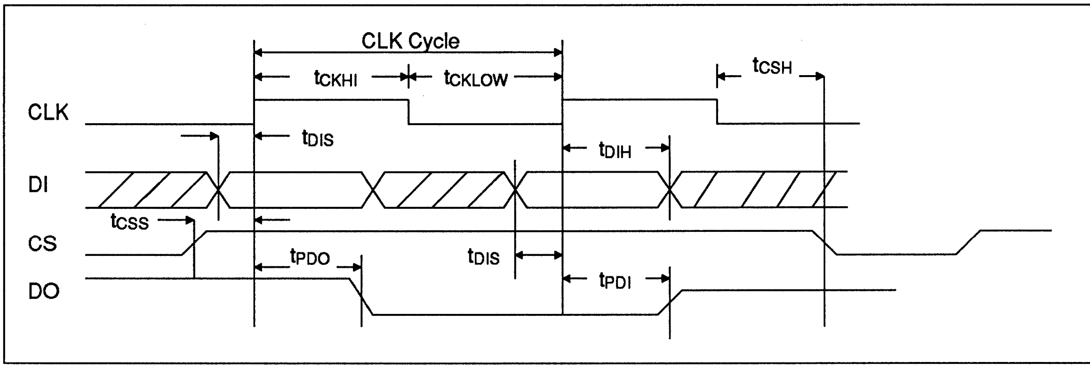
AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			µs
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				20	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minumun SK low time		1			µs
CK_{MAX}	Maximum frequency		DC		250	kHz

2

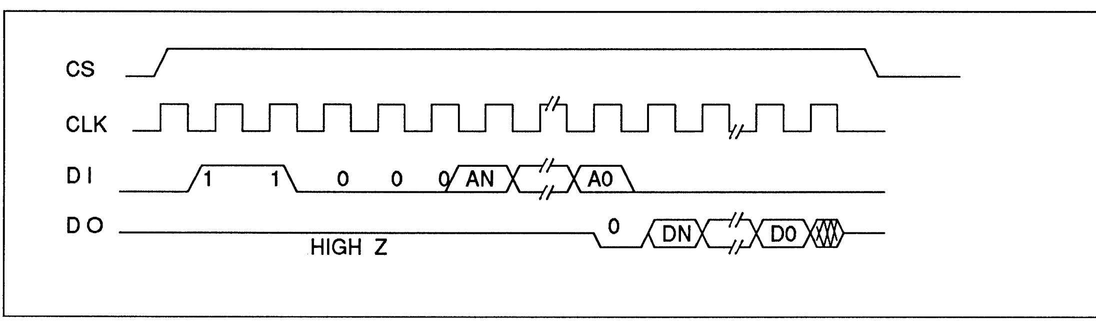
SYNCHRONOUS TIMINGS



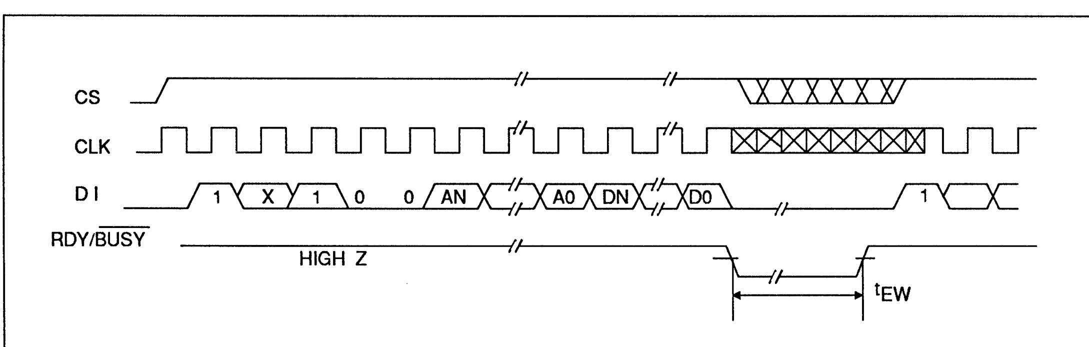
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

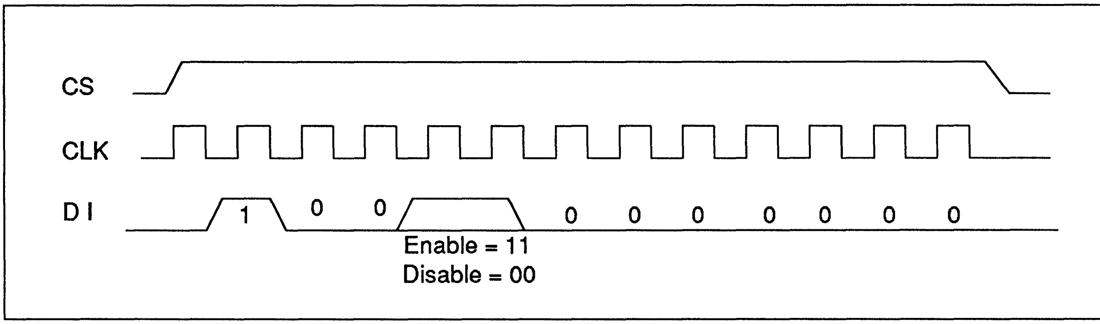
INSTRUCTION TIMING <READ>



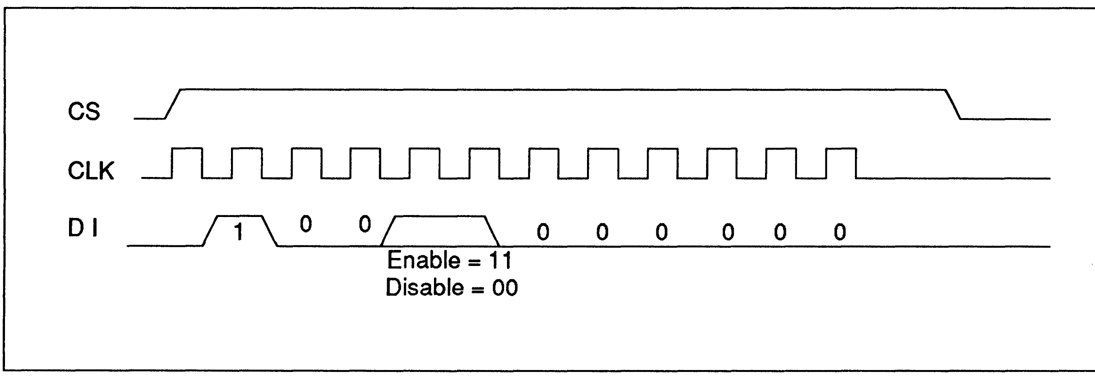
INSTRUCTION TIMING <PROGRAM>



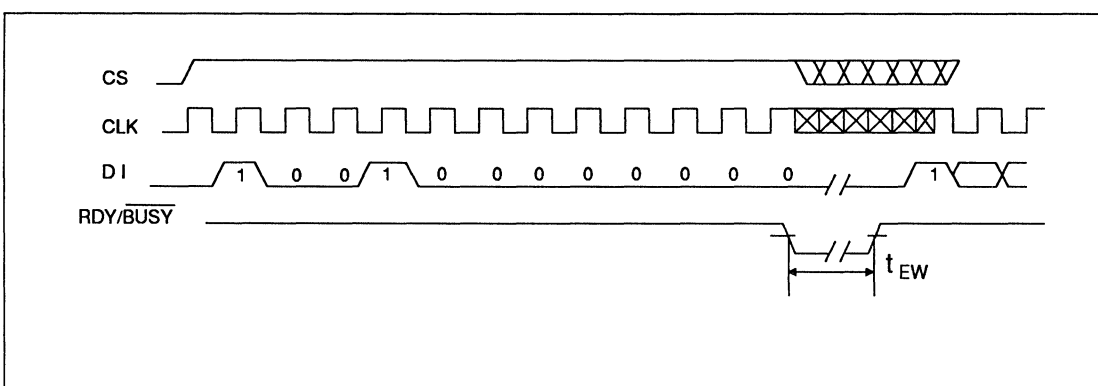
INSTRUCTION TIMING <PEN, PDS, for 128 x 8 organization>



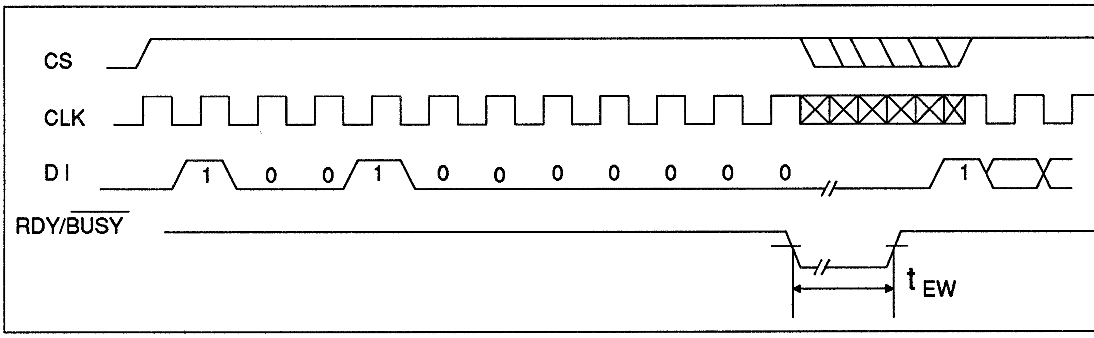
INSTRUCTION TIMING <PEN, PDS , for 64 x 16 organization>



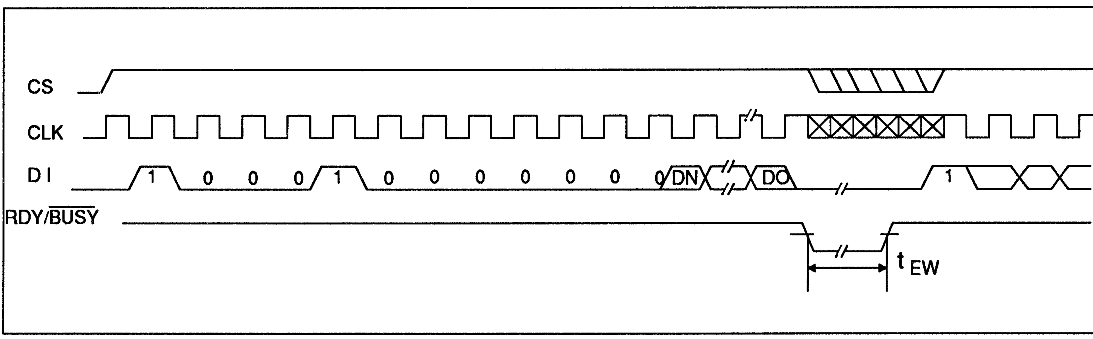
INSTRUCTION TIMING <ERAL, 128 x 8 organization>



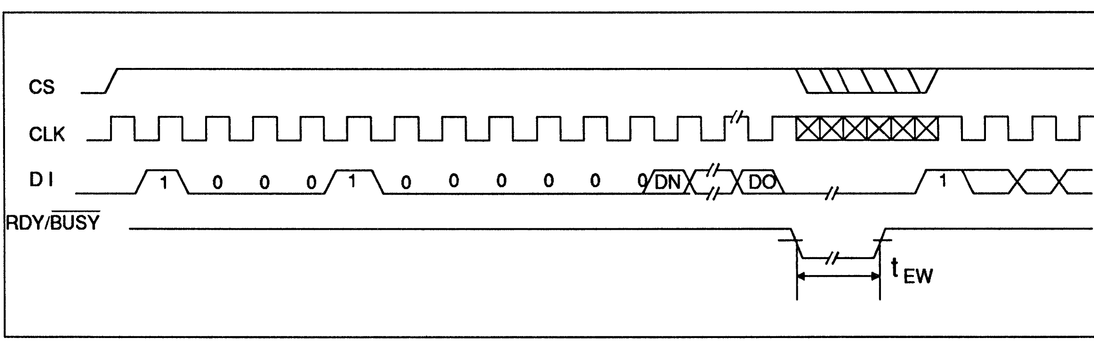
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11I is a 1024 bit non-volatile memory intended for use with all standard controllers. The CAT59C11I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six, 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11I operates on a single 5 Volt supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the CAT59C11I is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11I will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11I powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11I's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11I regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an WRAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT35C102
2K BIT SERIAL EEPROM

Preliminary

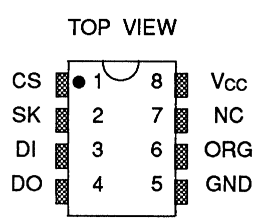
DESCRIPTION

The CAT35C102 is a 2K bit Serial EEPROM memory device organized in 128 registers of 16 bits (ORG pin at V_{CC}) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C102 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip or SO package. To be offered in a 3-volt version (CAT33C102).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- 128x16 or 256x8 user selectable serial memory
- Microwire ™ compatible
- Self timed programming cycle with Autoerase
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

PIN CONFIGURATION

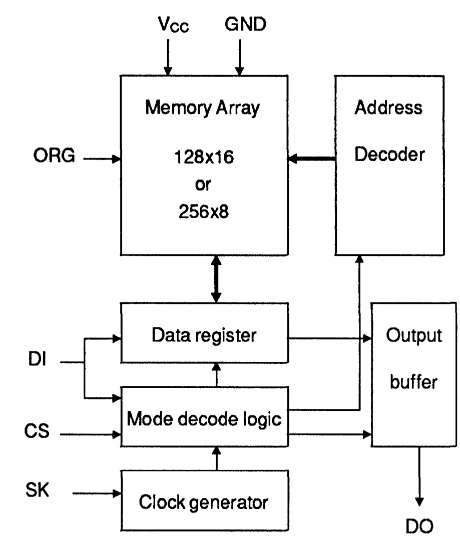


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the **ORG** pin is connected to +5V, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature T_{stg} . . . . -65°C to +150°C
Power supply V_{CC} . . . . +7 V
Voltage on any input pin . . . . -0.3 to +7V
Voltage on any output pin . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CC1}	Current consumption (operating)	V_{CC} =5.0V, CS = V_{IH} Output unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	μA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	μA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400μA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

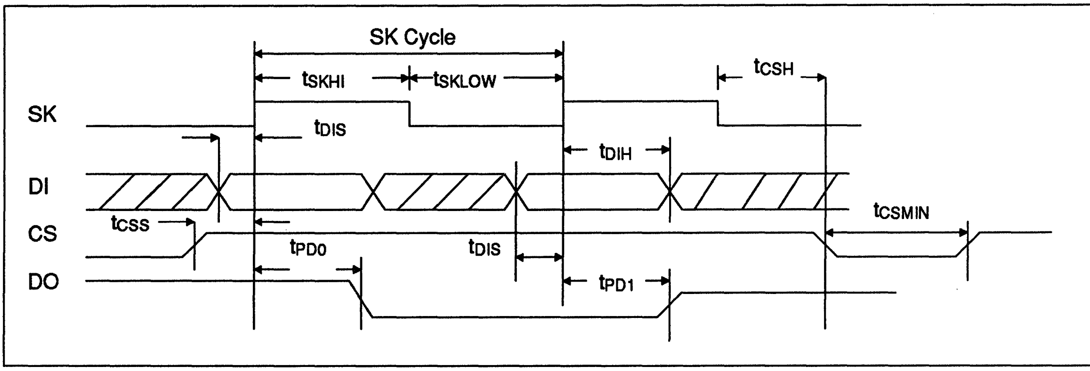
Instruction	Start Bit	Opcode	Address 256 x 8	Address 128 x 16	Data 256 x 8	Data 128 x 16	Comments
READ	1	1 0	A7 - A0	A6 - A0			Read address AN - A0
ERASE	1	1 1	A7 - A0	A6 - A0			ERASE address AN - A0
WRITE	1	0 1	A7 - A0	A6 - A0	D7 - D0	D15 - D0	WRITE address AN - A0
EWEN	1	0 0	11XXXXXX	11XXXXX			Program enable
EWDS	1	0 0	00XXXXXX	00XXXXX			Program disable
ERAL	1	0 0	10XXXXXX	10XXXXX			Erase all addresses
WRAL	1	0 0	01XXXXXX	01XXXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum frequency		DC		1	MHz

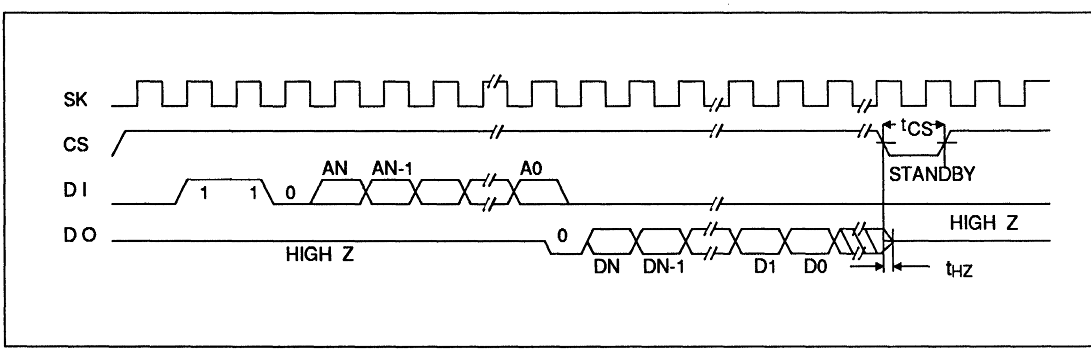
SYNCHRONOUS TIMINGS



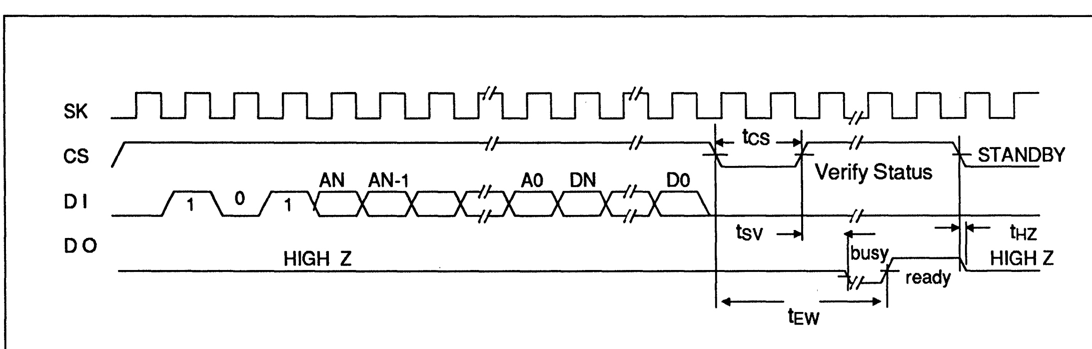
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

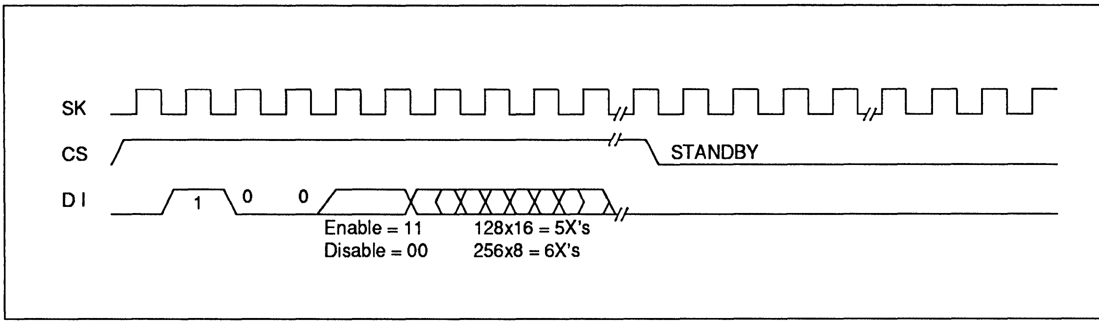
INSTRUCTION TIMING <READ>



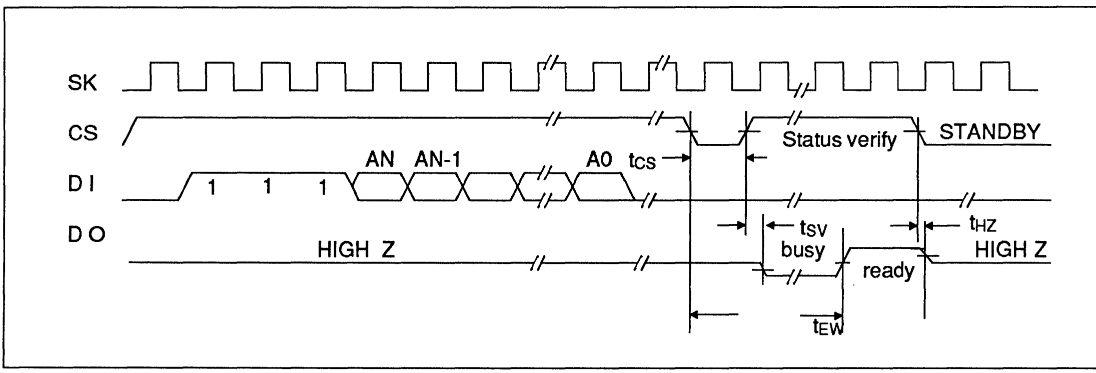
INSTRUCTION TIMING <WRITE>



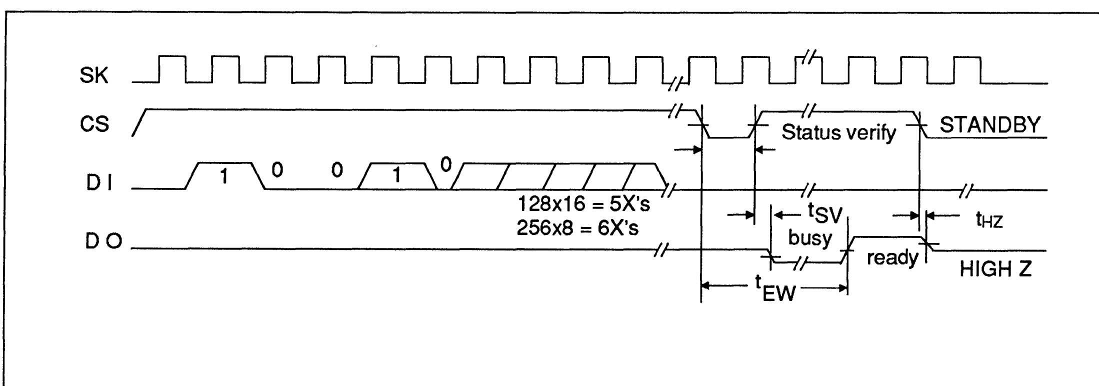
INSTRUCTION TIMING <EWENS, EWDS>



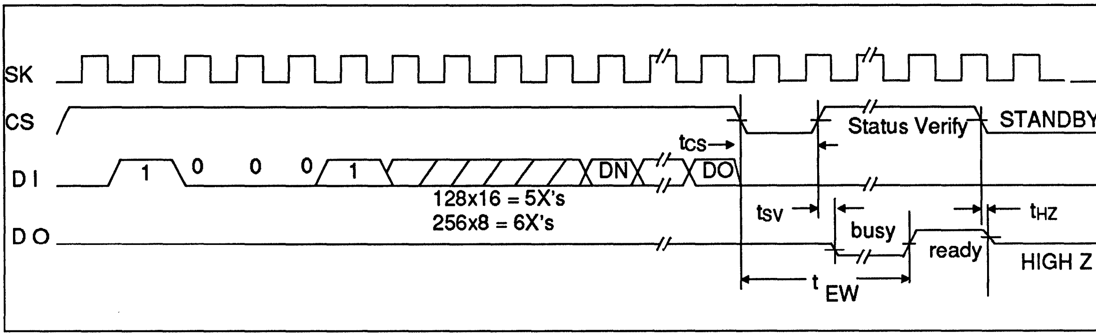
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C102 is a 2048 bit non-volatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT35C102 can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven, 10 bit instructions (11 bit instructions in 256 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C102 operates on a single 5 Volt supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the busy\ready status after a programming operation. The busy/ready status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C102 is 1 logical "1" start bit, a 2 bit (or 4 bit) op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C102 will come out of the high impedance state, after sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifting out. The data bits being shifted out will toggle on the rising edge of the SK clock is stable after the specified time delay t_{PD0} or t_{PD1}

ERASE/WRITE ENABLE AND DISABLE

The CAT35C102 powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C102 programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C102 regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C102 can be determined by selecting the device and polling the DO pin.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C102 can be determined by selecting the device and polling the DO pin. With the CAT35C102 it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERASE ALL command, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C102 can be determined by selecting the device and polling the DO pin.

WRITE ALL

Upon receiving a WRITE ALL command and data, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C102 can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRITE ALL command is executed.

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CAT35C202
2K BIT SERIAL EEPROM

Preliminary

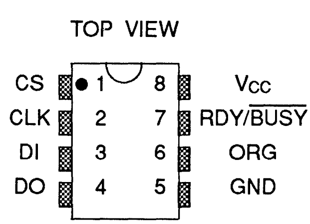
DESCRIPTION

The CAT35C202 is a 2K bit Serial EEPROM memory device organized in 128 registers of 16 bits (ORG pin at V_{CC}) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C202 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip and Small Outline packages. To be offered in a 3-volt version (CAT33C202).

FEATURES

- Highly reliable CMOS floating gate technology
- 10 ms programming cycle
- Single 5-volt supply
- 128x16 or 256x8 user selectable serial memory
- Compatible with General Instruments ER5912
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range $0^{o}C$ to $70^{o}C$ [Industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

PIN CONFIGURATION

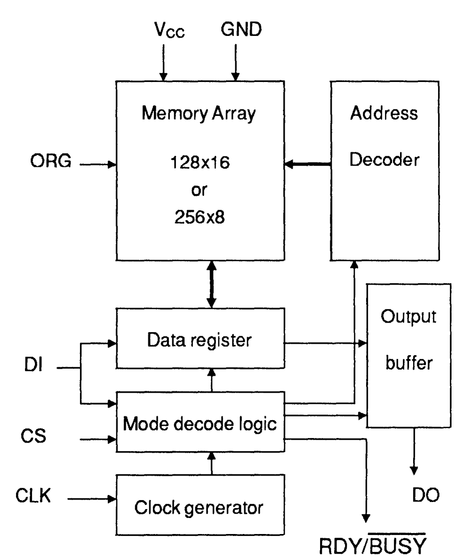


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/$\overline{\text{BUSY}}$	Status output
GND	Ground
ORG	Memory organization

Note: When the **ORG** pin is connected to +5V, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC1}	Current consumption (operating)	V_{CC} =5.0V, CS = 1 DO unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	VCC = 5.5V, CS = 0 DI = 0, SK = 0			100	μA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	μA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400μA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address 256 x 8	Address 128 x 16	Data 256 x 8	Data 128 x 16	Comments
READ	1	1000	A7 - A0	A6 - A0			Read address AN - A0
PROGRAM	1	X100	A7 - A0	A6 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	00000000	0000000			Program enable
PDS	1	0000	00000000	0000000			Program disable
ERAL	1	0010	00000000	0000000			Erase all addresses
WRAL	1	0001	00000000	0000000	D7 - D0	D15 - D0	Write all addresses

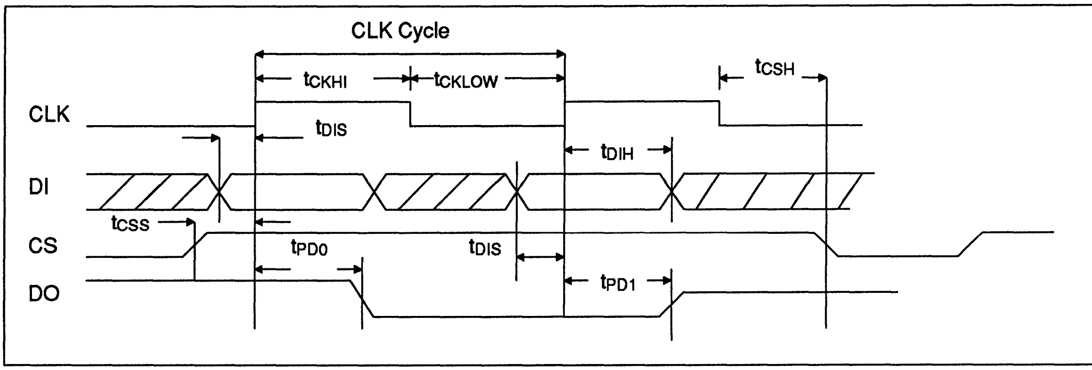
AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
CK_{MAX}	Maximum frequency		DC		1	MHz

2

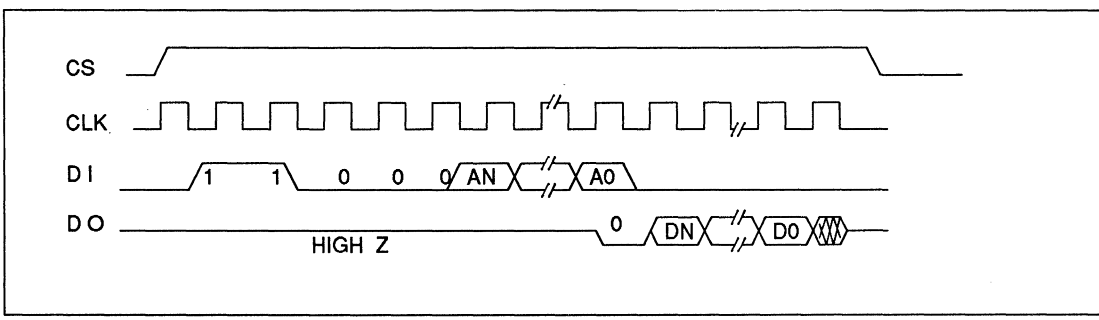
SYNCHRONOUS TIMINGS



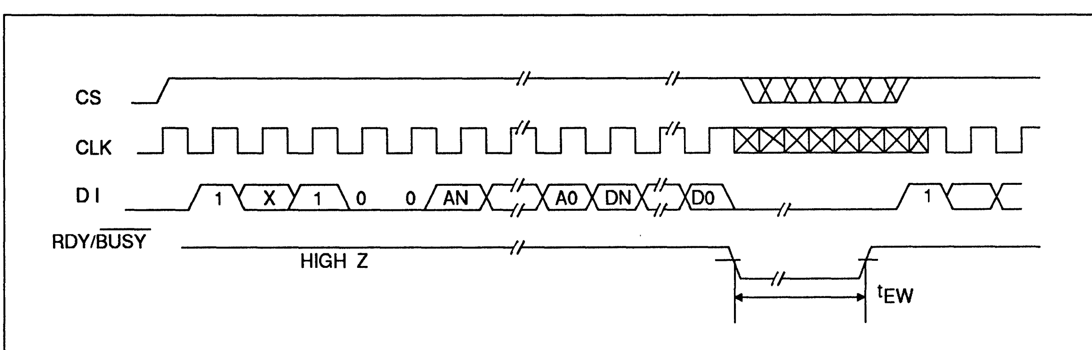
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

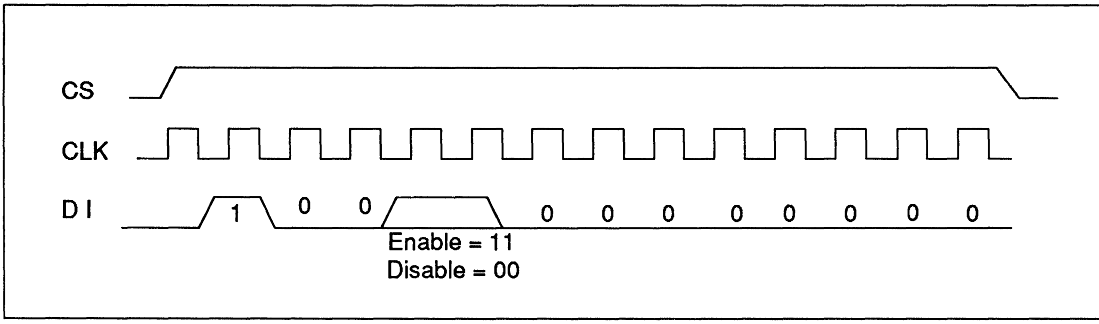
INSTRUCTION TIMING <READ>



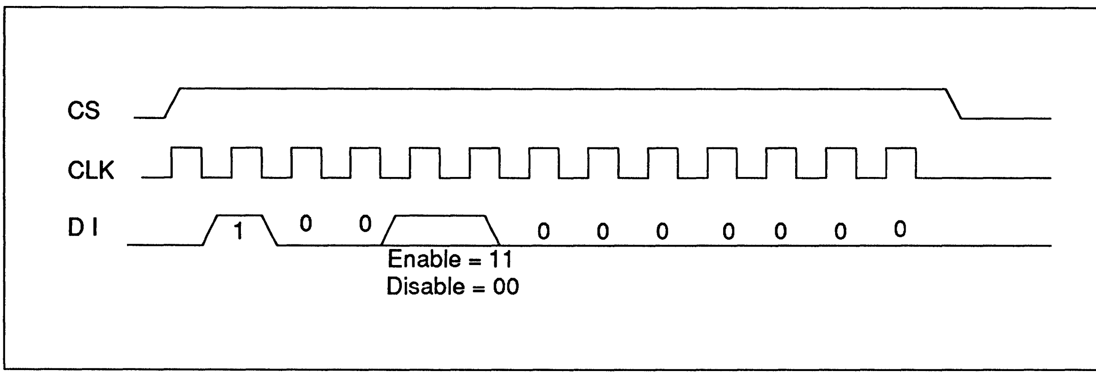
INSTRUCTION TIMING <PROGRAM>



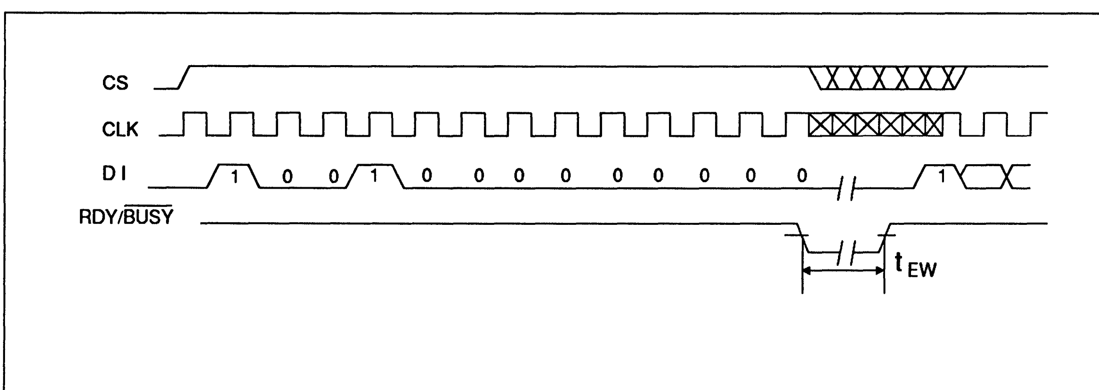
INSTRUCTION TIMING <PEN, PDS, for 256 x 8 organization>



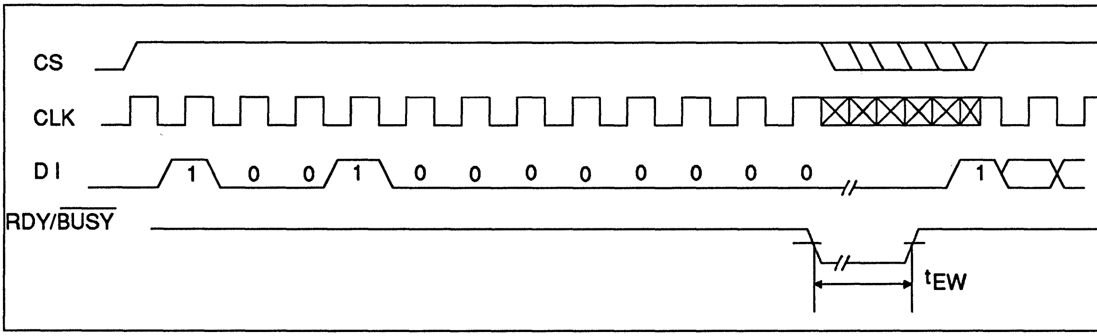
INSTRUCTION TIMING <PEN, PDS , for 128 x 16 organization>



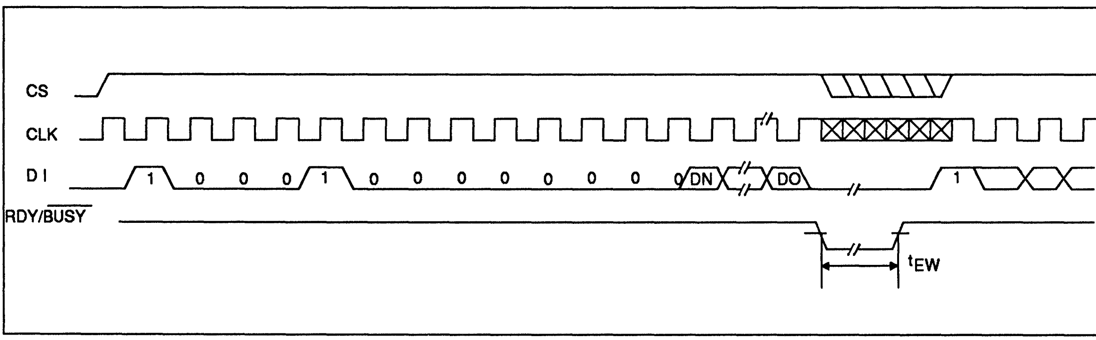
INSTRUCTION TIMING <ERAL, 256 x 8 organization>



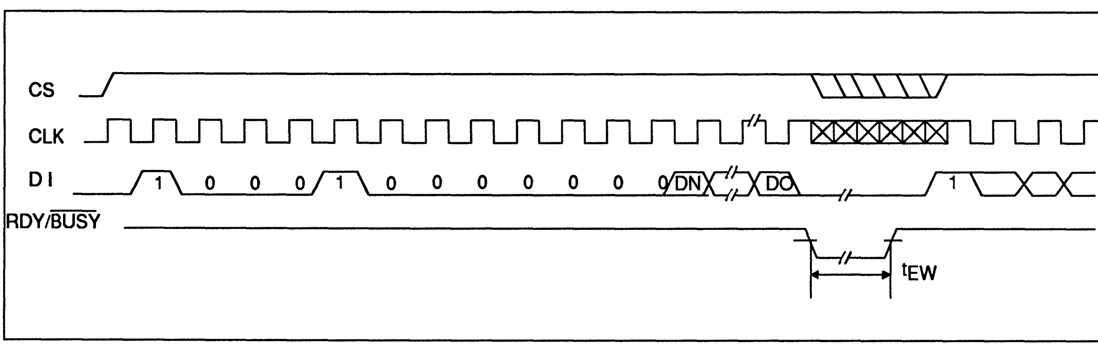
INSTRUCTION TIMING <ERAL 128 x 16 organization>



INSTRUCTION TIMING <WRAL 256 x 8 organization>



INSTRUCTION TIMING <WRAL 128 x 16 organization>



DEVICE OPERATION

The CAT35C202 is a 2048 bit non-volatile memory intended for use with all standard controllers. The CAT35C202 can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Six, 12 bit instructions (13 bit instruction in 256 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C202 operates on a single 5 Volt supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{BUSY}$ pin.

The format for all instructions sent to the CAT35C202 is one logical "1" start bit, a 4 bit op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C202 will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C202 powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT35C202's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C202 regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/BUSY pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202 can be determined by polling the RDY/BUSY pin.

ERASE ALL

Upon receiving an WRAL command, the RDY/BUSY pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202 can be determined by polling the RDY/BUSY pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/BUSY pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202 can be determined by polling the RDY/BUSY pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT35C104
4K BIT SERIAL EEPROM

Preliminary

DESCRIPTION

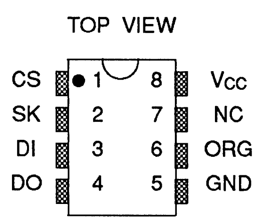
The CAT35C104* is a 4K bit Serial EEPROM memory device organized in 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C104 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin dip or SO package. To be offered in a 3-volt version (CAT33C104).

* Available in G.I. compatible protocol CAT35C204. Also to be offered in a 3-volt version (CAT33C204).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- Available in 8 pin DIP or S.O. package
- 256x16 or 512x8 user selectable serial memory
- Mircowire ™ compatible
- Self timed programming cycle with Autoerase
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-on data protection

PIN CONFIGURATION

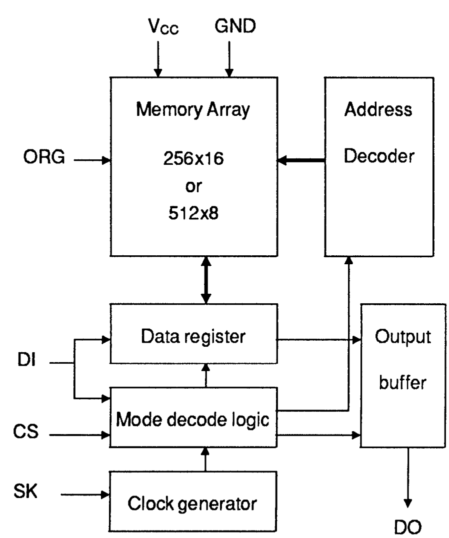


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the **ORG** pin is connected to +5V, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	V_{CC} =5.0V, CS = V_{IH} Output unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1 0	A8 - A0	A7 - A0			Read address AN - A0
ERASE	1	1 1	A8 - A0	A7 - A0			ERASE address AN - A0
WRITE	1	0 1	A8 - A0	A7 - A0	D7 - D0	D15 - D0	WRITE address AN - A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Program enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Program disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Erase all addresses
WRAL	1	0 0	01XXXXXXX	01XXXXXX	D7 - D0	D15 - D0	Program all addresses

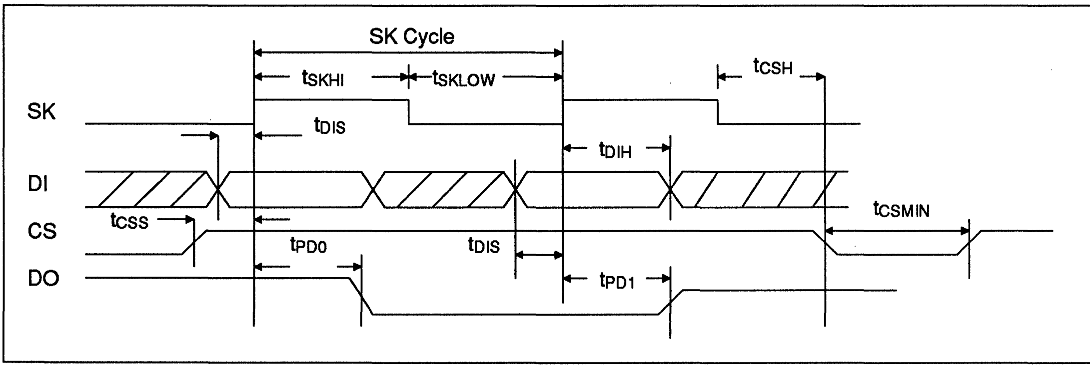
AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0 V_{IL} = 0.45, V_{IH} = 2.4	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum frequency		DC		1	MHz

2

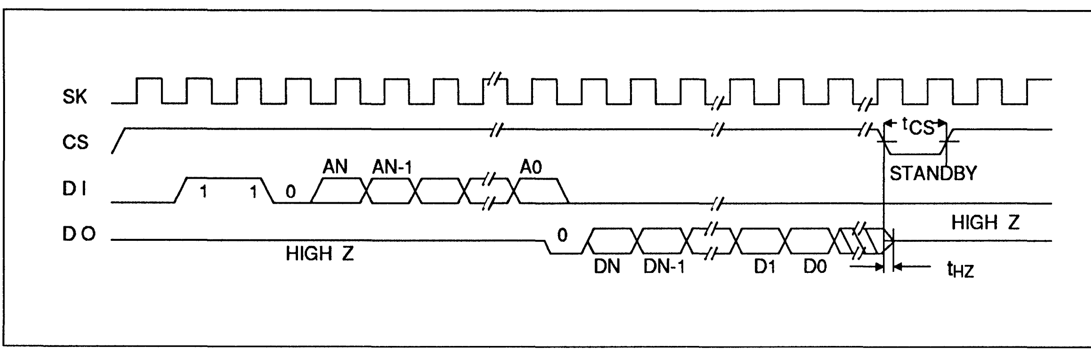
SYNCHRONOUS TIMINGS



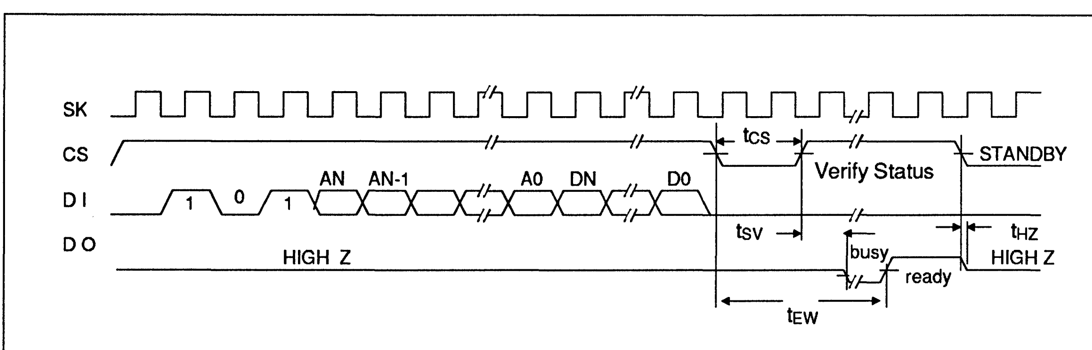
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

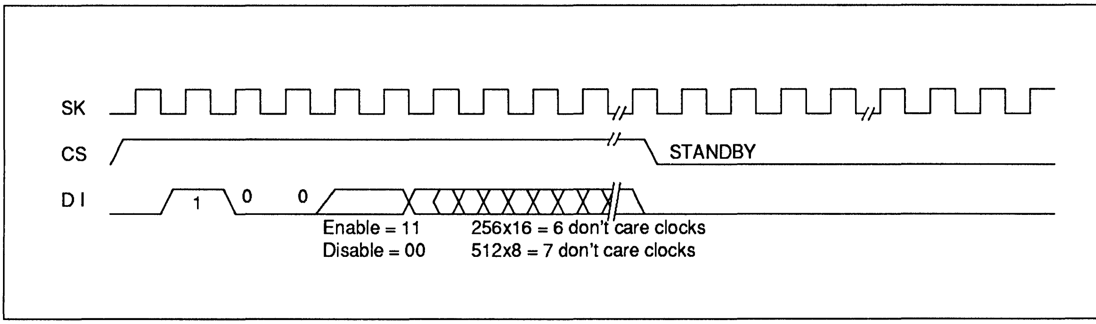
INSTRUCTION TIMING <READ>



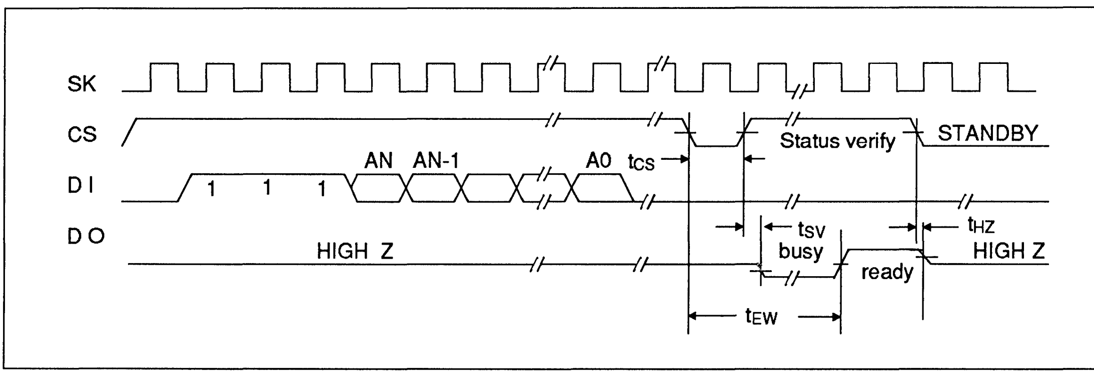
INSTRUCTION TIMING <WRITE>



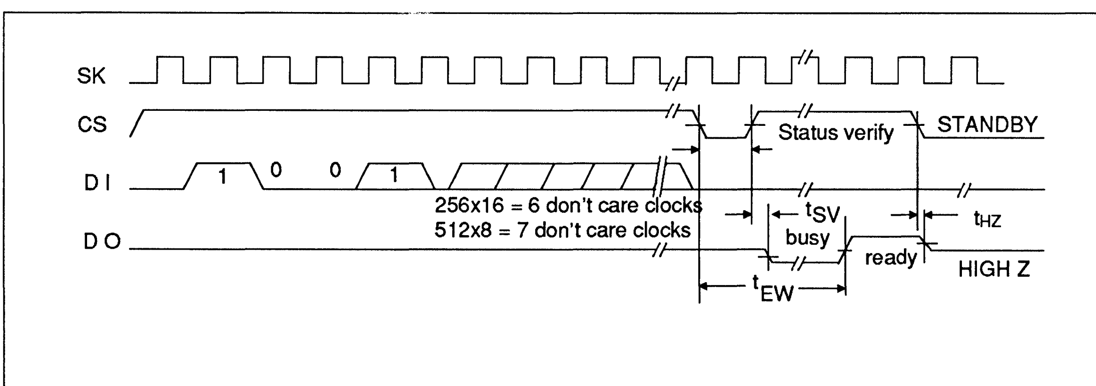
INSTRUCTION TIMING <EWENS, EWDS>



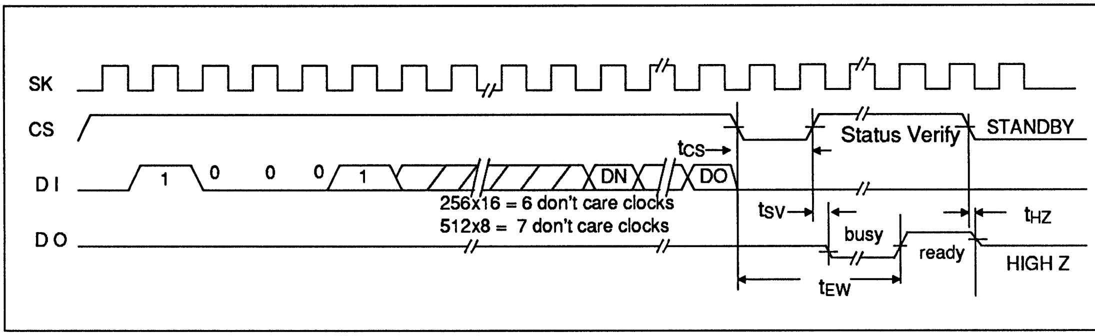
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C104 is a 4096 bit non-volatile memory intended for use with the COPS^{TM} family of microcontrollers, or other standard microprocessors such as the 8048, or 8051. The CAT35C104 can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Seven, 11 bit instructions (12 bit instructions in 512 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C104 operates on a single 5 Volt supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the busy/ready status after a programming operation. The busy/ready status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C104 is 1 logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C104 will come out of the high impedance state, after sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifting out. The data bits being shifted out will toggle on the rising edge of the SK clock is stable after the specified time delay t_{PD0} or t_{PD1}

ERASE/WRITE ENABLE AND DISABLE

The CAT35C104 powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C104 programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C102 regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C104 can be determined by selecting the device and polling the DO pin.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C104 can be determined by selecting the device and polling the DO pin. With the CAT35C104 it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERASE ALL command, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C104 can be determined by selecting the device and polling the DO pin.

WRITE ALL

Upon receiving a WRITE ALL command and data, the CS (chip select) must be deselected for a minimum of 250 ns (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The BUSY/READY status of the CAT35C104 can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRITE ALL command is executed.

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CAT28C16A, CAT28C16AI [Industrial Temperature]
2Kx8 BIT CMOS EEPROM

DESCRIPTION

The CAT28C16A is a fast, low power, 5V-only CMOS EEPROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time.

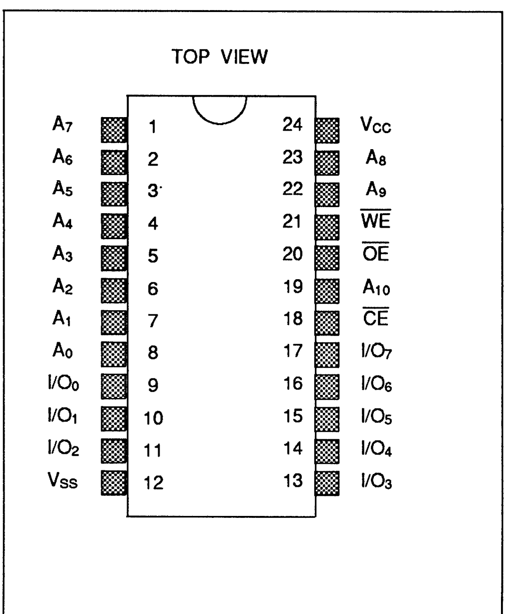
The CAT28C16A is fabricated in reliable floating gate CMOS technology. It is designed for up to10,000 write cycles and 10 years data retention.

FEATURES

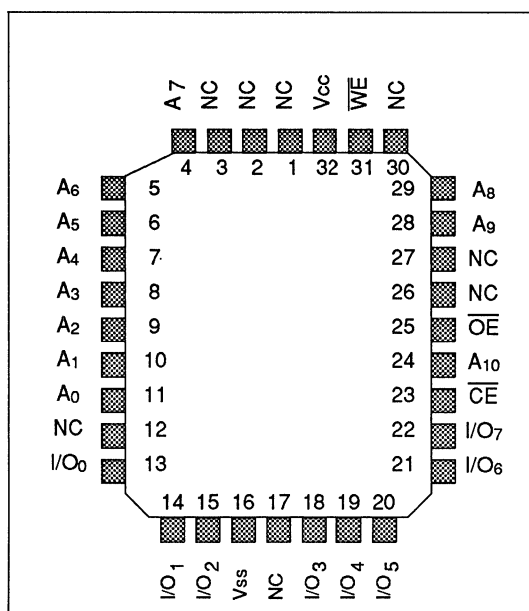
- Access time - 150 ns. and 200 ns.
- Low CMOS power:
  Active - 25 mA max
  Standby - 100µA max
- 5V-only operation
- Simple write operation:
  On-chip address and data latches
  Self-timed write cycle with auto-erase
  Data polling
  Power up/down write protection
- Fast write cycle time
  10 ms max byte write, 5 ms available
- Reliable floating gate CMOS technology
- JEDEC approved 24 pin DIP,Small Outline, and 32 pin PLCC packages available.

PIN CONFIGURATION

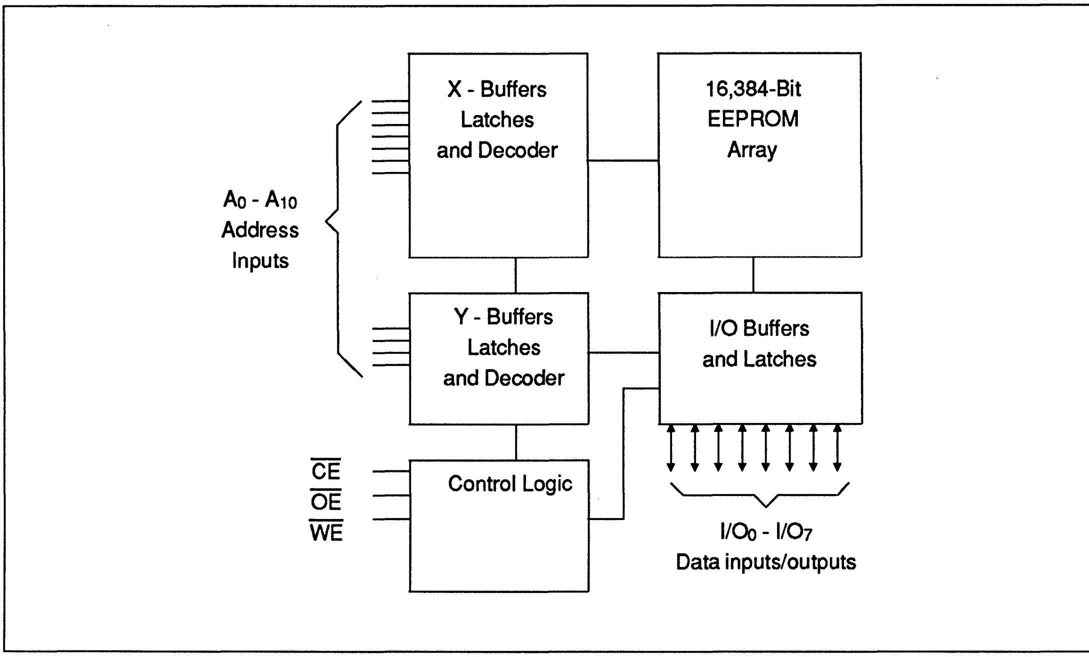
PIN CONFIGURATION 24-Pin DIP, and S.O.



PIN CONFIGURATION 32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{10}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . -40°C to +85°C
Storage temperature . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . -0.5 to +7V
Voltage on any output pin relative to V_{SS} . . . . -0.5 to V_{CC} +0.5V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT2816A T_A = 0°C to +70°C, CAT2816AI T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz, all I/O's = open			35	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=6.7MHz, all I/O's = open			25	mA
I_{SB}	V_{CC} current (stand-by, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (stand-by, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0	3.5		V

Note:
* V_{ILC} = -0.3V to +0.3V
** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 1.0V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write	L	‾‾╲_╱‾‾	H	D_{IN}	ACTIVE
Standby and write inhibit	H	X	X	HIGH Z	STANDBY
Write inhibit	X	X	L		
Write inhibit	X	H	X		
Chip erase	L	L	12V	HIGH Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4 V
Input rise and fall times	10 ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0 V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

CAT2816A T_A = 0°C to +70°C, CAT2816AI T_A = -40°C to +85°C, V_{CC} = +5V ±10%

Symbol	Parameter	28C16A-15 Min.	28C16A-15 Max.	28C16A-20 Min.	28C16A-20 Max.	Units
t_{RC}	Read cycle time	150		200		ns
t_{CE}	CE access time		150		200	ns
t_{AA}	Address access time		150		200	ns
t_{OE}	OE access time		70		80	ns
t_{LZ}	CE low to active output	10		10		ns
t_{OLZ}	OE low to active output	10		10		ns
t_{HZ}	CE high to high Z output	10	50	10	55	ns
t_{OHZ}	OE high to high Z output	10	50	10	55	ns
t_{OH}	Output hold from address change	20		20		ns

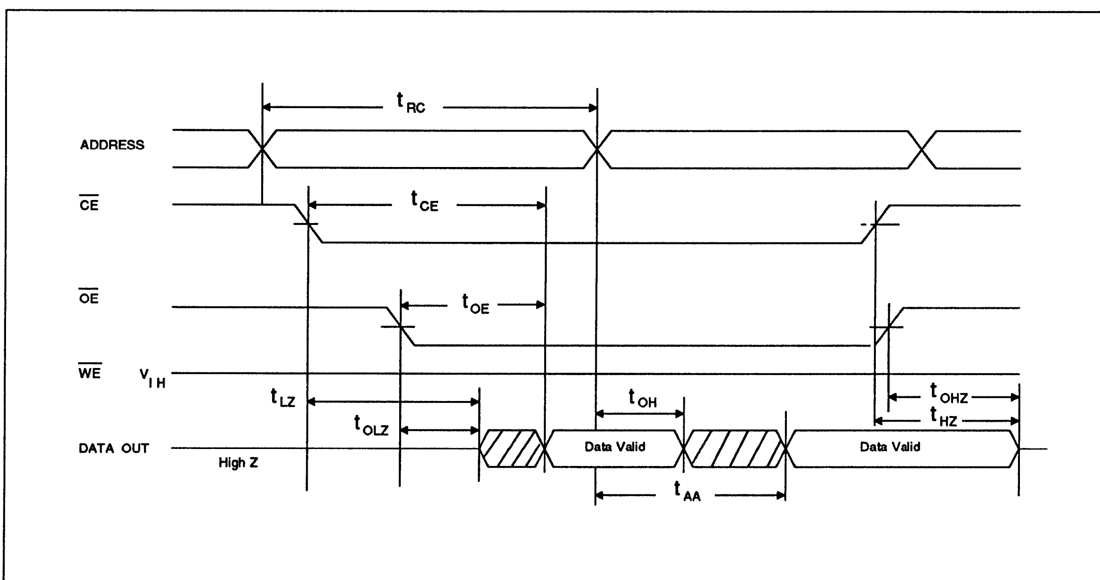
AC CHARACTERISTICS <Write Cycle>

(CAT2816A T_A = 0°C to +70°C, CAT2816AI T_A = -40°C to +85°C, V_{CC} = +5V ±10%)

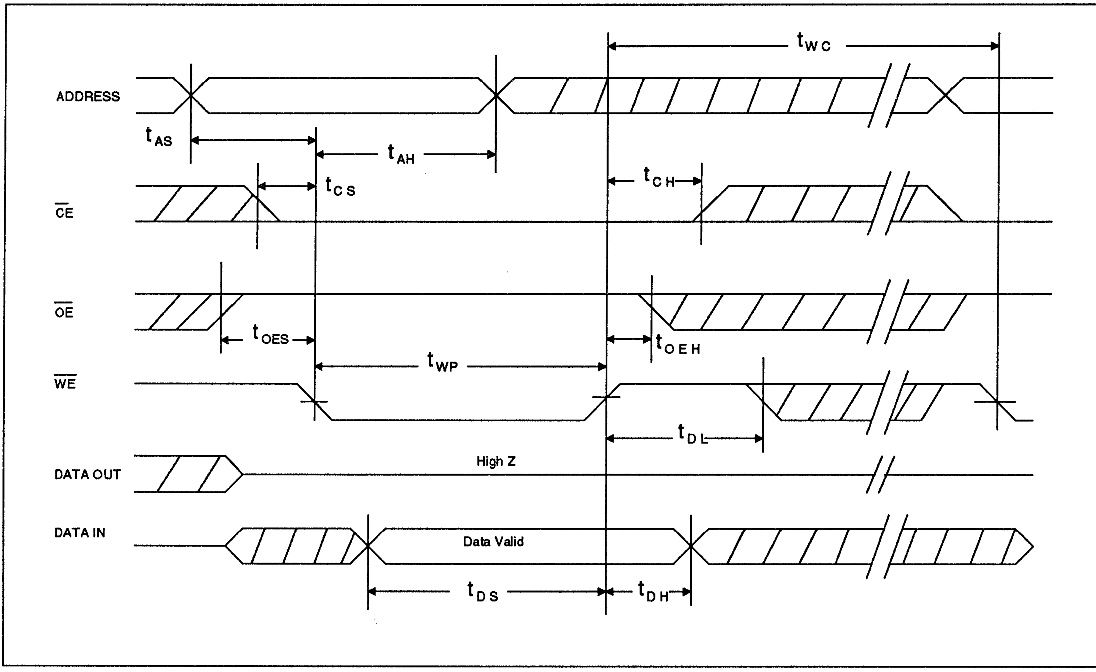
Symbol	Parameter	28C16A-15 Min	28C16A-15 Max	28C16A-20 Min	28C16A-20 Max	Units
t_{WC}	Write cycle time		10		10	ms
t_{AS}	Address setup time	10		10		ns
t_{AH}	Address hold time	70		100		ns
t_{CS}	Write setup time	0		0		ns
t_{CH}	Write hold time	0		0		ns
t_{CW} *	$\overline{CE}$ pulse time	100		150		ns
t_{OES}, t_{OEH}	$\overline{OE}$ setup time, $\overline{OE}$ hold time	10		15		ns
t_{WP} *	$\overline{WE}$ pulse width	100		150		ns
t_{DL}	Data latch time	50		50		ns
t_{DS}	Data setup time	50		50		ns
t_{DH}	Data hold time	10		10		ns
t_{INIT}	Write inhibit period after power-up	5	20	5	20	ms

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

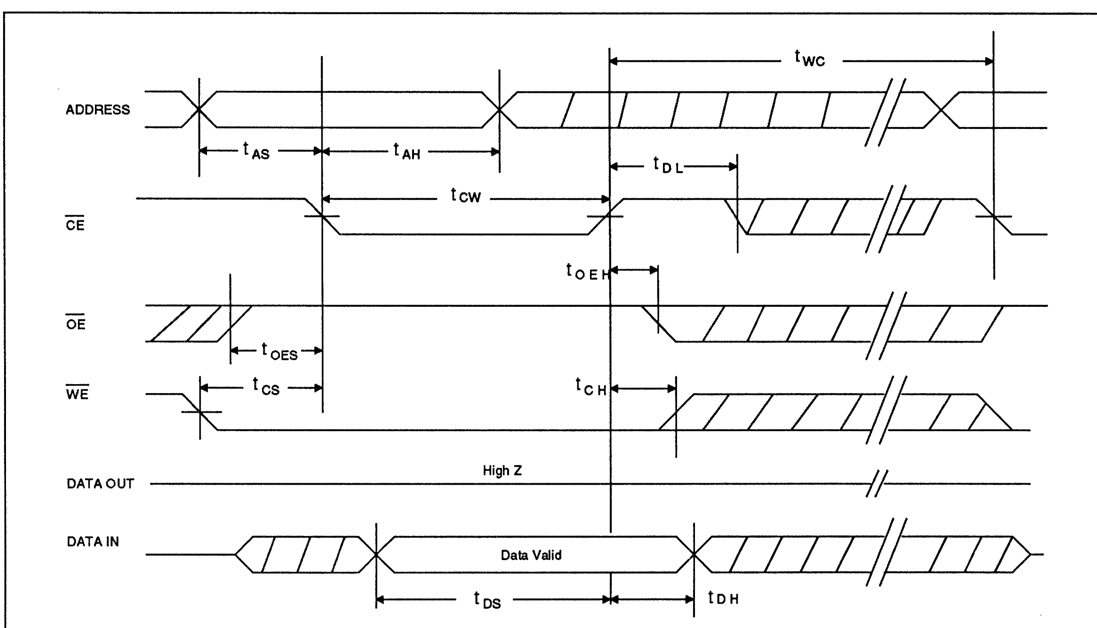
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{10})

The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)

The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)

The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)

Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)

The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

DEVICE OPERATION

READ

Device data is output to the data bus when both $\overline{OE}$ and $\overline{CE}$ are LOW. The data bus is high impedance when either $\overline{CE}$ or $\overline{OE}$ go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. Both $\overline{CE}$ and $\overline{WE}$ controlled write cycles can be executed, i.e., the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last, while data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

DATA POLLING

Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION

(I) The CAT28C16A has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

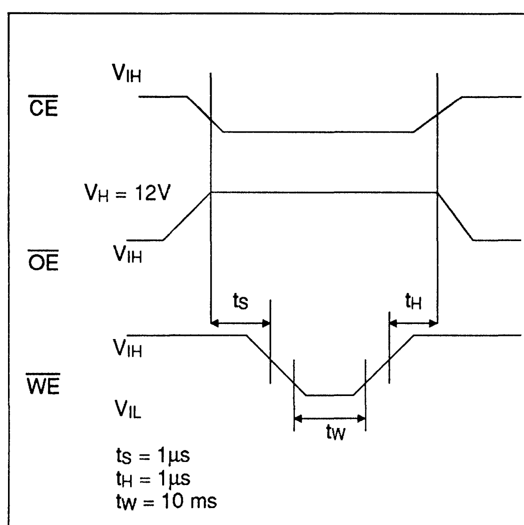
(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 3.0V. Read cycles are not affected during this initialization period.

(3) Write cycles are inhibited if $\overline{OE}$ is LOW, or $\overline{CE}$ or $\overline{WE}$ are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

CHIP ERASE

The entire memory can be set to 1's by setting $\overline{CE}$ LOW, $\overline{OE}$ to 12V, and pulsing $\overline{WE}$ LOW for 10ms.



CAT28C17A, CAT28C17AI [Industrial Temperature]
2Kx8 BIT CMOS EEPROM

DESCRIPTION

The CAT28C17A is a fast, low power, 5V-only CMOS EEPROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling and a RDY/$\overline{BUSY}$ pin are provided to allow the user to minimize write cycle time.

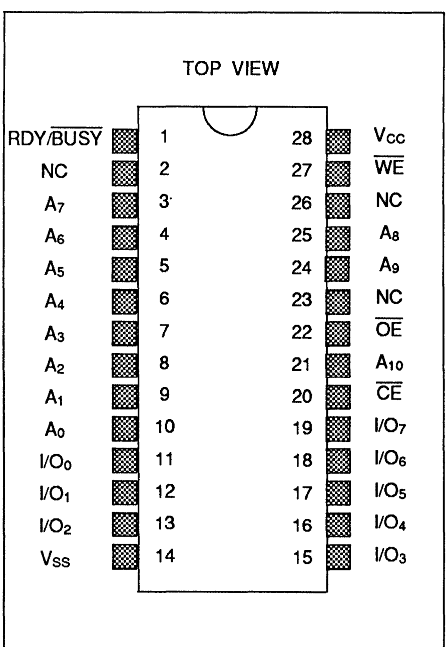
The CAT28C17A is fabricated in reliable floating gate CMOS technology. It is designed for up to10,000 write cycles and 10 years data retention.

FEATURES

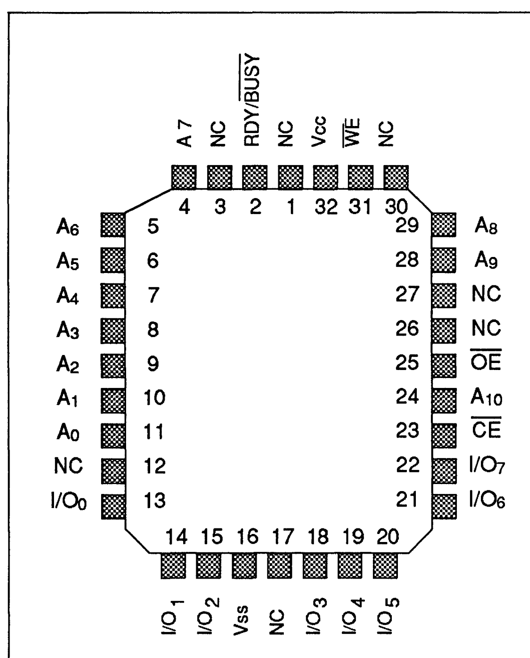
- Access time - 150 ns. and 200 ns.
- Low CMOS power:
  Active - 25 mA max.
  Standby - 100µA max.
- 5V-only operation
- Simple write operation:
  On-chip address and data latches
  Self-timed write cycle with auto-erase
  Data polling
  Power up/down write protection
- Fast write cycle time
  10 ms max. byte write, 5 ms available
- Reliable floating gate CMOS technology
- JEDEC approved 28 pin DIP,Small Outline, and 32 pin PLCC packages available.

PIN CONFIGURATION

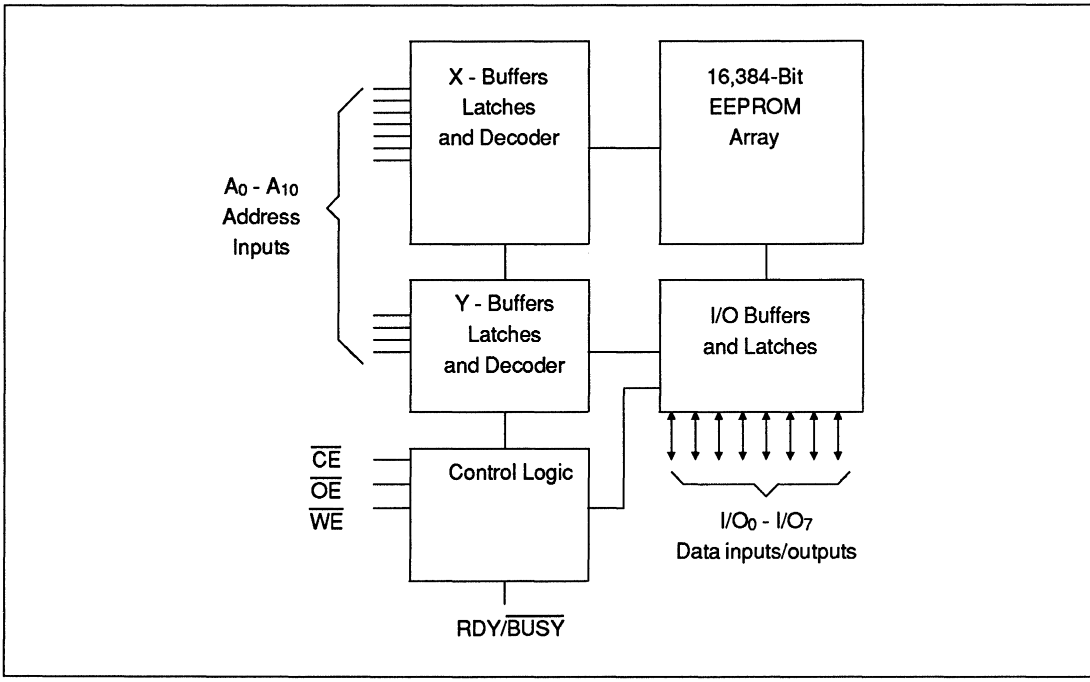
PIN CONFIGURATION 28-Pin DIP, and S.O.



PIN CONFIGURATION 32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{10}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
RDY/$\overline{BUSY}$	Ready/Busy indicator
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . -40°C to +85°C
Storage temperature . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . -0.5 to +7V
Voltage on any output pin relative to V_{SS} . . . . -0.5 to V_{CC} +0.5V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT28C17A T_A = 0°C to +70°C, CAT28C17AI T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz, all I/O's = open			35	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=6.7MHz, all I/O's = open			25	mA
I_{SB}	V_{CC} current (stand-by, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (stand-by, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0	3.5		V

Note:
* V_{ILC} = -0.3V to +0.3V
** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 1.0V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write	L	‾_/‾	H	D_{IN}	ACTIVE
Standby and write inhibit	H	X	X	HIGH Z	STANDBY
Write inhibit	X	X	L		
Write inhibit	X	H	X		
Chip erase	L	L	12V	HIGH Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4 V
Input rise and fall times	10 ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0 V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

CAT28C17A T_A = 0°C to +70°C, CAT28C17AI T_A = -40°C to +85°C, V_{CC} = +5V ±10%

Symbol	Parameter	28C17A-15 Min	28C17A-15 Max	28C17A-20 Min	28C17A-20 Max	Units
t_{RC}	Read cycle time	150		200		ns
t_{CE}	CE access time		150		200	ns
t_{AA}	Address access time		150		200	ns
t_{OE}	OE access time		70		80	ns
t_{LZ}	CE low to active output	10		10		ns
t_{OLZ}	OE low to active output	10		10		ns
t_{HZ}	CE high to high Z output	10	50	10	55	ns
t_{OHZ}	OE high to high Z output	10	50	10	55	ns
t_{OH}	Output hold from address change	20		20		ns

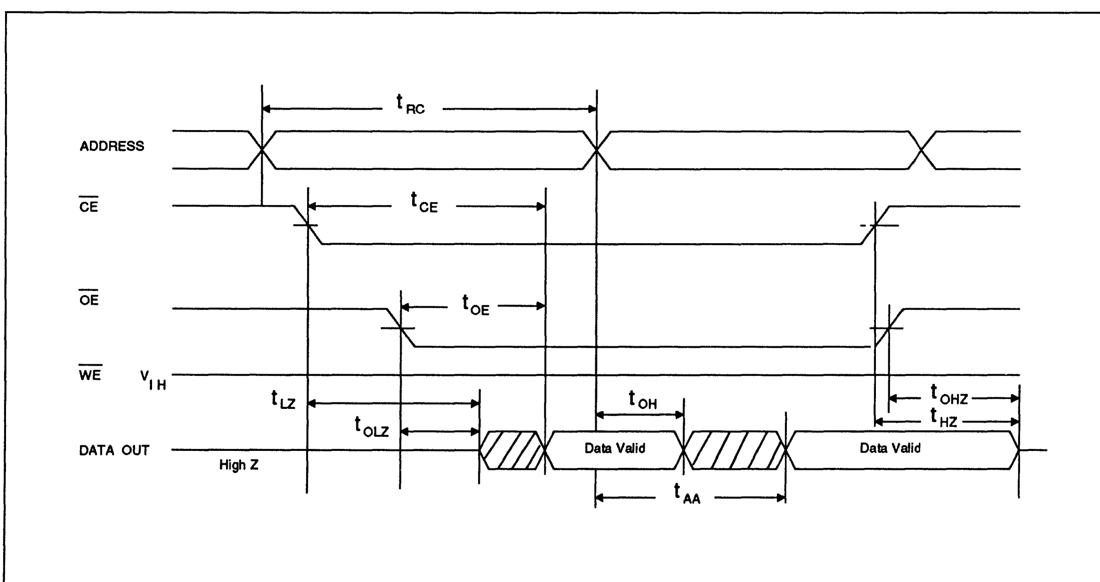
AC CHARACTERISTICS <Write Cycle>

(CAT28C17A T_A = 0°C to +70°C, CAT28C17AI T_A = -40°C to +85°C, V_{CC} = +5V ±10%)

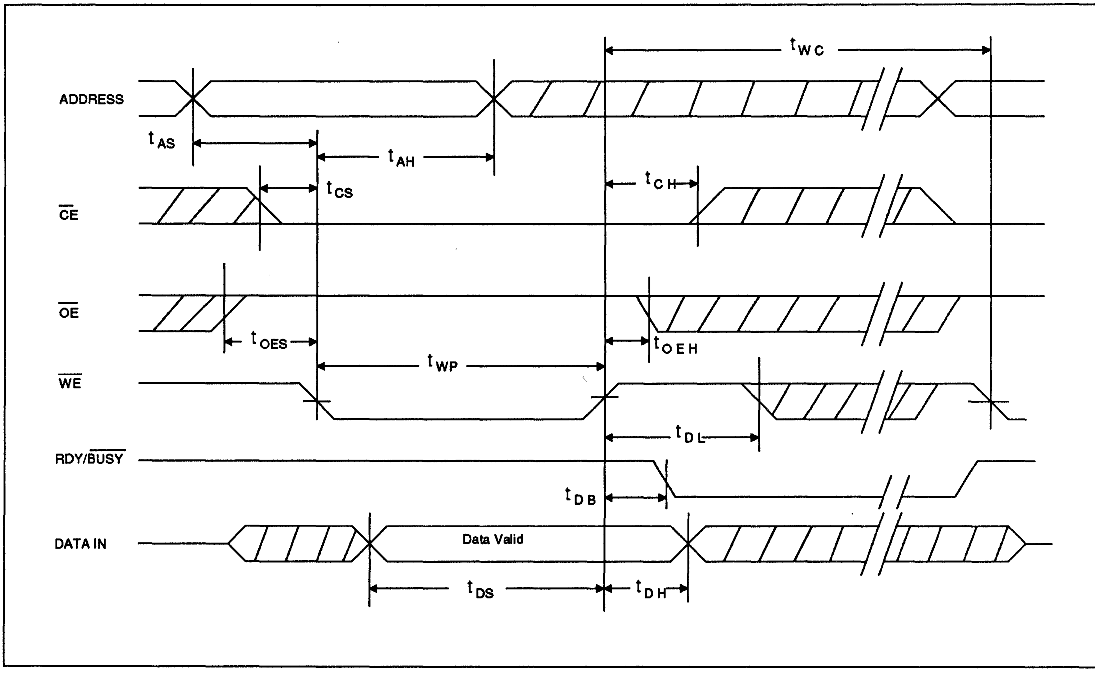
Symbol	Parameter	28C17A-15 Min	28C17A-15 Max	28C17A-20 Min	28C17A-20 Max	Units
t_{WC}	Write cycle time		10		10	ms
t_{AS}	Address setup time	10		10		ns
t_{AH}	Address hold time	70		100		ns
t_{CS}	Write setup time	0		0		ns
t_{CH}	Write hold time	0		0		ns
t_{CW} *	$\overline{CE}$ pulse time	100		150		ns
t_{OES}, t_{OEH}	$\overline{OE}$ setup time, $\overline{OE}$ hold time	10		15		ns
t_{WP} *	$\overline{WE}$ pulse width	100		150		ns
t_{DL}	Data latch time	50		50		ns
t_{DS}	Data setup time	50		50		ns
t_{DH}	Data hold time	10		10		ns
t_{INIT}	Write inhibit period after power-up	5	20	5	20	ms
t_{DB}	Time to device busy		70		80	ns

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

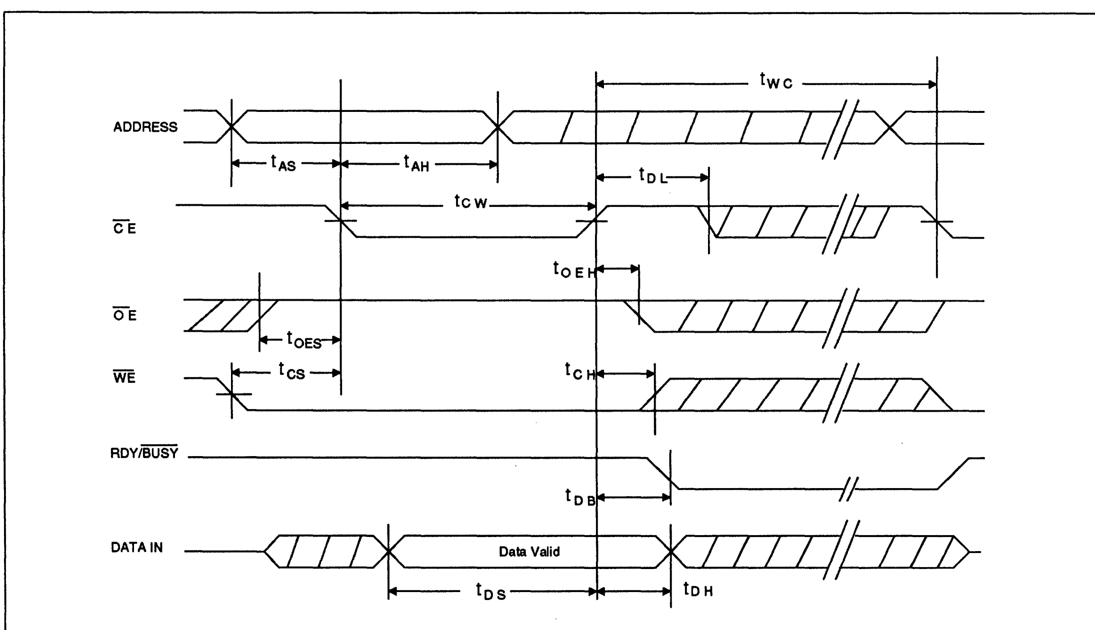
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{10})

The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)

The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)

The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)

Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)

The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

READ/BUSY (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. This output is pulled low during the write cycle and released at the end of programming., Several devices may be OR-tyed to the same RDY/$\overline{BUSY}$ line.

DEVICE OPERATION

READ

Device data is output to the data bus when both $\overline{OE}$ and $\overline{CE}$ are LOW. The data bus is high impedance when either $\overline{CE}$ or $\overline{OE}$ go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. Both $\overline{CE}$ and $\overline{WE}$ controlled write cycles can be executed, i.e., the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last, while data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

DATA POLLING

Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION

(l) The CAT28C17A has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

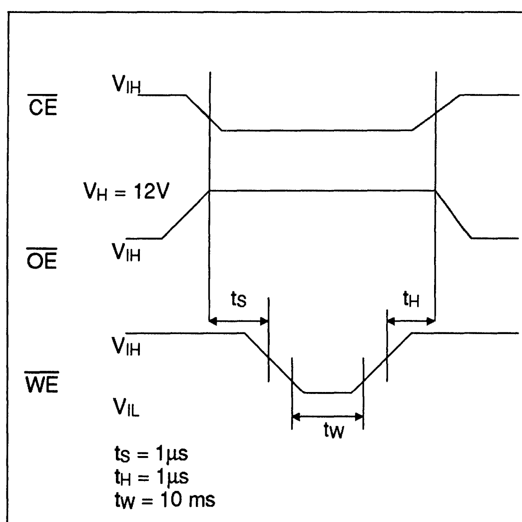
(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 3.0V. Read cycles are not affected during this initialization period.

(3) Write cycles are inhibited if $\overline{OE}$ is LOW, or $\overline{CE}$ or $\overline{WE}$ are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

CHIP ERASE

The entire memory can be set to 1's by setting $\overline{CE}$ LOW, $\overline{OE}$ to 12V, and pulsing $\overline{WE}$ LOW for 10ms.



CAT28C64A
8K x 8 BIT CMOS EEPROM

DESCRIPTION

The CAT28C64A is a fast, low power, 5V-only CMOS EEPROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time. Page write mode reduces programming time.

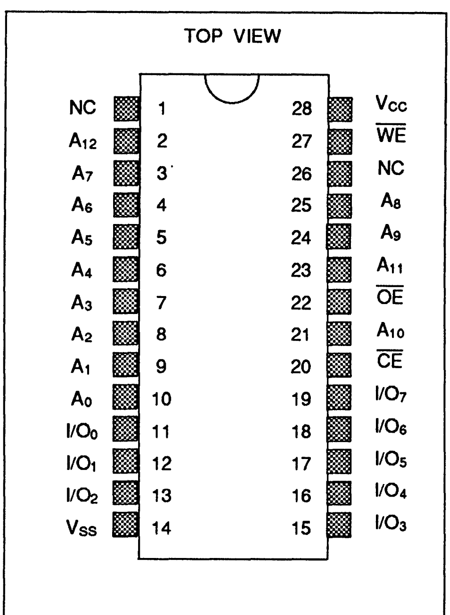
The CAT28C64A is fabricated in reliable floating gate CMOS technology. It is designed for up to10,000 write cycles and 10 years data retention.

FEATURES

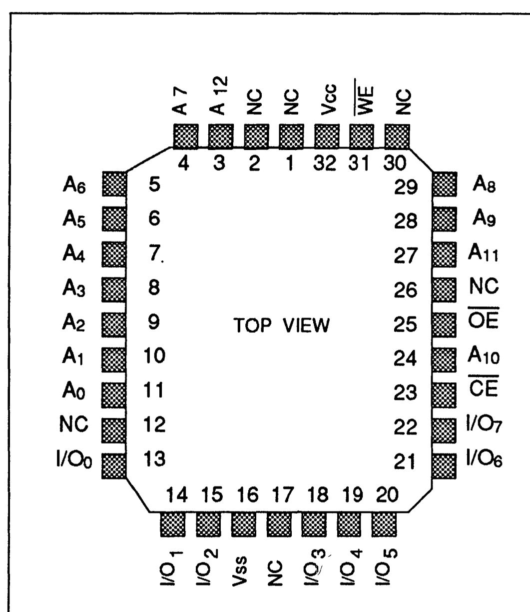
- Fast read access time: 150ns/200ns/250ns
- Low CMOS power:
  - Active 30 mA max., Standby 100µA max.
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
- Power up/down and software write protection
- Fast nonvolatile write cycle: 5 ms max.
- Automatic page write: 1 to 32 bytes in 5 ms
- TTL compatible I/O
- JEDEC approved 28 pin DIP,Small Outline, and 32 pin PLCC packages available.
- 10,000 rewrites/byte, 10 year data retention
- Effective byte-write cycle of 156 µs./byte

PIN CONFIGURATION

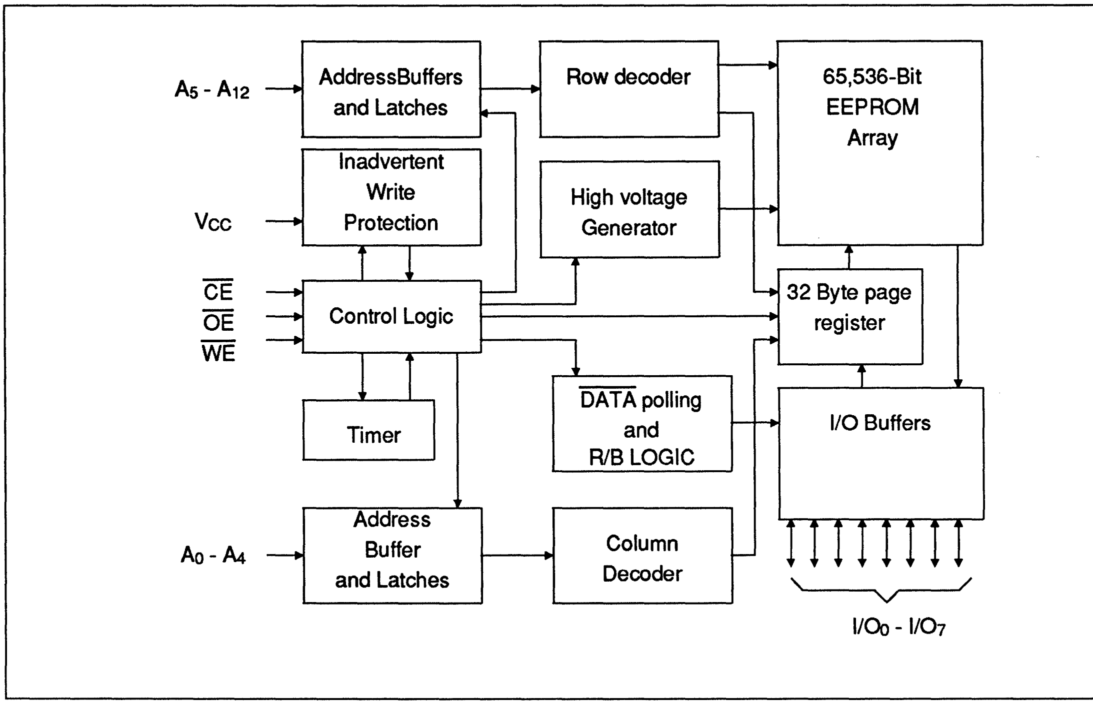
PIN CONFIGURATION 28-Pin DIP, and S.O.



PIN CONFIGURATION 32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{12}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . -10°C to +85°C
Storage temperature . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . -0.5 to +7V
Voltage on any output pin relative to V_{SS} . . . . -0.5 to V_{CC} +0.5V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz, all I/O's = open			40	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=6.7MHz, all I/O's = open			30	mA
I_{SB}	V_{CC} current (stand-by, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (stand-by, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	μA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}			10	μA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}			10	μA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400μA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0		4.0	V

Note:
* V_{ILC} = -0.3V to +0.3V
** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 1.0V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write- ($\overline{WE}$ controlled)	L	‾_/‾	H	D_{IN}	ACTIVE
Byte write ($\overline{CE}$ controlled)	‾_/‾	L	H	D_{IN}	ACTIVE
Standby, and Write inhibit	H	X	X	HIGH Z	STANDBY
Read and Write inhibit	L	H	H	HIGH Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4 V
Input rise and fall times	10 ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0 V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

$T_A = 0^oC$ to $+70^oC$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	28C64A-15 Min.	28C64A-15 Max.	28C64A-20 Min.	28C64A-20 Max.	28C64A-25 Min.	28C64A-25 Max.	Units
t_{RC}	Read cycle time	150		200		250		ns
t_{CE}	CE access time		150		200		250	ns
t_{AA}	Address access time		150		200		250	ns
t_{OE}	OE access time		70		80		100	ns
t_{LZ}	CE low to active output	10		10		10		ns
t_{OLZ}	OE low to active output	10		10		10		ns
t_{HZ}	CE high to high Z output	10	50	10	55	10	60	ns
t_{OHZ}	OE high to high Z output	10	50	10	55	10	60	ns
t_{OH}	Output hold from address change	20		20		20		ns

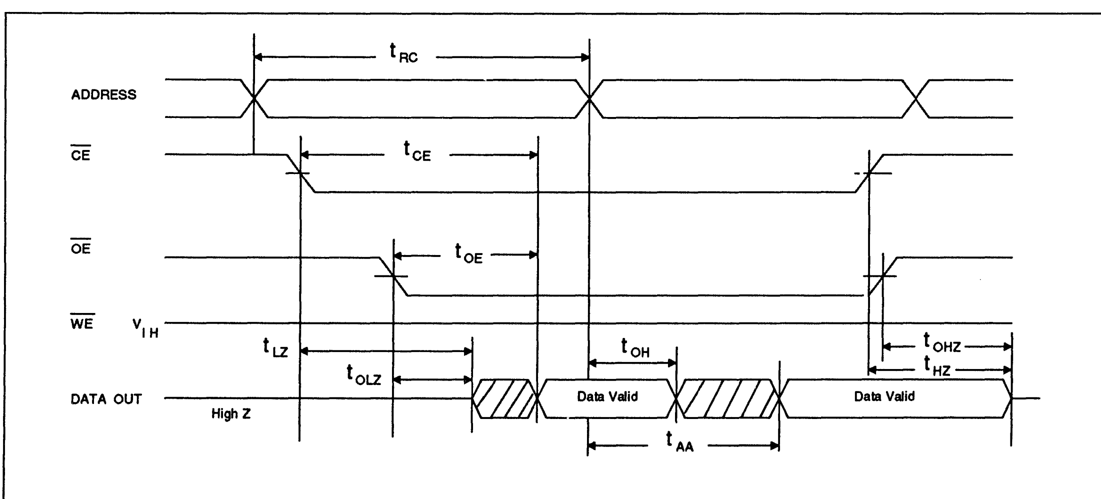
AC CHARACTERISTICS <Write Cycle>

(T_A = 0° to 70°C, V_{CC} = +5V ±10%)

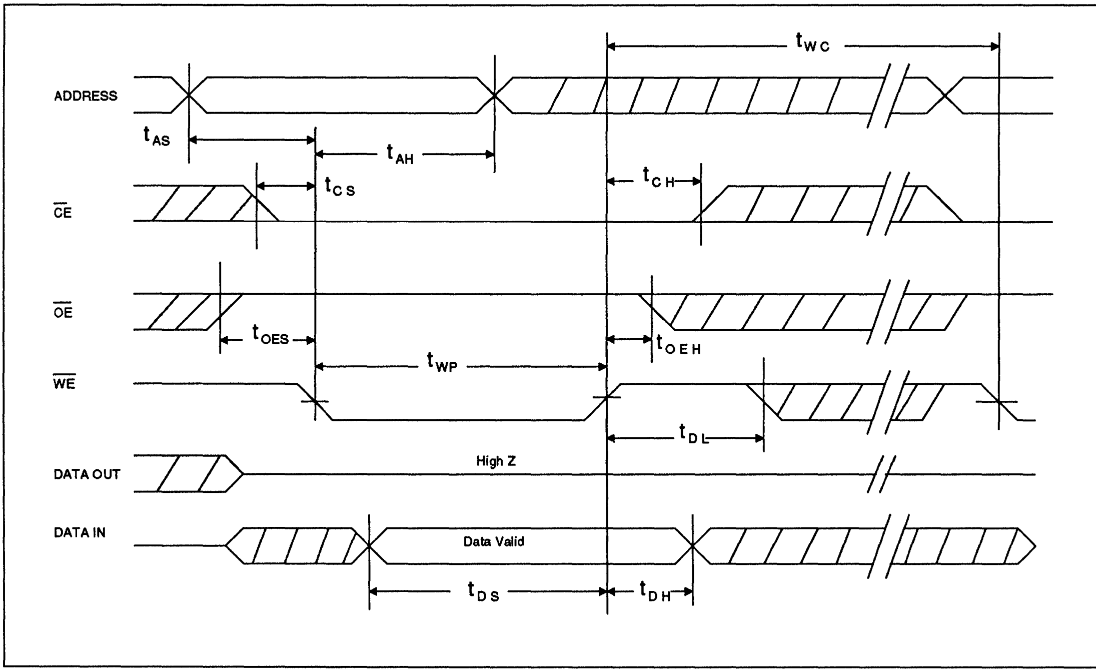
Symbol	Parameter	28C64A-15 Min	28C64A-15 Max	28C64A-20 Min	28C64A-20 Max	28C64A-25 Min	28C64A-25 Max	Units
t_{WC}	Write cycle time		5		10		10	ms
t_{AS}	Address setup time	10		10		10		ns
t_{AH}	Address hold time	70		100		120		ns
t_{CS}	Write setup time	0		0		0		ns
t_{CH}	Write hold time	0		0		0		ns
t_{CW} *	$\overline{CE}$ pulse time	100		120		150		ns
t_{OES}	$\overline{OE}$ setup time	10		10		10		ns
t_{OEH}	$\overline{OE}$ hold time	10		10		10		ns
t_{WP} *	$\overline{WE}$ pulse width	100		120		150		ns
t_{DL}	Data latch time	50		50		50		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	10		10		10		ns
t_{INIT}	Write inhibit period after power-up	5	20	5	20	5	20	ms
t_{DB}	Time to device busy		70		80		100	ns
t_{PL}	Page load time		30		30		30	µs

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

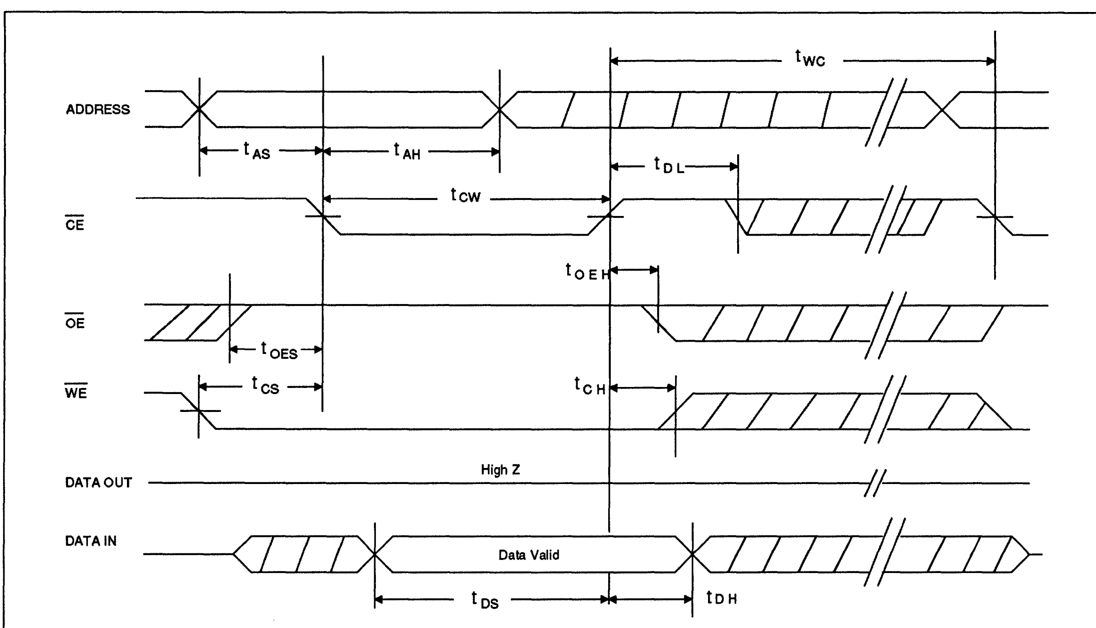
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{12})

The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)

The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)

The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)

Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)

The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

DEVICE OPERATION

READ

Device data is output to the data bus when both $\overline{OE}$ and $\overline{CE}$ are LOW. The data bus is high impedance when either $\overline{CE}$ or $\overline{OE}$ go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. Both $\overline{CE}$ and $\overline{WE}$ controlled write cycles can be executed, i.e., the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last, while data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

PAGE WRITE

The CAT28C64A contains a 32 byte temporary buffer which allows programming of 1 to 32 bytes on a single 5ms nonvolatile write cycle, which can effectively reduce programming time by a factor of 32. The 32 byte page into which the data will be written is specified by the addresses A_5 - A_{12} during the first system write operation following the completion of a previous nonvolatile write cycle. The byte within the specified page is identified by the addresses A_0 - A_4 during the first and subsequent system write cycles. Bytes can be written into the page in any order. Each successive byte load cycle, started by $\overline{WE}$ HIGH to LOW transition, must begin within 30 µs of the rising edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 30 µs, the internal automatic programming cycle will commence. There is no page write window limitation. The page window is infinitely wide so long as the host continues to access the device within the byte load cycle time of 30 µs.

DATA POLLING

Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION

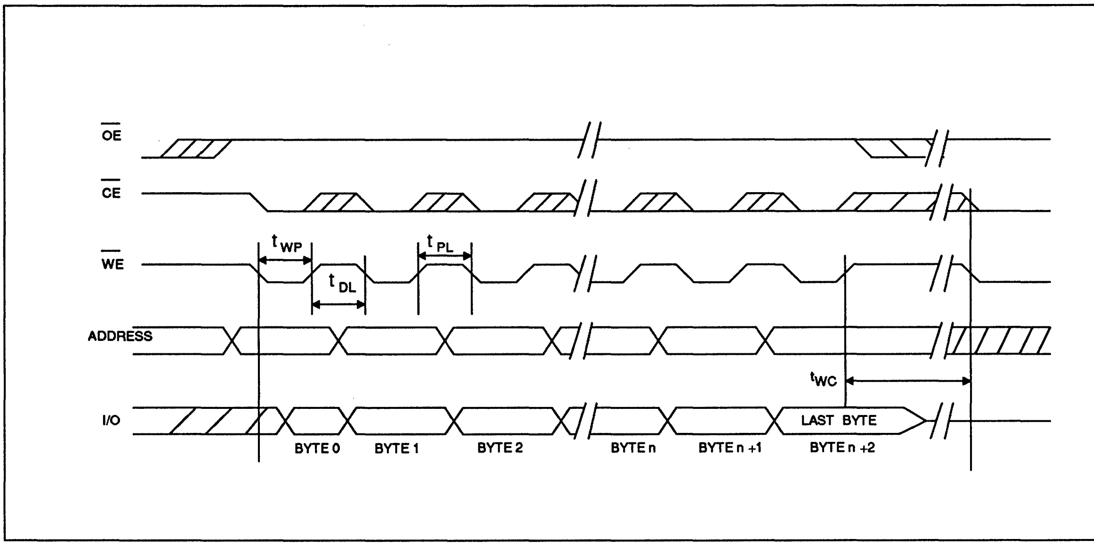
(I) The CAT28C64A has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 3.0V. Read cycles are not affected during this initialization period.

(3) Write cycles are inhibited if $\overline{OE}$ is LOW, or $\overline{CE}$ or $\overline{WE}$ are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

PAGE MODE WRITE CYCLE



CAT28C256
32K x 8 BIT CMOS EEPROM

Preliminary

DESCRIPTION

The CAT28C256 is a fast, low power, 5V-only CMOS EEPROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time. Page write mode reduces programming time.

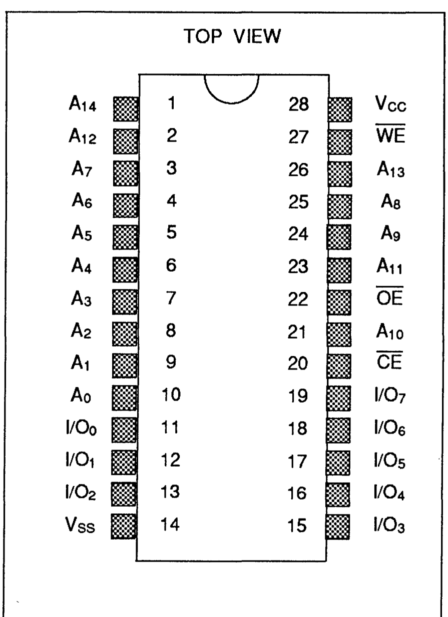
The CAT28C256 is fabricated in reliable floating gate CMOS technology. It is designed for up to10,000 write cycles and 10 years data retention.

FEATURES

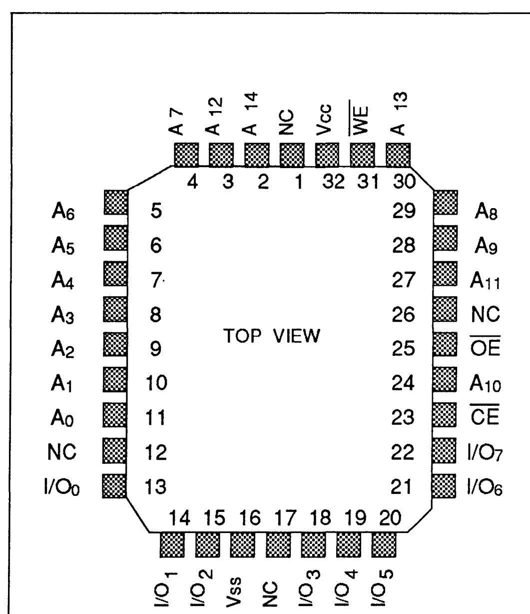
- Fast read access time: 150ns/200ns/250ns
- Low CMOS power:
  - Active 30 mA max., Standby 100µA max.
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
- Power up/down and software write protection
- Fast nonvolatile write cycle: 5 ms max.
- Automatic page write: 1 to 32 bytes in 5 ms
- TTL compatible I/O
- JEDEC approved 28 pin DIP,Small Outline, and 32 pin PLCC packages available.
- 10,000 rewrites/byte, 10 year data retention

PIN CONFIGURATION

PIN CONFIGURATION 28-Pin DIP, and S.O.



PIN CONFIGURATION 32-Pin PLCC



EPROMs

3

CAT2764A OTP

8,196 x 8-BIT ONE-TIME PROGRAMMABLE ROM

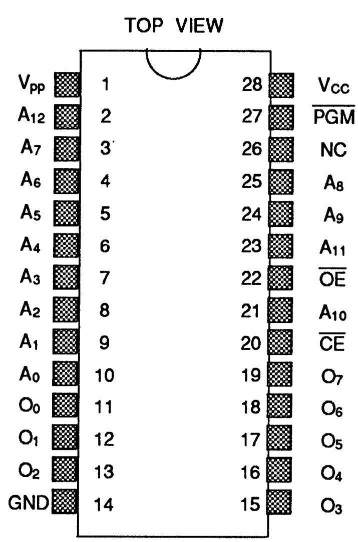
DESCRIPTION

The CAT2764A is a 8,192 X 8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT2764A allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT2764A is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC approved package.

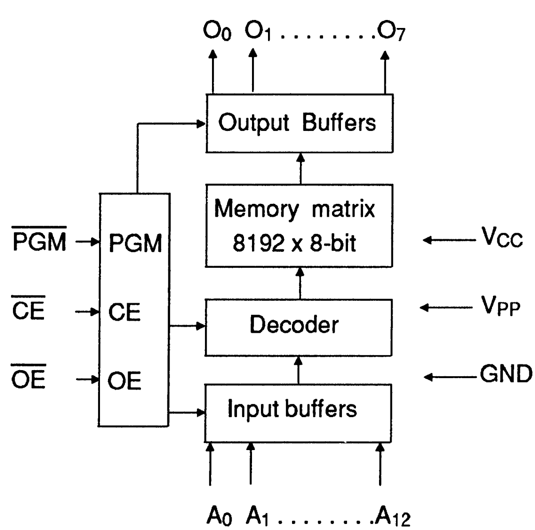
FEATURES

- 5V single power supply
- 8,192 words x 8-bit configuration
- Access time:
  - 150 ns. max. (CAT2764A-15)
  - 200 ns. max. (CAT2764A-20)
  - 250 ns. max. (CAT2764A-25)
- Power consumption:
  - 525 mW max. (read operation)
  - 184 mW (max. during stand-by)
- Fully static operation
- TTL compatible Input/Output
  - (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	+5 V	+5 V	High impedance
Stand-by	V_{IH}	-	-	+5 V	+5 V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{OUT}
Program inhibit	V_{IH}	-	-	+12.5 V	+6 V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	T_A	0 °C ~ 70 °C
Storage temperature	Tstg	- 55 °C ~ 125 °C
All input/output voltages	V_{IN}, V_{OUT}	- 0.6 ~ 13.5 V
V_{CC} supply voltage	V_{CC}	- 0.6V ~ 7 V
Program Voltage	V_{PP}	- 0.6 ~ 14 V
Power assembly voltage	P_D	1.5 W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

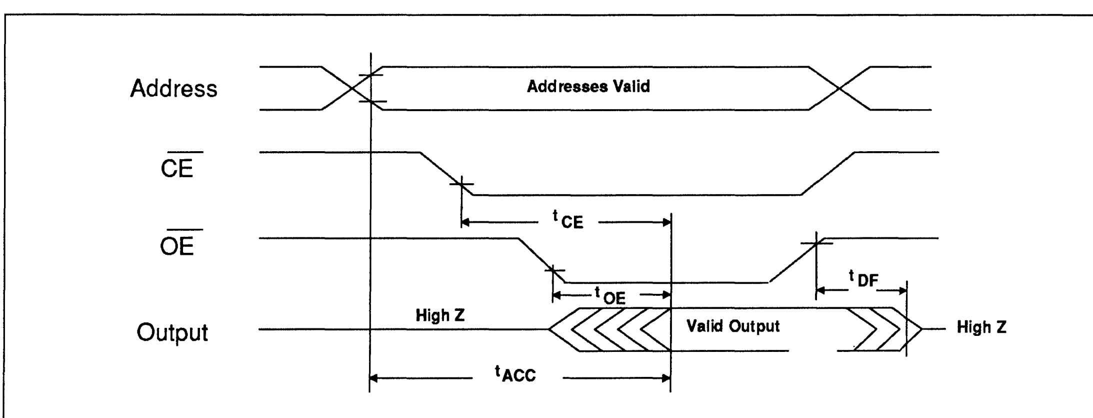
(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, voltages with respect to ground, T_A = 0°C ~ 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Units
I_{LI}	Input leakage current	V_{IN} = V_{IH} or V_{IL}	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (stand-by)	$\overline{CE}$ = V_{IH}, outputs unloaded	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}, outputs unloaded	-	-	100	mA
I_{PP1}	Program power current	V_{PP} = V_{CC}	-	-	5	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, $\overline{PGM}$ = V_{IH}, T_A = 0°C ~ 70°C)

Symbol	Parameter	Conditions	2764A-15 Min.	Max.	2764A-20 Min.	Max.	2764A-25 Min.	Max.	Unit
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	60	-	70	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	50	0	60	0	70	ns



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

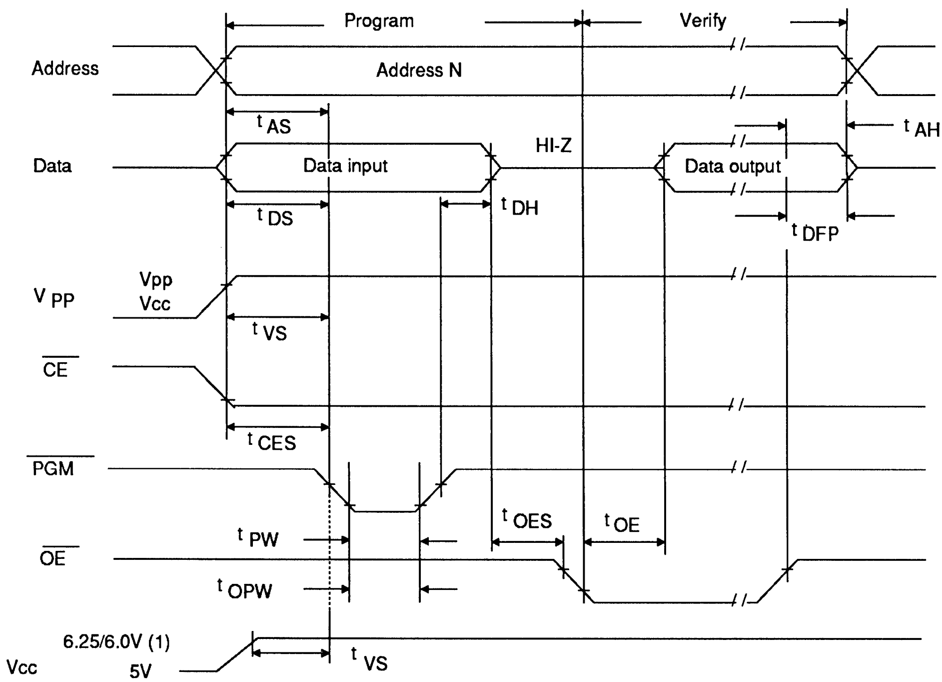
Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{IH}$ or V_{IL}	-	-	10	μA
I_{PP}	V_{PP} power current	$\overline{CE} = \overline{PGM} = V_{IL}$	-	-	50	mA
I_{CC}	V_{CC} power current	-	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400μA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-1.05	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{AS}	Address set-up time	-	2	-	-	μs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	μs
t_{DS}	Data set-up time	-	2	-	-	μs
t_{AH}	Address hold time	-	0	-	-	μs
t_{DH}	Data hold time	-	2	-	-	μs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} and V_{CC} power set-up times	-	2	-	-	μs
t_{PW}	$\overline{PGM}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High-speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	μs
t_{OPW}	$\overline{PGM}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{CES}	$\overline{CE}$ set-up time	-	2	-	-	μs
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

TIMING <Programming Operation>



(1) Note: VCC = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.0V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, the device must be selected ($\overline{CE}$ = V_{IL}), outputs are disabled ($\overline{OE}$ = V_{IH}), and a program write pulse must be applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may be verified by enabling the outputs ($\overline{OE}$ =V_{IL}) and comparing the written data to the read data. This device is compatible with the Intelligent Programming ™ algorithm, and the Quick Pulse Programming ™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: exceeding 14V on V_{PP} will permanently damage the device.

CAT27128A OTP

16,384 x 8-BIT ONE-TIME PROGRAMMABLE ROM

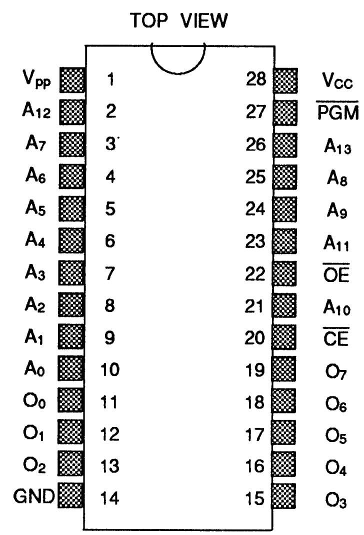
DESCRIPTION

The CAT27128A is a 16,384 X 8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT27128A allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT27128A is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC approved package.

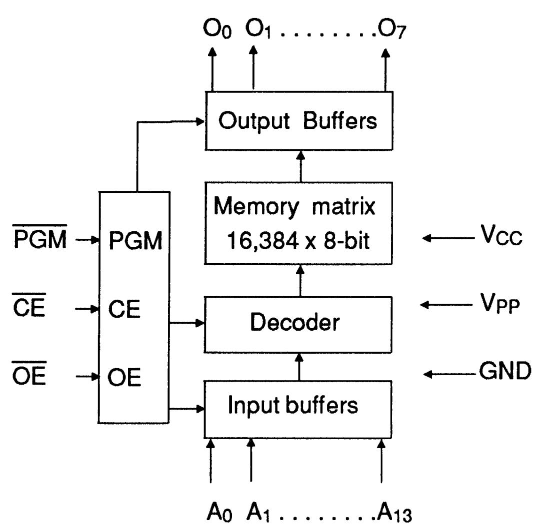
FEATURES

- 5V single power supply
- 16,384 words x 8-bit configuration
- Access time:
  - 150 ns. max. (CAT27128A-15)
  - 200 ns. max. (CAT27128A-20)
  - 250 ns. max. (CAT27128A-25)
- Power consumption:
  - 525 mW max. (read operation)
  - 184 mW (max. during stand-by)
- Fully static operation
- TTL compatible Input/Output
  - (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	+5 V	+5 V	High impedance
Stand-by	V_{IH}	-	-	+5 V	+5 V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{OUT}
Program inhibit	V_{IH}	-	-	+12.5 V	+6 V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	T_A	0 °C ~ 70 °C
Storage temperature	Tstg	- 55 °C ~ 125 °C
All input/output voltages	V_{IN}, V_{OUT}	- 0.6 ~ 13.5 V
V_{CC} supply voltage	V_{CC}	- 0.6V ~ 7 V
Program Voltage	V_{PP}	- 0.6 ~ 14 V
Power assembly voltage	P_D	1.5 W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC} voltages with respect to ground, T_A = 0°C ~ 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
I_{LI}	Input leakage current	V_{IN} = V_{IH} or V_{IL}	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (stand-by)	$\overline{CE}$ = V_{IH}, outputs unloaded	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL} , outputs unloaded	-	-	100	mA
I_{PP1}	Program power current	V_{PP} = V_{CC}	-	-	5	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

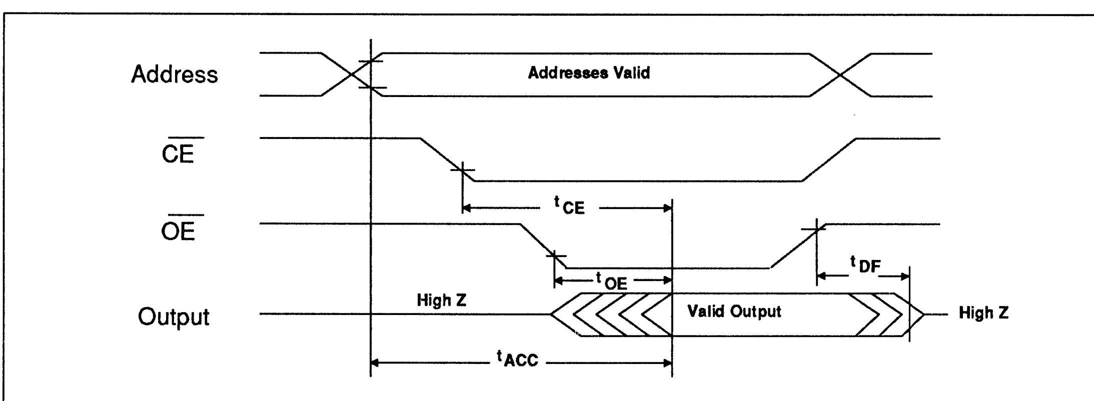
3

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, $\overline{PGM}$ = V_{IH}, T_A = 0°C ~ 70°C)

Symbol	Parameter	Conditions	27128A-15 Min.	27128A-15 Max.	27128A-20 Min.	27128A-20 Max.	27128A-25 Min.	27128A-25 Max.	Unit
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	60	-	75	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	50	0	60	0	70	ns

TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

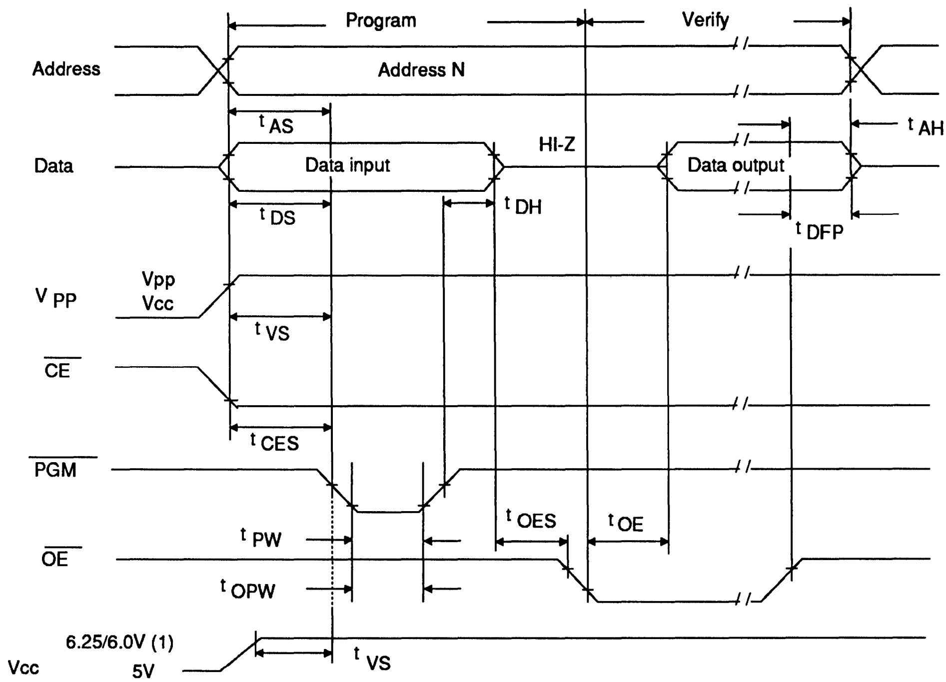
Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{IH}$ or V_{IL}	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE} = \overline{PGM} = V_{IL}$ All outputs unloaded	-	-	50	mA
I_{CC}	V_{CC} power current	All outputs unloaded	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} and V_{CC} power set-up times	-	2	-	-	µs
t_{PW}	$\overline{PGM}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High-speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{PGM}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{CES}	$\overline{CE}$ set-up time	-	2	-	-	µs
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

TIMING <Programming Operation>



(1) Note: VCC = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.0V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, the device must be selected ($\overline{CE} = V_{IL}$), outputs are disabled ($\overline{OE} = V_{IH}$), and a program write pulse must be applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may be verified by enabling the outputs ($\overline{OE} = V_{IL}$) and comparing the written data to the read data. This device is compatible with the Intelligent Programming ™ algorithm, and the Quick Pulse Programming ™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

CAT27256 OTP

32,768 x 8-BIT ONE-TIME PROGRAMMABLE ROM

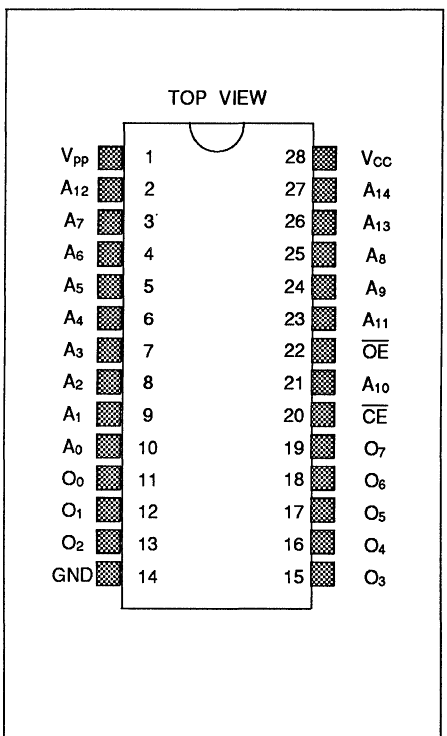
DESCRIPTION

The CAT27256 is a 32,768 X 8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT27256 allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT27256 is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC-approved package.

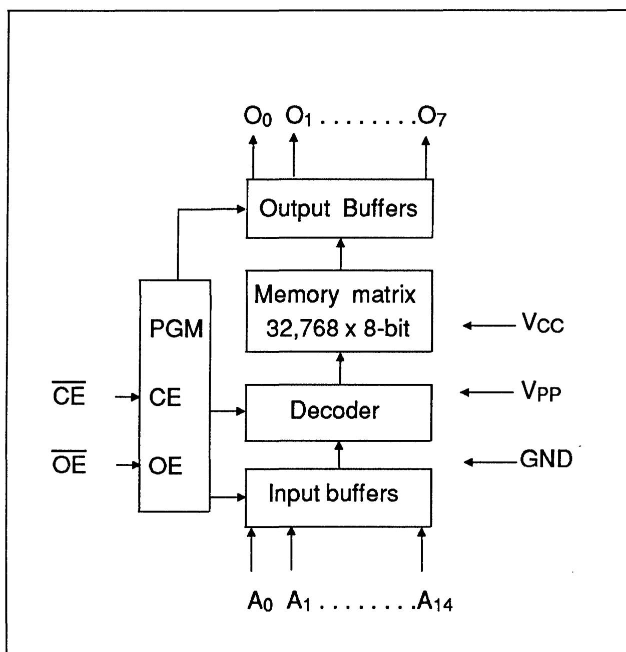
FEATURES

- 5V single power supply
- 32,768 words x 8-bit configuration
- Access time:
  - 170 ns. max. (CAT27256-17)
  - 200 ns. max. (CAT27256-20)
  - 250 ns. max. (CAT27256-25)
- Power consumption:
  - 525 mW max. (read operation)
  - 184 mW (max. during stand-by)
- Fully static operation
- TTL compatible Input/Output (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5 V	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5 V	+5 V	High impedance
Stand-by	V_{IH}	-	+5 V	+5 V	High impedance
Program	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{IN}
Program verify	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	+12.5 V	+6 V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	T_A	0 °C ~ 70 °C
Storage temperature	Tstg	- 55 °C ~ 125 °C
All input/output voltages	V_{IN}, V_{OUT}	- 0.6 ~ 13.5 V
V_{CC} supply voltage	V_{CC}	- 0.6V ~ 7 V
Program Voltage	V_{PP}	- 0.6 ~ 14 V
Power assembly voltage	P_D	1.5 W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, T_A = 0°C ~ 70°C)

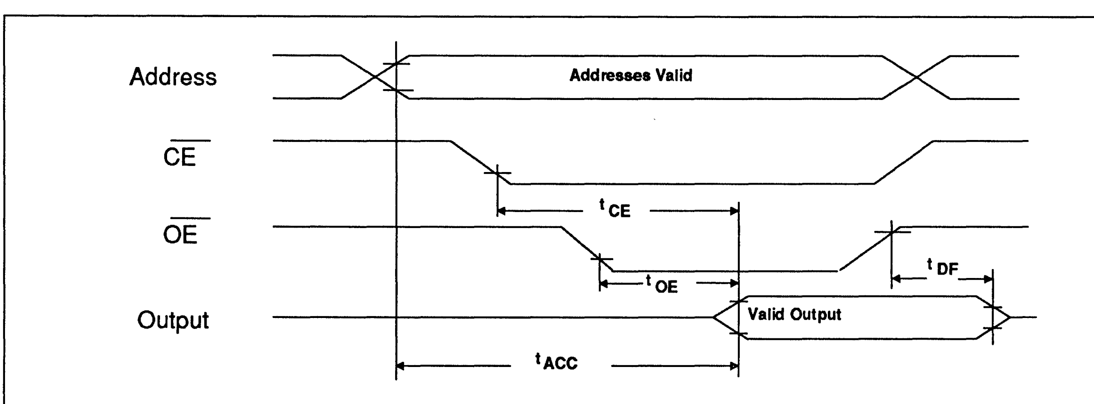
Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (stand-by)	$\overline{CE}$ = V_{IH}	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}	-	-	100	mA
I_{PP1}	Program power current	V_{PP} = V_{CC}	-	-	5	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{CC} = V_{PP}, T_A = 0°C ~ 70°C)

Symbol	Parameter	Conditions	27256-17 Min.	27256-17 Max.	27256-20 Min.	27256-20 Max.	27256-25 Min.	27256-25 Max.	Unit
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	170	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}$ = V_{IL}	-	170	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	60	-	75	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	50	0	55	0	60	ns

TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

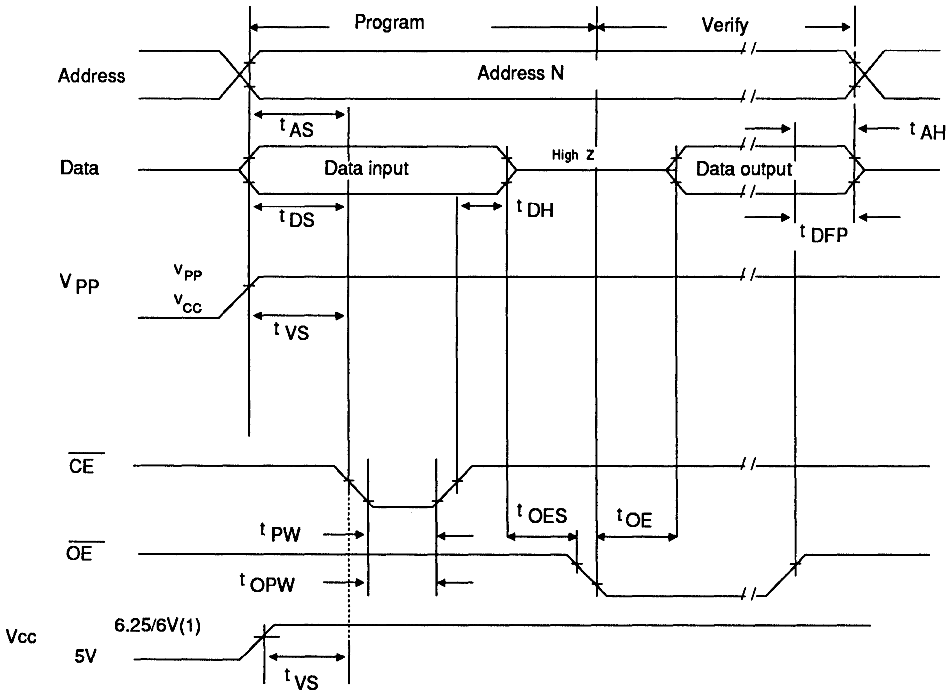
Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE}$ = V_{IL}	-	-	50	mA
I_{CC}	V_{CC} power current	-	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} power set-up time	-	2	-	-	µs
t_{PW}	$\overline{CE}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High-speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{CE}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

TIMING <Programming Operation>



(1) Note: VCC = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.0V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, outputs are disabled ($\overline{OE} = V_{IH}$), and a program write pulse must be applied to the $\overline{CE}$ pin. After the program write pulse the programmed data may be verified by enabling the outputs ($\overline{OE} = V_{IL}$) and comparing the written data to the read data. This device is compatible with the Intelligent Programming™ algorithm, and the Quick Pulse Programming™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

CAT27512 OTP

65,536 x 8-BIT ONE-TIME PROGRAMMABLE ROM

DESCRIPTION

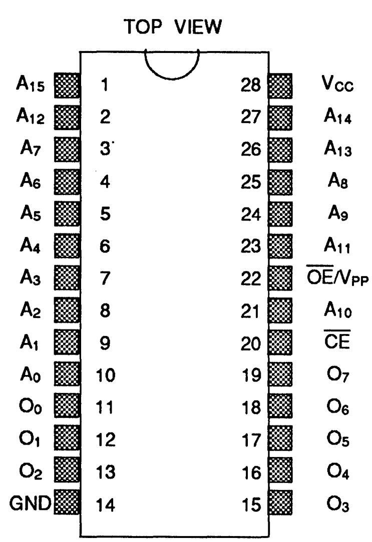
The CAT27512 is a 65,536 x 8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT27512 allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT27512 is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC-approved package.

FEATURES

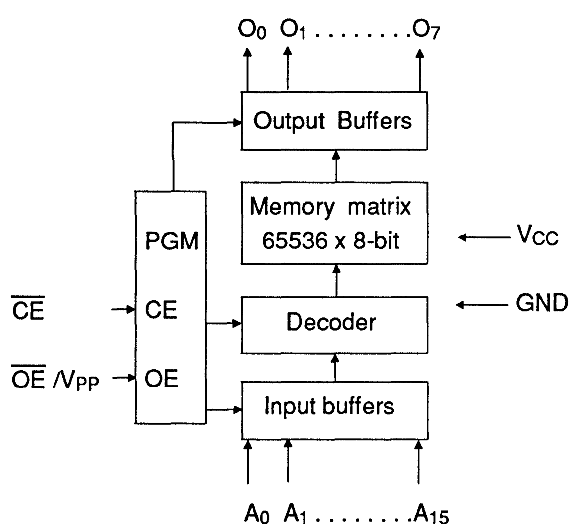
- 5V single power supply
- 65,536 words x 8-bit configuration
- Access time:
  200 ns. max. (CAT27512-20)
  250 ns. max. (CAT27512-25)
- Power consumption:
  525 mW max. (read operation)
  184 mW (max. during stand-by)
- Fully static operation
- TTL compatible Input/Output
  (3-state output)

3

PIN CONFIGURATION



BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5 V	High impedance
Stand-by	V_{IH}	-	+5 V	High impedance
Program	V_{IL}	12.5V	+6 V	D_{IN}
Program inhibit	V_{IH}	12.5V	+6 V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	T_A	0 °C ~ 70 °C
Storage temperature	Tstg	- 55 °C ~ 125 °C
All input/output voltages	V_{IN}, V_{OUT}	- 0.6 ~ 13.5 V
V_{CC} supply voltage	V_{CC}	- 0.6V ~ 7 V
Program Voltage	V_{PP}	- 0.6 ~ 14 V
Power assembly voltage	P_D	1.5 W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, T_A = 0°C ~ 70°C)

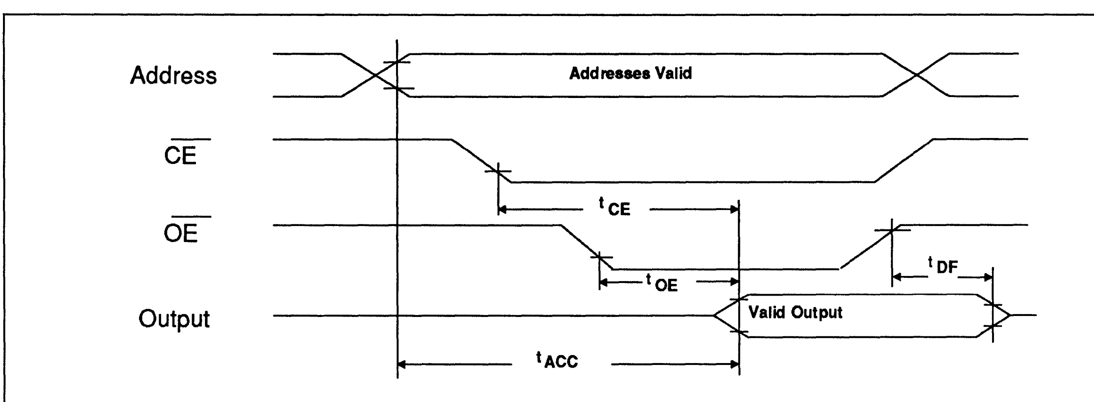
Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	μA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	μA
I_{CC1}	V_{CC} power current (stand-by)	$\overline{CE}$ = V_{IH}	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400μA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, T_A = 0°C ~ 70°C)

Symbol	Parameter	Conditions	27512-20 Min.	27512-20 Max.	27512-25 Min.	27512-25 Max.	Unit
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}/V_{PP}$ = V_{IL}	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	70	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	55	0	60	ns

TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

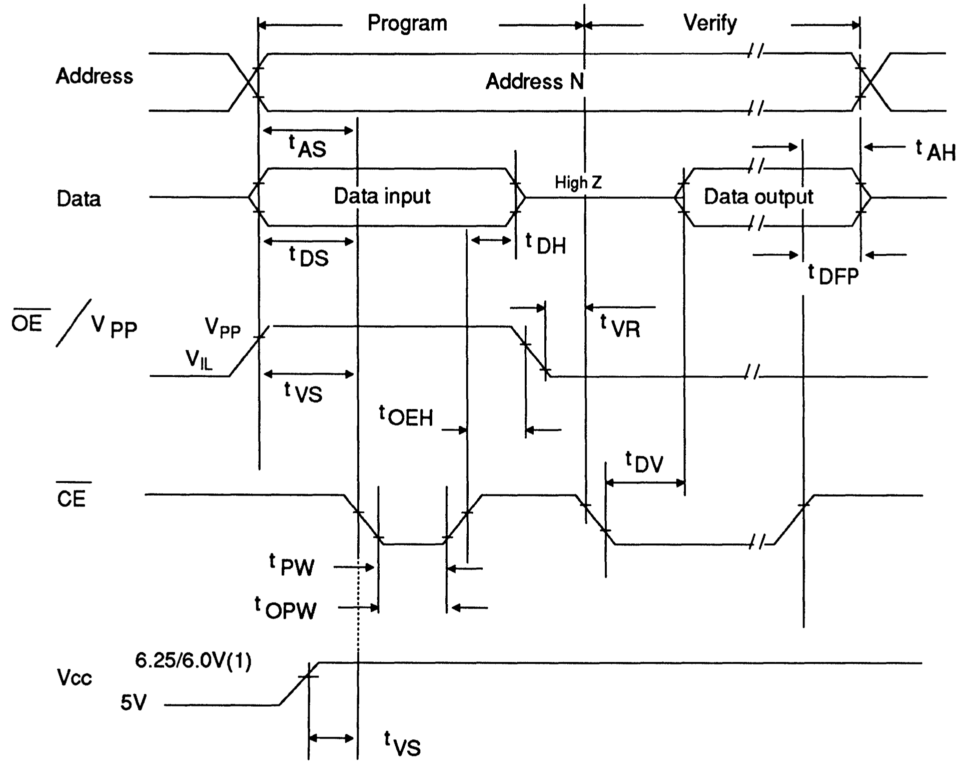
Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE} = V_{IL}$	-	-	50	mA
I_{CC}	V_{CC} power current	-	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ±0.5V, T_A = 25°C ±5°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OEH}	$\overline{OE}/V_{PP}$ hold time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	$\overline{CE}$ enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} power set-up time	-	2	-	-	µs
t_{PW}	$\overline{CE}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{CE}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{DV}	Data valid from $\overline{CE}$	-	-	-	1	µs
t_{VR}	$\overline{OE}/V_{PP}$ recovery time	-	2	-	-	µs

TIMING <Programming Operation>



(1) Note: VCC = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.0V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and $\overline{OE}/V_{PP}$ must be adjusted to their programming levels, and a program write pulse must be applied to the $\overline{CE}$ pin. After the program write pulse the programmed data may be verified by enabling the outputs ($\overline{OE}$ / V_{PP} = V_{IL} and $\overline{CE}$ = V_{IL}) and comparing the written data to the read data. This device is compatible with the Intelligent Programming ™ algorithm, and the Quick Pulse Programming ™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

3

CAT27C210
1 MEGABIT (64k X 16) CMOS EPROM

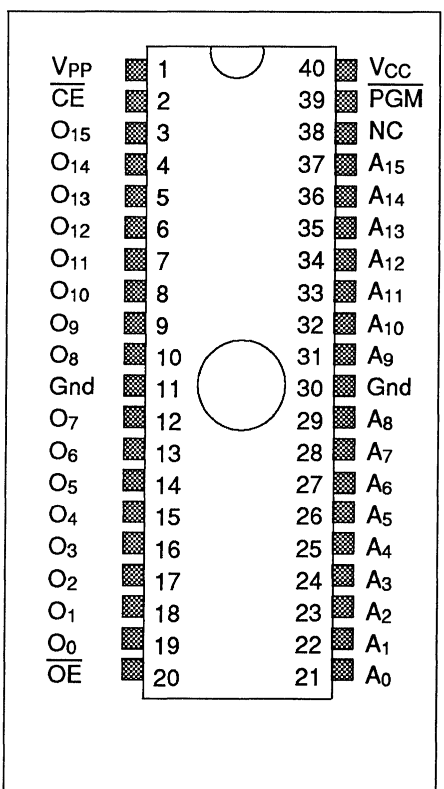
DESCRIPTION

The CAT27C210 is a 1 megabit high-speed EPROM. It features low power operation, 16 three state output buffers, and a pumping circuit to raise the EPROM cell's gate voltage to a level higher than V_{PP} during programming operation. Two control lines eliminate bus contention in microprocessor systems. The CAT27C210 is packaged in a 40 pin DIP (plastic OTP or CERDIP), or a 44 pin PLCC (OTP). The CERDIP is equipped with a transparent lid to enable device erasing.

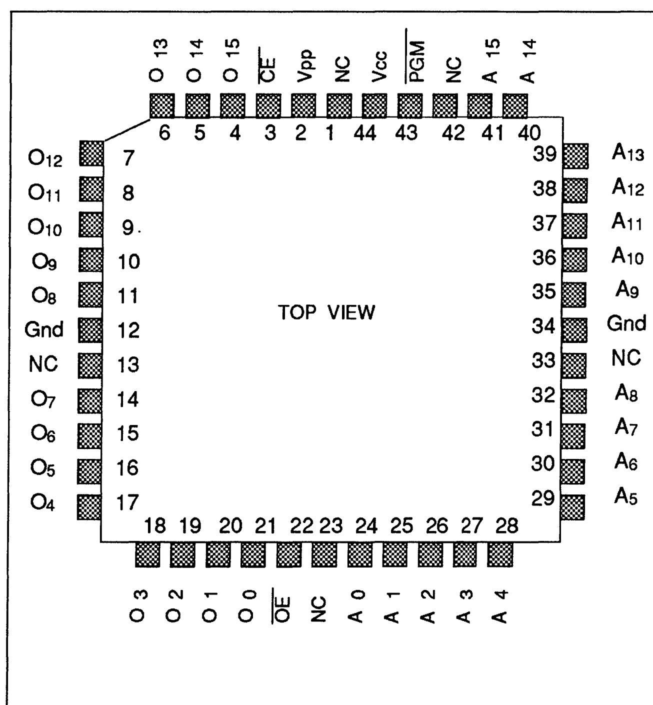
FEATURES

- Fast read access time: 150ns max.
- Low CMOS power:
  Active - 30 mA max. (CMOS input level)
  Standby - 100μA max.
- 16 three state output buffers
- ESD protection greater than 2000V
- 64K words by 16 bits
- TTL compatible I/O
- One-time-programmable option
- Pin/functional equivalent to Intel 27210
- 40 pin plastic DIP (OTP), 40 pin CERDIP, or 44 pin plastic leaded chip carrier (OTP) available.
- Compatible with Quick Pulse TM programming

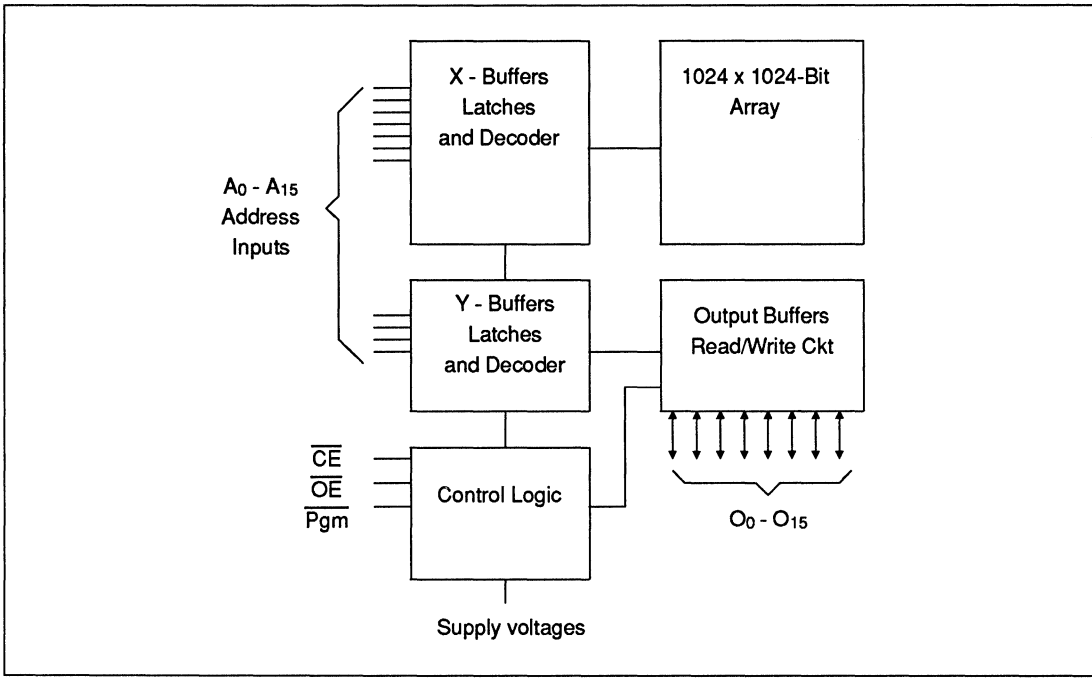
PIN CONFIGURATION 40 Pin DIP



PIN CONFIGURATION 44 Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	Address inputs
O_0 - O_{15}	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Write enable
V_{CC}	Read voltage supply
V_{SS}	Ground
V_{PP}	Program voltage supply

CAPACITANCE

(T_A= 25 °C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
C_{OUT}	Output capacitance	V_{OUT} = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF
C_{VPP}	V_{PP} supply capacitance	V_{PP} = 0V	25	pF

Note: These parameters are periodically sampled and are not 100% tested.

FUNCTION TABLE / Mode selection

Operating Conditions: V_{CC} = +5V, V_{CC} = V_{PP} (during read)

Mode \ Pins	V_{PP}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	I/O
Read	V_{CC}	V_{IL}	VIL	x	x	x	DOUT
Output disable	V_{CC}	V_{IL}	V_{IH}	x	x	x	HI Z
Stand-by	V_{CC}	V_{IH}	x	x	x	x	HI Z
Program	V_{PP}	V_{IL}	V_{IH}	V_{IL}	x	x	D_{IN}
Program verify	V_{PP}	V_{IL}	V_{IL}	V_{IH}	x	x	D_{OUT}
Program inhibit	V_{PP}	V_{IH}	x	x	x	x	HI Z
Signature MFG	V_{CC}	V_{IL}	V_{IL}	x	V_{IL}	V_{ID}	0031H
Signature device	V_{CC}	V_{IL}	V_{IL}	x	V_{IH}	V_{ID}	0007H

Notes on Modes table:

Logic levels	V_{IH} = TTL logic 1 level. V_{IL} = TTL logic 0 level
Supply Voltage	V_{PP} = programming (high V) V_{ID} = signature voltage (high V) x = supply voltage between ground and V_{CC}
Read	Read mode, the content of the addressed memory word is placed on the I/O pins O_0 to O_{15}
Output disable	Device is selected (active mode), programming is disabled and O_0 to O_{15} output buffers are tri-stated (PMOS and NMOS drivers are turned off.)
Standby	Device is deselected, low power dissipation.
Program	Word programming mode, logic zeros in the bit pattern driving the O_0 to to O_{15} input buffers are written into the respective memory cells of the addressed word.
Program verify	Following a programming cycle, to verify the cell contents of the memory word being programmed (not recommended as normal read operation)
Program inhibit	$\overline{CE}$ set to logic 1 level prevents programming and deselects the device.
Signature MFG.	Signature mode, code of IC manufacturer output on I/O pins O_0 to O_{15}
Signature Device.	Signature mode, code of IC type output on I/O pins O_0 to O_{15}

3

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias	-10°C t0 +85°C
Storage temperature	-65°C to +125°C
Voltage on all input/output pins relative to Gnd	-1.0 to +7V
Voltage on A9 relative to Gnd	-1.0 to 14.0V
D.C. output current, short-curcuit	20mA
Program supply voltage VPP	-1.0 to 14.0V
Read supply voltage VCC	-1.0 to +7V
Max power dissapation (T_A = 25°C)	1.0W
Max lead soldering temp (10 seconds)	260°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION AND STANDBY MODES

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic 0 state (TTL level V_{IL}), $\overline{CE}$ powers up all input and sensitive internal circuitry. In the logic 1 state (TTL level V_{IH}), $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off and the power dissipation is reduced to a minimum. A logic 1 on the output enable $\overline{OE}$ (output enable) disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{15} have been stable for a time equal to t_{ACC} - t_{OE}, the output data is available after a delay of t_{OE} from the falling edge of $\overline{OE}$.

SIGNATURE MODE

The signature mode allows the programmer to identify the manufacturer and the type of the part. This mode is entered as a regular READ mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, in addition to driving the input address bit A_9 to high voltage V_{IH} level.

A logic low level (V_{IL}) on the address pin A_0 outputs on O_0 to O_{15} the binary code of the IC manufacturer.

CATALYST Code: 0000 0000 0011 0001 (0031H)

A logic high level (V_{IH}) on the address pin A_0 outputs the device type on O_0 to O_{15}

Device type: 0000 0000 0000 01110 (007H)

AC CHARACTERISTICS <Read Operation>

$T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ	Max	Units
t_{ACC}	Address access time			150	ns
t_{CE}	$\overline{CE}$ to output delay			150	ns
t_{OE}	$\overline{OE}$ to output delay			60	ns
t_{DF}	$\overline{OE}$ high to output High Z	0.0		50	ns

Notes:

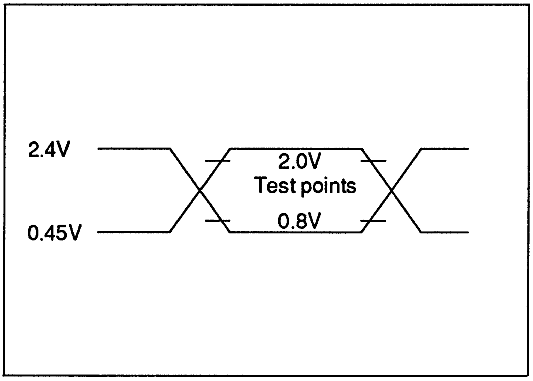
Output floating (OUT High Z) is defined as the state where the external data line is no longer driven by the output buffer.

Input rise and fall times (10 to 90%) 20ns

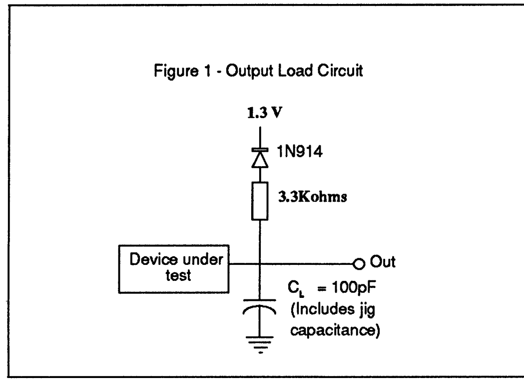
Input pulse levels . . . . 0.45 to 2.4V

Input and output timing reference . . . . 0.80 to 2.0V

AC TESTING IN/OUT WAVEFORM



AC TEST LOAD CIRCUIT



DC CHARACTERISTICS <Read and Standby Modes>

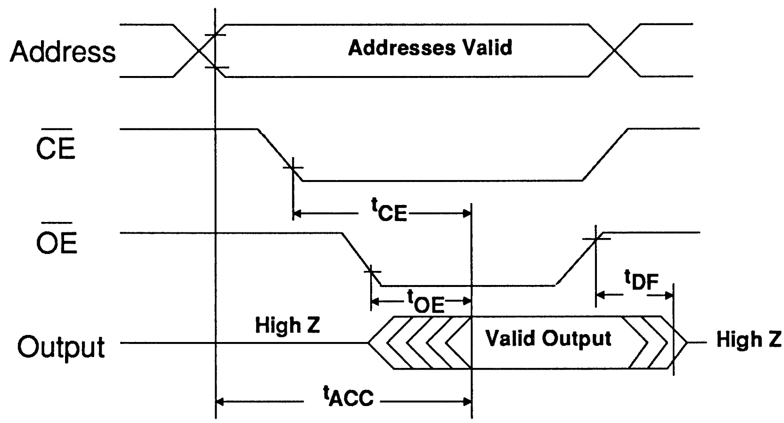
(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	V_{CC} current (operating, TTL)	f = DC to 5MHz			40	mA
I_{CCC}	V_{CC} current (operating, CMOS)	f = DC to 5MHz			30	mA
I_{SB}	V_{CC} current (stand-by, TTL)	$\overline{CE}$ = V_{IH}			1	mA
I_{SBC}	V_{CC} current (stand-by, CMOS)	$\overline{CE}$ = V_{IH}			100	µA
I_{LI}	Input load current	V_{IN} = 5.5V			1.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V			1.0	µA
V_{IH}	High level input voltage TTL		2.0		V_{CC} +0.5	V
V_{IHC}	High level input voltage CMOS		V_{CC} -0..5		V_{CC} +0.5	V
V_{IL}	Low level input voltage TTL		-0.5		0.8	V
V_{ILC}	Low level input voltage CMOS		-0.5		0.3	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
I_{PP}	V_{PP} load current (READ)	V_{PP} = 5.5V			1.0	µA

The maximum current values are with outputs O_0 to O_{15} unloaded.
V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC TIMING <Read Operation>

AC Waveforms (Read Mode)



Programming Mode

As shipped, all the bits of the CAT27C210 are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, $\overline{CE}$ is pulled to V_{IL}, and a program write pulse is applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may then be verified by enabling the outputs ($\overline{OE}$=V_{IL}, $\overline{CE}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}), then comparing the written data to the read data. This device is compatible with the Intelligent Programming TM and the Quick Pulse Programming TM algorithm. algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp.[9/87]

CAUTION: Exceeding 14V on the VPP pin will permanently damage the device.

DC CHARACTERISTICS <Programming Mode>

(V_{CC} = +5V ±10%, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
VCC	Low voltage supply Quick Pulse program		6.0		6.5	V
V_{CC}	Low voltage supply Intelligent program		5.75		6.25	V
V_{PP}	High voltage supply Quick Pulse program		12.5		13.0	V
V_{PP}	High voltage supply Intelligent program		12.0		13.0	V
I_{CCP}	V_{CC} current, program + verify	see note			45	mA
I_{PP}	V_{PP} current, program operation				40	mA
I_{LI}	Input load current	V_{IN} = 5.5V			1.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V			1.0	µA
V_{IL}	Input low level TTL		-0.5		0.8	V
V_{ILC}	Input low level CMOS		-0.5		0.3	V
V_{OL}	Output low level	I_{OL} = 2.4			0.45	V
V_{IH}	Input high level TTL		2.0		V_{CC}+0.5	V
V_{IHC}	Input high level CMOS		V_{CC}-0.5		V_{CC}+0.5	V
V_{OH}	Output high level	I_{OH} = -400µA	2.4			V
V_{ID}	A_9 signature level		11.5		12.5	V

Notes:

The maximum current values are with outputs O_0 to O_{15} unloaded.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming>

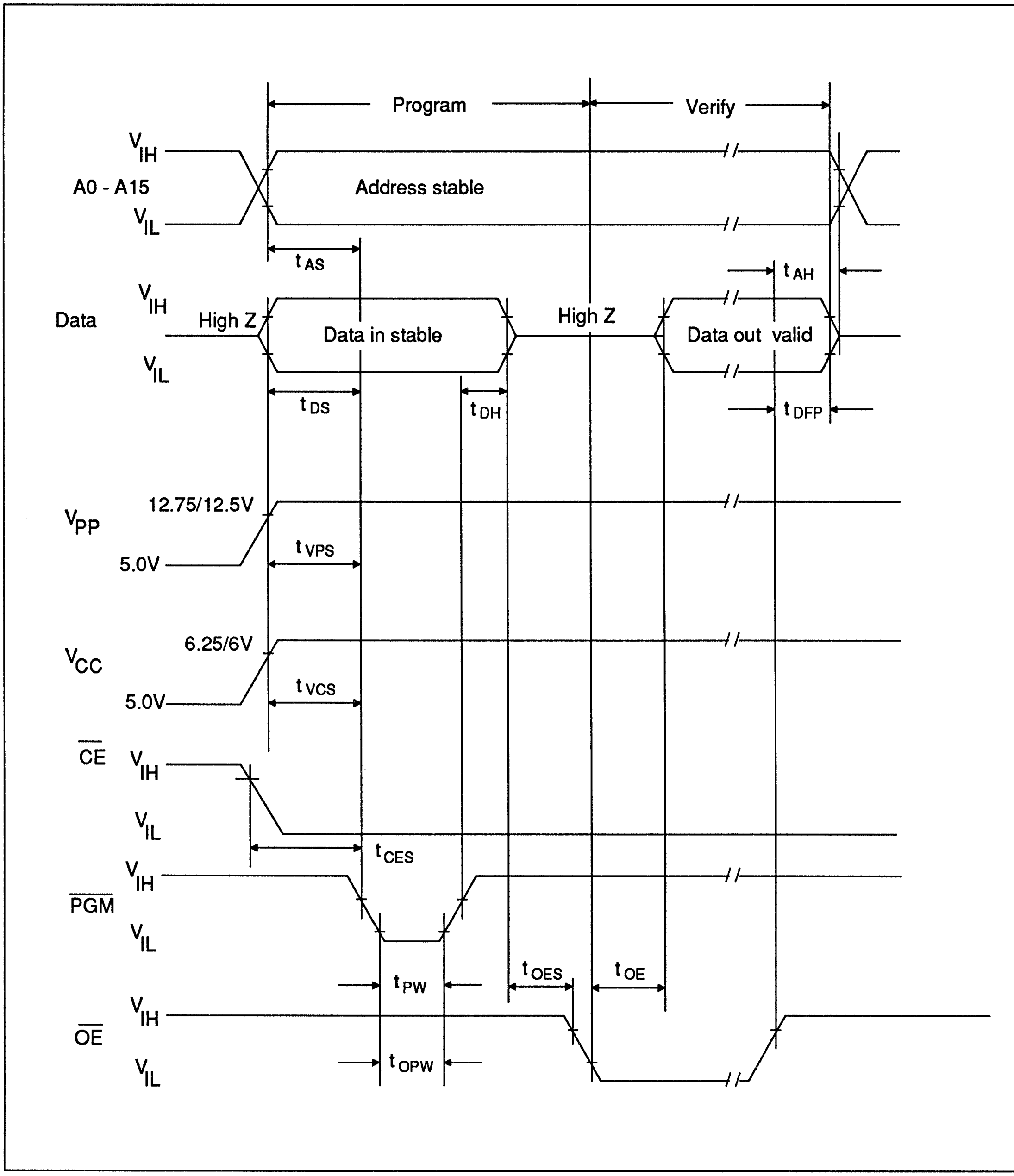
$T_A = 25^oC \pm 5^oC$

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
t_{AS}	Address set-up time		2			µs
t_{OES}	OE set-up time	Input rise and fall times: 10%-90% = 20ns Input pulse levels: 0.45 to 2.4V Input timing reference level: 0.8 to 2.0V Output timing reference	2			µs
t_{DS}	Data set-up time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{CES}	CE set-up time		2			µs
t_{VPS}	V_{PP} set-up time		2			µs
t_{VCS}	V_{CC} set-up time		2			µs
t_{PW}	$\overline{PGM}$ pulse width, Intelligent Pgm.		0.95	1.0	1.05	ms
t_{PW}	$\overline{PGM}$ pulse width, Quick Pulse Pgm.		95	100	105	µs
t_{OPW}	$\overline{PGM}$-overprogram pulse-Intelligent Pgm		2.85	-	78.5	ms
t_{OE}	Data valid from $\overline{OE}$		-		130	ns
t_{DFP}	$\overline{OE}$ high to output High Z		-		150	ns

Note:

Output floating (OUTPUT HIGH Z) is defined as the state where the external data line is no longer driven by the output buffer.

AC TIMING <Programming Operation>



Note: When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.

CAT27HC256

32,768 x 8-BIT HIGH-SPEED CMOS EPROM

Preliminary

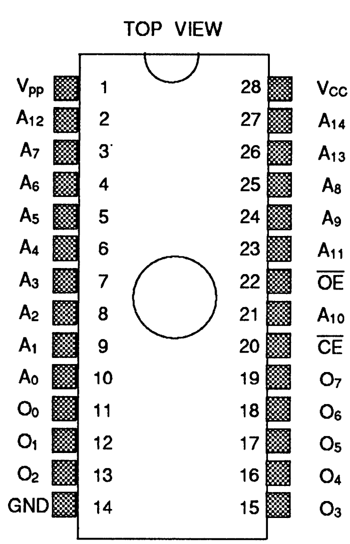
DESCRIPTION

The CAT27HC256 is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. The CAT27HC256 is packaged in a 28-pin ceramic dual-in-line package with a transparent lid. The lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, allowing new pattern to be written into the device by following the programming procedure.

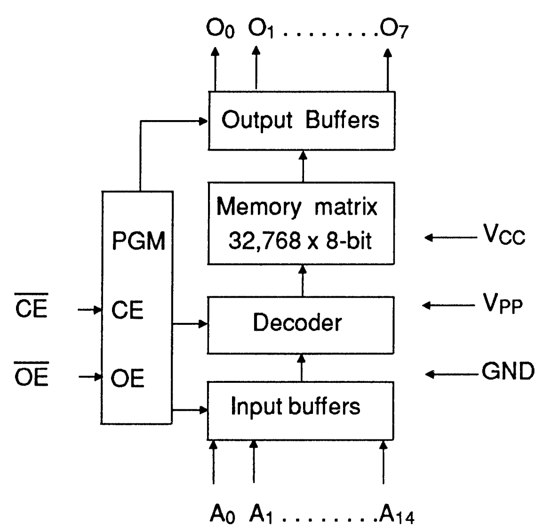
FEATURES

- 5V single power supply
- 32,768 words x 8-bit configuration
- Fast access time: 55 ns.
- Low current requirements:
  - Active: 40 mA max (TTL levels)
  - Standby: 1 mA max (TTL levels)
  - Standlby: 100μA (CMOS levels)
- High speed programming
- TTL compatible Input/Output
- 12.5V programming
- 28-pin JEDEC approved DIP
- Electronic signature
- Industrial and military temperature range available

PIN CONFIGURATION



BLOCK DIAGRAM



This specification may be changed without notification.

SRAMs

4

CAT71C88

16K X 4-BIT HIGH SPEED CMOS STATIC RAM

GENERAL DESCRIPTION

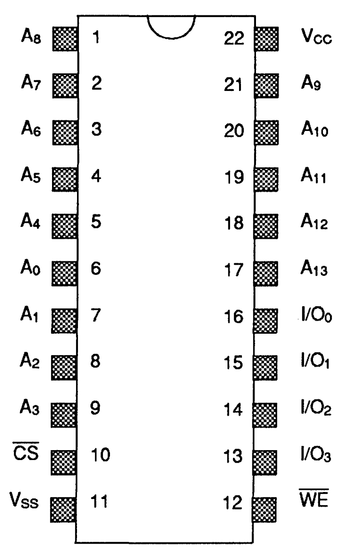
The CAT71C88 is a static CMOS RAM organized as a 16,384 word by 4 bit array. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refresh operations are unnecessary. The CAT71C88 is offered in a 22-pin slim package.

FEATURES

- CMOS technology - completely static operation
- Low power dissipation:
  Standby - 11 mW max.
  Operation 605 mW. max.
- Single power supply (+5V ±10%)
- Operating temperature $T_A = 0^{\circ}$ to $70^{\circ}C$
- Fully TTL compatible, input and output
- 3-state output
- JEDEC standard 22-pin 300-mil wide package
- Access time = 45/55/70 ns max.

PIN CONFIGURATION

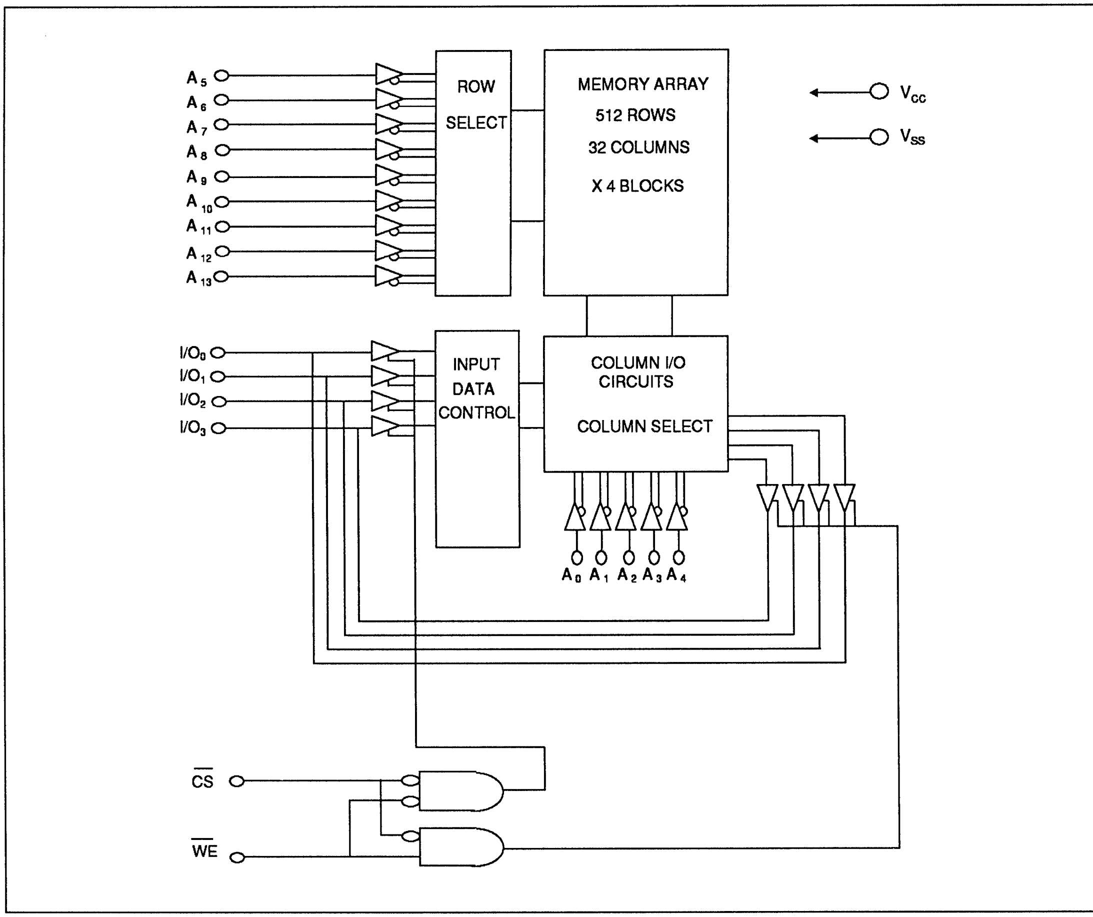
(TOP VIEW)



PIN NAMES

A_0-A_{13}	Address input
I/O_0-I/O_3	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}, V_{SS}	Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings

Symbol	Rating	Conditions	Value	Unit
V_{CC}	Supply voltage	$T_A = 25^{\circ}C$ with respect to V_{SS}	-0.3 to 7.0	V
V_{IN}	Input voltage		-0.3 to 7.0	V
PD	Power dissipation	$T_A = 25^{\circ}C$	1.0	W
T_{STG}	Storage temp.	-	-55 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	-	4.5	5	5.5	V
V_{IH}	"H" Input voltage	$V_{CC} = 5V \pm 10\%$	2.2	-	VCC+0.3	V
V_{IL}	"L" Input voltage		-0.3	-	0.8	V
T_{OPR}	Operating temperature	-	0		70	°C
CL	Output load	-	-	-	30	pF
TTL			-	-	1	-

Note: When pulse width is equal to or smaller than 20ns, V_{IH} max. $=V_{CC}+1.0V$, V_{IL} min = -1.0V.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{LI}	Input leakage current	V_I = 0 to V_{CC}	-1		1	µA
I_{LO}	Output leakage current	$\overline{CS} = V_{IH}$ $V_{I/O}$ = 0 to V_{CC}	-1		1	µA
V_{OH}	"H" output voltage	I_{OH} = -4mA	2.4		-	V
V_{OL}	"L" output voltage	I_{OL} = 8mA			0.4	V
I_{CCS}	Standby supply current (CMOS)	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ -0.2V			2	mA
I_{CCS1}	Standby supply current (TTL)	$\overline{CS} = V_{IH}$ T_{CYC} = min. cycle			30	mA
I_{CCA}	Operating supply current	Min. cycle			110	mA

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	$V_{IH} = 3.0V$, $V_{IL} = 0V$
Input rise and fall times	5 ns
Input/output timing reference level	1.5V
Output load	$C_L = 30pF$, 1 TTL gate

READ CYCLE

($V_{CC} = 5V \pm 10\%$, $T_A = 0^o$ to 70^oC)

Symbol	Parameter	71C88-45		71C88-55		71C88-70		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time		45		55		70	ns
t_{AC}	Address access time		45		55		70	ns
t_{CO}	Chip select access time		45		55		70	ns
t_{CX}	Chip selection to output active	5		5		5		ns
t_{OHA}	Output hold time from address change	5		5		5		ns
t_{OTD}	Output 3-state from deselection	0	25	0	25	0	30	ns
t_{PU}	Chip selection to power up time	0		0		0		ns
t_{PD}	Chip deselection to power down time	0	45	0	55	0	70	ns

Notes: 1. Read condition: During the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. T_{CX} and T_{OTD} are measured ± 200 mV from steady state voltage with specified loading in Figure 2.

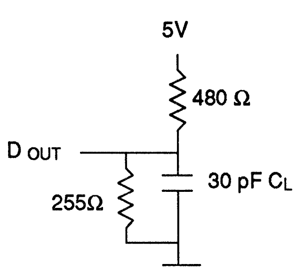


Fig. 1. Output load

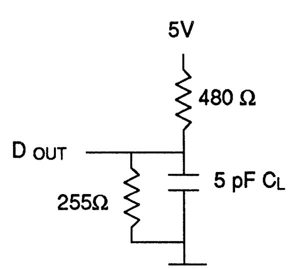
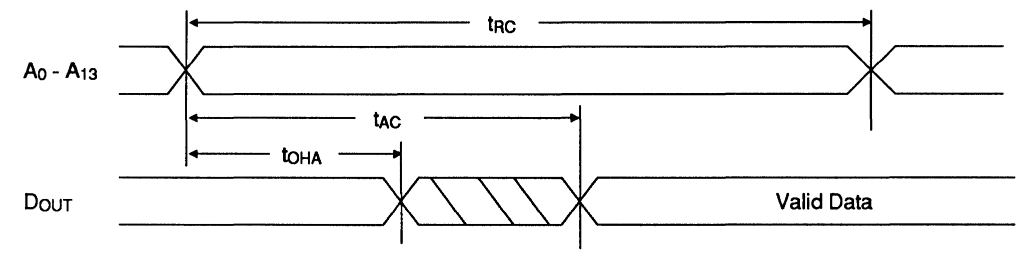


Fig. 2. Output load

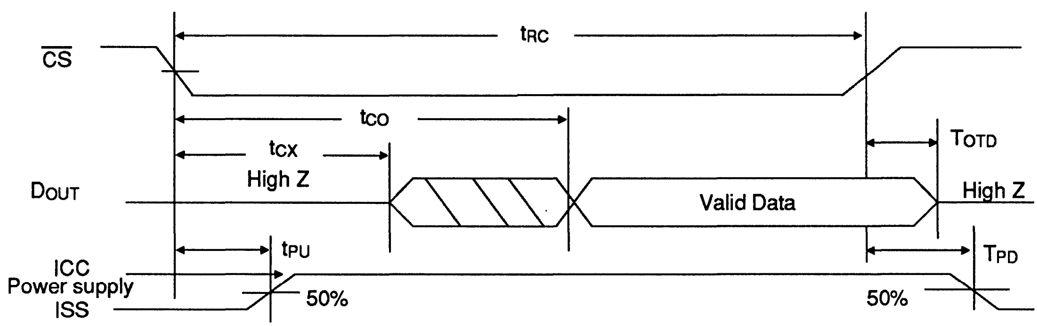
Note: C_L includes scope and jig.

READ CYCLE TIMING 1 <Address Controlled>



NOTE: $\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}

READ CYCLE TIMING 2 <CS Controlled>



NOTE: $\overline{WE}$ = V_{IH}

WRITE CYCLE [see notes following table for conditions]

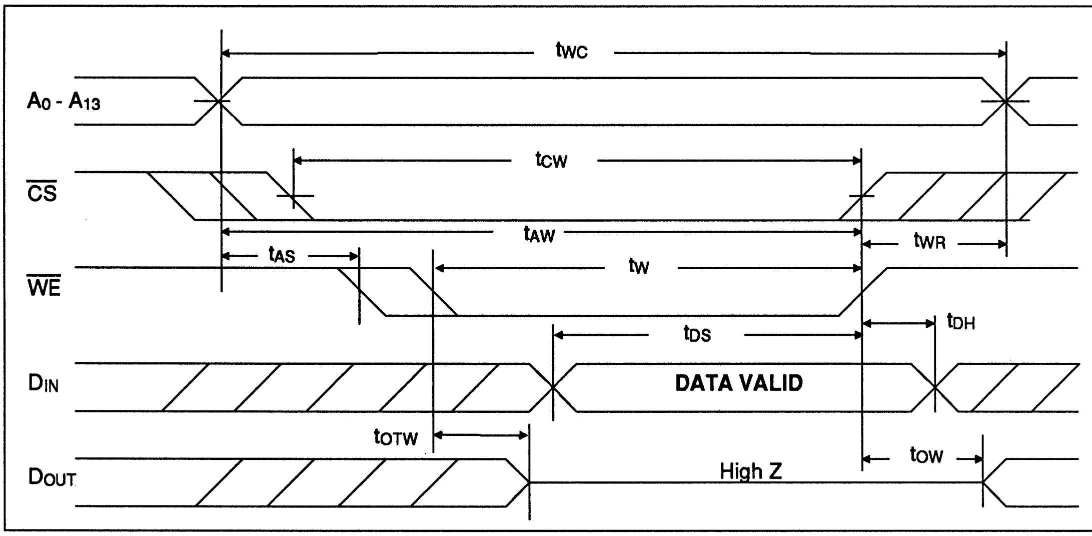
(T_A = 0° to 70°C)

Symbol	Parameter	71C88-45 Min.	71C88-45 Max.	71C88-55 Min.	71C88-55 Max.	71C88-70 Min.	71C88-70 Max.	Units
t_{WC}	Write cycle time	45		55		70		ns
t_{CW}	Chip selection to End of Write	40		45		55		ns
t_{AW}	Address valid to End of Write	40		45		55		ns
t_{AS}	Address to Write set-up time	0		0		0		ns
t_W	Write time	40		45		55		ns
t_{WR}	Write recovery time	5		10		15		ns
t_{DS}	Data set-up time	25		25		30		ns
t_{DH}	Data hold from write time	0		0		0		ns
t_{OTW}	Output 3-state from write	0	20	0	25	0	30	ns
t_{OW}	Output active from End of Write	0		0		0		ns

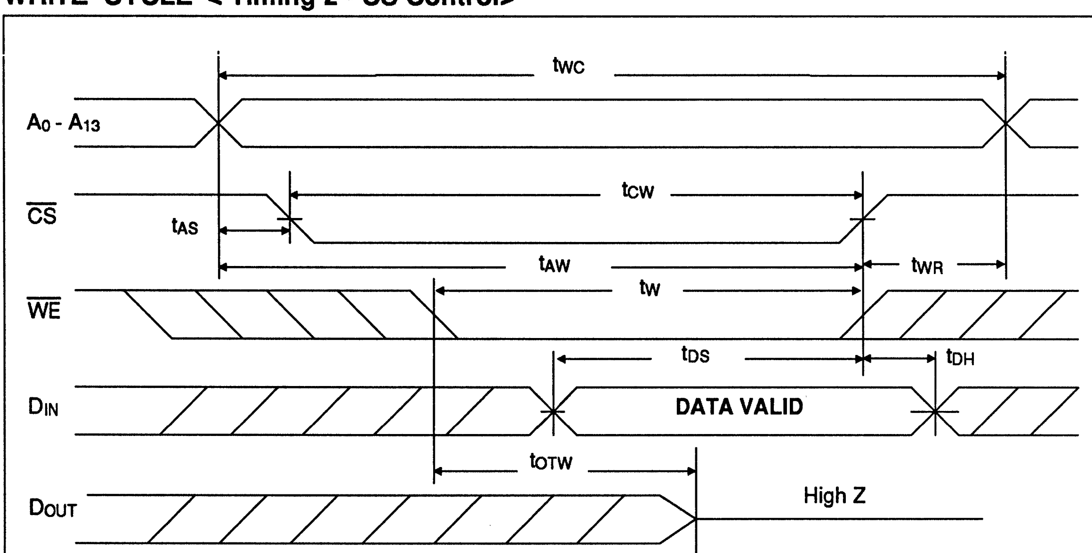
Notes:

1. Write condition: During the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
3. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
4. t_{WR}, t_{DS} and t_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
5. t_{OTW} and t_{OW} are measured ±200mV from steady state voltage with specified loading in Figure 2.
6. When I/O pins are in data output mode, don't force inverse input signals to those pins.

WRITE CYCLE <Timing 1 - $\overline{WE}$ Control>



WRITE CYCLE < Timing 2 - $\overline{CS}$ Control>



CAT71C256

32K x 8-BIT CMOS STATIC RAM

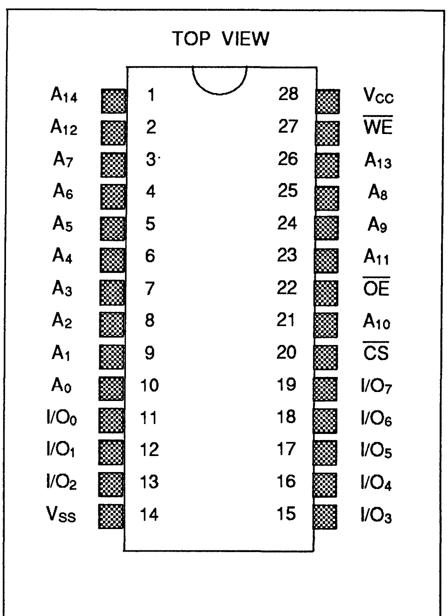
GENERAL DESCRIPTION

The CAT71C256 is a high performance 262,144 bit CMOS static RAM organized as a 32,768 X 8 bit array. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary. The CAT71C256 is a CMOS device that requires very low power during standby (1 mA). The $\overline{CS}$ and $\overline{OE}$ control signals facilitate OR-tying of the output lines, simplifying memory expansion.

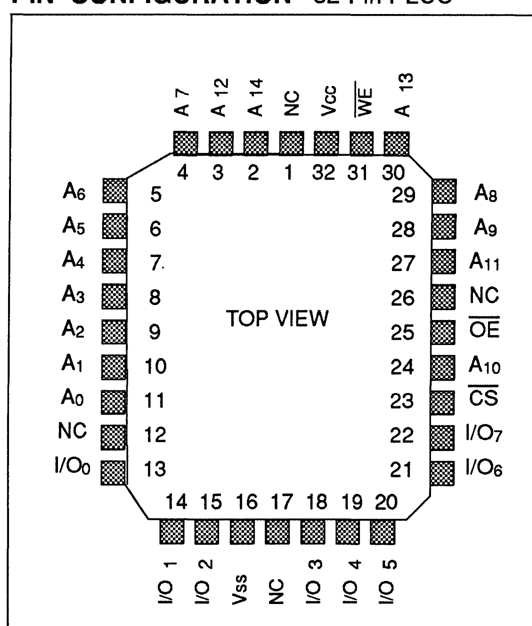
FEATURES

- Single 5 V supply (± 10%)
- Low power consumption
  385 mW max (operation)
  5.5 mW max (stand-by)
- 32,768 X 8 configuration
- Static operation
- Access / Cycle time
  85 ns max (CAT71C256-85)
  100 ns max (CAT71C256-10)
  120 ns max (CAT71C256-12)
- TTL compatible INPUT/OUTPUT
- Three state outputs
- 28-pin DIP, or 32-pin PLCC packages

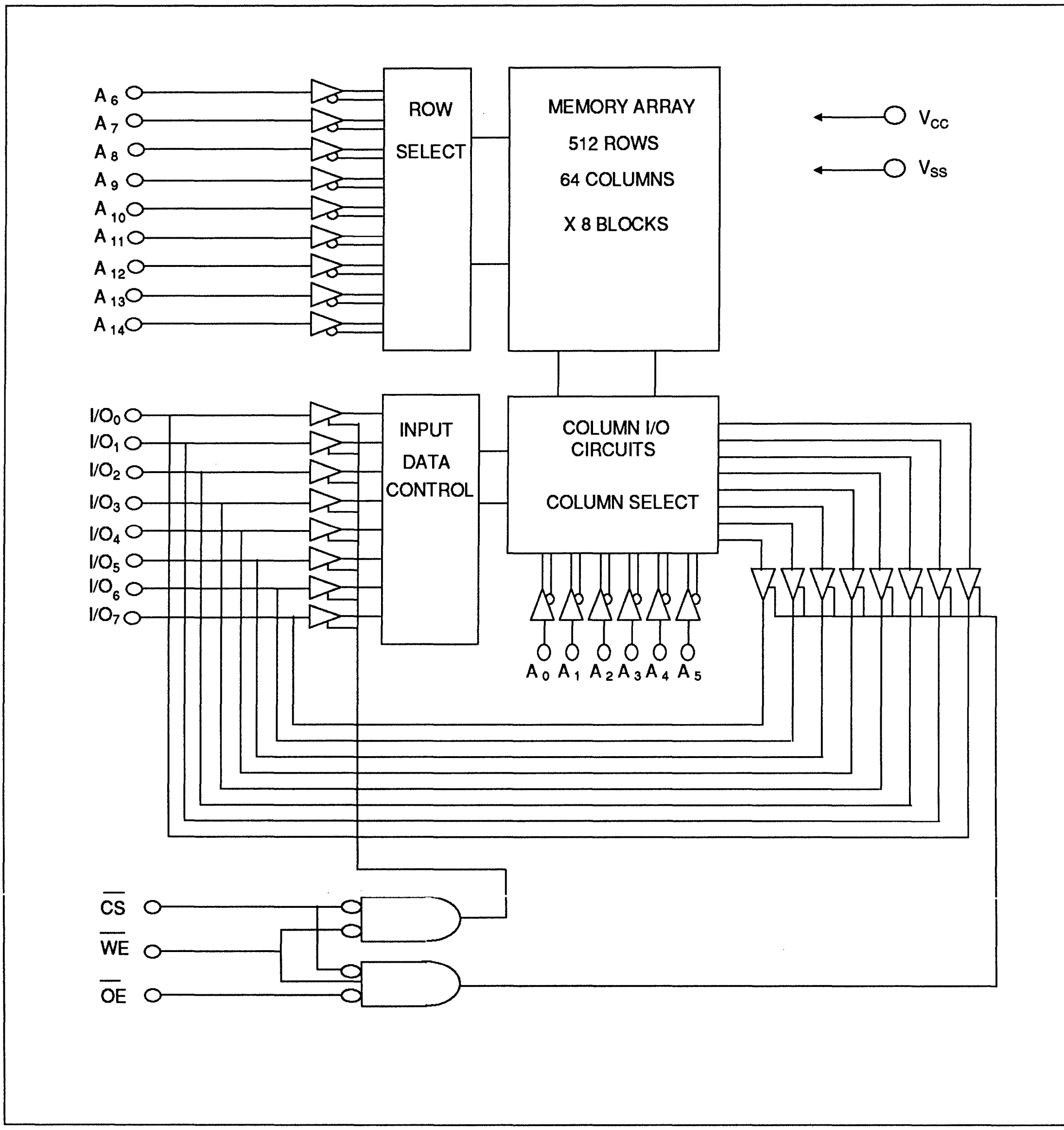
PIN CONFIGURATION 28-Pin DIP



PIN CONFIGURATION 32-Pin PLCC



BLOCK DIAGRAM



Pin Assignment [28 and 32 pin package]

A_0 - A_{14}	:Address inputs
I/O_0 - I/O_7	:Data input/output
$\overline{CS}$	:Chip select
$\overline{WE}$	:Write enable
$\overline{OE}$	:Output enable
V_{CC}, V_{SS}	:Supply voltage

MODES OF OPERATION

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X = H or L

Absolute Maximum Ratings

Symbol	Rating	Conditions	Value	Unit
V_{CC}	Supply voltage	T_A = 25°C, with respect to V_{SS}	-0.3 to 7.0	V
V_{IN}	Input voltage		-0.3 to V_{CC} +0.3	V
P_D	Power dissipation	T_A = 25°C	1.0	W
T_{STG}	Storage temp.	-	-55 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	V_{CC} = 5V ± 10%	4.5	5	5.5	V
V_{SS}				0		V
V_{CCH}	Data retention voltage		2	5	5.5	V
V_{IH}	"H" Input voltage	5V ± 10%	2.2	-	VCC +0.3	V
V_{IL}	"L" Input voltage		-0.3	-	0.8	V
T_{OPR}	Operating temp.		0	-	+70	°C
CL	Output load		-	-	100	pF
TTL			-	-	1	-

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{LI}	Input leakage current	V_{IN} = 0 to V_{CC}	-1		1	µA
I_{LO}	Output leakage current	$\overline{CS}$ or $\overline{OE}$ = V_{IH} VI/O = 0 to V_{CC}	-1		1	µA
V_{OH}	"H" output voltage	I_{OH} = -1mA	2.4		-	V
V_{OL}	"L" output voltage	I_{OL} = 2.1mA			0.4	V
I_{CCS}	Standby supply current (CMOS)	$\overline{CS}$ ≥V_{CC} -0.2V V_{IN} =0 to V_{CC}		0.2	1	mA
I_{CCS1}	Standby supply current (TTL)	$\overline{CS}$ = V_{IH} T_{CYC} = min. cycle			3	mA
I_{CCA}	Operating supply current	Min. cycle			70	mA

AC CHARACTERISTICS - TEST CONDITIONS

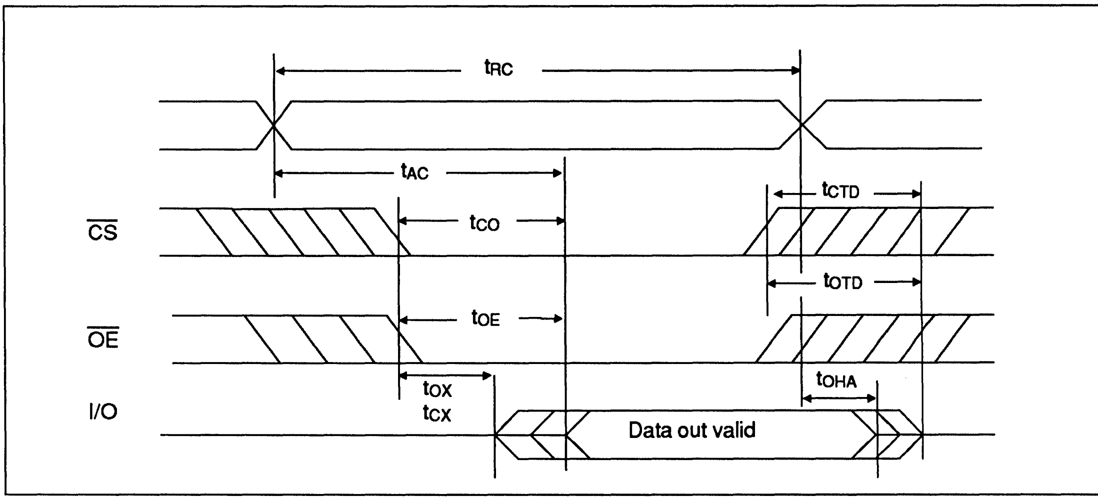
Parameter	Conditions
Input pulse level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall times	5 ns
Input/output timing reference level	1.5V
Output load	C_L = 100pF, 1 TTL gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_A = 0° to 70°C)

Symbol	Parameter	71C256-85 Min.	Max.	71C256-10 Min.	Max.	71C256-12 Min.	Max.	Units
t_{RC}	Read cycle time	85		100		120		ns
t_{AC}	Address access time		85		100		120	ns
t_{CO}	Chip select access time		85		100		120	ns
t_{OE}	Outut enable to output valid		45		50		60	ns
t_{CX}	Chip selection to output active	10		10		10		ns
t_{OHA}	Output hold time from address change	5		10		10		ns
t_{OTD}	Output 3-state from output disable	0	30	0	50	0	60	ns
t_{CTD}	Output 3-state from chip deselection		30		40		50	ns
t_{OX}	Output enable to output active	5		5		5		ns

READ CYCLE



NOTES:
1. A READ occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

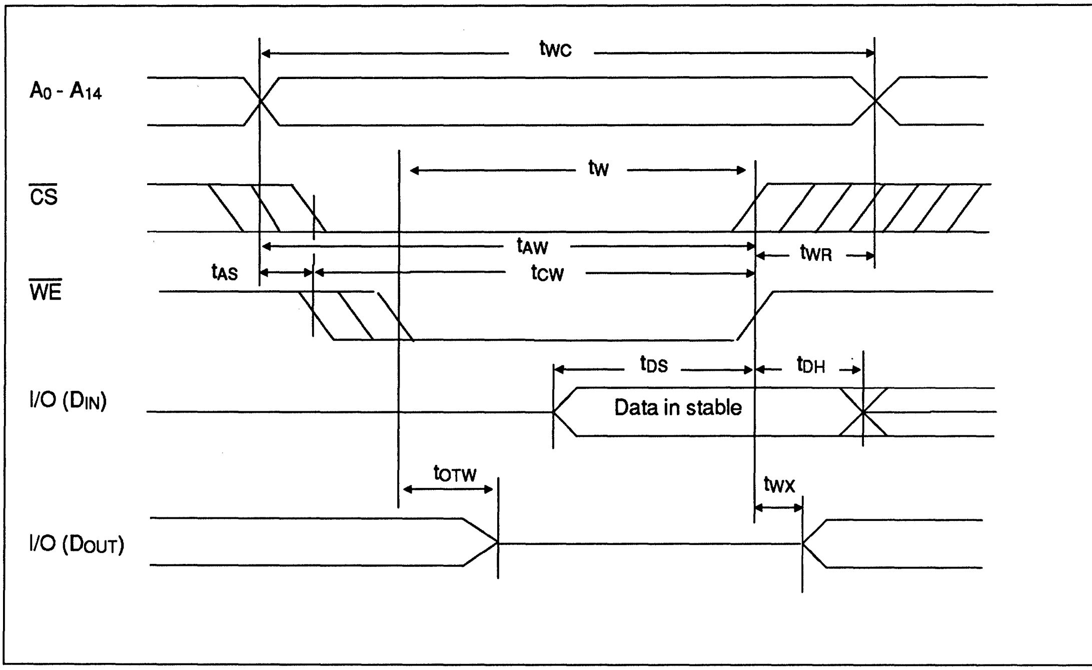
4

WRITE CYCLE

(T_A= 0° to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	71C256-85		71C256-10		71C256-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write cycle time	85		100		120		ns
t_{CW}	Chip selection to End of Write	75		90		100		ns
t_{AW}	Address valid to End of Write	75		90		100		ns
t_{AS}	Address to Write set-up time	0		0		0		ns
t_W	Write time	70		75		90		ns
t_{WR}	Write recovery time	5		10		10		ns
t_{DS}	Data set-up time	40		40		50		ns
t_{DH}	Data hold from write time	0		0		0		ns
t_{OTW}	Output 3-state from write	0	30	0	50	0	60	ns
t_{WX}	Output active from End of Write	5		5		5		ns

WRITE CYCLE TIMING



Notes:

1. Write condition: During the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write cycle.
3. t_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are in data output mode, don't force inverse input signals to those pins.

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	10	pF

Note: These parameters are periodically sampled and are not 100% tested.

CAT71C256L
32K x 8-BIT CMOS STATIC RAM

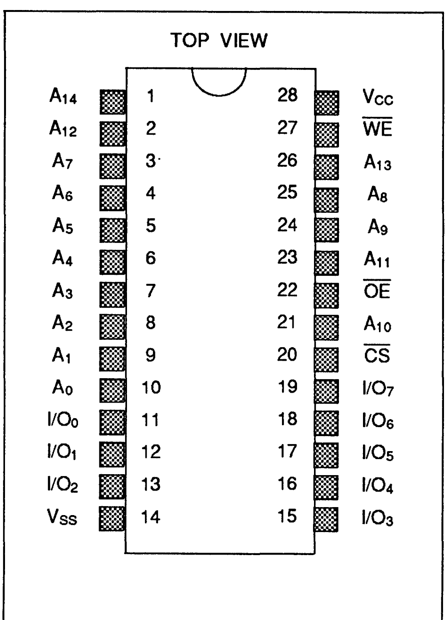
GENERAL DESCRIPTION

The CAT71C256L is a low power high performance 262,144 bit CMOS static RAM organized as a 32,768 X 8 bit array. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary. The CAT71C256L is a CMOS device that requires extremely low power during standby (100 μA). The $\overline{CS}$ and $\overline{OE}$ control signals facilitate OR-tying of the output lines, simplifying memory expansion.

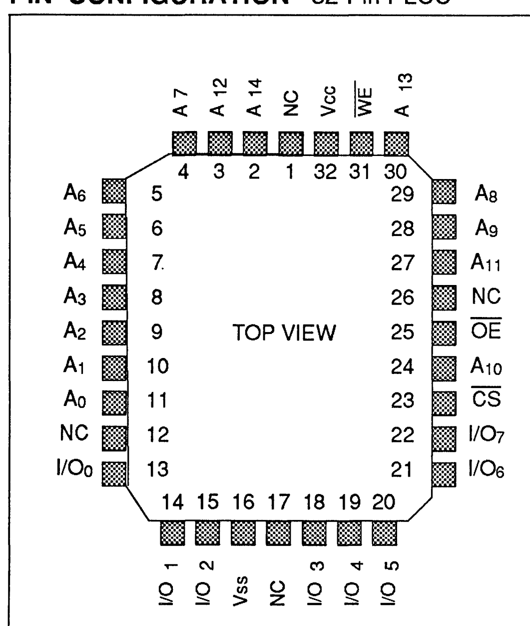
FEATURES

- Single 5 V supply (± 10%)
- Low power consumption
  385 mW max (operation)
  0.55 mW max (stand-by)
- 32,768 X 8 configuration
- Static operation
- Access / Cycle time
  85 ns max (CAT71C256L-85)
  100 ns max (CAT71C256L-10)
  120 ns max (CAT71C256L-12)
- TTL compatible INPUT/OUTPUT
- Three state outputs
- 28-pin DIP, or 32-pin PLCC packages

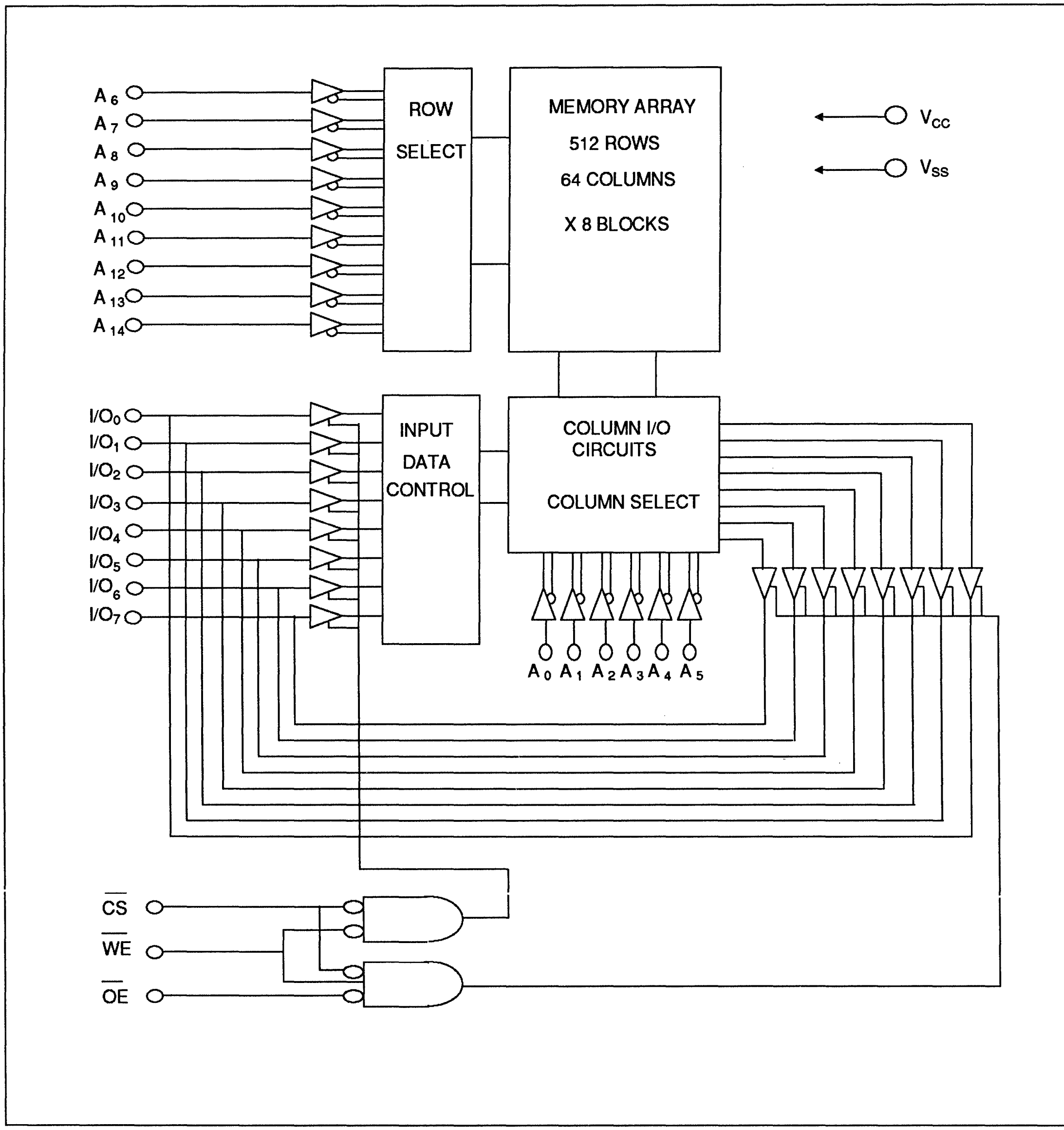
PIN CONFIGURATION 28-Pin DIP



PIN CONFIGURATION 32-Pin PLCC



BLOCK DIAGRAM



Pin Assignment [28 and 32 pin package]

A_0 - A_{14}	:Address inputs
I/O_0 - I/O_7	:Data input/output
$\overline{CS}$	:Chip select
$\overline{WE}$	:Write enable
$\overline{OE}$	:Output enable
V_{CC}, V_{SS}	:Supply voltage

MODES OF OPERATION

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X = H or L

Absolute Maximum Ratings

Symbol	Rating	Conditions	Value	Unit
V_{CC}	Supply voltage	T_A = 25°C, with respect to V_{SS}	-0.3 to 7.0	V
V_{IN}	Input voltage		-0.3 to V_{CC} +0.3	V
P_D	Power dissipation	T_A = 25°C	1.0	W
T_{STG}	Storage temp.	-	-55 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	V_{CC} = 5V ± 10%	4.5	5	5.5	V
V_{SS}				0		V
V_{CCH}	Data retention voltage		2	5	5.5	V
V_{IH}	"H" Input voltage	5V ± 10%	2.2	-	VCC +0.3	V
V_{IL}	"L" Input voltage		-0.3	-	0.8	V
T_{OPR}	Operating temp.		0	-	+70	°C
CL	Output load		-	-	100	pF
TTL			-	-	1	-

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{LI}	Input leakage current	V_{IN} = 0 to V_{CC}	-1		1	μA
I_{LO}	Output leakage current	$\overline{CS}$ or $\overline{OE}$ = V_{IH} VI/O = 0 to V_{CC}	-1		1	μA
V_{OH}	"H" output voltage	I_{OH} = -1 mA	2.4		-	V
V_{OL}	"L" output voltage	I_{OL} = 2.1 mA			0.4	V
I_{CCS}	Standby supply current (CMOS)	$\overline{CS}$ ≥V_{CC} -0.2V V_{IN} =0 to V_{CC}		2	100	μA
I_{CCS1}	Standby supply current (TTL)	$\overline{CS}$ = V_{IH} T_{CYC} = min. cycle			3	mA
I_{CCA}	Operating supply current	Min. cycle			70	mA

AC CHARACTERISTICS - TEST CONDITIONS

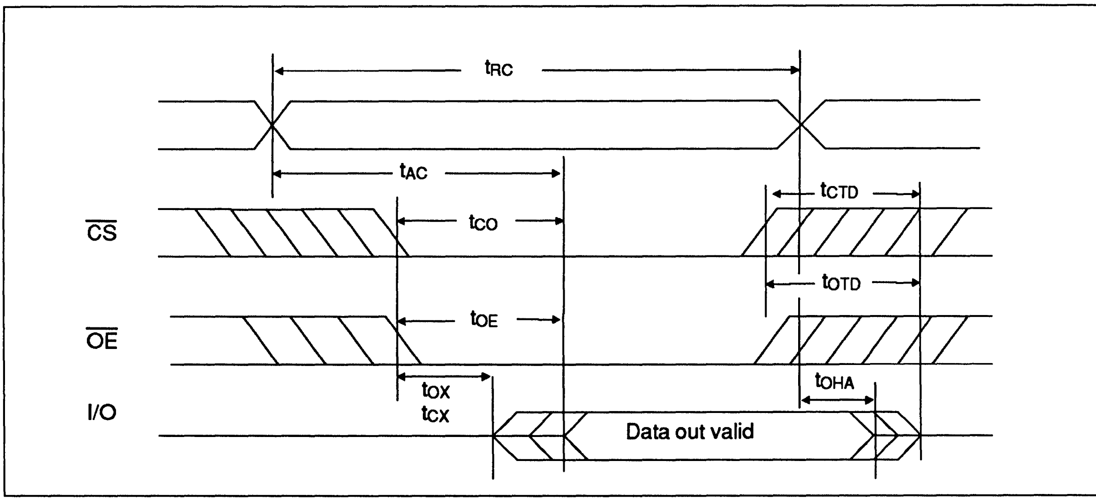
Parameter	Conditions
Input pulse level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall times	5 ns
Input/output timing reference level	1.5V
Output load	C_L = 100pF, 1 TTL gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_A = 0° to 70°C)

Symbol	Parameter	71C256L-85 Min.	71C256L-85 Max.	71C256L-10 Min.	71C256L-10 Max.	71C256L-12 Min.	71C256L-12 Max.	Units
t_{RC}	Read cycle time	85		100		120		ns
t_{AC}	Address access time		85		100		120	ns
t_{CO}	Chip select access time		85		100		120	ns
t_{OE}	Outut enable to output valid		45		50		60	ns
t_{CX}	Chip selection to output active	10		10		10		ns
t_{OHA}	Output hold time from address change	5		10		10		ns
t_{OTD}	Output 3-state from output disable	0	30	0	50	0	60	ns
t_{CTD}	Output 3-state from chip deselection		30		40		50	ns
t_{OX}	Output enable to output active	5		5		5		ns

READ CYCLE



NOTES:
1. A READ occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

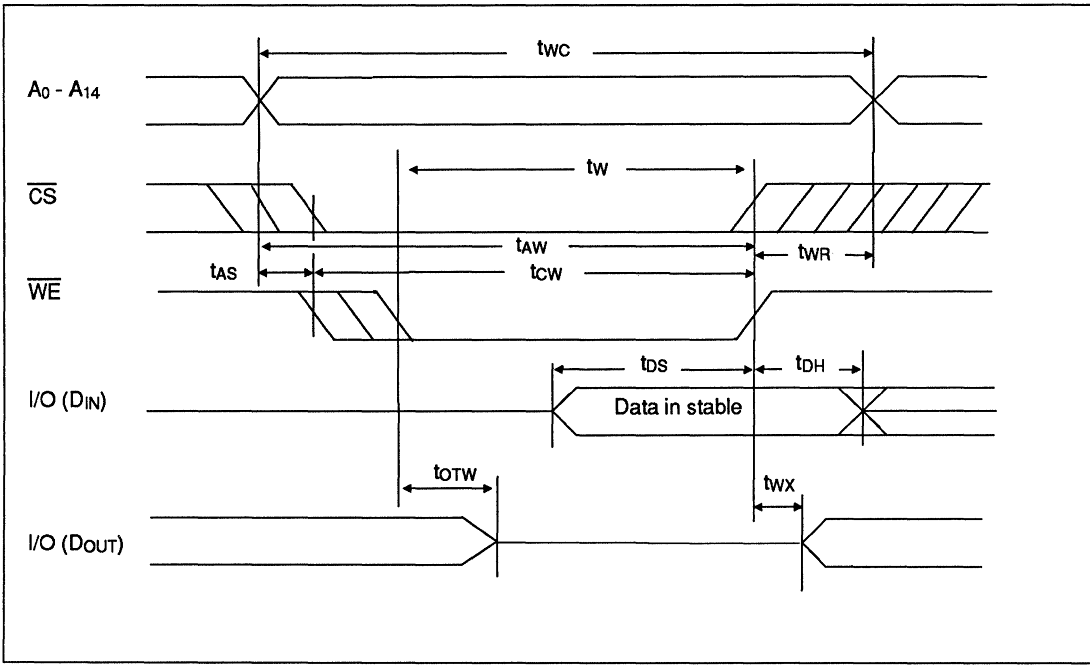
4

WRITE CYCLE

(T_A= 0° to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	71C256L-85		71C256L-10		71C256L-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write cycle time	85		100		120		ns
t_{CW}	Chip selection to End of Write	75		90		100		ns
t_{AW}	Address valid to End of Write	75		90		100		ns
t_{AS}	Address to Write set-up time	0		0		0		ns
t_W	Write time	70		75		90		ns
t_{WR}	Write recovery time	5		10		10		ns
t_{DS}	Data set-up time	40		40		50		ns
t_{DH}	Data hold from write time	0		0		0		ns
t_{OTW}	Output 3-state from write	0	30	0	50	0	60	ns
t_{WX}	Output active from End of Write	5		5		5		ns

WRITE CYCLE TIMING



Notes:

1. Write condition: During the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write cycle.
3. t_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are in data output mode, don't force inverse input signals to those pins.

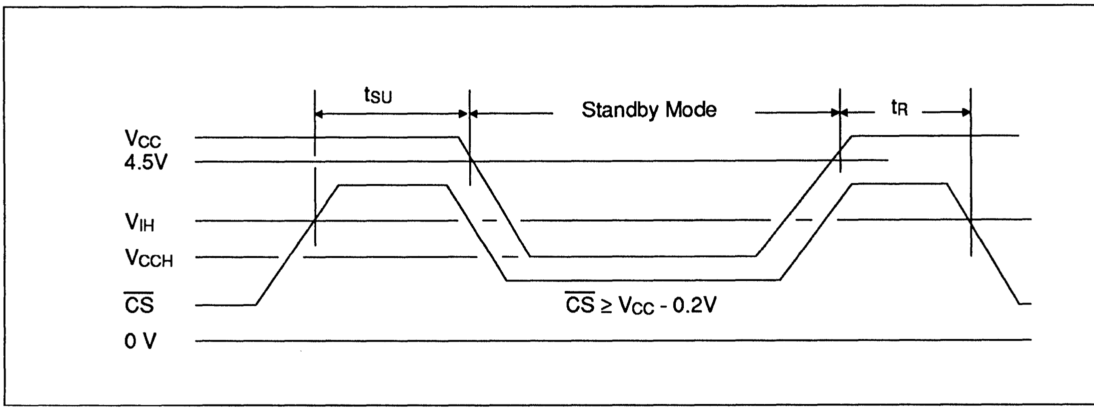
CAPACITANCE

($T_A = 25^oC$, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	10	pF

Note: These parameters are periodically sampled and are not 100% tested.

$\overline{CS}$ CONTROL



LOW V_{CC} DATA RETENTION CHARACTERISTICS

$T_A = 0^oC$ to 70^oC, unless otherwise noted.

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CCH}	V_{CC} for data retention	$\overline{CS} \geq V_{CC}$ -0.2V	2			V
I_{CCH}	Data retention current	$\overline{CS} \geq V_{CC}$ -0.2V, V_{CC} = 3V		1	50	µA
t_{SU}	$\overline{CS}$ to Data retention time		0			ns
t_R	Operation recovery time		t_{RC}			ns

4

MICROCOMPUTERs

5

CAT62C580

Smart Card Microcomputer

Description:

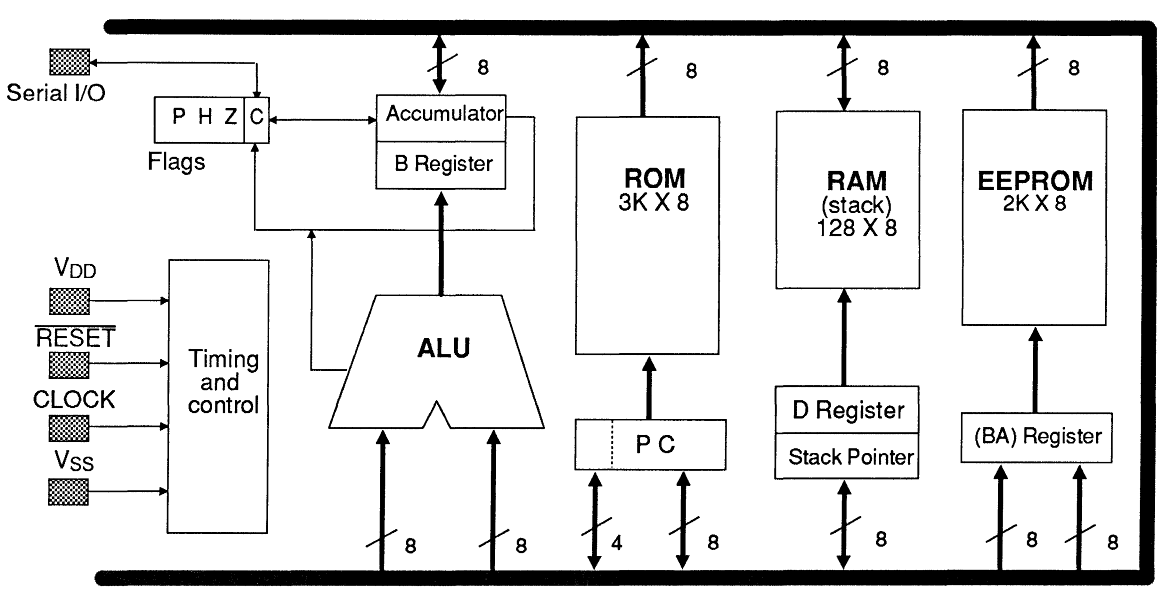
The **CAT62C580** is a single chip 8-bit microcomputer, with 16K-bits EEPROM, 3K-bytes ROM, and 128 bytes RAM. The built-in hardware security features protect the program memory (ROM cannot be dumped). The **CAT62C580**'s unique architecture makes it ideal for "***Portable Database***" applications, such as IC cards for banking, personal health records, and a variety of ID's including entry access, telephone debit cards, and large number of military applications.

Features:

- 8-Bit CPU, RAM, EEPROM, and ROM on a single chip
- Low Power CMOS Technology
- Hardware and Software Security
- Speed: 800 ns instruction cycle at 5 MHz
- Clock Frequency: D.C. to 5 MHz
- Single Pin, High Speed Serial I/O Interface
- 9600 baud using "DLY" instruction
- 14 Internal Registers
- 9 Addressing modes
- 95 Instructions
- 10,000 EEPROM erase/write cycles per byte
- Ten year EEPROM data retention

5

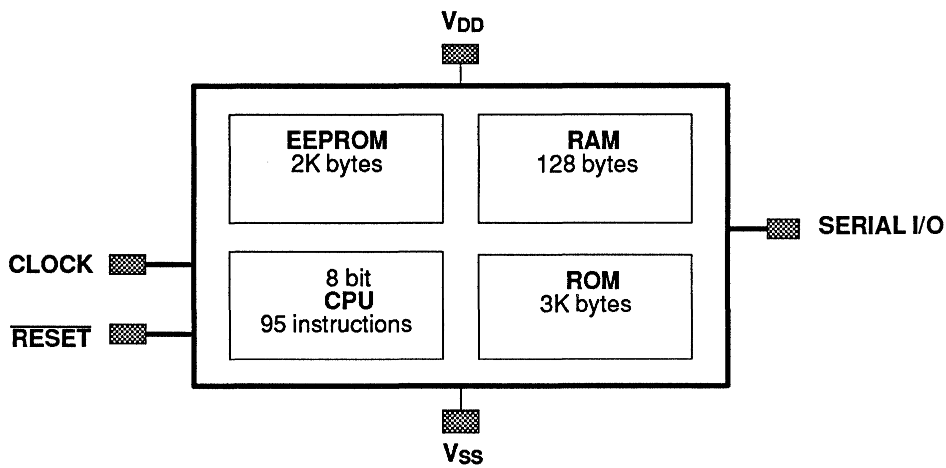
FUNCTIONAL BLOCK DIAGRAM



OPERATING CONDITIONS

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	4.5 to 5.5	Volts
Temperature Range	T_{OP}	0 to 70	^{o}C

PIN DESCRIPTION



Pin	Function	Input/Output
V_{DD}	Power supply pin, +5 Volts ± 10%	
V_{SS}	Power supply pin, 0 Volts	
CLOCK	CPU Clock input pin. Pulled down internally by approximately 100 K	INPUT
RESET	Resets the CPU. Pin is an active low input and is pulled down internally by approximately 100 K	INPUT
SERIAL I/O	Serial data input/output pin or pseudo bidirectional pin. The pin is pulled up by approximately 10 K, and is set high at CPU reset.	INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	$T_A = 25^oC$	-0.5 to 7	Volts
Input Voltage	V_I	$T_A = 25^oC$	-0.3 to V_{DD} +0.5	Volts
Output Voltage	V_O	$T_A = 25^oC$	-0.3 to V_{DD} +0.5	Volts
Storage Temperature	T_{stg}		-40 to 125	^oC

D.C. CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_A = 0^o$ to $+70^oC$)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current		I_{DD}	f = 5 MHz	-	4	10	mA
Low Input Voltage	CLOCK	V_{IL}	-	-0.3	-	0.5	Volts
	$\overline{RESET}$			-0.3	-	0.5	
	SERIAL I/O			-0.3	-	0.8	
High Input Voltage	CLOCK	V_{IH}	-	2.4	-	V_{DD}	Volts
	$\overline{RESET}$			4.0	-	V_{DD}	
	SERIAL I/O			2.0	-	V_{DD}	
Low Output Voltage		V_{OL}	I_{OL} MAX=1.6mA	0	-	0.4	Volts
High Output Voltage		V_{OH}	I_{OH} MAX $\geq$ -100μA	2.4	-	V_{DD}	Volts
Input Current (CLOCK, $\overline{RESET}$)		I_{IL1}	V_I = 0 (see note)	-	-	1	μA
		I_{IH1}	V_I =VDD (see note)	-	-	20	μA
Input Current (SIO) SERIAL I/O		I_{IL2}	V_I = 0 (see note)	-	-	-1	mA
		I_{IH2}	V_I =VDD (see note)	-	-	-1	μA
Input Capacitance		C_I	f = 1 MHz Ta = 25^oC	-	15	-	pF
Output Capacitance		C_O		-	20	-	pF

NOTE: CLOCK and $\overline{RESET}$ are pulled down internaly, and SERIAL I/O is pulled up.

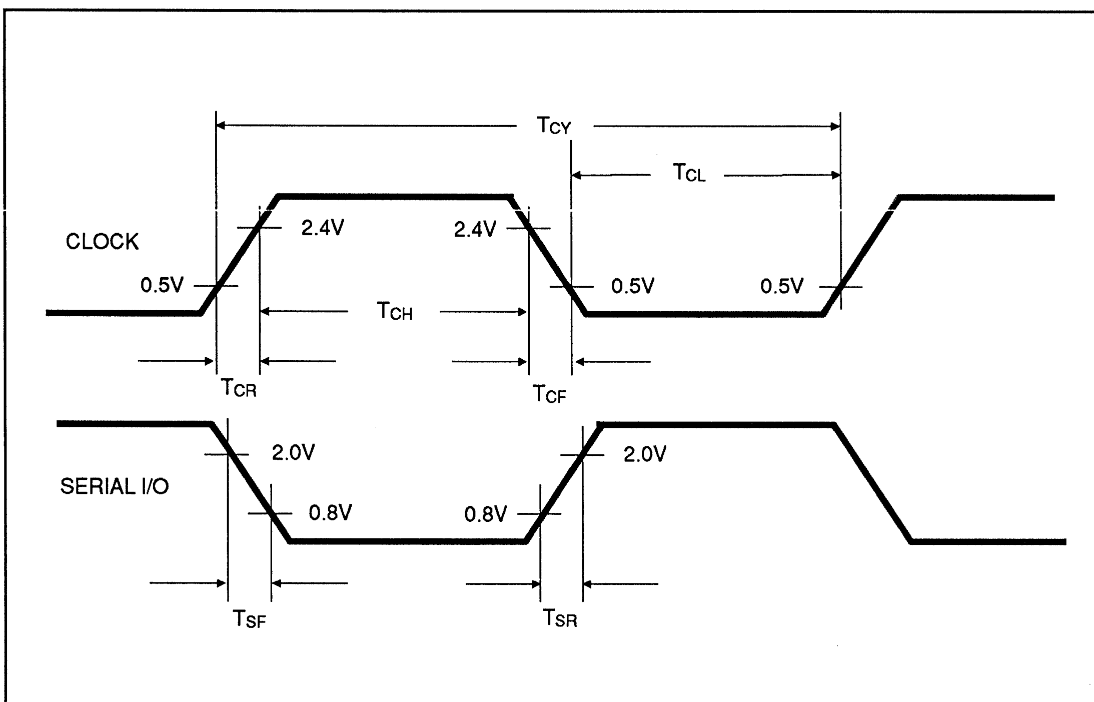
A.C. CHARACTERISTICS

(V_{DD} = 5 Volts ± 10%, Ta = 0° to +70°C)

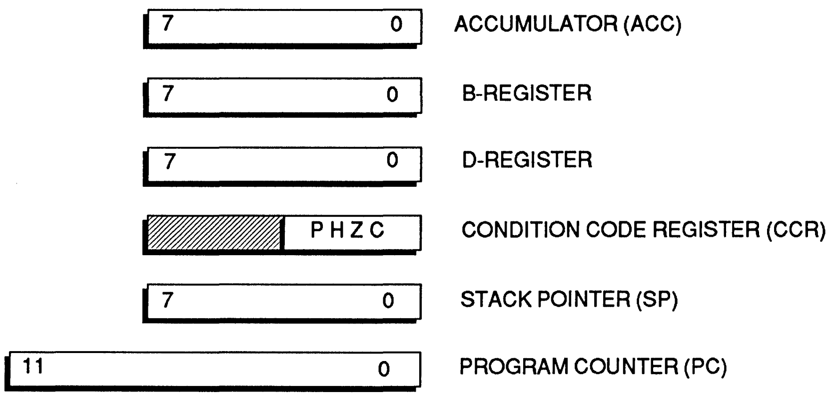
Parameter	Symbol	Min	Typ	Max	Unit
CLOCK Cycle Time	T_{CY}	200	-	-	ns
CLOCK Duty Cycle	$(T_{CH}/T_{CY})*100$	40	-	60	%
CLOCK Cycle Rise Time	T_{CR}	-	-	5.0	us
CLOCK Cycle Fall Time	T_{CF}	-	-	5.0	us
$\overline{\text{Reset}}$ Pulse Width	T_{RW}	$8*T_{CY}$	-	-	us
SERIAL I/O Rise Time	T_{SR}	-	-	5.0	us
SERIAL I/O Fall Time	T_{SF}	-	-	5.0	us

NOTE: Output load capacitance = 30pF.

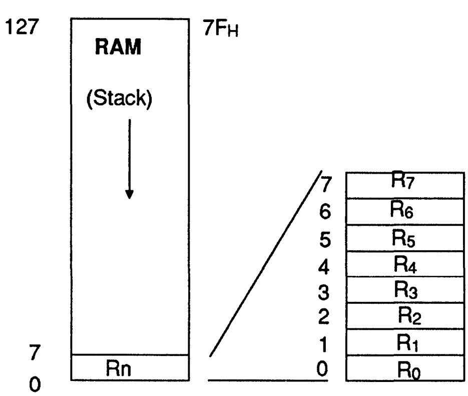
TIMING DIAGRAM



REGISTER SET

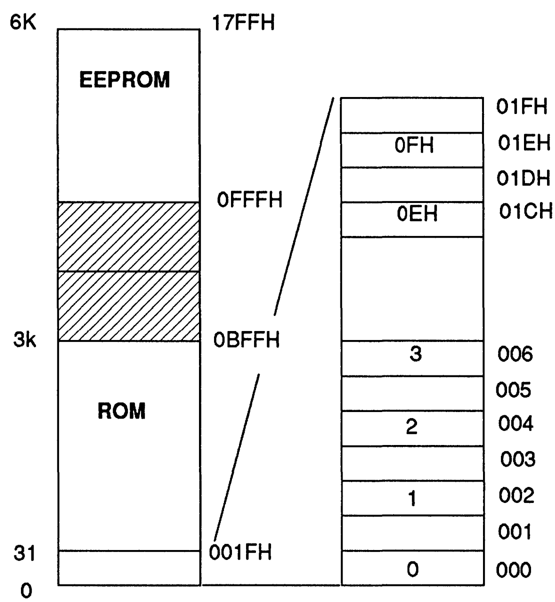


MEMORY MAP



Rn is the local register area of the RAM.

RAM map



ZP is the Zero Page addressed with the "CZP" instruction.

ROM and **EEPROM** map

INSTRUCTION SET

MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
MOV A, opr	B	A <-- B	1	1				*
	D	A <-- D	1	1				*
	@D	A <-- (D)	1	1				*
	@D+	A <-- (D), D <-- D+1	1	2				*
	@D-	A <-- (D), D <-- D-1	1	2				*
	N	A <-- (N)	2	2				*
	N+@D	A <-- (N + D)	2	3				*
	#N	A <-- #N	2	2				*
MOV opr, A	B	B <-- A	1	1				
	D	D <-- A	1	1				
	@D	(D) <-- (A)	1	1				
	@D+	(D) <-- A, D <-- D+1	1	2				
	@D-	(D) <-- A, D <-- D-1	1	2				
	N	(N) <--- A	2	2				
	N+@D	(N+D) <-- A	2	3				
MOV D, opr	Rn	D <-- Rn	1	2				
	#N	D <-- #N	2	2				
MOV Rn, opr	D	Rn <-- D	1	2				
	#N	Rn <-- #N	2	3				
MOV @BA, opr	@D	(BA) <--- (D)	1	4				
MOV @D, opr	@BA	(D) <--- (BA)	1	4				
MOV @D+, opr	#N	(D) <-- #N, D <-- D+1	2	2				
MOVW @D, opr	BA	(D) <-- A, (D+1) <-- B	1	3				
MOVW BA, opr	@D	A <-- (D), B <-- (D+1)	1	3				*
MOVW BA, opr	#N	A <-- #N_1, B <-- #N_2	3	3				*

MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
XCH A, opr	B	A <--> B	1	2				*
	D	A <--> D	1	2				*
	@D	A <--> (D)	1	2				*
	N	A <--> (N)	2	2				*
XCH D, opr	B	D <--> B	1	2				
	SP	D <--> SP	1	2				
XCH C, opr	P	C <--> P	1	1	*	*		
ADD A, opr	@D	A <-- A + (D)	1	1	*		*	*
	N	A <-- A + (N)	2	2	*		*	*
	#N	A <-- A + #N	2	2	*		*	*
ADC A, opr	@D	A <-- A + (D) + C	1	1	*		*	*
	N	A <-- A + (N) + C	2	2	*		*	*
	#N	A <-- A + #N +C	2	2	*		*	*
DAA		Decimal Adjust	1	1	*			*
CMP A, opr	@D	A is compared with (D)	1	1	*			*
	N	A is compared with (N)	2	2	*			*
	#N	A is compared with #N	2	2	*			*
CMP @D, opr	@BA	(D) is compared with (BA)	1	4	*			*
EOR A, opr	@D	A <-- A ⊻ (D)	1	1				*
	N	A <-- A ⊻ (N)	2	2				*
	#N	A <-- A ⊻ #N	2	2				*
OR A, opr	@D	A <-- A ORed with (D)	1	1				*
	N	A <-- A ORed with (N)	2	2				*
	#N	A <-- A ORed with #N	2	2				*
AND A, opr	@D	A <-- A ANDed with (D)	1	1				*
	N	A <-- A ANDed with (N)	2	2				*
	#N	A <-- A ANDed with #N	2	2				*

MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
INC opr	A	A <-- A + 1	1	1				*
	D	D <-- D + 1	1	1				
	@D	(D) <-- (D) + 1	1	1				*
	N	(N) <-- (N) + 1	2	2				*
DEC opr	A	A <-- A - 1	1	1				*
	D	D <-- D - 1	1	1				
	@D	(D) <-- (D) - 1	1	1				*
	N	(N) <-- (N) - 1	2	2				*
RRC opr	A	→ C → A_7 to A_0 →	1	1	*			*
	@D	→ C → $(D)_7$ to $(D)_0$ →	1	1	*			*
	N	→ C → $(N)_7$ to $(N)_0$ →	2	2	*			*
RLC opr	A	← C ← A_7 to A_0 ←	1	1	*			*
	@D	← C ← $(D)_7$ to $(D)_0$ ←	1	1	*			*
	N	← C ← $(N)_7$ to $(N)_0$ ←	2	2	*			*
PUSH opr	PSW	(SP) <- A, (SP -1) <- CCR, SP <-- SP -2	1	3				
	D	(SP) <-- D, SP <-- SP -1	1	2				
POP opr	PSW	CCR <-(SP -1), A <-(SP -2) SP <-- SP + 2	1	3	*	*	*	
	D	D <-- SP+1, SP <-- SP+1	1	2				
JZ opr	addr	if Z=1, PC <- PC+2+addr	2	2/3				
JNZ opr	addr	if Z=0, PC <- PC+2+addr	2	2/3				
JC opr	addr	if C=1, PC <- PC+2+addr	2	2/3				
JNC opr	addr	if C=0, PC <-- PC+2+addr	2	2/3				
JB opr	baddr,addr	if (baddr)=1, PC <-- PC+3+addr	2	3/4				
JNB opr	baddr,addr	if (baddr)=0, PC <-- PC+3+addr	2	3/4				
DJNZ opr	Rn,addr	(Rn) <-- (Rn)-1, if Rn = 0, PC <-- PC+2+addr (n=4 to 7)	2	3/4				
JMNE opr	#N,addr	if (D) ≠ #N, PC <-- PC + 3 + addr	3	3/4				
JDNE opr	#N,addr	if D ≠ #N, PC <-- PC + 3 + addr	3	3/4				
JMP opr	addr	PC <-- addr (0 to 4K)	2	2				

MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
CAL opr	addr	(SP) <-- PC+2, PC <-- addr, SP <-- SP - 2	2	4				
CZP opr	addr	(SP) <-- PC+2, PC <-- ZP, SP <-- SP - 2	1	4				
RT		PC <- (SP), SP <- SP+2	1	3				
NOP		No Operation	1	1				
CLR opr	A	A <-- 0	1	1				*
RC		C <-- 0	1	1	0			
SC		C <-- 1	1	1	1			
RB opr	baddr	(baddr) <-- 0	2	2				
SB opr	baddr	(baddr) <-- 1	2	2				
CPL opr	A	A <-- A	1	1				*
	C	C <-- C	1	1	*			
CHK opr	P	P <- C, if A=odd, C <- 1 else C <- 0	1	1	*	*		
SIN		C <-- SI/O	1	1	*			
SOUT		SI/O <-- C	1	1				
DLY opr	N	Delay N+3 Cycles	2	3 to 259				

NOTE: One instruction cycle time is equal to 4 divided by the clock frequency.

5

CAT62C780

Smart Card Microcomputer

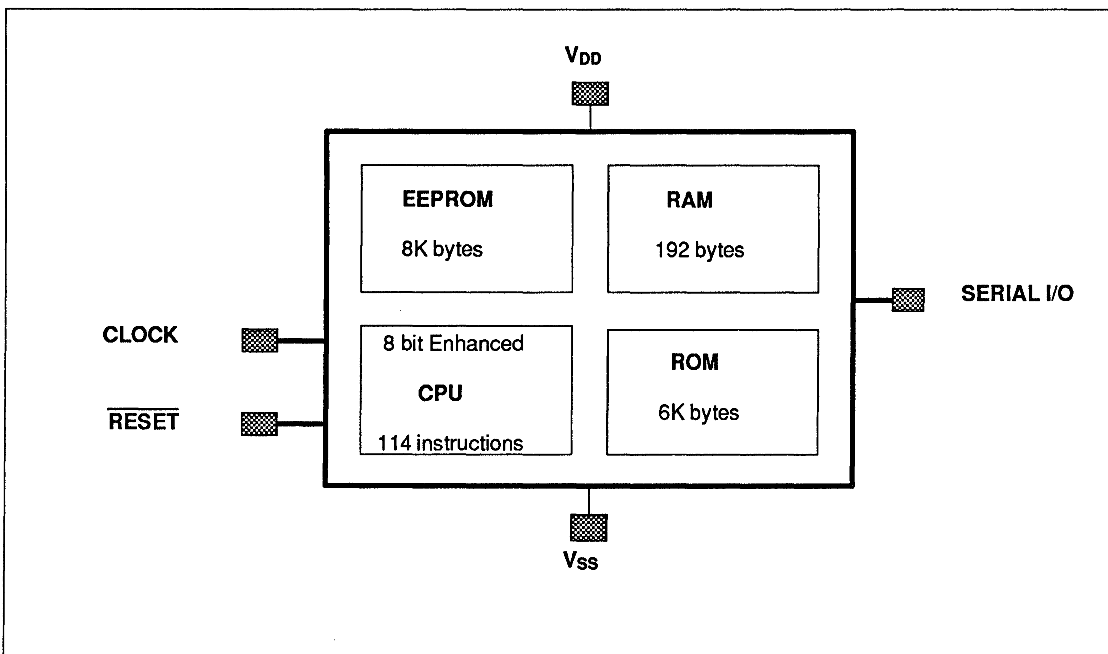
Preliminary

Description:

The **CAT62C780** is a single chip 8-bit microcomputer, with 8K-bytes of EEPROM, 6K-bytes ROM, and 192 bytes RAM. The built-in hardware security features protect the program memory (ROM cannot be dumped). The **CAT62C780**'s unique architecture makes it ideal for "***Portable Database***" applications, such as IC cards for banking, personal health records, and a variety of ID's including entry access, telephone debit cards, and large number of military applications.

Features:

- Enhanced 8-Bit CPU, RAM, EEPROM, and ROM in a single chip
- Low Power CMOS Technology
- Hardware and Software Security
- Speed: 800 ns instruction cycle at 5 MHz
- Clock Frequency: D.C. to 5 MHz
- Single Pin, High Speed Serial I/O Interface
- 114 Instructions
- 10,000 EEPROM erase/write cycles per byte
- Ten year EEPROM data retention
- Downward compatible with the CAT62C580
- ECC
- Page Write



APPLICATION NOTES

6

Using Catalyst's Serial EEPROMS in Shared Input/Output Configuration

by Asim Bajwa
5/88

Catalyst Semiconductor's family of serial EEPROMs utilizes four signals for the communication interface; Chip Select (CS) for device selection, Serial Clock (SK or CLK) for synchronizing serial data to and from the device, Data Input (DI) to input serial data to the device, Data Output (DO) to output serial data from the device. This interface can be reduced to 3 signals by sharing DI and DO as a common input/output signal. However, the following precautions should be taken to prevent problems due to DI/DO contention:

1) **READ Instruction in shared DI/DO configuration:**
(applies to 93C46, 59C11, 35C102/202, 35C104/204)

DO remains in high impedance while most of the READ instruction (i.e. start bit, opcode and address) is being input and offers no contention to the DI driver on a shared DI/DO signal. However, typically 50ns after the rising edge of the serial clock shifts in the least significant bit of the address stream (A0), DO outputs the '0' dummy bit to flag the beginning of the output data stream. If A0 is a '1' and the DI driver has not been disabled by the time the '0' dummy bit becomes valid, a low impedance path between the system power supply and ground is created through the DI driver pullup and DO pulldown device (Fig. 1).

Unless this condition causes excessive noise on the system power supply (which may in turn cause noisy or spurious signals to the device), the READ instruction will continue and complete normally since A0 is already shifted into the device.

To minimize potential problems during this low impedance condition, a current limiting resistor should be placed between the DI driver and the DO pin when using the shared DI/DO signal (Fig. 2).

Alternatively, an open drain (or open collector) DI driver with pullup resistor can be used (Fig. 2).

In either case, the clocking rate should be slow enough to ensure that the resistor can charge or discharge the shared DI/DO bus capacitance before the appropriate clock edge. For example, if the resistor used is 10kohm, and the bus capacitance is 100pF, then a safe clock rate is calculated to be:

Clock Period (T) = 2 x 3RC
= 2 x 3 x 10kΩ x 100pF
= 6 μsec

Frequency (f) = 1 / T
= 167kHz

2) **Programming Instructions in shared DI/DO configuration:**
(applies to 93C46, 35C102 and 35C104 only)

All devices in the Catalyst serial EEPROM family feature self-timed programming cycles. A programming status signal indicates whether the self-timed programming cycle is still in progress or has been completed. A '0' status signal indicates that the device is still programming. A '1' status signal indicates that the programming cycle has been completed and the device is is ready to receive the next instruction. This feature will allow a user to minimize the programming time (t_{EW}).

The 59C11, 35C202 and 35C204 devices have a separate ready/busy signal pin (RDY/BUSY) to output the programming status signal. The DO signal stays in high impedance throughout the programming cycle and therefore will not interfere with the DI signal in a shared DI/DO configuration.

On the 93C46, 35C102 and 35C104 serial EEPROMs, the programming status signal can be

6

read on the DO pin by bringing CS high after initiating a programming cycle. In a 4-signal interface, after a programming cycle the status signal is reset to high impedance by the start bit of the next instruction (Fig. 3).

In a shared DI/DO configuration, the '1' status signal on DO can be clocked into the device as a start bit and reset the status signal before it can be read, or otherwise interfere with the DI signal for the next instruction cycle. The following steps are recommended to avoid these conditions for a 3-signal interface (Fig. 4):

a) The clock (SK) should be stopped after shifting in the programming instruction. This prevents the '1' ready status from resetting the status signal before it can be read.

b) After reading the '1' ready status, at least one clock pulse should be input to the device while the DI/DO signal is '1' in order to reset the status signal.

c) CS should then be brought low to reset the instruction logic.

The next instruction can now be executed without any contention from the DO signal.

Figure 1a. DI/DO contention timing during read cycle

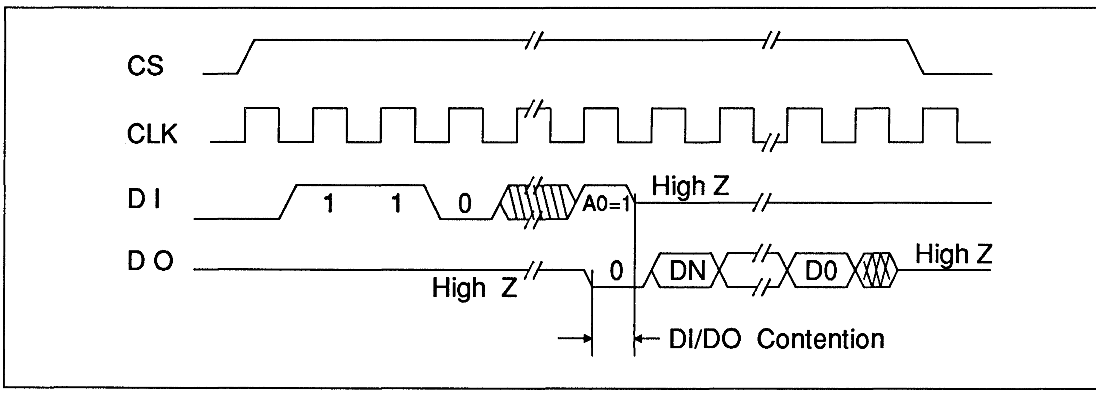


Figure 1b. Current path

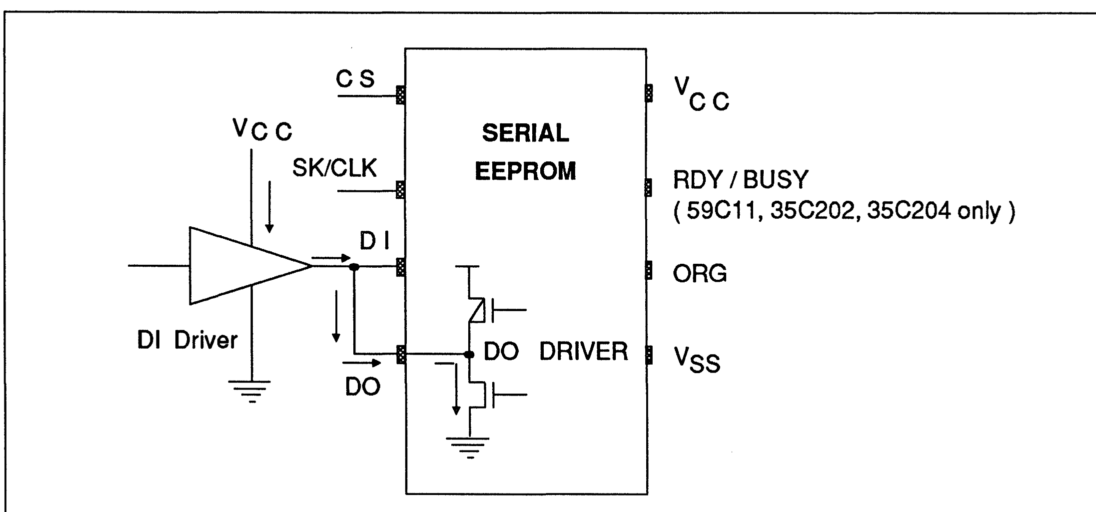


Figure 2. Three possible configurations to minimize problems due to contention

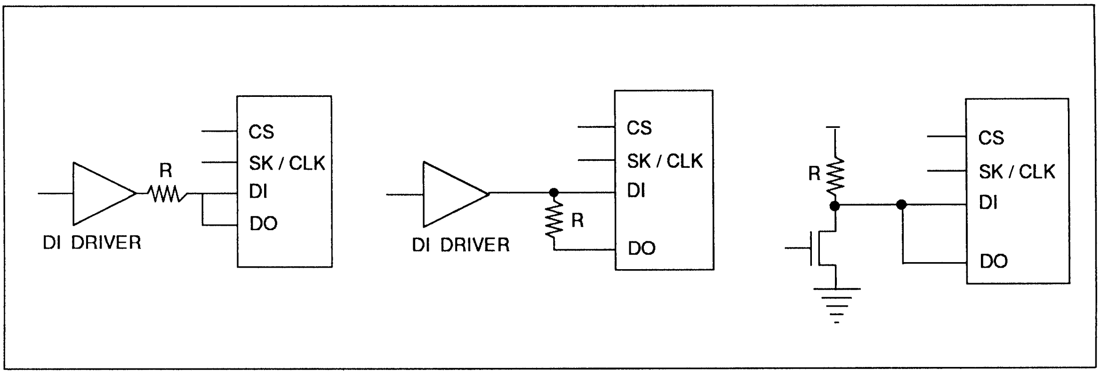


Figure 3. Programming instruction and status reset with 4-signal interface

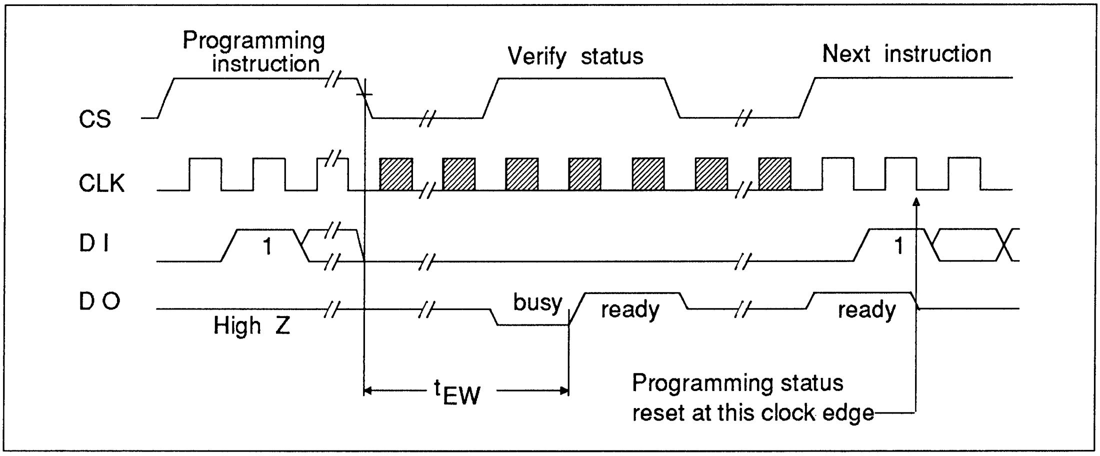
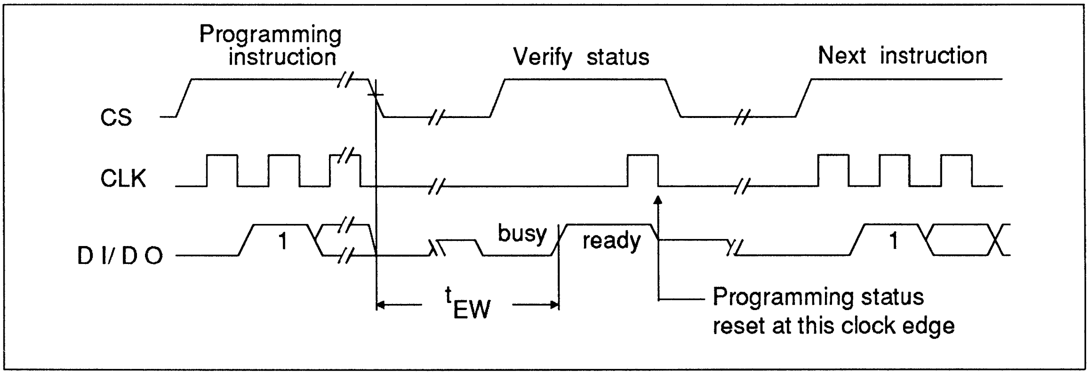


Figure 4. Programming instruction and status reset with 3-signal interface



6

Serial EEPROM Programming Time Optimization
Using the CAT59C11 and CAT93C46 in 8 and 16-bit word organization

by Christophe Chevallier
3/88

Many applications with serial EEPROMS require the storage of bytes. The best way to optimize programming speed is to program 2 bytes at a time, using the x16 organization, and then switch to the byte organization for the read operation.

In the 16-bit organization, 16 bits are programmed simultaneously. The write time is the same for 8 or 16 bits : maximum is 10 ms. Writing the whole array (128 bytes) this way will save 0.64s.

To operate the EEPROM this way, the processor controlling the data transfer should control the ORG pin (pin 6). At V_{IL} the chip is in the x8 (byte) organization, at V_{IH} the chip is in the x16 (word) organization.

Getting into programming mode
Before programming the memory, an EWEN (erase/write enable) operation should be performed. It needs to be done only once after the chip has been powered up. To protect the memory against undesirable write operations, the programming operations can be disabled by doing an EWDS (erase/write disable). It is safe to perform an EWDS if the chip is not being programmed, to avoid a false write in case of power transients. These operations (EWEN, EWDS) can be performed with the ORG pin high or low. Changing the state of the ORG pin will not change the status of the chip whether programming is enabled or disabled.

To write a 16-bit word, once the ORG and the CS pins are high, the start bit and the write opcode '01' are entered, followed by the 6-bit address (for a 1Kbit memory) and the 2 data bytes to be written. Since the device is functionally static, the SK clock can be maintained high or low long enough to give time to the processor to fetch the second data byte. The programming will start at the end of the data acquisition (59C11) or when CS goes down (93C46).

Reading at the correct address
The internal memory, in the byte organization, is divided into 2 pages of 64 bytes, the high page with A6=1 and the low page with A6=0. When writing a 16-bit word, the first 8 bits entered correspond to the high page address, the last 8 bits to the low page address. (See bit maps and example). Using hexadecimal notation, the low page addresses are 0 to 3F, the high page addresses are 40 to 7F. In the 16-bit organization, only the addresses 0 to 3F are used. To get the byte address of the first byte entered, add 40 to the address used in the x16 mode. (In the example, 40 + 2E = 6E).

For example, consider the following operations:

Using x16 mode, WRITE at address 2E the data A65B. (See map 1). This will be done with ORG pin high, entering a 6-bit address.

Using x8 mode (ORG pin low, entering a 7-bit address), a READ at address 2E wil output 5B, a READ at address 6E will output A6. (See map 2).

Floating the ORG pin
The ORG pin can be left floating, in this case an internal pull-up resistor will bring the pin high, selecting the 16-bit organization. When switching the ORG pin from V_{IL} to floating, care should be taken to leave enough time for the ORG pin to reach V_{IH}.

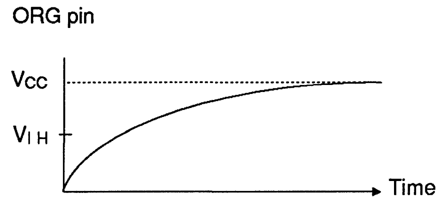
This time depends on the capacitance of the line arriving on the ORG pin. The internal pull-up is small, in order to stay within the 10 µA input leakage specification. Typically, the leakage current on this pin is around 5µA at V_{IL} = 0V, and will decrease at higher input voltage.

(continued)

6

Therefore, for a 100pF line capacitance, it will require $T = C\,V / I = 100pF \times 2V / 2.5\mu A$ (average pull-up current). $T = 80\ \mu s$

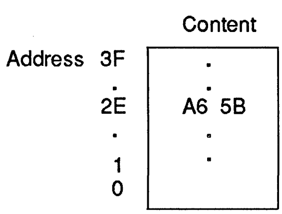
In this example, the processor should wait 100μs after releasing the ORG pin before starting a new operation. The best way to avoid this wait is to drive the ORG pin high instead of letting it float.



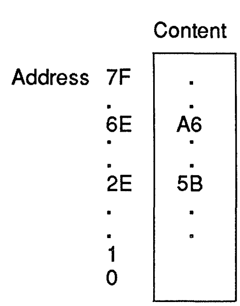
D_{IN} / D_{OUT} PATTERNS

	Start	Opcode	Address	Data
Write @ 2E, Data A65B	1	01	10 1110	1010 0110 0101 1011
Read @ 6E, Data A6	1	10	110 1110	1010 0110
Read @ 2E, Data 5B	1	10	010 1110	0101 1011

LOGICAL BIT MAP 1: x 16 ORGANIZATION



LOGICAL BIT MAP 2: x BYTE ORGANIZATION



CAT93C46 / CAT35C102 to 8051 Microcontroller Communication

Using the 8051's Built-in Shift Register

by Jim Troutner
5/88

The CAT93C46, and CAT35C102 are serial access EEPROMs intended for use with many of todays standard microcontrollers and microcomputers. To operate the serial EEPROM, first select the device by driving the CS pin to a logic one state, and shift in the instructions, address, and data into the EEPROMs DI pin. All data is shifted in on the rising edge of the SK clock, while data being read from the device appears at the DO pin a short time delay (tpd) after the rising edge of the SK clock.

This all seems to be very straight forward and in most application few problems will be encountered. However in some applications were it is desired to interface to microcontrollers with built in shift registers, such as the 8051, some special problems must be considered.

First the instruction, address, and data of the memory device can range from 9 bits (for the CAT93C46 organized as 64 X 16) to as many as 12 bits (for the CAT35C104 organized as 512 X 8). While the built in shift register of many microcontrollers will only send and receive multiples of 8 bits. This problem can be solved by shifting all the extra bits (require to make a multiple of 8) into the memory as zeros before the start bit is sent (all leading zeros shifted into the EEPROM will be ignored).

Next, the clock line on some of these microcontrollers is initially a logic one, a clock consist of a falling edge and then a rising edge. The problem here is that the EEPROM requires the last clock of any operation to have a falling edge before the EEPROM is deselected. With the 8051 (or any other microcontroller that clocks in the same manner) the falling edge the the first clock is ignored, and the last clock is left in the logic one state.

The solution here would be to simply add one additional clock pulse to the SK pin before deselecting the device. Another solution (for those processors that must send 8 clocks) is to send one byte of zeros then deselect the device. Additional zeros clocked into the EEPROM after the instruction, address, and data are shifted in will be ignored.

Also communicating using the processors built in shift register will requires that the DI and DO pin the the EEPROM be wired together to form a common DI/O pin. The problem here is that after an EEPROM erase or write operation the DO pin comes out of its high impedance state to indicated the EEPROM's ready/busy status. This status must be cleared and the DO pin returned to high impedance before any additional operations can be sent to the EEPROM. To return the DO pin to its high impedance state, deselect and then reselect the EEPROM to start the erase or write operation, at this time the DO pin will be driven to a logic zero state to indicated a busy status. At this point, all that needs to be done is to stop the SK clock and monitor the DO pin until it indicates a ready state, then clock the status into the DI pin (DI and DO are tied). The DO will return to the high impedance state on the falling edge of the clock. If 8 clocks must be sent at a time due to processor limitation, then when the EEPROM status indicates it is ready shift a byte of zeros to the EEPROM before deselecting it. What really happens here is the processor tries to shift zeros into the EEPROM, however the DO pin indicating ready (logic 1) will hold the DI pin high. After the one is clocked in, the DO pin will return to high impedance and the remainder of the byte from the processor will be clocked into the EEPROM as zeros. Deselect the

6

EEPROM after returning the DO pin to the high impedance state.

An example program has been provided containing all the 8051 routines needed to exercise the CAT93C46, CAT35C102, and CAT35C104. The connection of the memory device to the 8051 is illustrated in Figure 1. In this scheme the EEPROMs CS pin could have been connected to any available I/O line, and the ORG pin would probably be wired to Vcc or GND depending on the application. The DI pin and DO pin of the EEPROM are wired together to form a common DI/O pin, and must be connected (through a current limit resister) to the RxD pin (port 3, pin 0) of the 8051. The clock the the 8051 shift register appears at the TxD pin (port 3, pin 1).

This program utilizes the built in serial port of the 8051 set to the mode 0 configuration. This configuration defines the serial port of the 8051 as an 8 bit shift register which will receive and send data using the RxD pin as data, and the TxD pin as clock. The clock frequency of the shift register is defined as the 8051 oscillator frequency divided by 12, therefore care must be taken not to exceed the maximum SK clock frequency of the EEPROM by adjusting the 8051 oscillator.

The basic flow of the program is illustrated in Figure 2, and a complete assembled listing has also been provided. Subroutines in this program are used to enable the EEPROM for writing, erase the entire EEPROM memory array, and write or read a particular memory address within the EEPROM array.

In this application the 8051 does allow programmer access to the shift register clock pin (port 3 pin 1), therefore with this processor it is not necessary to send 8 additional clocks when only one additional clock is needed.

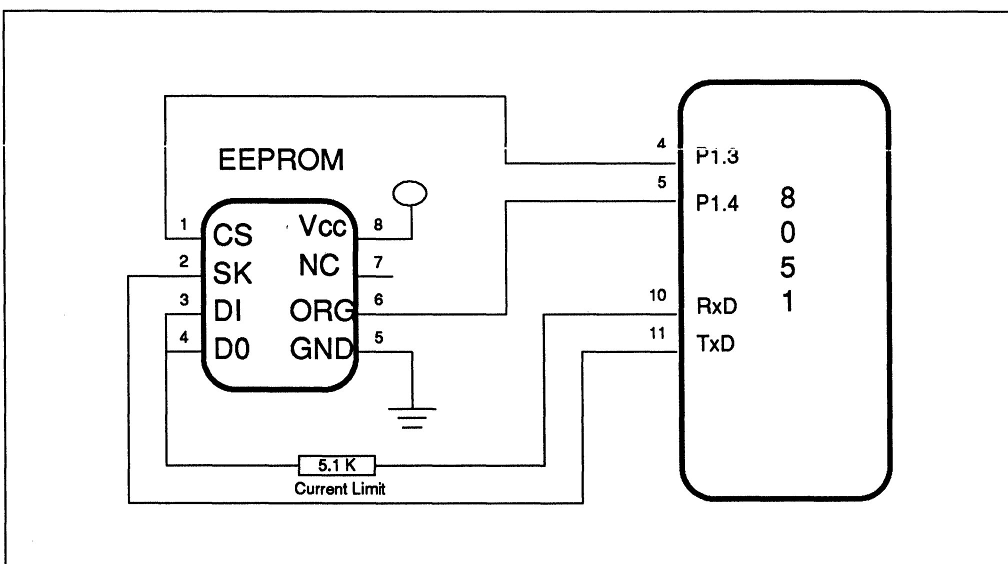


Figure 1.

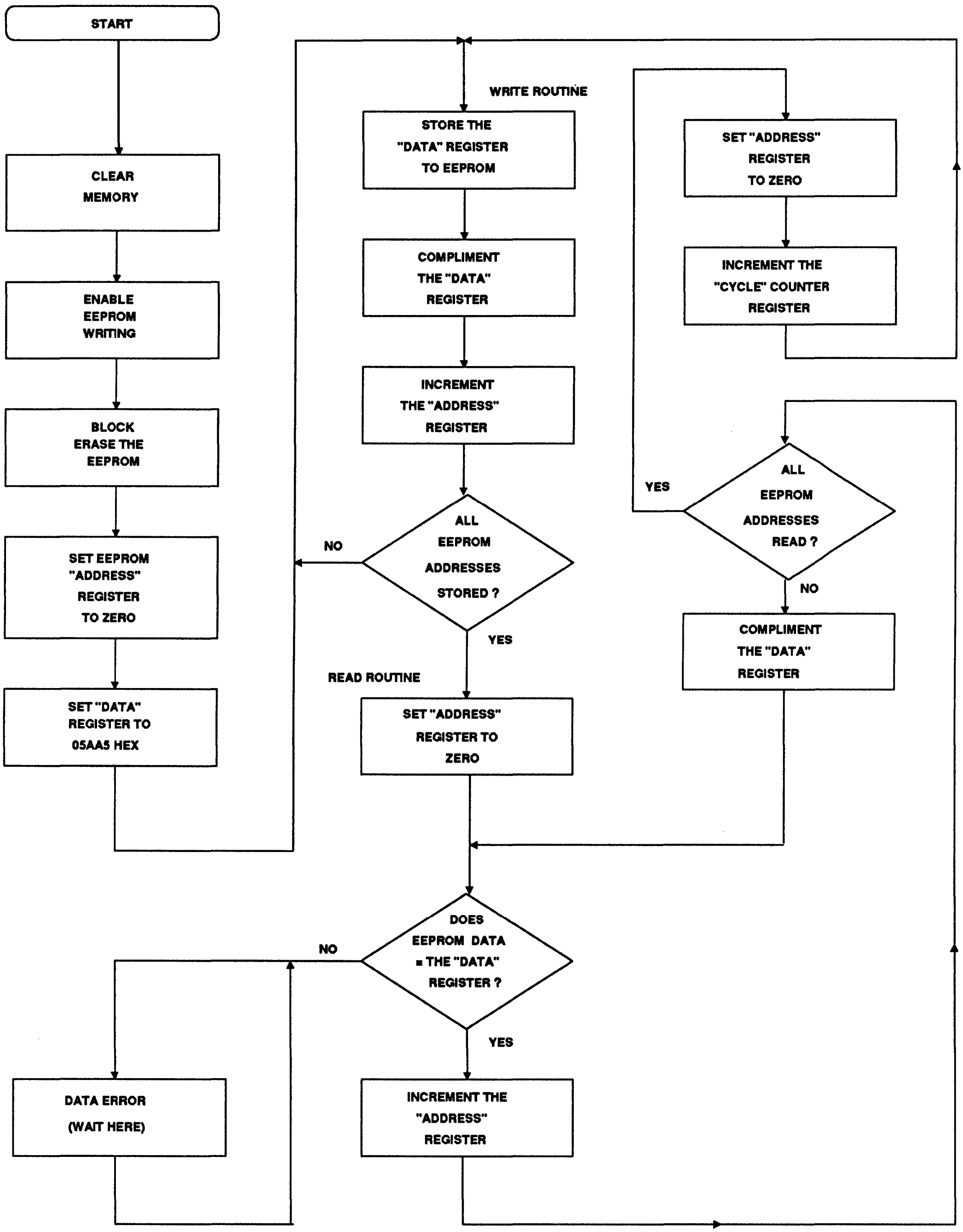

START
CLEAR
MEMORY
ENABLE
EEPROM
WRITING
BLOCK
ERASE THE
EEPROM
SET EEPROM
"ADDRESS"
REGISTER
TO ZERO
SET "DATA"
REGISTER TO
05AA5 HEX
WRITE ROUTINE
STORE THE
"DATA" REGISTER
TO EEPROM
COMPLIMENT
THE "DATA"
REGISTER
INCREMENT
THE "ADDRESS"
REGISTER
ALL
EEPROM
ADDRESSES
STORED ?
NO
YES
READ ROUTINE
SET "ADDRESS"
REGISTER TO
ZERO
SET "ADDRESS"
REGISTER
TO ZERO
INCREMENT THE
"CYCLE" COUNTER
REGISTER
YES
ALL
EEPROM
ADDRESSES
READ ?
NO
COMPLIMENT
THE "DATA"
REGISTER
DOES
EEPROM DATA
= THE "DATA"
REGISTER ?
NO
YES
DATA ERROR
(WAIT HERE)
INCREMENT THE
"ADDRESS"
REGISTER

Figure 2.

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:           PAGE:   1
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT              LINE    STATEMENT                         C46S_16.ASM
                                    ;
                                            $TITLE(CAT EEPROM - 8051 I/O ROUTINES)
                                    ;       Jim Troutner
                                    ;       Catalyst Semiconductor
                                    ;       Date 01/15/88

                                    ;       This routine drives the EEPROM using the 8 bit
                                    ;       shift register (in mode 0) of the 8051.

                                    ;*****************************************************************
                                    ;          8051 Port Assignments
                                    ;*****************************************************************


    00B0                            DATAIO     BIT      P3.0      ;SERIAL DATA INPUT/OUTPUT PIN (RxD)
    00B1                            SCLK       BIT      P3.1      ;SERIAL CLOCK (TxD)
    0093                            EESEL      BIT      P1.3      ;EEPROM CHIP SELECT
    0094                            EEORG      BIT      P1.4      ;EEPROM ORGANIZATION
    00B0                            EESTAT     BIT      P3.0      ;EEPROM STATUS WILL APPEAR HERE

                                    ;*****************************************************************
                                    ;          8051 DATA MEMORY MAP
                                    ;*****************************************************************
----                                         DSEG 0030
                                             ORG      030H
0030                                EE_ADDR:  DS       1         ;EEPROM data address.
0031                                INS_H:    DS       1         ;EEPROM instruction and address.
0032                                INS_L:    DS       1
0033                                DATAH:    DS       1         ;Data to be stored to, or compared
0034                                DATAL:    DS       1         ; to EEPROM data.
0035                                R_DATH:   DS       1         ;Data read from the EEPROM.
0036                                R_DATL:   DS       1
0040                                         ORG      040H
0040                                CYCMAX:   DS       4         ;Number of write/read cycles before
0044                                CYCCNT:   DS       1         ; a failure.

0060                                         ORG      060H
0060                                STACK:    DS       31


                                                $EJECT
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m   ASSEMBLE LIST DATE:         PAGE:   2
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE    STATEMENT                       C46S_16.ASM

                                ;*****************************************************************
                                ;       CONSTANTS
                                ;*****************************************************************


                                ; NOTE: User must enter the number of DATA bits, and  ADDRESS bits
                                ;        required for the EEPROM being tested. This program will
                                ;        automatically adjust the ORG pin of the EEPROM depending
                                ;        on the value entered for D_BITS.
                                ;
                                ;       This program was designed to address the CAT93C46
                                ;        or the CAT35C102 in an 8 bit or 16 bit data organization.
                                ;       It will also address the CAT35C104 in the 16 bit data
                                ;        organization only.
                                ;
                                ;       To modify this program to operate with a specific device
                                ;        such as the CAT93C46, first select the data organization
                                ;        mode desired (8 bits or 16 bits) by changing the D_BITS
                                ;        equate below. Then check the CATALYST DATA BOOK to
                                ;        determine the number of address bits required for that
                                ;        device at that data organization, and change the A_BITS
                                ;        below to the specified number of address bits. i.e  If
                                ;        A_BITS = 6, and D_BITS = 16 then the program is set up
                                ;        for the CAT93C46 in the 64 X 16 mode.
                                ;
                                ;      To run the program simply re-assemble it, load it the
                                ;      emulator, and run it.

 0006                           A_BITS   EQU      6             ;Number of address bit (6,7, or 8).
 0010                           D_BITS   EQU      16            ;Number of data bits (8, or 16).

 0004                           LONG     EQU      A_BITS - 2    ;Number used to adjust long
                                                                ; EEPROM instructions.
 0040                           ADDMAX   EQU   01H SHL A_BITS   ;Max EEPROM address + 1

                                         $EJECT
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   3
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT               LINE    STATEMENT                   C46S_16.ASM

                                ;*****************************************************************
                                ;         EEPROM INSTRUCTIONS
                                ;*****************************************************************
                                                                  ;SHORT INSTRUCTIONS
                                                                  ; 1 START, 2 INSTRUCTION BITS
 0001                           READ_H    EQU      HIGH(110B SHL A_BITS)  ;READ MEMORY @ SPECIFIED ADDRE
 0080                           READ_L    EQU      LOW(110B SHL A_BITS)
 0001                           ERASE_H   EQU      HIGH(111B SHL A_BITS)  ;ERASE CELL @ SPECIFIED ADDRES
 00C0                           ERASE_L   EQU      LOW(111B SHL A_BITS)
 0001                           WRITE_H   EQU      HIGH(101B SHL A_BITS)  ;WRITE DATA TO SPECIFIED ADDRE
 0040                           WRITE_L   EQU      LOW(101B SHL A_BITS)

                                                                  ;LONG BIT INSTRUCTIONS
                                                                  ; 1 START, 4 INSTRUCTION BITS
 0001                           EWEN_H    EQU      HIGH(10011B SHL LONG)  ;ENABLE PROGRAMING
 0030                           EWEN_L    EQU      LOW(10011B SHL LONG)
 0001                           EWDS_H    EQU      HIGH(10000B SHL LONG)  ;DISABLE PROGRAMING (DEFAULT)
 0000                           EWDS_L    EQU      LOW(10000B SHL LONG)
 0001                           ERAL_H    EQU      HIGH(10010B SHL LONG)  ;ERASE ALL ADDRESSES
 0020                           ERAL_L    EQU      LOW(10010B SHL LONG)
 0001                           WRAL_H    EQU      HIGH(10001B SHL LONG)  ;WRITE DATA TO ALL ADDRESSES
 0010                           WRAL_L    EQU      LOW(10001B SHL LONG)

 0001                           TEST_H    EQU      HIGH(06000H SHR A_BITS)
 0080                           TEST_L    EQU      LOW(06000H SHR A_BITS)

                                          $EJECT
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   4
CAT EEPROM - 8051 I/O ROUTINES
LOC. OBJECT              LINE    STATEMENT                       C46S_16.ASM

----                                      CSEG 0000
                                          ORG 0000

                                ;*******************************************************************
                                ;         PROGRAM START
                                ;*******************************************************************

                                START:
0000 02 00 30                             JMP    PSTINT         ;Jump over Interupt routines

0030                                      ORG   0030H

                                PSTINT:                         ;Program starting point
0030 C2 93                                CLR    EESEL          ;Deselect the EEPROM
0032 74 10                                MOV    A,#D_BITS      ;Set the EEPROM ORG pin.
0034 B4 08 02       [0039]                CJNE   A,#8,ORG16
                                ORG8:
0037 C2 94                                CLR    EEORG
                                ORG16:
0039 75 81 60                             MOV    SP,#STACK      ;Stack = 60H -- 7FH
003C E4                                   CLR    A              ;Clear the RAM
003D 78 7F                                MOV    R0,#7FH
                                CLRLOP:
003F F6                                   MOV    @R0,A
0040 D8 FD          [003F]                DJNZ   R0,CLRLOP

0042 11 93          [0093]                ACALL EN_EE           ;Enable the EEPROM for writing
0044 11 C9          [00C9]                ACALL BLKERA          ;Erase the EEPROM

0046 75 34 5A                             MOV    DATAL,#5AH     ;Init the store data registers
0049 75 33 A5                             MOV    DATAH,#0A5H

                                STORE:
004C 11 D6          [00D6]                ACALL EE_STR          ;Store data to the EEPROM

004E 63 34 FF                             XRL    DATAL,#0FFH    ;Complement the data located
0051 63 33 FF                             XRL    DATAH,#0FFH    ; in DATAL and DATAH

0054 11 83          [0083]                ACALL INCADD          ;Increment and test address
0056 50 F4          [004C]                JNC    STORE          ;Not finished store next addr.

                                READ:
0058 31 02          [0102]                ACALL EE_RD           ;Read data from the EEPROM

005A E5 36                                MOV    A,R_DATL       ;Compare the EEPROM read data
005C B5 34 14       [0073]                CJNE   A,DATAL,ERROR
005F 30 94 05       [0067]                JNB    EEORG,DATOK    ;Data ok if in 8 bit mode.
0062 E5 35                                MOV    A,R_DATH
0064 B5 33 0C       [0073]                CJNE   A,DATAH,ERROR
```

6

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:    5
CAT EEPROM - 8051 I/O ROUTINES
LOC. OBJECT               LINE    STATEMENT                            C46S_16.ASM

                                DATOK:
0067 11 83         [0083]                ACALL INCADD
0069 40 0A         [0075]                JC    INCCYC         ;Inc the cycle counter

006B 63 34 FF                            XRL   DATAL,#0FFH    ;Complement the data located
006E 63 33 FF                            XRL   DATAH,#0FFH    ; in DATAL and DATAH

0071 01 58         [0058]                AJMP  READ

                                ERROR:
0073 80 FE         [0073]                SJMP  ERROR          ;Data error,  wait here

                                INCCYC:
                                                              ;Increment the cycle counter
0075 78 44                               MOV   R0,#CYCCNT
0077 D3                                  SETB  C
0078 79 04                               MOV   R1,#(CYCCNT-CYCMAX)
                                NXT:
007A E4                                  CLR   A              ;Each time all the EEPROM addresses
007B 36                                  ADDC  A,@R0          ; are written and then read correctly
007C D4                                  DA    A              ; the register 'CYCCNT' is incremented
007D F6                                  MOV   @R0,A          ; by one. The counter is stored in
007E 18                                  DEC   R0             ; BCD so that it can be read directly
007F D9 F9         [007A]                DJNZ  R1,NXT         ; from data memory as a decimal number.
0081 01 4C         [004C]                AJMP STORE

                                ;*******************************************************************
                                ;        Sobroutine                        " I N C A D D "
                                ;*******************************************************************

                                ; Routine will increment the address located in the EE_ADDR register
                                ; by one. If an overflow occures, the address is set to 000H and
                                ; the routine will return with the carry bit set.

                                ;ENTRY:  EE_ADDR register = data address

                                ;EXIT:   EE_ADDR = New data address
                                ;        IF C = 1, then address was reset
                                ;           C = 0, then increment was OK
                                ;        Registers altered = AC, EE_ADDR, C flag.
                                INCADD:
0083 05 30                               INC   EE_ADDR
0085 E5 30                               MOV   A,EE_ADDR
0087 60 03         [008C]                JZ    OVRFLO
0089 B4 40 05      [0091]                CJNE  A,#ADDMAX,INCOK
                                OVRFLO:
008C 75 30 00                            MOV   EE_ADDR,#0
008F D3                                  SETB  C
0090 22                                  RET
                                INCOK:
0091 C3                                  CLR   C
0092 22                                  RET

                                ;END SUB
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   6
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT                STATEMENT                          C46S_16.ASM

                            ;**********************************************************************
                            ;         Soubroutine                           " E N _ E E "
                            ;**********************************************************************

                            ; Routine will enable the EEPROM for data writing.

                            ;ENTRY:   Nothing required

                            ;EXIT:    Registers altered = INS_H, INS_L, and P1.3

                            EN_EE:
0093 75 31 01                       MOV    INS_H,#EWEN_H       ;Store the Enable EEPROM write
0096 75 32 30                       MOV    INS_L,#EWEN_L       ; instruction to the INS buffer.
0099 11 B7         [00B7]           ACALL  MIRROR              ;Swap the bits within the bytes
                                                               ; to shift out.
009B 11 A0         [00A0]           ACALL OUT16
009D 02 01 18                       JMP    LSTCLK

                            ; END SUB
                            ;**********************************************************************
                            ;         Subroutine                            " O U T 1 6 " , " O U T 8 "
                            ;**********************************************************************

                            ; Routine will shift out the INS buffer to the EEPROM.

                            ;ENTRY:   INS_H and INS_L must contain the EEPROM instruction
                            ;          and address (or data to send to EEPROM).

                            ;EXIT:    Registers altered = P1.3

                            OUT16:
00A0 D2 B1                          SETB   SCLK
00A2 D2 93                          SETB   EESEL               ;Enable the EEPROM.
                            OUT16_2:
00A4 C2 99                          CLR    TI
00A6 85 31 99                       MOV    SBUF,INS_H          ;Shift out first 8 bits.
                            WFRST8:
00A9 30 99 FD      [00A9]           JNB    TI,WFRST8
                            OUT8:                              ;When entering at OUT8, the
                                                               ; EEPROM must already be selected.
00AC C2 99                          CLR    TI
00AE 85 32 99                       MOV    SBUF,INS_L          ;Shift out last 8 bits.
                            WLST8:
00B1 30 99 FD      [00B1]           JNB    TI,WLST8
00B4 C2 99                          CLR    TI
00B6 22                             RET

                            ;END SUB
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   7
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT                   LINE    STATEMENT                         C46S_16.ASM

                                       ;******************************************************************
                                       ;          Subroutine                         " M I R R O R "
                                       ;******************************************************************
                                       ; When shifting data out of the 8051, the data is shifted out LSB
                                       ;  to MSB. When shifting data into the 8051, data is shifted in
                                       ;  MSB to LSB.  These routines were written to represent the
                                       ;  EEPROM Instruction, address, and data in the same manner as
                                       ;  presented the Catalyst data sheet, however this data must
                                       ;  under go a bit swap (i.e. bit7  bit0, bit6  bit1, and so
                                       ;  on) just prior to shifting it out to accommodate the LSB
                                       ;  first output shifting of the 8051.  Since the 8051 will shift
                                       ;  the data in MSB first, no swap is necessary when data is read
                                       ;  from the EEPROM.

                                       ; ENTRY:  INS_H, and INS_L = EPROM instruction plus address, or data

                                       ; EXIT: Both INS_H and INS_L have a MSB to LSB bit swap.
                                       ;        Registers altered = AC, INS_H, INS_L, R1, and C flag.


                                       MIRROR:
00B7 E5 31                                      MOV    A,INS_H
00B9 79 08                                      MOV    R1,#8         ;Set up bit counter
                                       FIN_M:
00BB 13                                         RRC    A             ;Shift INS_H (AC) LSB into the
00BC C5 32                                      XCH    A,INS_L       ; LSB of INS_L while shifting the
00BE 33                                         RLC    A             ; MSB of INS_L into the MSB of
00BF C5 32                                      XCH    A,INS_L       ; INS_H (AC).
00C1 D9 F8         [00BB]                       DJNZ   R1,FIN_M      ;Check the bit counter.
00C3 13                                         RRC    A             ;Shift last bit into INS_L
00C4 C5 32                                      XCH    A,INS_L       ;Store the swapped INS_L to INS_L.
00C6 F5 31                                      MOV    INS_H,A       ;Store the swapped INS_H to INS_H.
00C8 22                                         RET

                                       ; END SUB
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   8
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT               LINE    STATEMENT                         C46S_16.ASM

                                  ;*******************************************************************
                                  ;        Subroutine                        " B L K E R A "
                                  ;*******************************************************************

                                  ; Routine will erase the entire EEPROM memory

                                  ;ENTRY:  Nothing required

                                  ;EXIT:   Registers altered = INS_H, and INS_L

                                  BLKERA:
00C9 75 31 01                              MOV    INS_H,#ERAL_H      ;Store the Erase ALL instruction
00CC 75 32 20                              MOV    INS_L,#ERAL_L      ; to the INS buffer.
00CF 11 B7          [00B7]                 ACALL  MIRROR             ;Swap the bits within the bytes
                                                                     ; to shift out.
00D1 11 A0          [00A0]                 ACALL OUT16
00D3 02 00 EE                              JMP    OUTRET

                                  ;END SUB
                                  ;*******************************************************************
                                  ;        Subroutine                        " E E _ S T R "
                                  ;*******************************************************************

                                  ; Routine will store the data located in DATAH and DATAL into
                                  ;  the EEPROM at the location pointed to by EE_ADDR. In 8 bit
                                  ;  data mode only DATAL will be stored to the EEPROM.

                                  ; NOTE: The EEPROM must be write enabled.

                                  ; ENTRY: EE_ADDR = address in EEPROM to store the data
                                  ;        DATAH, and DATAL = the data to store to EEPROM

                                  ; EXIT:  Registered altered = AC, INS_H, INS_L, and P1.3


                                  EE_STR:
00D6 75 31 01                              MOV    INS_H,#WRITE_H     ;Store the write instruction
00D9 74 40                                 MOV    A,#WRITE_L         ; plus address to the INS
00DB 45 30                                 ORL    A,EE_ADDR          ; register.
00DD F5 32                                 MOV    INS_L,A
00DF 11 B7          [00B7]                 ACALL  MIRROR             ;Swap the bits within the bytes
                                                                     ; to shift out.
00E1 11 A0          [00A0]                 ACALL OUT16               ;Shift out the instruction.
00E3 85 33 31                              MOV    INS_H,DATAH
00E6 85 34 32                              MOV    INS_L,DATAL
00E9 30 94 12       [00FE]                 JNB    EEORG,ONLY8
                                  ALL16:
00EC 11 A4          [00A4]                 ACALL OUT16_2             ;Shift out the DATA.
                                  OUTRET:
00EE C2 B1                                 CLR    SCLK               ;Falling edge of last clock
00F0 C2 93                                 CLR    EESEL              ;Deselect the EEPROM.
```

6

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:         PAGE:    9
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT             LINE    STATEMENT                        C46S_16.ASM

00F2 D2 93                                 SETB  EESEL              ;Check if EEPROM is ready for
                                   WAITRDY:                         ; the next operation.
00F4 30 B0 FD    [00F4]                    JNB   EESTAT,WAITRDY
00F7 D2 B1                                 SETB  SCLK               ;Put DO pin of EEPROM in
00F9 C2 B1                                 CLR   SCLK               ; high Z state.
00FB C2 93                                 CLR   EESEL
00FD 22                                    RET
                                   ONLY8:
00FE 11 AC       [00AC]                    ACALL OUT8
0100 80 EC       [00EE]                    JMP   OUTRET

                                   ;END SUB
                                   ;*******************************************************************
                                   ;           Subroutine                      " E E _ R D "
                                   ;*******************************************************************

                                   ; Routine will read the data located the EEPROM address specified
                                   ;  by EE_ADDR onto registers R_DATH and R_DATL. If in the 8 bit
                                   ;  data mode, data is read into the R_DATL register.

                                   ; ENTRY: EE_ADDR = address in EEPROM to read the data

                                   ; EXIT:  R_DATH, and RDATL = data read from the EEPROM
                                   ;        Registered altered = AC, INS_H, INS_L, R_DATH, R_DATL
                                   ;                             P3.1 and P1.3


                                   EE_RD:
0102 75 31 01                              MOV   INS_H,#READ_H      ;Store the read instruction
0105 74 80                                 MOV   A,#READ_L          ; plus the address to the
0107 45 30                                 ORL   A,EE_ADDR          ; INS register.
0109 F5 32                                 MOV   INS_L,A
010B 11 B7       [00B7]                    ACALL  MIRROR            ;Swap the bits within the bytes
                                                                    ; to shift out.
010D 11 A0       [00A0]                    ACALL OUT16              ;Send the instruction.
010F C2 B1                                 CLR   SCLK               ;Send an extra clock to clear
0111 D2 B1                                 SETB  SCLK               ; the dummy zero from the EEPROM.
0113 30 94 07    [011D]                    JNB   EEORG,I_ONLY8
                                   I_ALL16:
0116 31 21       [0121]                    ACALL IN16               ;Read the data from EEPROM.
                                   LSTCLK:
0118 C2 B1                                 CLR   SCLK               ;Falling edge of last clock
011A C2 93                                 CLR   EESEL              ;Deselect the EEPROM
011C 22                                    RET
                                   I_ONLY8:
011D 31 2B       [012B]                    ACALL IN8
011F 80 F7       [0118]                    JMP   LSTCLK
                                   ;END SUB
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:  10
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT              LINE    STATEMENT                          C46S_16.ASM

                                  ;**********************************************************************
                                  ;         Subroutine                           " I N 1 6 " , " I N 8 "
                                  ;**********************************************************************


                                  ; Routine will shift into the R_DATH, and R_DATL buffer
                                  ; the data from EEPROM. If 8 bit data mode is selected, the
                                  ; data is shifted into R_DATL.

                                  ;ENTRY:  Nothting required

                                  ;EXIT:   R_DATH, and RDATL = EEPROM read data.
                                  ;        Registers altered = R_DATH, and R_DATL

                                  IN16:
0121 C2 98                                CLR     RI                    ;Reset the receive done flag.
0123 D2 9C                                SETB    REN                   ;Enable serial input.
                                  R_W1ST8:
0125 30 98 FD     [0125]                  JNB     RI,R_W1ST8            ;Wait for the first 8 bits.
0128 85 99 35                             MOV     R_DATH,SBUF           ;Store first byte to memory.

                                  IN8:
012B C2 98                                CLR     RI                    ;Reset the receive done flag.
012D D2 9C                                SETB    REN
                                  R_WLST8:
012F 30 98 FD     [012F]                  JNB     RI,R_WLST8            ;Wait for last 8 bits.
0132 85 99 36                             MOV     R_DATL,SBUF           ;Store last byte to memory.
0135 C2 9C                                CLR     REN                   ;Disable serial input.
0137 C2 98                                CLR     RI
0139 22                                   RET

                                  ;END SUB
                                  ;**********************************************************************

                                  END

ASSEMBLY END , ERRORS:0
LAST CODE ADDRESS:0139
```

PACKAGE INFORMATION

GENERAL ORDERING INFORMATION

Prefix	Device #	Suffix
CAT	28C64A	P I -20

Speed (if applicable)

Temperature Range

None = Commercial (0° to 70° C)
I = Industrial (-40° to 85° C)

Package

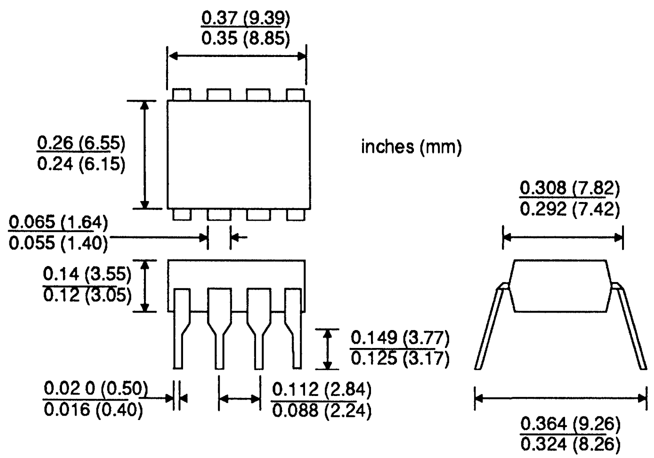
D = CERDIP
K = Small Outline
N = PLCC
P = Plastic DIP

Device part number , may be followed by:

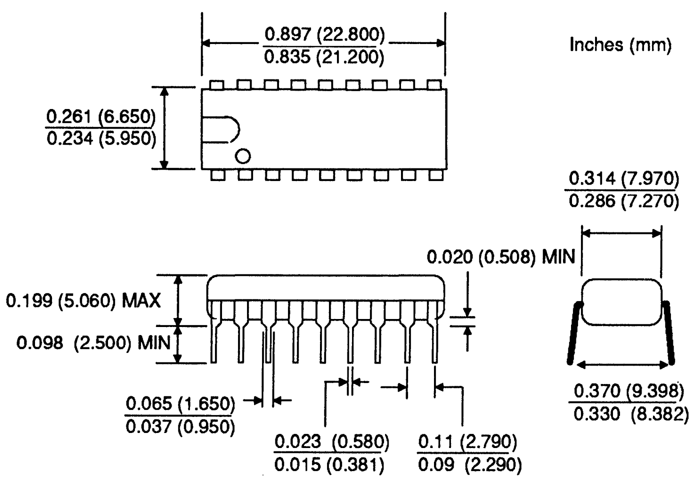
A = Advanced device
L = Low power device

Device used in the example above is a CAT28C64API-20 (Plastic DIP, Industrial temp., 200 ns access time)

8 PIN PLASTIC DIP

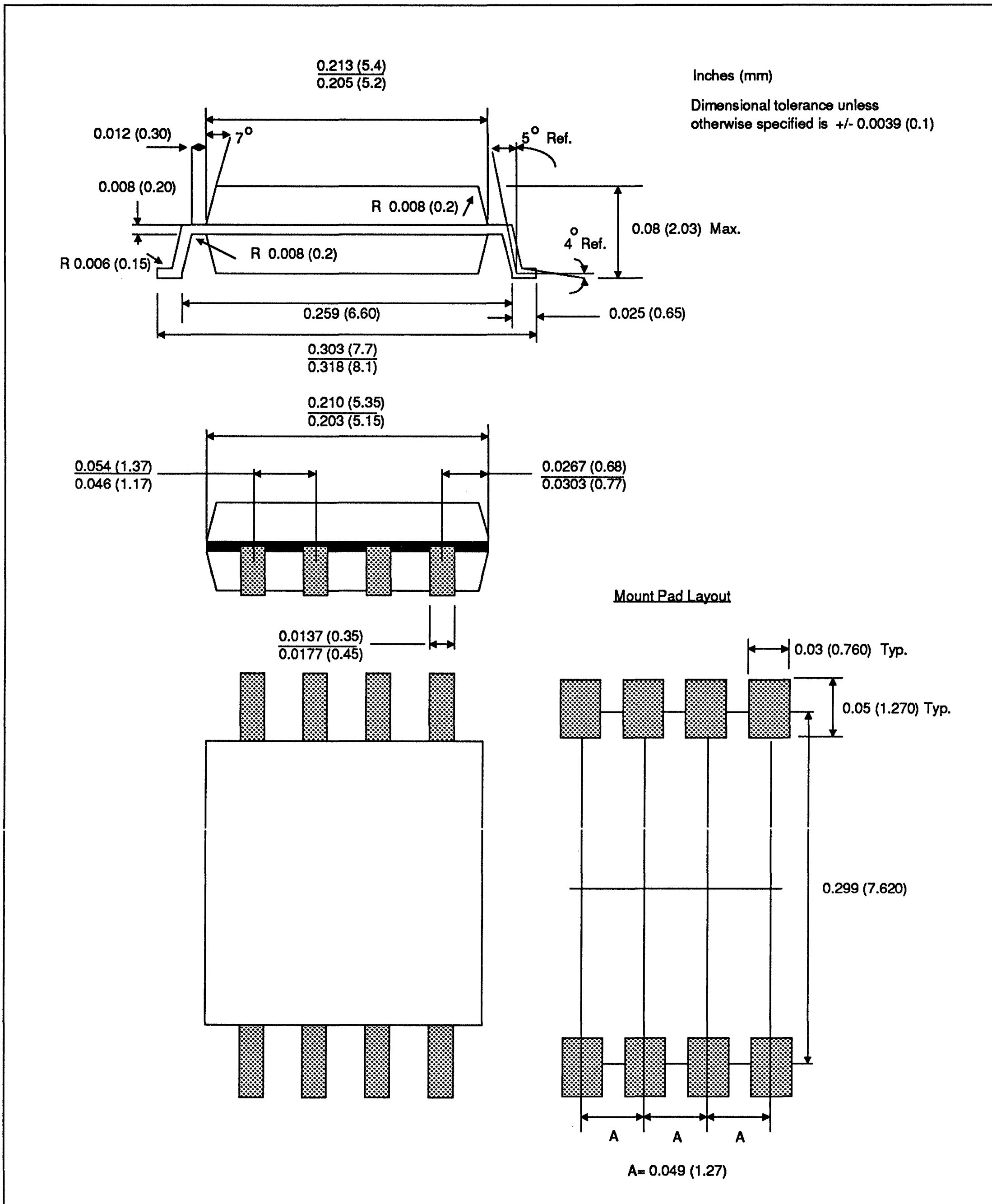


18 PIN PLASTIC DIP

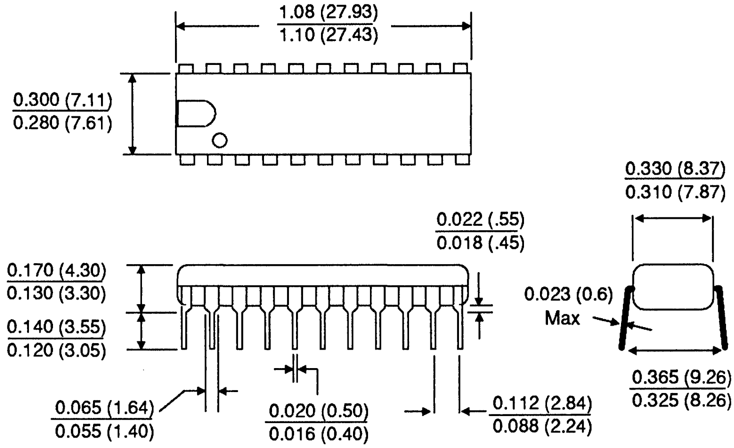


7

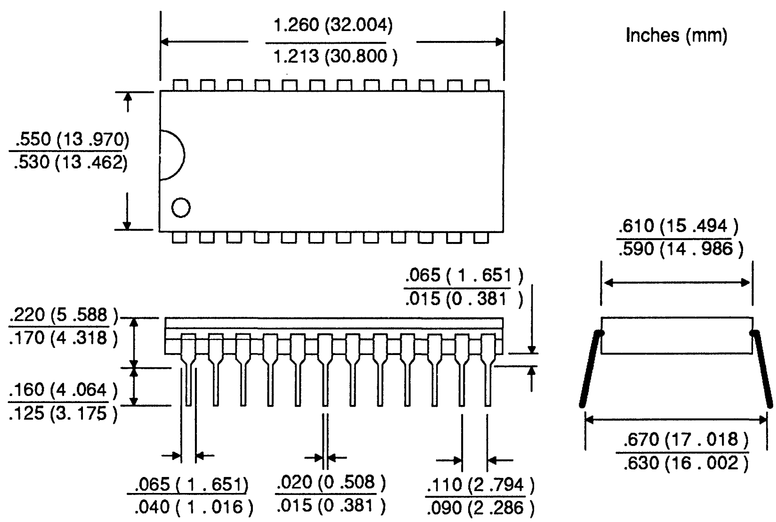
8 PIN S.O. DIP


0.213 (5.4)
0.205 (5.2)
Inches (mm)
Dimensional tolerance unless otherwise specified is +/- 0.0039 (0.1)
0.012 (0.30)
7°
5° Ref.
0.008 (0.20)
R 0.008 (0.2)
0.08 (2.03) Max.
4° Ref.
R 0.006 (0.15)
R 0.008 (0.2)
0.259 (6.60)
0.025 (0.65)
0.303 (7.7)
0.318 (8.1)
0.210 (5.35)
0.203 (5.15)
0.054 (1.37)
0.046 (1.17)
0.0267 (0.68)
0.0303 (0.77)
Mount Pad Layout
0.0137 (0.35)
0.0177 (0.45)
0.03 (0.760) Typ.
0.05 (1.270) Typ.
0.299 (7.620)
A A A
A= 0.049 (1.27)

22 PIN PLASTIC DIP

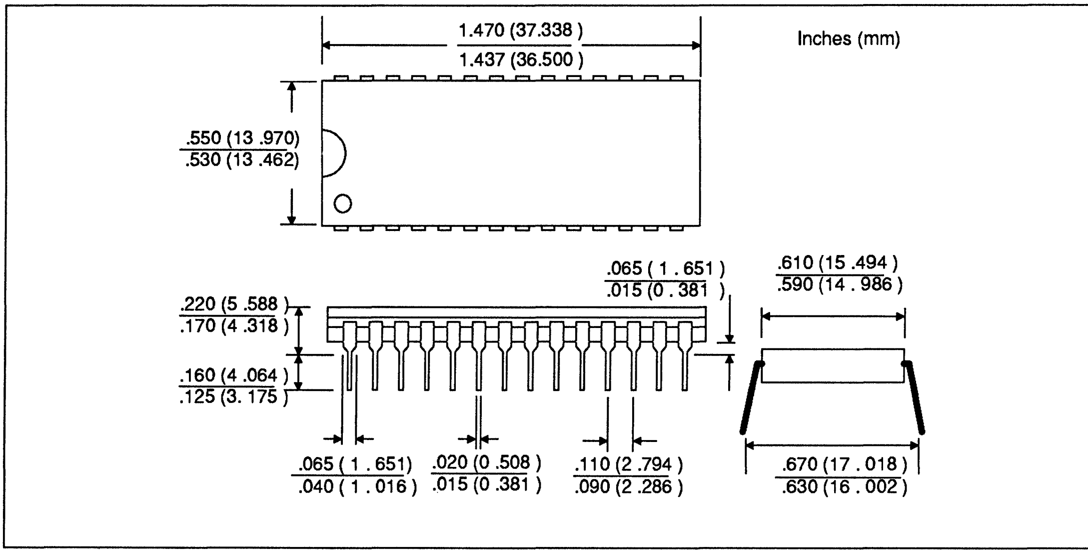


24 PIN PLASTIC DIP

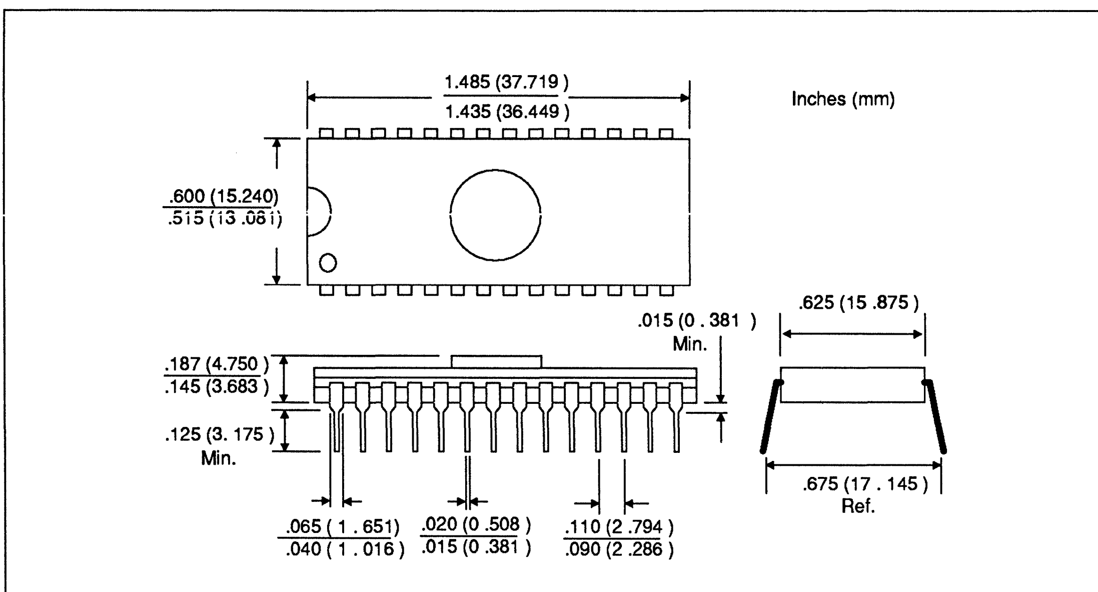


7

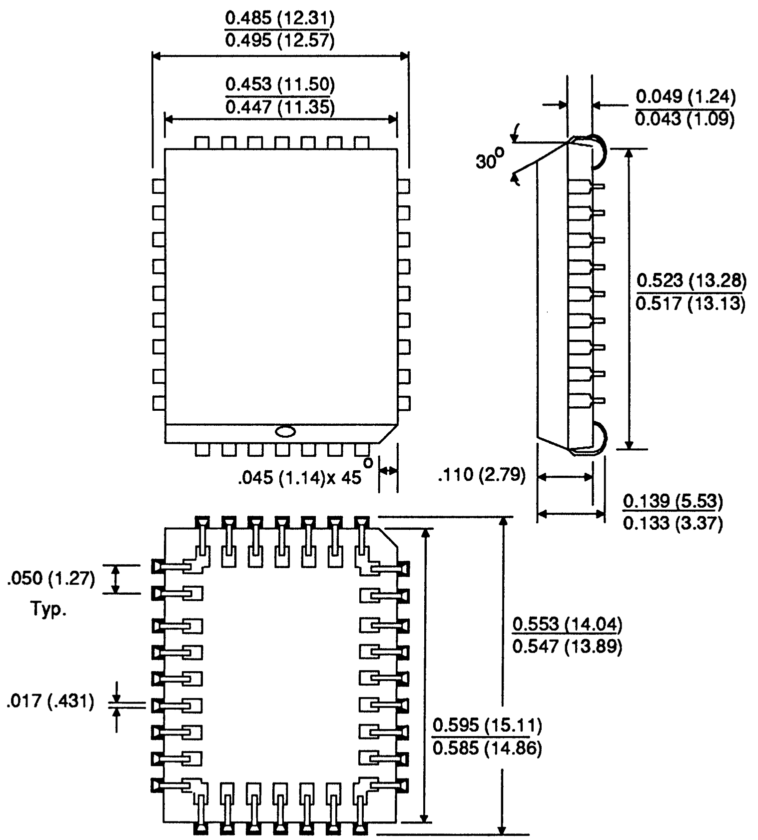
28 PIN PLASTIC DIP



28 PIN CERDIP

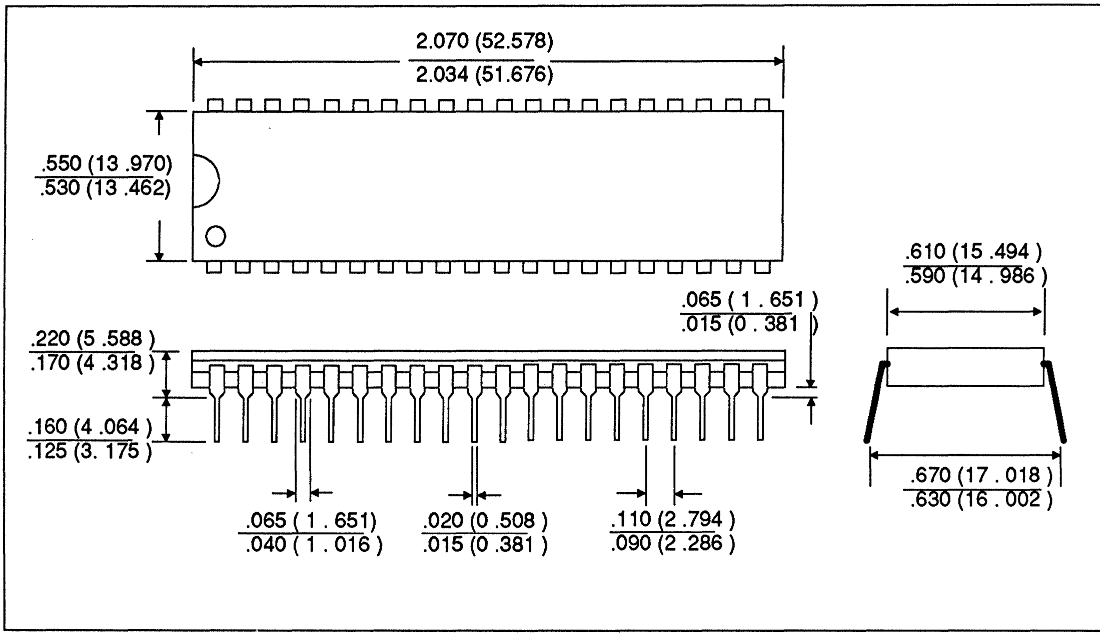


32 PIN PLCC

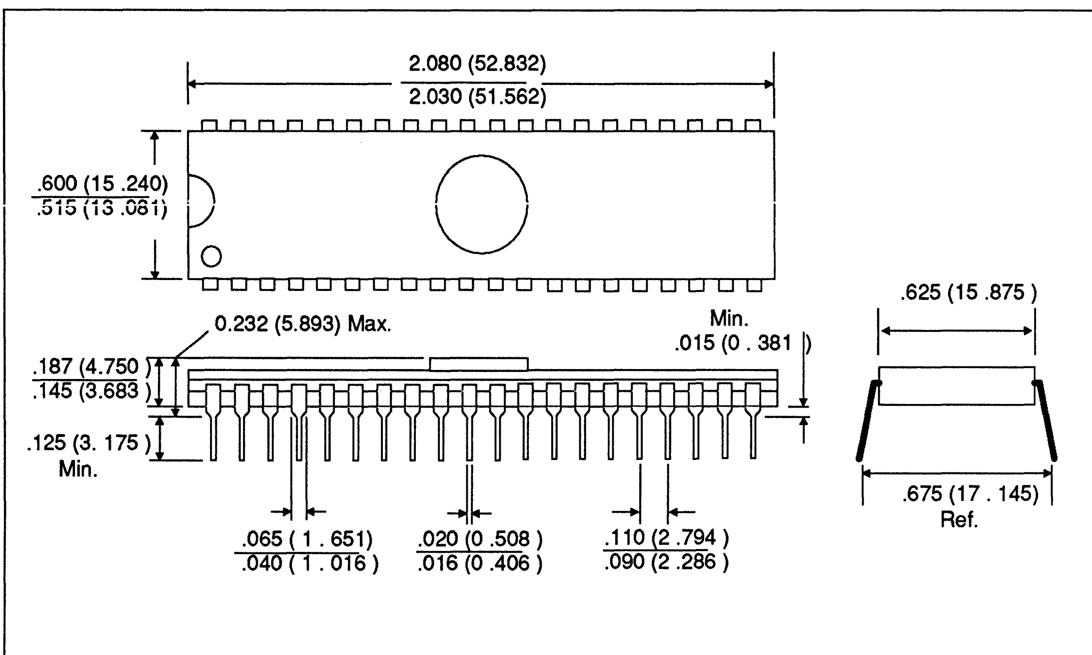

0.485 (12.31)
0.495 (12.57)
0.453 (11.50)
0.447 (11.35)
0.049 (1.24)
0.043 (1.09)
30°
0.523 (13.28)
0.517 (13.13)
.045 (1.14)x 45°
.110 (2.79)
0.139 (5.53)
0.133 (3.37)
.050 (1.27)
Typ.
0.553 (14.04)
0.547 (13.89)
.017 (.431)
0.595 (15.11)
0.585 (14.86)

7

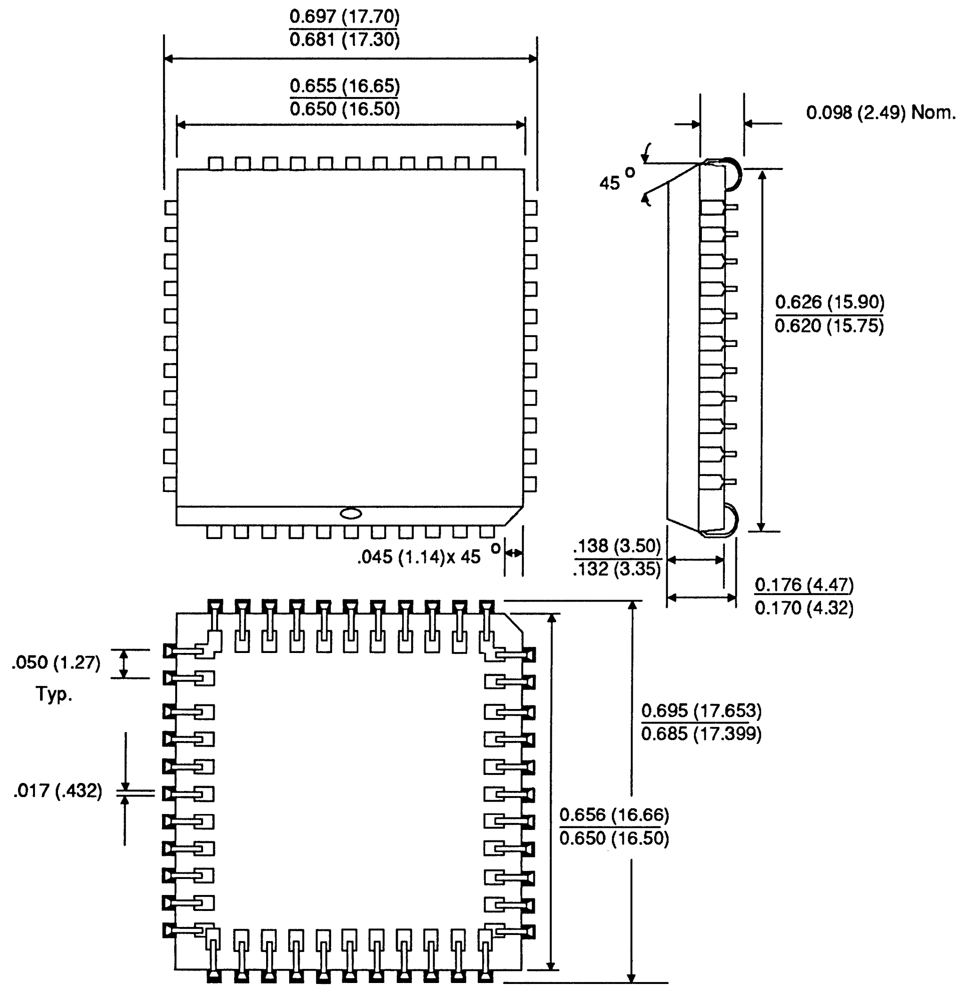
40 PIN PLASTIC DIP



40 PIN CERDIP



44 PIN PLCC


0.697 (17.70)
0.681 (17.30)
0.655 (16.65)
0.650 (16.50)
0.098 (2.49) Nom.
45 °
0.626 (15.90)
0.620 (15.75)
.045 (1.14)x 45 °
.138 (3.50)
.132 (3.35)
0.176 (4.47)
0.170 (4.32)
.050 (1.27)
Typ.
0.695 (17.653)
0.685 (17.399)
.017 (.432)
0.656 (16.66)
0.650 (16.50)

7

DIE PRODUCTS

A number of CATALYST SEMICONDUCTOR's products are available for purchase in die form.

Please contact the factory or your local CATALYST SEMICONDUCTOR, INC. representative for additional information.

CROSS REFERENCE

8

NVRAMS

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	ALTERNATE SOURCE	TECHNOLOGY	PINS
CAT22C10 256-Bit (64x4) Non-Volatile CMOS Static RAM	**CAT22C10**		**CMOS**	**18**
	NCR52210	NCR	SNOS	18
	X2210	XICOR	NMOS	18
CAT22C12 1024-Bit (256X4) Non-Volatile CMOS Static RAM	**CAT22C12**		**CMOS**	**18**
	NCR52212	NCR	SNOS	18
	X2212	XICOR	NMOS	18
CAT24C44 256-Bit (16x16) Non-Volatile Serial CMOS Static RAM	**CAT24C44**		**CMOS**	**8**
	X2444	XICOR	NMOS	8

8

EEPROMS

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	ALTERNATE SOURCE	TECHNOLOGY	PINS
CAT28C16A 2Kx8 CMOS EEPROM	**CAT28C16A**		**CMOS**	**24**
	2816A	INTEL / SEEQ	NMOS	24
	X2816A	XICOR	NMOS	24
	28C16	ATMEL	CMOS	24
	XL2816A	EXEL	NMOS	24
	TS28C16A	THOMSON	CMOS	24
	KM2816A	SAMSUNG	NMOS	24
	NMC2816	NATIONAL	NMOS	24
	M2816	SGS	NMOS	24
	MSM2816A	OKI	NMOS	24
	R2816A	ROCKWELL	NMOS	24
CAT28C17A 2Kx8 CMOS EEPROM	**CAT28C17A**		**CMOS**	**28**
	2817A	INTEL / SEEQ	NMOS	28
	28C17	ATMEL	CMOS	28
	AM2817A	AMD	NMOS	28
	TS28C17A	THOMSON	CMOS	28
	KM2817A	SAMSUNG	NMOS	28
CAT28C64A 8Kx8 CMOS EEPROM	**CAT28C64A**		**CMOS**	**28**
	2864	INTEL	HMOS	28
	X2864A	XICOR	NMOS	28
	28C64A	ATMEL	CMOS	28
	2864A	SEEQ	NMOS	28
	AM2864A	AMD	NMOS	28
	XL2864A	EXEL	NMOS	28
	MSM2864A	OKI	NMOS	28
	HN58064	HITACHI	NMOS	28

EEPROMS

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	ALTERNATE SOURCE	TECHNOLOGY	PINS
CAT93C46 (1) 1K-Bit Serial EEPROM	**CAT93C46**		**CMOS**	**8**
	NMC9346/COP495	NATIONAL	NMOS	8
	93C46	ICT	CMOS	8
	HY93C46	HYUNDAI	CMOS	8
	MSM16811	OKI (1)	CMOS	8
	TS93C46	THOMSON (1)	CMOS	8
	SC22011	SIERRA	CMOS	8
	NCR59308	NCR	SNOS	8
CAT59C11A 1K-Bit Serial EEPROM	**CAT59C11A**		**CMOS**	**8**
	ER5911	GI	SNOS	8
	MSM16911	OKI (1)	CMOS	8
	TS59C11	THOMSON (1)	CMOS	8
CAT35C102 (2) 2K-Bit Serial EEPROM	**CAT35C102**		**CMOS**	**8**
CAT35C202 (2) 2K Bit Serial EEPROM	**CAT35C202**		**CMOS**	**8**
	ER5912	GI (2)	SNOS	8

(1) User selectable organization: 64x16 or 128x8
(2) User selectable organization: 128x16 or 256x8

8

ONE-TIME PROGRAMMABLE EPROMS

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	ALTERNATE SOURCE	TECHNOLOGY	PINS
CAT2764A 8Kx8 EPROM VPP = 12.5V	**CAT2764A**		**NMOS**	**28**
	P2764A	INTEL	NMOS	28
	AM2764A	AMD	NMOS	28
	TMS27P64	TI	NMOS	28
	MSM2764	OKI	NMOS	28
	μPD2764	NEC	NMOS	28
	TMM2764	TOSHIBA	NMOS	28
CAT27128A 16Kx8 EPROM VPP = 12.5V	**CAT27128A**		**NMOS**	**28**
	P27128A	INTEL	NMOS	28
	AM27128A	AMD	NMOS	28
	MSM27128	OKI	NMOS	28
	μPD27128	NEC	NMOS	28
CAT27256 32Kx8 EPROM VPP = 12.5V	**CAT27256**		**NMOS**	**28**
	P27257	INTEL	NMOS	28
	AM27256	AMD	NMOS	28
	MSM27256	OKI	NMOS	28
CAT27512 64Kx8 EPROM VPP = 12.5V	**CAT27512**		**NMOS**	**28**
	AM27512	AMD	NMOS	28
	MSM27512	OKI	NMOS	28

SRAMS

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	ALTERNATE SOURCE	TECHNOLOGY	PINS
CAT71C88 16Kx4 CMOS FAST Static RAM	**CAT71C88**		**CMOS**	**22**
	MSM5188US	OKI	CMOS	22
	AM99C164	AMD	CMOS	22
	CY7C164	CYPRESS	CMOS	22
	IMS1620	INMOS	CMOS	22
	SR64K4	LATTICE	CMOS	22
	MCM6288	MOTOROLA	CMOS	22
	µPD4362	NEC	CMOS	22
	IDT7188	IDT	CMOS	22
	VT64KS4	VTI	CMOS	22
CAT71C256 32Kx8 CMOS Static RAM	**CAT71C256**		**CMOS**	**28**
	MSM51257RS/RJ	OKI	CMOS	28
	HM62256	HITACHI	CMOS	28
	MB84256	FUJITSU	CMOS	28
	TC53257	TOSHIBA	CMOS	28
	M5M5256	MITSUBISHI	MixMOS	28
CAT71C256L 32Kx8 CMOS Static RAM	**CAT71C256L**		**CMOS**	**28**
	MSM51257LRS/JS	OKI	CMOS	28
	HM62256	HITACHI	CMOS	28
	MB84256	FUJITSU	CMOS	28
	TC53257	TOSHIBA	CMOS	28
	M5M5256	MITSUBISHI	MixMOS	28

ARTICLE REPRINTS

HOW LINEAR IC DESIGNERS ARE BUILDING DENSER CHIPS/67

EXECUTIVE OUTLOOK: NO SLOWDOWN IN TECHNOLOGY/86

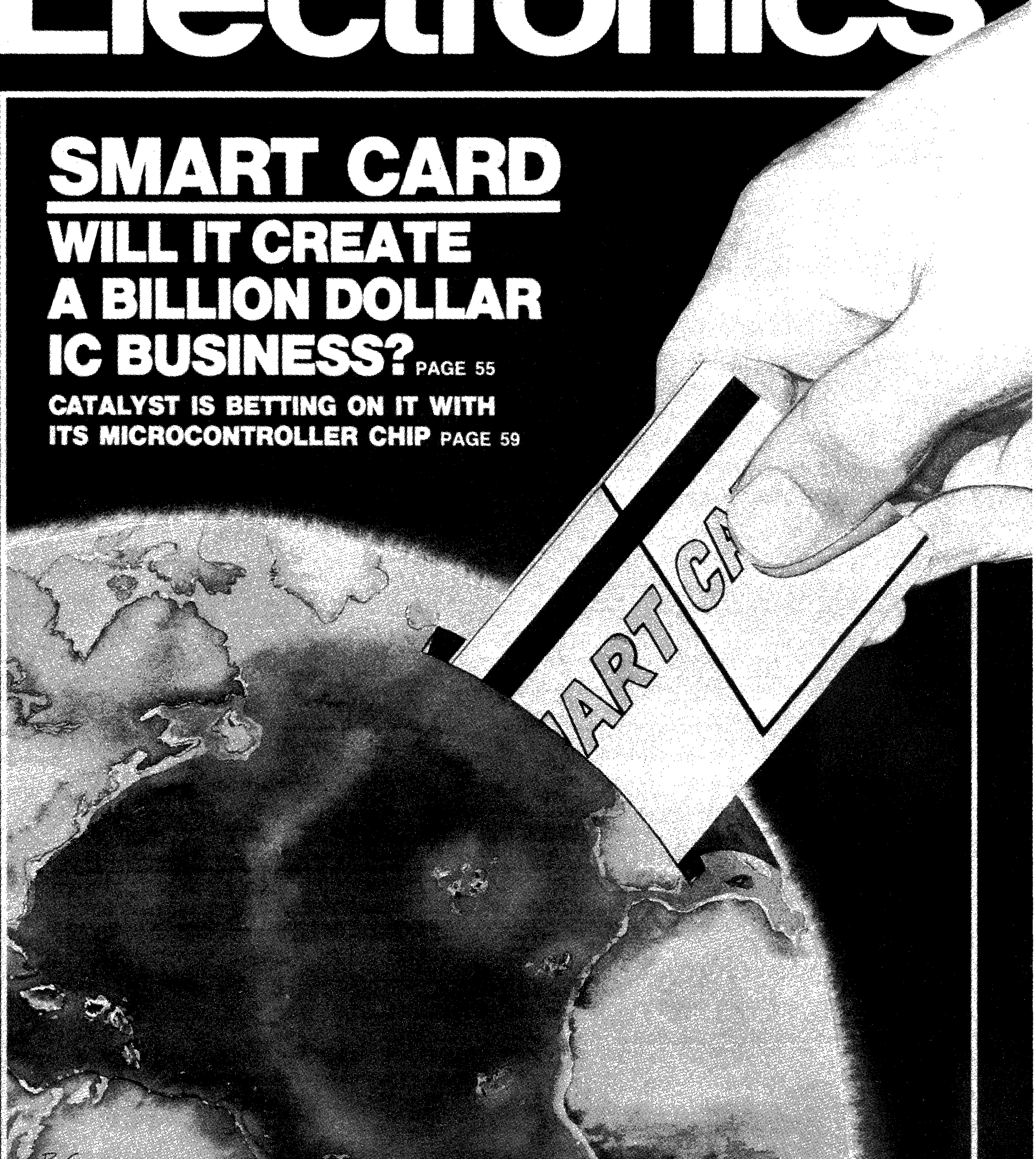
DECEMBER 18, 1986

Electronics®

SMART CARD

WILL IT CREATE A BILLION DOLLAR IC BUSINESS? PAGE 55

CATALYST IS BETTING ON IT WITH ITS MICROCONTROLLER CHIP PAGE 59



DOES CATALYST HAVE THE KEY TO SMART CARDS?

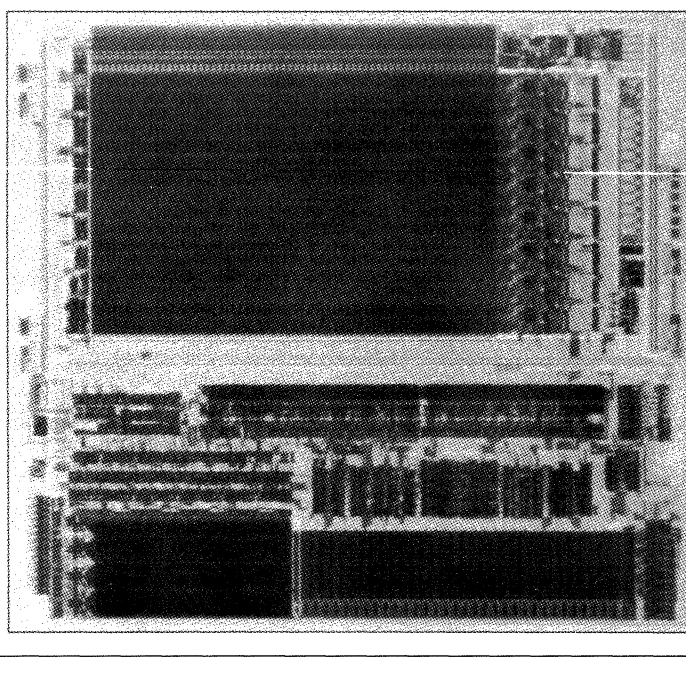
Catalyst Semiconductor thinks that its new chip, which meets ISO smart-card standards and has 2-K bytes of EEPROM, could finally open up the market

A tiny but powerful microcontroller from Catalyst Semiconductor Inc. may be the key that will unlock a worldwide billion-dollar business in smart-card chips. Measuring 4.5 by 5 mils by only 200 μm thick, the CAT61C580 chip is small enough to meet size requirements set by the International Organization for Standardization for smart-card applications, yet it packs 2-K bytes of electrically erasable, programmable read-only memory. That's at least four times the EEPROM of any other ISO-compliant smart-card chip now available using the same 2-μm CMOS design rules.

The Santa Clara, Calif., company achieved this density by stripping away the peripheral logic around the EEPROM and writing these functions into microcode. That left plenty of room for the 2-K bytes of EEPROM, and the chip is still about 30% smaller than competing devices that have only a fourth or less memory. What's more, Catalyst is working on an 8-K-byte chip, which will be made by shrinking the current 220-μm^2 EEPROM cell size to 80 μm^2 with a combination of proprietary design refinements and 1.5-μm geometries. The CAT61C580 is just being released; the 8-K-byte chip should be available next year.

Working in conjunction with joint developer Oki Electric Co., Tokyo, Catalyst designers modified an Oki microcontroller by adding a programmable logic array and 2-K bytes of EEPROM. (Fig. 1). They also managed to squeeze in 3-K bytes of ROM, 128 bytes of random-access memory, and enough electrostatic-discharge-protection circuitry to protect the chip from up to 15,000 kV, enough to protect against the static electricity generated by removing a credit card from a pocket or a billfold.

In addition, the CAT61C580 op-



1. LITTLE GIANT. Catalyst's 8-bit microcontroller is tiny enough for use in smart cards, yet it has an elephant's memory.

erates at the ISO-recommended frequency of 4.9 MHz with a high-speed instruction-cycle time of 813.8 ns, allowing it to run at the ISO's recommended 9,600 baud through a single serial input/output pin. Power dissipation of the 8-bit chip is only 20 mW.

The architecture of the chip allows asynchronous, two-way communications through a single serial I/O pin. This eliminates the need for a universal asynchronous receiver/transmitter and an interrupt, reducing the number of pins to only five—one third to one half of what's required in other approaches.

A TANTALIZING IDEA

The idea of EEPROM-based microcontrollers has long captured designers' imaginations because of the wide range of applications—not only for smart cards, but also for robotics, artificial intelligence, industrial controls, consumer products, and more. But so far, applications have been limited to a small number of niche markets for controllers, because of the small amount of EEPROM that could economically share the same chip as the microcontroller. Smart cards are one application that promises to allow EEPROM-based microcontrollers to break out of their niche; now that such a powerful chip that meets ISO smart-card standards exists, that breakout could be imminent. And with the increased memory that is promised, the chips will have a crack at the full range of potential microcontroller markets.

Catalyst president and founder B. K. Marya claims his is the only chip that meets, and in some cases exceeds, all of the ISO requirements for smart-card applications, including area, thickness, electrostatic discharge, power dissipation, and speed. Of these, the first three are the most critical, he says.

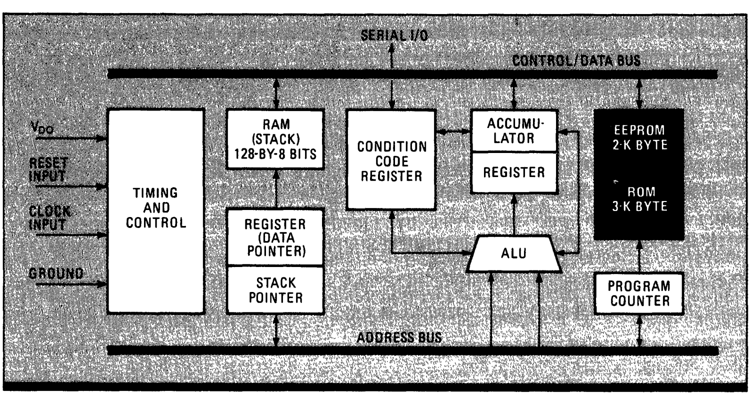
"The thickness must be no more than that of a standard credit card, 200 μm. And the area must not only be 5 by 5 mils or less, but [the chip must] be as square as possible, to prevent the possibility of breakage when the card is bent. In addition, the chip must be capable of withstanding the electrostatic discharge that builds up taking credit cards in and out of pockets and wallets." This buildup has been measured in excess of 10 kV, he says.

The 2-K-byte chip is aimed at a projected near-term market for smart cards that some estimate to be worth hundreds of millions of dollars (see p. 55). In a typical smart-card transaction, a card holder puts the card in a point-of-sale terminal. The terminal supplies the card with electric power and communicates to the card's microcontroller through pin contacts on the card's surface. The user is asked to enter a password. When the sale is rung up, the amount of the transaction is stored in the card's EEPROM, credited to the retailer's account, and debited from the card holder's credit balance, which is also stored in the card's memory. The card holder can replenish the credit balance at an automatic-banking machine.

What has held back the development of the EEPROM-based microcontroller market, Marya says, is the fact that, although stand-alone EEPROM parts of 16-K, 64-K, and 256-K densities are becoming commonplace, EEPROM-based microcontroller densities have trailed the stand-alone densities by at least four generations.

One way to achieve more on-board EEPROM is to advance the processing state of the art: scaling down the lateral dimensions from geometries between 2 and 3 μm to between 1.25 and 1.5 μm, and the vertical dimensions on the EEPROM from 150 to 250 Å down to 80 to 90 Å, which comes close to the limits at which EEPROMs operate reliably. The problem with this, says Marya, is that it requires manufacturers to push the process technology for microcontrollers beyond what is currently available even for stand-alone EEPROMs. And although such an advance is technically feasible for the high-volume applications that could use such large EEPROM/microcontroller combinations, the high cost of manufacturing such devices rules out their use. Marya says there is also the problem of reliability, which is critical for smart cards, where data integrity and security are important. So to make room for more EEPROM, Catalyst replaced the peripheral-function circuitry with microcode.

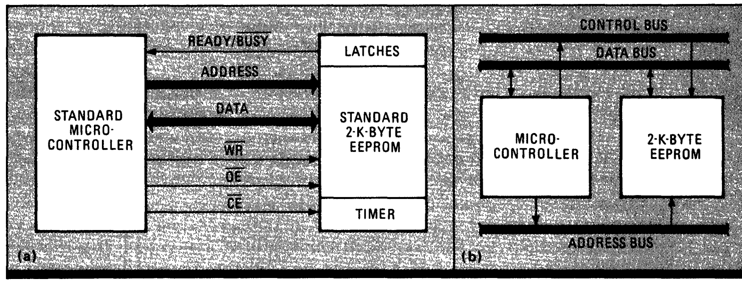
To get 2-K bytes of EEPROM into an ISO-standard smart-card chip, says Marya, "what is required is a fundamental rethinking of the architecture of EEPROM-based microcon-



2. ATTRACTIVE SWAP. By writing the latch, timer, and test logic functions into microcode, Catalyst designers were able to free up more than enough room on the chip for 2-K bytes of EEPROM.

trollers. Basically, most current implementations are 'brute-force' affairs combining the functions of an EEPROM and a microcontroller on the same chip, without any modification whatsoever."

By writing the functions of the EEPROM's peripheral logic into microcode, Catalyst has freed up real estate for more EEPROM. "Essentially, we have taken a standard EEPROM device, stripped off such peripheral circuitry as the latches, timers, and self-test logic, and incorporated these functions into the microcode of the on-board 8-bit microcontroller (Fig. 2), resulting in a 5-by-4.5-mm die size," says Marya. To achieve these breakthroughs, Catalyst designers came up with an architecture that differs from standard single-chip EEPROM/CPU implementations in five fundamental ways.



3. SIMPLIFIED BUS. By eliminating latches, timers, and test logic, the complex bus structure of a standard EEPROM-based chip (a) is replaced with a simpler three-bus arrangement (b).

First, even though it uses the same 200- to 250-μm^2 cell structure as the CPU, the 2-K-byte EEPROM takes up only half the area of the microcontroller. Second, the microcontroller's microcode has been expanded to include the latch, timing, and test functions usually associated with the operation of the EEPROM. Although this increases the area occupied by the microcode by 5%, eliminating the peripherals from the EEPROM circuitry saves 20% of the EEPROM's space.

Third, the bus architecture has been simplified. In the traditional one- and two-chip approach (Fig. 3a), at least six separate data, address, and control lines link the EEPROM and the CPU. Moreover, Marya says, the user has to provide necessary waveforms on control pins WE, OE, and CE, along with the valid data and address. The completion of programming is signaled via the RDY/BUSY pin, which has to be monitored by the microcontroller. In the CAT61C580, the interface between the CPU and the EEPROM is reduced to a three-bus structure (Fig. 3b), because the EEPROM's hard-wired latches and timer are eliminated. In addition, testing of the EEPROM is done internally, eliminating the need for test pads.

Fourth, the addressing scheme has been modified, says Marya, in that the EEPROM is above the ROM address space but, unlike the ROM, it is addressed through RAM. The addressing scheme is made efficient by eliminating page boundaries and providing both direct and indirect addressing of the RAM.

Finally, two additional registers have been added to the basic architecture: a B register to enhance the arithmetic logic unit's computation-intensive tasks, and a D register, which can be auto-incremented or -decremented to enhance the speed of the RAM's read and write operations. The 128-by-8-bit RAM provides 32 levels of nesting, and it can be used as a stack for pop and push operations.

WHAT'S IN THE MICROCODE

Most of the read, write, and erase functions are performed using two simple move commands incorporated into the CPU's microcode, MOV_1 and MOV_2. The first command transfers data from the internal RAM to the EEPROM, erasing previous data after receiving the appropriate 24-bit security code. The second command reads data out of the EEPROM locations and into the RAM. With these commands, EEPROM programming is made totally transparent to the user. "This transparency adds an additional level of security and reliability, since, unlike other implementations, the actual mechanism of writing into EEPROM is never revealed to the user," says Marya.

In addition to these special instructions, there are the 95 other housekeeping commands usually incorporated into a microcontroller: 55 one-byte instructions, 35 two-byte instructions, and 5 three-byte instructions. However, the instructions have been modified to reflect the chip's use in smart-card applications. The large number and smaller width of instructions provide more programming power to the user, and that's important in smart cards, where programming space is limited to on-board ROM, says Marya.

Security is also essential for smart-card applications, because the user stores important financial and personal information in the card's EEPROM. So Catalyst designers incorporated a set of special instructions into the microcode and a program into the on-board ROM that allows a three-level security scheme. "In a credit card application, this would make it possible not only for the primary user, say the financial institution, such as MasterCard or Visa, to have an access code, but the issuing bank and the individual card user as well—the first incorporated into the nonerasable ROM when the chip is sold to the issuing institution, and the other two inserted into the EEPROM when the card is issued to a customer," says Marya. "In any transaction, all three codes must be matched before any information is revealed to the user or any data is changed on the card—the first two between the card and the machine automatically, and the third by the user on request."

The high voltage for erasing and programming the EEPROM cell is generated on the CAT61C580, so the chip needs only a single power supply of 5 V. Fabricated with a 2-μm EEPROM process, which combines a 2-μm CMOS logic process with a conventional high-voltage two-transistor, floating-gate tunnel-oxide EEPROM process, the chip's EEPROM is specified for 10,000 program-erase cycles and 10 years of data retention. The process uses dual oxides—a thin oxide to obtain high-speed EEPROM read capability and a thicker oxide to withstand the 21 V required for erasing and programming the cell.

In this scheme, Marya says, the user can change his code at regular intervals, as can the issuing institution via the automatic teller machine. Also, the card-reading machine can be programmed to disqualify the card after a certain number of unsuccessful attempts to enter the code. In addition, he says, further levels of security can be incorporated into the EEPROM, such as specifying several individuals who are authorized to use the card, and their credit limits.

Catalyst is evaluating a number of strategies to take advantage of planned second-generation improvements. First, implementing the 2-K-byte architecture in 1.5-μm CMOS and using the 80-μm^2 cell that is now under development will reduce the die size of 2-K-byte devices by as much as 50%, while increasing the number of dice per wafer and lowering the cost of the finished devices. Alternatively, the same process improvements will allow an increase in EEPROM array capacity from 2-K bytes to 8-K bytes without substantially increasing the present die size. Finally, Marya says, the enhancements will allow fabrication of 16-bit microcontrollers with as much as 32-K bytes of EEPROM, opening a host of application areas that require real-time response, such as artificial intelligence, robotics, and high-performance industrial and military controllers. □

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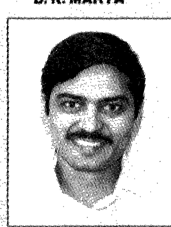
MARYA: THE MICROCONTROLLER COULD BE THE NEXT GREAT 'GIZMO'

"For years the semiconductor industry has been looking for the electronic gizmo that would approach the dollar and unit volumes that digital watches, calculators, and video games generated," says Bharat Kumar Marya—"B. K." to his friends and associates. The president and founder of Catalyst Semiconductor Inc., Santa Clara, Calif., believes that smart cards are just the tip of the iceberg in a market for nonvolatile memory-based microcontrollers that he thinks may reach $2 billion a year by the mid-1990s.

Marya, 38, thinks that many observers expect growth to come from the wrong places. "Almost everyone has turned their eyes toward personal computers and work stations, which have quickly moved from 8 to 16 to 32 bits," he says. But as explosive as that market was at its beginning, it has begun to level off in terms of growth and penetration. Moreover, he says, the largest share of the profits went to original-equipment manufacturers and system integrators, not to chip manufacturers.

"The only market that has a good chance of recreating the bonanza of dollars and unit volumes of the past is the market for smart integrated-circuit cards built around EEPROM-based, 8-bit microcontrollers," says Marya, who points out that there are some 200 million banking and credit cards in circulation. He projects that by 1990 about 25% of these cards will be integrated-circuit-based. Beyond this, he says, there are other potentially huge replacement markets, such as telephone credit cards, as well as new applications, such as health-history cards, warranty cards, security cards, military dog tags, welfare cards, and passport cards.

B. K. MARYA



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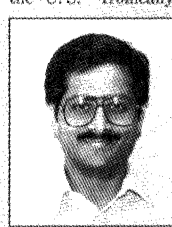


NAGESH CHALLA

Although many of these potential IC-card applications are already being test-marketed in Europe and Japan, Marya says, the major market will ultimately be the U. S. "Ironically, virtually no U. S. semiconductor company, with the exception of some tentative efforts on the part of Motorola, is taking steps to participate in this market," he says. "U. S. companies must act fast, or we'll lose another major market."

To enter Catalyst in this market sweepstakes, Barya set up a joint development agreement with Oki Electric Co., Tokyo, 18 months ago. "We provided the basic architecture modifications, the circuit design, and the EEPROM expertise," he says. "They provided the process and fabrication capability."

Maintaining communications and schedules for the joint project required many transoceanic flights by Marya, design manager Nagesh Challa, Catalyst senior design manager Samir Patel, and Tomoaki Yoshida, an Oki section manager in Japan.

Catalyst is Marya's second startup. His first, Exel Semiconductor, an EEPROM and EPROM manufacturer, was acquired this year by Exar Inc. Marya earned a BSEE from Punjab University, India, and an MSEE from the University of New Mexico. He has since directed the design, construction, and operation of fabrication lines at several companies, including Hewlett-Packard, National Semiconductor, Synertek, and Seeq Technology.

A NEW KIND OF SCOPE FOR WIDEBAND TESTS/72
TI MOVES TRENCH ETCHING INTO THE FACTORY/75

MIDYEAR MARKET REPORT PAGE 44

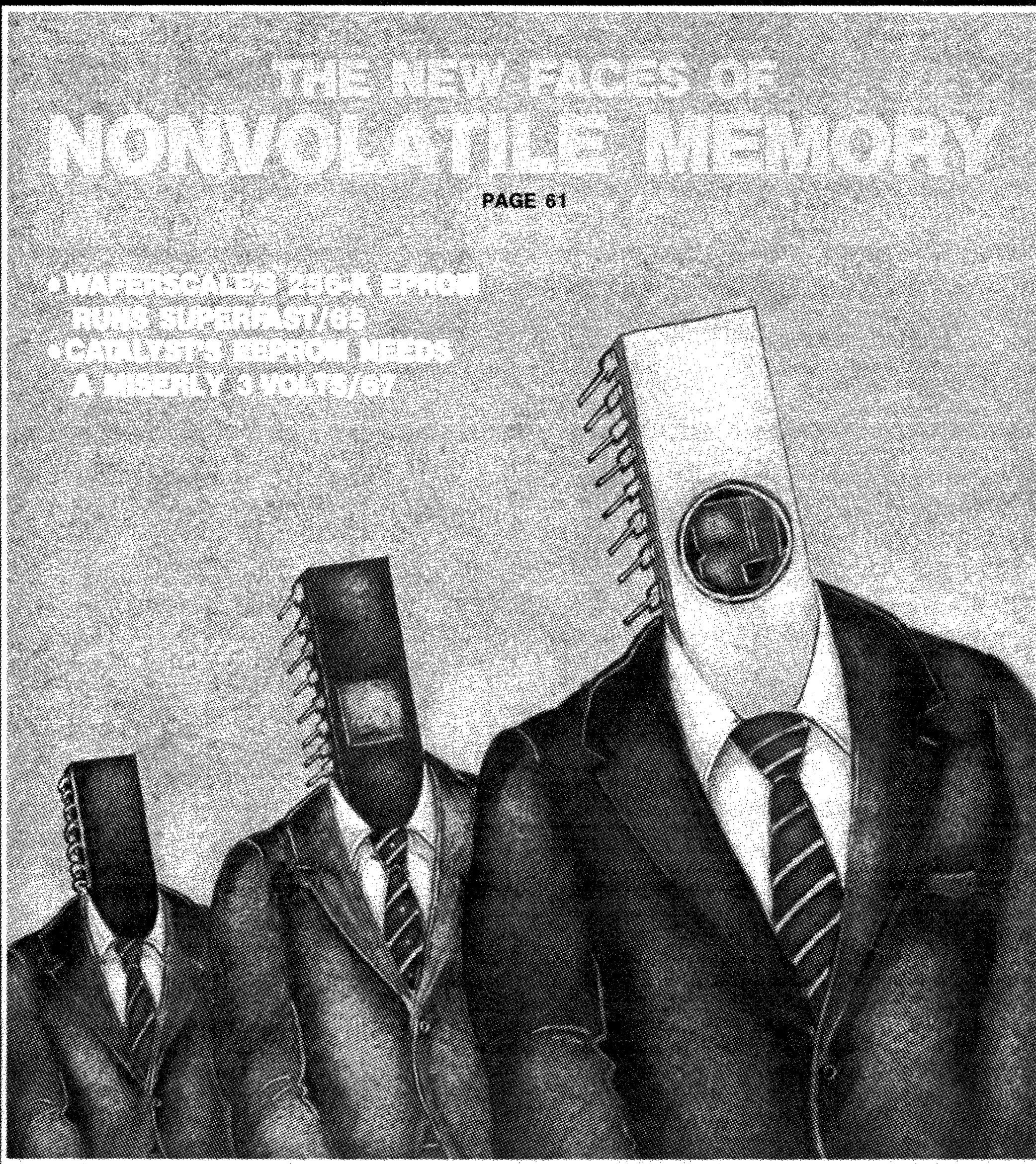
JULY 9, 1987

Electronics®

THE NEW FACES OF NONVOLATILE MEMORY

PAGE 61

- WAFERSCALE'S 256-K EPROM RUNS SUPERFAST/65
- CATALYST'S EEPROM NEEDS A MISERLY 3 VOLTS/67



THE CHANGING FACE OF NONVOLATILE MEMORIES

Faster, denser EPROMs and EEPROMs are finding new uses, displacing big ROMs and fast PROMs, for example; big chunks of them can also be added to ASICs

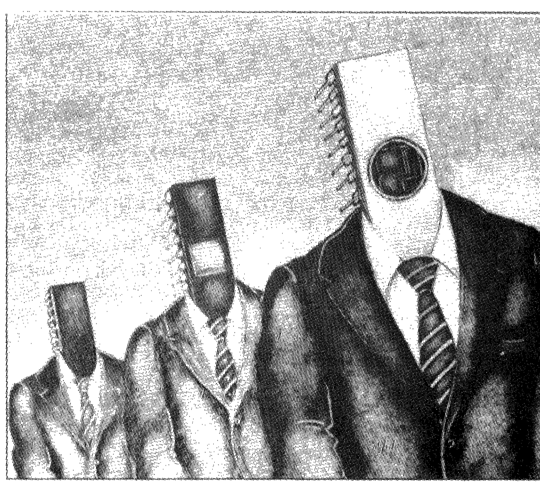
by Bernard C. Cole

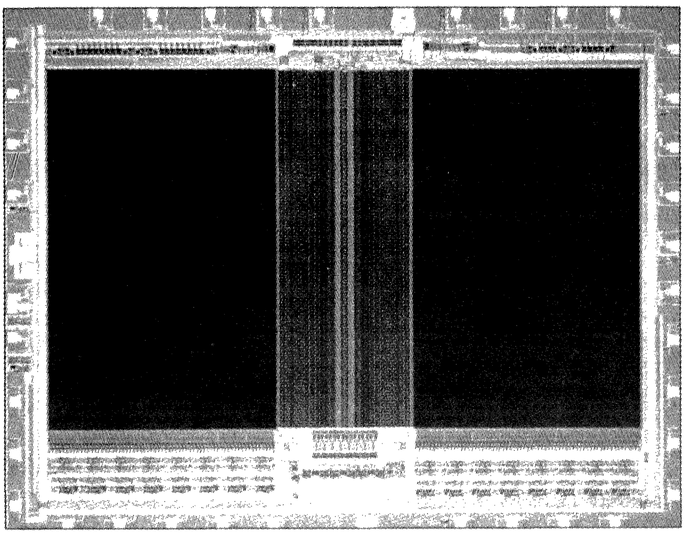
Nonvolatile memories are taking on a whole new look. As both erasable programmable read-only memories and electrically erasable PROMs get faster and denser, they are starting to displace high-density ROMs and high-speed PROMs in new applications. In current applications, nonvolatile memory will now take up significantly less board space. Higher densities also will make it easier to incorporate larger amounts of nonvolatile memory on other types of chips, opening the door to logic chips that integrate large arrays of EPROM and EEPROM.

A new generation of higher-density commodity parts is under development, while lower-density parts are being pushed to significantly faster access times. Moreover, the need for designers to choose between speed and density may disappear, as companies such as WaferScale Integration Inc. in Fremont, Calif., (see p. 65) develop parts that combine both features.

Beyond making improvements to conventional parts, a drive is under way among chip makers to develop memories tailored to specific market segments—markets where speed is paramount, or power requirements are important, for instance. An example of the latter is a 64-Kbit EEPROM that needs only 3 V, reducing backup battery requirements in lightweight portable equipment. The part was jointly developed by Catalyst Semiconductor Inc. of Santa Clara, Calif., and Oki Semiconductor Corp. of Tokyo (see p. 67). In addition, companies are looking to incorporate nonvolatile-memory technology into other non-memory chips, applying their expertise to a variety of logic circuits—including microcontrollers, digital signal processors, programmable logic, and even application-specific integrated circuits based on standard cells.

One reason for all the activity in nonvolatile-memory product development is today's healthy market. The current crop of EPROM and EEPROM products are chalking up very strong sales—so strong that cautious manufacturers are reluctant to believe the optimistic projections of future business, says Victor deDios, senior industry analyst at Dataquest Inc. of San Jose, Calif. Overall, he says, worldwide EPROM sales for 1987 can be expected to hit $1 billion, up 8% from $910 million in 1986 and up 14% from the reces-





1. FAST EPROM. A 64-K-by-16-bit EPROM developed jointly by Catalyst Semiconductor and Oki Semiconductor boasts a 150-ns access time.

sionary dip to $876 million in 1985. Next year, says deDios, with projected sales up 20% to $1.2 billion, they will again equal the sales for 1984, the industry's high point to date. Prospects are even brighter in EEPROMs. DeDios estimates that sales for 1987 will reach $231 million, up 61% from the $139 million in 1986. In 1988, he expects sales to grow by about 50% to $345 million.

And while the markets are taking off, somewhat surprisingly, Japanese makers of EPROM and EEPROM aren't keeping pace with the exploding market growth. They will slip from a market share of 15% to 20% in 1986 to less than 5% this year. To be sure, most U. S. manufacturers regard the Japanese slippage as temporary. Therefore, they're in a hurry to develop products that will put them in a strong position for both commodity parts and in high-return specialty niches when competition heats up again as the Japanese charge back into the marketplace.

For now, strong sales and the drop in Japanese competition is causing a period of price stability. And most EPROM manufacturers are using the resulting higher profits to fund more development work on CMOS processes that will take them to higher densities, higher speeds, and lower power, says deDios. The market is moving away from 64-Kbit EPROMs and toward 256-Kbit and 512-Kbit devices, says Dave Bostwick, director of strategic development for the memory group at Advanced Micro Devices Inc., Sunnyvale, Calif. Also entering the market in volume production are 1-Mbit EPROMs from AMD, Fujitsu, Hitachi, Intel, and Toshiba. One of the most recent arrivals on the 1-Mbit EPROM scene is the CAT27C210, a 64-K-by-16-bit CMOS device jointly developed by Catalyst and Oki (see fig. 1). Pin-for-pin compatible with Intel's 27210, it features 150-ns access times, an active power figure of only 150 mA, and a standby power of 500 μA.

One indicator of things to come is a 4-Mbit EPROM under development at Toshiba. Built using a 0.8-μm CMOS process, it incorporates a basic cell measuring only 9 μm^2, matching that of many single-transistor dynamic random-access memory cells. The 8-bit-wide device features a high cell current of about 10 μA, resulting in a low typical access time of 120 ns.

Access times are also being reduced in current lower-density EPROMs—from an average of 200 to 350 ns down to 150 to 200 ns, says Alan Ankerbrand, director of MOS memory marketing at National Semiconductor. And within a year, he says, speeds will edge downward even more, to about 100 to 150 ns. Dataquest's deDios agrees: "By this time next year anything under 512 Kbits in density with access times of more than 150 ns will be out of the mainstream."

In traditional full-function EEPROMs based on the Fowler-Nordheim effect, says deDios, the majority of the marketplace is moving from 64 Kbits to 256 Kbits. Most authorities agree current technology stops there, however: "Unless a radically new cell structure and architecture comes along, it will be difficult for EEPROMs to move beyond 256 Kbits," says Ian Wilson, director of product marketing at SGS Semiconductor Corp. U. S., in Phoenix, Ariz.

An alternative technology that many firms are looking at to break beyond 256 Kbits is "flash" architecture, so named because the contents of all the memory's array cells are erased simultaneously by a single field emission of electrons from the floating gate of an erase gate. Such an EEPROM combines the advantages of the ultraviolet-light-erasable PROM and floating-gate EEPROMs. It unites the high density, small size, low cost, and hot-electron-write capability of an EPROM with the easy erasability, on-board reprogrammability, high endurance, and cold-electron-tunnelling erasure of floating-gate EEPROMs.

So far, the only player in the flash EEPROM market is Seeq Technology Inc., San Jose, Calif., which introduced its first device, the 128-Kbit 48128, in August 1986. It is now following up this initial n-MOS part with two higher-density 1.5-μm CMOS parts, the 512-Kbit 48C512 and the 1-Mbit 48C1024, both with 8-bit-wide organizations. With a memory-cell size of only 20 μm^2—about one quarter the size of current EEPROM cells—these parts achieve EPROM die sizes, says

Mike Villott, vice president of marketing at Seeq, and they provide EEPROM features previously not available. Such features include on-chip address and data input latches to permit microprocessor-compatible write and erase cycles, as well as chip-erase and page-erase modes.

And whereas the 48128 required a 21-V power supply on multiple pins, the new flash EEPROMs require only a single 12-V external supply for programming and erasure. Moreover, he says, this programming voltage can be applied during read operations, which eliminates the need to switch it off when not erasing or programming. Byte write time is only 1 ms, and chip and byte erase times are no more than 5 s. Endurance—the number of times the device can be erased and written to—is 100 cycles minimum and can be screened to 1,000 cycles.

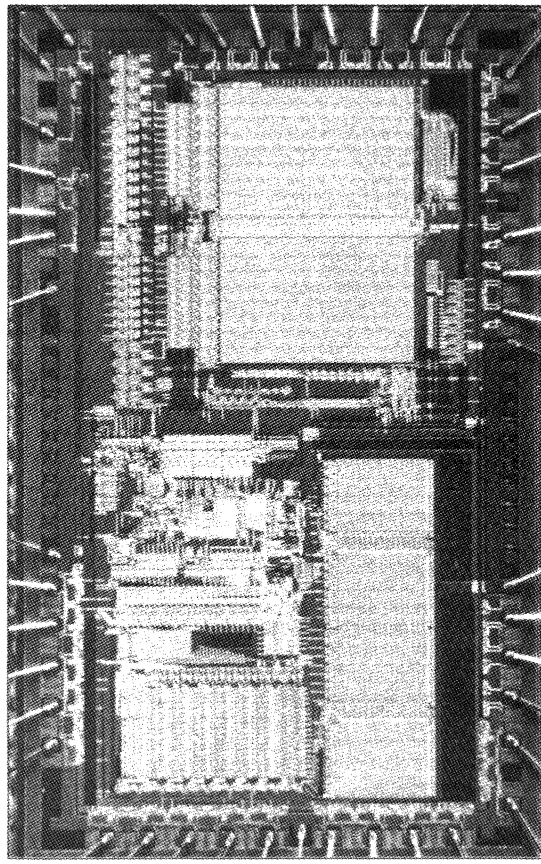
Hoping to follow Seeq into the market with a high-density flash EEPROM is Exel Microelectronics of San Jose, Calif., which is in development on a 512-Kbit device it expects to introduce early next year. Also investigating the technology as a way to achieve higher EEPROM densities are AMD, Fujitsu, Hitachi, National Semiconductor, Texas Instruments, and Toshiba.

Another recent convert appears to be Intel Corp., Santa Clara, Calif., although until recently it was enthusiastically exploring another approach to high-density EEPROMs, the thick-oxide technique pioneered by Xicor Inc. of San Jose, Calif. Intel, however, has abandoned its efforts in this area, says Don Knowlton, general manager of Intel's programmable-memory operations in Folsom, Calif., and is investigating other techniques for higher density, including the flash-EEPROM approach.

That leaves Xicor going it alone with the thick-oxide technique. The company is now in production with a 256-Kbit n-MOS device, the X28256 [*Electronics,* May 12, 1986, p. 30] and is also developing a CMOS version, the X28C256, which it expects to introduce later this year, and a 1-Mbit device tentatively scheduled for early next year.

For many manufacturers, however, the bright prospects in the mainstream EPROM and EEPROM market are essentially an opportunity to carve out new niches. The past has taught them a painful lesson: the memories may be nonvolatile, but their market is not. They want to find areas where price pressure and competition are less intense. Among the possibilities they're exploring are high-speed bipolar PROM replacements, parts tailored to specific applications such as smart cards, and other applications outside the traditional domain of EPROMs and EEPROMs.

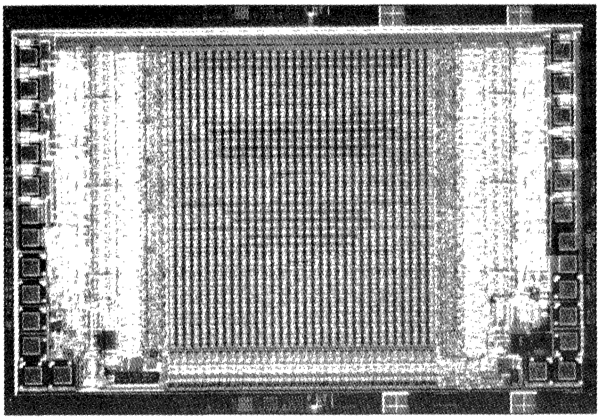
Two companies that have successfully established themselves in the bipolar PROM replacement market are Cypress Semiconductor Inc. of San Jose, Calif., and WaferScale Integration, with 16-Kbit and 64-Kbit CMOS EPROMs in the 35-to-50-ns range. Also looking to participate is Seeq, which has just introduced two byte-wide



2. REPROGRAMMABLE DSP. General Instrument has put 2.5 Kbytes of EEPROM on a digital signal processor chip.

35-ns EEPROMs, the 16-Kbit bit 36C16 and the 32-Kbit 36C32 [*Electronics,* April 30, 1987, p. 66]. Others thinking hard about entering the market include AMD, Intel, and SGS.

Another niche is being explored by Intel, which is looking at what Knowlton calls "application-oriented" EPROMs—nonvolatile memory devices with extra logic that optimizes the devices for specific applications. One of the company's first efforts in this direction was the 27916 KEPROM, or keyed-access EPROM, which combines the memory array with a pseudo-random number generator and encryption circuitry that can determine if the person accessing its contents is authorized. Taking the concept even further, the company this month introduced the first in a new series of such applications-oriented EPROMs, the 87C257 and 68C257—256-Kbit devices with on-chip latches that allow the memory's address and data pins to be tied directly to a microcontroller's multiplexed address and data



3. ERASIC. Exel's 78C800 is the first in a family of what it calls electrically reprogrammable ASICs, made with EEPROM technology.

pins. The two devices, intended for the 8051/8096 and 6800 series of microcontrollers, respectively, eliminate the need for the external logic, such as latches and inverters, that is typically required in microcontroller-based systems, says Tom Price, EPROM marketing manager.

Japanese firms seem to be carving out a niche for themselves in extremely high-density EEPROMs and EPROMs of more than 1 Mbit, for use in smart cards and memory cards. Estimated to be a billion-dollar market by the early 1990s [*Electronics,* Dec. 18, 1986, p. 55], smart cards will require high levels of built-in microcontroller intelligence, as well as memory that is both dense and nonvolatile. The only direct U. S. competitor to the Japanese in the EEPROM- and EPROM-based smart- and memory-card market is General Instrument Microelectronics, Chandler, Ariz. Besides planning to produce EPROMs and EEPROMs ranging from 256 Kbits to 1 Mbit over the next six months, the company has installed the equipment to make the smart cards themselves, as well as card readers, power supplies, and connectors. Also making efforts in this direction are Texas Instruments Inc. and Motorola Inc., but only at the chip level. The fourth contender in this arena is the team of Catalyst Semiconductor Inc. and Oki Semiconductor, which aims to produce controllers and EEPROMs.

Another strategy EPROM and EEPROM companies are following is diversification outside traditional stand-alone products. They are applying their improved nonvolatile technology to microcontrollers, DSPs, field-programmable logic, and even standard-cell ASICs.

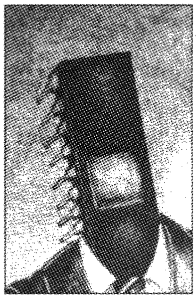
Traditionally, small amounts of EPROM or EEPROM—usually no more than 1,024 bits—have been incorporated into microcontrollers to give users some reprogrammability. "With new advances in nonvolatile memory technology, much higher levels can be incorporated," says B. K. Marya, president of Catalyst Semiconductor. In the new generation of devices from AMD, Catalyst, Intel, SGS, and Xicor, on-chip nonvolatile memory has risen to 32 Kbits or 64 Kbits.

On-chip nonvolatile memory is also being used on DSPs. One such device is the DSP320EE12 from General Instrument, a pin-for-pin compatible version of TI's TMS320C10 DSP chip, but with 2.5 Kbytes of EEPROM added (see fig. 2). In the very near future, says Marya, it should be possible to incorporate up to 256 Kbits onto the microcontroller chip.

In programmable logic devices, two nonvolatile memory vendors—Intel and the Exel subsidiary of Exar Corp., San Jose, Calif.—have already entered the market. A third, Seeq, has just entered into a technology exchange agreement with Monolithic Memories Inc., which dominates the field-programmable array-logic market with its bipolar devices.

Just entering the market this month with a PLD product based on its EEPROM technology is Exel, with the first in a family of what it calls ERASICs, or electrically reprogrammable ASICs. Designated the 78C800 (see fig. 3), it is the first commercially available CMOS PLD offering a single-plane folded-NOR architecture, says Narayan Purohit, Exel product marketing manager. This approach makes it possible to implement multilevel logic designs and does away with the limitations of the traditional AND/OR-based designs now used. Intel's first proprietary PLD is an EPROM-based programmable bus-interface controller designated the 5CBIC. A programmable three-port transceiver with embedded programmable logic macrocells and cross-point signal routing, it allows designers to implement any of a number of different bus interfaces with a single circuit. A third company, WaferScale Integration, is working with Altera Corp. of Santa Clara, Calif., a manufacturer of EPROM-based PLDs, on a new family of user-configurable microsequencers based on its proprietary high-speed split-gate technology [*Electronics,* March 19, 1987, p. 76].

On the standard-cell side, at least two nonvolatile-memory companies—WaferScale and Exel—are in the market with cell libraries that incorporate EPROM and EEPROM cells, respectively. Similar efforts are under way at Intel and National Semiconductor, among other companies. In the Exar effort, Exel's EEPROM technology has been incorporated in standard cells ranging from a single bit to arrays of 1 Kbits. The same family of products also includes a wide range of analog megacells, including analog-to-digital and digital-to-analog converters and a variety of switched-capacitor filters. At WaferScale, engineers are upgrading an already existing EPROM-based cell library with cells that incorporate the company's newest and fastest EPROM technology. □



CATALYST'S EEPROM NEEDS A MISERLY 3 VOLTS

Five volts is no longer the magic number when engineers talk portable and battery-backed applications. Catalyst Semiconductor Inc. of Santa Clara, Calif., has just put the finishing touches on a 64-Kbit EEPROM that reads and writes with a supply voltage as low as 3 V. And this diminutive appetite comes at no substantial cost in speed. With an access time of 120 ns, the memory keeps pace with many existing 5-V devices. When operated at 5 V, its reads take a mere 60 ns. Also in its favor is the fact that it draws an active current of only 7.5 mA at 8 MHz, about a fifth that of its rivals.

Low voltage opens up a wide range of battery-backed applications, says B. K. Marya, Catalyst's founder and president—among them, hand-held computers, smart cards, pagers, beepers, and many telecommunications devices, which require long-term battery backup as well as small size.

The memory also will compete with nonvolatile static random-access memories that incorporate a 3-V lithium battery. "The advantage of battery-powered nonvolatile SRAMs is their ability to read and write data with access times of 120 ns or less," Marya points out. Moreover, "traditional high-density EEPROMs of 64 Kbits or more usually require at least a 5-V read and write voltage. And they are not only slow but also difficult to operate if reprogramming is necessary, requiring as they do at least four AA-type batteries or an expensive lithium power source." Because it can be operated and programmed with a 3-V supply, the device requires only two 1.5-V batteries in portable consumer settings and makes it possible to go with small lithium power sources in smart cards. Eventually, Marya says, as the power-supply requirements of EEPROMs continue to decline, it may be possible to substitute solar cells for batteries in a wide variety of applications.

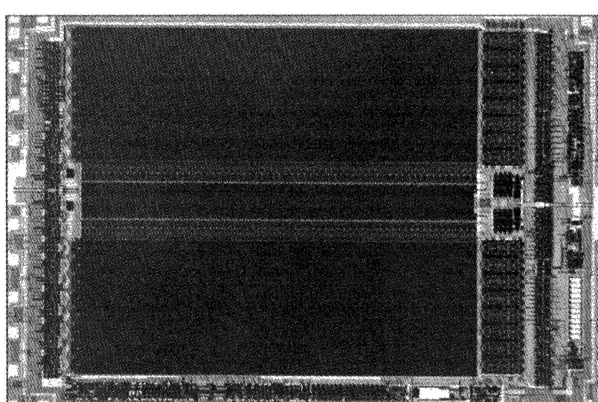
The EEPROM is the fruit of international cooperation. The cell and circuit design were contributed by Catalyst, which also created and modified the architecture. Oki Semiconductor of Tokyo furnished the process, jointly modified by the two partners, and served as the silicon foundry.

Critical to the success of the joint venture was a variety of proprietary circuit wizardry. Broadening the supply-voltage range ensured successful reads and writes despite voltage fluctuations. Bootstrapping capacitors and a clever differential sense amplifier make certain that reads are accomplished quickly in the face of low voltage and power-supply variations.

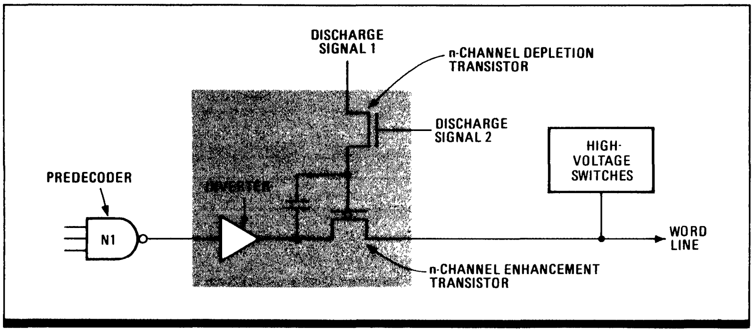
In addition, a dual-clocked, high-voltage switching circuit guarantees that switches are thrown reliably, even when the voltage fluctuates. And dynamic, rather than static, page latching keeps the memory writing even while supply voltage varies.

Measuring 4.84 by 7.06 mm and housed in a 28-pin plastic dual in-line package, the Catalyst MSM28C64A (see fig. 1) is fabricated with a slight modification of Oki's 1.5-μm n-well double-polysilicon CMOS floating-gate process. The memory incorporates five types of transistors: p-channel and n-channel enhancement-mode MOS transistors for fabricating the 3-V circuits, and enhancement, depletion, and non-ion-implanted n-type transistors for fabricating the charge-pumping circuitry that converts the 3-V supply to 18 V on-chip; in addition to these transistors, there are the floating-gate devices themselves.

The key to achieving low-voltage operation in portable applications is the ability to maintain stable reads and writes over long periods, despite the substantial variations in supply voltage associated with batteries. Relaxing the supply-voltage tolerances of the basic EEPROM cell makes that possible. With its dynamic page-mode latching scheme, the device is relatively insensitive to voltage changes and can operate even if the supply voltage varies 20% in either direction, Catalyst claims. By comparison, most competitive devices can operate only within variations of ± 10 V. When operated at, for example, 5 V, the Catalyst part's supply voltage can vary from 4 to 6 V, whereas conventional EEPROMs



1. LOW VOLTAGE. Catalyst's MSM28C64A EEPROM has five types of transistors that form the charge-pump circuit needed to convert the 3-V supply to 18 V on-chip.



2. BOOTSTRAP. A decoder circuit with bootstrapping capacitor beween the two cell transistors helps keep read operations fast despite lower voltages and wider supply tolerances.

have a much narrower operating margin, from 4.5 to 5.5 V.

An additional benefit of the lower operating voltage is that power dissipation is 25% to 50% less than that of comparable devices. At 8 MHz, active power is 49.5 milliwatts and standby is only 22.5 mW. At 1 MHz, active and standby power are 15 mW and 7.5 mW, respectively.

The low operating voltage was achieved with a variety of design improvements in both the read and write circuitry. Special bootstrap decoder circuits and a differential sense amplifier made it possible to keep reads fast despite the lower voltages and wider supply tolerances. In the first instance, the key was adding bootstrapping

Catalyst uses dynamic page-mode latching, opening the door to battery operation; the usual static latching needs a highly stable supply voltage that batteries can't supply

capacitors between the two transistors in the cell and between the decoder and the output to the word line (see fig. 2). "In present designs, when the supply voltage is too low, there is insufficient voltage across the enhancement-mode read transistor to allow it to switch reliably," Marya says. "With the addition of the bootstrap capacitor, sufficient charge is accumulated to stabilize the voltage during the read operation."

To prevent latchup that might be caused by a large instantaneous discharge of current from the capacitor onto the word line, which could occur during a write, the circuit also incorporates a predecoder to step down the discharge incrementally. The differential sense amplifier also boosts the EEPROM's reliability during reads. "In other designs, when the threshold voltage of a memory cell is set to the low state during a read, a very small current flows into the bit line, on the order of about 70 to 100 μA," says Marya. "Normally, in most 5-V designs there is sufficient voltage, on the order of 0.1 to 0.2 V, to trigger the sense amplifier." In Catalyst's 3-V design, however, the voltage change is only on the order of 0.02 V. With the use of a differential sense amplifier rather than a single-ended one, this minute voltage differential is magnified about 100 times to a level sufficient to trigger operation.

To achieve low-voltage programming, Marya says, Catalyst and Oki engineers made a number of improvements to the high-voltage switches and to the page-mode latches. Usually, the high-voltage switches are controlled by a single clock, so there is only a relatively narrow range within which the switch can sense the clock edge reliably. In 5-V devices, this occurs as long as the voltage is between 4.5 and 5.5 V. Below 4.5 V, such designs fail, switching erratically. Designers from the two companies solved this, he says, by going to a fail-safe switching scheme in which a dual clock is used, allowing the switches to operate reliably over the entire range from 3 to 7 V.

In the other critical improvement to the programming circuitry, company engineers went with a dynamic page-mode latching scheme, rather than the static configuration generally used, which is highly dependent on supply voltage for correct operation. "If the supply voltage varies outside a very narrow range of a few tenths of a volt, static latching no longer works," Marya says. "With a dynamic scheme, the page-latch threshold levels vary dynamically up and down as the supply voltage varies."

As with most other high-density EEPROMs, the 16-K-by-4-bit device also incorporates two redundant rows in the event of faulty array cells. This meant that it was necessary to modify the redundant cells to operate at lower voltages. Since they are located farther out on the array, they are served by longer lines, which means more capacitance or sensing lower-voltage signals. Here, the basic changes involved modifications to the interpoly oxide to take into account the lower voltage by reducing the load capacitance. Taking advantage of the differential-sensing scheme employed in the array, a special reset circuit selects a redundant word line when a faulty bit occurs in one of the word lines. The proprietary circuit works even when the supply voltage is as low as 1 V and consumes practically no power, Marya claims. The same scheme is also employed to select or key in EEPROM-based circuit elements to trim the programming voltage and the write cycle. *–Bernard C. Cole*

For more information, circle 481 on the reader service card.

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5/88

CATALYST SEMICONDUCTOR, INC. Headquarters
2231 Calle de Luna
Santa Clara, CA. 95054
Tel: 408-748-7700
TLX: 5106017631
FAX: 408-980-8209

UNITED KINGDOM:
CATALYST SEMICONDUCTOR, LTD.
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Great Holm
Milton Keynes
Bucks MK8 9HA
England
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Intl: 44 908 561229
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