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Dual Port Xpressview™ Advantiv HDMI Receiver Functionality and Features

SCOPE

This user guide provides a detailed description of the Advantiv™ ADV7619 functionality and features.

DISCLAIMER

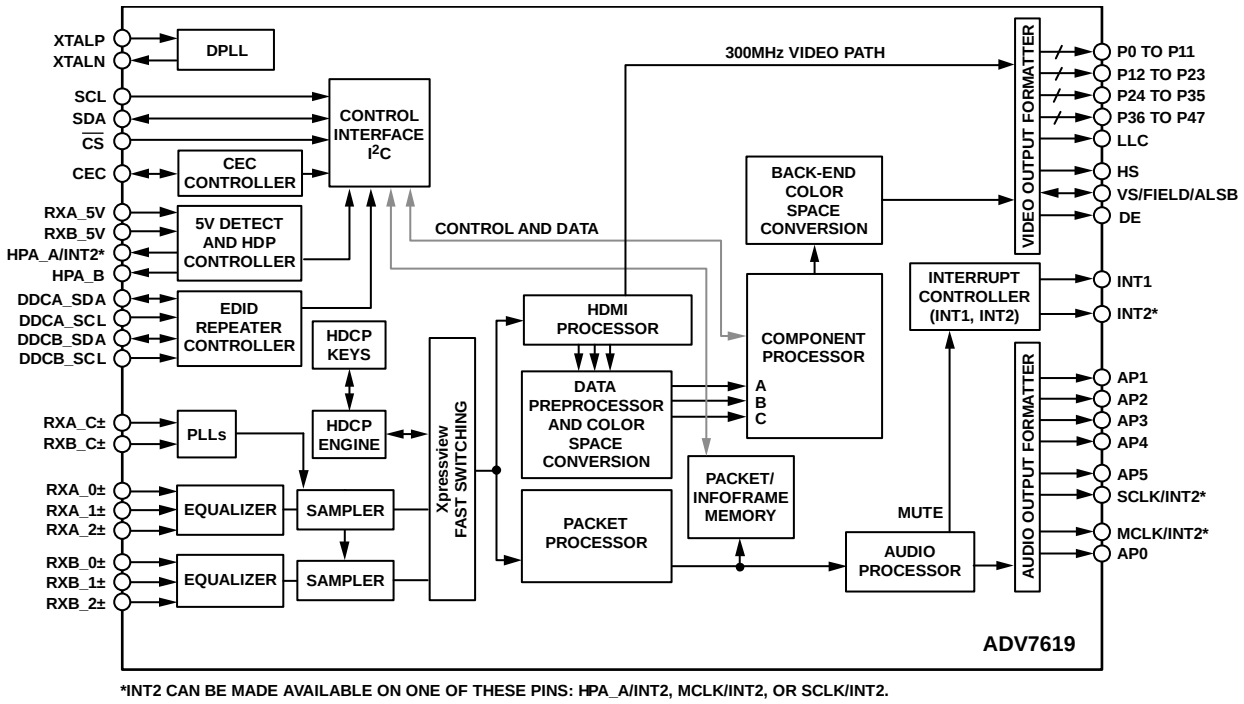

Figure 1. Functional Block Diagram

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8/11—Revision 0: Initial Version

USING THE ADV7619 HARDWARE USER GUIDE

NUMBER NOTATIONS

Table 1.

Notation	Description
Bit N	Bits are numbered in little endian format, that is, the least significant bit of a number is referred to as Bit 0.
V[X:Y]	Bit field representation covering Bit X to Bit Y of a value or a field (V).
0xNN	Hexadecimal (base-16) numbers are preceded by the prefix '0x'.
0bNN	Binary (base-2) numbers are preceded by the prefix '0b'.
NN	Decimal (base-10) are represented using no additional prefixes or suffixes.

REGISTER ACCESS CONVENTIONS

Table 2.

Mode	Description
R/W	Memory location has read and write access.
R	Memory location is read access only. A read always returns 0 unless otherwise specified.
W	Memory location is write access only.

ACRONYMS AND ABBREVIATIONS

Table 3.

Acronym/Abbreviation	Description
ACP	Audio content protection.
AGC	Automatic gain control.
Ainfo	HDCP register. Refer to HDCP documentation.
AKSV	HDCP transmitter key selection vector. Refer to HDCP documentation.
An	64-bit pseudo-random value generated by HDCP cipher function of Device A.
AP	Audio output pin.
AVI	Auxiliary video information.
BCAPS	HDCP register. Refer to HDCP documentation.
BKSV	HDCP receiver key selection vector. Refer to HDCP documentation.
CP	Component processor.
CSC	Color space converter/conversion.
DDR	Double data rate.
DE	Data enable.
DLL	Delay locked loop.
DPP	Data preprocessor.
DVI	Digital visual interface.
EAV	End of active video.
EMC	Electromagnetic compatibility.
EQ	Equalizer.
HD	High definition.
HDCP	High bandwidth digital content protection.
HDMI®	High bandwidth multimedia interface.
HDTV	High definition television.
HPA	Hot plug assert.
HPD	Hot plug detect.
HSync	Horizontal synchronization.
IC	Integrated circuit.
ISRC	International standard recording code.
I^2S	Inter IC sound.
I^2C	Inter integrated circuit.

Acronym/Abbreviation	Description
KSV	Key selection vector.
LLC	Line locked clock.
LSB	Least significant bit.
L-PCM	Linear pulse coded modulated.
Mbps	Megabit per second.
MPEG	Moving picture expert group.
ms	Millisecond.
MSB	Most significant bit.
NC	No connect.
OTP	One-time programmable.
Pj′	HDCP enhanced link verification response. Refer to HDCP documentation.
Ri′	HDCP link verification response. Refer to HDCP documentation.
Rx	Receiver.
SAV	Start of active video.
SDR	Single data rate.
SHA-1	Refer to HDCP documentation.
SMPTE	Society of Motion Picture and Television Engineers.
SOG	Sync on green.
SOY	Sync on Y.
SPA	Source physical address.
SPD	Source production descriptor.
STDI	Standard detection and identification.
TMDS	Transition minimized differential signaling.
Tx	Transmitter.
VBI	Video blanking interval.
VSync	Vertical synchronization.
XTAL	Crystal oscillator.

FIELD FUNCTION DESCRIPTIONS

Throughout this user guide, a series of function tables are provided. The function of a field is described in a table preceded by the bit name, a short function description, the I²C map, the register location within the I²C map, and a detailed description of the field.

The detailed description consists of:

- For a readable field, the values the field can take
- For a writable field, the values the field can be set to

Example Field Function Description

This section provides an example of a field function table followed by a description of each part of the table.

PRIM_MODE[3:0], IO Map, Address 0x01[3:0].

A control to select the primary mode of operation of the decoder.

Function

PRIM_MODE[3:0]	Description
0000	Reserved
0001	Reserved
0010	Reserved
0011	Reserved
0100	Reserved
0101	HDMI-Comp
0110 (default)	HDMI-GR
0111 to 1111	Reserved

In this example

- The name of the field is PRIM_MODE and it is four bit long.
- Address 0x01 is the I²C location of the field in big endian format (MSB first, LSB last).
- The address is followed by a detailed description of the field.
- The first column of the table lists values the field can take or can be set to. These values are in binary format if not preceded by 0x or in hexadecimal format if preceded by 0x.
- The second column describes the function of each field for each value the field can take or can be set to. Values are in binary format.

REFERENCES

CEA, CEA-861-D, A DTV Profile for Uncompressed High Speed Digital Interfaces, Revision D, July 18, 2006.

Digital Content Protection (DCP) LLC, High-Bandwidth Digital Content Protection System, Revision 1.4, July 8, 2009.

HDMI Licensing and LLC, High-Definition Multimedia Interface, Revision 1.4a, March 4, 2010.

ITU, ITU-R BT.656-4, Interface for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation ITU-R BT.601, February 1998.

INTRODUCTION TO THE ADV7619

The ADV7619 is a high quality, 3Gbps high bandwidth, 2:1 multiplexed High-Definition Multimedia Interface (HDMI®) receiver.

The ADV7619 incorporates a dual input HDMI receiver that supports all mandatory 3D TV formats defined in HDMI 1.4a specification, HDTV formats up to 1080p deep color 12-bit per channel or 2160p8bit color per channel and display resolutions up to 4k by 2k (3840 x 2160 at 30 Hz).

The ADV7619 also integrates an CEC controller that supports the capability discovery and control (CDC) feature.

The ADV7619 incorporates Xpressview™ fast switching on both input HDMI ports. Using Analog Devices' hardware-based HDCP engine that minimizes software overhead, Xpressview™ technology allows fast switching between both HDMI input ports in less than 1 second. Each HDMI port has dedicated +5V Detect and Hot Plug Assert pins. The HDMI receiver also includes an integrated equalizer that ensures robust operation of the interface with long cables.

Fabricated in an advanced CMOS process, the ADV7619 is provided in a 14 mm × 14 mm, 128-pin surface-mount TQFP_EP, RoHS-compliant package and is specified over 0°C to +70°C temperature range.

HDMI RECEIVER

The HDMI receiver on the ADV7619 supports 3Gbps data bandwidth allowing for video resolutions up to 4k by 2k. incorporates a fast switching feature that allows inactive ports to be HDCP authenticated to provide rapid switching between encrypted HDMI sources. The ADV7619 HDMI receiver incorporates active equalization of the HDMI data signals to compensate for the losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The equalizer is highly effective and is capable of equalizing for long cables to achieve robust receiver performance.

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the ADV7619 allows a video receiver to authenticate, decrypt encoded data and renew that authentication during transmission, as specified by the HDCP v1.4 protocol for both active and background HDMI ports.

The ADV7619 offers a flexible audio output port for audio data extraction from the HDMI stream. HDMI audio formats, including Super Audio CD (SACD) via DSD and HBR are supported by ADV7619. The HDMI receiver has advanced audio functionality, such as a mute controller, that prevents audible extraneous noise in the audio output.

COMPONENT PROCESSOR

The ADV7619 contains component processor (CP), which processes the video data up to 1080p 36-bitdeep color. The CP section provides color adjustment features, such as brightness, saturation, and hue. The color space conversion (CSC) matrix allows the color space to be changed as required. The standard detection and identification (STDI) block allows the detection of video timings.

MAIN FEATURES OF ADV7619

HDMI Receiver

- HDMI 1.4a features supported
  - 3D HDMI 1.4a video format support
  - Full colorimetry including sYCC601, Adobe RGB, Adobe YCC601, xvYCC extended gamut color
  - CEC 1.4-compatible
- HDCP 1.4 support
- 3D Video Support including Frame packing for all 3D formats up to a 297 MHz TMDS clock
- Xpressview™ fast switching between HDMI ports
- Supports display resolutions up to 4k by 2k (4096 x 2160 at 30 Hz)
- Supports all display resolutions up to UXGA (1600 x 1200 at 60Hz, 10-bit)
- Supports many audio formats including DSD, HBR, S/PDIF (IEC60958-compatible) with sampling with sampling frequency up to 192 kHz
- Programmable front-end equalization for long cable lengths
- Audio mute for removing extraneous noise
- Programmable interrupt generator to detect HDMI packets
- Internal EDID support
- Repeater support (up to 127 KSVs)

Component Video Processing

- Support video formats only up to 1080p 36-bit deep color and graphics up to UXGA 10-bit
- An any-to-any 3 × 3 CSC matrix support YCrCb to RGB and RGB to YCrCb
- Provides color controls, such as saturation, brightness, hue, and contrast
- STDI block that enables format detection
- Free run output mode provides stable timing when no video input is present

Video Output Formats

- Double data rate (DDR) 8-/10-/12-bit 4:2:2 YCrCb[1]
- Pseudo DDR (CCIR-656 type stream) 8-/10-/12-bit 4:2:2 YCrCb for 525i, 625i, 525P, and 625P
- SDR 16-/20-/24-bit 4:2:2 YCrCb for all standards
- SDR 24-/30-/36-bit 4:4:4 YCrCb/RGB for all HDMI standards
- DDR 12-/24-/30-/36-bit 4:4:4 RGB
- Interleaved 2x SDR 24 bit 422 YCrCb
- Interleaved 2x SDR 24 bit 444 YCrCb/RGB

[1] Double data rate (DDR) is supported only up to 50 MHz (an equivalent to data rate clocked with 100 MHz clock in SDR mode).

Additional Features

- HS, VS, FIELD, and DE output signals with programmable position, polarity, and width
- Numerous interrupt sources available for the INT1 and INT2 interrupt request output pins, available via one of the selected pins, that is, SCLK/INT2, MCLK/INT2, or HPA_A/INT2
- Temperature range of 0°C to +70°C
- 14 mm × 14 mm, 128-pin TQFP_EP package

FUNCTIONAL BLOCK DIAGRAM

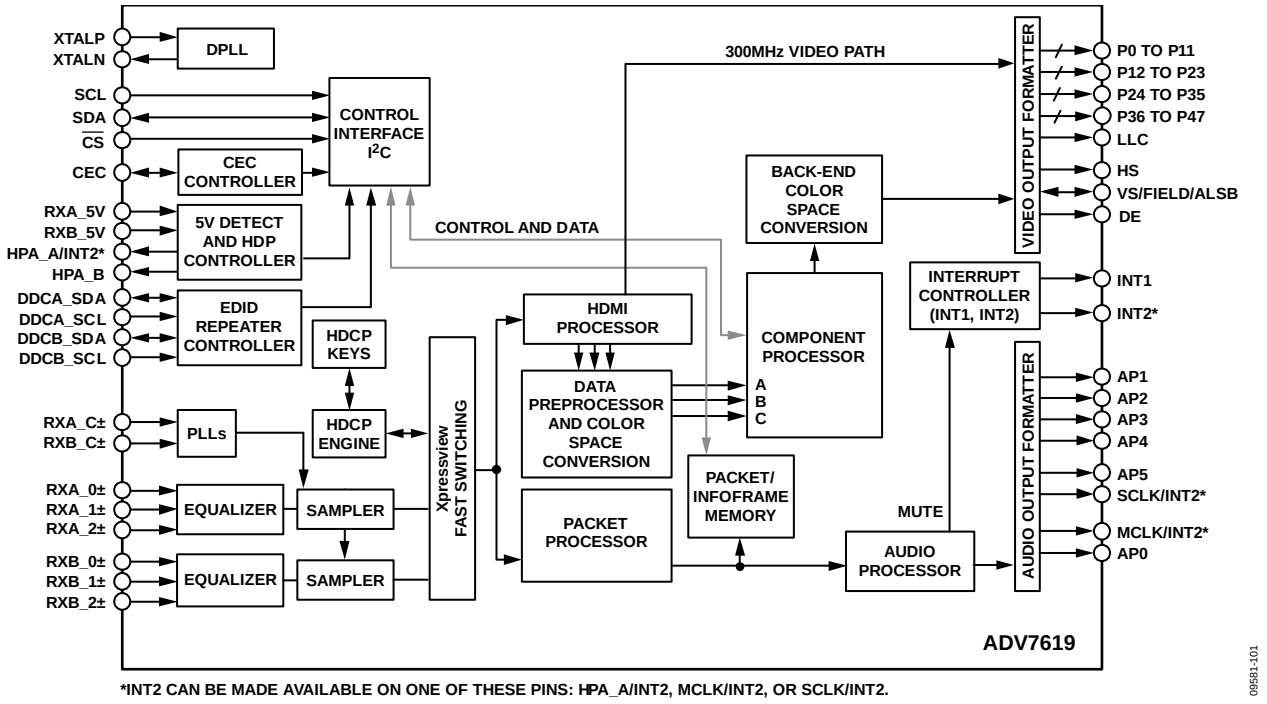
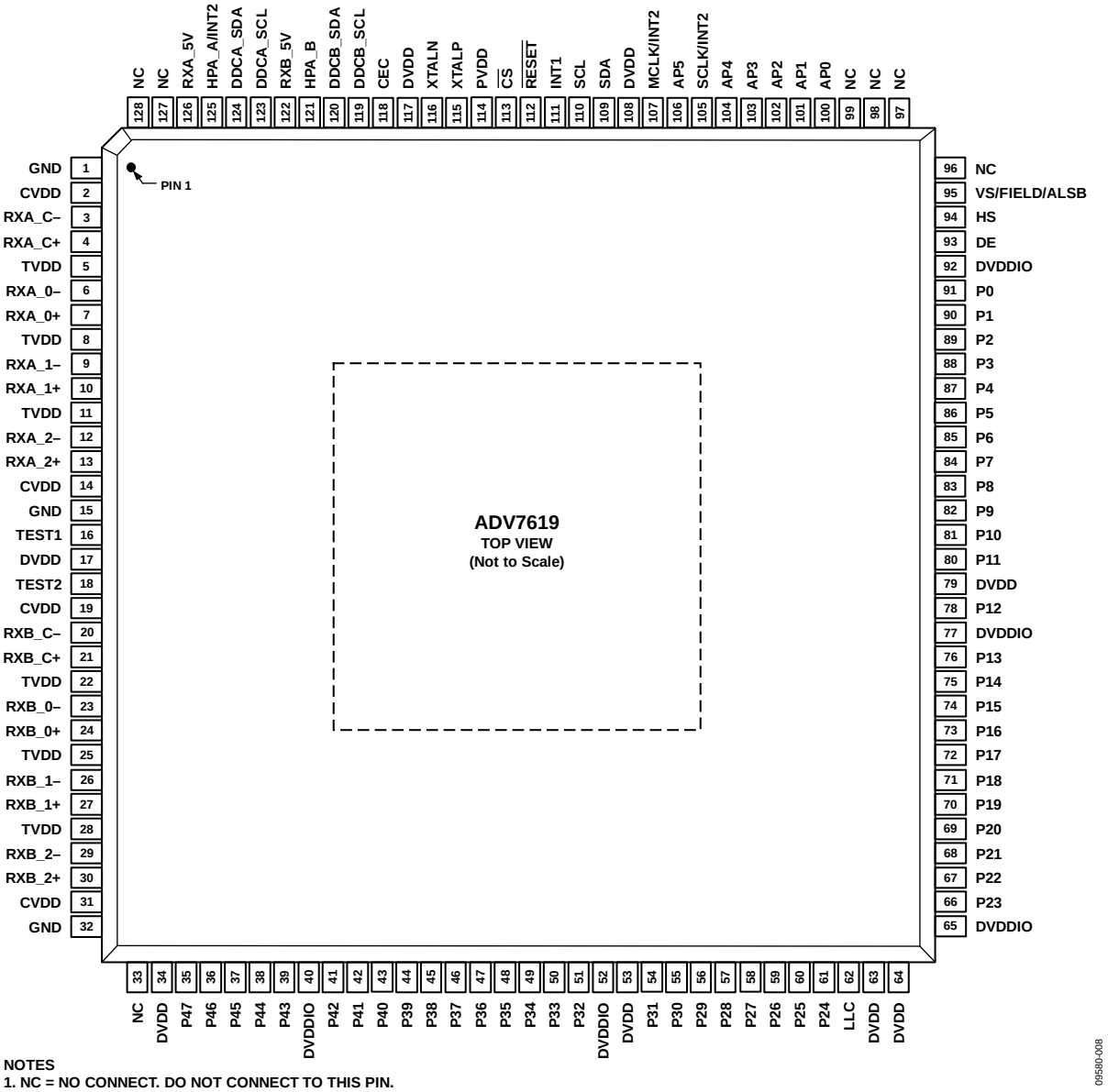


Figure 2. Functional Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. CONNECT THE EXPOSED PAD (PIN 0) ON THE BOTTOM OF THE PACKAGE TO GROUND.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	GND	Ground	Ground.
1	GND	Ground	Ground.
2	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
3	RXA_C–	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
4	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
5	TVDD	Power	Terminator Supply Voltage (3.3 V).
6	RXA_0–	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
7	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
8	TVDD	Power	Terminator Supply Voltage (3.3 V).
9	RXA_1–	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
10	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.

Pin No.	Mnemonic	Type	Description
11	TVDD	Power	Terminator Supply Voltage (3.3 V).
12	RXA_2–	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
13	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
14	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
15	GND	Ground	Ground.
16	TEST1	Test	This pin must be left floating.
17	DVDD	Power	Digital Core Supply Voltage (1.8 V)
18	TEST2	Test	This pin must be left floating.
19	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
20	RXB_C–	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
21	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
22	TVDD	Power	Terminator Supply Voltage (3.3 V).
23	RXB_0–	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
24	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
25	TVDD	Power	Terminator Supply Voltage (3.3 V).
26	RXB_1–	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
27	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
28	TVDD	Power	Terminator Supply Voltage (3.3 V).
29	RXB_2–	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
30	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
31	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
32	GND	Ground	Ground.
33	NC	No connect	No connect.
34	DVDD	Power	Digital Core Supply Voltage (1.8 V).
35	P47	Digital video output	Video Pixel Output Port.
36	P46	Digital video output	Video Pixel Output Port.
37	P45	Digital video output	Video Pixel Output Port.
38	P44	Digital video output	Video Pixel Output Port.
39	P43	Digital video output	Video Pixel Output Port.
40	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
41	P42	Digital video output	Video Pixel Output Port.
42	P41	Digital video output	Video Pixel Output Port.
43	P40	Digital video output	Video Pixel Output Port.
44	P39	Digital video output	Video Pixel Output Port.
45	P38	Digital video output	Video Pixel Output Port.
46	P37	Digital video output	Video Pixel Output Port.
47	P36	Digital video output	Video Pixel Output Port.
48	P35	Digital video output	Video Pixel Output Port.
49	P34	Digital video output	Video Pixel Output Port.
50	P33	Digital video output	Video Pixel Output Port.
51	P32	Digital video output	Video Pixel Output Port.
52	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
53	DVDD	Power	Digital Core Supply Voltage (1.8 V).
54	P31	Digital video output	Video Pixel Output Port.

Pin No.	Mnemonic	Type	Description
55	P30	Digital video output	Video Pixel Output Port.
56	P29	Digital video output	Video Pixel Output Port.
57	P28	Digital video output	Video Pixel Output Port.
58	P27	Digital video output	Video Pixel Output Port.
59	P26	Digital video output	Video Pixel Output Port.
60	P25	Digital video output	Video Pixel Output Port.
61	P24	Digital video output	Video Pixel Output Port.
62	LLC	Digital video output	Pixel Output Clock for the Pixel Data (Range is 13.5 MHz to 170 MHz).
63	DVDD	Power	Digital Core Supply Voltage (1.8 V).
64	DVDD	Power	Digital Core Supply Voltage (1.8 V).
65	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
66	P23	Digital video output	Video Pixel Output Port.
67	P22	Digital video output	Video Pixel Output Port.
68	P21	Digital video output	Video Pixel Output Port.
69	P20	Digital video output	Video Pixel Output Port.
70	P19	Digital video output	Video Pixel Output Port.
71	P18	Digital video output	Video Pixel Output Port.
72	P17	Digital video output	Video Pixel Output Port.
73	P16	Digital video output	Video Pixel Output Port.
74	P15	Digital video output	Video Pixel Output Port.
75	P14	Digital video output	Video Pixel Output Port.
76	P13	Digital video output	Video Pixel Output Port.
77	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
78	P12	Digital video output	Video Pixel Output Port.
79	DVDD	Power	Digital Core Supply Voltage (1.8 V).
80	P11	Digital video output	Video Pixel Output Port.
81	P10	Digital video output	Video Pixel Output Port.
82	P9	Digital video output	Video Pixel Output Port.
83	P8	Digital video output	Video Pixel Output Port.
84	P7	Digital video output	Video Pixel Output Port.
85	P6	Digital video output	Video Pixel Output Port.
86	P5	Digital video output	Video Pixel Output Port.
87	P4	Digital video output	Video Pixel Output Port.
88	P3	Digital video output	Video Pixel Output Port.
89	P2	Digital video output	Video Pixel Output Port.
90	P1	Digital video output	Video Pixel Output Port.
91	P0	Digital video output	Video Pixel Output Port.
92	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).

Pin No.	Mnemonic	Type	Description
93	DE	Miscellaneous digital	DE (data enable) is a signal that indicates active pixel data.
94	HS	Digital video output	HS is a horizontal synchronization output signal.
95	VS/FIELD/ALSB	Digital video output	VS is a vertical synchronization output signal. FIELD is a field synchronization output signal in all interlaced video modes. VS or FIELD can be configured for this pin. The ALSB allows selection of the I^2C address.
96	NC	No connect	No connect.
97	NC	No connect	No connect.
98	NC	No connect	No connect.
99	NC	No connect	No connect.
100	AP0	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD) or I^2S.
101	AP1	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD) or I^2S.
102	AP2	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD) or I^2S.
103	AP3	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD) or I^2S.
104	AP4	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD) or I^2S.
105	SCLK/INT2	Miscellaneous digital	A dual function pin that can be configured to output Audio Serial Clock or an Interrupt2 signal.
106	AP5	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD) or I^2S. Additionally pin AP5 can be configured to provide LRCLK.
107	MCLK/INT2	Miscellaneous	A dual function pin that can be configured to output Audio Master Clock or an Interrupt2 signal.
108	DVDD	Power	Digital Core Supply Voltage (1.8 V).
109	SDA	Miscellaneous digital	I^2C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
110	SCL	Miscellaneous digital	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
111	INT1	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user configuration.
112	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7619 circuitry.
113	$\overline{\text{CS}}$	Miscellaneous digital	Chip Select. This pin has an internal pull-down. Pulling this line up causes I^2C state machine to ignore I^2C transmission.
114	PVDD	Power	PLL Supply Voltage (1.8 V).
115	XTALP	Miscellaneous analog	Input Pin for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7619.
116	XTALN	Miscellaneous analog	Crystal Input. Input pin for 28.63636 MHz crystal.
117	DVDD	Power	Digital Core Supply Voltage (1.8 V).
118	CEC	Digital input/output	Consumer Electronic Control Channel.
119	DDCB_SCL	HDMI input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
120	DDCB_SDA	HDMI input	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input that is 5 V tolerant.
121	HPA_B	Miscellaneous digital	Hot Plug Assert signal output for HDMI Port B. This pin is open-drain.
122	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface.
123	DDCA_SCL	HDMI input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
124	DDCA_SDA	HDMI input	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input that is 5 V tolerant.
125	HPA_A/INT2	Miscellaneous digital	A dual function open-drain pin that can be configured to output Hot Plug Assert signal (for HDMI Port A) or an Interrupt2 signal.
126	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.
127	NC	No connect	No connect.
128	NC	No connect	No connect.

GLOBAL CONTROL REGISTERS

The register control bits described in this section deal with the general control of the chip, and the CP and the HDMI receiver sections of the ADV7619.

ADV7619 REVISION IDENTIFICATION

RD_INFO[15:0], IO, Address 0xEA[7:0]; Address 0xEB[7:0] (Read Only)

Chip revision code.

Function

RD_INFO[15:0]	Description
0x20C1	ADV7619

POWER-DOWN CONTROLS

Primary Power-Down Controls

POWER_DOWN is the main power-down control. It is the main control for power-down Mode 0 and Mode 1. See the Power-Down Modes section for more details.

POWER_DOWN, IO, Address 0x0C[5]

A control to enable power-down mode. This is the main I²C power-down control.

Function

POWER_DOWN	Description
0	Chip operational
1 (default)	Enables chip power down

Secondary Power-Down Controls

The following controls allow various sections of the ADV7619 to be powered down.

It is possible to stop the clock to the CP to reduce power for a power-sensitive application. The CP_PWRDN bit enables this power-save mode. The HDMI block is not affected by this power-save mode. This allows the use of limited HDMI, STDI monitoring features while reducing the power consumption. For full processing of the HDMI input, the CP core needs to be powered up.

CP_PWRDN, IO, Address 0x0C[2]

A power-down control for the CP core.

Function

CP_PWRDN	Description
0 (default)	Powers up clock to CP core.
1	Powers down clock to CP core. HDMI block not affected by this bit.

XTAL_PDN

XTAL_PDN allows the user to power down the XTAL clock in the following sections:

- STDI blocks
- Free run synchronization generation block
- I²C sequencer block, which is used for the configuration of the gain, clamp, and offset
- CP and HDMI section

The XTAL clock is also provided to the HDCP engine, EDID, and the repeater controller within the HDMI receiver. The XTAL clock within these sections is not affected by XTAL_PDN.

XTAL_PDN, IO, Address 0x0B[0]

A power-down control for the XTAL in the digital blocks.

Function

XTAL_PDN	Description
0 (default)	Powers up XTAL buffer to digital core
1	Powers down XTAL buffer to digital core

CORE_PDN

CORE_PDN allows the user to power down clocks, with the exception of the XTAL clock, in the following sections:

- CP block
- Digital section of the HDMI block

CORE_PDN, IO, Address 0x0B[1]

A power-down control for the DPP, CP core, and digital sections of the HDMI core.

Function

CORE_PDN	Description
0 (default)	Powers up CP and digital sections of HDMI block
1	Powers down CP and digital section of HDMI block

Power-Down Modes

The ADV7619 supports the following power-down modes:

- Power-Down Mode 0
- Power-Down Mode 1

Table 5 shows the power-down and normal modes of ADV7619.

Table 5. Power-Down Modes

POWER_DOWN Bit	CEC_POWER_UP Bit	CEC	EDID	Power-Down Mode
1	0	Disabled	Enabled	Power-Down Mode 0
1	1	Enabled	Enabled	Power-Down Mode 1
0	0	Disabled	Enabled[1]	Normal mode
0	1	Enabled	Enabled[1]	Normal mode

[1] Dependent on the values of EDID_X_ENABLE_CPU and EDID_X_ENABLE for the HDMI port (where X is A).

Power-Down Mode 0

In Power-Down Mode 0, selected sections and pads are kept active to provide EDID and +5 V antiglitch filter functionality.

In Power-Down Mode 0, the sections of the ADV7619 are disabled except for the following blocks:

- I^2C slave section
- EDID/repeater controller
- EDID ring oscillator
  The ring oscillator provides a clock to the EDID/repeater controller (refer to the E-EDID/Repeater Controller section) and the +5 V power supply antiglitch filter. The clock output from the ring oscillator runs at approximately 50 MHz.

The following pads only are enabled in Power-Down Mode 0:

- I^2C pads
  - SDA
  - SCL
- +5 V pads
  - RXA_5V
  - RXB_5V
  - HPA_A
  - HPA_B
- DDC pads
  - DDCA_SCL
  - DDCA_SDA
  - DDCB_SCL
  - DDCB_SDA
- Reset pad $\overline{\text{RESET}}$

Power-Down Mode 0 is initiated through a software (I^2C register) configuration.

Entering Power-Down Mode 0 via Software

The ADV7619 can be put into Power-Down Mode 0 by setting **POWER_DOWN** to 1 (default value) and **CEC_POWER_UP** to 0. This method allows an external processor to put the system in which the ADV7619 is integrated into standby mode. In this case, the CP and HDMI cores of the ADV7619 are kept powered up from the main power (for example, ac power) and set in or out of power-down Mode 0 through the POWER_DOWN bit.

Power-Down Mode 1

Power-Down Mode 1 is enabled when the following conditions are met:

- POWER_DOWN bit is set to 1
- CEC section is enabled by setting CEC_POWER_UP to 1

Power-Down Mode 1 provides the same functionality as Power-Down Mode 0, with the addition of the following sections:

- XTAL clock
- CEC section
- Interrupt controller section

The following pads are enabled in Power-Down Mode 1:

- Same pads as enabled in Power-Down Mode 0
- CEC pad
- INT1 and INT2 interrupt pads

The internal EDID is also accessible through the DDC bus for Port A and Port B in Power-Down Mode 0 and Power-Down Mode 1.

GLOBAL PIN CONTROL

$\overline{\text{RESET}}$ Pin

The ADV7619 can be reset by a low reset pulse on the reset pin with a minimum width of 5 ms. It is recommended to wait 5 ms after the low pulse before an I²C write is performed to the ADV7619.

Reset Controls

MAIN_RESET, IO, Address 0xFF[7] (Self-Clearing)

Main reset where I²C registers are reset to their default values.

Function

MAIN_RESET	Description
0 (default)	Normal operation
1	Applies main I²C reset

Tristate Output Drivers

PADS_PDN, IO, Address 0x0C[0]

A power-down control for pads of the digital outputs. When enabled, the pads are tristated and the input path is disabled. This control applies to the DE, HS, VS/FIELD/ALSB, INT1, and LLC pads and to the P0 to P47 pixel pads.

Function

PADS_PDN	Description
0 (default)	Powers up pads of digital output pins
1	Powers down pads of digital output pins

DDC_PWRDN, Addr 68 (HDMI), Address 0x73[0]

A power-down control for DDC pads.

Function

DDC_PWRDN	Description
0 (default)	Powers up all DDC pads
1	Powers down all DDC pads

TRI_PIX

This bit allows the user to tristate the output driver of pixel outputs. Upon setting TRI_PIX, the pixel output P[35:0] is tristated.

TRI_PIX, IO, Address 0x15[1]

A control to tristate the pixel data on the pixel pins, P[47:0].

Function

TRI_PIX	Description
0	Pixel bus active
1 (default)	Tristates pixel bus

Tristate LLC Driver

TRI_LLC, IO, Address 0x15[2]

A control to tristate the output pixel clock on the LLC pin.

Function

TRI_LLC	Description
0	LLC pin active
1 (default)	Tristates LLC pin

Tristate Synchronization Output Drivers

The following output synchronization signals are tristated when TRI_SYNCS is set:

- VS/FIELD/ALSB
- HS
- DE

The drive strength controls for these signals are provided via the DR_STR_SYNC bits. The ADV7619 does not support tristating via a dedicated pin.

TRI_SYNCS, IO, Address 0x15[3]

Synchronization output pins tristate control. The synchronization pins under this control are HS, VS/FIELD/ALSB, and DE.

Function

TRI_SYNCS	Description
0	Sync output pins active
1 (default)	Tristates sync output pins

Tristate Audio Output Drivers

TRI_AUDIO, IO Map, Address 0x15, [4]

TRI_AUDIO allows the user to tristate the drivers of the following audio output signals:

- AP0
- AP1
- AP2
- AP3
- AP4
- AP5
- SCLK/INT2
- MCLK/INT2

The drive strength for the output pins can be controlled by the DR_STR[1:0] bits. The ADV7619 does not support tristating via a dedicated pin.

TRI_AUDIO, IO, Address 0x15[4]

A control to tristate the audio output interface pins (AP0…AP5).

Function

TRI_AUDIO	Description
0	Audio output pins active
1 (default)	Tristates audio output pins

Drive Strength Selection

DR_STR

It may be desirable to strengthen or weaken the drive strength of the output drivers for Electromagnetic Compatibility (EMC) and crosstalk reasons. This section describes the controls to adjust the output drivers used by the CP and HDMI modes.

The drive strenth DR_STR_SYNC[1:0] bits allow the user to select the strength of the following synchronization signals:

- DE
- HS
- VS/FIELD

The DR_STR[1:0] drive strength bits affect output drivers for the following output pins:

- P[47:0]
- AP0 to AP5
- SCLK
- SDA
- SCL

The drive strength DR_STR_CLK[1:0] bits affect output driver for LLC line.

DR_STR[1:0], IO, Address 0x14[5:4]

A control to set the drive strength of the data output drivers.

Function

DR_STR[1:0]	Description
00	Reserved
01	Medium low (2×)
10 (default)	Medium high (3×)
11	High (4×)

DR_STR_CLK[1:0], IO, Address 0x14[3:2]

A control to set the drive strength control for the output pixel clock out signal on the LLC pin.

Function

DR_STR_CLK[1:0]	Description
00	Reserved
01	Medium low (2×) for LLC up to 60 MHz
10 (default)	Medium high (3×) for LLC from 44 MHz to 105 MHz
11	High (4×) for LLC greater than 100 MHz

DR_STR_SYNC[1:0], IO, Address 0x14[1:0]

A control to set the drive strength of the synchronization pins, HS, VS/FIELD/ALSB, and DE.

Function

DR_STR_SYNC[1:0]	Description
00	Reserved
01	Medium low (2×)
10 (default)	Medium high (3×)
11	High (4×)

Output Synchronization Selection

VS_OUT_SEL, IO, Address 0x06[7]

A control to select the VSync or FIELD signal to be output on the VS/FIELD/ALSB pin.

Function

VS_OUT_SEL	Description
0	Selects FIELD output on VS/FIELD/ALSB pin
1 (default)	Selects VSync output on VS/FIELD/ALSB pin

F_OUT_SEL, IO, Address 0x05[4]

A control to select the DE or FIELD signal to be output on the DE pin.

Function

F_OUT_SEL	Description
0 (default)	Selects DE output on DE pin
1	Selects FIELD output on DE pin

Output Synchronization Signals Polarity

INV_LLC_POL, IO Map, Address 0x06, [0]

The polarity of the pixel clock provided by the ADV7619 via the LLC pin can be inverted using the INV_LLC_POL bit. Note that this inversion affects only the LLC output pin. The other output pins are not affected by INV_LLC_POL.

Changing the polarity of the LLC clock output may be necessary in order to meet the setup and hold time expectations of the downstream devices processing the output data of the ADV7619. It is expected that these parameters must be matched regardless of the type of video data that is transmitted. Therefore, INV_LLC_POL is designed to be mode independent.

INV_LLC_POL, IO, Address 0x06[0]

A control to select the polarity of the LLC.

Function

INV_LLC_POL	Description
0 (default)	Does not invert LLC
1	Inverts LLC

The output synchronization signals HS, VS/FIELD/ALSB, and DE can be inverted using the following control bits:

- **INV_HS_POL**
- **INV_VS_POL**
- **INV_F_POL**

INV_HS_POL, IO, Address 0x06[1]

A control to select the polarity of the HS signal.

Function

INV_HS_POL	Description
0 (default)	Negative polarity HS
1	Positive polarity HS

INV_VS_POL, IO, Address 0x06[2]

A control to select the polarity of the VS/FIELD/ALSB signal.

Function

INV_VS_POL	Description
0 (default)	Negative polarity VS/FIELD/ALSB
1	Positive polarity VS/FIELD/ALSB

INV_F_POL, IO, Address 0x06[3]

A control to select the polarity of the DE signal.

Function

INV_F_POL	Description
0 (default)	Default FIELD/DE polarity (positive FIELD/DE polarity)
1	Inverted FIELD/DE polarity (negative FIELD/DE polarity)

Digital Synthesizer Controls

The ADV7619 features two digital encoder synthesizers that generate the following clocks:

- Video DPLL: this clock synthesizer generates the pixel clock. It undoes the effect of deep color and pixel repetition that are inherent to HDMI streams. The output of the LLC pin is either this pixel clock or a divided down version, depending on the datapath configuration. It takes less than one video frame for this synthesizer to lock.
- Audio DPLL: this clock synthesizer generates the audio clock. As per HDMI specification, the incomming HDMI clock is divided down by CTS and then multiplied up by N. This audio clock is used as the main clock in the audio stream section. The output of MCLK represents this clock. It takes less than 5 ms after a valid ACR packet for this synthesizer to lock.

Crystal Frequency Selection

The ADV7619 supports 27.0, 28.63636, 24.576 and 24.0 MHz frequency crystals. Following control allows selecting crystal frequency.

XTAL_FREQ_SEL[1:0], IO, Address 0x04[2:1]

A control to set the XTAL frequency used.

Function

XTAL_FREQ_SEL[1:0]	Description
00	27 MHz
01 (default)	28.63636 MHz
10	24.576 MHz
11	24.0 MHz

PRIMARY MODE AND VIDEO STANDARD

Setting the primary mode and choosing a video standard are the most fundamental settings when configuring the ADV7619. There are two primary modes for the ADV7619: HDMI-component and HDMI-graphic modes. The appropriate mode should be set with **PRIM_MODE[3:0]**.

In HDMI modes, the ADV7619 can receive and decode HDMI or DVI data throughout the DVI/HDMI receiver front end. Video data from the HDMI receiver is routed to the CP block while audio data is available on the audio interface. One of these modes is enabled by selecting either the HDMI-component or the HDMI-graphics primary mode.

Note: The HDMI receiver decodes and processes any applied HDMI stream irrespective of the video resolution. However, many primary mode and video standard combinations can be used to define how the decoded video data routed to the DPP and CP blocks is processed. This allows for free run features and data decimation modes that some systems may require.

If free run and decimation are not required, it is recommended to set the following configuration for HDMI mode:

- PRIM_MODE[3:0]: 0x06
- VID_STD[5:0]: 0x02

PRIMARY MODE AND VIDEO STANDARD CONTROLS

PRIM_MODE[3:0], IO, Address 0x01[3:0]

A control to select the primary mode of operation of the decoder. Setting the appropriate HDMI mode is important for free run mode to work properly. This control is used with VID_STD[5:0].

Function

PRIM_MODE[3:0]	Description
0000	Reserved
0001	Reserved
0010	Reserved
0011	Reserved
0100	Reserved
0101	HDMI component
0110 (default)	HDMI graphics
0111 to 1111	Reserved

VID_STD[5:0], IO, Address 0x00[5:0]

Sets the input video standard mode. Configuration is dependent on PRIM_MODE[3:0]. Setting the appropriate mode is important for free run mode to work properly.

Function

VID_STD[5:0]	Description
000010	Default value

PRIM_MODE[3:0] should be used with VID_STD[5:0] to select the required video mode. These controls are set according to Table 6.

Table 6. Primary Mode and Video Standard Selection

PRIM_MODE[3:0]		VID_STD[5:0]				
Code	Description	Processor	Code	Input Video	Output Resolution	Comment
0000	Reserved		xxxxxx	Reserved	Reserved	
0001	Reserved		xxxxxx	Reserved	Reserved	
0010	Reserved		xxxxxx	Reserved	Reserved	
0100	Reserved		xxxxxx	Reserved	Reserved	
0011	Reserved		xxxxxx	Reserved	Reserved	

PRIM_MODE[3:0]		VID_STD[5:0]				
Code	**Description**	**Processor**	**Code**	**Input Video**	**Output Resolution**	**Comment**
0101	HDMI-COMP (Component video)	CP	000000	SD 1×1 525i	720 × 480	HDMI receiver support
		CP	000001	SD 1×1 625i	720 × 576	
		CP	000010	SD 2×1 525i	720 × 480	
		CP	000011	SD 2×1 625i	720 × 576	
			000100	Reserved	Reserved	
			000101	Reserved	Reserved	
			000110	Reserved	Reserved	
			000111	Reserved	Reserved	
			001000	Reserved	Reserved	
			001001	Reserved	Reserved	
		CP	001010	PR 1×1 525p	720 × 480	
		CP	001011	PR 1×1 625p	720 × 576	
		CP	001100	PR 2×1 525p	720 × 480	
		CP	001101	PR 2×1 625p	720 × 576	
			001110	Reserved	Reserved	
			001111	Reserved	Reserved	
			010000	Reserved	Reserved	
			010001	Reserved	Reserved	
			010010	Reserved	Reserved	
		CP	010011	HD 1×1	1280 × 720	
		CP	010100	HD 1×1	1920 × 1080	
		CP	010101	HD 1×1	1920 × 1035	
		CP	010110	HD 1×1	1920 × 1080	
		CP	010111	HD 1×1	1920 × 1152	
			011000	Reserved	Reserved	
		CP	011001	HD 2×1 720p	1280 × 720	
		CP	011010	HD 2×1 1125	1920 × 1080	
		CP	011011	HD 2×1 1125	1920 × 1035	
		CP	011100	HD 2×1 1250	1920 × 1080	
		CP	011101	HD 2×1 1250	1920 × 1152	
		CP	011110	HD 1×1	1920 × 1080	
		CP	011111	HD 1×1	1920 × 1080	
0110	HDMI-GR (Graphics)	CP	000000	SVGA	800 × 600 @ 56	HDMI receiver support
		CP	000001	SVGA	800 × 600 @ 60	
		CP	000010	SVGA	800 × 600 @ 72	
		CP	000011	SVGA	800 × 600 @ 75	
		CP	000100	SVGA	800 × 600 @ 85	
		CP	000101	SXGA	1280 × 1024 @ 60	
		CP	000110	SXGA	1280 × 1024 @ 75	
			000111	Reserved	Reserved	
		CP	001000	VGA	640 × 480 @ 60	
		CP	001001	VGA	640 × 480 @ 72	
		CP	001010	VGA	640 × 480 @ 75	
		CP	001011	VGA	640 × 480 @ 85	
		CP	001100	XGA	1024 × 768 @ 60	
		CP	001101	XGA	1024 × 768 @ 70	
		CP	001110	XGA	1024 × 768 @ 75	
		CP	001111	XGA	1024 × 768 @ 85	
			01xxxx	Reserved		
		CP	10000	WXGA	1280 × 768 @ 60	
		CP	10001	WXGA-R[1]	1280 × 768 @ 60	
		CP	10010	WXGA+	1360 × 768 @ 60	

PRIM_MODE[3:0]		VID_STD[5:0]				
Code	**Description**	**Processor**	**Code**	**Input Video**	**Output Resolution**	**Comment**
		CP	10011	WXGA	1366 × 768 @ 60	
		CP	10100	SXGA+	1400 × 1050 @ 60	
		CP	10101	SXGA+	1400 × 1050 @ 75	
		CP	10110	UXGA	1600 × 1200 @ 60	
		CP	10111	UXGA-R[1]	1600 × 1200 @ 60	
		CP	11000	WSXGA	1680 × 1050 @ 60	
		CP	11001	WUXGA-R[1]	1920 × 1200 @ 60	
0111	Reserved		xxxxxx	Reserved	Reserved	
1000	Reserved		xxxxxx	Reserved	Reserved	
1001	Reserved		xxxxxx	Reserved	Reserved	
1010	Reserved		xxxxxx	Reserved	Reserved	
1011	Reserved		xxxxxx	Reserved	Reserved	
1100	Reserved		xxxxxx	Reserved	Reserved	
1101	Reserved		xxxxxx	Reserved	Reserved	
1110	Reserved		xxxxxx	Reserved	Reserved	
1111	Reserved		xxxxxx	Reserved	Reserved	

[1] R = reduced blanking.

V_FREQ

This control is set to allow free run to work correctly (refer to Table 7).

V_FREQ[2:0], IO, Address 0x01[6:4]

A control to set vertical frequency.

Function

V_FREQ[2:0]	Description
000 (default)	60 Hz
001	50 Hz
010	30 Hz
011	25 Hz
100	24 Hz
101	Reserved
110	Reserved
111	Reserved

HDMI DECIMATION MODES

Some of the modes defined by VID_STD have an inherent 2×1 decimation. For these modes, the main clock generator and the decimation filters in the DPP block are configured automatically. This ensures the correct data rate at the input to the CP block. Refer to the Data Preprocessor and Color Space Conversion and Color Controls section for more information on the automatic configuration of the DPP block.

The ADV7619 correctly decodes and processes any incoming HDMI stream with the required decimation, irrespective of its video resolution:

- In 1×1 mode (that is, without decimation), as long the PRIM_MODE and VID_STD registers are programmed for any HDMI mode without decimation.
  For example:
  - Set PRIM_MODE to 0x5 and VID_STD to 0x00
  - Set PRIM_MODE to 0x5 and VID_STD to 0x13
  - Set PRIM_MODE to 0x6 and VID_STD to 0x02
- In 2×1 decimation mode, as long the PRIM_MODE and VID_STD registers are programmed for any HDMI mode with 2×1 decimation. For example:
  - Set PRIM_MODE to 0x5 and VID_STD to 0x0C
  - Set PRIM_MODE to 0x5 and VID_STD to 0x19

Note: Decimating the video data from an HDMI stream is optional and should be performed only if it is required by the downstream devices connected to the ADV7619.

PRIMARY MODE AND VIDEO STANDARD CONFIGURATION FOR HDMI FREE RUN

If free run is enabled in HDMI mode, PRIM_MODE[3:0] and VID_STD[5:0] specify the input resolution expected by the ADV7619 (for free run Mode 1) and/or the output resolution to which the ADV7619 free runs (for free run Mode 0 and Mode 1). Refer to the Free Run Mode section for additional details on the free run feature for HDMI inputs and to **HDMI_FRUN_MODE**.

RECOMMENDED SETTINGS FOR HDMI INPUTS

This section provides the recommended settings for an HDMI input encapsulating a video resolution corresponding to a selection Video ID Code described in the 861 specification.

Table 7 provides the recommended settings for the following registers:

- PRIM_MODE
- VID_STD
- V_FREQ (V_FREQ should be set to 0x0 if not specified in Table 7.)
- INV_HS_POL = 1 (INV_HS_POL should be set to 1 if not specified in Table 7.)
- INV_VS_POL = 1 (INV_VS_POL should be set to 1 if not specified in Table 7.)

Table 7. Recommended Settings for HDMI Inputs

Video ID Codes (861 Specification)	Formats	Pixel Repetition	Recommended Settings if Free Run Used and DIS_AUTOPRAM_BUFFER = 0	Recommended Settings if Free Run Not Used or Free Run Used and DIS_AUTO_PARAM_BUFFER = 1
2, 3	720 × 480p @ 60 Hz	0	PRIM_MODE = 0x5 VID_STD = 0xA	PRIM_MODE = 0x6 VID_STD = 0x2
4	1280 × 720p @ 60 Hz	0	PRIM_MODE = 0x5 VID_STD = 0x13	PRIM_MODE = 0x6 VID_STD = 0x2
5	1920 × 1080i @ 60 Hz	0	PRIM_MODE = 0x5 VID_STD = 0x14	PRIM_MODE = 0x6 VID_STD = 0x2
6, 7	720 (1440) × 480i @ 60 Hz	1	PRIM_MODE = 0x5 VID_STD = 0x0	PRIM_MODE = 0x6 VID_STD = 0x2
10, 11	2880 × 480i @ 60 Hz	3	PRIM_MODE = 0x5 VID_STD = 0x0	PRIM_MODE = 0x6 VID_STD = 0x2
14, 15	1440 × 480p @ 60 Hz	1	PRIM_MODE=0x5 VID_STD = 0xA	PRIM_MODE = 0x6 VID_STD = 0x2
16	1920 × 1080p @ 60 Hz	0	PRIM_MODE = 0x5 VID_STD = 0x1E	PRIM_MODE = 0x6 VID_STD = 0x2
17, 18	720 × 576p @ 60 Hz	0	PRIM_MODE = 0x5 VID_STD = 0xB	PRIM_MODE = 0x6 VID_STD = 0x2
19	1280 × 720p @ 50 Hz	0	PRIM_MODE = 0x5 VID_STD = 0xA3 V_FREQ = 0x1	PRIM_MODE = 0x6 VID_STD = 0x2
20	1920 × 1080i @ 50 Hz	0	PRIM_MODE = 0x5 VID_STD = 0x14 V_FREQ = 0x1	PRIM_MODE = 0x6 VID_STD = 0x2
21, 22	720 (1440) ×576i @ 60 Hz	1	PRIM_MODE = 0x5 VID_STD = 0x1	PRIM_MODE = 0x6 VID_STD = 0x2
25, 26	2880 × 480i @ 60 Hz	3	PRIM_MODE=0x5 VID_STD = 0x1	PRIM_MODE = 0x6 VID_STD = 0x2
29, 30	144 0× 576p @ 60 Hz	1	PRIM_MODE = 0x5 VID_STD = 0xA	PRIM_MODE = 0x6 VID_STD = 0x2
31	1920 × 1080p @ 50 Hz	0	PRIM_MODE = 0x5 VID_STD = 0x1E V_FREQ = 0x1	PRIM_MODE = 0x6 VID_STD = 0x2
32	1920 × 1080p @ 24 Hz	0	PRIM_MODE = 0x5 VID_STD = 0x1E	PRIM_MODE = 0x6 VID_STD = 0x2

Video ID Codes (861 Specification)	Formats	Pixel Repetition	Recommended Settings if Free Run Used and DIS_AUTOPRAM_BUFFER = 0	Recommended Settings if Free Run Not Used or Free Run Used and DIS_AUTO_PARAM_BUFFER = 1
33	1920 × 1080p @ 25 Hz	0	V_FREQ = 0x4 PRIM_MODE = 0x5 VID_STD = 0x1E V_FREQ = 0x3	PRIM_MODE = 0x6 VID_STD = 0x2
35, 36	2880 × 480p @ 60 Hz	3	PRIM_MODE = 0x5 VID_STD = 0xA	PRIM_MODE = 0x6 VID_STD = 0x2
37, 38	2880 × 576p @ 60 Hz	3	PRIM_MODE = 0x5 VID_STD = 0xA	PRIM_MODE = 0x6 VID_STD = 0x2
N/A	SVGA 800 × 600p @ 56 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x0
N/A	SVGA 800 × 600p @ 60 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x1
N/A	SVGA 800 × 600p @ 72 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x2
N/A	SVGA 800 × 600p @ 75 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x3
N/A	SVGA 800 × 600p @ 85 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x04
N/A	SXGA 1280 × 1024p @ 60 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x05
N/A	SXGA 1280 × 1024p @ 75 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x06
N/A	VGA 640 × 480p @ 60 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x08
N/A	VGA 640 × 480p @ 72 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x09
N/A	VGA 640 × 480p @ 75 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x0A
N/A	VGA 640 × 480p @ 85 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x0B
N/A	VGA 1024 × 768p @ 60 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x0C
N/A	VGA 1024 × 768p @ 70 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x0D
N/A	VGA 1024 × 768p @ 75 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x0E
N/A	VGA 1024 × 768p @ 85 Hz	0	PRIM_MODE = 0x06 VID_STD = 0x0	PRIM_MODE = 0x06 VID_STD = 0x0F

PIXEL PORT CONFIGURATION

The ADV7619 has a very flexible pixel port, which can be configured in a variety of formats to accommodate downstream ICs. The ADV7619 can provide output modes up to 36 bits for video with pixel clock frequency below 170 MHz, and 48 bits for video with pixel rates above 170 MHz.

For an HDMI stream with bit pixel rates above 170 MHz, ADV7619 outputs data using two video buses running at half the video pixel clock frequency. Video data is interleaved. On a single clock edge, the first bus outputs information about odd pixels and the second video bus outputs information about even pixels. Video output modes for pixel rates above 170 MHz are shown in Table 83.

This section details the controls required to configure the ADV7619 pixel port. Appendix C contains tables describing some of the pixel port configurations.

PIXEL PORT OUTPUT MODES

OP_FORMAT_SEL[7:0], IO, Address 0x03[7:0]

A control to select the data format and pixel bus configuration. Refer to the Appendix for full information on pixel port modes and configuration settings.

Function

OP_FORMAT_SEL[7:0]	Description
0x00 «[1]	8-bit SDR ITU-656 mode
0x01[1]	10-bit SDR ITU-656 mode
0x02[1]	12-bit SDR ITU-656 Mode 0
0x06[1]	12-bit SDR ITU-656 Mode 1
0x0A	12-bit SDR ITU Mode 2
0x20	8-bit 4:2:2 DDR Mode
0x21	10-bit 4:2:2 DDR Mode
0x22	12-bit 4:2:2 DDR Mode 0
0x23	12-bit 4:2:2 DDR Mode 1
0x24	12-bit 4:2:2 DDR Mode 2
0x40	24-bit 4:4:4 SDR Mode
0x41	30-bit 4:4:4 SDR Mode
0x42	36-bit 4:4:4 SDR Mode 0
0x46	36-bit SDR 4:4:4 Mode 1
0x4C	24-bit SDR 4:4:4 Mode 3
0x50	24-bit SDR 4:4:4 Mode 4
0x51	30-bit SDR 4:4:4 Mode 4
0x52	36-bit SDR 4:4:4 Mode 4
0x54[2]	2 × 24-bit SDR 4:4:4 interleaved Mode 0
0x60	24-bit 4:4:4 DDR mode
0x61	30-bit 4:4:4 DDR mode
0x62	36-bit 4:4:4 DDR mode
0x80	16-bit ITU-656 SDR mode
0x81	20-bit ITU-656 SDR mode
0x82	24-bit ITU-656 SDR Mode 0
0x86	24-bit ITU-656 SDR Mode 1
0x8A	24-bit ITU-656 SDR Mode 2
0x90	16-bit SDR 4:2:2 Mode 4
0x94[2]	2 × 16-bit SDR 4:2:2 interleaved Mode 0
0x95[2]	2 × 20-bit SDR 4:2:2 interleaved Mode 0
0x96[2]	2 × 24-bit SDR 4:2:2 interleaved Mode 0

[1] Refer to DLL Settings for 656, 8-/10-/12-Bit Modes in chapter DLL on LLC Clock Path.
[2] The 0x54, 0x94, 0x95, 0x96 modes registers should be set as follows:
DPLL Map, Register 0xC3 to Register 0x80.
DPLL Map, Register 0xCF to Register0x03.
IO Map, Register 0xDD to Register 0xA0.
IO Map, Register 0xBF[0] = 0 (CP_COMPLETE_BYPASS_IN_HDMI_MODES disabled).

Bus Rotation and Reordering Controls

Bus reordering controls are available for ADV7619. OP_CH_SEL[2:0] allows the three output buses to be rearranged, thus providing six different output possibilities.

OP_CH_SEL[2:0], IO, Address 0x04[7:5]

A control to select the configuration of the pixel data bus on the pixel pins. Refer to the pixel port configuration for full information on pixel port modes and configuration settings.

Function

OP_CH_SEL[2:0]	Description
000	P[35:24] Y/G, P[23:12] U/CrCb/B, P[11:0] V/R
001	P[35:24] Y/G, P[23:12] V/R, P[11:0] U/CrCb/B
010	P[35:24] U/CrCb/B, P[23:12] Y/G, P[11:0] V/R
011 (default)	P[35:24] V/R, P[23:12] Y/G, P[11:0] U/CrCb/B
100	P[35:24] U/CrCb/B, P[23:12] V/R, P[11:0]Y/G
101	P[35:24] V/R, P[23:12] U/CrCb/B, P[11:0] Y/G
110	Reserved
111	Reserved

PIXBUS_MSB_TO_LSB_REORDER, IO, Address 0x30[4]

A control to swap the MSB to LSB orientation on the pixel bus.

Function

PIXBUS_MSB_TO_LSB_REORDER	Description
0 (default)	Output bus goes from MSB to LSB
1	Output bus goes from LSB to MSB

Pixel Data and Synchronization Signals Control

The polarity of the LLC and synchronization signals can be inverted, and the LLC, the synchronization signals, and the pixel data output can be tristated. Refer to the information on the following controls:

- **INV_F_POL**
- **INV_VS_POL**
- **INV_HS_POL**
- **TRI_PIX**
- **TRI_LLC**
- **TRI_SYNCS**

OP_SWAP_CB_CR, IO, Address 0x05[0]

A controls the swapping of Cr and Cb data on the pixel buses.

Function

OP_SWAP_CB_CR	Description
0 (default)	Outputs Cr and Cb as per OP_FORMAT_SEL
1	Inverts the order of Cb and Cr in the interleaved data stream

OP_SWAP_CB_CR swaps the order in which Cb and Cr are interleaved in the output data stream. It caters for cases in which the data on Channels B and C are swapped. It is effective only if OP_FORMAT_SEL[7:0] is set to a 4:2:2 compatible output mode.

Note: It has no effect for 36-bit SDR modes and DDR modes.

DDR OUTPUT INTERFACE

The ADV7619 allows data to be output in a DDR mode only for modes below 2.25GBps. To enable DDR mode - **OP_FORMAT_SEL[7:0]** should be set to one of DDR modes. Refer also to Pixel Output Formats section.

Important: The maximum frequency of the DDR clock supported by the ADV7844 is 50 MHz. The DDR clock is output through the LLC pin.

LLC CONTROLS

The ADV7619 has a number of adjustment features available for the line locked clock (LLC) output. The polarity of the LLC can be inverted and the LLC of the output driver can be tristated. Controls also exist to skew the LLC versus the output data to achieve suitable setup and hold times for any back end device. The LLC controls are as follows:

- **INV_LLC_POL**
- **TRI_LLC**
- **LLC_DLL_EN**
- **LLC_DLL_MUX**
- **LLC_DLL_PHASE[4:0]**

DLL ON LLC CLOCK PATH

A delay locked loop (DLL) block is implemented on the LLC clock path. This DLL allows the changing of the phase of the output pixel clock on the LLC pin.

Adjusting DLL Phase in All Modes

LLC_DLL_EN, IO, Address 0x19[7]

A control to enable the DLL for the output pixel clock.

Function

LLC_DLL_EN	Description
1	Enables LLC DLL
0 (default)	Disables LLC DLL

LLC_DLL_MUX, IO, Address 0x33[6]

A control to apply the pixel clock DLL to the pixel clock output on the LLC pin.

Function

LLC_DLL_MUX	Description
0 (default)	Bypasses the DLL
1	Muxes the DLL output on LLC output

LLC_DLL_PHASE[4:0], IO, Address 0x19[4:0]

A control to adjust LLC DLL phase in increments of 1/32 of a clock period.

Function

LLC_DLL_PHASE[4:0]	Description
00000 (default)	Default
xxxxx	Sets one of 32 phases of DLL to vary LLC CLK

LLC_DLL_DOUBLE, IO, 0x19[6]: Doubles LLC frequency.

Function

LLC_DLL_DOUBLE[6]	Description
0 (default)	Normal LLC Frequency
1	Double LLC Frequency

DLL Settings for 656, 8-/10-/12-Bit Modes

Table 8 and Table 9 show the settings that must be used to enable 8-/10-/12-bit, 656 output. Note that the 720p 8-/10-/12-bit mode must use OP_FORMAT_SEL = 0x20 or 0x2A (refer to Table 76). Doubling the clock as per Table 8 undoes the DDR mode.

Table 8. DLL Settings for 8-/12-Bit Pixel Bus Output

Address	Setting	Description
IO Map Address 0x03[7:0]	Refer to Table 9	OP_FORMAT_SEL value
IO Map Address 0x19[7]	1	Enables LLC DLL
IO Map Address 0x33[6]	1	Muxes the DLL output on LLC output
IO Map Address 0x19[6]	1	Doubles the clock

Table 9. OP_FORMAT_SEL Settings for 8-/12-Bit Pixel Bus Output (To Be Used with Settings From Table 8)

Input video	OP_FORMAT_SEL Value	Output clock frequency after clock doubling
480i, 576i 8-bit	0x00	27 MHz
480i, 576i 10-/12-bit	0x0A	27 MHz
480p, 576p 8-bit	0x00	54 MHz
480p, 576p 10-/12-bit	0x0A	54 MHz
720p 8-bit	0x20	148.5 MHz
720p 10-/12-bit	0x2A	148.5 MHz

HDMI RECEIVER

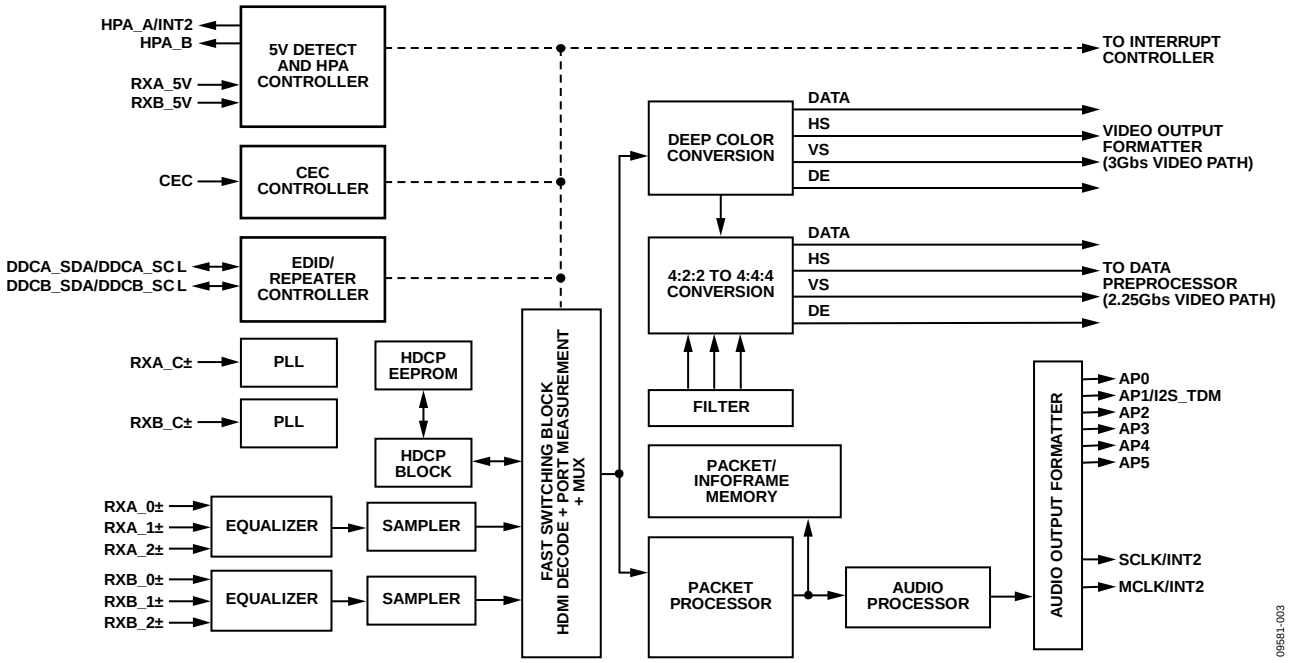


Figure 4. Functional Block Diagram of HDMI Core

ADV7619 feature HDMI 1.4a compliant HDMI Receiver capable to support HDMI stream with bit rate up to 3 Gbs. HDMI stream with bit rate below 2.25 Gbs is receiver and can be processes by CP core, where HDMI stream with bit rates above 2.25 Gbs and below 3 Gbs is directly output to OUTPUT DATA FORMATTER. These two video paths: 2.25 Gbs and 3 Gbs are shown in Figure 4.

+5 V CABLE DETECT

The HDMI receiver in the ADV7619 can monitor the level on the +5 V power signal pin of each connected HDMI port. The results of this detection can be read back from the following I²C registers. These readbacks are valid even when the part is not configured for HDMI mode.

CABLE_DET_A_RAW, IO, Address 0x6F[0] (Read Only)

Raw status of Port A +5 V cable detection signal.

Function

CABLE_DET_A_RAW	Description
0 (default)	No cable detected on Port A
1	Cable detected on Port A (high level on RXA_5V)

CABLE_DET_B_RAW, IO, Address 0x6A[7] (Read Only)

Raw status of Port B +5 V cable detection signal.

Function

CABLE_DET_B_RAW	Description
0 (default)	No cable detected on Port B
1	Cable detected on Port B (high level on RXB_5V)

The ADV7619 provides a digital glitch filter on the +5 V power signals from the HDMI port. The output of this filter is used to reset the HDMI block (refer to the HDMI Section Reset Strategy section).

The +5 V power signal must be constantly high for the duration of the timer (controlled by **FILT_5V_DET_TIMER[6:0]**), otherwise the output of the filter is low. The output of the filter returns low as soon as any change in the +5 V power signal is detected.

FILT_5V_DET_DIS, Addr 68 (HDMI), Address 0x56[7]

This control is used to disable the digital glitch filter on the HDMI 5 V detect signals. The filtered signals are used as interrupt flags and used to reset the HDMI section. The filter works from an internal ring oscillator clock and, therefore, is available in power-down mode. The clock frequency of the ring oscillator is 42 MHz ± 10%.

Function

FILT_5V_DET_DIS	Description
0 (default)	Enabled
1	Disabled

Note: If the +5 V pins are not used and are left unconnected, the +5 V detect circuitry must be disconnected from the HDMI reset signal by setting **DIS_CABLE_DET_RST** to 1. This avoids holding the HDMI section in reset.

FILT_5V_DET_TIMER[6:0], Addr 68 (HDMI), Address 0x56[6:0]

This control is used to set the timer for the digital glitch filter on the HDMI +5 V detect inputs. The unit of this parameter is two clock cycles of the ring oscillator (~ 47 ns). The input must be constantly high for the duration of the timer; otherwise, the filter output remains low. The output of the filter returns low as soon as any change in the +5 V power signal is detected.

Function

FILT_5V_DET_TIMER[6:0]	Description
1011000 (default)	Approximately 4.2 µs
xxxxxxx	Time duration of +5 V deglitch filter. Unit of this parameter is 2 clock cycles of the ring oscillator (~47 ns)

DIS_CABLE_DET_RST, Addr 68 (HDMI), Address 0x48[6]

This control disables the reset effects of cable detection. DIS_CABLE_DET_RST must be set to 1 if the +5 V pins are unused and left unconnected.

Function

DIS_CABLE_DET_RST	Description
0 (default)	Resets HDMI section if 5 V input pin corresponding to selected HDMI port (for example, RXA_5V for Port A) is inactive
1	Does not use 5 V input pins as reset signal for HDMI section

HOT PLUG ASSERT

The ADV7619 features hot plug assert (HPA) control for its HDMI port. The purpose of the control and its corresponding output pin is to communicate to an HDMI transmitter that it is possible to access the enhanced-extended display identification (E-EDID) connected to the DDC bus.

HPA_MANUAL, Addr 68 (HDMI), Address 0x6C[0]

Manual control enable for the HPA output pins. Automatic control of these pins is disabled by setting this bit. Manual control is determined by the HPA_MAN_VALUE_X (where X = A or B).

Function

HPA_MANUAL	Description
0 (default)	HPA takes its value based on HPA_AUTO_INT_EDID
1	HPA takes its value from HPA_MAN_VALUE_X

HPA_MAN_VALUE_A, IO, Address 0x20[7]

A manual control for the value of HPA on Port A. Valid only if HPA_MANUAL is set to 1.

Function

HPA_MAN_VALUE_A	Description
0	0 V applied to HPA_A pin
1 (default)	High level applied to HPA_A pin

HPA_MAN_VALUE_B, IO, Address 0x20[6]

A manual control for the value of HPB on Port A. Valid only if HPA_MANUAL is set to 1.

Function

HPA_MAN_VALUE_B	Description
0	0 V applied to HPA_B pin
1 (default)	High level applied to HPA_B pin

Note: The HPA_A and HPA_B pins is open drain. An external pull-up resistor is required to pull it high.

HPA_AUTO_INT_EDID[1:0], Addr 68 (HDMI), Address 0x6C[2:1]

This control selects the type of automatic control on the HPA output pins. This bit has no effect when HPA_MANUAL is set to 1.

Function

HPA_AUTO_INT_EDID[1:0]	Description
00	HPA of an HDMI port asserted high immediately after internal EDID activated for that port. HPA of a specific HDMI port deasserted low immediately after internal E-EDID is de-activated for that port.
01 (default)	HPA of an HDMI port asserted high following a programmable delay after part detects an HDMI cable plug on that port. HPA of an HDMI port immediately deasserted after part detects a cable disconnect on that HDMI port.
10	HPA of an HDMI port asserted high after two conditions met. 1. Internal EDID is active for that port. 2. Delayed version of cable detect signal CABLE_DET_X_RAW for that port is high. HPA of an HDMI port immediately deasserted after either of these two conditions are met: 1. Internal EDID is de-activated for that port. 2. Cable detect signal CABLE_DET_X_RAW for that port is low.
11	HPA of an HDMI port is asserted high after three conditions met: 1. Internal EDID is active for that port. 2. Delayed version of cable detect signal CABLE_DET_X_RAW for that port is high. 3. User has set manual HPA control for that port to 1 via HPA_MAN_VALUE_X controls. HPA of an HDMI port immediately deasserted after any of these three conditions met: 1. Internal EDID de-activated for that port. 2. Cable detect signal CABLE_DET_X_RAW for that port is low. 3. User sets the manual HPD control for that port to 0 via HPA_MAN_VALUE_X controls

Note: The delay is programmable via **HPA_DELAY_SEL[3:0]**. Refer to EDID_ENABLE for details on enabling the internal E-EDID for an HDMI port. In HPA_MAN_VALUE_X and CABLE_DET_X_RAW, X refers to A and B.

HPA_DELAY_SEL[3:0], Addr 68 (HDMI), Address 0x6C[7:4]

Sets a delay between +5 V detection and hot plug assertion on the HPA output pins, in increments of 100 ms per bit.

Function

HPA_DELAY_SEL[3:0]	Description
0000	No delay
0001	100 ms delay
0010	200 ms delay
1010 (default)	1 sec delay
1111	1.5 sec delay

HPA_TRISTATE_A, IO, Address 0x20[3]

Tristates HPA output pin for Port A.

Function

HPA_TRISTATE_A	Description
0 (default)	HPA_A pin active
1	Tristates HPA_A pin

HPA_TRISTATE_B, IO, Address 0x20[2]

Tristates HPA output pin for Port B.

Function

HPA_TRISTATE_B	Description
0 (default)	HPA_B pin active
1	Tristates HPA_B pin

HPA_STATUS_PORT_A, IO, Address 0x21[3] (Read Only)

Readback of HPA status for Port A.

Function

HPA_STATUS_PORT_A	Description
0 (default)	+5 V not applied to HPA_A pin by chip
1	+5 V applied to HPA_A pin by chip

HPA_STATUS_PORT_B, IO, Address 0x21[2] (Read Only)

Readback of HPA status for Port B.

Function

HPA_STATUS_PORT_B	Description
0 (default)	+5 V not applied to HPA_B pin by chip
1	+5 V applied to HPA_B pin by chip

HPA_OVR_TERM, Addr 68 (HDMI), Address 0x6C[3]

A control to set the termination control to be overridden by the HPA setting. When this bit is set, termination on a specific port is set according to the HPA status of that port.

Function

HPA_OVR_TERM	Description
0 (default)	Automatic or manual I²C control of port termination
1	Termination controls disabled and overridden by HPA controls

E-EDID/REPEATER CONTROLLER

The HDMI section incorporates an E-EDID/repeater controller, which performs the following tasks:

- Computes the E-EDID checksum for each port
- Performs the repeater routines described in the Repeater Support section

The E-EDID/repeater controller is powered from the DVDD supply and clocked by an internal ring oscillator. The controller and the internal DDC bus arbiter are kept active in power-down Mode 0 and power-down Mode 1. This allows the internal E-EDID to be functional and accessible through the DDC port, even when the part is powered down (refer to the Power-Down Modes section). These HDMI transmitters can then read the capabilities of the powered-down application integrating the ADV7619 by accessing its internal E-EDID through the DDC ports.

The E-EDID/repeater controller is reset when the DVDD supplies go low or when **HDCP_REPT_EDID_RESET** is set high. When the E-EDID/repeater controller reboots, it performs the following tasks:

- Clears the internal E-EDID and Key Selection Vector (KSV) RAM (refer to E-EDID Data Configuration section and the Internal HDCP Key OTP ROM section)
- Computes a checksums for two ports (refer to the Structure of Internal E-EDID for Port B section)
- Updates the SPA registers

HDCP_REPT_EDID_RESET, Addr 68 (HDMI), Address 0x5A[3] (Self-Clearing)

A reset control for the E-EDID/repeater controller. When asserted, it resets the E-EDID/repeater controller.

Function

HDCP_REPT_EDID_RESET	Description
0 (default)	Normal operation
1	Resets the E-EDID/repeater controller

E-EDID DATA CONFIGURATION

The ADV7619 features a RAM that can store an E-EDID. This internal E-EDID feature can be used for both HDMI ports A and B.

The following controls are provided to enable the internal E-EDID for each of the two HDMI ports.

EDID_A_ENABLE, Addr 64 (Repeater), Address 0x74[0]

Enables I²C access to the internal EDID RAM from DDC Port A.

Function

EDID_A_ENABLE	Description
0 (default)	Disables E-EDID for Port A
1	Enables E-EDID for Port A

EDID_B_ENABLE, Addr 64 (Repeater), Address 0x74[1]

Enables I²C access to the internal EDID RAM from DDC Port B.

Function

EDID_B_ENABLE	Description
0 (default)	Disables E-EDID for Port B
1	Enables E-EDID for Port B

When the internal E-EDID is enabled on either port, the ADV7619 must first calculate the E-EDID checksums for that port before the E-EDID is actually enabled.

EDID_A_ENABLE_CPU, Addr 64 (Repeater), Address 0x76[0] (Read Only)

Flags internal EDID enabling on Port A.

Function

EDID_A_ENABLE_CPU	Description
0 (default)	Disabled
1	Enabled

EDID_B_ENABLE_CPU, Addr 64 (Repeater), Address 0x76[1] (Read Only)

Flags internal EDID enabling on Port B.

Function

EDID_B_ENABLE_CPU	Description
0 (default)	Disabled
1	Enabled

Notes

- When the internal E-EDID is enabled on more than one port (such as Port A and Port B), the corresponding enable controls (such as **EDID_A_ENABLE** and **EDID_B_ENABLE**) should be set high in one single I²C write. This ensures the fastest calculation of the checksums.
- If the internal E-EDID RAM is enabled for one specific port (such as Port A), an external E-EDID storage device must not be connected on the DDC bus of that port.
- The internal E-EDID can be read by current address read sequences on the DDC port.
- The ADV7619 supports the segment pointer, which is set at device address 0x60 through the DDC bus, and used in combination with the internal E-EDID address (0xA0) to access the internal E-EDID.
- The contents of the EDID RAM are not to be trusted after power up or hardware reset. User should write proper contents to the EDID RAM memory inside the ADV7619 via an external MCU.

E-EDID Support for Power-Down Modes

The ADV7619 supports E-EDID access in Power-Down Mode 0 and Power-Down Mode 1. Using this feature, an application that integrates the ADV7619 in standby can make its E-EDID available to the HDMI transmitter. This allows support of CEC and provides compatibility with HDMI transmitters that require the E-EDID to be available when the HDMI receiver is powered down.

In Power-Down Mode 0, the part operates in a very low power state with only the minimum of internal circuitry enabled for the internal E-EDID.

For more details on E-EDID accessibility in power-down modes, refer to the Power-Down Modes section.

TRANSITIONING OF POWER MODES

If the part starts in Power-Down Mode 0 and then transitions into a different power mode (that is, Power-Down Mode 1 or normal operation mode), the information in the internal E-EDID is not overwritten. The internal E-EDID remains active on the HDMI port for which the E-EDID has been accessed. This prevents disturbing E-EDID read requests from HDMI sources connected to the ADV7619 while it is being powered on, or while the power mode is transitioning.

It is possible to disable the automatic enable of internal EDID on the HDMI ports when the part comes out of power-down mode, by setting the DISABLE_AUTO_EDID bit.

DISABLE_AUTO_EDID, Addr 64 (Repeater), Address 0x7A[1]

Disables all automatic enables for internal E-EDID.

Function

DISABLE_AUTO_EDID	Description
0 (default)	Automatic enable of internal E-EDID on HDMI port when the part comes out of Power-Down Mode 0
1	Disable automatic enable of internal E-EDID on HDMI port when the part comes out of Power-Down Mode 0

STRUCTURE OF INTERNAL E-EDID FOR PORT A

The internal E-EDID is enabled on Port A by setting **EDID_A_ENABLE** to 1. The structure of the internal E-EDID that is accessible on the DDC line of Port A is shown in Figure 5. The image of the internal E-EDID that is accessed on the DDC bus of Port A corresponds to the data image contained in the internal E-EDID RAM.

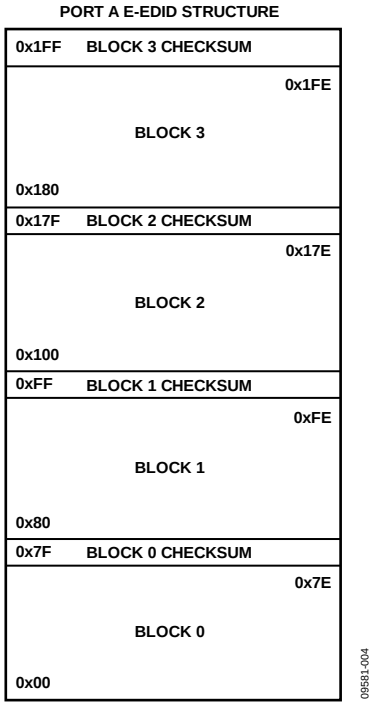


Figure 5. Port A E-EDID Structure and Mapping

Notes

- After **EDID_A_ENABLE** is set to 1, the ADV7619 E-EDID/Repeater controller calculates the four checksums of the E-EDID image for Port A and updates the internal RAM address locations 0x7F, 0xFF, 0x17F, and 0x1FF in the internal E-EDID RAM with the computed checksums.
- After power up, the ADV7619 E-EDID/Repeater controller sets all bytes in the internal E-EDID RAM to 0, this operation takes less than 1 ms. It is recommended to wait for at least 1 ms before initializing the EDID map with an E-EDID image.
- When internal E-EDID is enabled on Port A, the hot plug should not be asserted until the EDID map has been completely initialized with E-EDID.
- The internal E-EDID can be accessed in read-only mode through the DDC interface at the I^2C address 0xA0.
- The internal E-EDID can be accessed in read/write mode through the general I^2C interface at the EDID map I^2C address.

STRUCTURE OF INTERNAL E-EDID FOR PORT B

This section describes the structure of the internal E-EDID accessible through the DDC bus of Port B.

The internal E-EDID is enabled for Port B by setting the **EDID_B_ENABLE** bit to 1. The image of the internal E-EDID that is accessed on the DDC bus of Port B corresponds to the data image contained in the internal E-EDID RAM except for the SPA, SPA location, and the checksum of the E-EDID block where the SPA is located.

The structure of the internal E-EDID image for Port B is shown in the following figures:

- Figure 6—SPA located in E-EDID Block 1
- Figure 7—SPA located in E-EDIDBlock 2
- Figure 8—SPA located in E-EDIDBlock 3

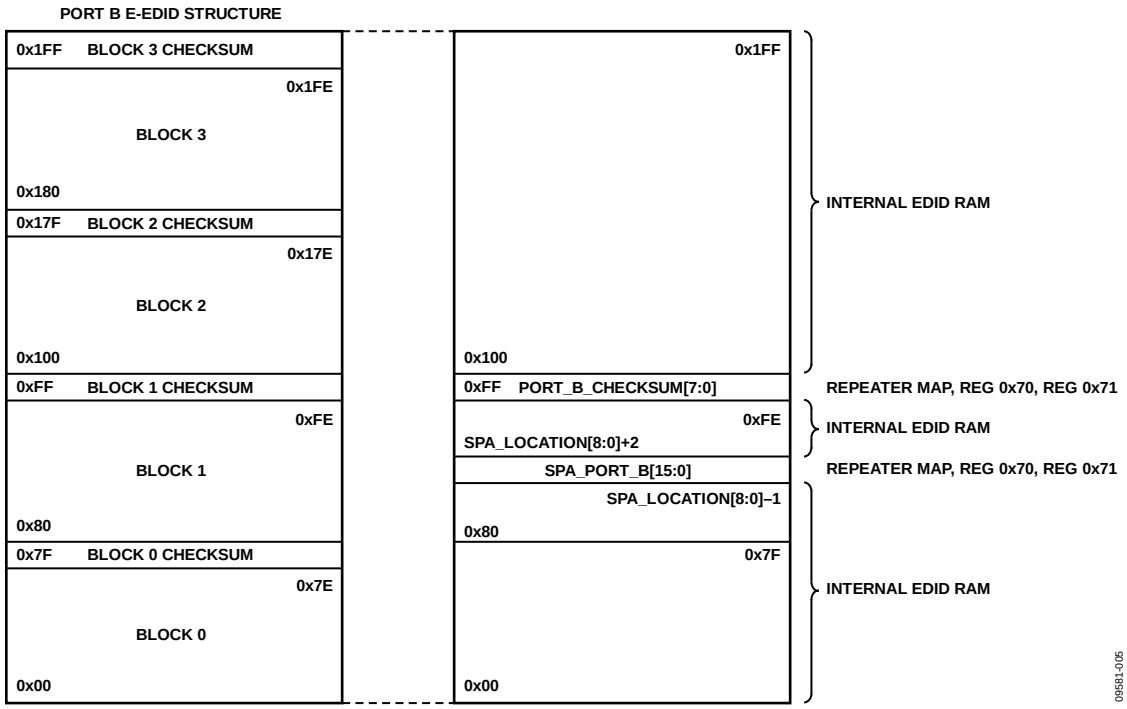


Figure 6. Port B E-EDID Structure and Mapping for SPA Located in E-EDID Block 1

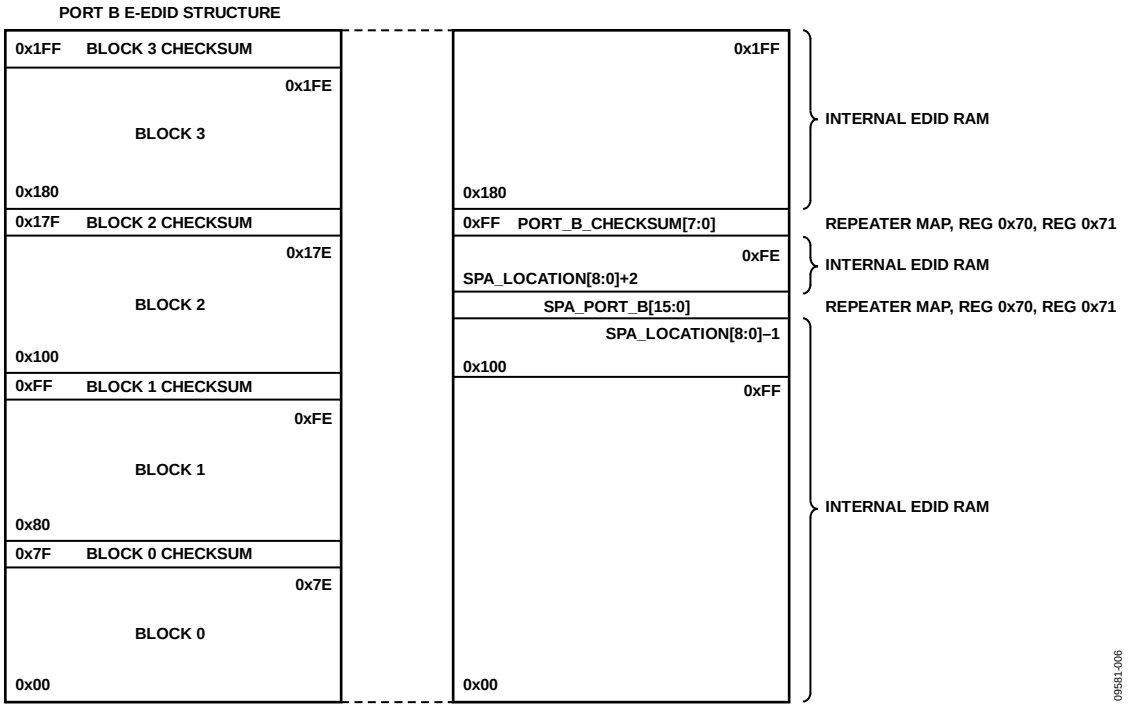


Figure 7. Port B E-EDID Structure and Mapping for SPA Located in E-EDID Block 2

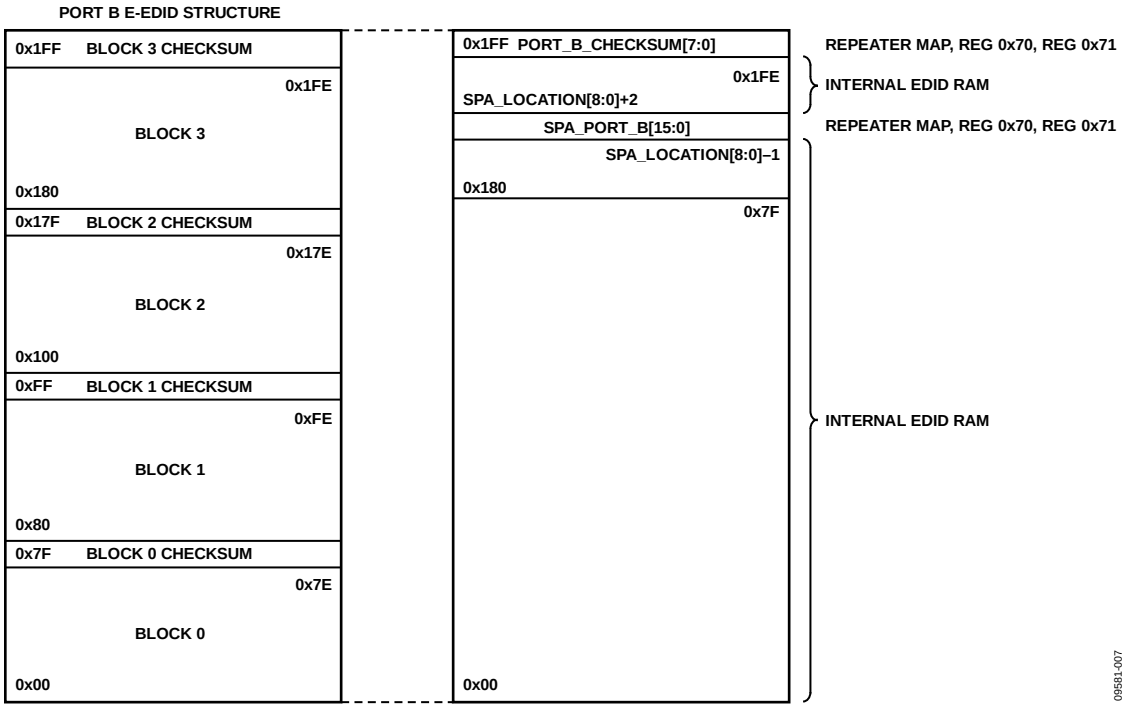


Figure 8. Port B E-EDID Structure and Mapping for SPA Located in E-EDID Block 3

The SPA of Port B is programmed in the **SPA_PORT_B[15:0]** register. The SPA location is programmed in the **SPA_LOCATION[7:0]** register. This register should contain a value greater than 0x7F since the SPA is located in an upper block of the E-EDID.

Notes

- When internal E-EDID is required for Port B, the SPA along with its location address in the E-EDID must be programmed in the Repeater Map, registers **SPA_PORT_B[15:0]**and **SPA_LOCATION[7:0],** respectively.
- Afte**r EDID_B_ENABLE** is set to 1, the ADV7619 EDID/Repeater controller computes the four checksums of the E-EDID image for Port B. The E-EDID controller then updates the checksum registers in the EDID RAM memory location 0x7F and the following three locations:
  - 0x17F, 0x1FF, and the register SPA_LOCATION[7:0], which is the SPA located in the EDID Block 1
  - 0xFF, 0x1FF, and the register SPA_LOCATION[7:0], which is the SPA located in the EDIDBlock 2
  - 0xFE, 0x17F, and the register SPA_LOCATION[7:0], which is the SPA located in the EDIDBlock 3
- After power up, the ADV7619 E-EDID controller sets all bytes in the internal EDID RAM to 0; this operation takes less than 1 ms. It is recommended to wait for at least 1 ms before initializing the EDID map with E-EDID.
- **SPA_LOCATION[7:0]** must be programmed with a value greater than 0x7F, as SPA is always located in the E-EDID Blocks 1, 2 or 3.
- When internal E-EDID is enabled on Port B, the hot plug should not be asserted until the EDID map has been completely initialized with E-EDID.
- The internal E-EDID can be accessed in read-only mode through the DDC interface at the I^2C address 0xA0.
- The internal E-EDID can be accessed in read/write mode through the general I^2C interface at the EDID map I^2C address.
- The **SPA_PORT_B[15:0]** register does not have to be programmed with an actual SPA value. It can be programmed with any value that must be read from the location **SPA_LOCATION[7:0]** when the internal E-EDID is accessed from the DDC lines of Port B. This allows support for non-CEA-861 compliant E-EDIDs (that is, VESA-only compliant E-EDID for analog inputs).

The SPA of Port B is the address of the Port B in the CEC interface. The SPA is comprised of four components, A, B, C, and D, as defined in the HDMI specification, which are programmed as follows:

- SPA_PORT_B[15:12] = A
- SPA_PORT_B[11:8] = B
- SPA_PORT_B[7:4] = C
- SPA_PORT_B[3:0] = D

SPA_PORT_B[15:0], Addr 64 (Repeater), Address 0x52[7:0]; Address 0x53[7:0]

Source Physical Address for Port B. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID.

Function

SPA_PORT_B[15:0]	Description
0000000000000000 (default)	Default value
xxxxxxxxxxxxxxxx	Source physical address of Port B

SPA_LOCATION[7:0], Addr 64 (Repeater), Address 0x70[7:0]

This is the location in the E-EDID record where the SPA is located.

Function

SPA_LOCATION[7:0]	Description
11000000 (default)	Default value
xxxxxxxx	Location of source physical address in internal E-EDID of Port B

PORT_B_CHECKSUM[7:0], Addr 64 (Repeater), Address 0x61[7:0]

This is the checksum for the second half of the Port B EDID. This is calculated automatically.

Function

PORT_B_CHECKSUM[7:0]	Description
xxxxxxxx	Checksum for E-EDID block containing SPA for Port B
00000000 (default)	Default value

TMDS EQUALIZATION

The ADV7619 incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at long lengths and higher frequencies. The ADV7619 is capable of equalizing for cable lengths up to 30 meters and for pixel clock frequencies up to 300 MHz.

Note that transition minimized differential signaling (TMDS) equalization frequency of the active HDMI port can be read back in the **TMDSFREQ[8:0]** and **TMDSFREQ_FRAC[6:0]** registers.

PORT SELECTION

HDMI_PORT_SELECT allows the selection of the active HDMI port. This register must be set to activate either HDMI Port A or HDMI Port B.

HDMI_PORT_SELECT[2:0], Addr 68 (HDMI), Address 0x00[2:0]

This two-bit control is used for HDMI primary port selection.

Function

HDMI_PORT_SELECT[2:0]	Description
000 (default)	Port A
001	Port B

FAST SWITCHING AND BACKGROUND PORT SELECTION

The ADV7619 incorporates a fast switching feature. This feature allows the user of a system containing the ADV7619 to seamlessly switch between HDCP encrypted sources. There is no delay in achieving video output which was previously caused by HDCP authentication. The time required to switch between HDMI sources with HDCP encryption is reduced to a fraction of a second.

If an HDMI port is not selected by **HDMI_PORT_SELECT[2:0]** then by default this port is disabled. Asserting **EN_BG_PORT_A** or **EN_BG_PORT_B** allows this unselected port to be enabled in background mode. Once a port is in background mode the ADV7619 establishes a HDCP link with its source even though it is not selected by HDMI_PORT_SELECT[2:0]. This background authentication allows for fast switching of the HDMI ports.

Note that **EN_BG_PORT_A** and **EN_BG_PORT_B** have no effect if the port is selected by HDMI_PORT_SELECT.

EN_BG_PORT_A, Addr 68 (HDMI), Address 0x02[0]

Background mode enable for Port A. Sets Port A in background mode to establish a HDCP link with its source even if the port is not selected by HDMI_PORT_SELECT. This control has no effect if the port is selected by **HDMI_PORT_SELECT[2:0]**.

Function

EN_BG_PORT_A	Description
0 (default)	Port disabled, unless selected with **HDMI_PORT_SELECT[2:0]**
1	Port enabled in background mode.

EN_BG_PORT_B, Addr 68 (HDMI), Address 0x02[1]

Background mode enable for Port B. Sets the Port B in background mode to establish a HDCP link with its source even if the port is not selected by **HDMI_PORT_SELECT[2:0].** This control has no effect if the port is selected by **HDMI_PORT_SELECT[2:0].**

Function

EN_BG_PORT_B	Description
0 (default)	Port disabled, unless selected with **HDMI_PORT_SELECT[2:0]**
1	Port enabled in background mode.

The ADV7619 can also perform HDMI parameter measurements on one background port. The following information can then be read from the background measurement and parameter registers.

- **BG_TMDSFREQ[8:0]**
- **BG_TMDSFREQ_FRAC[6:0]**
- **BG_DEEP_COLOR_MODE[1:0]**
- **BG_PIX_REP[3:0]**
- **BG_PARAM_LOCK**
- **BG_TOTAL_LINE_WIDTH[13:0]**

- **BG_LINE_WIDTH[12:0]**
- **BG_TOTAL_FIELD_HEIGHT[12:0]**
- **BG_FIELD_HEIGHT[12:0]**
- **BG_HDMI_INTERLACED**

BG_MEAS_PORT_SEL[2:0], Addr 68 (HDMI), Address 0x00[5:3]

BG_MEAS_PORT_SEL[2:0] selects a background port on which HDMI measurements are to be made and provided in the background measurement registers. The port in question must be set as a background port in order for this setting to be effective. There is no conflict if this matches the port selected by **HDMI_PORT_SELECT[2:0]**.

Function

BG_MEAS_PORT_SEL[2:0]	Description
000 (default)	Port A
001	Port B

BG_MEAS_REQ, Addr 68 (HDMI), Address 0x5A[5] (Self-Clearing)

This bit must be set to get correct measurements of the selected background port. Setting this control sends a request to update the synchronization parameter measurements of the currently selected background port. The port on which the measurement will be made is selected by **BG_MEAS_PORT_SEL[2:0]**.

Function

BG_MEAS_REQ	Description
0 (default)	No request to update selected background port synchronization parameter measurements
1	Requests an update of the selected background port synchronization parameter measurements

Note: After setting the self clearing **BG_MEAS_REQ** bit, the measurements of the TMDS frequency and video parameters of the background ports are valid when **BG_MEAS_DONE_RAW** goes high.

BG_MEAS_DONE_RAW, IO, Address 0x8D[1] (Read Only)

Status of Background port Measurement completed interrupt signal. When set to 1 it indicates measurements of TMDS frequency and video parameters on the selected background port have been completed. Once set, this bit will remain high until it is cleared via BG_MEAS_DONE_CLR.

Function

BG_MEAS_DONE_RAW	Description
0 (default)	Measurements of TMDS frequency and video parameters of background port not finished or not requested.
1	Measurements of TMDS frequency and video parameters of background port are ready

Note: This bit only informs the user that the measurement is complete and can be read back. One should ensure that **BG_PARAM_LOCK** is asserted so that the background parameter filters are locked and the measurement values are valid.

TMDS CLOCK ACTIVITY DETECTION

The ADV7619 provides circuitry to monitor TMDS clock activity on each of its HDMI ports. The firmware can poll the appropriate registers for TMDS clock activity detection and configure the ADV7619 as desired. TMDS clock detection control is active as soon as the ADV7619 detects activity above a 25 MHz on the TMDS clock input.

TMDS_CLK_A_RAW, IO, Address 0x6A[4] (Read Only)

Raw status of Port A TMDS clock detection signal.

Function

TMDS_CLK_A_RAW	Description
0 (default)	No TMDS clock detected on Port A
1	TMDS clock detected on Port A

TMDS_CLK_B_RAW, IO, Address 0x6A[3] (Read Only)

Raw status of Port B TMDS clock detection signal.

Function

TMDS_CLK_A_RAW	Description
0 (default)	No TMDS clock detected on Port B
1	TMDS clock detected on Port B

Important

- The clock detection flag is valid if the part is powered up or in Power Down Mode 1. Refer to Power-Down Mode 1 section.
- The clock detection flags is valid, irrespective of the mode the part is set into via the PRIM_MODE[3:0] register.

Clock and Data Termination Control

The ADV7619 provides controls for the TMDS clock and data termination on all HDMI ports. The ADV7619 also offers automatic manual termination closure of the selected port, and individual manual control over the HDMI ports.

Note: The clock termination of the port by **HDMI_PORT_SELECT[2:0]** must always be enabled.

Part does not support HDMI streams with clock lower than 25 MHz.

TERM_AUTO, Addr 68 (HDMI), Address 0x01[0]

This bit allows the user to select automatic or manual control of clock termination. If automatic mode termination is enabled, then the termination on the port selected via HDMI_PORT_SELECT[1:0] is enabled. The termination is disabled on all other ports

Function

TERM_AUTO	Description
0 (default)	Disable termination automatic control
1	Enable termination automatic control

Note: To enable the fast switching feature the termination should be set manually for each port. When manual mode is enabled, the termination for each port is set individually by the CLOCK_TERMX_DISABLE control bits (were X = A and B)

CLOCK_TERMA_DISABLE, Addr 68 (HDMI), Address 0x83[0]

Disable clock termination on Port A. Can be used when TERM_AUTO set to 0

Function

CLOCK_TERMA_DISABLE	Description
0	Enable Termination Port A
1 (default)	Disable Termination Port A

CLOCK_TERMB_DISABLE, Addr 68 (HDMI), Address 0x83[1]

Disable clock termination on Port B. Can be used when TERM_AUTO set to 0

Function

CLOCK_TERMB_DISABLE	Description
0	Enable Termination Port B
1 (default)	Disable Termination Port B

HDMI/DVI STATUS BITS

HDMI/DVI status mode is available through HDMI_MODE for active port and BG_HDMI_MODE for background port.

HDMI_MODE, Addr 68 (HDMI), Address 0x05[7] (Read Only)

A readback to indicate whether the stream processed by the HDMI core is a DVI or an HDMI stream.

Function

HDMI_MODE	Description
0 (default)	DVI mode detected
1	HDMI mode detected

BG_HDMI_MODE, Addr 68 (HDMI), Address 0xEB[0] (Read Only)

A readback to indicate whether the stream processed by the HDMI core is a DVI or an HDMI stream.

Function

BG_HDMI_MODE	Description
0 (default)	DVI mode detected
1	HDMI mode detected

VIDEO 3D DETECTION

Status of 3D Video is available through VIDEO_3D_RAW bit.

VIDEO_3D_RAW, IO, Address 0x6A[2] (Read Only)

Raw status of the Video 3D signal.

Function

VIDEO_3D_RAW	Description
0	Video 3D not detected
1	Video 3D detected

TMDS MEASUREMENT

The ADV7619 contains logic that measures the frequency of the TMDS clock transmitted. The TMDS frequency can be read back via the **TMDSFREQ[8:0]** and **TMDSFREQ_FRAC[6:0]** registers.

TMDS Measurement After TMDS PLL

The TMDSFREQ measurement is provided by a clock measurement circuit located after the TMDS PLL. The TMDS PLL must, therefore, be locked to the incoming TMDS clock in order for the TMDSFREQ and TMDSFREQ_FRAC registers to return a valid measurement. The TMDS frequency can be obtained using Equation 1, TMDS Frequency in MHz (Measured after TMDS PLL).

$$F_{TMDS} = TMDSFREQ + \frac{TMDSFREQ\_FRAC}{128} \qquad (1)$$

Notes

- The TMDS PLL lock status can be monitored via TMDS_PLL_LOCKED. Figure 9 shows the algorithm that can be implemented on an external controller to monitor the TMDS clock frequency.
- The TMDS_PLL_LOCKED flag should be considered valid if a TMDS clock is input on the HDMI port selected via **HDMI_PORT_SELECT[2:0]**.
- The NEW_TMDS_FRQ_RAW flag can be used to monitor if the TMDS frequency on the selected HDMI port changes by a programmable threshold.
- The ADV7619 can be configured to trigger an interrupt when the bit **NEW_TMDS_FRQ_RAW** changes from 0 to 1. In that configuration, the interrupt status **NEW_TMDS_FRQ_ST** indicates that **NEW_TMDS_FRQ_RAW** has changed from 0 to 1. Refer to the Interrupts section for additional information on the configuration of interrupts.

TMDSFREQ[8:0], Addr 68 (HDMI), Address 0x51[7:0]; Address 0x52[7] (Read Only)

This register provides a full precision integer TMDS frequency measurement.

Function

TMDSFREQ[8:0]	Description
000000000 (default)	Outputs 9-bit TMDS frequency measurement in MHz
xxxxxxxxx	Outputs 9-bit TMDS frequency measurement in MHz

TMDSFREQ_FRAC[6:0], Addr 68 (HDMI), Address 0x52[6:0] (Read Only)

A readback to indicate the fractional bits of measured frequency of PLL recovered TMDS clock. The unit is 1/128 MHz.

Function

TMDSFREQ_FRAC[6:0]	Description
0000000 (default)	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz
xxxxxxx	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz

BG_TMDSFREQ[8:0], Addr 68 (HDMI), Address 0xE0[7:0]; Address 0xE1[7] (Read Only)

This register provides a precision integer TMDS frequency measurement on the background port selected by **BG_MEAS_PORT_SEL[2:0]**. The value provided is the result of a single measurement of the TMDS PLL frequency in MHz. This value is updated when an update request is made via the **BG_MEAS_REQ** control bit. This measurement is only valid when **BG_PARAM_LOCK** is set to 1.

Function

BG_TMDSFREQ[8:0]	Description
xxxxxxxxx	Outputs 9-bit TMDS frequency measurement in MHz

BG_TMDSFREQ_FRAC[6:0], Addr 68 (HDMI), Address 0xE1[6:0] (Read Only)

This register provides a precision fractional measurement of the TMDS frequency on the background port selected by **BG_MEAS_PORT_SEL[2:0]**. The unit is 1/128 MHz and the value is updated when an update request is made via the **BG_MEAS_REQ** control bit. This measurement is only valid when **BG_PARAM_LOCK** is set to 1.

Function

BG_TMDSFREQ_FRAC[6:0]	Description
xxxxxxx	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz

TMDS_PLL_LOCKED, Addr 68 (HDMI), Address 0x04[1] (Read Only)

A readback to indicate if the TMDS PLL is locked to the TMDS clock input to the selected HDMI port.

Function

TMDS_PLL_LOCKED	Description
0 (default)	The TMDS PLL is not locked.
1	The TMDS PLL is locked to the TMDS clock input to the selected HDMI port.

TMDSPLL_LCK_A_RAW, IO, Address 0x6A[6] (Read Only)

A readback to indicate the raw status of the Port A TMDS PLL lock signal.

Function

TMDSPLL_LCK_A_RAW	Description
0 (default)	TMDS PLL on Port A is not locked.
1	TMDS PLL on Port A is locked to the incoming clock.

TMDSPLL_LCK_B_RAW, IO, Address 0x6A[5] (Read Only)

A readback to indicate the raw status of the Port B TMDS PLL lock signal.

Function

TMDSPLL_LCK_B_RAW	Description
0 (default)	TMDS PLL on Port B is not locked
1	TMDS PLL on Port B is locked to the incoming clock

NEW_TMDS_FRQ_RAW, IO, Address 0x83[1] (Read Only)

Status of new TMDS frequency interrupt signal. When set to 1, it indicates the TMDS Frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0]. Once set, this bit will remain high until it is cleared via NEW_TMDS_FREQ_CLR.

Function

NEW_TMDS_FRQ_RAW	Description
0 (default)	TMDS frequency has not changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI map.
1	TMDS frequency has changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI map.

FREQTOLERANCE[3:0], Addr 68 (HDMI), Address 0x0D[3:0]

Sets the tolerance in MHz for new TMDS frequency detection. This tolerance is used for the audio mute mask MT_MSK_VCLK_CHNG and the HDMI status bit NEW_TMDS_FRQ_RAW.

Function

FREQTOLERANCE[3:0]	Description
0100 (default)	Default tolerance in MHz for new TMDS frequency detection
xxxx	Tolerance in MHz for new TMDS frequency detection

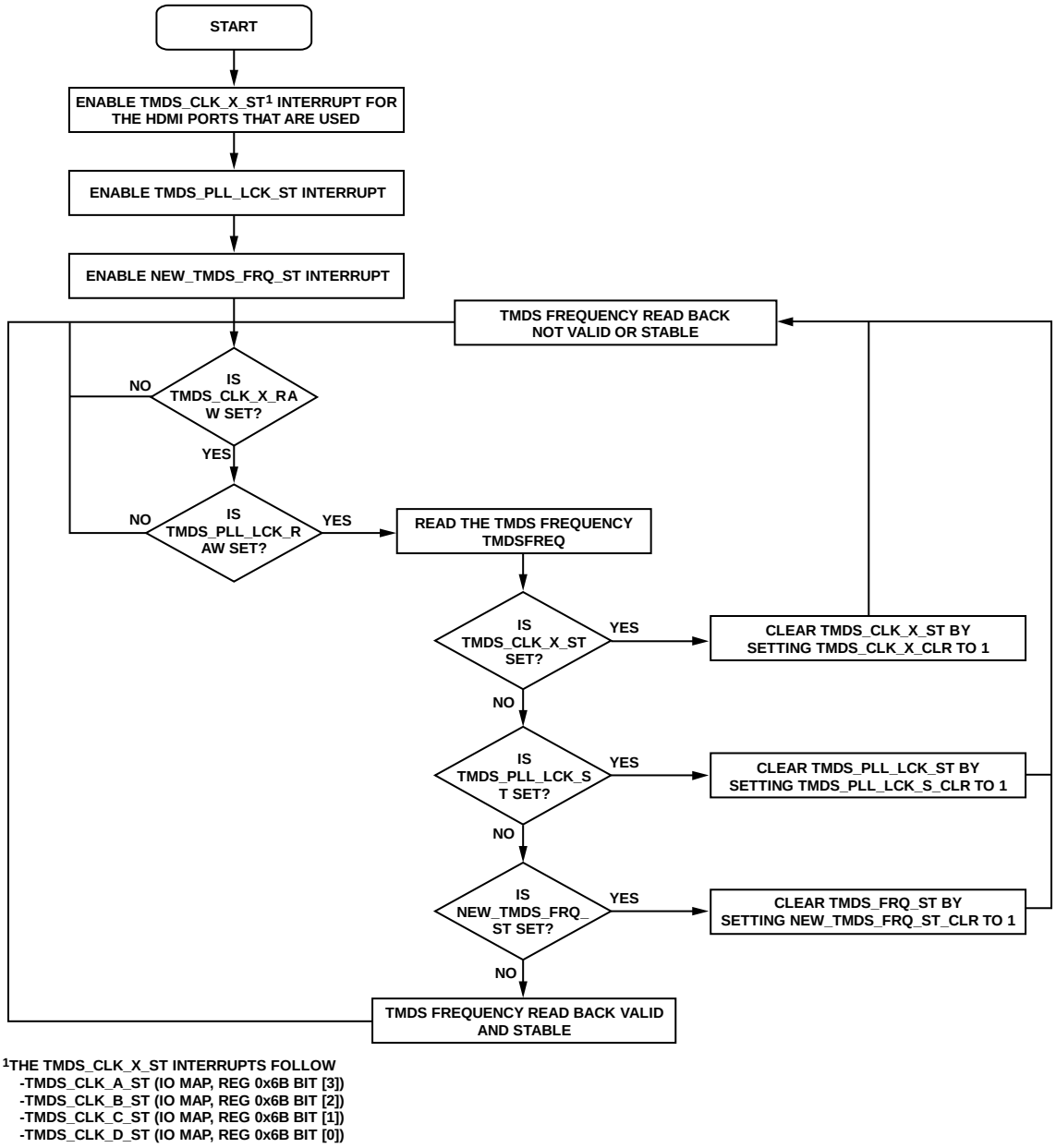


Figure 9. Monitoring TMDS Clock Frequency

DEEP COLOR MODE SUPPORT

The ADV7619 supports HDMI streams with 24 bit per sample and deep color modes of 30 or 36 bits per sample. The addition of a video FIFO (refer to the Video FIFO section) allows for the robust support of these modes.

The deep color mode information that the ADV7619 extracts from the general control packet can be read back from DEEP_COLOR_MODE[1:0]. It is possible to over ride the deep color mode that the ADV7619 unpacks from the video data encapsulated in the processed HDMI stream. This is achieved by configuring the **OVERRIDE_DEEP_COLOR_MODE** and **DEEP_COLOR_MODE_USER[1:0]** controls.

DEEP_COLOR_MODE[1:0], Addr 68 (HDMI), Address 0x0B[7:6] (Read Only)

A readback of the deep color mode information extracted from the general control packet

Function

DEEP_COLOR_MODE[1:0]	Description
00 (default)	8-bits per channel
01	10-bits per channel
10	12-bits per channel
11	16-bits per channel (not supported)

OVERRIDE_DEEP_COLOR_MODE, Addr 68 (HDMI), Address 0x40[6]

A control to override the deep color mode.

Function

OVERRIDE_DEEP_COLOR_MODE	Description
0 (default)	The HDMI section unpacks the video data according to the deep color information extracted from the general control packets (normal operation).
1	Override the deep color mode extracted from the general control packet. The HDMI section unpacks the video data according to the deep color mode set in **DEEP_COLOR_MODE_USER[1:0]**.

DEEP_COLOR_MODE_USER[1:0], Addr 68 (HDMI), Address 0x40[5:4]

A control to manually set the deep color mode. The value set in this register is effective when OVERRIDE_DEEP_COLOR_MODE is set to 1.

Function

DEEP_COLOR_MODE_USER[1:0]	Description
00 (default)	8 bits per channel
01	10 bits per channel
10	12 bits per channel

Notes

- Deep color mode can be monitored via **DEEP_COLOR_CHNG_RAW**, which indicates if the color depth of the processed HDMI stream has changed.
- The ADV7619 can be configured to trigger an interrupt when the DEEP_COLOR_CHNG_RAW bit changes from 0 to 1. In that configuration, the interrupt status DEEP_COLOR_CHNG_ST indicates that DEEP_COLOR_CHNG_RAW has changed from 0 to 1. Refer to the Interrupts section for additional information on the configuration of interrupts.

DEEP_COLOR_CHNG_RAW, IO, Address 0x83[7] (Read Only)

Status of deep color mode changed interrupt signal. When set to 1 it indicates a change in the deep color mode has been detected. Once set, this bit will remain high until it is cleared via DEEP_COLOR_CHNG_CLR.

Function

DEEP_COLOR_CHNG_RAW	Description
0 (default)	Deep color mode has not changed
1	Change in deep color triggered this interrupt

BG_DEEP_COLOR_MODE[1:0], Addr 68 (HDMI), Address 0xEA[3:2] (Read Only)

This readback provides the deep color status for the background HDMI port determined by **BG_MEAS_PORT_SEL[2:0].** The readback provides the HDMI color depth and is updated when an update request is made via the **BG_MEAS_REQ** control bit. This measurement is only valid when **BG_PARAM_LOCK** is set to 1.

Function

BG_DEEP_COLOR_MODE[1:0]	Description
00 (default)	8-bit color per channel
01	10-bit color per channel
10	12-bit color per channel
11	16-bit color per channel (not supported)

VIDEO FIFO

The ADV7619 contains a FIFO located between the incoming TMDS data and the CP core (refer to Figure 10). Data arriving over the HDMI link will be at 1X for non-deep color mode (8 bits per channel), and 1.25X, 1.5X, or 2X for deep color modes (30, 36, and 48 bits, respectively). Data unpacking and data rate reduction must be performed on the incoming HDMI data to provide the CP core with the correct data rate and data bit width. The video FIFO is used to pass data safely across the clock domains.

The video FIFO also provides extreme robustness to jitter on the TMDS clock. The CP clock is generated by a DPLL running on the incoming TMDS clock, and the CP clock may contain less jitter than the incoming TMDS clock. The video FIFO provides immunity to the incoming jitter and the resultant clock phase mismatch between the CP clock and the TMDS clock.

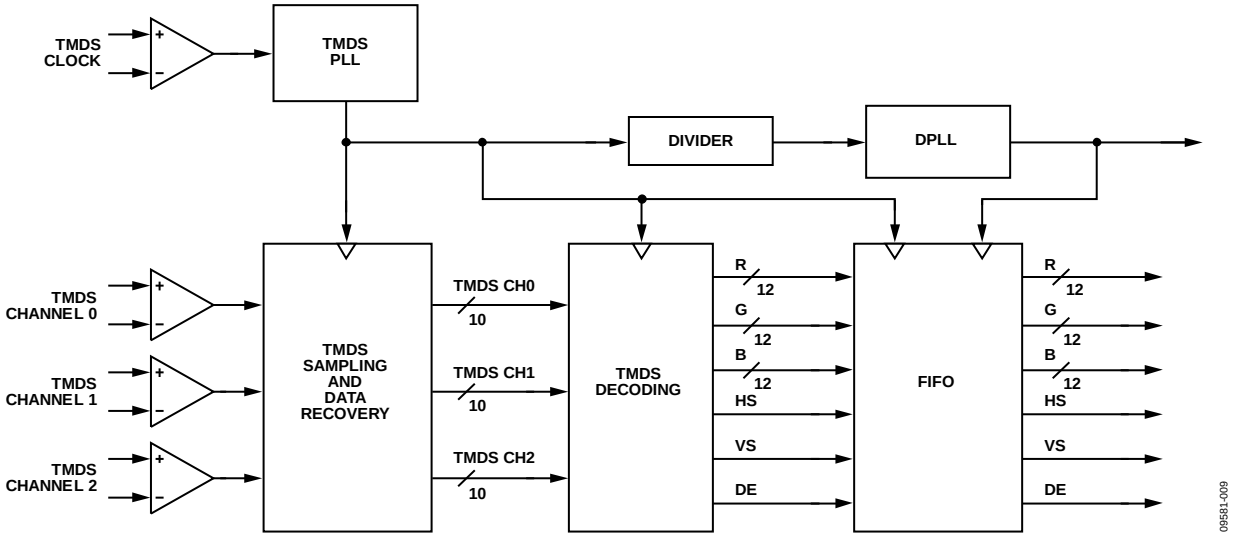


Figure 10. HDMI Video FIFO

The video FIFO is designed to operate completely autonomously. It automatically resynchronizes the read and write pointers if they are about to point to the same location. However, it is also possible for the user to observe and control the FIFO operation with a number of FIFO status and control registers.

For video with pixel clock above 170 MHz DPLL must be bypassed, in that FIFO is clocked by 1x TMDS PLL clock.

DCFIFO_LEVEL[2:0], Addr 68 (HDMI), Address 0x1C[2:0] (Read Only)

A readback that indicates the distance between the read and write pointers. Overflow/underflow would read as Level 0. Ideal centered functionality would read as 0b100.

Function

DCFIFO_LEVEL[2:0]	Description
000 (default)	FIFO has underflowed or overflowed.
001	FIFO is about to overflow.
010	FIFO has some margin.
011	FIFO has some margin.
100	FIFO perfectly balanced
101	FIFO has some margin.
110	FIFO has some margin.
111	FIFO is about to underflow.

DCFIFO_LOCKED, Addr 68 (HDMI), Address 0x1C[3] (Read Only)

A readback to indicate if video FIFO is locked.

Function

DCFIFO_LOCKED	Description
0 (default)	Video FIFO is not locked. Video FIFO had to resynchronize between previous two Vsyncs.
1	Video FIFO is locked. Video FIFO did not have to resynchronize between previous two Vsyncs.

DCFIFO_RECENTER, Addr 68 (HDMI), Address 0x5A[2] (Self-Clearing)

A reset to recenter the video FIFO. This is a self-clearing bit.

Function

DCFIFO_RECENTER	Description
0 (default)	Video FIFO normal operation
1	Video FIFO to recenter

DCFIFO_KILL_DIS, Addr 68 (HDMI), Address 0x1B[2]

The video FIFO output is zeroed if there is more than one resynchronization of the pointers within two FIFO cycles. This behavior can be disabled with this bit.

Function

DCFIFO_KILL_DIS	Description
0 (default)	FIFO output set to zero if more than one resynchronization is necessary during two FIFO cycles
1	FIFO output never set to zero regardless of how many resynchronizations occur

DCFIFO_KILL_NOT_LOCKED, Addr 68 (HDMI), Address 0x1B[3]

DCFIFO_KILL_NOT_LOCKED controls whether or not the output of the Video FIFO is set to zero when the video PLL is unlocked.

Function

DCFIFO_KILL_NOT_LOCKED	Description
0	FIFO data is output regardless of video PLL lock status.
1 (default)	FIFO output is zeroed if video PLL is unlocked.

The DCFIFO is programmed to reset itself automatically when the video PLL transitions from unlocked to locked. Note that the video PLL transition does not necessarily indicate that the overall system is stable.

DCFIFO_RESET_ON_LOCK, Addr 68 (HDMI), Address 0x1B[4]

Enables the reset/recentering of video FIFO on video PLL unlock

Function

DCFIFO_RESET_ON_LOCK	Description
0	Do not reset on video PLL lock
1 (default)	Reset FIFO on video PLL lock

PIXEL REPETITION

In HDMI mode, video formats with TMDS rates below 25 M pixels/sec require pixel repetition in order to be transmitted over the TMDS link. When the ADV7619 receives this type of video format, it discards repeated pixel data automatically, based on the pixel repetition field available in the AVI InfoFrame.

When HDMI_PIXEL_REPETITION is nonzero, video pixel data is discarded and the pixel clock frequency is divided by (HDMI_PIXEL_REPETITION) + 1.

HDMI_PIXEL_REPETITION[3:0], Addr 68 (HDMI), Address 0x05[3:0] (Read Only)

A readback to provide the current HDMI pixel repetition value decoded from the AVI InfoFrame received. The HDMI receiver automatically discards repeated pixel data and divides the pixel clock frequency appropriately as per the pixel repetition value.

Function

HDMI_PIXEL_REPETITION[3:0]	Description
0000 (default)	1×
0001	2×
0010	3×
0011	4×
0100	5×

Function

HDMI_PIXEL_REPETITION[3:0]	Description
0101	6×
0110	7×
0111	8×
1000	9×
1001	10×
1010 to 1111	Reserved

DEREP_N_OVERRIDE, Addr 68 (HDMI), Address 0x41[4]

This control allows the user to override the pixel repetition factor. The ADV7619 then uses DEREP_N instead of HDMI_PIXEL_REPETITION[3:0] to discard video pixel data from the incoming HDMI stream.

Function

DEREP_N_OVERRIDE	Description
0 (default)	Automatic detection and processing of procession of pixel repeated modes using the AVI InfoFrame information.
1	Enables manual setting of the pixel repetition factor as per DEREP_N[3:0].

DEREP_N[3:0], Addr 68 (HDMI), Address 0x41[3:0]

Sets the derepetition value if derepetition is overridden by setting DEREP_N_OVERRIDE.

Function

DEREP_N[3:0]	Description
0000 (default)	DEREP_N+1 indicates the pixel and clock discard factor
xxxx	DEREP_N+1 indicates the pixel and clock discard factor

BG_PIX_REP[3:0], Addr 68 (HDMI), Address 0xEA[7:4] (Read Only)

Background port pixel repetition status for the background HDMI port determined by **BG_MEAS_PORT_SEL[2:0]**. The readback provides the pixel repetition value in AVI Infoframe and is updated when an update request is made via the **BG_MEAS_REQ** control bit. This measurement is only valid when BG_PARAM_LOCK is set to 1.

Function

BG_PIX_REP[3:0]	Description
0000 «	1x
0001	2x
0010	3x
0011	4x
0100	5x
0101	6x
0110	7x
0111	8x
1000	9x
1001	10x
1010 - 1111	Reserved

Following registers allow forcing YCrCb 444 and YCrCb 422 regardless of the AVI Infoframe. This feature is useful when source switches between YCrCb 444 and YCrCb 422 modes without sending appropriate update in AVI Infoframe.

FORCE_YCRCB_444, Addr 68 (HDMI), Address 0x46[4]

Forces a 4:4:4 interpretation of the video contents, regardless of the description in the AVI infoframe. This bit carries higher priority than FORCE_YCRCB_422.

Function

FORCE_YCRCB_444	Description
0 (default)	Not forced
1	Forced

FORCE_YCRCB_422, Addr 68 (HDMI), Address 0x47[4]

Forces a 4:2:2 interpretation of the video contents, regardless of the description in the AVI infoframe. This bit is only valid if FORCE_YCRCB_444 is zero.

Function

FORCE_YCRCB_422	Description
0 (default)	Not forced
1	Forced

HDCP SUPPORT

HDCP Decryption Engine

The HDCP decryption engine allows for the reception and decryption of HDCP content-protected video and audio data. In the HDCP authentication protocol, the transmitter authenticates the receiver by accessing the HDCP registers of the ADV7619 over the DDC bus. Once the authentication is initiated, the HDCP decryption integrated in the ADV7619 computes and updates a decryption mask for every video frame. This mask is applied to the incoming data at every clock cycle to yield decrypted video and audio data.

HDCP_A0, Addr 68 (HDMI), Address 0x00[7]

A control to set the second LSB of the HDCP port I^2C address.

Function

HDCP_A0	Description
0 (default)	I^2C address for HDCP port is 0x74. Used for single-link mode or 1st Receiver in dual-link mode.
1	I^2C address for HDCP port is 0x76. Used only for a second receiver dual-link mode.

HDMI_CONTENT_ENCRYPTED, Addr 68 (HDMI), Address 0x05[6] (Read Only)

A readback to indicate the use of HDCP encryption.

Function

HDMI_CONTENT_ENCRYPTED	Description
0 (default)	The input stream processed by the HDMI core is not HDCP encrypted.
1	The input stream processed by the HDMI core is HDCP encrypted.

HDMI_ENCRPT_X_RAW reports the encryption status of the data present on each individual HDMI port (where X = A or B).

Note: These bits are reset to 0 if an HDMI packet detection reset occurs. (Refer to the HDMI Packet Detection Flag Reset section.)

HDMI_ENCRPT_A_RAW, IO, Address 0x6F[2] (Read Only)

Raw status of Port A encryption detection signal.

Function

HDMI_ENCRPT_A_RAW	Description
0 (default)	Current frame in Port A is not encrypted.
1	Current frame in Port A is encrypted.

HDMI_ENCRPT_B_RAW, IO, Address 0x6F[1] (Read Only)

Raw status of Port B Encryption detection signal.

Function

HDMI_ENCRPT_B_RAW	Description
0 (default)	Current frame in Port B is not encrypted.
1	Current frame in Port B is encrypted.

Notes

- The ADV7619 supports the 1.1_FEATURES, FAST_REAUTHENTICATION, and FAST_I2C speed HDCP features. The BCAPS register must be initialized appropriately if these features are to be supported by the application integrating the ADV7619, for example, set BCAPS[0] to 1 to support FAST_REAUTHENTICATION.
- It is recommended to set **BCAPS[7:0]** bit [7] to 1 if the ADV7619 is used as the front end of an HDMI receiver. This bit should be set to 0 for DVI applications.

Internal HDCP Key OTP ROM

The ADV7619 features an on-chip nonvolatile memory that is preprogrammed with a set of HDCP keys.

HDCP Keys Access Flags

The ADV7619 accesses the internal HDCP key OTP ROM (also referred to as HDCP ROM) on two different occasions:

- After a power up, the ADV7619 reads the KSV from the internal HDCP ROM (refer to Figure 11).
- After a KSV update from an HDCP transmitter, the ADV7619 reads the KSV and all keys in order to carry out the link verification response (refer to Figure 12).

The host processor can read the HDCP_KEYS_READ and HDCP_KEY_ERROR flags to check that the ADV7619 successfully accessed the HDCP ROM.

HDCP_KEYS_READ, Addr 68 (HDMI), Address 0x04[5] (Read Only)

A readback to indicate a successful read of the HDCP keys and/or KSV from the internal HDCP Key OTP ROM. A logic high is returned when the read is successful.

Function

HDCP_KEYS_READ	Description
0 (default)	HDCP keys and/or KSV not yet read
1	HDCP keys and/or KSV HDCP keys read

HDCP_KEY_ERROR, Addr 68 (HDMI), Address 0x04[4] (Read Only)

A readback to indicate if a checksum error occurred while reading the HDCP and/or KSV from the HDCP Key ROM Returns 1 when HDCP Key master encounters an error while reading the HDCP Key OTP ROM

Function

HDCP_KEY_ERROR	Description
0 (default)	No error occurred while reading HDCP keys
1	HDCP keys read error

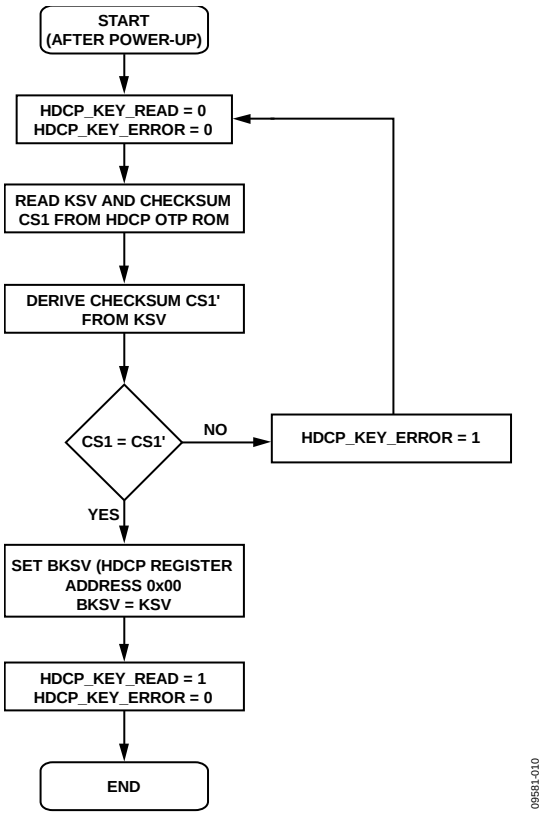


Figure 11. HDCP ROM Access After Power-Up

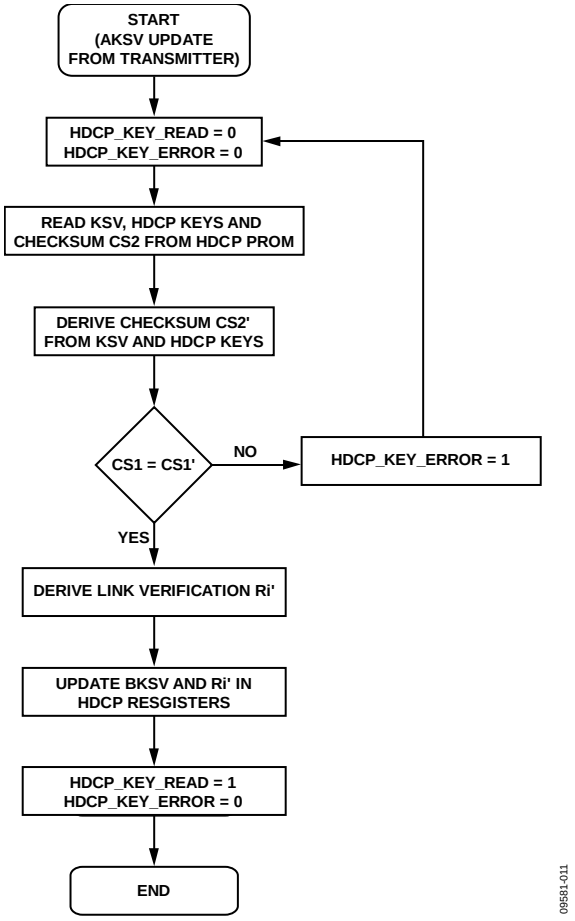


Figure 12. HDCP ROM Access After KSV Update from the Transmitter

Notes

- After the part has powered up, it is recommended to wait for 1 ms before checking the **HDCP_KEYS_READ** and **HDCP_KEY_ERROR** flag bits. This ensures that the ADV7619 had sufficient time to access the internal HDCP ROM and set the **HDCP_KEYS_READ** and **HDCP_KEY_ERROR** flag bits.
- After an AKSV update from the transmitter, it is recommended to wait for 2 ms before checking the **HDCP_KEYS_READ** and **HDCP_KEY_ERROR** flag bits. This ensures that the ADV7619 had sufficient time to access the internal HDCP ROM, and set the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits.
- When the ADV7619 successfully retrieves the HDCP keys and/or KSV from the internal HDCP ROM, the HDCP_KEYS_READ flag bit is set to 1 and the HDCP_KEY_ERROR flag bit is set to 0.
- The I^2C controllers for the main I^2C lines and the HDCP lines are independent of each other. It is, therefore, possible to access the internal registers of the ADV7619 while it reads the HDCP keys and/or the KSV from the internal HDCP ROM.
- A hardware reset (that is, reset via the reset pin) does not lead the ADV7619 to read the KSV or the keys from the HDCP ROM.
- The ADV7619 takes 1.8 ms to read the keys from the HDCP ROM

HDCP Ri Expired

Following register allows early detection of HDMI TX failure. Please also refer to interrupt status controls **RI_EXPIRED_A_ST**, **RI_EXPIRED_B_ST**.

HDCP_RI_EXPIRED, Addr 68 (HDMI), Address 0x04[3] (Read Only)

Readback high when a calculated Ri has not been read by the source TX, on the active port. It remains high until next Aksv update.

Function

HDCP_RI_EXPIRED	Description
0 (default)	Calculated Ri has been read by the source TX
1	Calculated Ri has not been read by the source TX

HDMI SYNCHRONIZATION PARAMETERS

The ADV7619 contains the logic required to measure the details of the incoming video resolution. The HDMI synchronization parameters readback registers from the HDMI map can be used, in addition to the STDI registers from the CP (refer to the Standard Detection and Identification section), to estimate the video resolution of the incoming HDMI stream.

Note

- The synchronization parameters are valid if the part is configured in HDMI mode via **PRIM_MODE[3:0]**.
- The HDMI synchronization filter readback parameters are valid even while the part free runs (refer to the Free Run Mode section) on the condition that the measurement filters have locked.

Horizontal Filter and Measurements

The HDMI horizontal filter performs measurements on the DE and HSync of the HDMI stream on the selected port. The ADV7619 also performs horizontal measurements on the background port as selected by **BG_MEAS_PORT_SEL[2:0]**. These measurements are available in the HDMI map and can be used to determine the resolution of the incoming video data streams.

Primary Port Horizontal Filter Measurements

The HDMI horizontal filter performs the measurements described in this section on the HDMI port selected by **HDMI_PORT_SELECT[2:0]**.

Notes

- The horizontal measurements are valid only if **DE_REGEN_LCK_RAW** is set to 1.
- The HDMI horizontal filter is used solely to measure the horizontal synchronization signals decoded from the HDMI stream. The HDMI horizontal filter is not in the main path of the synchronization processed by the part and does not delay the overall HDMI data into video data out latency.
- The unit for horizontal filter measurement is a pixel, that is, the actual element of the picture content encapsulated in the HDMI/DVI stream which the ADV7619 processes. A pixel has a duration T_{PIXEL}, which is provided in Equation 2, unit time of horizontal filter measurements.

$$T_{Pixel} = T_{FTMDS} \times DEEP\_COLOR\_RATIO \times (PIXEL\_REPETITION + 1) \quad (2)$$

where:
T_{FTMDS} is the TMDS frequency.
DEEP_COLOR_RATIO = 1 for 24-bit deep color.
DEEP_COLOR_RATIO = 5/4 for 30-bit deep color.
DEEP_COLOR_RATIO = 3/2 for 36-bit deep color.
DEEP_COLOR_RATIO = 2 for 48-bit deep color.
PIXEL_REPETITION is the number of repeated pixels in the input HDMI stream.

DE_REGEN_FILTER_LOCKED, Addr 68 (HDMI), Address 0x07[5] (Read Only)

DE regeneration filter lock status. Indicates that the DE regeneration section has locked to the received DE and horizontal synchronization parameter measurements are valid for readback.

Function

DE_REGEN_FILTER_LOCKED	Description
0 (default)	DE regeneration not locked
1	DE regeneration locked to incoming DE

DE_REGEN_LCK_RAW, IO, Address 0x6A[0] (Read Only)

Raw status of the DE regeneration lock signal.

Function

DE_REGEN_LCK_RAW	Description
0 (default)	DE regeneration block has not been locked.
1	DE regeneration block has been locked to the incoming DE signal.

TOTAL_LINE_WIDTH[13:0], Addr 68 (HDMI), Address 0x1E[5:0]; Address 0x1F[7:0] (Read Only)

Total line width is a horizontal synchronization measurement. This gives the total number of pixels per line. This measurement is valid only when the DE regeneration filter has locked.

Function

TOTAL_LINE_WIDTH[13:0]	Description
xxxxxxxxxxxxx	Total number of pixels per line

LINE_WIDTH[12:0], Addr 68 (HDMI), Address 0x07[4:0]; Address 0x08[7:0] (Read Only)

Line width is a horizontal synchronization measurement, which gives the number of active pixels in a line. This measurement is only valid when the DE regeneration filter is locked.

Function

LINE_WIDTH[12:0]	Description
00000000000 (default)	Total number of active pixels per line
xxxxxxxxxxx	Total number of active pixels per line

HSYNC_FRONT_PORCH[12:0], Addr 68 (HDMI), Address 0x20[4:0]; Address 0x21[7:0] (Read Only)

HSync front porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked.

Function

HSYNC_FRONT_PORCH[12:0]	Description
xxxxxxxxxxx	Total number of pixels in the front porch

HSYNC_PULSE_WIDTH[12:0], Addr 68 (HDMI), Address 0x22[4:0]; Address 0x23[7:0] (Read Only)

HSync pulse width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked.

Function

HSYNC_PULSE_WIDTH[12:0]	Description
xxxxxxxxxxx	Total number of pixels in the hsync pulse

HSYNC_BACK_PORCH[12:0], Addr 68 (HDMI), Address 0x24[4:0]; Address 0x25[7:0] (Read Only)

HSync back porch width is a horizontal synchronization measurement. The unit of this measurement is unique pixels. This measurement is valid only when the DE regeneration filter has locked.

Function

HSYNC_BACK_PORCH[12:0]	Description
xxxxxxxxxxx	Total number of pixels in the back porch

DVI_HSYNC_POLARITY, Addr 68 (HDMI), Address 0x05[5] (Read Only)

A readback to indicate the polarity of the HSync encoded in the input stream

Function

DVI_HSYNC_POLARITY	Description
0 (default)	The HSync is active low.
1	The HSync is active high.

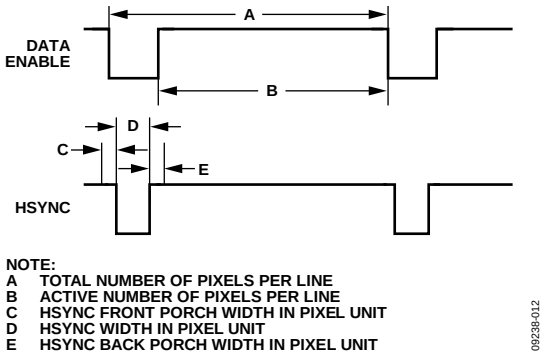


Figure 13. Horizontal Timing Parameters

Background Port Horizontal Filter Measurements

The HDMI horizontal filter performs the measurements described in this section on the HDMI port selected by **BG_MEAS_PORT_SEL[2:0]**.

Note: **BG_PARAM_LOCK** must be high for background horiztonal and vertical measurements to be valid.

BG_PARAM_LOCK, Addr 68 (HDMI), Address 0xEA[1] (Read Only)

A flag to indicate that vertical and horizontal parameters have been locked during a background measurement.

Function

BG_PARAM_LOCK	Description
0 (default)	Horizontal and Vertical were not locked when measurement for select background HDMI port were taken.
1	Horizontal and Vertical were locked when measurement for select background HDMI port were taken.

BG_TOTAL_LINE_WIDTH[13:0], Addr 68 (HDMI), Address 0xE4[5:0]; Address 0xE5[7:0] (Read Only)

Background port total line width, a horizontal synchronization measurement for the background HDMI Port determined by **BG_MEAS_PORT_SEL[2:0]**. The value represents the total number of pixels in a line and is updated when a update request is made via the **BG_MEAS_REQ** control bit. This measurement is only valid when **BG_PARAM_LOCK** is set to 1.

Function

BG_TOTAL_LINE_WIDTH[13:0]	Description
xxxxxxxxxxxxx	The total number of pixels per line on the background measurement port

BG_LINE_WIDTH[12:0], Addr 68 (HDMI), Address 0xE2[4:0]; Address 0xE3[7:0] (Read Only)

Background port line width, a horizontal synchronization measurement for the background HDMI Port determined by **BG_MEAS_PORT_SEL[2:0]**. The value represents the number of active pixels in a line and is updated when a update request is made via the **BG_MEAS_REQ** control bit.

Function

BG_LINE_WIDTH[12:0]	Description
0000000000000 (default)	The number of active pixels per line on the background measurement port.
xxxxxxxxxxxxx	The number of active pixels per line on the background measurement port.

Horizontal Filter Locking Mechanism

The locking/unlocking mechanism of the HDMI horizontal filter is as follows:

- The HDMI horizontal filter locks if the following two conditions are met:
  - The DE transitions occur at the exact same pixel count for eight consecutive video lines
  - The HSync transitions occur at the exact same pixel count for eight consecutive video lines
- The HDMI horizontal filter unlocks if either of the two following conditions are met:
  - The DE transitions occur on different pixels count for 15 consecutive video lines
  - The HSync transitions occur on different pixels count for 15 consecutive video lines

Vertical Filters and Measurements

The ADV7619 integrates a HDMI vertical filter which performs measurements on the VSync of the HDMI stream on the selected port. The ADV7619 also performs vertical measurements on the background port as selected by **BG_MEAS_PORT_SEL[2:0]**.These measurements are available in the HDMI map and can be used to determine the resolution of the incoming video data streams.

Primary Port Vertical Filter Measurements

The HDMI vertical filter performs the measurements on the HDMI port selected by **HDMI_PORT_SELECT[2:0]**.

The Field 0 measurements are adequate to determine the standard of incoming progressive modes. A combination of Field 0 and field 1 measurements should be used to determine the standard of interlaced modes.

Notes

- The vertical measurements are valid only if **V_LOCKED_RAW** is set to 1.
- The HDMI vertical filter is used solely to measure the vertical synchronization signals decoded from the HDMI stream. This filter is not in the main path of the synchronization processed by the part and does not delay the overall HDMI data into video data out latency.

VERT_FILTER_LOCKED, Addr 68 (HDMI), Address 0x07[7] (Read Only)

Vertical filter lock status. Indicates whether the vertical filter is locked and vertical synchronization parameter measurements are valid for readback.

Function

VERT_FILTER_LOCKED	Description
0	Vertical filter has not locked.
1	Vertical filter has locked.

V_LOCKED_RAW, IO, Address 0x6A[1] (Read Only)

Raw status of the vertical sync filter locked signal.

Function

V_LOCKED_RAW	Description
0	Vertical sync filter has not locked and vertical sync parameters are not valid
1	Vertical sync filter has locked and vertical sync parameters are valid

Note: Field 0 measurements are used to determine the video modes that are progressive.

FIELD0_TOTAL_HEIGHT[13:0], Addr 68 (HDMI), Address 0x26[5:0]; Address 0x27[7:0] (Read Only)

Field 0 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 0. This measurement is valid only when the vertical filter has locked.

Function

FIELD0_TOTAL_HEIGHT[13:0]	Description
xxxxxxxxxxxxx	The total number of half lines in Field 0 (divide readback by 2 to get number of lines)

FIELD0_HEIGHT[12:0], Addr 68 (HDMI), Address 0x09[4:0]; Address 0x0A[7:0] (Read Only)

Field 0 height is a vertical filter measurement. This readback gives the number of active lines in Field 0. This measurement is valid only when the vertical filter has locked.

Function

FIELD0_HEIGHT[12:0]	Description
xxxxxxxxxxxx	The number of active lines in Field 0

FIELD0_VS_FRONT_PORCH[13:0], Addr 68 (HDMI), Address 0x2A[5:0]; Address 0x2B[7:0] (Read Only)

Field 0 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the vertical filter has locked.

Function

FIELD0_VS_FRONT_PORCH[13:0]	Description
xxxxxxxxxxxxx	The total number of half lines in the VSync front porch of Field 0 (divide readback by 2 to get number of lines)

FIELD0_VS_PULSE_WIDTH[13:0], Addr 68 (HDMI), Address 0x2E[5:0]; Address 0x2F[7:0] (Read Only)

Field 0 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked.

Function

FIELD0_VS_PULSE_WIDTH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSync pulse of Field 0 (divide readback by 2 to get number of lines)

FIELD0_VS_BACK_PORCH[13:0], Addr 68 (HDMI), Address 0x32[5:0]; Address 0x33[7:0] (Read Only)

Field 0 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines.

Function

FIELD0_VS_BACK_PORCH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSync Back Porch of Field 0 (divide readback by 2 to get number of lines)

DVI_VSYNC_POLARITY, Addr 68 (HDMI), Address 0x05[4] (Read Only)

A readback to indicate the polarity of the VSync encoded in the input stream

Function

DVI_VSYNC_POLARITY	Description
0	The Vsync is active low.
1	The VSync is active high.

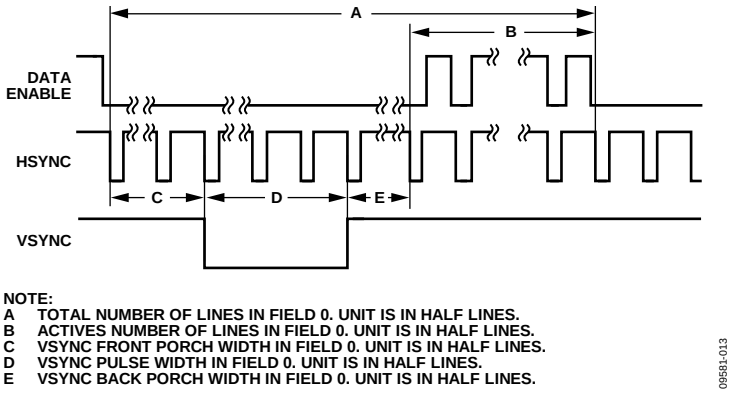


Figure 14. Vertical Parameters for FIELD 0

Note: Field 1 measurements should not be used for progressive video modes.

FIELD1_TOTAL_HEIGHT[13:0], Addr 68 (HDMI), Address 0x28[5:0]; Address 0x29[7:0] (Read Only)

Field 1 total height is a vertical synchronization measurement. This readback gives the total number of half lines in Field 1. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Function

FIELD1_TOTAL_HEIGHT[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in Field 1 (divide readback by 2 to get number of lines)

FIELD1_HEIGHT[12:0], Addr 68 (HDMI), Address 0x0B[4:0]; Address 0x0C[7:0] (Read Only)

Field 1 height is a vertical filter measurement. This readback gives the number of active lines in field. This measurement is valid only when the vertical filter has locked. Field 1 measurements are only valid when HDMI_INTERLACED is set to 1.

Function

FIELD1_HEIGHT[12:0]	Description
xxxxxxxxxxxxx	The number of active lines in Field 1

FIELD1_VS_FRONT_PORCH[13:0], Addr 68 (HDMI), Address 0x2C[5:0]; Address 0x2D[7:0] (Read Only)

Field 1 VSync front porch width is a vertical synchronization measurement. The unit of this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Function

FIELD1_VS_FRONT_PORCH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSync front porch of Field 1 (divide readback by 2 to get number of lines)

FIELD1_VS_PULSE_WIDTH[13:0], Addr 68 (HDMI), Address 0x30[5:0]; Address 0x31[7:0] (Read Only)

Field 1 VSync width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Function

FIELD1_VS_PULSE_WIDTH[13:0]	Description
xxxxxxxxxxxxxx	The total number of half lines in the VSync pulse of Field 1 (divide readback by 2 to get number of lines)

FIELD1_VS_BACK_PORCH[13:0], Addr 68 (HDMI), Address 0x34[5:0]; Address 0x35[7:0] (Read Only)

Field 1 VSync back porch width is a vertical synchronization measurement. The unit for this measurement is half lines. This measurement is valid only when the vertical filter has locked. Field 1 measurements are valid when HDMI_INTERLACED is set to 1.

Function

FIELD1_VS_BACK_PORCH[13:0]	Description
xxxxxxxxxxxxxx	The number of half lines in the VSync back porch of Field 1 (divide readback by 2 to get number of lines)

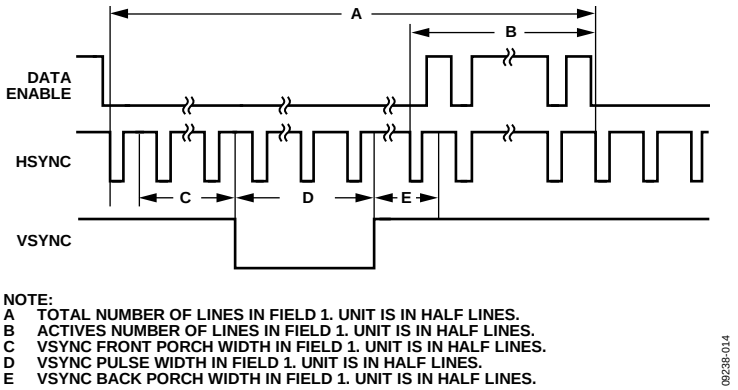


Figure 15. Vertical Parameters for FIELD 1

The vertical filter provides the interlaced status of the video stream. The interlaced status HDMI_INTERLACED is valid only if the vertical filter is locked and V_LOCKED_RAW is set to 1.

HDMI_INTERLACED, Addr 68 (HDMI), Address 0x0B[5] (Read Only)

HDMI input interlace status, a vertical filter measurement.

Function

HDMI_INTERLACED	Description
0	Progressive Input
1	Interlaced Input

Background Port Vertical Filter Measurements

The HDMI vertical filter performs the measurements described in this section on the HDMI port selected by **BG_MEAS_PORT_SEL[2:0]**.

Note: **BG_PARAM_LOCK** must be high for background horizontal and vertical measurements to be valid.

BG_TOTAL_FIELD_HEIGHT[12:0], Addr 68 (HDMI), Address 0xE8[4:0]; Address 0xE9[7:0] (Read Only)

Background port total field height is a vertical synchronization measurement for the background HDMI port determined by **BG_MEAS_PORT_SEL[2:0].** The value represents the total number of lines in a field and is updated when an update request is made via the **BG_MEAS_REQ** control bit.

Function

BG_TOTAL_FIELD_HEIGHT[12:0]	Description
0000000000000 « xxxxxxxxxxxxx	The total number of lines in a Field on the background measurement port The total number of lines in a Field on the background measurement port

BG_FIELD_HEIGHT[12:0], Addr 68 (HDMI), Address 0xE6[4:0]; Address 0xE7[7:0] (Read Only)

Background port field height is a vertical synchronization measurement for a background HDMI port determined by **BG_MEAS_PORT_SEL[2:0].** The value represents the number of active lines in a field and is updated when an update request is made via the **BG_MEAS_REQ** control bit.

Function

BG_FIELD_HEIGHT[12:0]	Description
0000000000000 « xxxxxxxxxxxxx	The number of active lines in a Field on the background measurement port The number of active lines in a Field on the background measurement port

BG_HDMI_INTERLACED, Addr 68 (HDMI), Address 0xEA[0] (Read Only)

Background port HDMI input interlace status is a vertical filter measurement for a background HDMI port determined by **BG_MEAS_PORT_SEL[2:0]**. The status readback is updated when a update request is made via the **BG_MEAS_REQ** control bit. This measurement is only valid when **BG_PARAM_LOCK** is set to 1.

Function

BG_HDMI_INTERLACED	Description
0 « 1	Progressive Input Interlaced Input

Vertical Filter Locking Mechanism

The HDMI vertical filter locks if the input VSync comes at exactly the same line count for two consecutive frames. The HDMI vertical filter unlocks if the VSync comes at a different pixels count for two consecutive frames.

Low Frequency Formats

To process the low frame rate video formats such as 720p24, 720p25, 720p30, 1080p23, 1080p24, and 1080p30, the **NEW_VS_PARAM** bit should be set. Refer to Figure 16.

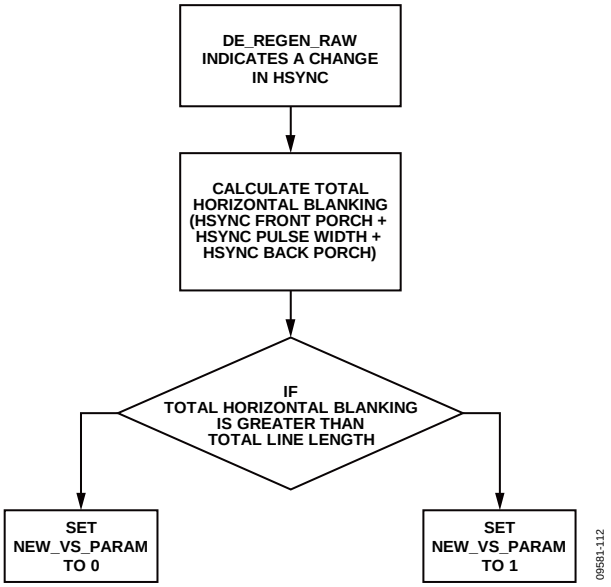


Figure 16. Low Frame Rate Algorithm

NEW_VS_PARAM, HDMI, Address 0x4C[2]

Enables a new version of vertical parameter extraction for evaluation purposes. That is the version in the background port measurement blocks.

Function

NEW_VS_PARAM	Description
0	NEW_VS_PARAM disabled
1	NEW_VS_PARAM enabled

AUDIO CONTROL AND CONFIGURATION

The ADV7619 extracts an L-PCM, IEC 61937 compressed DSD or high-bit rate (HBR) audio data stream from their corresponding audio packets (that is, audio sample, DSD or HBR) encapsulated inside the HDMI data stream.

The ADV7619 also regenerates an audio master clock along with the extraction of the audio data. The clock regeneration is performed by an integrated DPLL. The regenerated clock is used to output audio data from the 64 stereo sample depth FIFO to the audio interface configuration pins.

Important

- The ADV7619 supports the extraction of stereo audio data (noncompressed or compressed) at audio sampling frequency up to 192 kHz
- The ADV7619 supports the extraction of multichannel audio data

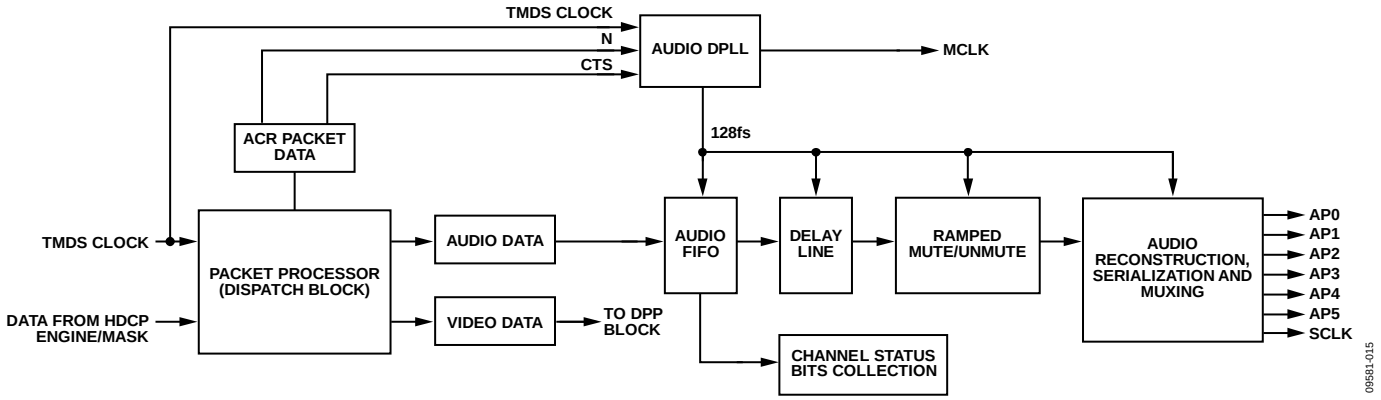


Figure 17. Audio Processor Block Diagram

Audio DPLL

The audio DPLL generates an internal audio master clock with a frequency of 128 times the audio sampling frequency, usually called fs. The audio master clock is used to clock the audio processing section.

Locking Mechanism

When the upstream HDMI transmitter outputs a stable TMDS frequency and consistent audio clock regeneration values, the audio DPLL locks within two cycles of the audio master clock after the following two conditions are met:

- TMDS PLL is locked (refer to **TMDS_PLL_LOCKED**)
- ADV7619 has received an ACR packet with N and CTS parameters within a valid range

The audio DPLL lock status can be monitored via **AUDIO_PLL_LOCKED**.

AUDIO_PLL_LOCKED, Addr 68 (HDMI), Address 0x04[0] (Read Only)

A readback to indicate the Audio DPLL lock status.

Function

AUDIO_PLL_LOCKED	Description
0 (default)	The audio DPLL is not locked.
1	The audio DPLL is locked.

ACR Parameters Loading Method

The N and CTS parameters from the ACR packets are used to regenerate the audio clock and are reloaded into the DPLL anytime they change. The self-clearing bit **FORCE_N_UPDATE** provides a means to reset the audio DPLL by forcing a reload of the N and CTS parameters from the ACR packet into the audio DPLL.

FORCE_N_UPDATE, Addr 68 (HDMI), Address 0x5A[0] (Self-Clearing)

A control to force an N and CTS value update to the audio DPLL. The audio DPLL regenerates the audio clock.

Function

FORCE_N_UPDATE	Description
0 (default)	No effect
1	Forces an update on the N and CTS values for audio clock regeneration

Audio DPLL Coast Feature

The audio DPLL incorporates a coast feature that allows it to indefinitely output a stable audio master clock when selectable events occur. The coast feature allows the audio DPLL to provide an audio master clock when the audio processor mutes the audio following a mute condition (refer to the Audio Muting section). The events that cause the audio DPLL to coast are selected via the coasts masks listed in Table 10.

Table 10. Selectable Coast Conditions

Bit Name	HDMI Map Address	Description	Corresponding Status Registers(s)
AC_MSK_VCLK_CHNG	0x13[6]	When set to 1, audio DPLL coasts if TMDS clock has any irregular/missing pulses	VCLK_CHNG_RAW
AC_MSK_VPLL_UNLOCK	0x13[5]	When set to 1, audio DPLL coasts if TMDS PLL unlocks	TMDS_PLL_LOCKED
AC_MSK_NEW_CTS	0x13[3]	When set to 1, audio DPLL coasts if CTS changes by more than the threshold set in **CTS_CHANGE_THRESHOLD[5:0]**	**CTS_PASS_THRSH_RAW**
AC_MSK_NEW_N	0x13[2]	When set to 1, audio DPLL coasts if N changes	**CHANGE_N_RAW**
AC_MSK_CHNG_PORT	0x13[1]	When set to 1, audio DPLL coasts if active port is changed	**HDMI_PORT_SELECT[2:0]**
AC_MSK_VCLK_DET	0x13[0]	When set to 1, audio DPLL coasts if no TMDS clock is detected on the active port	TMDS_CLK_A_RAW TMDS_CLK_B_RAW

AUDIO FIFO

The audio FIFO can store up to 128 audio stereo data from the audio sample, DSD or HBR packets. Stereo audio data are added into the FIFO from the audio packet received. Stereo audio data are retrieved from the FIFO at a rate corresponding to 128 times the audio sampling frequency, f_s.

The status of the audio FIFO can be monitored through the status flags **FIFO_UNDERFLO_RAW, FIFO_OVERFLO_RAW, FIFO_NEAR_OVFL_RAW**, and **FIFO_NEAR_UFLO_RAW.**

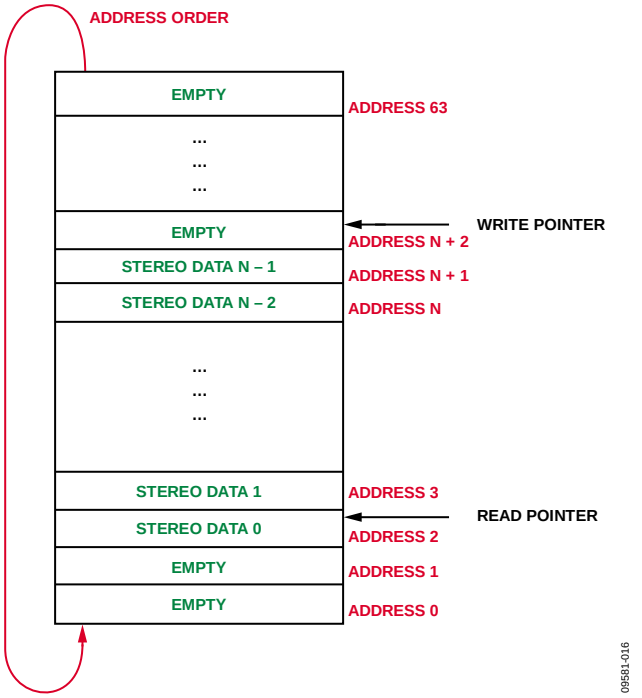


Figure 18. Audio FIFO

FIFO_UNDERFLO_RAW, IO, Address 0x7E[6] (Read Only)

Status of audio FIFO underflow interrupt signal. When set to 1, it indicates the audio FIFO read pointer has reached the write pointer causing the audio FIFO to underflow. Once set, this bit will remain high until it is cleared via AUDIO_FIFO_UNDERFLO_CLR.

Function

FIFO_UNDERFLO_RAW	Description
0 (default)	Audio FIFO has not underflowed.
1	Audio FIFO has underflowed.

FIFO_OVERFLO_RAW, IO, Address 0x7E[5] (Read Only)

Status of audio FIFO overflow interrupt signal. When set to 1, it indicates audio FIFO write pointer has reached the read pointer causing the audio FIFO to overflow. Once set, this bit will remain high until it is cleared via AUDIO_FIFO_OVERFLO_CLR.

Function

FIFO_OVERFLO_RAW	Description
0 (default)	Audio FIFO has not overflowed.
1	Audio FIFO has overflowed.

FIFO_NEAR_UFLO_RAW, IO, Address 0x83[0] (Read Only)

Status of audio FIFO near underflow interrupt signal. When set to 1, it indicates the audio FIFO is near underflow as the number of FIFO registers containing stereo data is less or equal to value set in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD. Once set, this bit will remain high until it is cleared via FIFO_NEAR_UFLO_CLR.

Function

FIFO_NEAR_UFLO_RAW	Description
0 (default)	Audio FIFO has not reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0].
1	Audio FIFO has reached low threshold defined in AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD [5:0].

FIFO_NEAR_OVFL_RAW, IO, Address 0x7E[7] (Read Only)

Status of audio FIFO near overflow interrupt signal. When set to 1, it indicates the audio FIFO is near overflow as the number FIFO registers containing stereo data is greater or equal to value set in AUDIO_FIFO_ALMOST_FULL_THRESHOLD. Once set, this bit will remain high until it is cleared via FIFO_NEAR_OVFL_CLR.

Function

FIFO_NEAR_OVFL_RAW	Description
0 (default)	Audio FIFO has not reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0]
1	Audio FIFO has reached high threshold defined in AUDIO_FIFO_ALMOST_FULL_THRESHOLD [5:0]

AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0], Addr 68 (HDMI), Address 0x12[6:0]

Sets the threshold used for FIFO_NEAR_UFLO_RAW. FIFO_NEAR_UFLO_ST interrupt is triggered if audio FIFO goes below this level.

Function

AUDIO_FIFO_ALMOST_EMPTY_THRESHOLD[6:0]	Description
0x02 (default)	Default value

AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0], Addr 68 (HDMI), Address 0x11[6:0]

Sets the threshold used for FIFO_NEAR_OVRFL_RAW. FIFO_NEAR_OVRFL_ST interrupt is triggered if audio FIFO reaches this level.

Function

AUDIO_FIFO_ALMOST_FULL_THRESHOLD[6:0]	Description
0x7D (default)	Default value

AUDIO PACKET TYPE FLAGS

The ADV7619 can receive the following audio packets:

- Audio sample packets—receive and process
- HBR packets—receive and process
- DSD packets— receive and process
- DST packets—detection only

The following flags are provided to monitor the type of audio packets received by the ADV7619. Figure 19 shows the algorithm that can be implemented to monitor the type of audio packet processed by the ADV7619.

AUDIO_MODE_CHNG_RAW, IO, Address 0x83[5] (Read Only)

Status of audio mode change interrupt signal. When set to 1, it indicates that the type of audio packet received has changed. The following are considered audio modes, no audio packets, audio sample packet, DSD packet, HBR packet or DST packet. Once set, this bit remains high until it is cleared via AUDIO_MODE_CHNG_CLR.

Function

AUDIO_MODE_CHNG_RAW	Description
0 (default)	Audio mode has not changed.
1	Audio mode has changed.

AUDIO_SAMPLE_PCKT_DET, Addr 68 (HDMI), Address 0x18[0] (Read Only)

Audio sample packet detection bit. This bit resets to zero on the 11th HSync leading edge following an audio packet if a subsequent audio sample packet has not been received or if a DSD, DST, or HBR audio packet sample packet has been received.

Function

AUDIO_SAMPLE_PCKT_DET	Description
0 (default)	No L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSync
1	L_PCM or IEC 61937 compressed audio sample packet received within the last 10 HSyncs

DSD_PACKET_DET, Addr 68 (HDMI), Address 0x18[1] (Read Only)

DSD audio packet detection bit. This bit resets to zero on the 11th HSync leading edge following a DSD packet or if an audio, DST, or HBR packet sample packet has been received or after an HDMI reset condition.

Function

DSD_PACKET_DET	Description
0 (default)	No DSD packet received within the last 10 HSync
1	DSD packet received within the last 10 HSync

DST_AUDIO_PCKT_DET, Addr 68 (HDMI), Address 0x18[2] (Read Only)

DST audio packet detection bit. This bit resets to zero on the 11th HSync leading edge following a DST packet if a subsequent DST has not been received. Or if an audio, DSD, or HBR packet sample packet has been received or after an HDMI reset condition.

Function

DST_AUDIO_PCKT_DET	Description
0 (default)	No DST packet received within the last 10 HSync
1	DST packet received within the last 10 HSync

HBR_AUDIO_PCKT_DET, Addr 68 (HDMI), Address 0x18[3] (Read Only)

HBR Packet detection bit. This bit resets to zero on the 11th HSync leading edge following an HBR packet if a subsequent HBR packet has not been detected. It also resets if an Audio, DSD or DST packet sample packet has been received and after an HDMI reset condition.

Function

HBR_AUDIO_PCKT_DET	Description
0 (default)	No HBR audio packet received within the last 10 HSync
1	HBR audio packet received within the last 10 HSync

Notes

- The ADV7619 processes only one type of audio packet at a time.
- The ADV7619 processes the latest type of audio packet that it received.
- AUDIO_SAMPL_PCKT_DET, DSD_PACKET_DET, DST_AUDIO_PCKT_DET, and HBR_AUDIO_PCKT_DET are reset to 0 when a HDMI packet detect reset condition occurs.
- A corresponding interrupt can be enabled for AUDIO_MODE_CHNG_RAW by setting the mask AUDIO_MODE_CHNG_MB1 or AUDIO_MODE_CHNG_MB2. Refer to the Interrupts section for additional information on the interrupt feature.

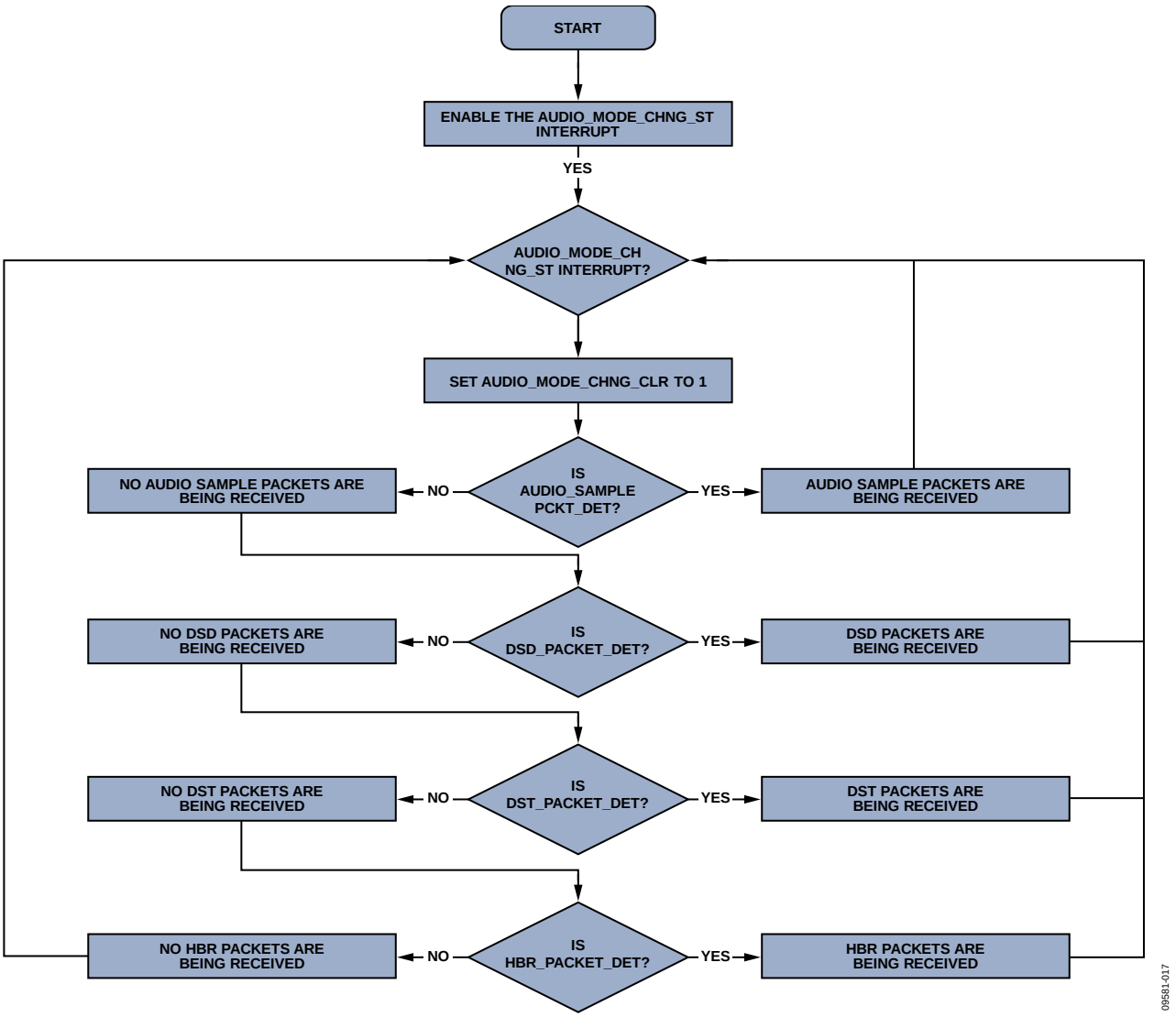


Figure 19. Monitoring Audio Packet Type Processed by ADV7619

AUDIO OUTPUT INTERFACE

The ADV7619 has a dedicated three-pin audio output interface. The output pin names and descriptions are shown in Table 11.

Table 11. Audio Outputs and Clocks

Output Pixel Port	Description
AP0	Audio Output Port 0
AP1	Audio Output Port 1
AP2	Audio Output Port 2
AP3	Audio Output Port 3
AP4	Audio Output Port 4
AP5	Audio Output Port 5
SCLK/INT2	Bit Clock
MCLK/INT2	Audio Master Clock

Table 12 shows the default configurations for the various possible output interfaces.

Table 12. Default Audio Output Pixel Port Mapping

Output Pixel Port	I²S/SPDIF Interface	DSD Interface
AP0	SPDIF0	DSD0A
AP1	I2S0/SDPIF0	DSD0B
AP2	I2S1/SDPIF1	DSD1A
AP3	I2S2/SPDIF2	DSD1B
AP4	I2S3/SPDIF3	DSD2A
AP5	LRCLK	DSD2B

Note that it is possible to tristate the audio pins using the global controls, as described in the Tristate Audio Output Drivers section. It is possible to output AP0 signal (SPDIF0) to the AP1 pin using MUX_SPDIF_TO_I2S_ENABLE.

MUX_SPDIF_TO_I2S_ENABLE, Addr 68 (HDMI), Address 0x6E[3]

Enables muxing SPDF data into I²S pins (AP1)

Function

MUX_SPDIF_TO_I2S_ENABLE	Description
0 (default)	Do not modify I²S outputs
1	Mux SPDIF into I²S pins

I²S/SPDIF Audio Interface and Output Controls

Two controls are provided to change the mapping between the audio output ports and the I²S and SPDIF (IEC60958) signals.

I2S_SPDIF_MAP_ROT[1:0], Addr 68 (HDMI), Address 0x6D[5:4]

A control to select the arrangement of the I²S/SPDIF interface on the audio output port pins.

Function

I2S_SPDIF_MAP_ROT[1:0]	Description
00 (default)	[I2S0/SPDIF0 on AP1] [I2S1/SPDIF1 on AP2] [I2S2/SPDIF2 on AP3] [I2S3/SPDIF3 on AP4]
01	[I2S3/SPDIF3 on AP1] [I2S0/SPDIF0 on AP2] [I2S1/SPDIF1 on AP3] [I2S2/SPDIF2 on AP4]
10	[I2S2/SPDIF2 on AP1] [I2S3/SPDIF3 on AP2] [I2S0/SPDIF0 on AP3] [I2S1/SPDIF1 on AP4]
11	[I2S1/SPDIF1 on AP1] [I2S2/SPDIF2 on AP2] [I2S3/SPDIF3 on AP3] [I2S0/SPDIF0 on AP4]

I2S_SPDIF_MAP_INV, Addr 68 (HDMI), Address 0x6D[6]

A control to invert the arrangement of the I²S/SPDIF interface on the audio output port pins. Note the arrangement of the I²S/SPDIF interface on the audio output port pins is determined by I2S_SPDIF_MAP_ROT.

Function

I2S_SPDIF_MAP_INV	Description
0 (default)	Do not invert arrangement of I²S/SPDIF channels in audio output port pins
1	Invert arrangement of I²S/SPDIF channels in audio output port pins

I2S_SPDIF_MAP_ROT[1:0] and **I2S_SPDIF_MAP_INV** are independent controls. Any combination of values is therefore allowed for **I2S_SPDIF_MAP_ROT[1:0]** and **I2S_SPDIF_MAP_INV**. Table 13 and Table 14 show examples of mappings for the I²S/SPDIF signals.

Table 13. Audio Mappings for I2S_SPDIF_MAP_ROT = 00, I2S_SPDIF_MAP_INV = 0 (Default)

Output Audio Port	I²S/SPDIF Interface
AP1	I2S0/SDPIF0
AP2	I2S1/SDPIF1
AP3	I2S2/SDPIF2
AP4	I2S3/SDPIF3

Table 14. Audio Mappings for I2S_SPDIF_MAP_ROT = 00, I2S_SPDIF_MAP_INV = 1

Output Audio Port	I2S/SPDIF Interface
AP1	I2S3/SDPIF3
AP2	I2S2/SDPIF2
AP3	I2S1/SDPIF1
AP4	I2S0/SDPIF0

I2SBITWIDTH[4:0], Addr 68 (HDMI), Address 0x03[4:0]

A control to adjust the bit width for right justified mode on the I²S interface.

Function

I2SBITWIDTH[4:0]	Description
00000	0 bit
00001	1 bit
00010	2 bits
…	…
11000 (default)	24 bits
11110	30 bits
11111	31 bits

I2SOUTMODE[1:0], Addr 68 (HDMI), Address 0x03[6:5]

A control to configure the I²S output interface.

Function

I2SOUTMODE[1:0]	Description
00 (default)	I²S mode
01	Right justified
10	Left justified
11	Raw SPDIF (IEC60958) mode

Notes

I2SOUTMODE[1:0] is effective when the ADV7619 is configured to output I²S streams or AES3 streams. This is the case in the following situation:

- The ADV7619 receives audio sample packets.
- The ADV7619 receives HBR packets, **OVR_MUX_HBR** is set to 1, and **MUX_HBR_OUT** is set to 2'b00, 2'b01, 2'b10, or 2'b11.
- In HBR mode, it is required that the part outputs four SPDIF, I²S, or raw IEC60958 streams encapsulating a 24-bit audio sample word. Therefore, I2SBITSWIDTH[4:0] should always be set to 0b11000.

The following audio formats can be output when the ADV7619 receives audio sample packets:

- L-PCM audio data is output on the audio output pins if the part received audio sample packets with L-PCM encoded audio data. Each audio output pin carries stereo data that can be output in I²S, right justified, or left justified mode (refer to Figure 20, Figure 21, and Figure 22). The **I2SOUTMODE[1:0]** control must be set to 0x0, 0x01, or 0x2 to output I²S, right justified, and left justified respectively on the audio output pins.
- A stream conforming to the IEC60958 specification when the part receives audio sample packets with L-PCM encoded data (refer to Figure 23).
- An AES3 stream if the **I2SOUTMODE[1:0]** control is set to 0x3 (refer to Figure 24 and Figure 25). Note that AES3 is also referred to as raw SPDIF. Each AES3 stream may encapsulate stereo L-PCM audio data or multichannel non L-PCM audio data (for example, 5.1 Dolby Digital).
- Binary stream on the audio output pins when the part receives audio sample packets with non L-PCM encoded audio data (that is, AC-3 compressed audio) and if the following configuration is used:
  - I2SOUTMODE must be set to 0x0, 0x01, or 0x2 for I²S, right justified, and left justified format, respectively (refer to Figure 20, Figure 21, and Figure 22).
  - MT_MSK_COMPRS_AUD is set to 0.

  Note that no audio flags are output by the part in that configuration. Each binary stream output by the part may encapsulate stereo L-PCM audio data or multichannel non L-PCM audio data (for example, 5.1 Dolby Digital).

- A stream conforming to the IEC61937 specification when the part receives audio sample packets with non L-PCM encoded audio data (for example, AC-3 compressed audio). The audio outputs can carry an audio stream that may be stereo or multichannel audio (for example, 5.1 Dolby Digital).

Table 15. I²S/SPDIF Interface Description

I²S/SPDIF Interface IO	Function
SPDIF0	SPDIF audio output
I2S0/SPDIF0	I²S audio (Channel 1, Channel 2)/SPDIF0
I2S1/SPDIF1	I²S audio (Channel 3, Channel 4)/SPDIF1
I2S2/SPDIF2	I²S audio (Channel 5, Channel 6)/SPDIF2
I2S3/SPDIF3	I²S audio (Channel 7, Channel 8)/SPDIF3
SCLK	Bit clock
LRCLK	Data output clock for left and right channel
MCLKOUT	Audio master clock output

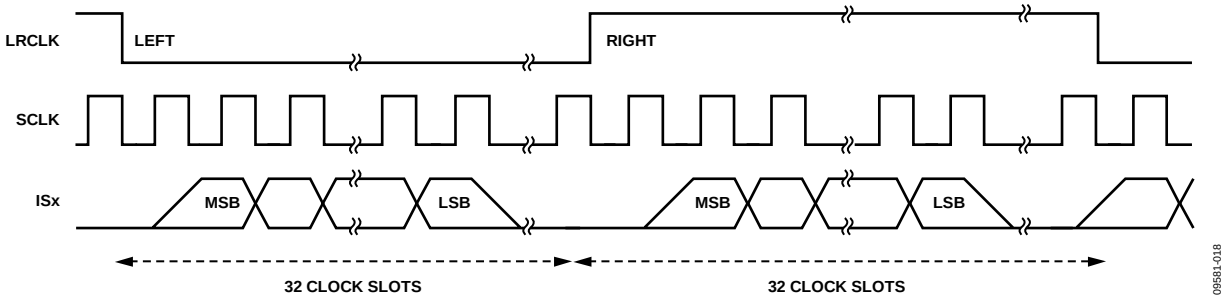


Figure 20. Timing Audio Data Output in I²S Mode

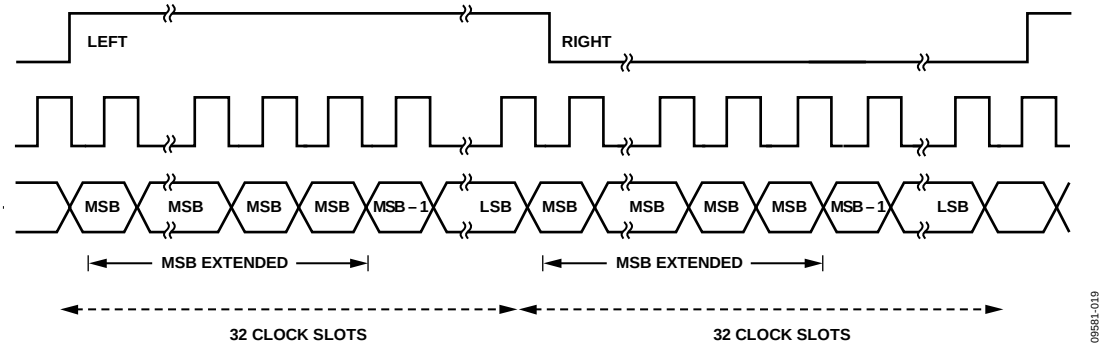


Figure 21. Timing Audio Data Output in Right Justified Mode

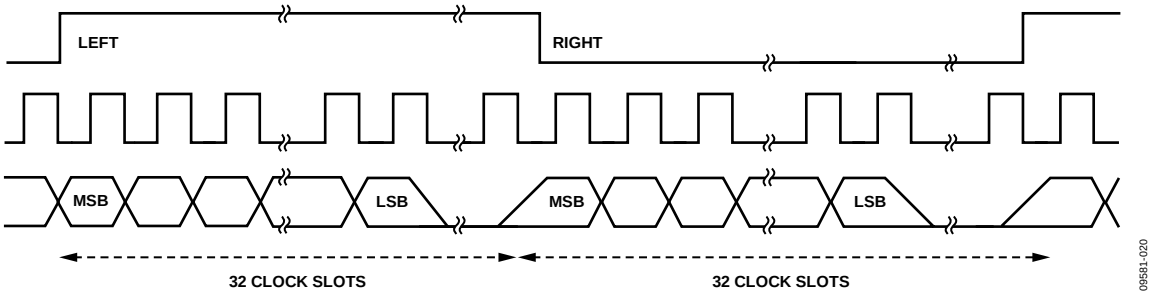


Figure 22. Timing Audio Data Output in Left Justified Mode

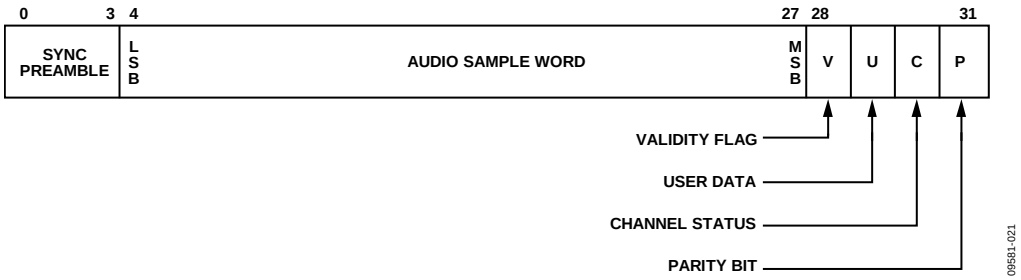


Figure 23. IEC 60958 Subframe Timing Diagram

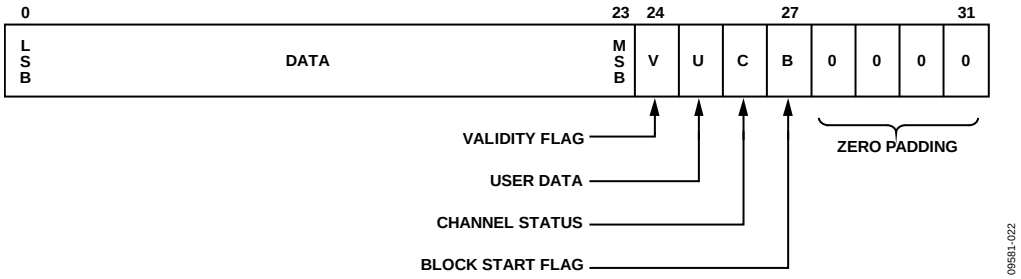


Figure 24. AES3 Subframe Timing Diagram

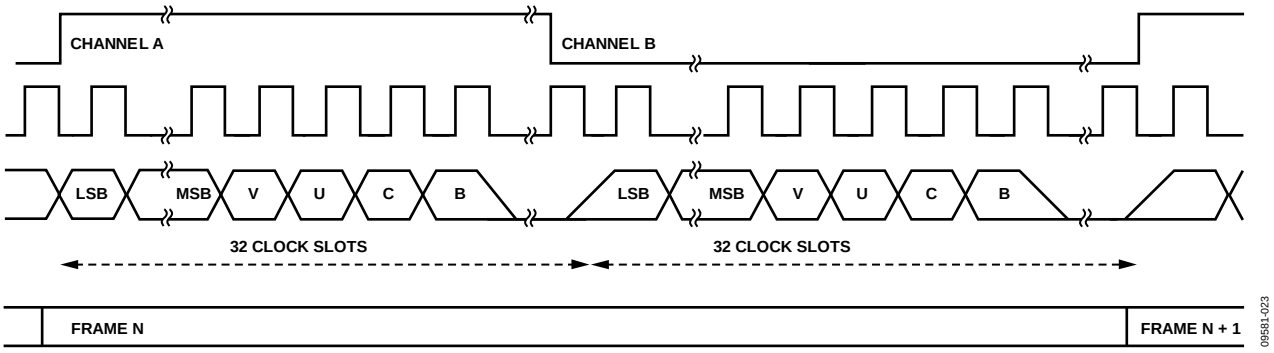


Figure 25. AES3 Stream Timing Diagram

DSD Audio Interface and Output Controls

The ADV7619 incorporates a 6-DSD channel interface used to output the audio stream extracted from DSD packets. Each of the DSD channels carries an oversampled 1-bit representation of the audio signal as delivered on super audio CDs (SACDs).

Table 16. DSD Interface Description

DSD Interface IO	Function
DSD0A	1st DSD data channel
DSD0B	2nd DSD data channel
DSD1A	3rd DSD data channel
DSD1B	4th DSD data channel
DSD2A	5th DSD data channel
DSD2B	6th DSD data channel
SCLK	Bit clock
MCLKOUT	Audio master clock output

Two controls are provided to change the mapping between the audio output ports and DSD signals.

DSD_MAP_ROT[2:0], Addr 68 (HDMI), Address 0x6D[2:0]

A control to select the arrangement of the DSD interface on the audio output port pins.

Function

DSD_MAP_ROT[2:0]	Description
000 (default)	[DSD0A on AP0] [DSD0B on AP1] [DSD1A on AP2] [DSD1B on AP3] [DSD2A on AP4] [DSD2B on AP5]
001	[DSD2B on AP0] [DSD0A on AP1] [DSD0B on AP2] [DSD1A on AP3] [DSD1B on AP4] [DSD2A on AP5]
010	[DSD2A on AP0] [DSD2B on AP1] [DSD0A on AP2] [DSD0B on AP3] [DSD1A on AP4] [DSD1B on AP5]
011	[DSD1B on AP0] [DSD2A on AP1] [DSD2B on AP2] [DSD0A on AP3] [DSD0B on AP4] [DSD1A on AP5]
100	[DSD1A on AP0] [DSD1B on AP1] [DSD2A on AP2] [DSD2B on AP3] [DSD0A on AP4] [DSD0B on AP5]
101	[DSD0B on AP0] [DSD1A on AP1] [DSD1B on AP2] [DSD2A on AP3] [DSD2B on AP4] [DSD0A on AP5]
110	Reserved
111	Reserved

DSD_MAP_INV, Addr 68 (HDMI), Address 0x6D[3]

A control to invert the arrangement of the DSD interface on the audio output port pins. Note the arrangement of the DSD interface on the audio output port pins is determined by **DSD_MAP_ROT[2:0]**.

Function

DSD_MAP_INV	Description
0 (default)	Do not invert arrangement of the DSD channels on the audio output port pins
1	Invert arrangement of the DSD channels on the audio output port pins

DSD_MAP_ROT[2:0] and **DSD_MAP_INV** are independent controls. Any combination of values is therefore allowed for **DSD_MAP_ROT[2:0]** and **DSD_MAP_INV**. Table 17 and Table 18 show examples of mappings for the DSD signals.

Table 17. Audio Mapping for DSD_MAP_ROT = 00, DSD_MAP_INV = 0 (Default)

Output Pixel Port Name	DSD Interface
AP0	DSD0A
AP1	DSD0B
AP2	DSD1A
AP3	DSD1B
AP4	DSD2A
AP5	DSD2B

Table 18. Audio Mapping for DSD_MAP_ROT = 00, DSD_MAP_INV = 1

Output Pixel Port Name	DSD Interface
AP0	DSD2B
AP1	DSD2A
AP2	DSD1B
AP3	DSD1A
AP4	DSD0B
AP5	DSD0A

Notes

DSD0A and DSD0B output must be used when in stereo mode only. DSD0A and DSD0B always carry the main two-channel audio data.

DSD1A, DSD1B, DSD2A, and DSD2B are the surround channels.

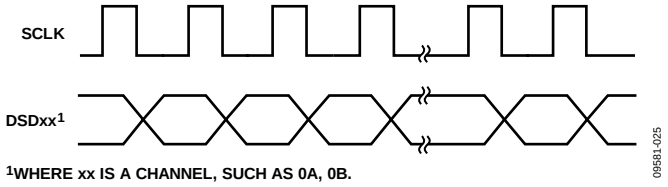


Figure 26. DSD Timing Diagram

By default, the ADV7619 automatically enables the DSD interface if it receives DSD packets. The ADV7619 also automatically enables the I²S interface if it receives audio sample packets or if it does not receive any audio packets. However, it is possible to override the audio interface that is used via the OVR_AUTO_MUX_DSD_OUT and MUX_DSD_OUT controls.

OVR_AUTO_MUX_DSD_OUT, Addr 68 (HDMI), Address 0x01[3]

DSD/DST override control. In automatic control, DSD or I²S interface is selected according to the type of packet received. DSD/DST interface enabled if part receives DSD or DST audio sample packet. I²S interface is enabled when part receives audio sample packets or when no packet is received. In manual mode, MUX_DSD_OUT selects the output interface.

Function

OVR_AUTO_MUX_DSD_OUT	Description
0 (default)	Automatic DSD/DST output control
1	Override DSD/DST output control

MUX_DSD_OUT, Addr 68 (HDMI), Address 0x01[4]

An override control for the DSD output.

Function

MUX_DSD_OUT	Description
0 «	Override by outputting I²S data
1	Override by outputting DSD/DST data

HBR Interface and Output Controls

The ADV7619 can receive HBR audio stream packets. The ADV7619 outputs HBR data over four of the audio output pins in any of the following formats:

- An SDPIF stream conforming to the IEC60958 specification (refer to Figure 23). The following configuration is required to output an SPDIF stream on the HBR output pins:
  - **OVR_MUX_HBR** is set to 0 or
  - **OVR_MUX_HBR** is set to 1 and **MUX_HBR_OUT** is set to 1.
- A binary stream, if one of the following configurations is used:
  - **OVR_MUX_HBR** is set to 1, **MUX_HBR_OUT** is set to 0, and **I2SOUTMODE[1:0]** is set to 0x0 for an I²S mode binary stream (refer to Figure 20).
  - **OVR_MUX_HBR** is set to 1, **MUX_HBR_OUT** is set to 0, and **I2SOUTMODE[1:0]** is set to 0x1 for a right justified stream (refer to Figure 21).
  - **OVR_MUX_HBR** is set to 1, **MUX_HBR_OUT** is set to 0, and **I2SOUTMODE[1:0]** is set to 0x2 for a left justified stream (refer to Figure 22).
  - Note that no audio flags are output by the part in these configurations.
- An AES3 stream on each HBR interface output pin (refer to Figure 24 and Figure 25). The following configuration is required to output AES3 streams:
  - **OVR_MUX_HBR** is set to 1.
  - **I2SOUTMODE[1:0]** is set to 0b11.

Important:

- Each of the four HBR outputs carry one of four consecutive blocks of the HBR stream
- The four streams on the four HBR pin are output at one quarter of the audio sample rate, fs

Table 19. HBR Interface Description

HBR Interface IO	Function
AP1	1st block of HBR stream.
AP2	2nd block of HBR stream
AP3	3rd block of HBR stream
AP4	4th block of HBR stream
SCLK	Bit clock
LRCLK	Data output clock for left and right channel
MCLKOUT	Audio master clock output

Note:

- The audio output mapping controls: **I2S_SPDIF_MAP_ROT[1:0]** and **I2S_SPDIF_MAP_INV** also apply to the HBR output signals.
- The audio output interface pin AP0 will also carry the SPDIF0 output, regardless of **I2S_SPDIF_MAP_ROT[1:0]** and **I2S_SPDIF_MAP_INV.**

OVR_MUX_HBR, Addr 68 (HDMI), Address 0x01[2]

A control to select automatic or manual configuration for HBR outputs. Automatically, HBR outputs are encoded as SPDIF streams. In manual mode, MUX_HBR_OUT selects the audio output interface.

Function

OVR_MUX_HBR	Description
0 (default)	Automatic HBR output control
1	Manual HBR output control

MUX_HBR_OUT, Addr 68 (HDMI), Address 0x01[1]

A control to manually select the audio output interface for HBR data. Valid when **OVR_MUX_HBR** is set to 1.

Function

MUX_HBR_OUT	Description
0 (default)	Override by outputting I²S data
1	Override by outputting SPDIF data

MCLKOUT SETTING

The frequency of audio master clock MCLKOUT is set using the MCLK_FS_N[2:0] register, as shown in Equation 3, in the relationship between MCLKOUT, MCLKFS_N, and f_s.

$$MCLKOUT = (MCLKFS\_N[2:0] + 1) \times 128 \times f_S \quad (3)$$

MCLK_FS_N[2:0], Addr 4C (DPLL), Address 0xB5[2:0]

Selects the frequency of MCLK out as multiple of 128 fs.

Function

MCLK_FS_N[2:0]	Description
000	128 fs
001 (default)	256 fs
010	384 fs
011	512 fs
100	640 fs
101	768 fs
110	Not valid
111	Not valid

AUDIO CHANNEL MODE

AUDIO_CH_MD_RAW indicates if 2-channel audio data or multichannel audio data is received.

AUDIO_CH_MD_RAW, IO, Address 0x65[4] (Read Only)

Raw status signal indicating the layout value of the audio packets that were last received.

Function

AUDIO_CH_MD_RAW	Description
0	The last audio packets received have a layout value of 1. (For example, Layout-1 corresponds to 2-channel audio when audio sample packets are received.)
1	The last audio packets received have a layout value of 0. (For example, Layout-0 corresponds to 8-channel audio when audio sample packets are received.)

Note: The Audio CH_MD_RAW flag is valid for audio sample packets and DSD packets.

AUDIO_CHANNEL_MODE, Addr 68 (HDMI), Address 0x07[6] (Read Only)

Flags stereo or multichannel audio packets. Note stereo packets may carry compressed multichannel audio.

Function

AUDIO_CHANNEL_MODE	Description
0	Stereo audio (may be compressed multichannel)
1	Multichannel uncompressed audio detected (Channel 3 to Channel 8).

AUDIO MUTING

The ADV7619 integrates an advanced audio mute function that is designed to remove all extraneous noise and pops from a 2-channel L-PCM audio stream at sample frequencies up to 48 kHz.

The hardware for audio mute function is composed of the following three blocks:

- Audio delay line that delays Channel 1 and Channel 2 by 512 stereo samples.
- Audio mute controller takes in event detection signals that can be used to determine when an audio mute is needed. The controller generates a mute signal to the ramped audio block and a coast signal to the digital PLL generating the audio clock.
- Ramped audio mute block that can mute the audio over the course of 512 stereo samples.

Notes

- The ADV7619 mutes only the noncompressed data from the audio sample packets output through the I^2S and the SPDIF interface.
- The audio delay line is automatically bypassed when the ADV7619 receives multichannel audio or when it receives the following audio packets:
  - DSD packets
  - HBR packets
- The ramped audio mute block is always bypassed when the part received compressed audio or when it received the following audio packets:
  - DSD packets
  - HBR packets

Delay Line Control

The audio delay line should be enabled when the ADV7619 is configured for automatic mute. The audio delay line is controlled by the **MAN_AUDIO_DL_BYPASS** and **AUDIO_DELAY_LINE_BYPASS** bits.

MAN_AUDIO_DL_BYPASS, Addr 68 (HDMI), Address 0x0F[7]

Audio delay bypass manual enable. The audio delay line is automatically active for stereo samples and bypassed for multichannel samples. By setting MAN_AUDIO_DL_BYPASS to 1, the audio delay bypass configuration can be set by the user with the AUDIO_DELAY_LINE_BYPASS control.

Function

MAN_AUDIO_DL_BYPASS	Description
0 (default)	Audio delay line is automatically bypassed if multichannel audio is received. The audio delay line is automatically enabled if stereo audio is received.
1	Overrides automatic bypass of audio delay line. Audio delay line is applied depending on the AUDIO_DELAY_LINE_BYPASS control.

AUDIO_DELAY_LINE_BYPASS, Addr 68 (HDMI), Address 0x0F[6]

Manual bypass control for the audio delay line. Only valid if MAN_AUDIO_DL_BYPASS is set to 1.

Function

AUDIO_DELAY_LINE_BYPASS	Description
0 (default)	Enables the audio delay line
1	Bypasses the audio delay line

Audio Mute Configuration

The ADV7619 can be configured to automatically mute an L-PCM audio stream when selectable mute conditions occur. The audio muting is configured as follows:

- Set the audio muting speed via **AUDIO_MUTE_SPEED[4:0]**.
- Set **NOT_AUTO_UNMUTE**, as follows:
  - Set NOT_AUDIO_UNMUTE[2:0] to 0 if the audio must be unmuted automatically after a delay set in **WAIT_UNMUTE[2:0]** after all selected mute conditions have become inactive.

    - Set NOT_AUTO_UNMUTE to 1 if the audio must be unmuted manually (for example, by an external controller) when all selected mute conditions have become inactive.
    - Select the mute conditions that trigger an audio mute (refer to Table 20).
- Select the Audio PLL coast conditions (refer to the Audio DPLL Coast Feature section).
- Set **WAIT_UNMUTE[2:0]** to configure the audio counter that triggers the audio unmute when it has timed out after all selected mute conditions have become inactive.

The ADV7619 internally unmutes the audio if the following three conditions (listed in order of priority) are met:

- Mute conditions are inactive.
- **NOT_AUTO_UNMUTE** is set to 0.
- Audio unmute counter has finished counting down or is disabled.

Notes

- Both Table 10 and Table 20 provide a column with the heading: Corresponding Status Register(s). This column lists the status registers that convey information related to their corresponding audio mute masks or coast masks.
- The ADV7619 also mutes the DSD stream when one of the selected mute conditions occurs (refer to Table 20) by outputting the DSD mute pattern 0101010101… A DSD decoder receiving this stream outputs a 0 V mean analog stream.
- The ADV7619 can mute the audio data with compressed audio data or HBR packets. In these cases mute will output constant stream of 0
- For the best audio muting performance, the following setting is recommended when the ADV7619 receives multichannel sample packets:
    - Set AUDIO_MUTE_SPEED to 1
- For best audio muting performance, the following settings are recommended when the audio sampling frequency of the audio stream is greater than 48 kHz:
    - Set AUDIO_MUTE_SPEED to 1
    - Set MAN_AUDIO_DL_BYPASS to 1
    - Set AUDIO_DELAY_LINE_BYPASS to 1
- For best audio muting performance, the following settings are recommended when the audio sampling frequency of the audio stream is equal to or lower than 48 kHz:
    - Set AUDIO_MUTE_SPEED to 0x1F
    - Set MAN_AUDIO_DL_BYPASS to 0

MUTE_AUDIO, Addr 68 (HDMI), Address 0x1A[4]

A control to force an internal mute independently of the mute mask conditions

Function

MUTE_AUDIO	Description
0 (default)	Audio in normal operation
1	Force audio mute

AUDIO_MUTE_SPEED[4:0], Addr 68 (HDMI), Address 0x0F[4:0]

Number of samples between each volume change of 1.5dB when muting and unmuting

Function

AUDIO_MUTE_SPEED[4:0]	Description
0x1F (default)	Default value

NOT_AUTO_UNMUTE, Addr 68 (HDMI), Address 0x1A[0]

A control to disable the auto unmute feature. When set to 1, audio can be unmuted manually if all mute conditions are inactive by setting NOT_AUTO_UNMUTE to 0 and then back to 1.

Function

NOT_AUTO_UNMUTE	Description
0 (default)	Audio unmutes following a delay set by WAIT_UNMUTE after all mute conditions have become inactive
1	Prevents audio from unmuting automatically

WAIT_UNMUTE[2:0], Addr 68 (HDMI), Address 0x1A[3:1]

A control to delay audio unmute. Once all mute conditions are inactive WAIT_UNMUTE[2:0] can specify a further delay time before unmuting. NOT_AUTO_UNMUTE must be set to 0 for this control to be effective.

Function

WAIT_UNMUTE[2:0]	Description
000 (default)	Disables/cancels delayed unmute. Audio unmutes directly after all mute conditions become inactive.
001	Unmutes 250 ms after all mute conditions become inactive.
010	Unmutes 500 ms after all mute conditions become inactive.
011	Unmutes 750 ms after all mute conditions become inactive.
100	Unmutes 1 sec after all mute conditions become inactive.

Table 20. Selectable Mute Conditions

Bit Name	HDMI Map Address	Description	Corresponding Status Register(s)
MT_MSK_COMPRS_AUD	0x14[5]	Causes audio mute if audio is compressed	CS_DATA[1]
MT_MSK_AUD_MODE_CHNG	0x14[4]	Causes audio mute if audio mode changes between PCM, DSD, DST, or HBR formats	**AUDIO_SAMPLE_PCKT_DET**
MT_MSK_PARITY_ERR	0x14[1]	Causes audio mute if parity bits in audio samples are not correct	PARITY_ERROR_RAW
MT_MSK_VCLK_CHNG	0x14[0]	Causes audio mute if TMDS clock has irregular/missing pulses	VCLK_CHNG_RAW
MT_MSK_APLL_UNLOCK	0x15[7]	Causes audio mute if audio PLL unlocks	**AUDIO_PLL_LOCKED**
MT_MSK_VPLL_UNLOCK	0x15[6]	Causes audio mute if TMDS PLL unlocks	TMDS_PLL_LOCKED
MT_MSK_ACR_NOT_DET	0x15[5]	Causes audio mute if ACR packets are not received within one VSync	**AUDIO_C_PCKT_RAW**
MT_MSK_FLATLINE_DET	0x15[3]	Causes audio mute if flatline bit in audio packets is set	AUDIO_FLT_LINE_RAW
MT_MSK_FIFO_UNDERFLOW	0x15[1]	Causes audio mute if audio FIFO underflows	FIFO_UNDERFLO_RAW
MT_MSK_FIFO_OVERFLOW	0x15[0]	Causes audio mute if audio FIFO overflows	FIFO_OVERFLO_RAW
MT_MSK_AVMUTE	0x16[7]	Causes audio mute if AVMute is set in the general control packet	AV_MUTE_RAW
MT_MSK_NOT_HDMIMODE	0x16[6]	Causes audio mute if HDMI_MODE bit goes low	HDMI_MODE
MT_MSK_NEW_CTS	0x16[5]	Causes audio mute if CTS changes by more than the threshold set in **CTS_CHANGE_THRESHOLD[5:0]**	**CTS_PASS_THRSH_RAW**
MT_MSK_NEW_N	0x16[4]	Causes audio mute if N changes	**CHANGE_N_RAW**
MT_MSK_CHMODE_CHNG	0x16[3]	Causes audio mute if the channel mode changes from stereo to multichannel, or vice versa	AUDIO_MODE_CHNG_RAW
MT_MSK_APCKT_ECC_ERR	0x16[2]	Causes audio mute if uncorrectable error is detected in the audio packets by the ECC block	AUDIO_PCKT_ERR_RAW
MT_MSK_CHNG_PORT	0x16[1]	Causes audio mute if HDMI port is changed	**HDMI_PORT_SELECT[2:0]**
MT_MSK_VCLK_DET	0x16[0]	Causes audio mute if TMDS clock is not detected	TMDS_CLK_A_RAW

Internal Mute Status

The internal mute status is provided through the INTERNAL_MUTE_RAW bit.

INTERNAL_MUTE_RAW, IO, Address 0x65[6] (Read Only)

Raw status signal of internal mute signal.

Function

INTERNAL_MUTE_RAW	Description
0 (default)	Audio is not muted
1	Audio is muted

AV Mute Status

AV_MUTE, Addr 68 (HDMI), Address 0x04[6] (Read Only)

Readback of AVMUTE status received in the last general control packet received.

Function

AV_MUTE	Description
0 (default)	AVMUTE not set
1	AVMUTE set

Audio Mute Signal

The ADV7619 can output an audio mute signal that can be used to control the muting in a back end audio device processing the audio data output by the ADV7619 (for example, DSP).

The audio mute signal is output on the INT1 pin by setting **EN_UMASK_RAW_INTRQ** to 1. The mute signal is active high.

The audio mute signal can also be output on the INT2 signal (via one of the following pins: SCLK/INT2, HPA_A/INT2 or MCLK/INT2) by setting **INTRQ2_MUX_SEL[1:0]** to 1 and EN_MUTE_OUT_INTRQ2 to 1.

Important

The ADV7619 may interface with an audio processor (for example, DSP) in which the muting of the audio is implemented. In this case, the audio processor typically features a delay line followed by a mute block for audio mute and unmuting purposes. The following hardware and software configuration is recommended for optimum muting performance of the ADV7619 and audio processor system:

- Connect the mute signal of the ADV7619 to the audio processor mute input. The ADV7619 mute signal can now drive the muting/unmuting of the audio data inside the audio processor.
- Bypass the audio delay line of the ADV7619 with the following settings:
  - Set **MAN_AUDIO_DL_BYPASS** to 1.
  - Set **AUDIO_DELAY_LINE_BYPASS** to 1.
  - Configure the ADV7619 to mute the audio over one audio sample clock as follows:
    - Set **AUDIO_MUTE_SPEED[4:0]** to 1. This ensures that the ADV7619 never outputs invalid audio data out to the audio processor.

EN_UMASK_RAW_INTRQ, IO Map, Address 0x40[3]

A control to apply the audio mute signal on INT1 interrupt pin.

Function

EN_UMASK_OUT_INTRQ	Description
0 (default)	Does not output raw interrupt flag on INT1
1	Outputs raw interrupt flag on INT1

EN_UMASK_RAW_INTRQ2, IO Map, Address 0x41[3]

A control to apply the internal audio mute signal on INT2 interrupt pin.

Function

EN_UMASK_OUT_INTRQ2	Description
0 (default)	Does not output raw interrupt flag on INT2
1	Outputs raw interrupt flag on INT2

Audio Stream with Incorrect Parity Error

The ADV7619 discards audio sample packets that have an incorrect parity bit. When these samples are received, the ADV7619 repeats the previous audio sample with a valid parity bit. The audio stream out of the ADV7619 can be muted in this situation if the audio mute mask MT_MSK_PARITY_ERR is set.

It is possible to configure the ADV7619 so that it processes audio sample packets that have an incorrect parity bit and corrects the parity bit. The ADV7619 can then output an audio stream even when the parity bits from the audio sample packet are invalid. This configuration is activated by setting MT_MSK_PARITY_ERR 0 and IGNORE_PARITY_ERR to 1.

IGNORE_PARITY_ERR, Addr 68 (HDMI), Address 0x1A[6]

A control to select the processing of audio samples even when they have a parity error.

Function

IGNORE_PARITY_ERR	Description
0 (default)	Discard audio sample packets that have an invalid parity bit
1	Process audio sample packets that have an invalid parity bit

MT_MSK_PARITY_ERR, Addr 68 (HDMI), Address 0x14[1]

Audio mute mask for a parity error. It sets the audio mutes if an audio sample packet is received with an incorrect parity bit.

Function

MT_MSK_PARITY_ERR	Description
1 (default)	Audio mute occurs if an audio sample packet is received with an incorrect parity bit

AUDIO CLOCK REGENERATION PARAMETERS

The ADV7619 recreates an internal audio master clock using audio clock regeneration (ACR) values transmitted by the HDMI source.

ACR Parameters Readbacks

The registers N and CTS can be read back from the HDMI map.

CTS[19:0], Addr 68 (HDMI), Address 0x5B[7:0]; Address 0x5C[7:0]; Address 0x5D[7:4] (Read Only)

A readback for the CTS value received in the HDMI data stream.

Function

CTS[19:0]	Description
00000000000000000000 (default)	Default CTS value readback from HDMI stream
xxxxxxxxxxxxxxxxxxxx	CTS value readback from HDMI stream

N[19:0], Addr 68 (HDMI), Address 0x5D[3:0]; Address 0x5E[7:0]; Address 0x5F[7:0] (Read Only)

A readback for the N value received in the HDMI data stream.

Function

N[19:0]	Description
00000000000000000000 (default)	Default N value readback from HDMI stream
xxxxxxxxxxxxxxxxxxxx	N value readback from HDMI stream

Note: A buffer has been implemented for the N and CTS readback registers. A read of the HDMI map, Address 0x5B register updates the buffer that stores the N and CTS readback registers. The buffer implemented for N and CTS readback allows the reading of both N and CTS registers within an I^2C block read.

Monitoring ACR Parameters

The reception of ACR packets can be notified via the **AUDIO_C_PCKT_RAW** flag. Changes in N and CTS can be monitored via the **CHANGE_N_RAW** and **CTS_PASS_THRSH_RAW** flags, as described in this section.

AUDIO_C_PCKT_RAW, IO, Address 0x65[1] (Read Only)

Raw status signal of audio clock regeneration packet detection signal.

Function

AUDIO_C_PCKT_RAW	Description
0 (default)	No audio clock regeneration packets received since the last HDMI reset condition
1	Audio clock regeneration packets received

CHANGE_N_RAW, IO, Address 0x7E[3] (Read Only)

Status of the ACR N Value changed interrupt signal. When set to 1 it indicates the N Value of the ACR packets has changed. Once set, this bit will remain high until it is cleared via CHANGE_N_CLR.

Function

CHANGE_N_RAW	Description
0 (default)	Audio clock regeneration N value has not changed.
1	Audio clock regeneration N value has changed.

CTS_PASS_THRSH_RAW, IO, Address 0x7E[4] (Read Only)

Status of the ACR CTS value exceed threshold interrupt signal. When set to 1, it indicates the CTS Value of the ACR packets has exceeded the threshold set by CTS_CHANGE_THRESHOLD. Once set, this bit will remain high until it is cleared via CTS_PASS_THRSH_CLR.

Function

CTS_PASS_THRSH_RAW	Description
0 (default)	Audio clock regeneration CTS value has not passed the threshold.
1	Audio clock regeneration CTS value has changed more than threshold.

CTS_CHANGE_THRESHOLD[5:0], Addr 68 (HDMI), Address 0x10[5:0]

Sets the tolerance for change in the CTS value. This tolerance is used for the audio mute mask MT_MSK_NEW_CTS and the HDMI status bit CTS_PASS_THRSH_RAW and the HDMI interrupt status bit CTS_PASS_THRSH_ST. This register controls the amounts of LSBs that the CTS can change before an audio mute, status change or interrupt is triggered.

Function

CTS_CHANGE_THRESHOLD[5:0]	Description
100101 (default)	Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS
xxxxxx	Tolerance of CTS value for CTS_PASS_THRSH_RAW and MT_MSK_NEW_CTS

CHANNEL STATUS

Channel status bits are extracted from the HDMI audio packets of the 1st audio channel (that is, Channel 0) and stored in registers CHANNEL_STATUS_DATA_X of the HDMI Map (where X = 1, 2, 3, 4, and 5).

Validity Status Flag

The channel status readback described in the Channel Status section should be considered valid if **CS_DATA_VALID_RAW** is set to 1. Figure 27 shows the algorithm that can be implemented to monitor the read valid channel status bit using the CS_DATA_VALID_RAW flag.

CS_DATA_VALID_RAW, IO, Address 0x65[7] (Read Only)

Raw status signal of channel status data valid signal.

Function

CS_DATA_VALID_RAW	Description
0 (default)	Channel status data is not valid.
1	Channel status data is valid.

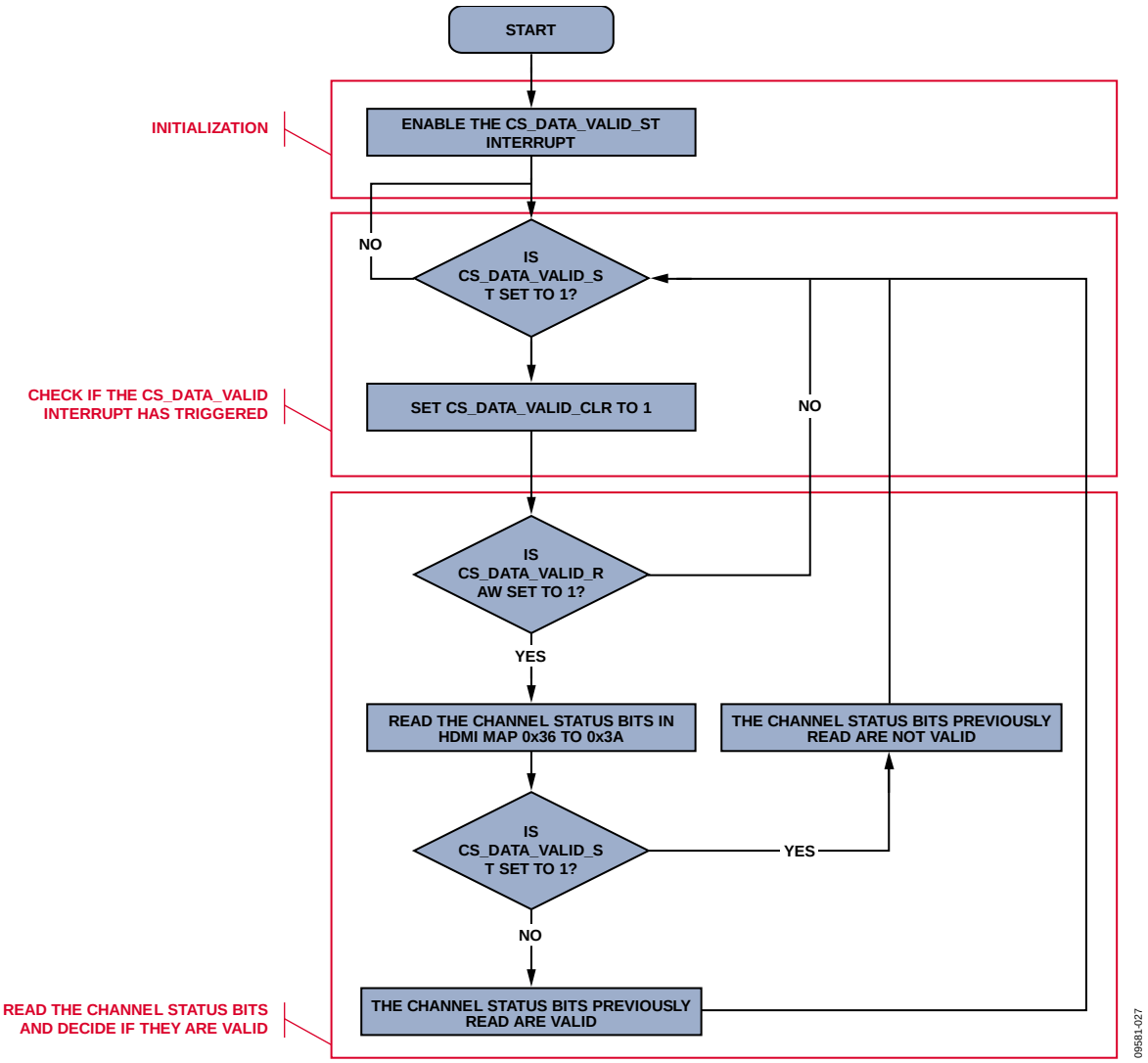


Figure 27. Reading Valid Channel Status Flags

Notes

- CS_DATA_VALID_RAW indicates that the first 40 of the channel status bits sent by the upstream transmitter have been correctly collected. This bit does not indicate if the content of the channel status bit is corrupted as this is indeterminable.
- A corresponding interrupt can be enabled for CS_DATA_VALID_RAW by setting the mask CS_DATA_VALID_MB1 or CS_DATA_VALID_MB2. Refer to the Interrupts section for additional information on the interrupt feature.

General Control and Mode Information

The general control and mode information are specified in Byte 0 of the channel status. For more information, refer to the IEC60958 standards.

CS_DATA[0], Consumer/Professional Application, HDMI Map, Address 0x36[0]

Function

CS_DATA[0]	Description
0 (default)	Consumer application
1	Professional application

CS_DATA[1], PCM/non-PCM Audio Sample, HDMI Map, Address 0x36[1]

Function

CS_DATA[1]	Description
0 (default)	Audio sample word represents linear PCM samples
1	Audio sample word used for other purposes

CS_DATA[2], Copyright, HDMI Map, Address 0x36[2]

Function

CS_DATA[2]	Description
0 (default)	Software for which copyright is asserted
1	Software for which no copyright is asserted

CS_DATA[5:3], Emphasis, HDMI Map, Address 0x36[5:3]

Function

CS_DATA[5:3][1]	Description
000 (default)	Two audio channels without pre-emphasis
001	Two audio channels with 50/15 pre-emphasis

[1] Unspecified values are reserved.

CS_DATA[7:6], Channel Status Mode, HDMI Map, Address 0x36[7:6]

Function

CS_DATA[7:6][1]	Description
00 (default)	Mode 0

[1] Unspecified values are reserved.

Category Code

The category code is specified in Byte 1 of the channel status. The category code indicates the type of equipment that generates the digital audio interface signal. For more information, refer to the IEC60958 standards.

CS_DATA[15:8], Category Code, HDMI Map, Address 0x37[7:0]

Function

CS_DATA[15:8]	Description
xxxx xxxx	Category code[1]
0000 0000 (default)	Reset value

[1] Refer to IEC60958-3 standards.

Source Number and Channel Number

CS_DATA[19:16], Source Number, HDMI Map, Address 0x38[3:0]

Function

CS_DATA[19:16]	Description
xxxx	Source number[1]
0000 (default)	Reset value

[1] Refer to IEC60958-3 standards.

CS_DATA[23:20], Channel Number, HDMI Map, Address 0x38[7:4]

Function

CS_DATA[23:20]	Description
xxxxx	Channel number[1]
00000 (default)	Reset value

[1] Refer to IEC60958-3 standards.

Sampling and Frequency Accuracy

The sampling frequency and clock accuracy are specified by Byte 3 of the channel status. For additional information, refer to the IEC60958 standards.

CS_DATA[27:24], Sampling Frequency, HDMI Map, Address 0x39[3:0]

Function

CS_DATA[27:24][1]	Description
0000 (default)	44.1 kHz
0010	48 kHz
0011	32 kHz
1000	88.2 kHz
1001	768 kHz
1010	96 kHz
1100	176 kHz
1110	192 kHz

[1] Unspecified values are reserved.

CS_DATA[29:28], Clock Accuracy, HDMI Map, Address 0x39[5:4]

Function

CS_DATA[29:28]	Description
00 (default)	Level II, ±1000 ppm
01	Level I, ±50 ppm
10	Level III, variable pitch shifted
11	Reserved

CS_DATA[31:30], Reserved Register, HDMI Map, Address 0x39[7:6]

Function

CS_DATA[31:30]	Description
XX	Reserved
00 (default)	Reset value

Word Length

Word length information is specified in Byte 4 of the channel status bit. For more information, refer to the IEC60958 standards.

CS_DATA[32], Maximum Word Length Size, HDMI Map, Address 0x3A, [0]

Function

CS_DATA[32]	Description
0 (default)	Maximum audio sample word length is 20 bits.
1	Maximum audio sample word length is 24 bits.

CS_DATA[35:33], Word Length, HDMI Map, Address 0x3A, [3:1]

Function

CS_DATA[35:33][1]	Description	
	Audio sample word length if maximum length is 24 as indicated by CS_DATA_[32]	Audio sample word length if maximum length is 20 as indicated by CS_DATA_[32]
000 (default)	Word length not indicated	Word length not indicated
001	20 bits	16 bits
010	22 bits	18 bits
100	23 bits	19 bits
101	24 bits	20 bits
110	21 bits	21 bits

[1] Unspecified values are reserved.

Channel Status Copyright Value Assertion

It is possible to overwrite the copyright value of the channel status bit that is passed to the SPDIF output. This is done via the **CS_COPYRIGHT_MANUAL** and **CS_COPYRIGHT_VALUE** controls.

CS_COPYRIGHT_MANUAL, Addr 68 (HDMI), Address 0x50[1]

A control to select automatic or manual setting of the copyright value of the channel status bit that is passed to the SPDIF output. Manual control is set with the CS_COPYRIGHT_VALUE bit.

Function

CS_COPYRIGHT_MANUAL	Description
0 (default)	Automatic CS copyright control.
1	Manual CS copyright control. Manual value is set by CS_COPYRIGHT_VALUE.

CS_COPYRIGHT_VALUE, Addr 68 (HDMI), Address 0x50[0]

A control to set the CS copyright value when in manual configuration of the CS copyright bit that is passed to the SPDIF output.

Function

CS_COPYRIGHT_VALUE	Description
0 (default)	Copyright value of channel status bit is 0. Valid only if CS_COPYRIGHT_MANUAL is set to 1.
1	Copyright value of channel status bit is 1. Valid only if CS_COPYRIGHT_MANUAL is set to 1.

Monitoring Change of Audio Sampling Frequency

The ADV7619 features the NEW_SAMP_RT_RAW flag to monitor changes in the audio sampling frequency field of the channel status bits.

NEW_SAMP_RT_RAW, IO, Address 0x83[3] (Read Only)

Status of new sampling rate interrupt signal. When set to 1, it indicates that audio sampling frequency field in channel status data has changed. Once set, this bit will remain high until it is cleared via NEW_SAMP_RT _CLR.

Function

NEW_SAMP_RT_RAW	Description
0 (default)	Sampling rate bits of the channel status data on audio Channel 0 have not changed.
1	Sampling rate bits of the channel status data on audio Channel 0 have changed.

Important

The **NEW_SAMP_RT_RAW** flag does not trigger if **CS_DATA_VALID_RAW** is set to 0. This prevents the notification of a change from a valid to an invalid audio sampling frequency readback in the channel status bits, and vice versa.

PACKETS AND INFOFRAMES REGISTERS

In HDMI, auxiliary data is carried across the digital link using a series of packets. The ADV7619 automatically detects and stores the following HDMI packets:

- InfoFrames
- Audio content protection (ACP)
- International standard recording code (ISRC)
- Gamut metadata

When the ADV7619 receives one of these packets, it computes the packet checksum and compares it with the checksum available in the packet. If these checksums are the same, the packets are stored in the corresponding registers. If the checksums are not the same, the packets are discarded. Refer to the EIA/CEA-861D specifications for more information on the packets fields.

InfoFrames Registers

The ADV7619 can store the following InfoFrames:

- Auxiliary video information (AVI) InfoFrame
- Source production descriptor (SPD) InfoFrame
- Audio InfoFrame
- Moving picture expert group (MPEG) source InfoFrame

InfoFrame Collection Mode

The ADV7619 has two modes for storing the InfoFrame packet sent from the source into the internal memory. By default, the ADV7619 only stores the InfoFrame packets received if the checksum is correct for each InfoFrame.

The ADV7619 also provides a mode to store every InfoFrame sent from the source, regardless of a InfoFrame packet checksum error.

ALWAYS_STORE_INF, Addr 68 (HDMI), Address 0x47[0]

A control to force InfoFrames with checksum errors to be stored.

Function

ALWAYS_STORE_INF	Description
0 (default)	Stores data from received InfoFrames only if their checksum is correct
1	Always store the data from received InfoFrame regardless of their checksum

InfoFrame Checksum Error Flags

The following checksum error status registers flag when the last InfoFrame received has a checksum error. Once set, these bits remain high until the interrupt is cleared via their corresponding clear bits.

AVI_INF_CKS_ERR_RAW, IO, Address 0x88[4] (Read Only)

Status of AVI InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an AVI InfoFrame. Once set, this bit remains high until it is cleared via AVI_INF_CKS_ERR_CLR.

Function

AVI_INF_CKS_ERR_RAW	Description
0 (default)	No AVI InfoFrame checksum error has occurred.
1	An AVI InfoFrame checksum error has occurred.

AUD_INF_CKS_ERR_RAW, IO, Address 0x88[5] (Read Only)

Status of audio InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an audio InfoFrame. Once set, this bit remains high until it is cleared via AUDIO_INF_CKS_ERR_CLR.

Function

AUD_INF_CKS_ERR_RAW	Description
0 (default)	No audio InfoFrame checksum error has occurred.
1	An audio InfoFrame checksum error has occurred.

SPD_INF_CKS_ERR_RAW, IO, Address 0x88[6] (Read Only)

Status of SPD InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an SPD InfoFrame. Once set, this bit remains high until it is cleared via ASPD_INF_CKS_ERR_CLR.

Function

SPD_INF_CKS_ERR_RAW	Description
0 (default)	No SPD InfoFrame checksum error has occurred.
1	An SPD InfoFrame checksum error has occurred.

MS_INF_CKS_ERR_RAW, IO, Address 0x88[7] (Read Only)

Status of MPEG source InfoFrame checksum error interrupt signal. When set to 1. it indicates that a checksum error has been detected for an MPEG source InfoFrame. Once set, this bit remains high until it is cleared via MS_INF_CKS_ERR_CLR.

Function

MS_INF_CKS_ERR_RAW	Description
0 (default)	No MPEG source InfoFrame checksum error has occurred.
1	An MPEG source InfoFrame checksum error has occurred.

VS_INF_CKS_ERR_RAW, IO, Address 0x8D[0] (Read Only)

Status of vendor specific InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an Vendor Specific InfoFrame. Once set, this bit will remain high until it is cleared via VS_INF_CKS_ERR_CLR.

Function

VS_INF_CKS_ERR_RAW	Description
0 (default)	No VS InfoFrame checksum error has occurred
1	A VS InfoFrame checksum error has occurred

AVI InfoFrame Registers

Table 21 provides a list of readback registers for the AVI InfoFrame data. Refer to the EIA/CEA-861D specifications for a detailed explanation of the AVI InfoFrame fields.

Table 21. AVI InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE0	R/W	**AVI_PACKET_ID[7:0]**	Packet type value
0xE1	R	AVI_INF_VER	InfoFrame version number
0xE2	R	AVI_INF_LEN	InfoFrame length
0x00	R	AVI_INF_PB_0_1	Checksum
0x01	R	AVI_INF_PB_0_2	Data Byte 1
0x02	R	AVI_INF_PB_0_3	Data Byte 2
0x03	R	AVI_INF_PB_0_4	Data Byte 3
0x04	R	AVI_INF_PB_0_5	Data Byte 4
0x05	R	AVI_INF_PB_0_6	Data Byte 5
0x06	R	AVI_INF_PB_0_7	Data Byte 6
0x07	R	AVI_INF_PB_0_8	Data Byte 7
0x08	R	AVI_INF_PB_0_9	Data Byte 8
0x09	R	AVI_INF_PB_0_10	Data Byte 9
0x0A	R	AVI_INF_PB_0_11	Data Byte 10
0x0B	R	AVI_INF_PB_0_12	Data Byte 11
0x0C	R	AVI_INF_PB_0_13	Data Byte 12
0x0D	R	AVI_INF_PB_0_14	Data Byte 13
0x0E	R	AVI_INF_PB_0_15	Data Byte 14
0x0F	R	AVI_INF_PB_0_16	Data Byte 15
0x10	R	AVI_INF_PB_0_17	Data Byte 16
0x11	R	AVI_INF_PB_0_18	Data Byte 17
0x12	R	AVI_INF_PB_0_19	Data Byte 18
0x13	R	AVI_INF_PB_0_20	Data Byte 19
0x14	R	AVI_INF_PB_0_21	Data Byte 20
0x15	R	AVI_INF_PB_0_22	Data Byte 21
0x16	R	AVI_INF_PB_0_23	Data Byte 22
0x17	R	AVI_INF_PB_0_24	Data Byte 23
0x18	R	AVI_INF_PB_0_25	Data Byte 24
0x19	R	AVI_INF_PB_0_26	Data Byte 25
0x1A	R	AVI_INF_PB_0_27	Data Byte 26
0x1B	R	AVI_INF_PB_0_28	Data Byte 27

[1] As defined by the EIA/CEA-861D specifications.

The AVI InfoFrame registers are considered valid if the following two conditions are met:

- **AVI_INFO_RAW** is 1.
- **AVI_INF_CKS_ERR_RAW** is 0. This condition applies only if **ALWAYS_STORE_INF** is set to 1.

AVI_INFO_RAW is described in the Interrupt Architecture Overview section.

Audio InfoFrame Registers

Table 22 provides the list of readback registers available for the Audio InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the audio InfoFrame fields.

Table 22. Audio InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE3	R/W	**AUD_PACKET_ID[7:0]**	Packet type value
0xE4	R	AUD_INF_VERS	InfoFrame version number
0xE5	R	AUD_INF_LEN	InfoFrame length
0x1C	R	AUD_INF_PB_0_1	Checksum
0x1D	R	AUD_INF_PB_0_2	Data Byte 1
0x1E	R	AUD_INF_PB_0_3	Data Byte 2
0x1F	R	AUD_INF_PB_0_4	Data Byte 3
0x20	R	AUD_INF_PB_0_5	Data Byte 4
0x21	R	AUD_INF_PB_0_6	Data Byte 5
0x22	R	AUD_INF_PB_0_7	Data Byte 6
0x23	R	AUD_INF_PB_0_8	Data Byte 7
0x24	R	AUD_INF_PB_0_9	Data Byte 8
0x25	R	AUD_INF_PB_0_10	Data Byte 9
0x26	R	AUD_INF_PB_0_11	Data Byte 10
0x27	R	AUD_INF_PB_0_12	Data Byte 11
0x28	R	AUD_INF_PB_0_13	Data Byte 12
0x29	R	AUD_INF_PB_0_14	Data Byte 13

[1] As defined by the EIA/CEA-861D specifications.

The audio InfoFrame registers are considered valid if the following two conditions are met:

- **AUDIO_INFO_RAW** is 1.
- **AUD_INF_CKS_ERR_RAW** is 0. This condition applies only if **ALWAYS_STORE_INF** is set to 1.

AUDIO_INFO_RAW, IO, Address 0x60[1] (Read Only)

Raw status of audio InfoFrame detected signal.

Function

AUDIO_INFO_RAW	Description
0 (default)	No AVI InfoFrame has been received within the last three VSyncs or since the last HDMI packet detection reset.
1	An Audio InfoFrame has been received within the last three VSyncs. This bit will reset to zero on the fourth VSync leading edge following an Audio InfoFrame, after an HDMI packet detection reset or upon writing to AUD_PACKET_ID.

SPD InfoFrame Registers

Table 23 provides a list of readback registers available for the SPD InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the SPD InfoFrame fields.

Table 23. SPD InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE6	R/W	**SPD_PACKET_ID[7:0]**	Packet type value
0xE7	R	SPD_INF_VER	InfoFrame version number
0xE8	R	SPD_INF_LEN	InfoFrame length
0x2A	R	SPD_INF_PB_0_1	Checksum
0x2B	R	SPD_INF_PB_0_2	Data Byte 1
0x2C	R	SPD_INF_PB_0_3	Data Byte 2
0x2D	R	SPD_INF_PB_0_4	Data Byte 3
0x2E	R	SPD_INF_PB_0_5	Data Byte 4
0x2F	R	SPD_INF_PB_0_6	Data Byte 5
0x30	R	SPD_INF_PB_0_7	Data Byte 6
0x31	R	SPD_INF_PB_0_8	Data Byte 7
0x32	R	SPD_INF_PB_0_9	Data Byte 8
0x33	R	SPD_INF_PB_0_10	Data Byte 9
0x34	R	SPD_INF_PB_0_11	Data Byte 10
0x35	R	SPD_INF_PB_0_12	Data Byte 11
0x36	R	SPD_INF_PB_0_13	Data Byte 12
0x37	R	SPD_INF_PB_0_14	Data Byte 13
0x38	R	SPD_INF_PB_0_15	Data Byte 14
0x39	R	SPD_INF_PB_0_16	Data Byte 15
0x3A	R	SPD_INF_PB_0_17	Data Byte 16
0x3B	R	SPD_INF_PB_0_18	Data Byte 17
0x3C	R	SPD_INF_PB_0_19	Data Byte 18
0x3D	R	SPD_INF_PB_0_20	Data Byte 19
0x3E	R	SPD_INF_PB_0_21	Data Byte 20
0x3F	R	SPD_INF_PB_0_22	Data Byte 21
0x40	R	SPD_INF_PB_0_23	Data Byte 22
0x41	R	SPD_INF_PB_0_24	Data Byte 23
0x42	R	SPD_INF_PB_0_25	Data Byte 24
0x43	R	SPD_INF_PB_0_26	Data Byte 25
0x44	R	SPD_INF_PB_0_27	Data Byte 26
0x45	R	SPD_INF_PB_0_28	Data Byte 27

[1] As defined by the EIA/CEA-861D specifications.

The Source Product Descriptor InfoFrame registers are considered valid if the following two conditions are met:

- **SPD_INFO_RAW** is 1.
- **SPD_INF_CKS_ERR_RAW** is 0. This condition only applies if **ALWAYS_STORE_INF** is set to 1.

SPD_INFO_RAW, IO, Address 0x60[2] (Read Only)

Raw status of SPD InfoFrame detected signal.

Function

SPD_INFO_RAW	Description
0 (default)	No source product description InfoFrame received since the last HDMI packet detection reset.
1	Source product description InfoFrame received. This bit resets to zero after an HDMI packet detection reset or upon writing to SPD_PACKET_ID.

MPEG Source InfoFrame Registers

Table 24 provides a list of readback registers available for the MPEG InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the MPEG InfoFrame fields.

Table 24. MPEG InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE9	R/W	**MS_PACKET_ID[7:0]**	Packet type value
0xEA	R	MS_INF_VERS	InfoFrame version number
0xEB	R	MS_INF_LEN	InfoFrame length
0x46	R	MS_INF_PB_0_1	Checksum
0x47	R	MS_INF_PB_0_2	Data Byte 1
0x48	R	MS_INF_PB_0_3	Data Byte 2
0x49	R	MS_INF_PB_0_4	Data Byte 3
0x4A	R	MS_INF_PB_0_5	Data Byte 4
0x4B	R	MS_INF_PB_0_6	Data Byte 5
0x4C	R	MS_INF_PB_0_7	Data Byte 6
0x4D	R	MS_INF_PB_0_8	Data Byte 7
0x4E	R	MS_INF_PB_0_9	Data Byte 8
0x4F	R	MS_INF_PB_0_10	Data Byte 9
0x50	R	MS_INF_PB_0_11	Data Byte 10
0x51	R	MS_INF_PB_0_12	Data Byte 11
0x52	R	MS_INF_PB_0_13	Data Byte 12
0x53	R	MS_INF_PB_0_14	Data Byte 13

[1] As defined by the EIA/CEA-861D specifications.

The MPEG InfoFrame registers are considered valid if the following two conditions are met:

- **MS_INFO_RAW** is 1.
- **MS_INF_CKS_ERR_RAW** is 0. This condition applies only if **ALWAYS_STORE_INF** is set to 1.

MS_INFO_RAW, IO, Address 0x60[3] (Read Only)

Raw status signal of MPEG source InfoFrame detection signal.

Function

MS_INFO_RAW	Description
0 (default)	No source product description InfoFrame received within the last three VSyncs or since the last HDMI packet detection reset.
1	MPEG Source InfoFrame received. This bit resets to zero after an HDMI packet detection reset or upon writing to MS_PACKET_ID.

Vendor Specific InfoFrame Registers

Table 25 provides a list of readback registers available for the vendor specific InfoFrame.

Table 25. VS InfoFrame Registers

InfoFrame Map Address	R/W	Register Name	Byte Name
0xEC	R	**VS_PACKET_ID[7:0]**	Packet type value
0xED	R	VS_INF_VERS	InfoFrame version number
0xEE	R	VS_INF_LEN	InfoFrame length
0x54	R	VS_INF_PB_0_1	Checksum
0x55	R	VS_INF_PB_0_2	Data Byte 1
0x56	R	VS_INF_PB_0_3	Data Byte 2
0x57	R	VS_INF_PB_0_4	Data Byte 3
0x58	R	VS_INF_PB_0_5	Data Byte 4
0x59	R	VS_INF_PB_0_6	Data Byte 5
0x5A	R	VS_INF_PB_0_7	Data Byte 6
0x5B	R	VS_INF_PB_0_8	Data Byte 7
0x5C	R	VS_INF_PB_0_9	Data Byte 8
0x5D	R	VS_INF_PB_0_10	Data Byte 9
0x5E	R	VS_INF_PB_0_11	Data Byte 10
0x5F	R	VS_INF_PB_0_12	Data Byte 11
0x60	R	VS_INF_PB_0_13	Data Byte 12
0x61	R	VS_INF_PB_0_14	Data Byte 13
0x62	R	VS_INF_PB_0_15	Data Byte 14
0x63	R	VS_INF_PB_0_16	Data Byte 15
0x64	R	VS_INF_PB_0_17	Data Byte 16
0x65	R	VS_INF_PB_0_18	Data Byte 17
0x66	R	VS_INF_PB_0_19	Data Byte 18
0x67	R	VS_INF_PB_0_20	Data Byte 19
0x68	R	VS_INF_PB_0_21	Data Byte 20
0x69	R	VS_INF_PB_0_22	Data Byte 21
0x6A	R	VS_INF_PB_0_23	Data Byte 22
0x6B	R	VS_INF_PB_0_24	Data Byte 23
0x6C	R	VS_INF_PB_0_25	Data Byte 24
0x6D	R	VS_INF_PB_0_26	Data Byte 25
0x6E	R	VS_INF_PB_0_27	Data Byte 26
0x6F	R	VS_INF_PB_0_28	Data Byte 27

The vendor specific InfoFrame registers are considered valid if the following two conditions are met:

- **VS_INFO_RAW** is 1.
- **VS_INF_CKS_ERR_RAW** is 0. This condition applies only if **ALWAYS_STORE_INF** is set to 1.

VS_INFO_RAW, IO, Address 0x60[4] (Read Only)

Raw status signal of vendor specific InfoFrame detection signal.

Function

VS_INFO_RAW	Description
0 (default)	No new VS InfoFrame has been received since the last HDMI packet detection reset.
1	A new VS InfoFrame has been received. This bit resets to zero after an HDMI packet detection reset or upon writing to VS_PACKET_ID.

PACKET REGISTERS

ACP Packet Registers

Table 26 provides the list of readback registers available for the ACP packets. Refer to the HDMI 1.3 specifications for a detailed explanation of the ACP packet fields.

Table 26. ACP Packet Registers

InfoFrame Map Address	R/W	Register Name	Packet Byte No.[1]
0xEF	R/W	**ACP_PACKET_ID[7:0]**	Packet type value
0xF0	R	ACP_TYPE	HB1
0xF1	R	ACP_HEADER2	HB2
0x70	R	ACP_PB_0_1	PB0
0x71	R	ACP_PB_0_2	PB1
0x72	R	ACP_PB_0_3	PB2
0x73	R	ACP_PB_0_4	PB3
0x74	R	ACP_PB_0_5	PB4
0x75	R	ACP_PB_0_6	PB5
0x76	R	ACP_PB_0_7	PB6
0x77	R	ACP_PB_0_8	PB7
0x78	R	ACP_PB_0_9	PB8
0x79	R	ACP_PB_0_10	PB9
0x7A	R	ACP_PB_0_11	PB10
0x7B	R	ACP_PB_0_12	PB11
0x7C	R	ACP_PB_0_13	PB12
0x7D	R	ACP_PB_0_14	PB13
0x7E	R	ACP_PB_0_15	PB14
0x7F	R	ACP_PB_0_16	PB15
0x80	R	ACP_PB_0_17	PB16
0x81	R	ACP_PB_0_18	PB17
0x82	R	ACP_PB_0_19	PB18
0x83	R	ACP_PB_0_20	PB19
0x84	R	ACP_PB_0_21	PB20
0x85	R	ACP_PB_0_22	PB21
0x86	R	ACP_PB_0_23	PB22
0x87	R	ACP_PB_0_24	PB23
0x88	R	ACP_PB_0_25	PB24
0x89	R	ACP_PB_0_26	PB25
0x8A	R	ACP_PB_0_27	PB26
0x8B	R	ACP_PB_0_28	PB27

[1] As defined by the HDMI 1.3 specifications.

The ACP InfoFrame registers are considered valid if **ACP_PCKT_RAW** is set to 1.

ACP_PCKT_RAW, IO, Address 0x60[5] (Read Only)

Raw status signal of audio content protection packet detection signal.

Function

ACP_PCKT_RAW	Description
0 (default)	No ACP packet received within the last 600 ms or since the last HDMI packet detection reset.
1	ACP packets have been received within the last 600 ms. This bit resets to zero after an HDMI packet detection reset or upon writing to ACP_PACKET_ID.

ISRC Packet Registers

Table 27 and Table 28 provide lists of readback registers available for the ISRC packets. Refer to the HDMI 1.3 specifications for a detailed explanation of the ISRC packet fields.

Table 27. ISRC1 Packet Registers

InfoFrame Map Address	R/W	Register Name	Packet Byte No.[1]
0xF2	R/W	**ISRC1_PACKET_ID[7:0]**	Packet type value
0xF3	R	ISRC1_HEADER1	HB1
0xF4	R	ISRC1_HEADER2	HB2
0x8C	R	ISRC1_PB_0_1	PB0
0x8D	R	ISRC1_PB_0_2	PB1
0x8E	R	ISRC1_PB_0_3	PB2
0x8F	R	ISRC1_PB_0_4	PB3
0x90	R	ISRC1_PB_0_5	PB4
0x91	R	ISRC1_PB_0_6	PB5
0x92	R	ISRC1_PB_0_7	PB6
0x93	R	ISRC1_PB_0_8	PB7
0x94	R	ISRC1_PB_0_9	PB8
0x95	R	ISRC1_PB_0_10	PB9
0x96	R	ISRC1_PB_0_11	PB10
0x97	R	ISRC1_PB_0_12	PB11
0x98	R	ISRC1_PB_0_13	PB12
0x99	R	ISRC1_PB_0_14	PB13
0x9A	R	ISRC1_PB_0_15	PB14
0x9B	R	ISRC1_PB_0_16	PB15
0x9C	R	ISRC1_PB_0_17	PB16
0x9D	R	ISRC1_PB_0_18	PB17
0x9E	R	ISRC1_PB_0_19	PB18
0x9F	R	ISRC1_PB_0_20	PB19
0xA0	R	ISRC1_PB_0_21	PB20
0xA1	R	ISRC1_PB_0_22	PB21
0xA2	R	ISRC1_PB_0_23	PB22
0xA3	R	ISRC1_PB_0_24	PB23
0xA4	R	ISRC1_PB_0_25	PB24
0xA5	R	ISRC1_PB_0_26	PB25
0xA6	R	ISRC1_PB_0_27	PB26
0xA7	R	ISRC1_PB_0_28	PB27

[1] As defined by the HDMI specifications.

The ISRC1 packet registers are considered valid if **ISRC1_PCKT_RAW** is set to 1.

ISRC1_PCKT_RAW, IO, Address 0x60[6] (Read Only)

Raw status signal of International Standard Recording Code 1 (ISRC1) packet detection signal.

Function

ISRC1_PCKT_RAW	Description
0 (default)	No ISRC1 packets received since the last HDMI packet detection reset.
1	ISRC1 packets have been received. This bit resets to zero after an HDMI packet detection reset or upon writing to ISRC1_PACKET_ID.

Table 28. ISRC2 Packet Registers

InfoFrame Map Address	R/W	Register Name	Packet Byte No.[1]
0xF5	R/W	**ISRC2_PACKET_ID[7:0]**	Packet type value
0xF6	R	ISRC2_HEADER1	HB1
0xF7	R	ISRC2_HEADER2	HB2
0xA8	R	ISRC2_PB_0_1	PB0
0xA9	R	ISRC2_PB_0_2	PB1
0xAA	R	ISRC2_PB_0_3	PB2
0xAB	R	ISRC2_PB_0_4	PB3
0xAC	R	ISRC2_PB_0_5	PB4
0xAD	R	ISRC2_PB_0_6	PB5
0xAE	R	ISRC2_PB_0_7	PB6
0xAF	R	ISRC2_PB_0_8	PB7
0xB0	R	ISRC2_PB_0_9	PB8
0xB1	R	ISRC2_PB_0_10	PB9
0xB2	R	ISRC2_PB_0_11	PB10
0xB3	R	ISRC2_PB_0_12	PB11
0xB4	R	ISRC2_PB_0_13	PB12
0xB5	R	ISRC2_PB_0_14	PB13
0xB6	R	ISRC2_PB_0_15	PB14
0xB7	R	ISRC2_PB_0_16	PB15
0xB8	R	ISRC2_PB_0_17	PB16
0xB9	R	ISRC2_PB_0_18	PB17
0xBA	R	ISRC2_PB_0_19	PB18
0xBB	R	ISRC2_PB_0_20	PB19
0xBC	R	ISRC2_PB_0_21	PB20
0xBD	R	ISRC2_PB_0_22	PB21
0xBE	R	ISRC2_PB_0_23	PB22
0xBF	R	ISRC2_PB_0_24	PB23
0xC0	R	ISRC2_PB_0_25	PB24
0xC1	R	ISRC2_PB_0_26	PB25
0xC2	R	ISRC2_PB_0_27	PB26
0xC3	R	ISRC2_PB_0_28	PB27

[1] As defined by the HDMI 1.3 specifications.

The ISRC2 packet registers are considered valid if, and only, if ISRC1_PCKT_RAW is set to 1.

ISRC2_PCKT_RAW, IO, Address 0x60[7] (Read Only)

Raw status signal of International Standard Recording Code 2 (ISRC2) packet detection signal.

Function

ISRC2_PCKT_RAW	Description
0 (default)	No ISRC2 packets received since the last HDMI packet detection reset.
1	ISRC2 packets have been received. This bit resets to zero after an HDMI packet detection reset or upon writing to ISRC2_PACKET_ID.

Gamut Metadata Packets

Refer to the HDMI specifications for a detailed explanation of the gamut metadata packet fields.

Table 29. Gamut Metadata Packet Registers

HDMI Map Address	R/W	Register Name	Packet Byte No.[1]
0xF8	R/W	**GAMUT_PACKET_ID[7:0]**	Packet type value
0xF9	R	GAMUT_HEADER1	HB1
0xFA	R	GAMUT_HEADER2	HB2
0xC4	R	GAMUT_MDATA_PB_0_1	PB0
0xC5	R	GAMUT_MDATA_PB_0_2	PB1
0xC6	R	GAMUT_MDATA_PB_0_3	PB2
0xC7	R	GAMUT_MDATA_PB_0_4	PB3
0xC8	R	GAMUT_MDATA_PB_0_5	PB4
0xC9	R	GAMUT_MDATA_PB_0_6	PB5
0xCA	R	GAMUT_MDATA_PB_0_7	PB6
0xCB	R	GAMUT_MDATA_PB_0_8	PB7
0xCC	R	GAMUT_MDATA_PB_0_9	PB8
0xCD	R	GAMUT_MDATA_PB_0_10	PB9
0xCE	R	GAMUT_MDATA_PB_0_11	PB10
0xCF	R	GAMUT_MDATA_PB_0_12	PB11
0xD0	R	GAMUT_MDATA_PB_0_13	PB12
0xD1	R	GAMUT_MDATA_PB_0_14	PB13
0xD2	R	GAMUT_MDATA_PB_0_15	PB14
0xD3	R	GAMUT_MDATA_PB_0_16	PB15
0xD4	R	GAMUT_MDATA_PB_0_17	PB16
0xD5	R	GAMUT_MDATA_PB_0_18	PB17
0xD6	R	GAMUT_MDATA_PB_0_19	PB18
0xD7	R	GAMUT_MDATA_PB_0_20	PB19
0xD8	R	GAMUT_MDATA_PB_0_21	PB20
0xD9	R	GAMUT_MDATA_PB_0_22	PB21
0xDA	R	GAMUT_MDATA_PB_0_23	PB22
0xDB	R	GAMUT_MDATA_PB_0_24	PB23
0xDC	R	GAMUT_MDATA_PB_0_25	PB24
0xDD	R	GAMUT_MDATA_PB_0_26	PB25
0xDE	R	GAMUT_MDATA_PB_0_27	PB26
0xDF	R	GAMUT_MDATA_PB_0_28	PB27

[1] As defined by the HDMI specifications.

The gamut metadata packet registers are considered valid if **GAMUT_MDATA_RAW** is set to 1.

GAMUT_MDATA_RAW, IO, Address 0x65[0] (Read Only)

Raw status signal of gamut metadata packet detection signal.

Function

GAMUT_MDATA_RAW	Description
0 (default)	No gamut metadata packet has been received in the last video frame or since the last HDMI packet detection reset.
1	A gamut metadata packet has been received in the last video frame. This bit resets to zero after an HDMI packet detection reset or upon writing to GAMUT_PACKET_ID.

GAMUT_IRQ_NEXT_FIELD, Addr 68 (HDMI), Address 0x50[4]

A control set the NEW_GAMUT_MDATA_RAW interrupt to detect when the new contents are applicable to next field or to indicate that the gamut packet is new. This is done using header information of the gamut packet.

Function

GAMUT_IRQ_NEXT_FIELD	Description
0 (default)	Interrupt flag indicates that gamut packet is new.
1	Interrupt flag indicates that gamut packet is to be applied next field.

CUSTOMIZING PACKET/INFOFRAME STORAGE REGISTERS

The packet type value of each set of packet and InfoFrame registers in the InfoFrame map is programmable. This allows the user to configure the ADV7619 to store the payload data of any packet and InfoFrames sent by the transmitter connected on the selected HDMI port.

Note that writing to any of the nine following packet ID registers also clears the corresponding raw InfoFrame /packet detection bit. For example, writing 0x82, or any other value, to AVI_PACKET_ID clears **AVI_INFO_RAW**.

AVI_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xE0[7:0]

AVI InfoFrame ID.

Function

AVI_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x00 to 0x1B
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x00 to 0x1B

AUD_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xE3[7:0]

Audio InfoFrame ID.

Function

AUD_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x1C to 0x29
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x1C to 0x29

SPD_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xE6[7:0]

Source Prod InfoFrame ID.

Function

SPD_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x2A to 0x45
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x2A to 0x45

MS_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xE9[7:0]

MPEG source InfoFrame ID.

Function

MS_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x46 to 0x53
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x46 to 0x53

VS_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xEC[7:0]

Vendor specific InfoFrame ID.

Function

VS_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x54 to 0x6F
1xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x54 to 0x6F

ACP_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xEF[7:0]

ACP InfoFrame ID.

Function

ACP_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x70 to 0x8B
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x70 to 0x8B

ISRC1_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xF2[7:0]

ISRC1 InfoFrame ID.

Function

ISRC1_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x8C to 0xA7
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x8C to 0xA7

ISRC2_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xF5[7:0]

ISRC2 InfoFrame ID.

Function

ISRC2_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0xA8 to 0xC3
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0xA8 to 0xC3

GAMUT_PACKET_ID[7:0], Addr 7C (InfoFrame), Address 0xF8[7:0]

Gamut InfoFrame ID.

Function

GAMUT_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0xC4 to 0xDF
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0xC4 to 0xDF

Note: The packet type values and corresponding packets should not be programmed in the packet type values registers. These packets are always processed internally and cannot be stored in the packet/InfoFrame registers in the InfoFrame map:

- 0x01: audio clock regeneration packet
- 0x02: audio sample packet
- 0x03: general control packet
- 0x07: DSD audio sample packet
- 0x08: DST audio packet
- 0x09: HBR audio stream packet

REPEATER SUPPORT

The ADV7619 incorporates an EDID/repeater controller that provides all the features required for a receiver front end of a fully HDCP 1.4 compliant repeater system. The ADV7619 has a RAM that can store up to 127 KSVs, which allows it to handle up to 127 downstream devices in repeater mode (refer to Table 30).

The ADV7619 features a set of HDCP registers, defined in the HDCP specifications, which are accessible through the DDC bus (refer to the DDC Ports section) of the selected port. A subset of the HDCP registers (defined in the following subsections) are also available in the Repeater map and are accessible through the main I^2C port (refer to the Main I^2C Port section).

Repeater Routines Performed by the EDID/Repeater Controller

Power Up

A power-on reset circuitry on the DVDD supply is used to reset the EDID/repeater controller when the ADV7619 is powered up. When the EDID/repeater controller reboots after reset, it resets all the KSV registers listed in Table 30 to 0x00.

AKSV Update

The EDID/repeater controller resets automatically the BCAPS [5] bit to 0 when an HDCP transmitter writes its AKSV into the ADV7619 HDCP registers through the DDC bus of the HDMI port.

Note: Writing a value in the AKSV[39:32] triggers an AKSV update and AKSV_UPDATE_ST interrupt if AKSV_UPDATE_MB1 or AKSV_UPDATE_MB2 has been set to 1 This triggers the EDID/repeater controller to reset the BCAPS [5] bit back to 0.

KSV List Ready

The **KSV_LIST_READY** bit is set by an external controller driving the ADV7619. This notifies the ADV7619 on-chip EDID/repeater controller that the KSV list registers have been updated with the KSV's of the attached and active downstream HDCP devices.

When KSV_LIST_READY is set to 1, the EDID/repeater controller computes the SHA-1 hash value V', updates the corresponding V' registers (refer to Table 31), and sets the READY bit (that is, BCAPS[5]) to 1. This indicates to the transmitter attached to the ADV7619 that the KSV FIFO and SHA-1 hash value V' are ready to be read.

KSV_LIST_READY, Addr 64 (Repeater), Address 0x71[7]

The system sets this bit in order to indicate that the KSV list has been read from the Tx IC(s) and written into the repeater map. The system must also set Bits[11:0] of BSTATUS before setting this bit.

Function

KSV_LIST_READY	Description
0 (default)	Not ready
1	Ready

Notes

- The SHA-1 hash value will be computed if the bit KSV_LIST_READY is set after the part has received an AKSV update from the upstream source. The external controller should therefore set KSV_LST_READY to 1 only after the part has received an AKSV update from the upstream source.
- The ADV7619 does not automatically clear KSV_LIST_READY to 0, after it has finished computed the SHA-1 has value. Therefore, the external controller needs to clear KSV_LIST_READY.

HDMI Mode

The BSTATUS[12]bit is updated automatically by the ADV7619 and follows the HDMI mode status of the HDMI/DVI stream input on the active HDMI port. BSTATUS [12] is set to 1 if the ADV7619 receives an HDMI stream, and set to 0 if the ADV7619 receives a DVI stream.

Repeater Actions Required by External Controller

The external controller must set the BCAPS register and notify the ADV7619 when the KSV list is updated, as described in the following sections: Repeater Bit, KSV FIFO Read from HDCP Registers, First AKSV Update, and AKSV_UPDATE_B_RAW.

Note that many more routines must be implemented into the external controller driving the ADV7619 to implement a full repeater. Such routines are described in the HDCP and HDMI specifications (for example, copying InfoFrame and packet data image from the HDMI receiver into the HDMI transmitter, momentarily deasserting the hot plug detect and disabling the clock termination on a change of downstream topology, and so on).

Repeater Bit

The REPEATER bit (that is, BCAPS[6]) must be set to 1 by the external controller in the routine that initializes the ADV7619. The repeater bit must be left as such as long as the ADV7619 is configured as the front end of a repeater system.

Note: The registers in the KSV list (refer to Table 30) should always be set to 0x0 if the REPEATER bit is set to 0. The firmware running on the external controller, therefore, always sets the registers in the KSV list to 0x0 if the repeater bit is changed from 1 to 0.

KSV FIFO Read from HDCP Registers

The KSV FIFO read at address 0x43 through the HDCP port of the selected HDMI port is dependent on the value of the REPEATER bit (that is, BCAPS[6]):

- When the REPEATER bit is set to 0, the KSV FIFO read from the HDCP port always returns 0x0
- When the REPEATER bit is set to 1, the KSV FIFO read from the HDCP port matches the KSV list which is set in the Repeater map at addresses 0x80 to 0xF7 (refer to Table 30)

First AKSV Update

When the upstream transmitter writes its AKSV for the first time into the ADV7619 HDCP registers, the external controller driving the ADV7619 should perform the following tasks:

- Update BSTATUS[11:0] according to the topology of the downstream device attached to the repeater.
- Update the KSV list (refer to Table 30) with the KSV from the transmitter on the back end of the repeater as well as the KSV from all the downstream devices connected to the repeater.
- Set **KSV_LIST_READY** to 1.
- The external controller can monitor the AKSV_UPDATE_X_RAW bits to be notified when the transmitter writes its AKSV into the HDCP registers of the ADV7619 (where X = A and B).

AKSV_UPDATE_A_RAW, IO, Address 0x88[0] (Read Only)

Status of Port A AKSV update interrupt signal. When set to 1 it indicates that transmitter has written its AKSV into HDCP registers for Port A. Once set, this bit will remain high until it is cleared via AKSV_UPDATE_A_CLR.

Function

AKSV_UPDATE_A_RAW	Description
0 (default)	No AKSV updates on Port A
1	Detected a write access to the AKSV register on Port A

AKSV_UPDATE_B_RAW, IO, Address 0x88[1] (Read Only)

Status of Port B AKSV Update Interrupt signal. When set to 1, it indicates that transmitter has written its AKSV into HDCP registers for Port B. Once set, this bit remains high until it is cleared via AKSV_UPDATE_B_CLR.

Function

AKSV_UPDATE_B_RAW	Description
0 «	No AKSV updates on Port B
1	Detected a write access to the AKSV register on Port B

Second and Subsequent AKSV Updates

When the upstream transmitter writes its AKSV for the second time or more into the ADV7619 HDCP registers, the external controller driving the ADV7619 should set **KSV_LIST_READY** to 1.

HDCP Registers Available in Repeater Map

In order to enable fast switching of the HDCP encrypted HDMI ports, the registers 0x00 to 0x42 in the repeater map are replicated for each port. **AUTO_HDCP_MAP_ENABLE** and **HDCP_MAP_SELECT[2:0]** determine which port is currently visible to the user.

AUTO_HDCP_MAP_ENABLE, Addr 64 (Repeater), Address 0x79[3]

Selects which port will be accessed for HDCP addresses: the HDMI active port (selected by HDMI_PORT_SELECT, HDMI map) or the one selected in HDCP_MAP_SELECT.

Function

AUTO_HDCP_MAP_ENABLE	Description
0	HDCP data read from port given by HDCP_MAP_SELECT
1 (default)	HDCP data read from the active HDMI port

HDCP_MAP_SELECT[2:0], Addr 64 (Repeater), Address 0x79[2:0]

Selects which port will be accessed for HDCP addresses (0x00 to 0x42 in Repeater map). This only takes effect when AUTO HDCP MAN ENABLE is 0.

Function

HDCP_MAP_SELECT[2:0]	Description
000 (default)	Select Port A
001	Select Port B

BKSV[39:0], Addr 64 (Repeater), Address 0x04[7:0]; Address 0x03[7:0]; Address 0x02[7:0]; Address 0x01[7:0]; Address 0x00[7:0] (Read Only)

The receiver key selection vector (BKSV) can be read back once the part has successfully accessed the HDCP ROM. The following registers contain the BKSV read from the EEPROM.

Function

BKSV[39:0]	Description
0x00[7:0]	BKSV[7:0]
0x01[7:0]	BKSV[15:8]
0x02[7:0]	BKSV[23:16]
0x03[7:0]	BKSV[31:24]
0x04[7:0]	BKSV[39:32]

AKSV[39:0], Addr 64 (Repeater), Address 0x14[7:0]; Address 0x13[7:0]; Address 0x12[7:0]; Address 0x11[7:0]; Address 0x10[7:0]

The AKSV of the transmitter attached to the active HDMI port can be read back after an AKSV update. The following registers contain the AKSV written by the Tx.

Function

AKSV[39:0]	Description
0x10[7:0]	AKSV[7:0]
0x11[7:0]	AKSV[15:8]
0x12[7:0]	AKSV[23:16]
0x13[7:0]	AKSV[31:24]
0x14[7:0]	AKSV[39:32]

BCAPS[7:0], Addr 64 (Repeater), Address 0x40[7:0]

This is the BCAPS register presented to the Tx attached to the active HDMI port.

Function

BCAPS[7:0]	Description
10000011 (default)	Default BCAPS register value presented to the Tx
xxxxxxxx	BCAPS register value presented to the Tx

BSTATUS[15:0], Addr 64 (Repeater), Address 0x42[7:0]; Address 0x41[7:0]

These registers contain the BSTATUS information presented to the Tx attached to the active HDMI port. Bits [11:0] must be set by the system software acting as a repeater.

Function

BSTATUS[15:0]	Description
xxxxxxxxxxxxxxxx	BSTATUS register presented to Tx.
0000000000000000 (default)	Reset value. BSTATUS register is reset only after power up.
0x41[7:0]	BSTATUS[7:0].
0x42[7:0]	BSTATUS[15:8].

KSV registers are stored consecutively in RAM, which is split into 5x128 bytes bank maps. Maps are accessible through KSV_BYTE_0 to KSV_BYTE_127. Proper segment can be selected via **KSV_MAP_SELECT[2:0]** register, as shown in Figure 28.

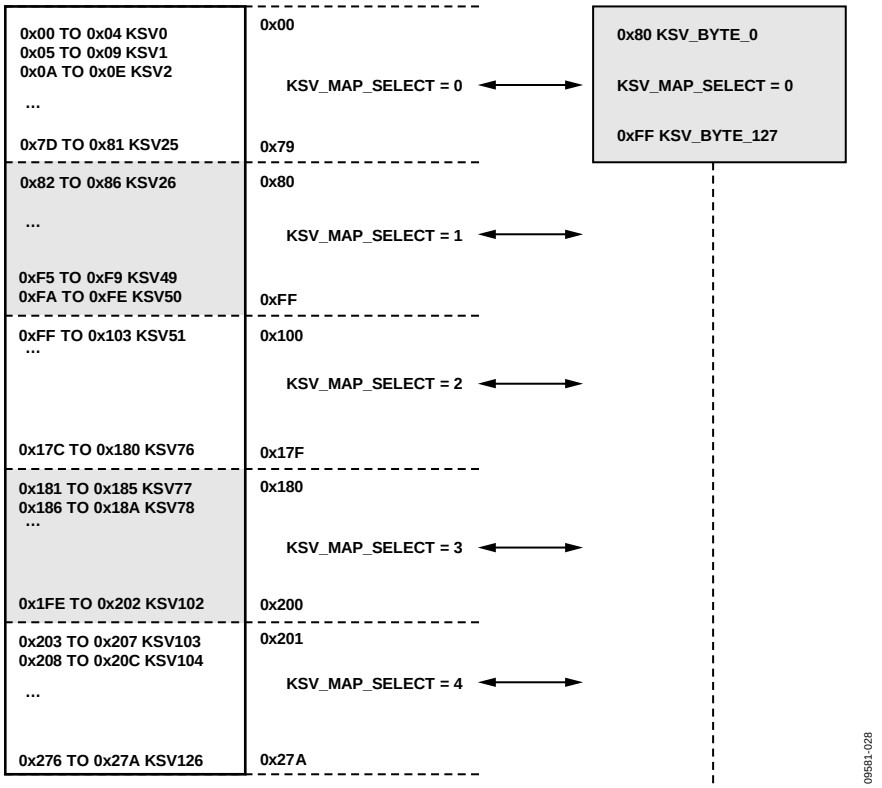


Figure 28. Addressing Block Using KSV_MAP_SELECT and Register KSV_BYTE_0 to Register KSV_BYTE_127

KSV_MAP_SELECT[2:0], Addr 64 (Repeater), Address 0x79[6:4]

Selects which 128 bytes of KSV list will be accessed when reading or writing to addresses 0x80 to 0xFF in this map. Values from 5 and upwards are not valid

Function

KSV_MAP_SELECT[2:0]	Description
000 (default)	KSV Map 0 selected
001	KSV Map 1 selected
010	KSV Map 2 selected
011	KSV Map 3 selected
100	KSV Map 4 selected
101	Reserved
110	Reserved
111	Reserved

Table 30. KSV Byte Registers Location

KSV Byte Number	Register Name	Register Addresses[1]
0	KSV_BYTE_0[7:0]	0x80[7:0]
1	KSV_BYTE_1[7:0]	0x81[7:0]
2	KSV_BYTE_2[7:0]	0x82[7:0]
3	KSV_BYTE_3[7:0]	0x83[7:0]
4	KSV_BYTE_4[7:0]	0x84[7:0]
5	KSV_BYTE_5[7:0]	0x85[7:0]
6	KSV_BYTE_6[7:0]	0x86[7:0]
7	KSV_BYTE_7[7:0]	0x87[7:0]
8	KSV_BYTE_8[7:0]	0x88[7:0]
9	KSV_BYTE_9[7:0]	0x89[7:0]
10	KSV_BYTE_10[7:0]	0x8A[7:0]
11	KSV_BYTE_11[7:0]	0x8B[7:0]
12	KSV_BYTE_12[7:0]	0x8C[7:0]
13	KSV_BYTE_13[7:0]	0x8D[7:0]
14	KSV_BYTE_14[7:0]	0x8E[7:0]
15	KSV_BYTE_15[7:0]	0x8F[7:0]
16	KSV_BYTE_16[7:0]	0x90[7:0]
17	KSV_BYTE_17[7:0]	0x91[7:0]
18	KSV_BYTE_18[7:0]	0x92[7:0]
19	KSV_BYTE_19[7:0]	0x93[7:0]
20	KSV_BYTE_20[7:0]	0x94[7:0]
21	KSV_BYTE_21[7:0]	0x95[7:0]
22	KSV_BYTE_22[7:0]	0x96[7:0]
23	KSV_BYTE_23[7:0]	0x97[7:0]
24	KSV_BYTE_24[7:0]	0x98[7:0]
25	KSV_BYTE_25[7:0]	0x99[7:0]
26	KSV_BYTE_26[7:0]	0x9A[7:0]
27	KSV_BYTE_27[7:0]	0x9B[7:0]
28	KSV_BYTE_28[7:0]	0x9C[7:0]
29	KSV_BYTE_29[7:0]	0x9D[7:0]
30	KSV_BYTE_30[7:0]	0x9E[7:0]
31	KSV_BYTE_31[7:0]	0x9F[7:0]
32	KSV_BYTE_32[7:0]	0xA0[7:0]
33	KSV_BYTE_33[7:0]	0xA1[7:0]
34	KSV_BYTE_34[7:0]	0xA2[7:0]
35	KSV_BYTE_35[7:0]	0xA3[7:0]
36	KSV_BYTE_36[7:0]	0xA4[7:0]
37	KSV_BYTE_37[7:0]	0xA5[7:0]

KSV Byte Number	Register Name	Register Addresses[1]
38	KSV_BYTE_38[7:0]	0xA6[7:0]
39	KSV_BYTE_39[7:0]	0xA7[7:0]
40	KSV_BYTE_40[7:0]	0xA8[7:0]
41	KSV_BYTE_41[7:0]	0xA9[7:0]
42	KSV_BYTE_42[7:0]	0xAA[7:0]
43	KSV_BYTE_43[7:0]	0xAB[7:0]
44	KSV_BYTE_44[7:0]	0xAC[7:0]
45	KSV_BYTE_45[7:0]	0xAD[7:0]
46	KSV_BYTE_46[7:0]	0xAE[7:0]
47	KSV_BYTE_47[7:0]	0xAF[7:0]
48	KSV_BYTE_48[7:0]	0xB0[7:0]
49	KSV_BYTE_49[7:0]	0xB1[7:0]
50	KSV_BYTE_50[7:0]	0xB2[7:0]
51	KSV_BYTE_51[7:0]	0xB3[7:0]
52	KSV_BYTE_52[7:0]	0xB4[7:0]
53	KSV_BYTE_53[7:0]	0xB5[7:0]
54	KSV_BYTE_54[7:0]	0xB6[7:0]
55	KSV_BYTE_55[7:0]	0xB7[7:0]
56	KSV_BYTE_56[7:0]	0xB8[7:0]
57	KSV_BYTE_57[7:0]	0xB9[7:0]
58	KSV_BYTE_58[7:0]	0xBA[7:0]
59	KSV_BYTE_59[7:0]	0xBB[7:0]
60	KSV_BYTE_60[7:0]	0xBC[7:0]
61	KSV_BYTE_61[7:0]	0xBD[7:0]
62	KSV_BYTE_62[7:0]	0xBE[7:0]
63	KSV_BYTE_63[7:0]	0xBF[7:0]
64	KSV_BYTE_64[7:0]	0xC0[7:0]
65	KSV_BYTE_65[7:0]	0xC1[7:0]
66	KSV_BYTE_66[7:0]	0xC2[7:0]
67	KSV_BYTE_67[7:0]	0xC3[7:0]
68	KSV_BYTE_68[7:0]	0xC4[7:0]
69	KSV_BYTE_69[7:0]	0xC5[7:0]
70	KSV_BYTE_70[7:0]	0xC6[7:0]
71	KSV_BYTE_71[7:0]	0xC7[7:0]
72	KSV_BYTE_72[7:0]	0xC8[7:0]
73	KSV_BYTE_73[7:0]	0xC9[7:0]
74	KSV_BYTE_74[7:0]	0xCA[7:0]
75	KSV_BYTE_75[7:0]	0xCB[7:0]
76	KSV_BYTE_76[7:0]	0xCC[7:0]
77	KSV_BYTE_77[7:0]	0xCD[7:0]
78	KSV_BYTE_78[7:0]	0xCE[7:0]
79	KSV_BYTE_79[7:0]	0xCF[7:0]
80	KSV_BYTE_80[7:0]	0xD0[7:0]
81	KSV_BYTE_81[7:0]	0xD1[7:0]
82	KSV_BYTE_82[7:0]	0xD2[7:0]
83	KSV_BYTE_83[7:0]	0xD3[7:0]
84	KSV_BYTE_84[7:0]	0xD4[7:0]
85	KSV_BYTE_85[7:0]	0xD5[7:0]
86	KSV_BYTE_86[7:0]	0xD6[7:0]
87	KSV_BYTE_87[7:0]	0xD7[7:0]
88	KSV_BYTE_88[7:0]	0xD8[7:0]
89	KSV_BYTE_89[7:0]	0xD9[7:0]
90	KSV_BYTE_90[7:0]	0xDA[7:0]

KSV Byte Number	Register Name	Register Addresses[1]
91	KSV_BYTE_91[7:0]	0xDB[7:0]
92	KSV_BYTE_92[7:0]	0xDC[7:0]
93	KSV_BYTE_93[7:0]	0xDD[7:0]
94	KSV_BYTE_94[7:0]	0xDE[7:0]
95	KSV_BYTE_95[7:0]	0xDF[7:0]
96	KSV_BYTE_96[7:0]	0xE0[7:0]
97	KSV_BYTE_97[7:0]	0xE1[7:0]
98	KSV_BYTE_98[7:0]	0xE2[7:0]
99	KSV_BYTE_99[7:0]	0xE3[7:0]
100	KSV_BYTE_100[7:0]	0xE4[7:0]
101	KSV_BYTE_101[7:0]	0xE5[7:0]
102	KSV_BYTE_102[7:0]	0xE6[7:0]
103	KSV_BYTE_103[7:0]	0xE7[7:0]
104	KSV_BYTE_104[7:0]	0xE8[7:0]
105	KSV_BYTE_105[7:0]	0xE9[7:0]
106	KSV_BYTE_106[7:0]	0xEA[7:0]
107	KSV_BYTE_107[7:0]	0xEB[7:0]
108	KSV_BYTE_108[7:0]	0xEC[7:0]
109	KSV_BYTE_109[7:0]	0xED[7:0]
110	KSV_BYTE_110[7:0]	0xEE[7:0]
111	KSV_BYTE_111[7:0]	0xEF[7:0]
112	KSV_BYTE_112[7:0]	0xF0[7:0]
113	KSV_BYTE_113[7:0]	0xF1[7:0]
114	KSV_BYTE_114[7:0]	0xF2[7:0]
115	KSV_BYTE_115[7:0]	0xF3[7:0]
116	KSV_BYTE_116[7:0]	0xF4[7:0]
117	KSV_BYTE_117[7:0]	0xF5[7:0]
118	KSV_BYTE_118[7:0]	0xF6[7:0]
119	KSV_BYTE_119[7:0]	0xF7[7:0]
120	KSV_BYTE_120[7:0]	0xF8[7:0]
121	KSV_BYTE_121[7:0]	0xF9[7:0]
122	KSV_BYTE_122[7:0]	0xFA[7:0]
123	KSV_BYTE_123[7:0]	0xFB[7:0]
124	KSV_BYTE_124[7:0]	0xFC[7:0]
125	KSV_BYTE_125[7:0]	0xFD[7:0]
126	KSV_BYTE_126[7:0]	0xFE[7:0]
127	KSV_BYTE_127[7:0]	0xFF[7:0]

[1] All KSVs are located in the repeater map.

Table 31. Registers Location for SHA-1 Hash Value V'

Register Name	Address Location[1]	Function
SHA_A[31:0]	0x20[7:0]: SHA_A[7:0] 0x21[7:0]: SHA_A[15:8] 0x22[7:0]: SHA_A[23:16] 0x23[7:0]: SHA_A[31:24]	H0 part of SHA-1 hash value V'. Register also called (V'.H1)[2]
SHA_B[31:0]	0x24[7:0]: SHA_B[7:0] 0x25[7:0]: SHA_B[15:8] 0x26[7:0]: SHA_B[23:16] 0x27[7:0]: SHA_B[31:24]	H1 part of SHA-1 hash value V'. Register also called (V'.H1)[2]
SHA_C[31:0]	0x28[7:0]: SHA_C[7:0] 0x29[7:0]: SHA_C[15:8] 0x2A[7:0]: SHA_C[23:16] 0x2B[7:0]: SHA_C[31:24]	H2 part of SHA-1 hash value V'. Register also called (V'.H2)[2]

Register Name	Address Location[1]	Function
SHA_D[31:0]	0x2C[7:0]: SHA_D[7:0] 0x2D[7:0]: SHA_D[15:8] 0x2E[7:0]: SHA_D[23:16] 0x2F[7:0]: SHA_D[31:24]	H3 part of SHA-1 hash value V′. Register also called (V′.H3)[2]
SHA_E[31:0]	0x30[7:0]: SHA_E[7:0] 0x31[7:0]: SHA_E[15:8] 0x32[7:0]: SHA_E[23:16] 0x33[7:0]: SHA_E[31:24]	H4 part of SHA-1 hash value V′. Register also called (V′.H4)[2]

[1] All registers specified in Table 31 are located in the repeater map.
[2] Refer to HDCP protection system Standards.

INTERFACE TO DPP SECTION

The video databelow 2.25Gbps from the HDMI section is sent to the CP section via the DPP block. The video data output by the HDMI section is always in a 4:4:4 format with 36 bits per pixel. This is irrespective of the encoding format of the video data encapsulated in the HDMI/DVI stream input to the HDMI receiver section (that is, 4:2:2 or 4:4:4).

- If the HDMI section receives a stream with video encoded in a 4:4:4 format, it passes the video data to the DPP section.
- If the HDMI section receives a stream with video encoded in a 4:2:2 format (refer to Figure 29), the HDMI section upconverts the video data into a 4:4:4 format, according to the **UP_CONVERSION_MODE** bit, and passes the upconverted video data to the DPP section (refer to Figure 30).
- If the HDMI receiver receives video data with fewer than 12 bits used per channel, the valid bits are left-shifted on each component channel with zeroes padding the bit below the LSB, before being sent to the DPP section.
- If the HDMI receiver receives video data above 2.25 GBps, data must be send directly to the video ouput formatter, bypassing the DPP and CP core, where it is output using two video buses running at half pixel clock frequency

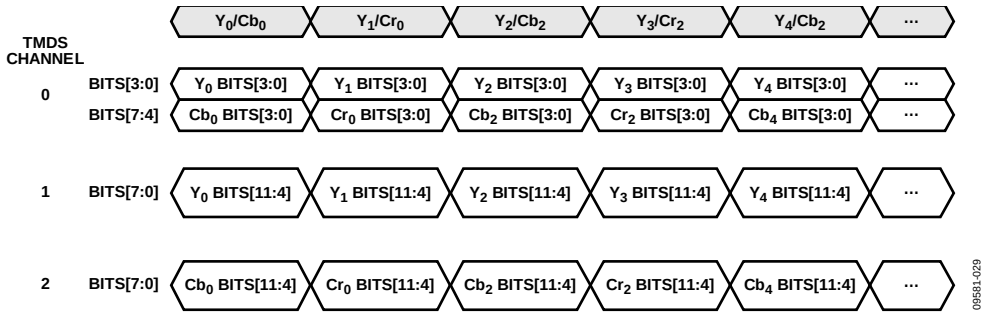


Figure 29. YC_bC_r 4:2:2 Video Data Encapsulated in HDMI Stream

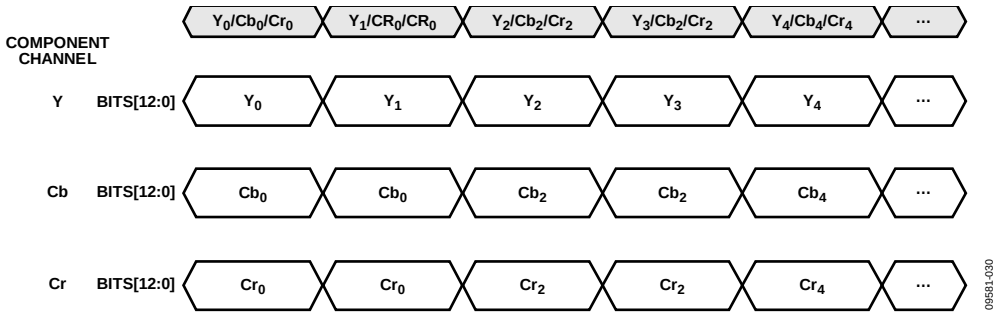


Figure 30. Video Stream Output by HDMI Core for YC_bC_r 4:2:2 Input and UP_CONVERSION = 0

UP_CONVERSION_MODE, Addr 68 (HDMI), Address 0x1D[5]

A control to select linear or interpolated 4:2:2 to 4:4:4 conversion. A 4:2:2 incoming stream is upconverted to a 4:4:4 stream before being sent to the CP.

Function

UP_CONVERSION_MODE	Description
0 (default)	Cr and Cb samples are repeated in their respective channel
1	Interpolate Cr and Cb values

Notes

When the ADV7619 pixel output format is set to 4:2:2 (refer to the Pixel Port Output Modes section), the DPP section down converts the 4:4:4 stream from the HDMI section according to **DS_WITHOUT_FILTER**.

- For a 4:4:4 HDMI input stream to the ADV7619
  - The DPP section filters and downsamples the video data from 4:4:4 to 4:2:2 format if **DS_WITHOUT_FILTER** is set to 0. The DPP section only downsamples, without filtering, the video data from the HDMI section if **DS_WITHOUT_FILTER** is set to 1.
- For a 4:2:2 HDMI input stream, the functionality of DS_WITHOUT_FILTER is reversed.
  - This inversion ensures that for a 4:2:2 HDMI input stream no filtering will be applied if DS_WITHOUT_FILTER is left to its default value 0. When a 4:2:2 HDMI input stream is input to the ADV7619, the DPP section downsamples, without filtering, the video data from 4:4:4 to 4:2:2 format if DS_WITHOUT_FILTER is set to 0. If DS_WITHOUT_FILTER is set to 1, the DPP filters and downsamples the video data from 4:4:4 to 4:2:2 format.

DS_WITHOUT_FILTER, Addr 40 (IO), Address 0xE0[7]

Disables the chroma filters on Channel B and Channel C while keeping the downsampler functional.

Function

DS_WITHOUT_FILTER	Description
0 (default)	Filters and downsamples
1	Downsamples only (no filtering)

PASS THROUGH MODE

The ADV7619 can process streams up to 3 Gbps only in the case where the CP core is fully bypassed. This is the mandatory mode for frequencies above 2.25 Gbps and must be set by setting **CP_COMPLETE_BYPASS_IN_HDMI_MODE**.

ADV7619 offers also pass through modes for frequencies below 2.25GBps. It can pass through the video data of an HDMI stream with no formatting. The video is passed from the HDMI section through the DPP and CP cores, out through the pixel output formatter without filtering or alteration. This can be achieved with the following settings:

4:2:2 Pass Through

- Set **DPP_BYPASS_EN** to 1 to use the CP CSC
- Set **UP_CONVERSION_MODE** to 0
- Set **DS_WITHOUT_FILTER** to 0
- Configure the pixel output formatter to output a 4:2:2 stream (refer to the Pixel Port Output Modes section)

4:4:4 Pass Through

- Set UP_CONVERSION_MODE to 0 or to 1
- Set DS_WITHOUT_FILTER to 0 or to 1
- Configure the pixel output formatter to output a 4:4:4 stream (refer to the Pixel Port Output Modes section)

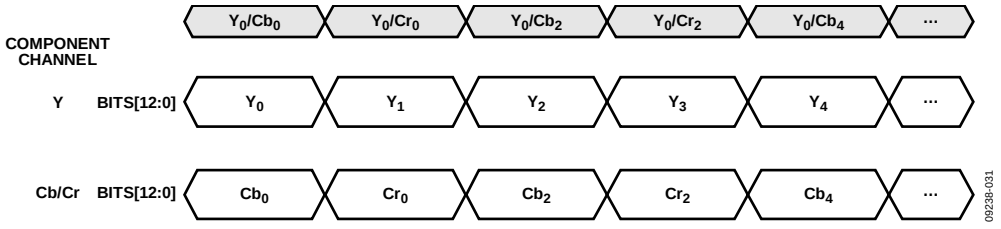


Figure 31. Video Data Output by DPP in 4:2:2 Pass Through Mode

DPP_BYPASS_EN, Addr 44 (CP), Address 0xBD[4]

Manual control to enable DPP block.

Function

DPP_BYPASS_EN	Description
1 (default)	DPP bypassed
0	DPP enabled

COLOR SPACE INFORMATION SENT TO THE DPP AND CP SECTIONS

The HDMI section sends information regarding the color space of the video it outputs to the DPP and the CP sections. This color space information is derived from the DVI/HDMI status of the input stream the HDMI stection processes and from the AVI InfoFrame that the HDMI section decodes from the input stream.

The color space information sent by the HDMI section to the DDP and CP sections can be read via the **HDMI_COLORSPACE[3:0]**.

HDMI_COLORSPACE[3:0], Addr 68 (HDMI), Address 0x53[3:0] (Read Only)

A readback of the HDMI input color space decoded from several fields in the AVI InfoFrame.

Function

HDMI_COLORSPACE[3:0]	Description
0000 (default)	RGB_LIMITED
0001	RGB_FULL
0010	YUV_601
0011	YUV_709
0100	XVYCC_601
0101	XVYCC_709
0110	YUV_601_FULL
0111	YUV_709_FULL
1000	sYCC 601
1001	Adobe YCC 601
1010	Adobe RGB

STATUS REGISTERS

Many status bit are available throughout the IO and HDMI maps. These status bits are listed in Table 32 to Table 41.

Table 32. HDMI Flags in IO Map Register 0x60

Bit Name	Bit Position	Description
AVI_INFO_RAW	0 (LSB)	Returns 1 if an AVI InfoFrame was received within last seven VSync. For additional information, see the Interrupt Architecture Overview section.
AUDIO_INFO_RAW	1	Returns 1 if an AVI InfoFrame was received within last three VSyncs. For additional information, see the Audio InfoFrame Registers section.
SPD_INFO_RAW	2	Returns 1 if a Source Product Descriptor InfoFrame has been received. For additional information, see the SPD InfoFrame Registers section.
MS_INFO_RAW	3	Returns 1 if a MPEG InfoFrame was received within the last three VSyncs. For additional information, see the MPEG Source InfoFrame Registers section.
VS_INFO_RAW	4	Returns 1 if a Vendor Specific InfoFrame has been received. For additional information, see the Vendor Specific InfoFrame Registers section.
ACP_PCKT_RAW	5	Returns 1 if an ACP packet was received within last 600 ms. For additional information, see the ACP Packet Registers section.
ISRC1_PCKT_RAW	6	Returns 1 if an ISRC1 packet was received. For additional information, see the ISRC Packet Registers section.
ISRC2_PCKT_RAW	7 (MSB)	Returns 1 if an ISRC2 packet was received. For additional information, see the ISRC Packet Registers section.

Table 33. HDMI Flags in IO Map Register 0x65

Bit Name	Bit Position	Description
GAMUT_MDATA_RAW	0 (LSB)	Returns 1 if a Gamut Metadata packet was received. For additional information, see the Gamut Metadata Packets section.
AUDIO_C_PCKT_RAW	1	Returns 1 if an audio clock regeneration packet has been received. Reset to 0 following a packet detection flag reset condition.
GEN_CTL_PCKT_RAW	2	Returns 1 if general control packet has been received. Reset to 0 following a packet detection flag reset condition.
HDMI_MODE_RAW	3	Returns 1 if a HDMI stream is being received. For additional information, see HDMI/DVI Status Bits section
AUDIO_CH_MD_RAW	4	Returns 1 if the audio channel mode is multichannel (2-, 4-, 6-, or 8-channel) audio. Reset to 0 following a packet detection flag reset condition. For additional information, see the Audio Channel Mode section.
AV_MUTE_RAW	5	Returns 1 if the latest general control packet received has AV_MUTE asserted. Reset to 0 following packet detection flag reset condition.
INTERNAL_MUTE_RAW	6	Returns 1 if ADV7619 has internally muted the audio data. For additional information, see the Internal Mute Status section.
CS_DATA_VALID_RAW	7 (MSB)	Returns 1 if channel status bit readback registers in HDMI map, Address 0x36 to 0x3A are valid. For additional information, see the Validity Status Flag section.

Table 34. HDMI Flags in IO Map Register 0x6A

Bit Name	Bit Position	Description
DE_REGEN_LCK_RAW	0 (LSB)	Description available in the Primary Port Horizontal Filter Measurements section.
V_LOCKED_RAW	1	Description available in the Primary Port Horizontal Filter Measurements section.
VIDEO_3D_RAW	2	Raw interrupt status of 3D video detection flag. Refer to **VIDEO_3D_ST**.
TMDS_CLK_B_RAW	3	Description available in the Fast Switching and Background Port Selection section
TMDS_CLK_A_RAW	4	Description available in the TMDS Clock Activity Detection section
TMDSPLL_LCK_B_RAW	5	Description available in the TMDS Measurement After TMDS PLL section
TMDSPLL_LCK_A_RAW	6	Description available in the TMDS Measurement After TMDS PLL section
CABLE_DET_B_RAW	7	Description available in the +5 V Cable Detect section.

Table 35. HDMI Flags in IO Map Register 0x6F

Bit Name	Bit Position	Description
CABLE_DET_A_RAW	0	Description available in the +5 V Cable Detect section.
HDMI_ENCRPT_B_RAW	1	Description available here.
HDMI_ENCRPT_A_RAW	2	Description available in the HDCP Decryption Engine section.

Table 36. HDMI Flags in IO Map Register 0x79

Bit Name	Bit Position
NEW_AVI_INFO_RAW	0 (LSB)
NEW_AUDIO_INFO_RAW	1
NEW_SPD_INFO_RAW	2
NEW_MS_INFO_RAW	3
NEW_VS_INFO_RAW	4
NEW_ACP_PCKT_RAW	5
NEW_ISRC1_PCKT_RAW	6
NEW_ISRC2_PCKT_RAW	7 (MSB)

Table 37. HDMI Flags in IO Map Register 0x7E

Bit Name	Bit Position	Description
NEW_GAMUT_MDATA_RAW	0 (LSB)	When set to 1 indicates that a gamut metadata packet with new content has been received. Once set, this bit remains high until the interrupt is cleared via NEW_GAMUT_ MDATA_PCKT_CLR. (IO Map 0x80[0]).
AUDIO_PCKT_ERR_RAW	1	When set to 1 indicates that an uncorrectable error was detected in the body of an audio packet. Once set, this bit remains high until the interrupt is cleared via AUDIO_PCKT_ERR_CLR (IO Map 0x80[1]).
PACKET_ERROR_RAW	2	When set to 1 it indicates an uncorrectable EEC error was detected in the body or header of any packet. Once set, this bit remains high until the interrupt is cleared via PACKET_ERROR_CLR (IO Map 0x80[2]).
CHANGE_N_RAW	3	When set to 1 it indicates the N value of the ACR packets has changed. Once set, this bit remains high until the interrupt is cleared via CHANGE_N_CLR (IO Map 0x80 [3]).
CTS_PASS_THRSH_RAW	4	When set to 1 it indicates the CTS value of the ACR packets has exceeded the threshold set by CTS_CHANGE_THRESHOLD. Once set, this bit remains high until the interrupt is cleared via CTS_PASS_THRSH_CLR (IO Map 0x80[4]).
FIFO_OVERFLO_RAW	5	When set to 1 it indicates the audio FIFO write pointer has reached the read pointer causing the audio FIFO to overflow. Once set, this bit remains high until the interrupt is cleared via FIFO_OVERFLO_CLR (IO Map 0x80[5]).
FIFO_UNDERFLO_RAW	6	When set to 1 it indicates the audio FIFO read pointer has reached the write pointer causing the audio FIFO to underflow. Once set, this bit remains high until the interrupt is cleared via FIFO_UNDERFLO_CLR (IO Map 0x80[6]).
FIFO_NEAR_OVFL_RAW	7 (MSB)	When set to 1 it indicates the audio FIFO is near overflow as the number FIFO registers containing stereo data is greater or equal to value set in AUDIO_FIFO_ALMOST_FULL_ THRESHOLD. Once set, this bit remains high until the interrupt is cleared via FIFO_NEAR_OVFL_CLR (IO Map 0x80[7]).

Table 38. HDMI Flags in IO Map Register 0x83

Bit Name	Bit Position	Description
FIFO_NEAR_UFLO_RAW	0 (LSB)	When set to 1 it indicates the audio FIFO is near underflow as the number of FIFO registers containing stereo data is less or equal to value set in AUDIO_FIFO_ALMOST_EMPTY_ THRESHOLD. Once set, this bit remains high until the interrupt is cleared via FIFO_NEAR_UFLO_CLR (IO Map 0x85[0]).
NEW_TMDS_FRQ_RAW	1	When set to 1 it indicates the TMDS frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0] Once set, this bit remains high until the interrupt is cleared via NEW_TMDS_FREQ_CLR (IO Map 0x85[1]).
AUDIO_FLT_LINE_RAW	2	When set to 1 it indicates audio sample packet has been received with the flat line bit set to 1. Once set, this bit remains high until the interrupt is cleared via AUDIO_FLT_LINE_ CLR (IO Map 0x85[2]).
NEW_SAMP_RT_RAW	3	When set to 1 it indicates that audio sampling frequency field in channel status data has changed. Once set, this bit remains high until the interrupt is cleared via NEW_SAMP_ RT_CLR (IO Map 0x85[3]).
PARITY_ERROR_RAW	4	When set to 1 it indicates an audio sample packet has been received with parity error. Once set, this bit remains high until the interrupt is cleared via PARITY_ERROR_CLR (IO Map 0x85 [4]).
AUDIO_MODE_CHNG_RAW	5	When set to 1 it indicates that the type of audio packet received has changed. The following are considered audio modes, no audio, PCM, DSD, HBR, or DST. AUDIO_SAMPL_PCKT_DET, DSD_PACKET_DET, DST_AUDIO_PCKT_DET, and HBR_AUDIO_PCKT_DET used identify type of audio packet currently received. Once set, this bit remains high until the interrupt is cleared via AUDIO_MODE_CHNG_CLR (IO Map 0x85[5]).
VCLK_CHNG_RAW	6	When set to 1 it indicates that irregular or missing pulses are detected in the TMDS clock. Once set, this bit remains high until the interrupt is cleared via VCLK_CHNG_CLR (IO Map 0x85[6]).
DEEP_COLOR_CHNG_RAW	7 (MSB)	When set to 1 it indicates a change in the deep color mode has been detected. Once set, this bit remains high until the interrupt is cleared via DEEP_COLOR_CHNG_CLR (IO Map 0x85[7]).

Table 39. HDMI InfoFrame Checksum Error Flags in IO Map

Bit Name	IO Map Location	Description
AVI_INF_CKS_ERR_RAW	0x88[4]	Description available in the InfoFrame Checksum Error Flags section
AUD_INF_CKS_ERR_RAW	0x88[5]	Description available in the InfoFrame Checksum Error Flags section
SPD_INF_CKS_ERR_RAW	0x88[6]	Description available in the InfoFrame Checksum Error Flags section
MS_INF_CKS_ERR_RAW	0x88[7]	Description available in the InfoFrame Checksum Error Flags section
VS_INF_CKS_ERR_RAW	0x8D[0]	Description available in the InfoFrame Checksum Error Flags section

Table 40. AKSV Update Flags and RI expired flag in IO Map Register 0x88

Bit Name	Bit Position	Description
AKSV_UPDATE_A_RAW	0	When set to 1 it indicates that transmitter has written its AKSV into HDCP registers for Port A. Once set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_A_CLR (IO Map 0x8A[0]).
AKSV_UPDATE_B_RAW	1	When set to 1 it indicates that transmitter has written its AKSV into HDCP registers for Port B. Once set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_B_CLR (IO Map 0x8A[1]).
RI_EXPIRED_A_RAW	2	Status of Port A Ri expired interrupt signal. When set to 1, it indicates that HDCP cipher Ri value for Port A is expired. Once set, this bit remains high until it is cleared via RI_EXPIRED_A_CLR (HDMI Map, 0x8A[2].
RI_EXPIRED_B_RAW	3	Status of Port B Ri expired interrupt signal. When set to 1, it indicates that HDCP cipher Ri value for Port B is expired. Once set, this bit remains high until it is cleared via RI_EXPIRED_B_CLR (0x8A[3].

Table 41. HDMI Flags in HDMI Map

Bit Name	HDMI Map Location	Description
AUDIO_PLL_LOCKED	0x04[0]	Description available in the Locking Mechanism section
AUDIO_SAMPLE_PCKT_DET	0x18[0]	Description available in the Audio Packet Type Flags section
DSD_PACKET_DET	0x18[1]	Description available in the Audio Packet Type Flags section
DST_AUDIO_PCKT_DET	0x18[2]	Description available in the Audio Packet Type Flags section
HBR_AUDIO_PCKT_DET	0x18[3]	Description available in the Audio Packet Type Flags section
DCFIFO_LOCKED	0x1C[3]	Description available in the Video FIFO section

HDMI SECTION RESET STRATEGY

The reset strategy implemented for the HDMI section is as follows:

- Global chip reset
  A global chip reset is triggered by asserting the reset pin to a low level. The HDMI section, excluding the EDID/repeater controller, is reset when a global reset is triggered.
- Loss of TMDS clock or 5 V signal reset
  A loss of TMDS clock or 5 V signal on the HDMI port selected via **HDMI_PORT_SELECT[2:0]** resets the entire HDMI section except for the EDID/repeater controller and the audio section.
  The loss of a 5 V signal condition is discarded if **DIS_CABLE_DET_RST** is set high.
- DVI mode reset
  The packet processing block, including InfoFrame memory is held in reset when the HDMI section processes a DVI stream.
- EDID/repeater controller reset
  The EDID/repeater controller is reset when the DVDD supplies go low or when HDCP_REPT_EDID_RESET is set high.

HDMI PACKET DETECTION FLAG RESET

A packet detection flag reset is triggered when any of the following events occur:

- The ADV7619 is powered up.
- The ADV7619 is reset.
- A TMDS clock is detected, after a period of no clock activity, on the selected HDMI port.
- The selected HDMI port is changed.
- The signal from the 5 V input pin of the HDMI port selected through HDMI_PORT_SELECT transitions to a high. This condition is discarded if **DIS_CABLE_DET_RST** is set high.

DATA PREPROCESSOR AND COLOR SPACE CONVERSION AND COLOR CONTROLS

COLOR SPACE CONVERSION MATRIX

The ADV7619 provides any-to-any color space support. It supports formats such as RGB, YUV, YCbCr and many other color spaces. Data Preprocessor and Component Processor are designed to run at speeds of up to 170 MHz. Therefore HDMI video with pixel clock frequencies above 170 MHz must be routed directly to Video Output Formatter bypassing Data Preprocessor (DPP) and Component Preprocessor (CP). For more information about bypassing DPP and CP please refer to Pass Through Mode section. The ADV7619 features a 3×3 CSC in the CP block (CP CSC), as shown in Figure 32. The CP CSC also provides color controls for brightness, contrast, saturation and hue adjustments. The DPP block features an automatic CSC. The ADV7619 automatically configures the DPP CSC depending on the input and output formats and the use of the color control feature.

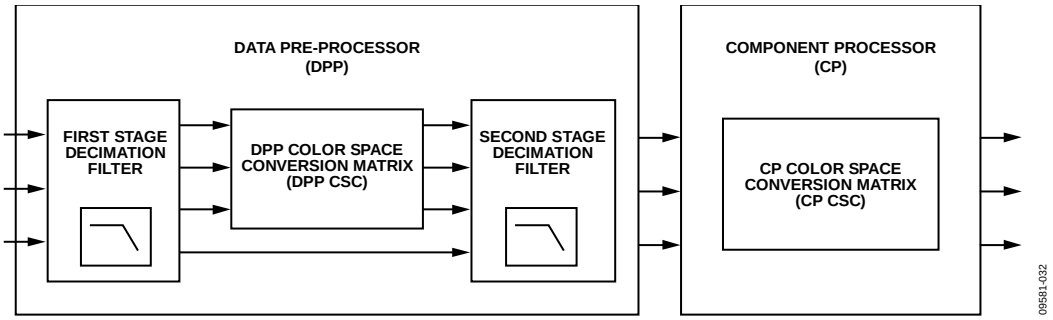


Figure 32. DPP/CP CSC Block Diagram

The configuration of the color space conversion using the CP CSC block and a description of the adjustable register bits are provided in Figure 33.

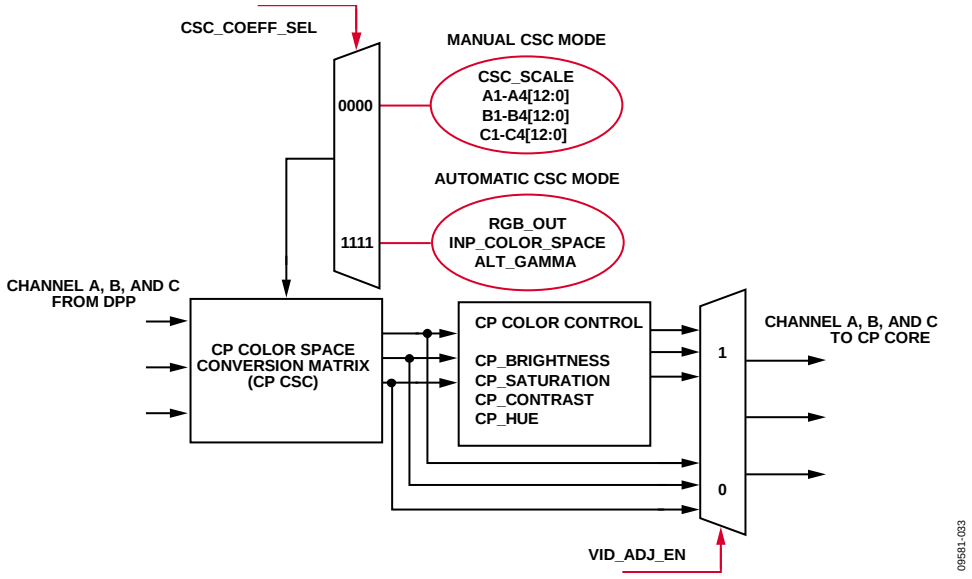


Figure 33. Configuring CP CSC Block

CP CSC Selection

MAN_CP_CSC_EN, Addr 44 (CP), Address 0x69[4]

A control to manually enable the CP CSC. By default the CP CSC will be automatically enabled in the case that either a color-space conversion or video-adjustments (hue, saturation, contrast, brightness) is determined to be required due to other I²C settings. If MAN_CP_CSC_EN is set to 1, the CP CSC is forced into the enabled state.

Function	
MAN_CP_CSC_EN	**Description**
0 (default)	CP CSC will be automatically enabled if required. For example, if either a color-space conversion or video-adjustments (hue, saturation, contrast, brightness) is determined to be required due to other I²C settings.
1	Manual override to force CP-CSC to be enabled.

Selecting Auto or Manual CP CSC Conversion Mode

The ADV7619 CP CSC provides two modes for the CSC configuration: automatic CSC mode and manual CSC mode.

In automatic CSC mode, the user is required to program the input color space and the output color space for the correct operation of the CSC matrix. Manual CSC mode allows the user to program all the color space conversion by manually programming CSC coefficients.

CSC_COEFF_SEL[3:0], Addr 44 (CP), Address 0x68[7:4]

A control to select the mode the CP CSC operates in.

Function

CSC_COEFF_SEL[3:0]	Description
0000	CP CSC configuration in manual mode
1111 (default)	CP CSC configured in automatic mode
xxxx	Reserved

The selection of the CSC is automated in the ADV7619. Automatic or manual CSC mode can be selected by setting the CSC_COEFF_SEL[3:0] bits. When CSC_COEFF_SEL[3:0] is set to 0b1111, the CSC mode is automatically selected, based on the input color space and output color space required and set through the following registers:

- **INP_COLOR_SPACE[3:0]**
- **RGB_OUT**
- **ALT_GAMMA**

Auto Color Space Conversion Matrix

The CSC matrix, AGC target gain values, and offset values can be configured automatically via the following set of registers:

- INP_COLOR_SPACE[3:0]
- RGB_OUT
- ALT_GAMMA
- OP_656_RANGE_SEL

INP_COLOR_SPACE[3:0], IO, Address 0x02[7:4]

A control to set the color space of the input video. To be used in conjunction with ALT_GAMMA and RGB_OUT to configure the color space converter. A value of 4'b1111 selects automatic setting of the input color space base on the primary mode and video standard settings. Setting 1000 to Setting 1110 are undefined.

Function

INP_COLOR_SPACE[3:0]	Description
0000	Forces RGB (range 16 to 235) input
0001	Forces RGB (range 0 to 255) input
0010	Forces YCrCb input (601 color space) (range 16 to 235)
0011	Forces YCrCb input (709 color space) (range 16 to 235)
0100	Forces XVYCC 601
0101	Forces XVYCC 709
0110	Forces YCrCb input (601 color space) (range 0 to 255)
0111	Forces YCrCb input (709 color space) (range 0 to 255)
1111 (default)	Input color space depends on color space reported by HDMI block.

Table 42. Automatic Input Color Space Selection

PRIM_MODE[3:0]	VID_STD[5:0]	Input Color Space	Input Range	Comments
0101	xxxx	Dependent on AVI InfoFrame	0:255 for YUV Dependent on AVI InfoFrame for RGB	HDMI component modes
0110	xxxx	Dependent on AVI InfoFrame	0:255 for YUV Dependent on AVI InfoFrame for RGB	HDMI graphic modes

RGB_OUT, IO, Address 0x02[1]

A control to select output color space and the correct digital blank level and offsets on the RGB or YPrPb outputs. It is used in conjunction with the INP_COLOR_SPACE[3:0] and ALT_GAMMA bits to select the applied CSC.

Function

RGB_OUT	Description
0 (default)	YPbPr color space output
1	RGB color space output

ALT_GAMMA, IO, Address 0x02[3]

A control to set the color space of the input video. To be used in conjunction with ALT_GAMMA and RGB_OUT to configure the color space converter. A value of 4'b1111 selects automatic setting of the input color space base on the primary mode and video standard settings. Setting 1000 to Setting 1110 are undefined.

Function

ALT_GAMMA	Description
0 (default)	No conversion
1	YUV601 to YUV709 conversion applied if input is YUV601. YUV709 to YUV601 conversion applied if input is YUV709

Table 43. Automatic CSC Selection

		CSC Mode Used (Output)	
INP_COLOR_SPACE[3:0] (Input Color Space)	RGB_OUT	ALT_GAMMA = 0	ALT_GAMMA = 1
00 = RGB	0	YCbCr 601	YCbCr 709
	1	RGB	RGB
01 = (YCbCr /YUV 601)	0	YCbCr 601	YCbCr 709
	1	RGB	RGB
10 = (YCbCr /YUV 709)	0	YCbCr 709	YCbCr 601
	1	RGB	RGB

CSC_COEFF_SEL_RB[3:0], Addr 44 (CP), Address 0xF4[7:4] (Read Only)

Readback of the CP CSC conversion when configured in automatic mode.

Function

CSC_COEFF_SEL_RB[3:0]	Description
0000 (default)	CSC is bypassed
0001	YPbPr 601 to RGB
0011	YPbPr 709 to RGB
0101	RGB to YPbPr 601
0111	RGB to YPbPr 709
1001	YPbPr 709 to YPbPr 601
1010	YPbPr 601 to YPbPr 709
1111	CSC in manual mode
xxxx	Reserved

Table 44. CSC Configuration for All CSC Modes Reported by CSC_COEFF_SEL_RB

CSC Mode	CSC_ SCALE [1:0]	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4
0b0000	CSC in bypass mode. In this mode the CSC effectively performs a color conversion based on the CSC coefficients set in registers CSC_SCALE, A1, A2, A3, A4, B1, B2, B3, B4, C1, C2, C3, and C4.												
0b0001	0b01	0x0800	0x1A6A	0x1D50	0x0423	0x0800	0x0AF8	0x0000	0x1A84	0x0800	0x0000	0x0DDB	0x1912
0b0011	0b01	0x0800	0x1C54	0x1E89	0x0291	0x0800	0x0C52	0x0000	0x19D7	0x0800	0x0000	0x0E87	0x18BC
0b0101	0b00	0x0964	0x04C9	0x01D3	0x0000	0x1927	0x082D	0x1EAC	0x0800	0x1A93	0x1D3F	0x082D	0x0800
0b0111	0b00	0x0B71	0x0368	0x0127	0x0000	0x1893	0x082D	0x1F3F	0x0800	0x19B2	0x1E21	0x082D	0x0800
0b1001	0b01	0x0800	0x0188	0x00CB	0x1ED7	0x0000	0x07DE	0x1F6C	0x005B	0x0000	0x1F1D	0x07EB	0x007B
0b1010	0b01	0x0800	0x1E56	0x1F14	0x014A	0x0000	0x0834	0x009A	0x1F9A	0x0000	0x00EB	0x0826	0x1F78

HDMI Automatic CSC Operation

In HDMI mode, the ADV7619 provides an automatic CSC function based on the AVI InfoFrame sent from the source. The flowchart in Figure 34 shows the mechanism of the ADV7619 auto CSC functionality in HDMI mode.

Note: In the following flowcharts, a red dashed line represents a state that is undefined according to the CEA-861D specification, and therefore should never happen. In the event that it did somehow occur, the ADV7619 retains the previous colorimetry.

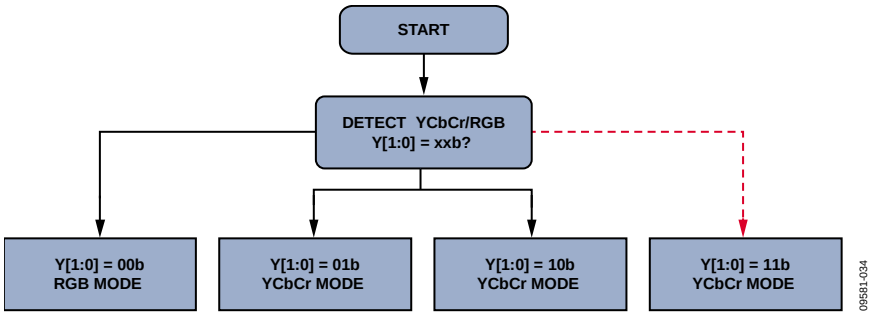


Figure 34. HDMI Auto CSC Flowchart

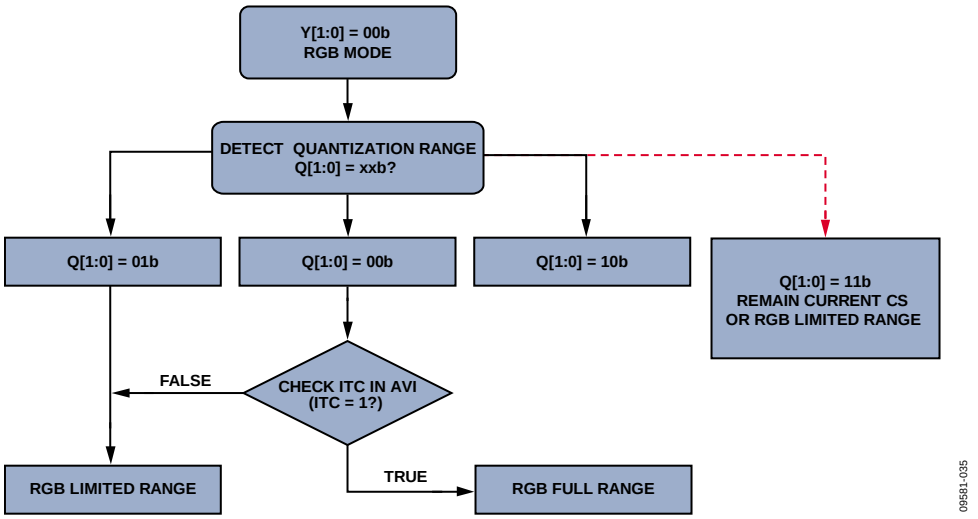


Figure 35. HDMI Auto CSC Flowchart (Case RGB)

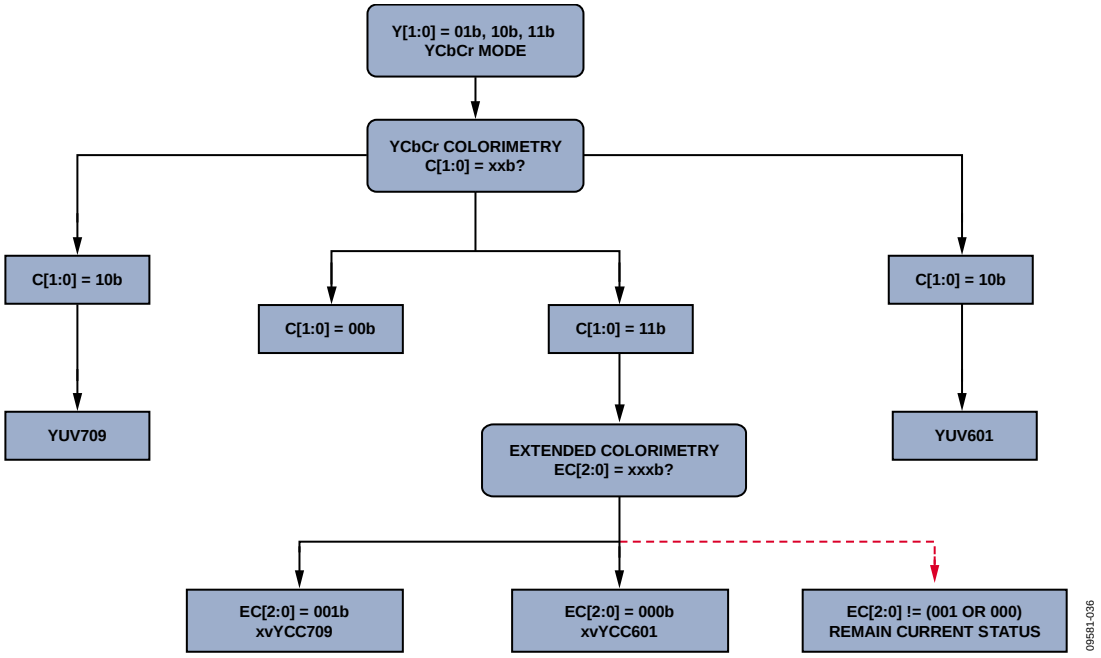


Figure 36. HDMI Auto CSC Flowchart (Case YCbCr-1)

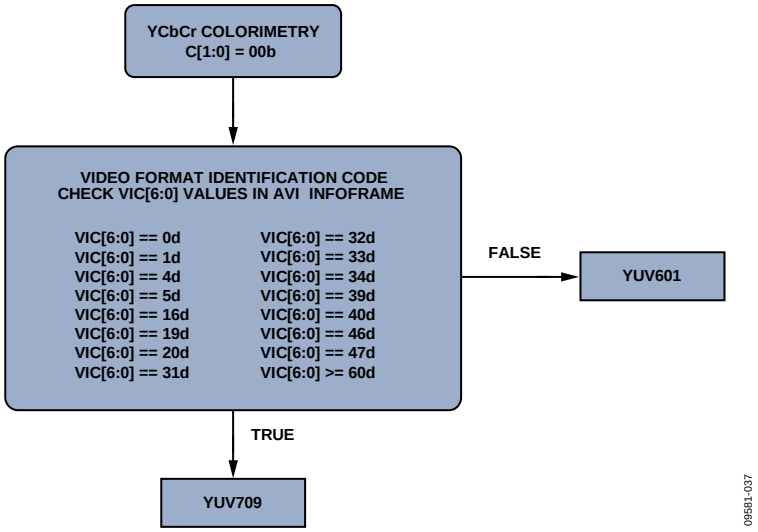


Figure 37. HDMI Auto CSC Flowchart (Case YCbCr-2)

In the RGB case (refer to Figure 38), the ADV7619 has the programmability to control manually the RGB limited/full range regardless of the ITC bit.

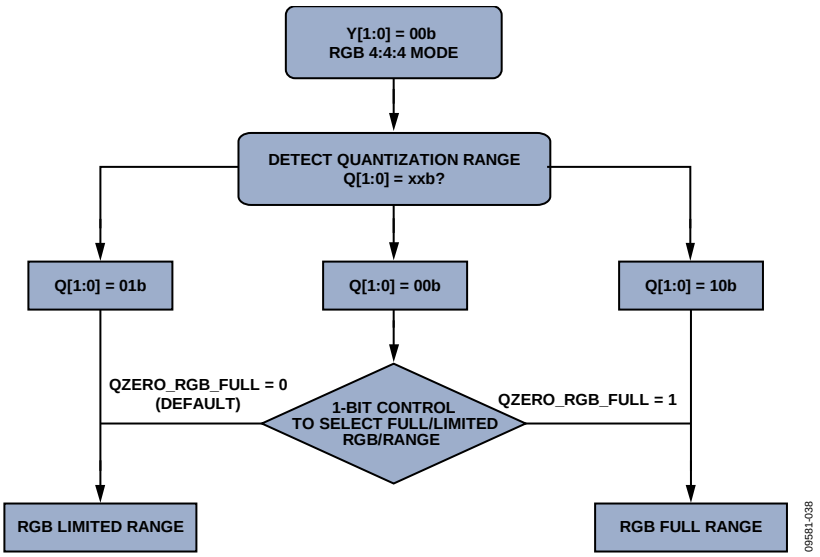


Figure 38. Manual RGB Range Control Flowchart for Auto CSC (Case RGB)

QZERO_ITC_DIS, Addr 68 (HDMI), Address 0x47[2]

A control to select manual control of the RGB colorimetry when the AVI InfoFrame field Q[1:0] = 00. To be used in conjunction with QZERO_RGB_FULL.

Function

QZERO_ITC_DIS	Description
0 (default)	AVI InfoFrame ITC bit decides RGB-full or limited range in case Q[1:0] = 00
1	Manual RGB range as per QZERO_RGB_FULL

QZERO_RGB_FULL, Addr 68 (HDMI), Address 0x47[1]

A control to manually select the HDMI colorimetry when AVI InfoFrame field Q[1:0] = 00. Valid only when QZERO_ITC_DIS is set to 1.

Function

QZERO_RGB_FULL	Description
0 (default)	RGB-limited range when Q[1:0] = 00
1	RGB-full when Q[1:0] = 00

Manual Color Space Conversion Matrix

The CP CSC matrix in the ADV7619 is a 3 x 3 matrix with full programmability of all coefficients in the matrix in manual mode. Each coefficient is 12-bits wide to ensure signal integrity is maintained in the CP CSC section. The CP CSC contains three identical processing channels, one of which is shown in Figure 39. The main inputs labeled In_A, In_B, and In_C come from the 36-bit digital input from the HDMI section. Each input to the individual channels to the CSC is multiplied by a separate coefficient for each channel.

In Figure 39, these coefficients are marked A1, A2 and A3. The variable labeled A4 is used as an offset control for channel A in the CSC. There is also a further CP CSC control bit labeled **CSC_SCALE[1:0]**; this control can be used to accommodate coefficients that extend the supported range. The functional diagram for a single channel in the CP CSC as per Figure 39 is repeated for the other two remaining channels, B and C. The coefficients for these channels are called B1, B2, B3, B4, C1, C2, C3, and C4.

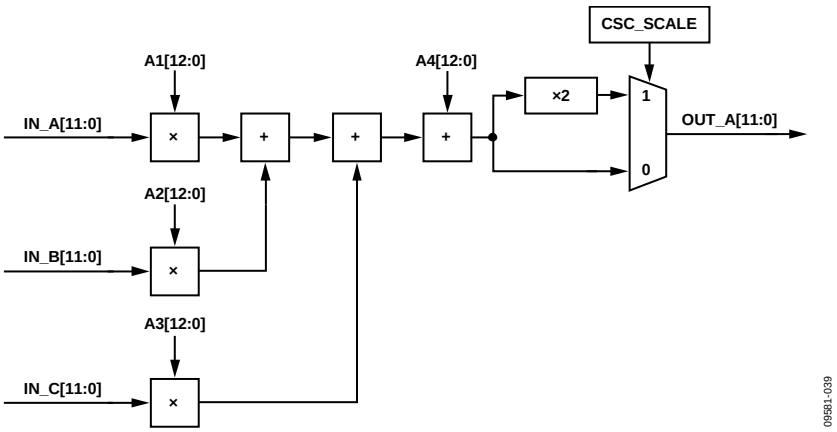


Figure 39. Single CSC Channel

The coefficients mentioned previously are detailed in Table 45 along with the default values for these coefficients.

Table 45. CSC Coefficients

Function Bit	CP Map Address	Reset Value (Hex)	Description
A1[12:0]	0x57[4:0], 0x58[7:0]	0x800	Coefficient for Channel A
A2[12:0]	0x55[1:0], 0x56[7:0], 0x57[7:5]	0x000	Coefficient for Channel A
A3[12:0]	0x54[6:0], 0x55[7:2]	0x000	Coefficient for Channel A
B1[12:0]	0x5E[4:0], 0x5F[7:0]	0x000	Coefficient for Channel B
B2[12:0]	0x5C[1:0], 0x5D[7:0], 0x5E[7:5]	0x800	Coefficient for Channel B
B3[12:0]	0x5B[6:0], 0x5C[7:2]	0x000	Coefficient for Channel B
C1[12:0]	0x65[4:0], 0x66[7:0]	0x000	Coefficient for Channel C
C2[12:0]	0x63[1:0], 0x64[7:0], 0x65[7:5]	0x000	Coefficient for Channel C
C3[12:0]	0x62[6:0], 0x63[7:2]	0x800	Coefficient for Channel C
CSC_SCALE[1:0]	0x52[7:6]	0x01	Scaling for CSC formula
A4[12:0]	0x52[4:0], 0x53[7:0]	0x000	Offset for Channel A
B4[12:0]	0x59[4:0], 0x5A[7:0]	0x000	Offset for Channel B
C4[12:0]	0x60[4:0], 0x61[7:0]	0x000	Offset for Channel C

CSC_SCALE[1:0], Addr 44 (CP), Address 0x52[7:6]

A control to set the CSC coefficient scalar.

Function

CSC_SCALE[1:0]	Description
00	CSC scalar set to 1.
01 (default)	CSC scalar set to 2.
10	Reserved. Do not use.
11	Reserved. Do not use.

CSC Manual Programming

The equations performed by the CP CSC are as follows:

CSC Channel A

$$Out\_A = \left[In\_A \times \frac{A1[12:0]}{4096} + In\_B \times \frac{A2[12:0]}{4096} + In\_C \times \frac{A3[12:0]}{4096} + A4[12:0] \right] \times 2^{CSC\_scale} \quad (4)$$

CSC Channel B

$$Out\_B = \left[In\_A \times \frac{B1[12:0]}{4096} + In\_B \times \frac{B2[12:0]}{4096} + In\_C \times \frac{B3[12:0]}{4096} + B4[12:0] \right] \times 2^{CSC\_scale} \quad (5)$$

CSC Channel C

$$Out\_C = \left[In\_A \times \frac{C1[12:0]}{4096} + In\_B \times \frac{C2[12:0]}{4096} + In\_C \times \frac{C3[12:0]}{4096} + C4[12:0] \right] \times 2^{CSC\_scale} \quad (6)$$

As can be seen from Equation 4, Equation 5, and Equation 6, the A1, A2, A3; B1, B2, B3; and C1, C2, C3 coefficients are used to scale the primary inputs. The values of A4, B4, and C4 are added as offsets. The **CSC_SCALE[1:0]** bits allows the user to implement conversion formulain which the coefficients exceed the standard range of [-4095/4096 .. 4095/4096]. The overall range of the CSC is [0..1] for unipolar signals (for example, Y, R, G, and B) and [−0.5 … +0.5] for bipolar signals (for example, Pr and Pb).

Note: The bipolar signals must be offset to midrange, for example, 2048.

To arrive at programming values from typical formulas, the following steps are performed:

1. Determine the dynamic range of the equation.
   The dynamic range of the CSC is [0 … 1] or [−0.5 … +0.5]. Equations with a gain larger than 1 need to be scaled back. Errors in the gain can be compensated for in the gain stages of the follow on blocks.
   - Scale the equations, if necessary.
2. Check the value of each coefficient. The coefficients can only be programmed in the range [−0.99 … +0.99].
3. To support larger coefficients, the **CSC_SCALE[1:0]** function should be used.
4. Determine the setting for **CSC_SCALE[1:0]** and adjust coefficients, if necessary.
5. Program the coefficient values. Convert the float point coefficients into 12-bit fixed decimal format. Convert into binary format, using twos complement for negative values.
   - Program A1 to A3, B1 to B3, C1 to C3.
6. Program the offset values. Depending on the type of CSC, offsets may have to be used.
   - Program A4, B4, C4.

CSC Example

The following set of equations gives an example of a conversion from a gamma corrected RGB signal into a YCbCr color space signal.

$$Out\_A = \left[In\_A \times \frac{A1[12:0]}{4096} + In\_B \times \frac{A2[12:0]}{4096} + In\_C \times \frac{A3[12:0]}{4096} + A4[12:0] \right] \times 2^{CSC\_scale}$$

$$Out\_B = \left[In\_A \times \frac{B1[12:0]}{4096} + In\_B \times \frac{B2[12:0]}{4096} + In\_C \times \frac{B3[12:0]}{4096} + B4[12:0] \right] \times 2^{CSC\_scale}$$

$$Out\_C = \left[In\_A \times \frac{C1[12:0]}{4096} + In\_B \times \frac{C2[12:0]}{4096} + In\_C \times \frac{C3[12:0]}{4096} + C4[12:0] \right] \times 2^{CSC\_scale}$$

Note: The original equations give offset values of 128 for the Pr and Pb components. The value of 128 equates to half the range on an 8-bit system. It must be noted that the CSC operates on a 12-bit range. The offsets, therefore, must be changed from 128 to half the range of a 12-bit system, which equates to 2048.

The maximum range for each equation, that is, each output data path, can only be [0 ... 1] or [−0.5 ... +0.5]. Equations with a larger gain must be scaled back into range. The gain error can be compensated for in the gain stage of the follow on blocks.

The ranges of the three equations are shown in Table 46.

Table 46. Equation Ranges

Equation	Minimum Value	Maximum Value	Range
Y	0 + 0 + 0 = 0	0.59 + 0.3 + 0.11 = 1	[0 … 1] = 1
Pb	(−0.34) + (−0.17) = −0.51	0.51	[−0.51 …+ 0.51] = 1.02
Pr	(−0.43) + (−0.08) = −0.51	0.51	[−0.51 … +0.51] = 1.02

As can be seen from this table, the range for the Y component fits into the CSC operating range. However, the Pb and Pr ranges slightly exceed the range. To bring all equations back into the supported range, they should be scaled back by 1/1.02.

If equations fall outside the supported range, overflow or underflow can occur and undesirable wrap around effects (large number overflowing to small ones) can happen.

$$Y = \frac{0.59}{1.02} \times G + \frac{0.3}{1.02} \times R + \frac{0.11}{1.02} \times B = 0.58 \times G + 0.29 \times R + 0.11 \times B$$

$$Pb = \frac{-0.34}{1.02} \times G + \frac{-0.17}{1.02} \times R + \frac{0.51}{1.02} \times B + 2048 = -0.33 \times G - 0.17 \times R + 0.5 \times B + 2048$$

$$Pr = \frac{-0.43}{1.02} \times G + \frac{0.51}{1.02} \times R + \frac{-0.08}{1.02} \times B + 2048 = -0.42 \times G + 0.5 \times R - 0.08 \times B + 2048$$

Note that the scaling of the dynamic range does not affect the static offset.

Check the Value of Each Coefficient

The maximum value for each coefficient on its own can only be within the range of −4096/+4096 to 4095/4096, which equals [1… +0.999755859375]. Values outside this range do not fit into the 12-bit fixed point format used to program the coefficients.

If the value of one or more coefficients after scaling of the overall equation exceeds the supported coefficient range, the **CSC_SCALE[1:0]** should be set.

With the **CSC_SCALE[1:0]** set high, all coefficients must be scaled by half, which makes them fit into the given coefficient range. The overall outputs of the CSC are gained up by a fixed value of two, thus compensating for the scaled down coefficients.

In the preceding example, each coefficient on its own is within the range of

$$\frac{-4095}{4096} \leq Coeff \leq \frac{4095}{4096}$$

Therefore, all coefficients can be programmed directly and the **CSC_SCALE[1:0]** bit should be set to 0.

Notes

- To achieve a coefficient value of 1.0 for any given coefficient, CSC_SCALE should be set high and the coefficient should actually be programmed to a value of 0.5. Otherwise, the largest value would be 4095/4096 = 0.9997, which is not exactly 1. While this value could be interpreted as a 1, it is recommended to use the value of 0.5 and the CSC_SCALE bit for maximum accuracy.
- For very large coefficient values, for example, 2.58, a combination of **CSC_SCALE[1:0]** and equation scaling should be used.
- Set CSC_SCALE high (2.58/2 = 1.29) and scale the overall equation by slightly more than 1.28 (coefficient falls within the supported range of [−0.999 … +0.999]).

CSC in Pass-Through Mode

It is possible to configure the CP CSC in a pass-through mode. In this mode, the CP CSC is used but does not alter the data it processes.

The CP CSC pass-through mode is obtained using the following settings:

1. Set **MAN_CP_CSC_EN** to 1'b1.
2. Set **CSC_COEFF_SEL[3:0]** to 4'b0000.
3. Leave the following registers from the CP map at the default:
   CSC_SCALE = 1 (default value)
   A4 = A3 = A2 = 0x000 (default value)
   B4 = B3 = B1 = 0x000 (default value)
   C4 = C2 = C1 = 0x000 (default value)
   A1 = B2 = C3 = 0x800 (default value)

Note: The DPP CSC is always in pass-through mode unless the ADV7619 is processing an RGB input, outputting this input in the RGB color space and **VID_ADJ_EN** is enabled.

COLOR CONTROLS

The ADV7619 has a color control feature that can adjust the brightness, contrast, saturation, and hue properties.

VID_ADJ_EN, Addr 44 (CP), Address 0x3E[7]

Video adjustment enable. This control selects whether or not the color controls feature is enabled. The color controls feature is configured via the parameters CP_CONTRAST[7:0], CP_SATURATION[7:0], CP_BRIGHTNESS[7:0] and CP_HUE[7:0]. The CP CSC must also be enabled for the color controls to be effective.

Function

VID_ADJ_EN	Description
0 (default)	Disable color controls
1	Enable color controls

CP_CONTRAST[7:0], Addr 44 (CP), Address 0x3A[7:0]

A control to set the contrast. This field is a unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value, which is either 0 or 1. The seven LSBs represent the fractional part of the contrast value. The fractional part has the range [0 to 0.99]. This control is functional if VID_ADJ_EN is set to 1.

Function

CP_CONTRAST[7:0]	Description
00000000	Contrast set to minimum
10000000 (default)	Default
11111111	Contrast set to maximum

CP_SATURATION[7:0], Addr 44 (CP), Address 0x3B[7:0]

A control to set the saturation. This field is an unsigned value represented in a 1.7 binary format. The MSB represents the integer part of the contrast value, which is either 0 or 1. The seven LSBs represent the fractional part of the saturation value. The fractional part has a [0 to 0.99] range. This control is functional if VID_ADJ_EN is set to 1.

Function

CP_SATURATION[7:0]	Description
00000000	Saturation set to minimum
10000000 (default)	Default
11111111	Saturation set to maximum

CP_BRIGHTNESS[7:0], Addr 44 (CP), Address 0x3C[7:0]

A control to set the brightness. This field is a signed value. The effective brightness value applied to the luma is obtained by multiplying the programmed value CP_BRIGHTNESS with a gain of 4. The brightness applied to the luma has a range of [−512 to +508]. This control is functional if VID_ADJ_EN is set to 1.

Function

CP_BRIGHTNESS[7:0]	Description
00000000 (default)	The offset applied to the luma is 0.
01111111	The offset applied to the luma is 508d. This value corresponds to the brightness setting.
11111111	The offset applied to the luma is −512d. This value corresponds to the darkest setting.

CP_HUE[7:0], Addr 44 (CP), Address 0x3D[7:0]

A control to set the hue. This register a represent an unsigned value which provides hue adjustment. Following control processes, Cb and Cr stream as follow:

$$Cb\_out = Cb \times cos(hue) + Cr \times sin(hue)$$

$$Cr\_out = Cr \times cos(hue) - Cb \times sin(hue)$$

It allows for rotating hue by any angle <0; 360). This control is functional if VID_ADJ_EN is set to 1.

Function

CP_HUE[7:0]	Description
0x00 (default)	A hue of 0° is applied to the chroma
0x40	A hue of 90° is applied to the chroma
0x80	A hue of 180° is applied to the chroma
0xC0	A hue of 270° is applied to the chroma

COMPONENT PROCESSOR

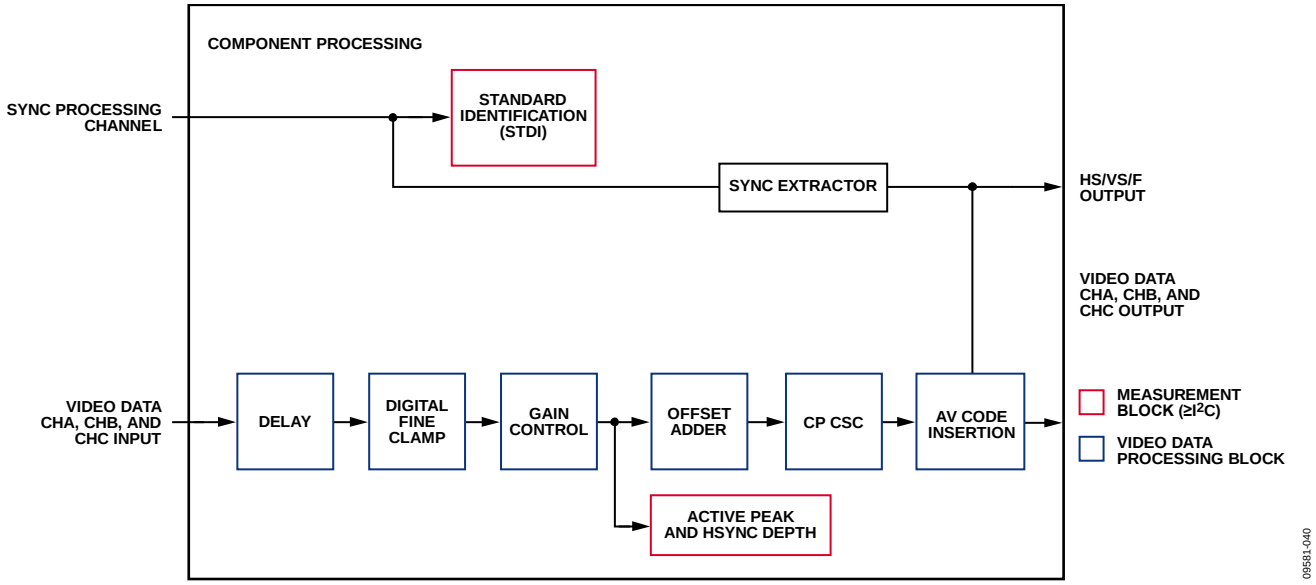


Figure 40. Component Processor Block Diagram

INTRODUCTION TO THE COMPONENT PROCESSOR

A simplified block diagram of the the component processor (CP) on the ADV7619 is shown in Figure 40. Data is supplied to the CP from the data preprocessor (DPP). The CP circuitry is activated under the control of **PRIM_MODE[3:0]** and **VID_STD[5:0]**.

The CP is designed to run at speeds of up to 170 MHz. Therefore HDMI video with pixel clock frequencies above 170 MHz must be routed directly to Video Output Formatter bypassing Data Preprocessor (DPP) and Component Preprocessor (CP). For more information about bypassing DPP and CP refer to Pass Through Mode section.

The CP is activated for the following modes of operation:

- Manual and automatic gain control
- Manual offset correction
- Saturation
- Insertion of timing codes and blanking data

The CP also has the following capabilities:

- Generates HSync, VSync, FIELD, and data enable (DE) timing reference outputs
- Color space conversion
- Color control adjustment

CLAMP OPERATION

The CP contains a digital fine clamp block. Its main purposes is to allow a clamp to operate even if the input signal is coming from a digital source

The digital fine clamp operates in three separate feedback loops, one for each channel. The incoming video signal level is measured at the back porch. The level error, that is, clamp error, is compensated for by subtracting or adding a digital number to the data stream.

The digital clamp loop can be operated in an automatic or a manual mode with the following options:

- The clamp values for Channel B and Channel C can be set manually. This is the recommended mode.
- The clamp value is determined automatically on a line-by-line basis.
- The clamp loops can be frozen. This means that the currently active offsets will no longer be updated but will be applied permanently.
- The clamp value for channel A can be set manually (static value).

Note: The target clamp level for black input is a digital code of 0. This is to facilitate the highest possible signal to noise ratio (SNR). Some interfaces, for example, ITU-R. BT656, require black to correspond to a value other than 0. To facilitate this, there is an additional independent offset adder block after the gain multipliers for which separate fixed offset values can be supplied. Refer to the CP Offset Block section for additional information.

CLMP_FREEZE, Addr 44 (CP), Address 0x6C[5]

Stops the digital fine clamp loops for Channel A, Channel B, and Channel C from updating.

Function

CLMP_FREEZE	Description
0 (default)	Clamp value updated on every active video line
1	Clamp loops are stopped and not updated

CLMP_A_MAN, Addr 44 (CP), Address 0x6C[7]

Manual clamping enable for Channel A.

Function

CLMP_A_MAN	Description
0 (default)	Ignore internal digital fine clamp loop result. Use CLMP_A[11:0].
1	Use the digital fine clamp value determined by the on-chip clamp loop.

CLMP_A[11:0], Addr 44 (CP), Address 0x6C[3:0]; Address 0x6D[7:0]

Manual clamp value for Channel A. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_A_MAN is set to 1. To change the CLMP_A[11:0], Register Address 0x6C and Register Address 0x6D must be updated with the desired clamp value written to in this order and with no other I^2C access in between.

Function

CLMP_A[11:0]	Description
0x000 (default)	Minimum range
…	…
0xFFF	Maximum range

To facilitate an external clamp loop for Channel B and Channel C, the internal clamp value determined by the digital fine clamp block can be overridden by manual values programmed in the CP map. Both Channel B and Channel C are either in manual or automatic mode. There is no individual control for them.

The corresponding control values are **CLMP_BC_MAN**, **CLMP_B[11:0]**, **CLMP_C[11:0]**.

CLMP_BC_MAN, Addr 44 (CP), Address 0x6C[6]

Manual clamping enable for Channel B and Channel C.

Function

CLMP_BC_MAN	Description
0 (default)	Ignore internal digital fine clamp loop result. Use CLMP_B[11:0] for Channel B and CLMP_C[11:0] for Channel C.
1	Use the digital fine clamp value determined by the on-chip clamp loop.

CLMP_B[11:0], Addr 44 (CP), Address 0x6E[7:0]; Address 0x6F[7:4]

Manual clamp value for Channel B. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_BC_MAN is set to 1. To change the CLMP_B[11:0], Register Address 0x6E and Register Address 0x6F must be updated with the desired clamp value written to in this order and with no other I^2C access in between.

Function

CLMP_B[11:0]	Description
0x000 (default)	Minimum range
…	…
0xFFF	Maximum range

CLMP_C[11:0], Addr 44 (CP), Address 0x6F[3:0]; Address 0x70[7:0]

Manual clamp value for Channel C. This field is an unsigned 12-bit value to be subtracted from the incoming video signal. This value programmed in this register is effective if the CLMP_BC_MAN is set to 1. To change the CLMP_C[11:0], Register Address 0x6F and Register Address 0x70 must be updated with the desired clamp value written to in this order and with no other I²C access in between.

Function

CLMP_C[11:0]	Description
0x000 (default)	Minimum range
…	…
0xFFF	Maximum range

CP GAIN OPERATION

The digital gain block of the CP consists of three multipliers in the data paths of Channel A, Channel B, and Channel C, as well as one single automatic gain control loop. The gain control can be operated in manual or automatic mode.

Features of Manual Gain Control

The gain values for the three channels can be programmed separately via I²C registers. This is the recommended mode.

Features of Automatic Gain Control

The gain value is determined automatically, based on a signal with an embedded horizontal synchronization pulse on Channel A. The automatic gain control loop can be frozen, for example, after settling.

The gain value inputs are controlled via the **OP_656_RANGE** bit.

Manual Gain and Automatic Gain Control Selection

Figure 41 shows how the gain is applied to the video data processed by the CP section. The following gain configurations are available:

- Automatic gain configuration in HDMI mode
  This configuration is enabled by setting **AGC_MODE_MAN** to 0 and by setting the part in HDMI mode via **PRIM_MODE[3:0]** and **VID_STD[5:0]**. In that case, the gain applied to the video data depends on the input and output range configuration. The input range is set by control register INP_COLOR_SPACE and the read back register **HDMI_COLORSPACE[3:0]** as per Table 47. The output color space is determined the control bit **OP_656_RANGE**.
- Manual gain configuration
  This configuration is enabled by setting **AGC_MODE_MAN** to 1 and **GAIN_MAN** to 1. In this case the gain applied to the video data processed by the CP core is configured via the control registers **A_GAIN[9:0]**, **B_GAIN[9:0]** and **C_GAIN[9:0]**.

Table 47. Input Ranges for HDMI Modes

INP_COLOR_SPACE	Input Range
0b0000	16 to 235
0b0001	0 to 255
0b0010	16 to 235
0b0011	16 to 235
0b0100	0 to 255
0b0101	0 to 255
0b0110	0 to 255
0b0111	0 to 255
0b1111	16 to 235 if HDMI_COLORSPACE = 0b000 0 to 255 if HDMI_COLORSPACE = 0b001 16 to 235 if HDMI_COLORSPACE = 0b010 16 to 235 if HDMI_COLORSPACE = 0b011 0 to 255 if HDMI_COLORSPACE = 0b100 0 to 255 if HDMI_COLORSPACE = 0b101 0 to 255 if HDMI_COLORSPACE = 0b110 0 to 255 if HDMI_COLORSPACE = 0b111
0b1000 to 0b1110	Reserved

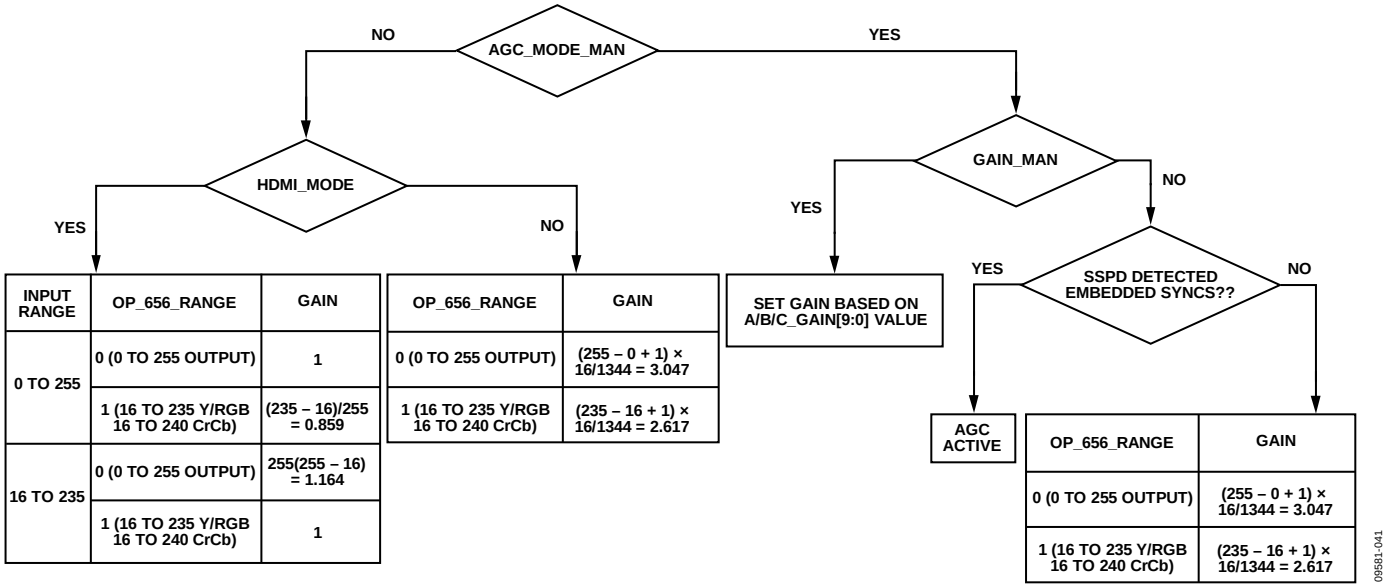


Figure 41. CP Automatic Gain Controls

AGC_MODE_MAN, Addr 44 (CP), Address 0x73[6]

A control to set how the gains for all three channels are configured.

Function

AGC_MODE_MAN	Description
0 (default)	The gain is dependent on the type of input and OP_656_RANGE.
1	Gain operation controlled by GAIN_MAN.

Manual Gain Control

By setting the **GAIN_MAN** bit, the gain factors for Channel A, Channel B, and Channel C are no longer taken from the AGC, but are replaced by three dedicated I^2C registers.

Using these factors with the **HSD_FB[11:0]** register, it is possible to implement an off-chip AGC if desired. The range for the gain is [0…3.999]. The **A_GAIN[9:0]**, **B_GAIN[9:0]**, **C_GAIN[9:0]** registers are in 2.8 binary format and can be set as shown in Equation 8, CP manual gain.

$$X\_GAIN[9:0] = \text{floor}(GAIN \times 256) \quad (8)$$

where:
$0 \leq GAIN < 4$.
floor( ) is the floor function that returns the largest integer not greater than its input parameter.
X refers to A, B, and C.

Table 48. Example

Example $Gain_{dec}$	A_GAIN[9:0]
0.5	0x80
0.98887	0xFD
2.5	0x280

GAIN_MAN, Addr 44 (CP), Address 0x73[7]

Enables the gain factor to be set by the AGC or manually.

Function

GAIN_MAN	Description
0 (default)	AGC controls the gain for all three channels.
1	Manual gains are used for all three channels.

A_GAIN[9:0], Addr 44 (CP), Address 0x73[5:0]; Address 0x74[7:4]

A control to set the manual gain value for Channel A.

This register is an unsigned value in a 2.8 binary format. To change A_GAIN[9:0], the register at Address 0x73 and Address 0x74 must be written to in this order with no I²C access in between.

Function

A_GAIN[9:0]	Description
0x000	Gain of 0
0x100 (default)	Unity gain
0x3FF	Gain of 3.99

B_GAIN[9:0], Addr 44 (CP), Address 0x74[3:0]; Address 0x75[7:2]

A control to set the manual gain value for Channel B.

This register stores an unsigned value in a 2.8 binary format. To change B_GAIN[9:0], the register at Address 0x74 and Address 0x75 must be written to in this order with no I²C access in between.

Function

B_GAIN[9:0]	Description
0x000	Gain of 0
0x100 (default)	Unity gain
0x3FF	Gain of 3.99

C_GAIN[9:0], Addr 44 (CP), Address 0x75[1:0]; Address 0x76[7:0]

A control to set the manual gain value for Channel C.

This register stores an unsigned value in a 2.8 binary format. To change C_GAIN[9:0], the register at Address 0x75 and Address 0x76 must be written to in this order with no I²C access in between.

Function

C_GAIN[9:0]	Description
0x000	Gain of 0
0x100 (default)	Unity gain
0x3FF	Gain of 3.99

HSD_FB[11:0], Addr 44 (CP), Address 0xEB[3:0]; Address 0xEC[7:0] (Read Only)

A readback for the measured value of HSync depth on Channel A, after gain multiplier, for external feedback loop.

The value is presented in twos complement form. This means that only a standard adder is needed to subtract the actual HSync depth (as per HSD_FB) from a nominal value, as the HSD_FB value is already in negative format.

Function

HSD_FB[11:0]	Description
xxxxxxxxxxxx	Readback value

Manual Gain Filter Mode

The ADV7619 provides a special filter option for the manual gain mode. This is functional only when manual gain is enabled. The purpose of this filter is a smoothing mechanism when the manual gain value is updated continuously by an external system based on either external or readback conditions in the ADV7619. The filter designed is an IIR filter with a transfer function of the form:

$$YN = (1 - A) \times YN - 1 + A \times XN$$

where A is the filter coefficient.

The values possible for A can vary from 1 (no filtering) to 1/128K (K = 1024). The value of coefficient A is chosen by programming **CP_GAIN_FILT[3:0]**.

CP_GAIN_FILT[3:0], Addr 44 (CP), Address 0x84[7:4]

A control to set the coefficient A of the IIF filter to filter the gain applied to the video signal when the gain is manually set. The value set in this register is effective only when manual gain is enabled. The filter is designed as an IIR filter with a transfer function of the form

$$Y[N] = (1 - A) \times y[N - 1] + A \times X[N]$$

Function

CP_GAIN_FILT[3:0]	Description
0000 (default)	No filtering, that is, coefficient A = 1.
0001	Coefficient A = 1/128 lines.
0010	Coefficient A = 1/256 lines.
0011	Coefficient A = 1/512 lines.
0100	Coefficient A = 1/1024 lines.
0101	Coefficient A = 1/2048 lines.
0110	Coefficient A = 1/4096 lines.
0111	Coefficient A = 1/8192 lines.
1000	Coefficient A = 1/16,384 lines.
1001	Coefficient A = 1/32,768 lines.
1010	Coefficient A = 1/65,536 lines.
1011	Coefficient A = 1/131,072 lines.
All other values	Reserved. Do not use.

Other Gain Controls

OP_656_RANGE, IO, Address 0x02[2]

A control to set the output range of the digital data. It also automatically the data saturator setting.

Function

OP_656_RANGE	Description
0 (default)	Enables full output range (0 to 255)
1	Enables limited output range (16 to 235)

Table 49. OP_656_RANGE Description for HDMI Receiver Input Mode

Input Range	OP_656_RANGE	Gain
0 to 255	0 (0 to 255 output)	1
	1 (16 to 235 RGB output, 16 to 240 CrCb output)	(235 − 16)/255 = 0.859
16 to 235	0 (0 to 255 output)	255/(235 − 16) = 1.164
	1 (16 to 235 RGB output, 16 to 240 CrCb output)	1

Table 50. OP_656_RANGE Description for Analog Front-End Input Mode

OP_656_RANGE	Gain
0 (0 to 255 output)	(255 − 0 + 1) × 16/1792 = 2.29
1 (16 to 235 RGB output, 16 to 240 CrCb output)	(235 − 16 + 1) × 16/1792 = 1.96

ALT_DATA_SAT, IO, Address 0x02[0]

A control to disable the data saturator that limits the output range independently of OP_656_RANGE. This bit is used to support extended data range modes.

Function

ALT_DATA_SAT	Description
0 (default)	Data saturator enabled or disabled according to OP_656_RANGE setting
1	Reverses OP_656_RANGE decision to enable or disable the data saturator

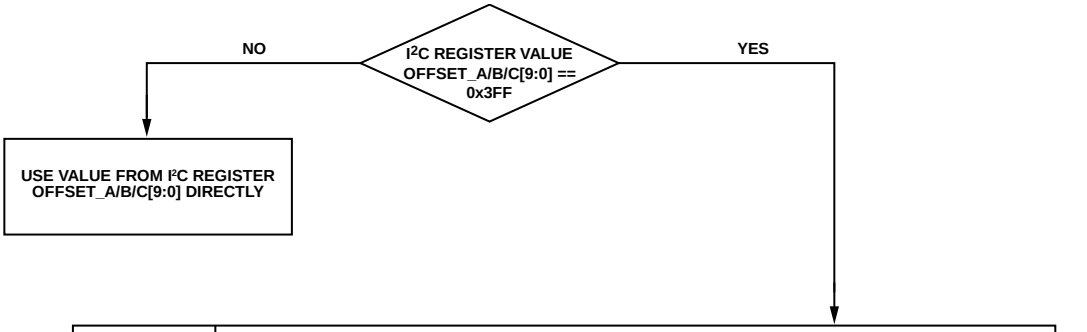
CP OFFSET BLOCK

The offset block consists of three independent adders, one for each channel. Using the A_OFFSET, B_OFFSET, and C_OFFSET registers, a fixed offset value can be added to the data. The actual offset used can come from two different sources:

The ADV7619 includes an automatic selection of the offset value, dependent on the CSC mode that is programmed by the user. The **RGB_OUT** and **OP_656_RANGE** bits are used to derive offset values.

A manual, user defined value can be programmed.

When the offset registers (A_OFFSET, B_OFFSET, and C_OFFSET) contain the value 0x3FF (reset default), the offset used is determined using the automatic selection process. For any other value in the offset registers, the automatic selection is disabled and the user-programmed offset value is applied directly to the video. Refer to the flowchart in Figure 42.



CHANNEL	OFFSET			
	RGB_OUT = 1		RGB_OUT = 0	
	OP_656_RANGE = 1	OP_656_RANGE = 0	OP_656_RANGE = 1	OP_656_RANGE = 0
A	64dec	0dec	64dec	0dec
B	64dec	0dec	512dec	512dec
C	64dec	0dec	512dec	512dec

09581-042

Figure 42. Channel A, Channel B, and Channel C Automatic Value Selection

For RGB type output data, the three offset values should be programmed to 0 or 64 (desired code output for black video). For YPbPr type output data, A_OFFSET[9:0] should be set to 64 (desired code for black); B_OFFSET[9:0] and C_OFFSET[9:0] (for Pr and Pb) are typically set to 512 (midrange).

Notes

- Adding an excessive offset onto the data will result in clipping of the signal.
- The offset value can only be positive; it is an unsigned number.
- ADV7619 employs sequencers for the offset values that prohibit intermediate wrong values to be applied.
- The I²C sequencer treats the three offset values as separate entities. To update all three offset values, a single sweep of I²C writes to the CP map, Register 0x77, Register 0x78, Register 0x79, and Register 0x7A is sufficient.

A_OFFSET[9:0], Addr 44 (CP), Address 0x77[5:0]; Address 0x78[7:4]

A control to set the manual offset for Channel A.

This field stores an unsigned value. To change A_OFFSET[9:0], Register Address 0x77 and Register Address 0x78 must be written to in this order with no I²C access in between.

Function

A_OFFSET[9:0]	Description
0x3FF (default)	Auto offset to Channel A
Any other value	Channel A offset

Note that to change the A_OFFSET[9:0] value, Register 0x77 and Register 0x78 must be written to in this order with no other I²C access in between.

B_OFFSET[9:0], Addr 44 (CP), Address 0x78[3:0]; Address 0x79[7:2]

A control to set the manual offset for Channel B.

This field stores an unsigned value. To change B_OFFSET[9:0], Register Addresses 0x78 and Register Address 0x79 must be written to in this order with no I²C access in between.

Function

B_OFFSET[9:0]	Description
0x3FF (default)	Auto offset to Channel B
Any other value	Channel B offset

Note: To change the A_OFFSET[9:0] value, register 0x77 and 0x78 must be written to in this order with no other I²C access in between.

C_OFFSET[9:0], Addr 44 (CP), Address 0x79[1:0]; Address 0x7A[7:0]

A control to set the manual offset for Channel C.

This field stores an unsigned value. To change C_OFFSET[9:0], Register Address 0x79 and Register Address 0x7A must be written to in this order with no I^2C access in between.

Function

C_OFFSET[9:0]	Description
0x3FF (default)	Auto offset to Channel C
Any other value	Channel C offset

Note: To change the A_OFFSET[9:0] value, Register 0x77 and Register 0x78 must be written to in this order with no other I^2C access in between.

AV CODE BLOCK

The AV code block is used to insert AV codes into the video data stream. The codes follow the standards outlined in ITU-R BT.656-4.

The following functions are supported by this block:

- AV code insertion can be enabled or disabled.
- Data between the end of active video (EAV) and the start of active video (SAV) can be blanked, for example, overwritten with default values. This function can be enabled or disabled. In addition, the default blanking value can be set for RGB or YPbPr.
- AV codes can be output on all channels or spread across the Y and PrPb buses for 20-bit output modes.
- F and V bits within the codes can be inserted directly or can be inverted before insertion.
- The position of the codes within the data stream (timing of the insertion) can be set to a default or can be slaved off the signal from the selected HS input pin.

The insertion point for the AV codes is predetermined by default and is adjusted automatically to suit the current video standard as per the **PRIM_MODE[3:0]** and **VID_STD[5:0]** settings. To cater for nonstandard signals, however, the AV code insertion point can also be taken off the HSync signal before it goes to the selected HS input pin. This gives the user great flexibility since the HSync signal position can be programmed to quite a wide range with LLC accuracy.

AVCODE_INSERT_EN, IO, Address 0x05[2]

A control to select AV code insertion into the data stream.

Function

AVCODE_INSERT_EN	Description
0	Does not insert AV codes into data stream
1 (default)	Inserts AV codes into data stream

AV_POS_SEL, Addr 44 (CP), Address 0x7B[2]

A control to select AV codes position.

Function

AV_POS_SEL	Description
0	SAV code at HS falling edge and EAV code at HS rising edge
1 (default)	Uses predetermined (default) positions for AV codes

AV_INV_V, Addr 44 (CP), Address 0x7B[6]

A control to invert V bit in AV codes.

Function

AV_INV_V	Description
0 (default)	Do not invert V bit polarity before inserting it into the AV code
1	Invert V bit polarity before inserting it into the AV code

AV_INV_F, Addr 44 (CP), Address 0x7B[7]

A control to invert the F bit in the AV codes.

Function

AV_INV_F	Description
0 (default)	Inserts the F bit with default polarity
1	Inverts the F bit before inserting it into the AV code

DATA_BLANK_EN, IO, Address 0x05[3]

A control to blank data during video blanking sections.

Function

DATA_BLANK_EN	Description
0	Do not blank data during horizontal and vertical blanking periods
1 (default)	Blank data during horizontal and vertical blanking periods

DE_WITH_AVCODE, Addr 44 (CP), Address 0x7B[0]

A control to insert AV codes in relation to the DE output signal.

Function

DE_WITH_AVCODE	Description
0	AV codes locked to default values. DE position can be moved independently of AV codes.
1 (default)	Inserted AV codes moves in relation to DE position change.

REPL_AV_CODE, IO, Address 0x05[1]

A control to select the duplication of the AV codes and insertion on all data channels of the output data stream.

Function

REPL_AV_CODE	Description
0 (default)	Outputs complete SAV/EAV codes on all channels, Channel A, Channel B, and Channel C.
1	Spreads AV code across the three channels. Channel B and Channel C contain the first two ten bit words, 0x3FF and 0x000. Channel A contains the final two 10-bit words 0x00 and 0xXYZ.

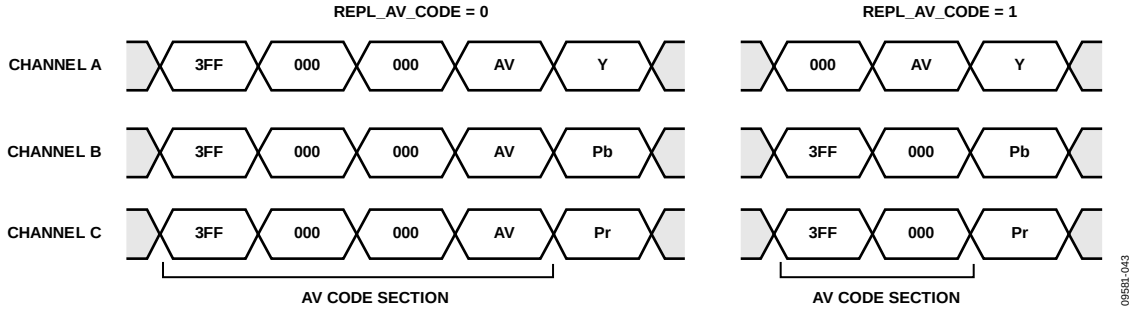


Figure 43. AV Code Output Options (CP)

SWAP_SPLIT_AV, Addr 44 (CP), Address 0xC9[2]

A control to swap the luma and chroma AV codes in DDR modes.

Function

SWAP_SPLIT_AV	Description
0	Swap the luma and chroma AV codes in DDR mode.
1 (default)	Do not swap the luma and chroma AV codes in DDR mode.

CP DATA PATH FOR HDMI MODES

Figure 44 and Figure 45 depict the data path of the video for HDMI mode. These figures depict the gains and offsets applied when using the automatic control, **OP_656_RANGE**, and the manual options for setting the clamp level, gain, and offset.

The I²C settings are detailed in Table 51 for use when processing extended range video signals with blacker than black and/or whiter than white video levels.

Table 51. Settings Required to Support Extended Range Video Input

I²C Setting/Mode	Analog Modes	HDMI Mode YUV	HDMI Mode RGB [0 to 255]	HDMI Mode RGB [16 to 235]
OP_656_RANGE	1	1	0	1
ALT_DATA_SAT	1	1	0	1

Pregain Block

To compensate for signal attenuation in the analog front end of the ADV7619 and input buffer gain, a pregain block is provided in the CP path. The pregain block is controlled by **CP_MODE_GAIN_ADJ[7:0]**, which represents an unsigned value in a 1.7 binary format. The range of **CP_MODE_GAIN_ADJ[7:0]** is 0 to 1.99.

The MSB of **CP_MODE_GAIN_ADJ[7:0]** represents the integer part of the pregain value while the 7 LSBs represents the fractional part of the pregain value.

CP_MODE_GAIN_ADJ[7:0], Addr 44 (CP), Address 0x40[7:0]

Pregain adjustment to compensate for the gain of the analog front end. This register stores a value in a 1.7 binary format.

Function

CP_MODE_GAIN_ADJ[7:0]	Description
0xxxxxxx	Gain of (0 + (xxxxxxx/128))
10000000	Default pregain (pregain of 1.0)
1xxxxxxx	Gain of (1 + (xxxxxxx/128))

CP_MODE_GAIN_ADJ_EN, Addr 44 (CP), Address 0x3E[2]

A control to enable pregain.

Function

CP_MODE_GAIN_ADJ_EN	Description
0 (default)	The pregain block is bypassed.
1	The pregain block is enabled.

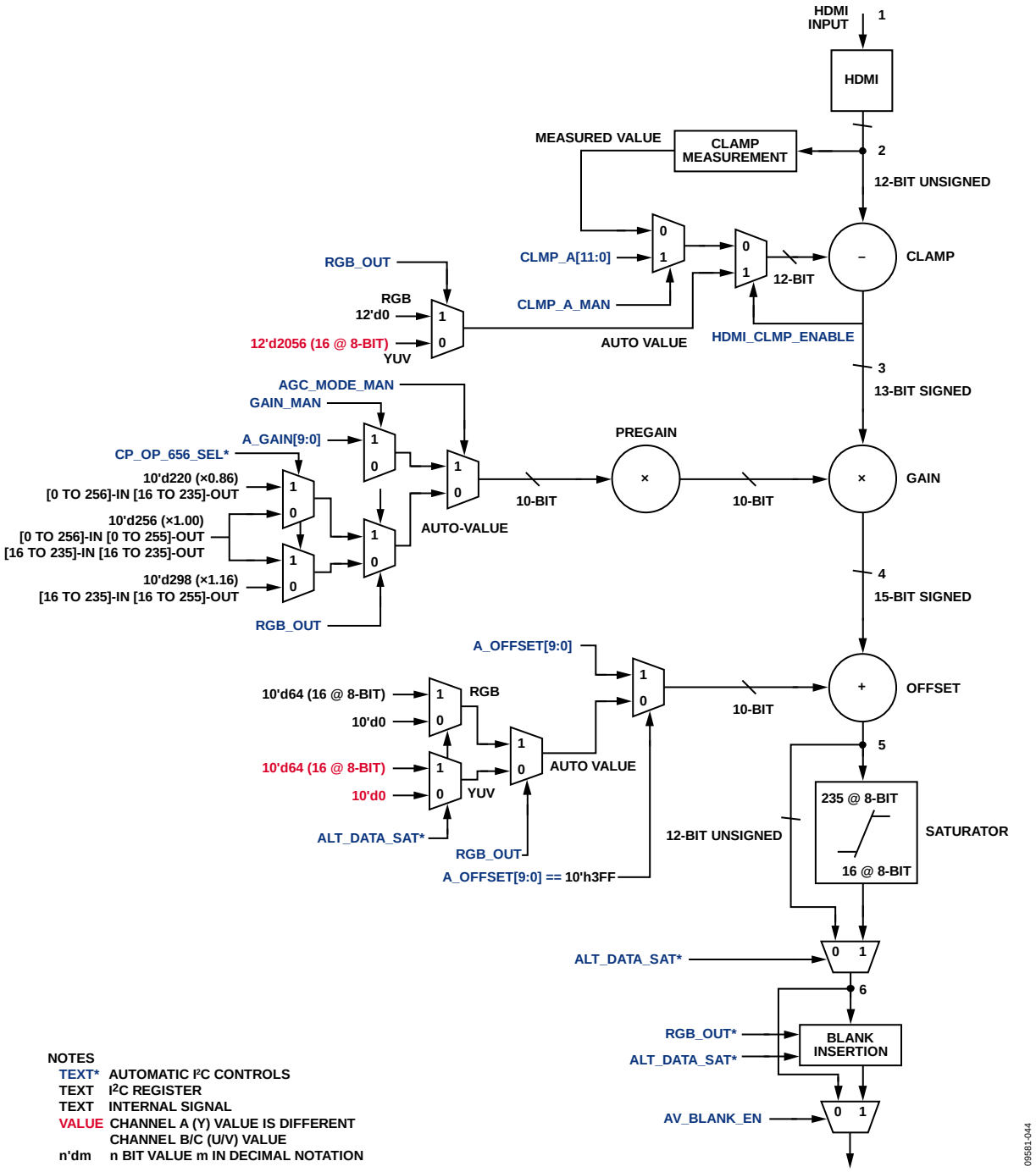


Figure 44. CP Data Path Channel A (Y) for HDMI Mode

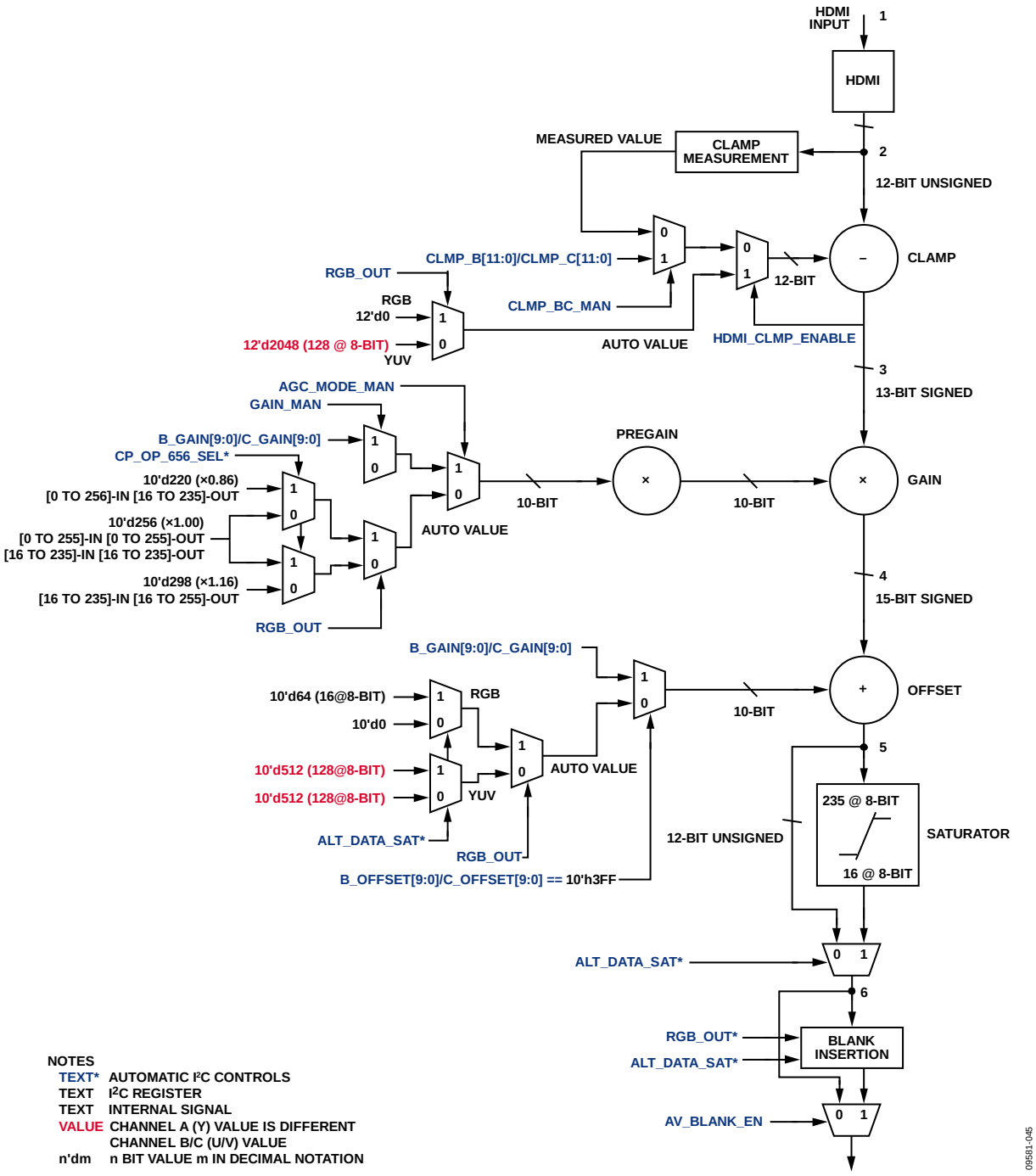


Figure 45. CP Data Paths Channel B and Channel C for HDMI Mode

SYNC PROCESSED BY CP SECTION

The CP Core uses the HDMI section as its source of HSync, VSync and DE.

Sync Routing from HDMI Section

The CP section receives syncs from the HDMI section, as shown in Figure 46.

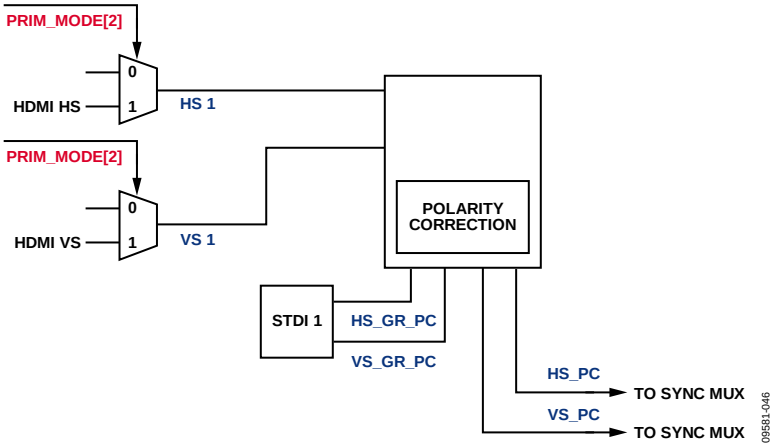


Figure 46. External/HDMI Syncs Routing to CP Section

Signals Routing to Synchronization Channels

The ADV7619 has one synchronization channel consisting of one STDI section. When an HDMI input is applied, the HDMI core will generate HSync, VSync, and DE signals and supply them as input to the each synchronization channel shown in Figure 46. HSync from the HDMI block is denoted as HDMI_HS, and VSync from the HDMI block is denoted as HDMI_VS. DE from the HDMI block is not shown in Figure 46 as it is passed directly to the CP core without any processing when an HDMI input is selected.

Standard Detection and Identification

As shown in Figure 46, the synchronization channel also contains standard detection and identification (STDI) block. These monitor the synchronization signals to determine the video input standard.

The STDI blocks perform four key measurements:

- Block Length CH1_BL[13:0]
  This is the number of 28.6363 MHz clock cycles (XTAL frequency) in a block of eight lines. From this, the time duration of one line can be concluded.
- Line count in Field CH1_LCF[10:0]
  The CH1_LCF[10:0] readback value is the number of lines between two VSyncs, that is, over one field measured by channel.
- Line count in VSYNC CH1_LCVS[4:0]
  The LCVS[4:0] readback value is the number of lines within one VSync period.
- Field Length CH1_FCL[12:0]
  This is the number of 28.6363 MHz clock cycles in a 1/256th of a field. Alternately, this value of FCL multiplied by 256 gives one field length count in 28.6363 MHz (XTAL) clocks.

By interpreting these four parameters, it is possible to distinguish between the different types of input signals.

In ADV7619, there are three operational modes for the STDI block:

- Continuous mode:
  The STDI block performs continuous measurements on lock/unlock bases and updates the corresponding I²C registers based on the lock status bit (STDI_DVALID).
- Real-time continuous mode:
  The STDI block performs continuous measurement regardless of the lock/unlock bases and always updates real-time measurement data to the corresponding I²C registers.
- Single shot mode:
  The STDI block waits for a trigger (0 to 1 transition on CH1_TRIG_STDI) to start the measurements. Single shot mode can be useful in complex systems where the scheduling of functions is important.

A data valid flag, CH1_STDI_DVALID, is provided, which is based on the status of the horizontal/vertical lock of the block and is held low during the measurements. The four parameters should only be read after the CH1_STDI_DVALID flag has gone high for the continuous/single shot mode. In real-time continuous mode, the ADV7619 allows the user to monitor the real-time timing measurement regardless of the CH1_STDI_DVALID flag. Refer to the STDI Readback Values section for information on the readback values.

Notes

- Synchronization type pulses include horizontal synchronization, equalization and serration pulses.
- The CH1_TRIG_STDI flag is not self-clearing. The measurements are only started upon setting the CH1_TRIG_STDI flag. This means that after setting it, it must be cleared again by writing a 0 to it. This second write (to clear the flag) can be done at any time and does not have any effect on running measurements. It also does not invalidate previous measurement results.
- The ADV7619 only measures those parameters, but does not take any action based upon them. The part does not reconfigure itself. To avoid unforeseen problems in the scheduling of a system controller, the part merely helps to identify the input.
- Since real-time continuous mode provides the capability to monitor the real-time measurement data regardless of the block lock status, the user should be aware that the timing readback values may not be a valid readback measurement in this mode.

CH1_STDI_CONT, Addr 44 (CP), Address 0x86[1]

A control to set the synchronization source polarity detection mode for Sync Channel 1 STDI.

Function

CH1_STDI_CONT	Description
0	Sync Channel 1 STDI works in one-shot mode (triggered by a 0 to 1 transition on the CH1_TRIG_STDI bit)
1 (default)	Sync Channel 1 STDI works in continuous mode

BYPASS_STDI1_LOCKING, Addr 44 (CP), Address 0xF5[1]

Bypass STDI locking for Sync Channel 1.

Function

BYPASS_STDI1_LOCKING	Description
0 (default)	Update CH1_BL, CH1_LCF and CH1_LCVS only the sync Channel 1 STDI locks and CH1_STDI_DVALID is set to 1
1	Update CH1_BL, CH1_LCF,CH1_LCVS from the sync Channel 1 STDI as they are measured

CH1_TRIG_STDI, Addr 44 (CP), Address 0x86[2]

Trigger synchronization source and polarity detector for Sync Channel 1 STDI. A 0-to-1 transition in this bit restarts the auto-sync detection algorithm. This is not a self-clearing bit and must be set to 0 to prepare for next trigger.

Function

CH1_TRIG_STDI	Description
0 (default)	Default value—transition 0 to 1 restarts auto-sync detection algorithm
1	Transition 0 to 1 restarts auto-sync detection algorithm

CH1_STDI_DVALID, Addr 44 (CP), Address 0xB1[7] (Read Only)

This bit is set when the measurements performed by Sync Channel 1 STDI are completed. High level signals validity for CH1_BL, CH1_LCF, CH1_LCVS, CH1_FCL, and CH1_STDI_INTLCD parameters. To prevent false readouts, especially during signal acquisition, CH1_SDTI_DVALID only goes high after four fields with same length are recorded. As a result, STDI measurements can take up to five fields to finish.

Function

CH1_STDI_DVALID	Description
0 (default)	Sync Channel 1 STDI measurements are not valid.
1	Sync Channel 1 STDI measurements are valid.

CP_STDI_INTERLACED, IO, Address 0x12[4] (Read Only)

A readback to indicate the interlaced status of the currently selected STDI block applied to the CP core.

Function

CP_STDI_INTERLACED	Description
0 (default)	Selected STDI has detected a progressive input.
1	Selected STDI has detected a interlaced input.

CP_INTERLACED, IO, Address 0x12[3] (Read Only)

A readback to indicate the interlaced status of the CP core based on configuration of video standard and INTERLACED bit in the CP map.

Function

CP_INTERLACED	Description
0 (default)	CP core is processing the input as a progressive input.
1	CP core is processing the input as a interlaced input.

CP_PROG_PARM_FOR_INT, IO, Address 0x12[2] (Read Only)

A readback to indicate if the CP core is processing for progressive standard while the vdeo standard and the INTERLACED bit in the CP map are configured for an interlaced standard.

Function

CP_PROG_PARM_FOR_INT	Description
0 (default)	CP core processing for a progressive standard while video standard and the INTERLACED bits are configured for an interlaced standard
1	CP core processing for a progressive standard while video standard and the INTERLACED bits+ are configured for a progressive standard

CP_FORCE_INTERLACED, IO, Address 0x12[1] (Read Only)

A readback to indicate forced-interlaced status of the CP core based on configuration of video standard and INTERLACED bit in the CP map.

Function

CP_FORCE_INTERLACED	Description
0 (default)	Input is detected as interlaced and the CP is programmed in an interlaced mode via VID_STD[5:0].
1	Input is detected as progressive and the CP is programmed in an interlaced mode.

Detailed Mechanism of STDI Block Horizontal/Vertical Lock Mechanism

STDI Horizontal Locking Operation

For the STDI horizontal locking operation, the STDI block compares adjacent line length differences (in XTAL clock cycles) with the programmed threshold. If 128 consecutive adjacent lines lengths are within the threshold, the STDI horizontally locks to the incoming video.

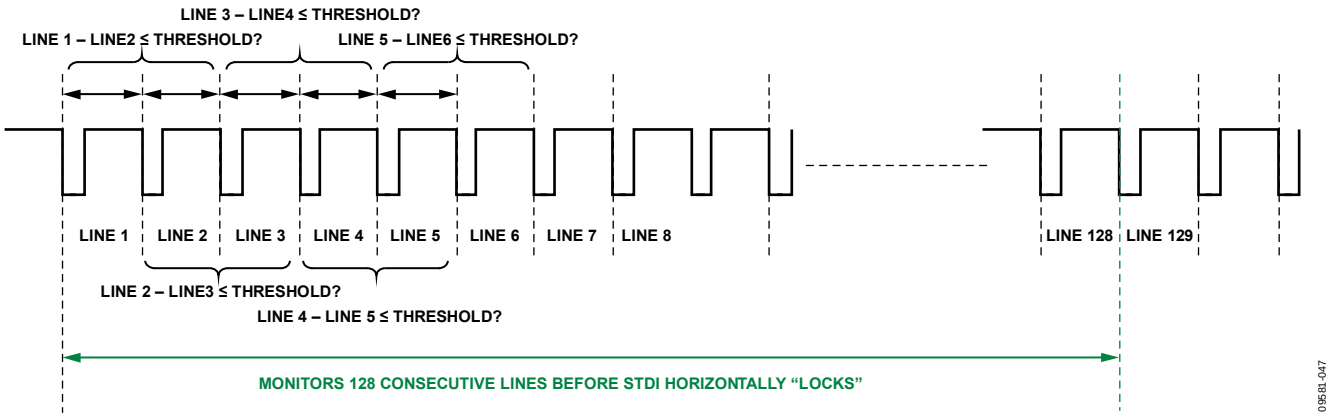


Figure 47. STDI Horizontal Locking Operation

Once the STDI locks to the incoming video, it registers the first BL measurement (first eight lines) as latched data (absolute line length: L) and keeps monitoring and comparing each successive line length with the absolute line length (L/8).

The STDI horizontally unlocks if 128 consecutive lines have a line length greater than the threshold.

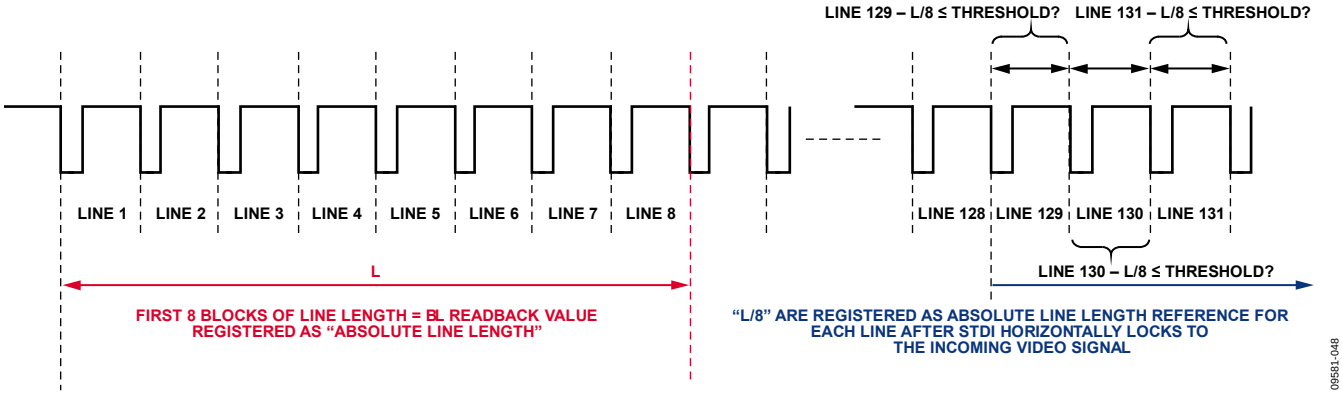


Figure 48. STDI HSync Monitoring Operation

STDI Vertical Locking

The STDI block compares adjacent field length differences and VSync lengths in line counts and compares them with a threshold. If four consecutive adjacent field lengths (LCF) and line counts in VSync (LCVS) are within the threshold, the STDI locks vertically to the incoming video.

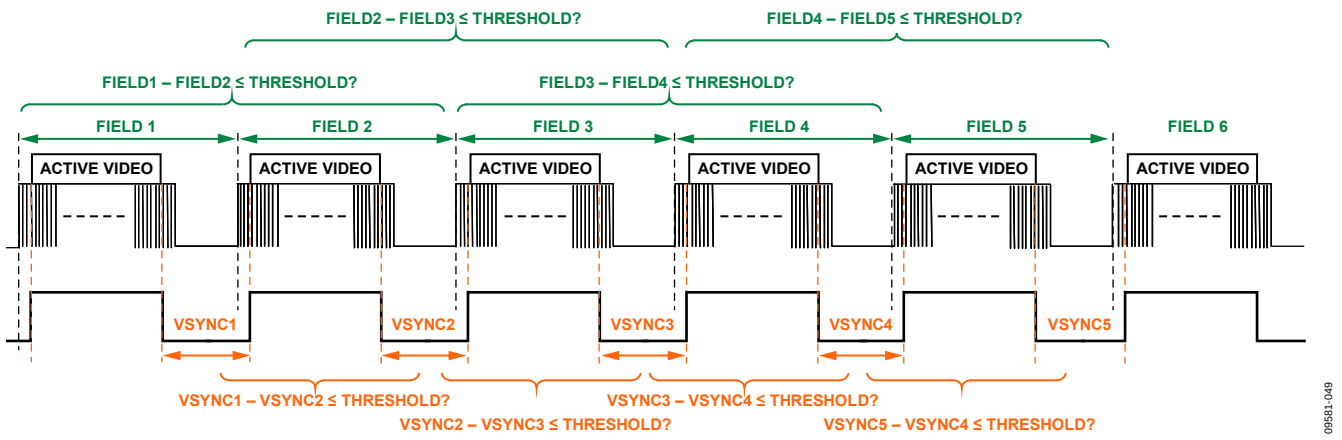


Figure 49. STDI Vertical Locking Operation

Once the STDI locks to the incoming video, the STDI registers the latest field length/VSync length as latched data (absolute field length: F, absolute VSync length: V). The STDI keeps monitoring and comparing FIELD/VSync lengths with the respective absolute length (F, V) once vertically locked. The STDI vertically unlocks if four consecutive FIELD or VSync lengths are greater than the respective threshold.

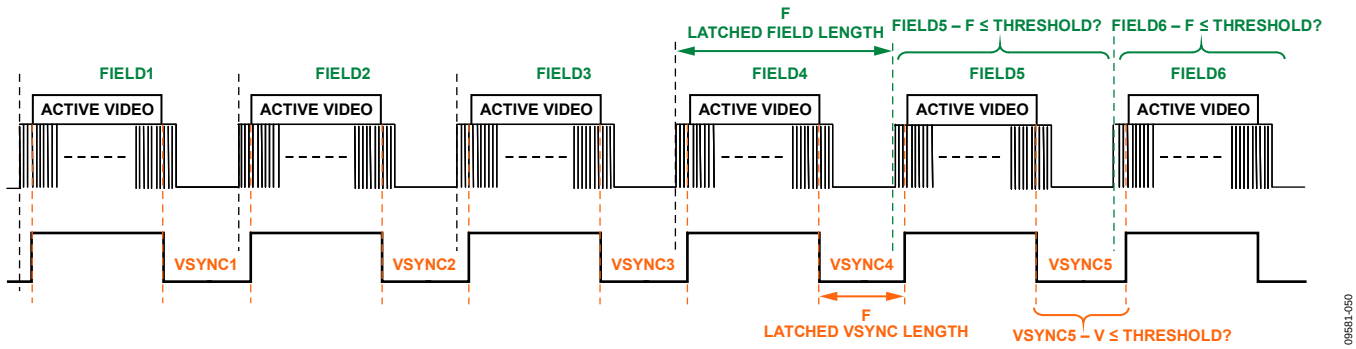


Figure 50. STDI VSync Monitoring Operation

CH1_BL[13:0], Addr 44 (CP), Address 0xB1[5:0]; Address 0xB2[7:0] (Read Only)

A readback for the block length for Sync Channel 1. Number of crystal cycle cycles in a block of eight lines of incoming video. This readback is valid if CH1_STDI_DVALID is high.

Function

CH1_BL[13:0]	Description
xxxxxxxxxxxxx	Readback value

CH1_LCVS[4:0], Addr 44 (CP), Address 0xB3[7:3] (Read Only)

A readback for the Sync Channel 1 line count in a VSync.

Number of lines in a VSync period measured on Sync Channel 1. The readback from this field is valid if CH1_STDI_DVALID is high.

Function

CH1_LCVS[4:0]	Description
xxxxx	Readback value

CH1_LCF[11:0], Addr 44 (CP), Address 0xA3[3:0]; Address 0xA4[7:0] (Read Only)

A readback for the Sync Channel 1 line count in a field.

Number of lines between two VSyncs measured on Sync Channel 1. The readback from this field is valid if CH1_STDI_DVALID is high.

Function

CH1_LCF[11:0]	Description
xxxxxxxxxxx	Readback value

CH1_FCL[12:0], Addr 44 (CP), Address 0xB8[4:0]; Address 0xB9[7:0] (Read Only)

A readback for the Sync Channel 1 field count length.

Number of crystal clock cycles between successive VSyncs measured by Sync Channel 1 STDI or in 1/256th of a field. The readback from this field is valid if CH1_STDI_DVALID is high.

Function

CH1_FCL[12:0]	Description
xxxxxxxxxxxxx	Readback value

CH1_STDI_INTLCD, Addr 44 (CP), Address 0xB1[6] (Read Only)

Interlaced vs. progressive mode detected by Sync Channel 1 STDI. The readback from this register is valid if CH1_STDI_DVALID is high.

Function

CH1_STDI_INTLCD	Description
0 (default)	Indicates a video signal on Sync Channel 1 with noninterlaced timing
1	Indicates a signal on Sync Channel 1 with interlaced timing

STDI Usage

Figure 51 shows a flowchart of the intended usage of the STDI block.

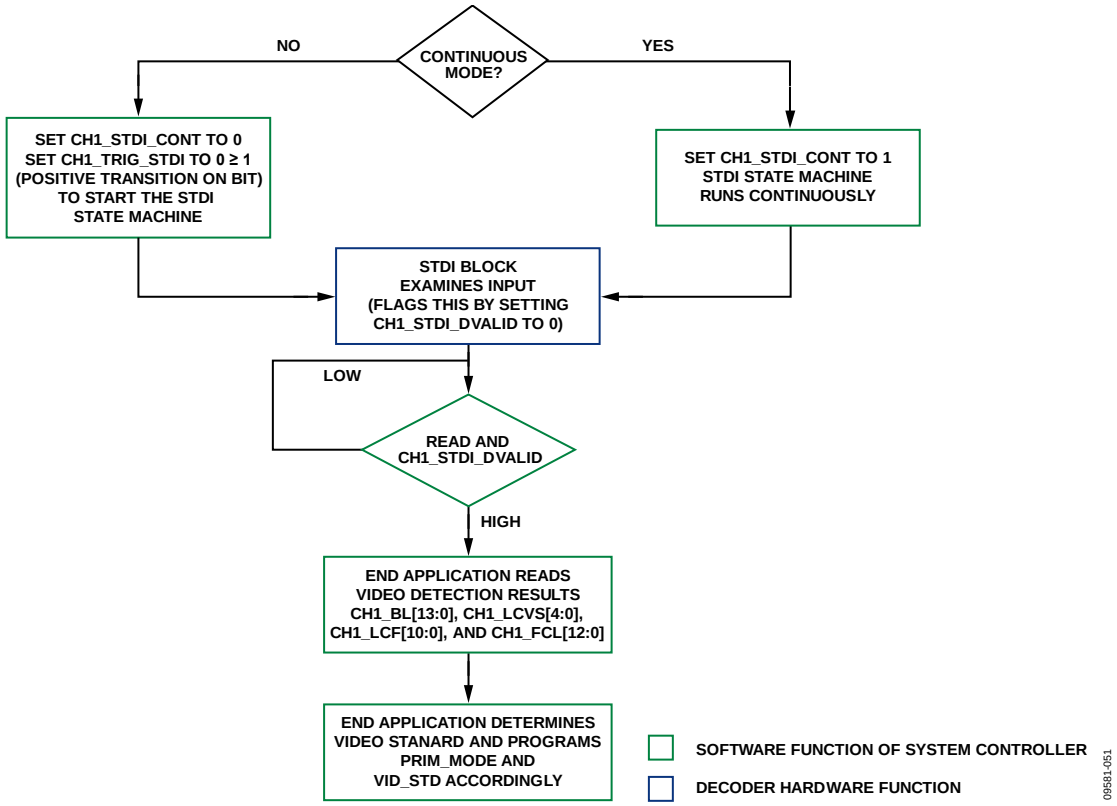


Figure 51. STDI Usage Flowchart

STDI Readback Values

Table 52. STDI Readback Values for SD, PR, and HD

Standard	CHx_BL[13:0] 28.63636 MHz XTAL	CHx_LCF[10:0]	CHx_LCVS[4:0]	FCL[12:0] 28.63636 MHz XTAL
720p SMPTE 296M	5091	750	4 to 5	1868
1125i SMPTE 274M	6788	562 to 563	4 to 5	1868
525p BT 1358	7270	525	5 to 6	1868
625p BT 1358	7331	625	4 to 5	2237
1250i BT 709/SMPTE 295	7331	625	1	4474
1125i SMPTE 274M 6	8145	562 to 563	4 to 5	1868
1125p SMPTE 274M 10	848	1125	4 to 5	1868
525i	14560	262 to 263	3	1868
625i	14662	312 to 313	2 to 3	2237

Note: To obtain the expected values of BL or FL at any other XTAL frequency, use the formula in Equation 9, computation of expected BL and FCL for XTAL in use.

$$BL_{XTAL\_F1\_MHz} = BL_{28.63636MHz\_XTAL} \times XTAL\_FREQ/28.6363 \quad (9)$$

where *XTAL_FREQ* is the clock frequency of the XTAL used.

Example: For SD525i at 24.576 MHz XTAL:

$BL = 14585 \times 24.576/28.6363 \approx 12{,}517$

$FL = 1868 \times 24.576/28.6363 \approx 1603$

The values of LCF and LCVS do not change with the XTAL frequency.

STDI Readback Values for GR

Table 53. STDI Results for Graphics Standards

Standard	CHx_BL[13:0] 28.63636 MHz XTAL	CHx_LCF[10:0]	CHx_LCVS[4:0]	FCL[12:0] 28.63636 MHz XTAL
XGA 85	3327	805 to 808	0 to 3	1316
SXGA 60	3571	1063 to 1066	0 to 3	1868
XGA 75	3808	797 to 800	0 to 3	1493
XGA 70	4048	800 to 806	0 to 6	1598
SVGA 85	4259	628 to 631	0 to 3	1316
XGA 60	4726	800 to 806	0 to 6	1868
SVGA 72	4756	660 to 666	0 to 6	1554
SVGA 75	4878	622 to 625	0 to 3	1493
VGA 85	5286	506 to 509	0 to 3	1316
VGA 72	6042	517 to 520	0 to 3	1554
SVGA 60	6039	624 to 628	0 to 4	1868
VGA 75	6098	497 to 500	0 to 3	1493
SVGA 56	6508	623 to 625	0 to 2	1997
VGA 60	7272	523 to 525	0 to 2	1868

Note: To obtain the expected values of BL or FCL at any other XTAL frequency, use the formula shown in Equation 9.

Example: For XGA75 at 24.576 MHz XTAL:

$BL = 3824 \times 24.576/28.63636 \approx 3282$

$FCL = 1493 \times 24.576/28.63636 \approx 1281$

Figure 52 shows the parameters from Table 53 plotted against each other at the recommended 28.63636 MHz XTAL operation.

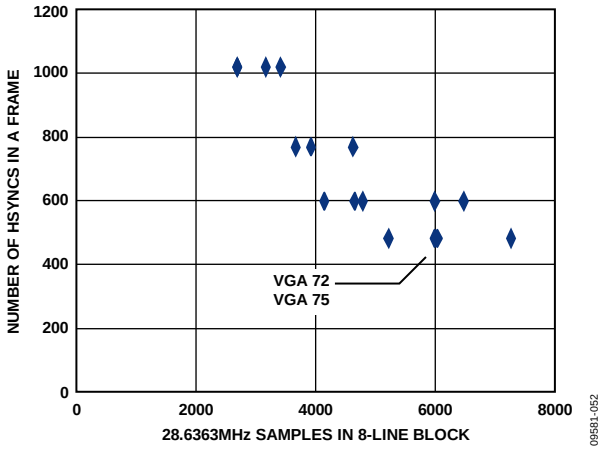


Figure 52. STDI Values for GR Mode (Plot)

Note: Although the two points for VGA72 and VGA75 look very close, it is anticipated that the difference in the parameters is sufficient to distinguish between them.

CP OUTPUT SYNCHRONIZATION SIGNAL POSITIONING

The ADV7619 overall synchronization processing flow is shown in the block diagram in Figure 53. The user can reposition the synchronization signal output from the regenerated input synchronization signal within the CP block with the control bits marked in red in Figure 15.

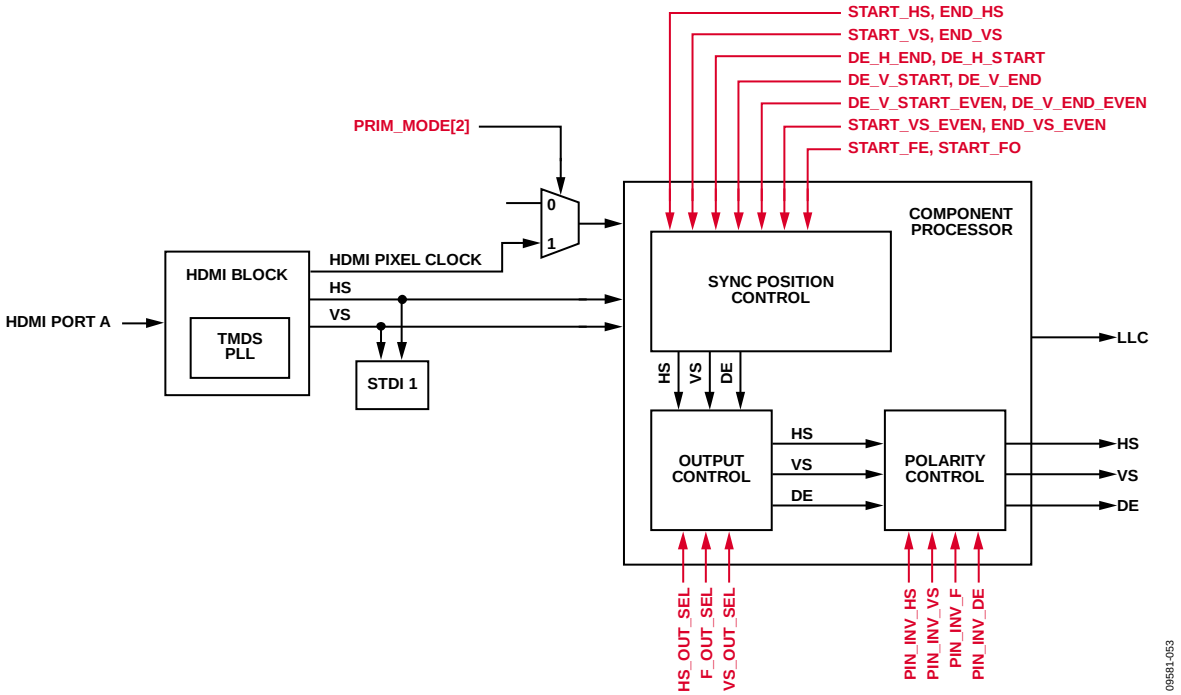


Figure 53. ADV7619 Simplified Synchronization Signal Processing Flow Diagram

As shown in Figure 53, the ADV7619 CP can output the following three primary and one secondary synchronization signals, which are controlled by the output control block in the CP block.

Primary:

- Horizontal synchronization timing reference output on the HS pin
- Vertical synchronization timing reference output on the VS/FIELD/ALSB pin
- DE (indicates active region) shared with the FIELD pin

Secondary:

- Field timing reference output on the DE pin or as a secondary signal on the VS/FIELD/ALSB pin

Timing reference signals with shared pins are controlled via I²C.

Table 54. CP Synchronization Signal Output Pins

Pin Name	Primary Signal (Default)	Secondary Signal	Controlled by I²C Bit
DE	DE out	FIELD out	**F_OUT_SEL**
VS/FIELD/ALSB	VS out	FIELD out	**VS_OUT_SEL**

The user can program the primary and secondary synchronization signals, repositioning them in order to control the display area, as shown in Figure 54.

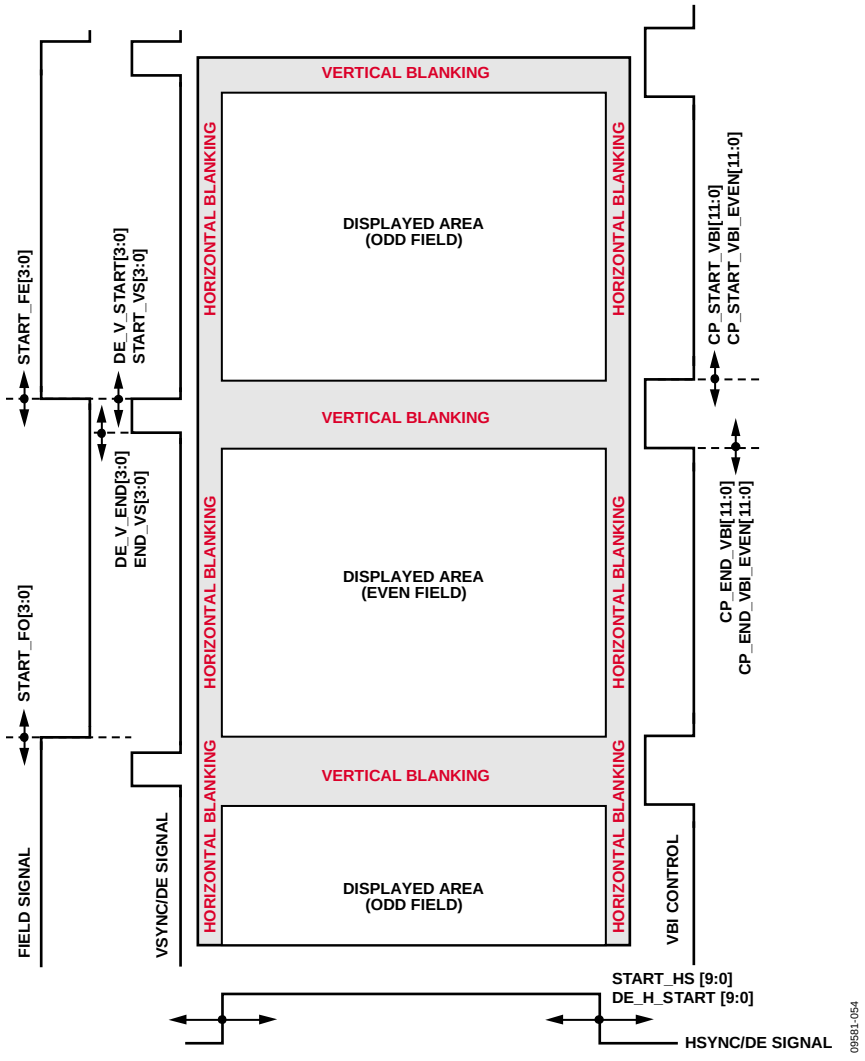


Figure 54. Synchronization Repositioning and Displayed Area

CP Synchronization Signals

The three primary synchronization signals have certain default positions, depending on the video standard in use.

To allow for a glueless interface to downstream ICs, there is the facility to adjust the position of edges on the three primary synchronization signals Figure 55, Figure 56, Figure 57, Figure 58, Figure 59, Figure 60, Figure 61, Figure 62, show the nominal position of HS, VS, and FIELD. The positions of those signals can be adjusted in both directions by using the following controls:

- **START_HS[9:0]**
- **END_HS[9:0]**
- **START_VS[3:0]**
- **END_VS[3:0]**
- **START_VS_EVEN[3:0]**
- **START_FE[3:0]**
- **START_FO[3:0]**

All seven above parameters are given as signed values. This means that rather than adjusting the absolute position of a signal, these adjustments allow the user to advance (negative value) or delay (positive value) the respective timing reference signals.

In addition, the polarity of the synchronization output signals can be inverted by using:

- **INV_HS_POL**
- **INV_F_POL**
- **INV_VS_POL**

HSync Timing Controls

Programming the registers listed in this section, the HS signal as shown in Figure 55 can be adjusted in the described manner.

Table 55. HS Default Timing

Symbol	Characteristic	Note	525i	625i	525p	625p	720p	1080i	1080p
a	HS to start of active video	Default	118	128	116	126	256	188	118
			All values are for 1× outputs						
d	HS width	Default	64	64	64	64	40	44	44
b	Active video samples		720	720	720	720	1280	1920	1920
c	Total samples/line		858	864	858	864	1650	2200/2376	2200

Table 56. HS Default Timing (Continued, 1)

Symbol	Characteristic	Note	680 × 480 at 60 Hz	640 × 480 at 72 Hz	640 × 480 at 75 Hz	640 × 480 at 85 Hz
a	HS to start of active video	Default	140	164	180	132
			All values are for 1× outputs			
d	HS width	Default	96	40	64	56
b	Active video samples		640	640	640	640
c	Total samples/line		800	832	840	832

Table 57. HS Default Timing (Continued, 2)

Symbol	Characteristic	Note	800 × 600 at 56 Hz	800 × 600 at 60 Hz	800 × 600 at 72 Hz	800 × 600 at 75 Hz	800 × 600 at 85 Hz
a	HS to start of active video	Default	196	212	180	236	212
			All values are for 1× outputs				
d	HS width	Default	72	128	120	80	64
b	Active video samples		800	800	800	800	800
c	Total samples/line		1024	1056	1040	1056	1048

Table 58. HS Default Timing (Continued, 3)

Symbol	Characteristic	Note	1024 × 768 at 60 Hz	1024 × 768 at 70 Hz	1024 × 768 at 75 Hz	1024 × 768at 85 Hz
a	HS to start of active video	Default	292	276	268	300
			All values are for 1x outputs			
d	HS width	Default	136	136	96	96
b	Active video samples		1024	1024	1024	1024
c	Total samples/line		1344	1328	1312	1376

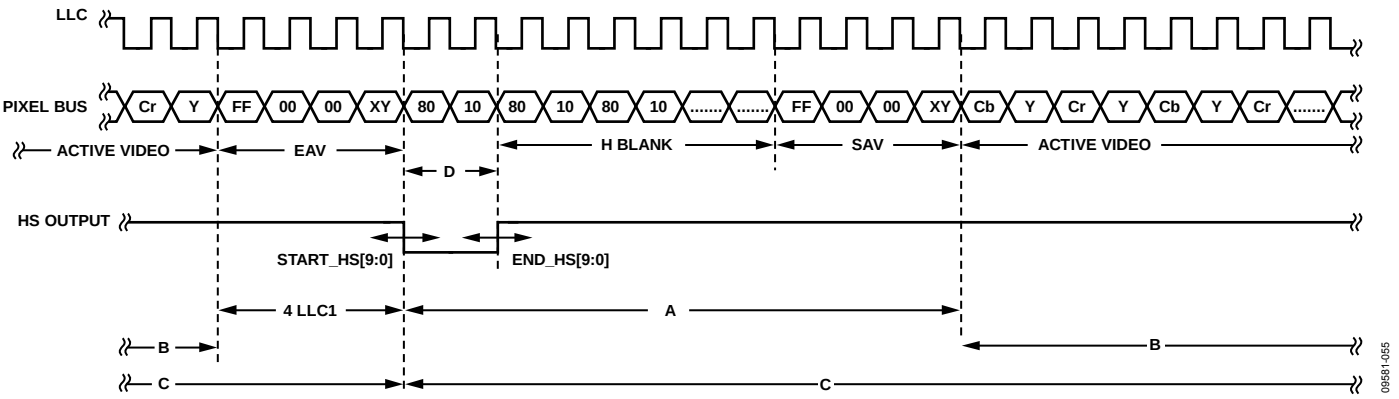


Figure 55. HS Timing

START_HS[9:0], Addr 44 (CP), Address 0x7C[3:2]; Address 0x7E[7:0]

A control to shift the position of the leading edge of the HSync output by the CP core.

This register stores a signed value in a twos complement format. START_HS[9:0] is the number of pixel clocks by which the leading edge of the HSync is shifted (for example, 0x3FF corresponds to a shift of one pixel clock away from the active video, 0x005 corresponds to a shift of five pixel clocks toward the active video).

Function

START_HS[9:0]	Description
0x000 (default)	Default value.
0x000 to 0x1FF	The leading edge of the HSync is shifted toward the active video.
0x200 to 0x3FF	The leading edge of the HSync is shifted away from the active video.

Table 59. Controlling the Beginning of the HS Timing Signal

START_HS[9:0]	Hex	Result	Note
0000000000 ↻	0x000	No move	Default
0000000001	0x001	$1 \times \frac{1}{LLC}$ sec shift later than default[1]	Minimum →
0100000000	0x100	$256 \times \frac{1}{LLC}$ sec shift later than default	
0111111111	0x1FF	$511 \times \frac{1}{LLC}$ sec shift later than default	Maximum →
1111111111	0x3FF	$1 \times \frac{1}{LLC}$ sec shift earlier than default[2]	Minimum ←
1011111111	0x3FE	$256 \times \frac{1}{LLC}$ sec shift earlier than default	
1000000000	0x200	$512 \times \frac{1}{LLC}$ sec shift earlier than default	Maximum ←

[1] HS START closer to active video.
[2] HS START away from active video.

END_HS[9:0], Addr 44 (CP), Address 0x7C[1:0]; Address 0x7D[7:0]

A control to shift the position of the trailing edge of the HSync output by the CP core.

This register stores a signed value in a twos complement format. HS_END[9:0] is the number of pixel clocks by which the leading edge of the HSync is shifted (for example, 0x3FF corresponds to a shift of one pixel clock away from the active video, 0x005 corresponds to a shift of five pixel clocks toward the active video).

Function

END_HS[9:0]	Description
0x000 (default)	Default value.
0x000 to 0x1FF	The trailing edge of the HSync is shifted toward the active video.
0x200 to 0x3FF	The trailing edge of the HSync is shifted away from the active video.

Table 60. Controlling the End of the HS Timing Signal

END_HS[9:0]	Hex	Result	Note
0000000000 ↻	0x000	No move (default)	
0000000001	0x001	$1 \times \frac{1}{LLC}$ sec shift later than default[1]	Minimum →
0100000000	0x100	$256 \times \frac{1}{LLC}$ sec shift later than default	
0111111111	0x1FF	$511 \times \frac{1}{LLC}$ sec shift later than default	Maximum →
1111111111	0x3FF	$1 \times \frac{1}{LLC}$ sec shift earlier than default[2]	Minimum ←
1011111111	0x3FE	$256 \times \frac{1}{LLC}$ sec shift earlier than default	
1000000000	0x200	$512 \times \frac{1}{LLC}$ sec shift earlier than default	Maximum ←

[1] Closer to active video.
[2] Away from active video.

EIA_861_COMPLIANCE, Addr 44 (CP), Address 0x69[2]

Control for compliance to 861B for 525p.This bit set the start of the VBI for the 525p standard only.

Function

EIA_861_COMPLIANCE	Description
0 (default)	The VBI region starts on Line 1.
1	The VBI region starts on Line 523. The start of the VBI region is compliant with the 861 specification.

VSync Timing Controls

This section describes the programming of the VS timing signals. The VS signal is shown in Figure 56, Figure 57, Figure 58, Figure 59, Figure 60, Figure 61, and Figure 62 and can be adjusted in the described manner.

Table 61. VS Default Timing

Characteristic	Units	Direction	525i	625i	525p	625p	720p	1080i
START_VS range maximum	Lines	→	7	7	7	7	7	7
START_VS range minimum	Lines	←	8	8	8	8	8	8
END_VS range maximum	Lines	→	7	7	7	7	7	7
END_VS range minimum	Lines	←	8	8	8	8	8	8

START_VS[3:0], Addr 44 (CP), Address 0x7F[7:4]

A control to shift the position of the leading edge of the VSync output by the CP core.

This register stores a signed value in a twos complement format. START_VS[3:0] is the number of lines by which the leading edge of the VSync is shifted (for example, 0x0F corresponds to a shift by 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video).

Function

START_VS[3:0]	Description
0x0 (default)	Default value.
0x0 to 0x7	The leading edge of the VSync is shifted toward the active video.
0x8 to 0xF	The leading edge of the VSync is shifted away from the active video.

Table 62. Controlling the Start of the VS Timing Signal

START_VS[3:0]	Hex	Result	Note
0000 (default)	0x0	No move (default)	
0001	0x1	1 HS shift later than default[1]	Minimum →
0011	0x3	3 HS shift later than default	
0111	0x0	7 HS shift later than default	Maximum →
1111	0xF	1 HS shift earlier than default[2]	Minimum ←
1101	0xD	3 HS shift earlier than default	
1000	0x8	8 HS shift earlier than default	Maximum ←

[1] VS closer to start of active video.
[2] VS away from start of active video.

END_VS[3:0], Addr 44 (CP), Address 0x7F[3:0]

A control to shift the position of the trailing edge of the VSync output by the CP core.

This register stores a signed value in a twos complement format. SEND_VS[3:0] is the number of lines by which the trailing edge of the VSync is shifted (for example, 0x0F corresponds to a shift of one line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video).

Function

END_VS[3:0]	Description
0x0 (default)	Default value.
0x0 to 0x7	The trailing edge of the VSync is shifted toward the active video.
0x8 to 0xF	The trailing edge of the VSync is shifted away from the active video.

Table 63. Controlling the End of the VS Timing Signal

END_VS[3:0]	Hex	Result	Note
0000 (default)	0x0	No move (default)	
0001	0x1	1 HS shift later than default[1]	Minimum →
0011	0x3	3 HS shift later than default	
0111	0x0	7 HS shift later than default	Maximum →
1111	0xF	1 HS shift earlier than default[2]	Minimum ←
1101	0xD	3 HS shift earlier than default	
1000	0x8	8 HS shift earlier than default	Maximum ←

[1] VS closer to start of active video.
[2] VS away from start of active video.

START_VS_EVEN[3:0], Addr 44 (CP), Address 0x89[7:4]

A control to shift the position of the leading edge of the Vsync output by the CP core.

This register stores a signed value in a twos complement format. START_VS_EVEN[3:0] is the number of lines by which the leading edge of the Vsync is shifted (for example, 0x0F corresponds to a shift by one line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video).

Function

START_VS_EVEN[3:0]	Description
0x0 to 0x7	The leading edge of the even Vsync is shifted toward the active video.
0x8 to 0xF	The leading edge of the even Vsync is shifted away from the active video.

END_VS_EVEN[3:0], Addr 44 (CP), Address 0x89[3:0]

A control to shift the position of the trailing edge of the Vsync output by the CP core.

This register stores a signed value in a twos complement format. SEND_VS_EVEN[3:0] is the number of lines by which the trailing edge of the Vsync is shifted (for example, 0x0F corresponds to a shift of 1 line toward the active video, 0x01 corresponds to a shift of 1 line away from the active video).

Function

END_VS_EVEN[3:0]	Description
0x0 to 0x7	The trailing edge of the even Vsync is shifted toward the active video.
0x8 to 0xF	The trailing edge of the even Vsync is shifted away from the active video.

DE Timing Controls

DE_H_END[9:0], Addr 44 (CP), Address 0x8B[1:0]; Address 0x8C[7:0]

A control to vary the trailing edge position of the DE signal output by the CP core.

This register stores a signed value in a twos complement format. The unit of DE_H_END[9:0] is one pixel clock.

Function

DE_H_END[9:0]	Description
0x200	−512 pixels of shift
0x3FF	−1 pixel of shift
0x000 (default)	Default value (no shift)
0x001	+1 pixel of shift
0x1FF	+511 pixels

DE_H_START[9:0], Addr 44 (CP), Address 0x8B[3:2]; Address 0x8D[7:0]

A control to vary the leading edge position of the DE signal output by the CP core.

This register stores a signed value in a twos complement format. The unit of DE_H_START[9:0] is one pixel clock.

Function

DE_H_START[9:0]	Description
0x200	−512 pixels of shift
0x3FF	−1 pixel of shift
0x000 (default)	Default value (no shift)
0x001	+1 pixel of shift
0x1FF	+511 pixels

DE_V_START[3:0], Addr 44 (CP), Address 0x8E[7:4]

A control to vary the start position of the VBI region.

This register stores a signed value represented in a twos complement format. The unit of DE_V_START[9:0] is one line.

Function

DE_V_START[3:0]	Description
1000	−8 lines of shift
1111	−1 line of shift
0000 (default)	Default
0001	+1 line of shift
0111	+7 lines of shift

DE_V_END[3:0], Addr 44 (CP), Address 0x8E[3:0]

A control to vary the position of the end of the VBI region.

This register stores a signed value represented in a twos complement format. The unit of DE_V_START[9:0] is one line.

Function

DE_V_END[3:0]	Description
1000	−8 lines of shift
1111	−1 line of shift
0000 (default)	Default
0001	+1 line of shift
0111	+7 lines of shift

DE_V_START_EVEN[3:0], Addr 44 (CP), Address 0x88[7:4]

A control to vary the start position of the VBI region in even field.

This register stores a signed value represented in a twos complement format. The unit of DE_V_START_EVEN[9:0] is one pixel clock.

Function

DE_V_START_EVEN[3:0]	Description
Range	−8 to +7 lines

DE_V_END_EVEN[3:0], Addr 44 (CP), Address 0x88[3:0]

A control to vary the position of the end of the VBI region in even field.

This register stores a signed value represented in a twos complement format. The unit of DE_V_END_EVEN[9:0] is one pixel clock.

Function

DE_V_END_EVEN[3:0]	Description
Range	−8 to +7 lines

FIELD Timing Controls

Programming of the FIELD timing signals is listed in this section. The FIELD signal is shown in Figure 56, Figure 57, Figure 58, and Figure 61 can be adjusted in the described manner. (Progressive systems do not have a FIELD signal.)

Table 64. FIELD Default Timing

Characteristic	Units	525i	625i	525p	625p	720p	1080i
START_FO END_FO range maximum	Line	7	7	N/A	N/A	N/A	7
START_FO END_FO range maximum	Line	8	8	N/A	N/A	N/A	8

START_FE[3:0], Addr 44 (CP), Address 0x80[7:4]

A control to shift the position of the start of even field edge of the FIELD signal output by the CP core.

This register stores a signed value in a twos complement format. START_FE[3:0] the number of lines by which the start of the even fields edge of the FIELD signal is shifted (for example, 0x0D corresponds to a shift of three lines toward the active video, 0x05 corresponds to a shift of five lines away from the active video).

Function

START_FE[3:0]	Description
0x0 (default)	Default value.
0x0 to 0x7	The edge of the FIELD signal corresponding to the start of the even field is shifted toward the active video.
0x8 to 0xF	The trailing of the FIELD signal corresponding to the start of the even field is shifted away from the active video.

Table 65. Controlling the Even Field Section of the FIELD Timing Signal

START_FE[3:0]	Hex	Result	Note
0000 (default)	0x0	No move (default)	
0001	0x1	1 HS shift later than default[1]	Minimum →
0011	0x3	3 HS shift later than default	
0111	0x7	7 HS shift later than default	Maximum →
1111	0xF	1 HS shift earlier than default[2]	Minimum ←
1101	0xD	3 HS shift earlier than default	
1000	0x8	8 HS shift earlier than default	Maximum ←

[1] Closer to active video.
[2] Away from active video.

START_FO[3:0], Addr 44 (CP), Address 0x80[3:0]

A control to shift the position of the start of odd field edge of the FIELD signal output by the CP core.

This register stores a signed value in a twos complement format. START_FO[3:0] the number of lines by which the start of the odd fields edge of the FIELD signal is shifted (for example, 0x0D corresponds to a shift of 3 lines toward the active video, 0x05 corresponds to a shift of 5 line away from the active video).

Function

START_FO[3:0]	Description
0x0 (default)	Default value.
0x0 to 0x7	The edge of the FIELD signal corresponding to the start of the odd field is shifted toward the active video.
0x8 to 0xF	The trailing of the FIELD signal corresponding to the start of the odd field is shifted away from the active video.

Table 66. Controlling the Odd Field Section of FIELD Timing Signal

START_FO[3:0]	Hex	Result	Note
0000 (default)	0x0	No move (default)	
0001	0x1	1 HS shift later than default[1]	Minimum →
0011	0x3	3 HS shift later than default	
0111	0x0	7 HS shift later than default	Maximum →
1111	0xF	1 HS shift earlier than default[2]	Minimum ←
1101	0xD	3 HS shift earlier than default	
1000	0x8	8 HS shift earlier than default	Maximum ←

[1] Closer to active video.
[2] Away from active video.

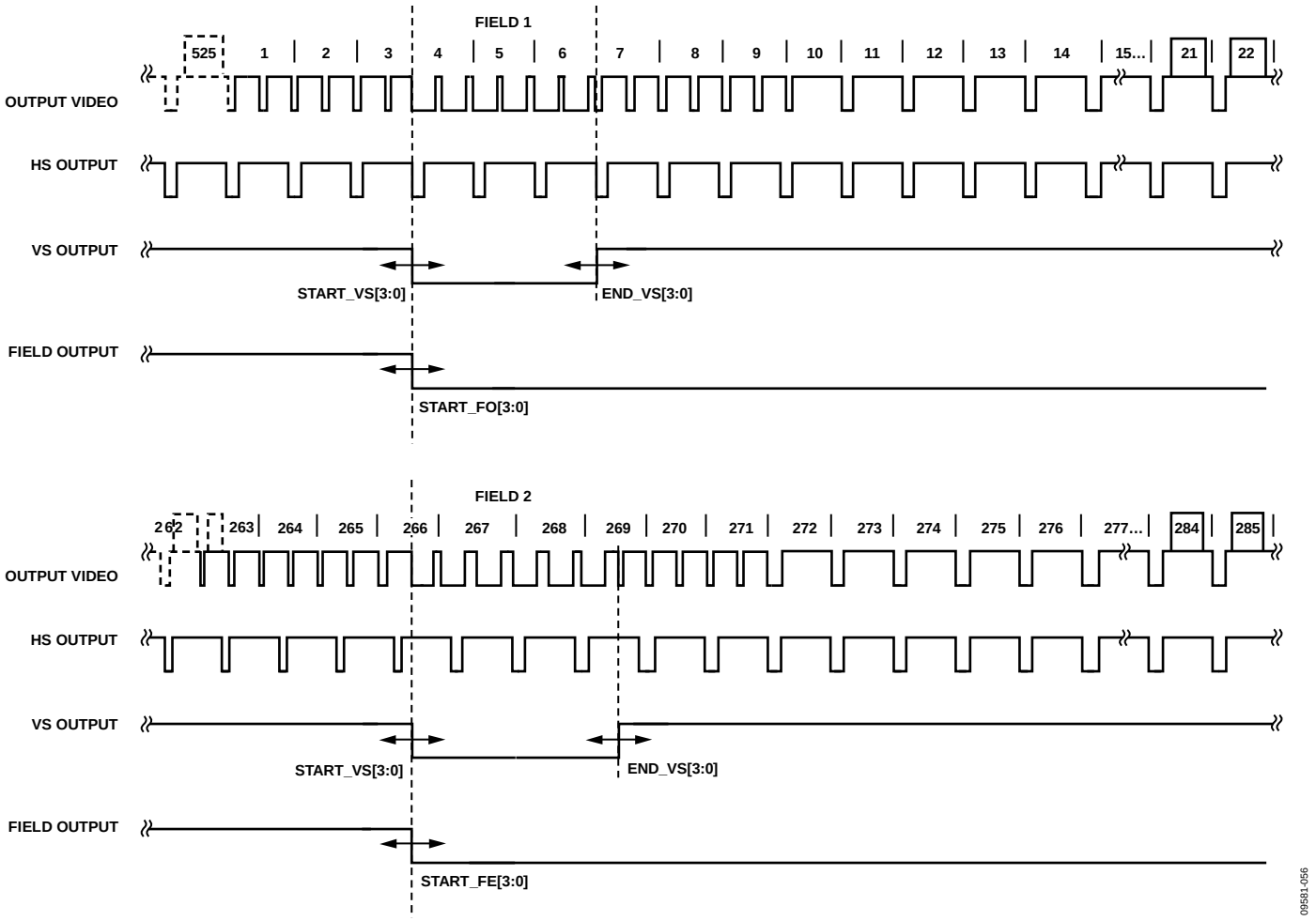


Figure 56. 525i VS Timing

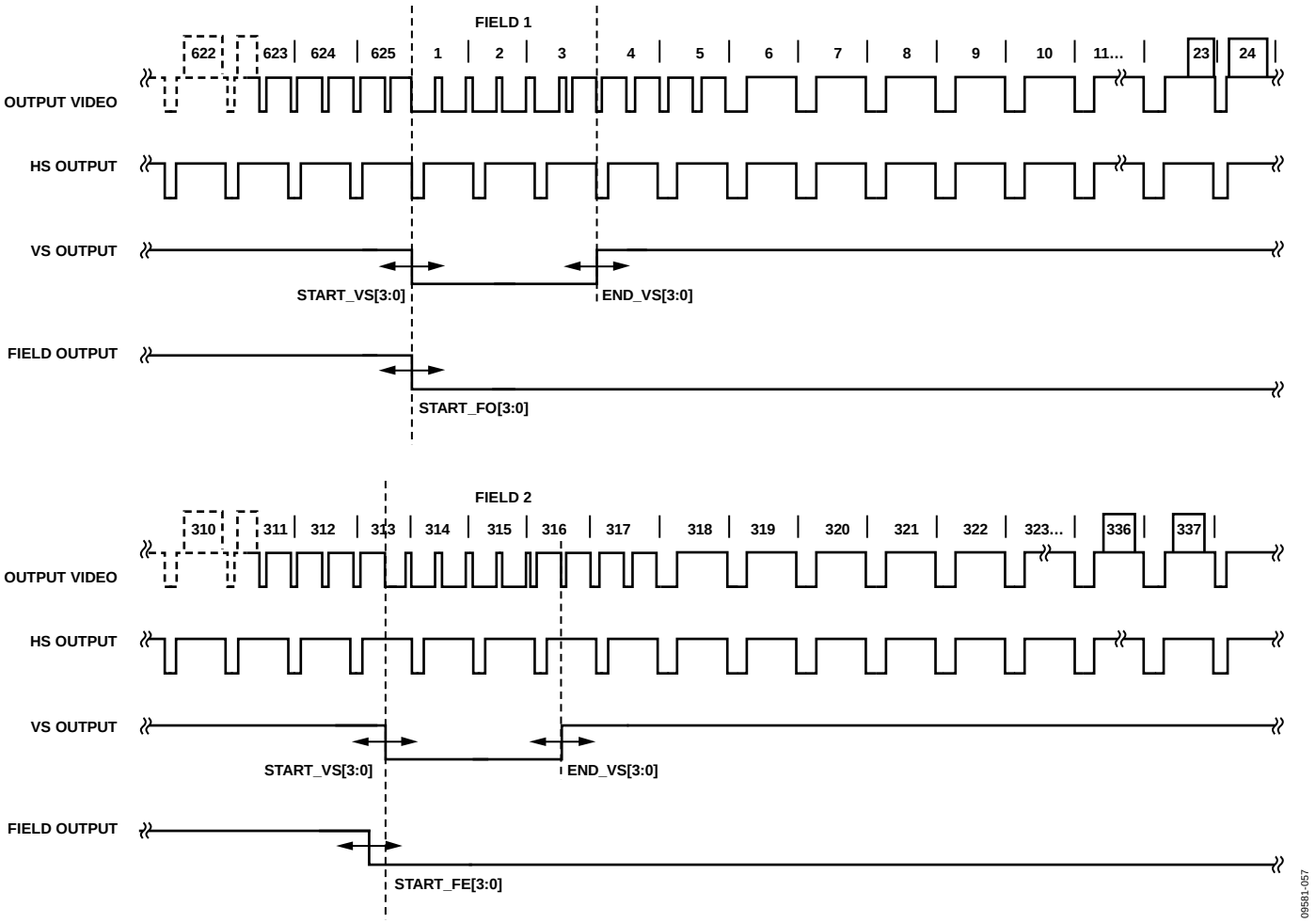


Figure 57. 625i VS Timing

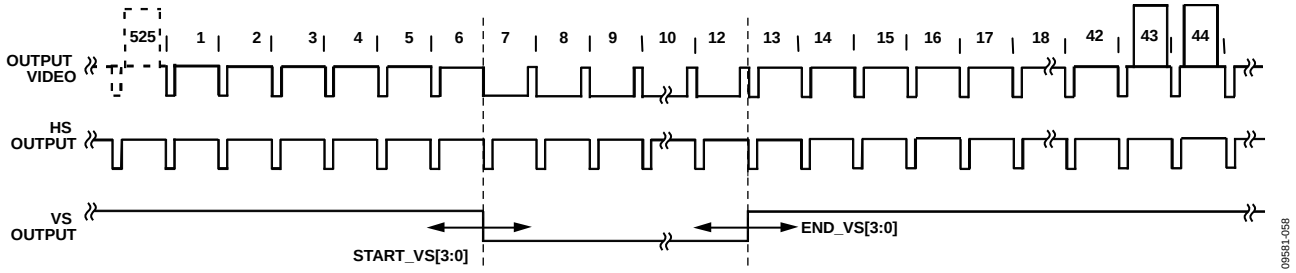


Figure 58. 525p VS Timing

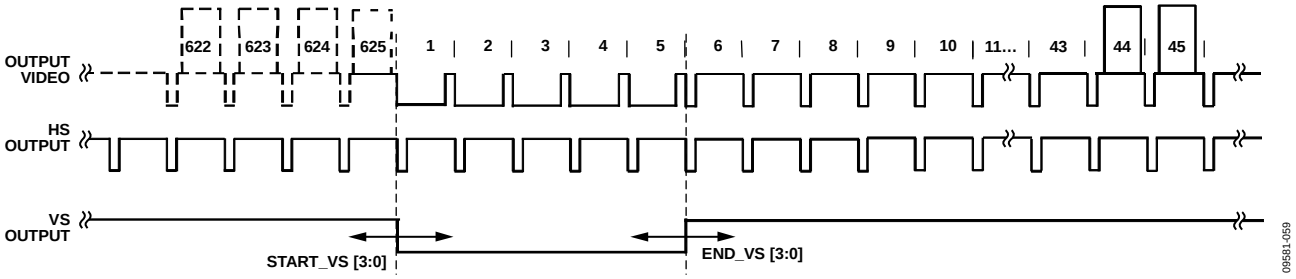


Figure 59. 625p VS Timing

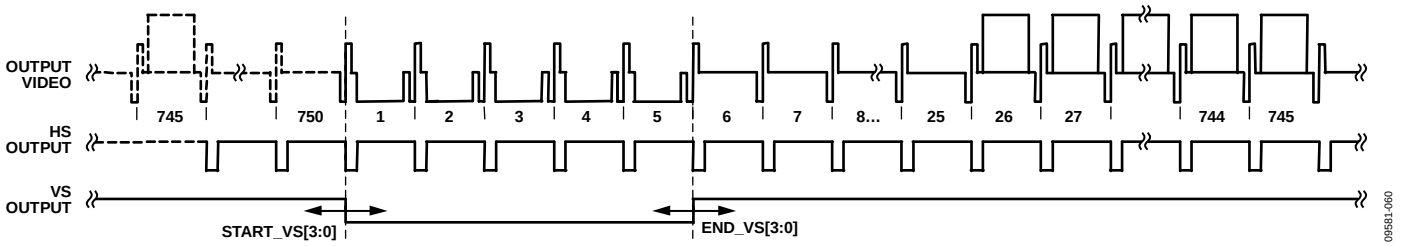


Figure 60. 720p VS Timing

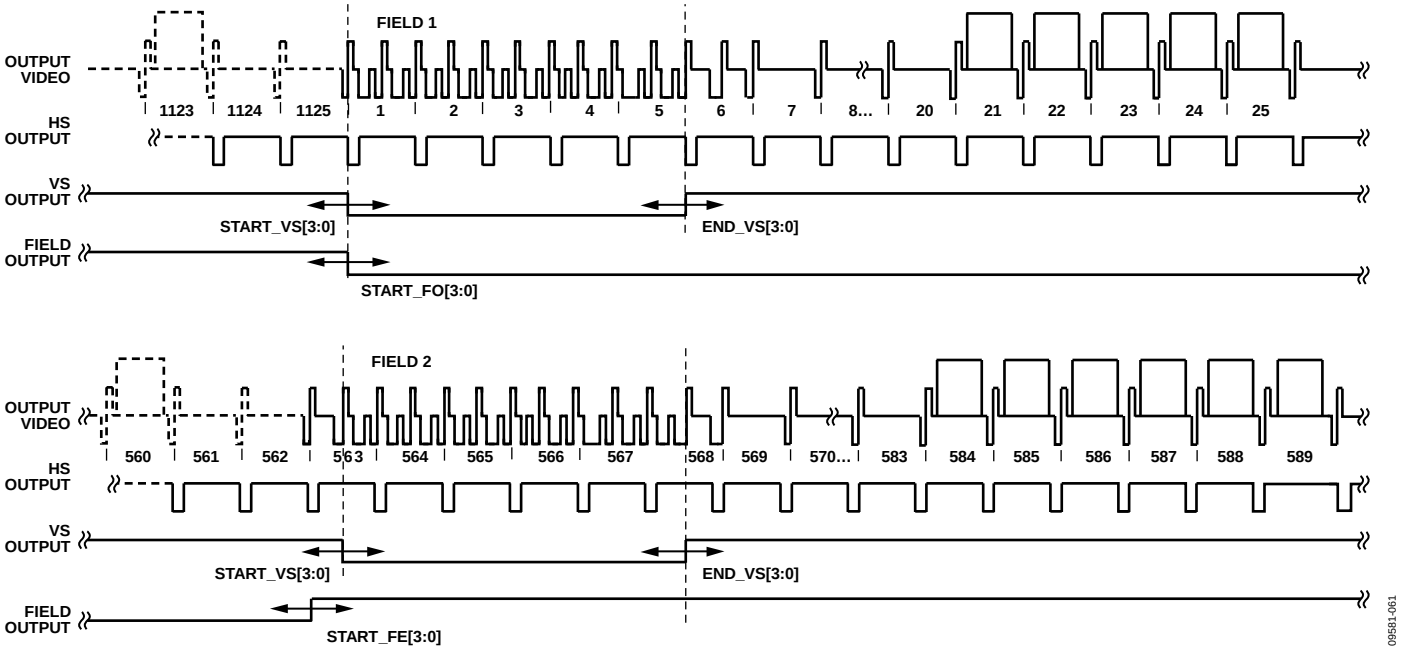


Figure 61. 1080i VS Timing

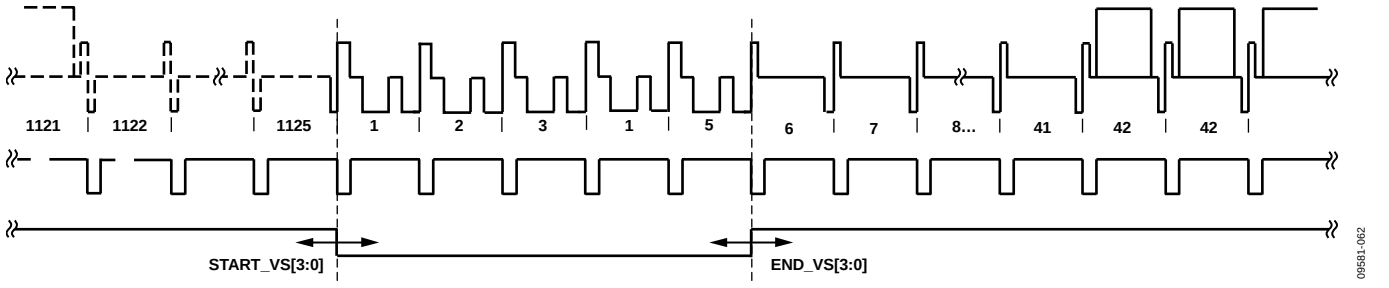


Figure 62. 1080p VS Timing

HCOUNT Timing Control

HCOUNT_ALIGN_ADJ[4:0], Addr 44 (CP), Address 0xBE[1:0]; Address 0xBF[7:5]

Manual adjustment for internally generated hcount offset. This register allows an adjustment of 15 pixels to the left or to the right. The MSB sets the direction (left or right) and the 4 LSBs set the number of pixels to move. This is an unsigned control.

Function

HCOUNT_ALIGN_ADJ[4:0]	Description
00000 (default)	Default value

CP HDMI CONTROLS

HDMI_CP_LOCK_THRESHOLD[1:0], Addr 44 (CP), Address 0xCB[1:0]

Locking time of filter used for buffering of timing parameters in HDMI mode.

Function

HDMI_CP_LOCK_THRESHOLD[1:0]	Description
00 (default)	Slowest locking time
01	Medium locking time
10	Fastest locking time
11	Fixed step size of 0.5 pixels

FREE RUN MODE

Free run mode provides the user with a stable clock and predictable data if the input signal cannot be decoded, for example, if input video is not present. It controls default color insertion and causes the ADV7619 to generate a default clock. The state in which this happens can be monitored via the **CP_FREE_RUN** status bit. (Refer to the CP Status section for more information.). The free run feature is not configured automatically for HDMI modes. In addition ADV7619 can free run only to HDMI video up to 2.25 Gbps.

Free Run Mode Thresholds

The free run threshold parameters define the horizontal and vertical conditions under which free run mode is entered. The horizontal and vertical parameters of the incoming video signal are measured and compared with internally stored parameters, and the magnitude of the difference decides whether to enter free run. The internally stored parameters are decoded by default from **PRIM_MODE[3:0]** and **VID_STD[5:0]**. For video standards other than the preprogrammed settings of **PRIM_MODE[3:0]** and **VID_STD[5:0]**, the parameters can be set manually.

Horizontal Conditions

In the case of the horizontal conditions, the length of the incoming video line is measured based on the 28.6363 MHz crystal clock. This value is compared with the internally stored horizontal parameter, the ideal line length. The CH1_F_RUN_TH[2:0] control bits allow the user to select the threshold for Channel 1. The ideal line length can be manually set via the Free-run Line Length control, CH1_FR_LL[10:0].

CH1_F_RUN_THR[2:0], Addr 44 (CP), Address 0xF3[2:0]

Free run threshold select for Sync Channel 1. Determines the horizontal conditions under which free run mode is entered or left. The length of the incoming video line is measured based on the crystal clock and compared to an internally stored parameter. The magnitude of the difference decides whether or not sync Channel 1 enters free run mode.

Function

CH1_F_RUN_THR[2:0]	Description
000	Minimum difference to switch into free run is 2. Maximum difference to switch out of free run is 1.
001	Minimum difference to switch into free run is 256. Maximum difference to switch out of free run is 200.
010	Minimum difference to switch into free run is 128. Maximum difference to switch out of free run is 112.
011	Minimum difference to switch into free run is 64. Maximum difference to switch out of free run is 48.
100 (default)	Minimum difference to switch into free run is 32. Maximum difference to switch out of free run is 24.
101	Minimum difference to switch into free run is 16. Maximum difference to switch out of free run is 12.
110	Minimum difference to switch into free run is 8. Maximum difference to switch out of free run is 6.
111	Minimum difference to switch into free run is 4. Maximum difference to switch out of free run is 3.

CH1_FR_LL[10:0], Addr 44 (CP), Address 0x8F[2:0]; Address 0x90[7:0]

Free run line length in number of crystal clock cycles in one line of video for Sync Channel 1 STDI. This register should only be programmed video standards that are not supported by PRIM_MODE[3:0] and VID_STD[5:0].

Function

CH1_FR_LL[10:0]	Description
0x000 (default)	Internal free run line length is decoded from PRIM_MODE[3:0] and VID_STD[5:0].
All other values	Number of crystal clocks in the ideal line length. Used to enter or exit free run mode.

Notes

- This parameter has no effect on the video decoding.
- If CH1_FR_LL[10:0] is not programmed, then the free-run line length parameter is decoded from **PRIM_MODE[3:0]** and **VID_STD[5:0]**.

Vertical Conditions

In the case of the vertical conditions, the STDI section measures the number of lines per field of incoming video signal. This value is compared with an internally stored vertical parameter, the ideal field length. The CH1_FL_FR_THRESHOLD[1:0] control bits allow the user to select the threshold for Channel 1. The ideal number of lines per field can be set manually via the CP_LCOUNT_MAX[11:0] register.

CH1_FL_FR_THRESHOLD[2:0], Addr 44 (CP), Address 0xF3[5:3]

Threshold for difference between input video field length and internally stored standard to enter and exit free run.

Function

CH1_FL_FR_THRESHOLD[2:0]	Description
000	Minimum difference to switch into free run is 36 lines. Maximum difference to switch out of free run is 31 lines.
001	Minimum difference to switch into free run is 18 lines. Maximum difference to switch out of free run is 15 lines.
010 (default)	Minimum difference to switch into free run is 10 lines. Maximum difference to switch out of free run is 7 lines.
011	Minimum difference to switch into free run is 4 lines. Maximum difference to switch out of free run is 3 lines.
100	Minimum difference to switch into free run is 51 lines. Maximum difference to switch out of free run is 46 lines.
101	Minimum difference to switch into free run is 69 lines. Maximum difference to switch out of free run is 63 lines.
110	Minimum difference to switch into free run is 134 lines. Maximum difference to switch out of free run is 127 lines.
111	Minimum difference to switch into free run is 263 lines. Maximum difference to switch out of free run is 255 lines.

CP_LCOUNT_MAX[11:0], Addr 44 (CP), Address 0xAB[7:0]; Address 0xAC[7:4]

Manual value for total number of lines in a frame expected by the CP core. CP_LCOUNT_MAX[11:0] is an unsigned value. This register is used for manual configuration of the free run feature. The value programmed in this register is used for Sync Channel 1. The value programmed in this register is used also for Sync Channel 2 if CH2_FR_FIELD_LENGTH[10:0] set to 0x000.

Function

CP_LCOUNT_MAX[11:0]	Description
0x000 (default)	Ideal number of lines per frame is decoded from PRIM_MODE[3:0] and VID_STD[5:0] for Sync Channel 1.
All other values	Use the programmed value as ideal number of lines per frame in free run decision for Sync Channel 1.

INTERLACED, Addr 44 (CP), Address 0x91[6]

Sets the interlaced/progressive mode of the incoming video processed in CP mode.

Function

INTERLACED	Description
0	The CP core expects progressive video mode
1 (default)	the CP core expects interlaced video mode

Field line count is the vertical parameter that holds the ideal number of lines per field for a given video standard. It affects the way CP handles the unlocked state. It affects the way CP handles the unlocked state. If **CP_LCOUNT_MAX[11:0]** is set to 0, the internally used free run line length value is decoded from the current setting of PRIM_MODE[3:0] and VID_STD[5:0].

For standards not covered by the preprogrammed values, the **CP_LCOUNT_MAX[11:0]** and **INTERLACED** parameters must be set to the ideally expected number of lines per field.

Notes

- The CP_LCOUNT_MAX[11:0] parameter has no effect on the video decoding.
- If CP_LCOUNT_MAX[11:0] is not programmed, then the Free-run Line Length parameter is decoded from **PRIM_MODE[3:0]** and **VID_STD[5:0]**.
- If CP_LCOUNT_MAX[11:0] is programmed, then Free-run Line Length parameter defined by CP_LCOUNT_MAX[11:0] and INTERLACED, is used for Channel 1.

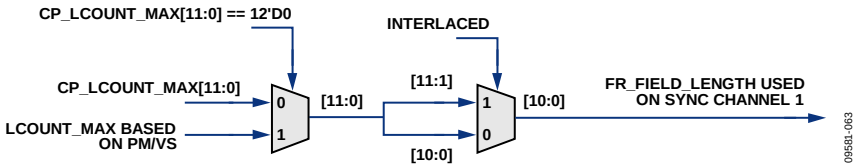


Figure 63. Free Run Field Length Selection for Channel 1 and Channel 2

Free Run Feature in HDMI Mode

This section describes how to configure the free run feature when the ADV7619 is in HDMI mode. The ADV7619 HDMI mode is defined in the Primary Mode and Video Standard section.

There are two free run modes in HDMI: Free Run Mode 0 and Free Run Mode 1. The HDMI_FRUN_MODE control selects which free run mode is enabled.

- HDMI Free Run Mode 0:
  The decoder enters free run when the TMDS clock is not detected, for example, in a cable disconnect situation.
- HDMI Free Run Mode 1:
  The decoder enters free run when the TMDS clock is not detected or when the detected input format does not match the format dictated by the **PRIM_MODE[3:0]** and **VID_STD[5:0]** settings.

For either free run mode to be implemented, HDMI free run operation must be enabled. This is done via the HDMI_FRUN_EN control.

HDMI_FRUN_EN, Addr 44 (CP), Address 0xBA[0]

A control to enable free run in HDMI mode.

Function

HDMI_FRUN_EN	Description
0	Disable the free run feature in HDMI mode
1 (default)	Enable the free run feature in HDMI mode

HDMI_FRUN_MODE, Addr 44 (CP), Address 0xBA[1]

A control to configure the free run feature in HDMI mode.

Function

HDMI_FRUN_MODE	Description
0 (default)	HDMI free run Mode 0. The part free runs when the TMDS clock is not detected on the selected HDMI port.
1	HDMI free run Mode 1. The CP core free runs when the TMDS clock is not detected on the selected HDMI port or it the video resolution of HDMI stream processed by the part does not match the video resolution programmed in PRIM_MODE[3:0] and VID_STD[5:0].

DIS_AUTO_PARAM_BUFF, Addr 44 (CP), Address 0xC9[0]

A control to disable the buffering of the timing parameters used for free run in HDMI mode.

Function

DIS_AUTO_PARAM_BUFF	Description
0 (default)	Buffer the last measured parameters in HDMI mode used to determine video resolution the part free runs into.
1	Disable the buffering of measured parameters in HDMI mode. Free run standard determined by PRIM_MODE[3:0], VID_STD[5:0] and V_FREQ[2:0]

It is also possible to custom program the resolution that the ADV7619 should expect for free run Mode 1 by programming the free-run line length, line count max, and interlaced registers. Refer to the Free Run Mode section for the configuration of these registers.

Note: This mode (that is, DIS_AUTOPARAM_BUFFER = 1) does not support HDMI input with deep color.

Free Run Default Color Output

In the event of loss of input signal, the ADV7619 may enter free run and can be configured to output a default color rather than noise. The default color values are given in Table 67.

The times at which the default colors are inserted can be set as follows:

- Free run is forced: default colors are always output
- Automatic free run mode: default colors are output when the system detects a loss of video signal

Table 67. Default Color Output Values (CP)

Mode	CP_DEF_COL_MAN_VAL	Signal	Value
Default—GR	0	CH_A (G)	0
		CH_B (R)	0
		CH_C (B)	135_d
Default—COMP	0	CH_A (Y)	35_d
		CH_A (Pr)	114_d
		CH_A (Pb)	212_d
Man. Override	1	CH_A	4·DEF_COL_CHA[7:0]
		CH_B	4·DEF_COL_CHB[7:0]
		CH_C	4·DEF_COL_CHC[7:0]

CP_FORCE_FREERUN, Addr 44 (CP), Address 0xBF[0]

A control to force the CP to free run.

Function

CP_FORCE_FREERUN	Description
0 (default)	Do not force the CP core free run.
1	Force the CP core to free run.

CP_DEF_COL_AUTO, Addr 44 (CP), Address 0xBF[1]

A control to enable the insertion of default color when the CP free runs.

Function

CP_DEF_COL_AUTO	Description
0	Disable automatic insertion of default color
1 (default)	Output default colors when the CP free runs

CP_DEF_COL_MAN_VAL, Addr 44 (CP), Address 0xBF[2]

A control to enable manual selection of the color used when the CP core free runs.

Function

CP_DEF_COL_MAN_VAL	Description
0 (default)	Uses default color blue
1	Outputs default colors as given in CP_DEF_COL_CHA, CP_DEF_COL_B and CP_DEF_COL_C

Table 67 shows the default colors for component and graphics based video. The values describe the color blue. Setting the CP_DEF_COL_MAN_VAL bit high enables the user to overwrite the default colors with the values given in DEF_COL_CHA[7:0], DEF_COL_CHB[7:0], and DEF_COL_CHC[7:0].

The three parameters DEF_COL_CHA[7:0], DEF_COL_CHB[7:0], and DEF_COL_CHC[7:0] allow the user to specify their own default values.

Note: CP_DEF_COL_MAN_VAL must be set high for the three parameters to be used. See Table 67 for more information on the automatic values.

DEF_COL_CHA[7:0], Addr 44 (CP), Address 0xC0[7:0]

A control the set the default color for Channel A. To be used if CP_DEF_COL_MAN_VAL is 1.

Function

DEF_COL_CHA[7:0]	Description
0x00 (default)	Default value

DEF_COL_CHB[7:0], Addr 44 (CP), Address 0xC1[7:0]

A control to set the default color for Channel B. To be used if CP_DEF_COL_MAN_VAL is 1.

Function

DEF_COL_CHB[7:0]	Description
0x00 (default)	Default value

DEF_COL_CHC[7:0], Addr 44 (CP), Address 0xC2[7:0]

A control to set the default color for Channel C. To be used if CP_DEF_COL_MAN_VAL is 1.

Function

DEF_COL_CHC[7:0]	Description
0x00 (default)	Default value

CP STATUS

CP_REG_FF

CP_REG_FF is a status register that contains status bits for the CP core. Register CP_REG_FF holds field: CP_FREE_RUN.

CP_REG_FF Bit Number	Bit Name	Description
0	Reserved	
1	Reserved	
2	Reserved	
3	Reserved	
4	CP_FREE_RUN	CP is free running (no valid video signal found)
5	Reserved	
6	Reserved	
7	Reserved	

CP_FREE_RUN, Addr 44 (CP), Address 0xFF[4] (Read Only)

Component processor free run status.

Function

CP_FREE_RUN	Description
0 (default)	The CP is not free running.
1	The CP is free running.

CP CORE BYPASSING

It is possible to bypass CP core completely with using following register. When OP_FORMAT_SEL is set to 0x94, 0x95, 0x96, 0x54 CP_COMPLETE_BYPASS_IN_HDMI_MODE must be set to 0.

CP_COMPLETE_BYPASS_IN_HDMI_MODE, IO, Address 0xBF[0]

Function

CP_COMPLETE_BYPASS_IN_HDMI_MODE	Description
0 «	Normat mode
1	HDMI data directly fed to output bypassing CP completely, CP_CLK can be powered down

CONSUMER ELECTRONICS CONTROL

The Consumer Electronics Control (CEC) module features the hardware required to behave as an initiator or a follower as per the specifications for a CEC device. The CEC module contains four main sections:

- Transmit section CEC_TX
- Receive section CEC_RX
- Clock generator section CEC_CLK_GEN
- Antiglitch filter section CEC_ANTI_GLITCH

The block diagram of the CEC module is shown in Figure 64.

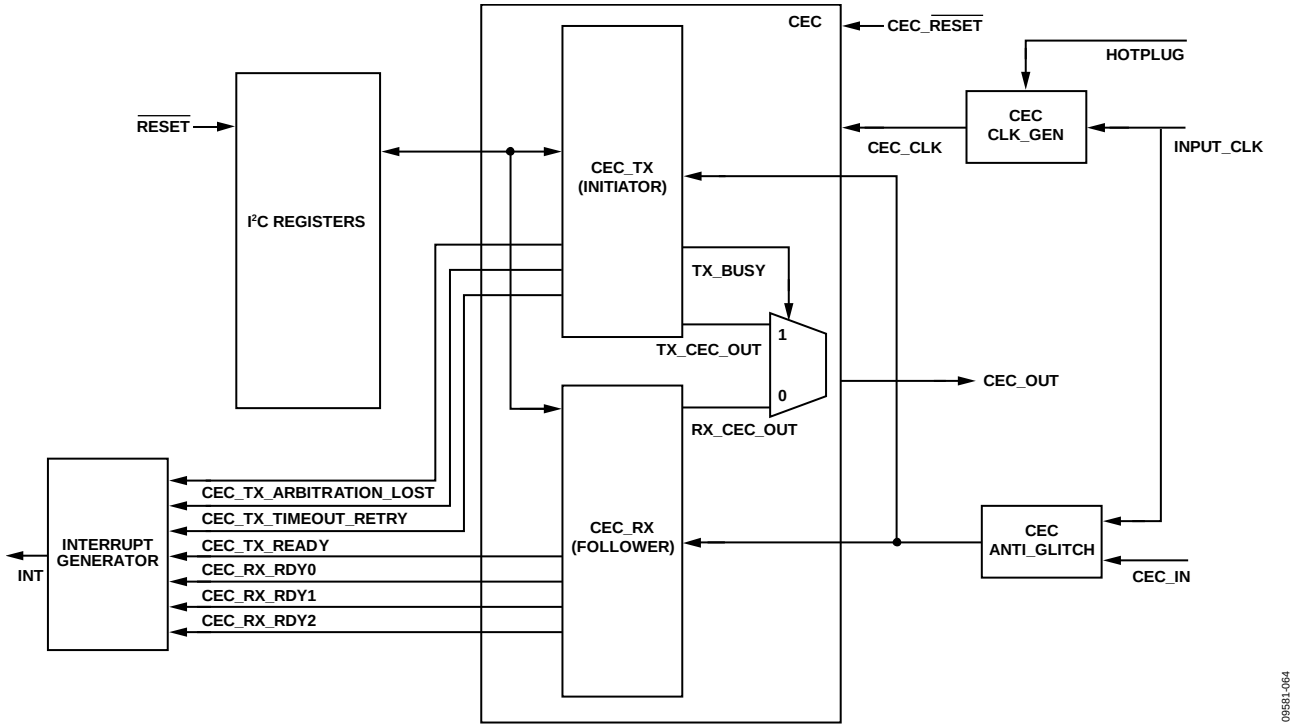


Figure 64. CEC Module Block Diagram

MAIN CONTROLS

This section describes the main controls for the CEC module.

CEC_POWER_UP, Addr 80 (CEC), Address 0x2A[0]

Power mode of CEC module.

Function

CEC_POWER_UP	Description
0 (default)	Power down the CEC module
1	Power up the CEC module

CEC_SOFT_RESET, Addr 80 (CEC), Address 0x2C[0] (Self-Clearing)

CEC module software reset.

Function

CEC_SOFT_RESET	Description
0 (default)	No function
1	Reset the CEC module

Note that the CEC_POWER_UP bit can be used to set the ADV7619 to Power-Down Mode 1 (refer to the Power-Down Mode 1 section).

CEC TRANSMIT SECTION

The transmit section features the hardware required for the CEC module to act as an initiator. The host utilizes this section to transmit directly addressed messages or broadcast messages on the CEC bus. When the host wants to a send message to other CEC devices, it writes the message to the CEC outgoing message registers (refer to Table 68) and the message length register. Then, the host enables the transmission process by setting the CEC_TX_ENABLE bit to 1. When the message transmission is completed, or if an error occurs, the CEC transmitter section generates an interrupt (assuming the corresponding interrupt mask bits are set accordingly).

Table 68. CEC Outgoing Message Buffer Registers

Register Name	CEC Map Address	Description
CEC_TX_FRAME_HEADER[7:0]	0x00	Header of next outgoing message
CEC_TX_FRAME_DATA0[7:0]	0x01	Byte 0 of next outgoing message
CEC_TX_FRAME_DATA1[7:0]	0x02	Byte 1 of next outgoing message
CEC_TX_FRAME_DATA2[7:0]	0x03	Byte 2 of next outgoing message
CEC_TX_FRAME_DATA3[7:0]	0x04	Byte 3 of next outgoing message
CEC_TX_FRAME_DATA4[7:0]	0x05	Byte 4 of next outgoing message
CEC_TX_FRAME_DATA5[7:0]	0x06	Byte 5 of next outgoing message
CEC_TX_FRAME_DATA6[7:0]	0x07	Byte 6 of next outgoing message
CEC_TX_FRAME_DATA7[7:0]	0x08	Byte 7 of next outgoing message
CEC_TX_FRAME_DATA8[7:0]	0x09	Byte 8 of next outgoing message
CEC_TX_FRAME_DATA9[7:0]	0x0A	Byte 9 of next outgoing message
CEC_TX_FRAME_DATA10[7:0]	0x0B	Byte 10 of next outgoing message
CEC_TX_FRAME_DATA11[7:0]	0x0C	Byte 11 of next outgoing message
CEC_TX_FRAME_DATA12[7:0]	0x0D	Byte 12 of next outgoing message
CEC_TX_FRAME_DATA13[7:0]	0x0E	Byte 13 of next outgoing message
CEC_TX_FRAME_DATA14[7:0]	0x0F	Byte 14 of next outgoing message

CEC_TX_FRAME_LENGTH[4:0], Addr 80 (CEC), Address 0x10[4:0]

Message size of the transmitted frame. This is the number of byte in the outgoing message including the header.

Function

CEC_TX_FRAME_LENGTH[4:0]	Description
xxxxx	Total number of bytes (including header byte) to be sent

CEC_TX_ENABLE, Addr 80 (CEC), Address 0x11[0]

This bit enables the TX section. When set to 1, it initiates the start of transmission of the message in the outgoing message buffer. When the message transmission is completed, this bit is automatically reset to 0. If it is manually set to 0 during a message transmission it may terminate the transmission depending on what stage of the transmission process has been reached. If the message transmission is sill in the 'signal free time' stage the message transmission will be terminated. If data transmission has begun then the transmission will continue until the message is fully sent, or until an error condition occurs.

Function

CEC_TX_ENABLE	Description
0 (default)	Transmission mode disabled
1	Transmission mode enabled and message transmission started

The ADV7619 features three status bits related to the transmission of CEC messages. The events that set these bits are mutually exclusive, that is, only one of the three events can occur during any given message transmission.

- **CEC_TX_READY_ST**
- **CEC_TX_ARBITRATION_LOST_ST**
- **CEC_TX_RETRY_TIMEOUT_ST**

CEC_TX_READY_ST, IO, Address 0x93[0] (Read Only)

Latched status of CEC_TX_READY_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When the CEC TX successfully sends the current message this bit is set. Once set, this bit will remain high until the interrupt is cleared via CEC_TX_READY_CLR.

Function

CEC_TX_READY_ST	Description
0 (default)	No change
1	Message transmitted successfully

CEC_TX_ARBITRATION_LOST_ST, IO, Address 0x93[1] (Read Only)

Latched status of CEC_TX_ARBITRATION_LOST_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX loses arbitration while trying to send a message this bit is set. Once set, this bit will remain high until the interrupt is cleared via CEC_TX_ARBITRATION_LOST_CLR.

Function

CEC_TX_ARBITRATION_LOST_ST	Description
0 (default)	No change
1	The CEC TX has lost arbitration to another TX

CEC_TX_RETRY_TIMEOUT_ST, IO, Address 0x93[2] (Read Only)

Latched status of CEC_TX_RETRY_TIMEOUT_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. If the CEC TX fails to send the current message within the number of retry attempts specified by CEC_TX_RETRY this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_TX_RETRY_TIMEOUT_CLR.

Function

CEC_TX_RETRY_TIMEOUT_ST	Description
0 (default)	No change
1	CEC TX has tried but failed to resend the current message for the number of times specified by CEC_TX_RETRY

CEC_TX_RETRY[2:0], Addr 80 (CEC), Address 0x12[6:4]

The number of times the CEC TX should try to retransmit the message if an error condition is encountered. Per the CEC specificationthis value should not be set to a value greater than 5.

Function

CEC_TX_RETRY[2:0]	Description
001 (default)	Try to retransmit the message 1 time if an error occurs
xxx	Try to retransmit the message xxx times if an error occurs

CEC_TX_NACK_COUNTER[3:0], Addr 80 (CEC), Address 0x14[3:0] (Read Only)

The number of times that the NACK error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1.

Function

CEC_TX_NACK_COUNTER[3:0]	Description
0000 (default)	No error condition
XXXX	The number of times the NACK error condition was encountered

CEC_TX_LOWDRIVE_COUNTER[3:0], Addr 80 (CEC), Address 0x14[7:4] (Read Only)

The number of times that the LOWDRIVE error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1.

Function

CEC_TX_LOWDRIVE_COUNTER[3:0]	Description
0000 (default)	No error condition
XXXX	The number of times the LOWDRIVE error condition was encountered

CEC RECEIVE SECTION

The receive section features the hardware required for the CEC module to act as a follower. Once the CEC module is powered up via the CEC_POWER_UP bit the CEC Rx section will immediately begin monitoring the CEC bus for messages with the correct logical address(es). When the message reception is completed the CEC receive section generates an interrupt (assuming the corresponding interrupt mask bits are set accordingly).

The host can disable message reception while keeping the CEC module powered up by using the FORCE_NACK bit to not acknowledge received messages.

CEC_FORCE_NACK, Addr 80 (CEC), Address 0x27[1]

Force NO-ACK control.

Setting this bit forces the CEC controller not acknowledge any received messages.

Function

CEC_FORCE_NACK	Description
0 (default)	Acknowledge received messages
1	Do not acknowledge received messages

Logical Address Configuration

The host must set the destination logical address(es) that the CEC receive section will respond to. Up to three logical addresses can be enabled allowing support for multifunction devices such as DVD recorders with TV tuners, which require multiple logical addresses. The logical address(es) are set via the following registers:

- CEC_LOGICAL_ADDRESS2[3:0] if CEC_LOGICAL_ADDRESS_MASK[2] is set to 1
- CEC_LOGICAL_ADDRESS1[3:0] if CEC_LOGICAL_ADDRESS_MASK[1] is set to 1
- CEC_LOGICAL_ADDRESS0[3:0] if CEC_LOGICAL_ADDRESS_MASK[0] is set to 1

CEC_LOGICAL_ADDRESS2[3:0], Addr 80 (CEC), Address 0x29[3:0]

Logical address 2—this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[2] to 1.

Function

CEC_LOGICAL_ADDRESS2[3:0]	Description
1111 (default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS1[3:0], Addr 80 (CEC), Address 0x28[7:4]

Logical Address 1—this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[1] to 1.

Function

CEC_LOGICAL_ADDRESS1[3:0]	Description
1111 (default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS0[3:0], Addr 80 (CEC), Address 0x28[3:0]

Logical Address 0—this address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[0] to 1.

Function

CEC_LOGICAL_ADDRESS0[3:0]	Description
1111 (default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS_MASK[2:0], Addr 80 (CEC), Address 0x27[6:4]

Logical address mask of the CEC logical devices. Up to three logical devices are supported. When the mask bits are set for a particular logical device, the logical device is enabled and messages whose destination address matches that of the selected logical address are accepted.

Function

CEC_LOGICAL_ADDRESS_MASK[2:0]	Description
[4]	Mask bit for Logical Device 0
[5]	Mask bit for Logical Device 1
[6]	Mask bit for Logical Device 2

Receive Buffers

The ADV7619 features three frame buffers that allow the receiver to receive up to three messages before the host processor needs to read a message out. When three messages have been received, no further message reception is possible until the host reads at least one message.

Note that for backwards compatibility with previous generation ADI CEC-enabled parts, only one frame buffer is enabled by default. In this default mode, after a message is received, the host processor must read the message out before any further message reception is possible. The decision to use one or three messages buffers is controlled by the CEC_USE_ALL_BUFS bit.

CEC_USE_ALL_BUFS, Addr 80 (CEC), Address 0x77[0]

Control to enable supplementary receiver frame buffers.

Function

CEC_USE_ALL_BUFS	Description
0 (default)	Use only buffer 0 to store CEC frames
1	Use all 3 buffers to stores the CEC frames

For each of the frame buffers there is a corresponding two-bit time stamp and a raw flag.

CEC_BUF0_TIMESTAMP[1:0], Addr 80 (CEC), Address 0x53[1:0] (Read Only)

Time stamp for frame stored in Receiver Frame Buffer 0. This can be used to determine which frame should be read next from the receiver frame buffers.

Function

CEC_BUF0_TIMESTAMP[1:0]	Description
00 (default)	Invalid timestamp, no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered, this frame was the third to be received

CEC_BUF1_TIMESTAMP[1:0], Addr 80 (CEC), Address 0x53[3:2] (Read Only)

Time stamp for frame stored in Receiver Frame Buffer 1. This can be used to determine which frame should be read next from the receiver frame buffers.

Function

CEC_BUF1_TIMESTAMP[1:0]	Description
00 (default)	Invalid timestamp, no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered, this frame was the third to be received

CEC_BUF2_TIMESTAMP[1:0], Addr 80 (CEC), Address 0x53[5:4] (Read Only)

Time stamp for frame stored in Receiver Frame Buffer 2. This can be used to determine which frame should be read next from the receiver frame buffers.

Function

CEC_BUF2_TIMESTAMP[1:0]	Description
00 (default)	Invalid timestamp, no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered, this frame was the third to be received

CEC_RX_RDY0_ST, IO, Address 0x93[3] (Read Only)

Latched status of CEC_RX_RDY0_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into Buffer 0, this bit is set. Once set, this bit will remain high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Function

CEC_RX_RDY0_ST	Description
0 (default)	No change
1	New CEC message received in Buffer 0

CEC_RX_RDY1_ST, IO, Address 0x93[4] (Read Only)

Latched status of CEC_RX_RDY1_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into Buffer 1, this bit is set. Once set, this bit will remain high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Function

CEC_RX_RDY1_ST	Description
0 (default)	No change
1	New CEC message received in Buffer 1

CEC_RX_RDY2_ST, IO, Address 0x93[5] (Read Only)

Latched status of CEC_RX_RDY2_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. When a message has been received into Buffer 2, this bit is set. Once set, this bit will remain high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Function

CEC_RX_RDY2_ST	Description
0 (default)	No change
1	New CEC message received in Buffer 2

When a message (other than a polling message) is received it is loaded into the first available frame buffer (starting with Buffer 0) and a 2-bit time stamp is generated for that buffer. If the corresponding interrupt mask bit is set the status bit relating to that buffer is set and an interrupt is generated to alert the host processor to the fact that a message has been received.

When all three frame buffers are full, the receive module can no longer receive CEC messages and will not acknowledge any new messages (other than polling messages). In the case that only one frame buffer is enabled (the default condition) then only one message can be received. In this case the received message is always available in Buffer 0.

The host can read the receive buffers (refer to Table 69, Table 70 and Table 71) to get the messages that were addressed to the CEC receiver. The length of each received message is available in the corresponding frame length register.

Table 69. CEC Incoming Frame Buffer 0 Registers

Register Name	CEC Map Address	Description
CEC_BUF0_RX_FRAME_HEADER[7:0]	0x15	Header of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA0[7:0]	0x16	Byte 0 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA1[7:0]	0x17	Byte 1 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA2[7:0]	0x18	Byte 2 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA3[7:0]	0x19	Byte 3 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA4[7:0]	0x1A	Byte 4 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA5[7:0]	0x1B	Byte 5 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA6[7:0]	0x1C	Byte 6 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA7[7:0]	0x1D	Byte 7 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA8[7:0]	0x1E	Byte 8 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA9[7:0]	0x1F	Byte 9 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA10[7:0]	0x20	Byte 10 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA11[7:0]	0x21	Byte 11 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA12[7:0]	0x22	Byte 12 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA13[7:0]	0x23	Byte 13 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA14[7:0]	0x24	Byte 14 of message in Frame Buffer 0

CEC_BUF0_RX_FRAME_LENGTH[4:0], Addr 80 (CEC), Address 0x25[4:0] (Read Only)

Function

CEC_BUF0_RX_FRAME_LENGTH[4:0]	Description
xxxxx	The total number of bytes (including header byte) that were received into Buffer 0

CEC_CLR_RX_RDY0, Addr 80 (CEC), Address 0x2C[1] (Self-Clearing)

Clear control for CEC_RX_RDY0.

Function

CEC_CLR_RX_RDY0	Description
0 (default)	Retain the value of the CEC_RX_RDY0 flag
1	Clear the value of the CEC_RX_RDY0 flag

Table 70. CEC Incoming Frame Buffer 1 Registers

Register Name	CEC Map Address	Description
CEC_BUF1_RX_FRAME_HEADER[7:0]	0x54	Header of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA0[7:0]	0x55	Byte 0 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA1[7:0]	0x56	Byte 1 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA2[7:0]	0x57	Byte 2 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA3[7:0]	0x58	Byte 3 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA4[7:0]	0x59	Byte 4 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA5[7:0]	0x5A	Byte 5 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA6[7:0]	0x5B	Byte 6 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA7[7:0]	0x5C	Byte 7 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA8[7:0]	0x5D	Byte 8 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA9[7:0]	0x5E	Byte 9 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA10[7:0]	0x5F	Byte 10 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA11[7:0]	0x60	Byte 11 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA12[7:0]	0x61	Byte 12 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA13[7:0]	0x62	Byte 13 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA14[7:0]	0x63	Byte 14 of message in Frame Buffer 1

CEC_BUF1_RX_FRAME_LENGTH[4:0], Addr 80 (CEC), Address 0x64[4:0] (Read Only)

Function

CEC_BUF1_RX_FRAME_LENGTH[4:0]	Description
xxxxx	The total number of bytes (including header byte) that were received into buffer 1

CEC_CLR_RX_RDY1, Addr 80 (CEC), Address 0x2C[2] (Self-Clearing)

Clear control for CEC_RX_RDY1.

Function

CEC_CLR_RX_RDY1	Description
0 (default)	Retain the value of the CEC_ RX_RDY1 flag
1	Clear the value of the CEC_RX_RDY1 flag

Table 71. CEC Incoming Frame Buffer 2 Registers

Register Name	CEC Map Address	Description
CEC_BUF2_RX_FRAME_HEADER[7:0]	0x65	Header of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA0[7:0]	0x66	Byte 0 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA1[7:0]	0x67	Byte 1 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA2[7:0]	0x68	Byte 2 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA3[7:0]	0x69	Byte 3 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA4[7:0]	0x6A	Byte 4 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA5[7:0]	0x6B	Byte 5 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA6[7:0]	0x6C	Byte 6 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA7[7:0]	0x6D	Byte 7 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA8[7:0]	0x6E	Byte 8 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA9[7:0]	0x6F	Byte 9 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA10[7:0]	0x70	Byte 10 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA11[7:0]	0x71	Byte 11 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA12[7:0]	0x72	Byte 12 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA13[7:0]	0x73	Byte 13 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA14[7:0]	0x74	Byte 14 of message in Frame Buffer 2

CEC_BUF2_RX_FRAME_LENGTH[4:0], Addr 80 (CEC), Address 0x75[4:0] (Read Only)

Function

CEC_BUF2_RX_FRAME_LENGTH[4:0]	Description
xxxxx	The total number of bytes (including header byte) that were received into buffer 2

CEC_CLR_RX_RDY2, Addr 80 (CEC), Address 0x2C[3] (Self-Clearing)

Clear control for CEC_RX_RDY2.

Function

CEC_CLR_RX_RDY2	Description
0 (default)	Retain the value of the CEC_RX_RDY2 flag
1	Clear the value of the CEC_RX_RDY2 flag

CEC Message Reception Overview

This section describes how messages are received and stored when only one frame buffer is enabled (default condition).

1. Initially the receive buffer (Buffer 0) is empty.
2. A message is received and stored in receive buffer 0, and CEC_BUF0_TIMESTAMP is set to 0b01. If the corresponding interrupt mask bit is set CEC_RX_RDY0_ST goes high and an interrupt is generated to alert the host processor that a message has been received. No more messages can be received until the processor reads out the received message.
3. The host processor responds to the interrupt, or polls the CEC_BUF0_TIMESTAMP register and realizes a message has been received, and reads receive buffer 0. Once the message is read the processor sets CEC_RX_RDY0_CLR which resets the buffer 0 timestamp to 0b00 and will also clear the buffer 0 status bit (if applicable). The CEC module is now ready to receive the next incoming message.

This section describes how messages are received and stored, how the time stamps are generated, and what happens when the host reads a received message when all three frame buffers are enabled.

1. Initially all buffers are empty and all time stamps are 0b00.
2. A message is received and stored in receive buffer 0, and CEC_BUF0_TIMESTAMP is set to 0b01. If the corresponding interrupt mask bit is set CEC_RX_RDY0_ST goes high and an interrupt is generated to alert the host processor that a message has been received.
3. Another message is received and stored in Receive Buffer 1, and CEC_BUF1_TIMESTAMP is set to 0b10. If the corresponding interrupt mask bit is set CEC_RX_RDY1_ST goes high and an interrupt is generated to alert the host processor that a message has been received.
4. The host processor responds to the interrupts, or polls the timestamps and realizes that messages have been received, and reads the three time stamps to determine which receive buffer to read first. The buffer with the earliest time stamp should be read first, so in this example the processor should read Receive Buffer 0 first. Once the message has been read the processor sets CEC_RX_RDY0_CLR, which resets the Buffer 0 timestamp to 0b00 and will also clear the buffer 0 status bit (if applicable).

5. Another message is received. The receiver module checks to see which of the three buffers are available, starting with Buffer 0. In this example, Buffer 0 has been read out already by the host processor and is available so the new message is stored in Receive Buffer 0. At this time the timestamp for Receive Buffer 1 is adjusted to 0b01 to show that it contains the first received message, and a timestamp of 0b10 is assigned to Receive Buffer 0 to show that it contains the second received message. If the corresponding interrupt mask bit is set the CEC_RX_RDY0_ST bit goes high and an interrupt is generated to alert the host processor that a message has been received.
6. Another message is received. This message is stored in Receive Buffer 2 (Buffer 0 and Buffer 1 are full). Time stamp 0b11 is assigned to Receive Buffer 2 to show that it contains an unread message that was the third to be received. If the corresponding interrupt mask bit is set the CEC_RX_RDY2_ST bit goes high and an interrupt is generated to alert the host processor that a message has been received. At this time all receive buffers are full and no more messages can be received until the processor reads at least one message.
7. The host processor responds to the interrupts, or polls the timestamps and realizes that messages have been received, and reads the three time stamps. The buffer with the earliest time stamp should be read first, therefore Receive Buffer 1 is read first, followed by Receive Buffer 0 and then Receive Buffer 2. Once the messages are read the processor sets CEC_RX_RDY0_CLR, CEC_RX_RDY1_CLR, and CEC_RX_RDY2_CLR. The time stamps for all three buffers are reset to 0b00.

ANTIGLITCH FILTER MODULE

This module is used to remove any glitches on the CEC bus to make the CEC input signal cleaner before it enters the CEC module. The glitch filter is programmable through the CEC_GLITCH_FILTER_CTRL register. The register value specifies the minimum pulse width that will be passed through by the module. Any pulses with narrower widths will be rejected. There is a CEC_GLITCH_FILTER_CTRL + 1 number of clock delays introduced by the antiglitch filter.

CEC_GLITCH_FILTER_CTRL[5:0], Addr 80 (CEC), Address 0x2B[5:0]

The CEC input signal is sampled by the input clock (XTAL clock). CEC_GLITCH_FILTER_CTRL specifies the minimum pulse width requirement in input clock cycles. Pulses of widths less than the minimum specified width are considered glitches and will be removed by the filter.

Function

CEC_GLITCH_FILTER_CTRL[5:0]	Description
000000	Disable the glitch filter
000001	Filter out pulses with width less than 1 clock cycle
000010	Filter out pulses with width less than 2 clock cycles
…	…
000111 (default)	Filter out pulses with width less than 7 clock cycles
…	…
111111	Filter out pulses with width less than 63 clock cycles

TYPICAL OPERATION FLOW

This section describes the algorithm that should be implemented in the host processor controlling the CEC module.

Initializing CEC Module

Figure 65 shows the flow that can be implemented in the host processor controlling the ADV7619 to initialize the CEC module.

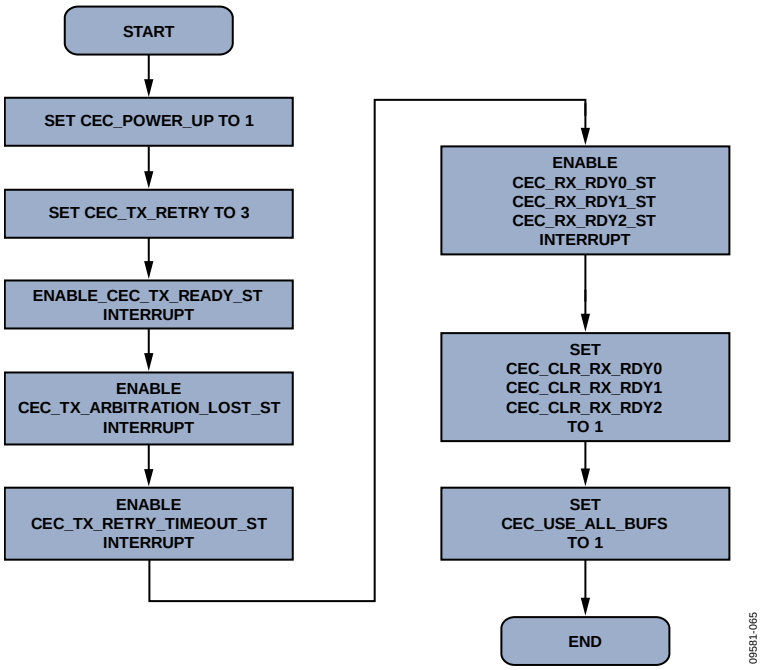


Figure 65. CEC Module Initialization

Using CEC Module as Initiator

Figure 66 shows the algorithm that can be implemented in the host processor controlling the ADV7619 to use the CEC module as an initiator.

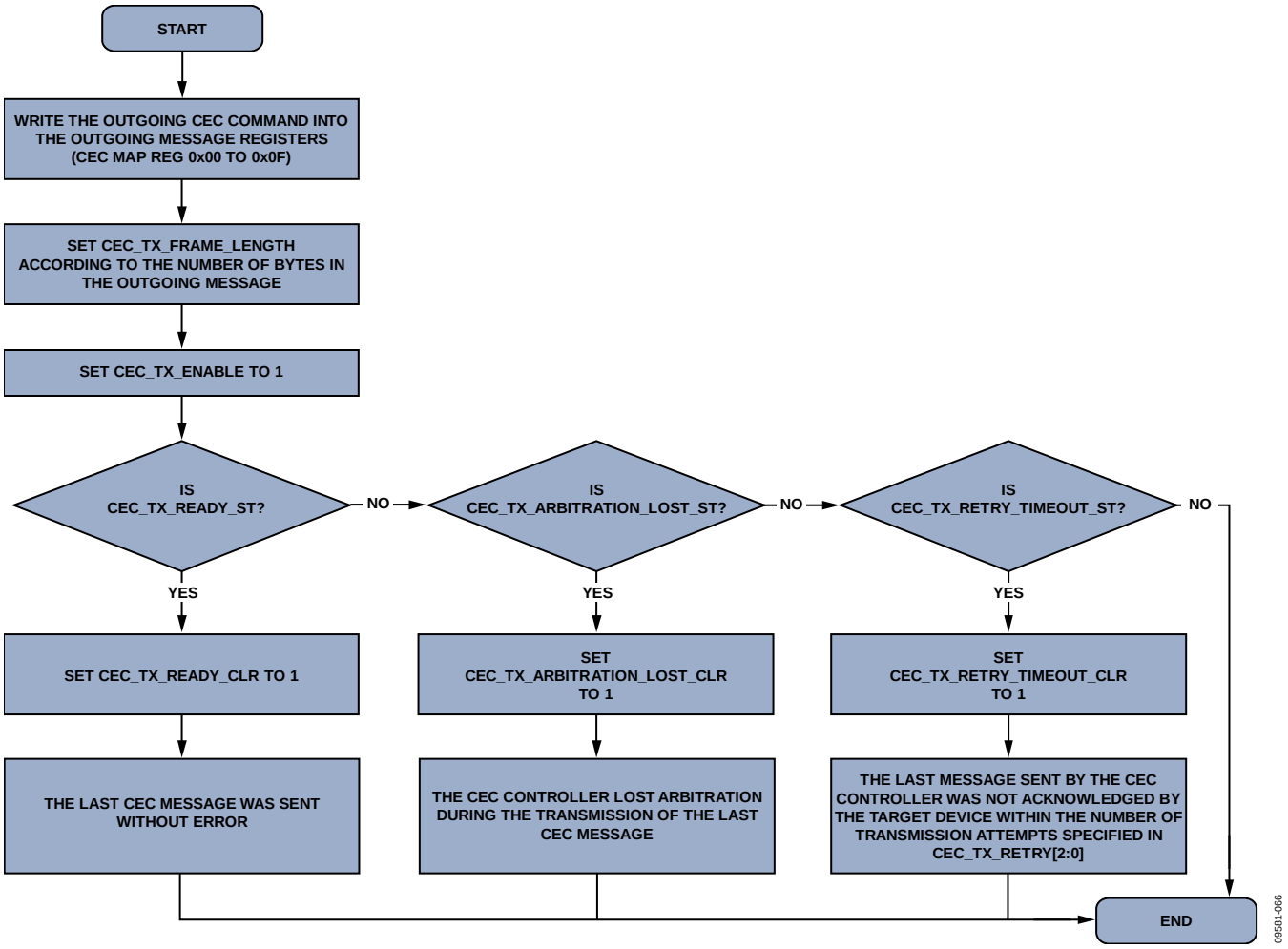


Figure 66. Using CEC Module as Initiator

Using CEC Module as Follower

Figure 67 shows the algorithm that can be implemented in the host processor controlling the ADV7619 to use the CEC module as a follower.

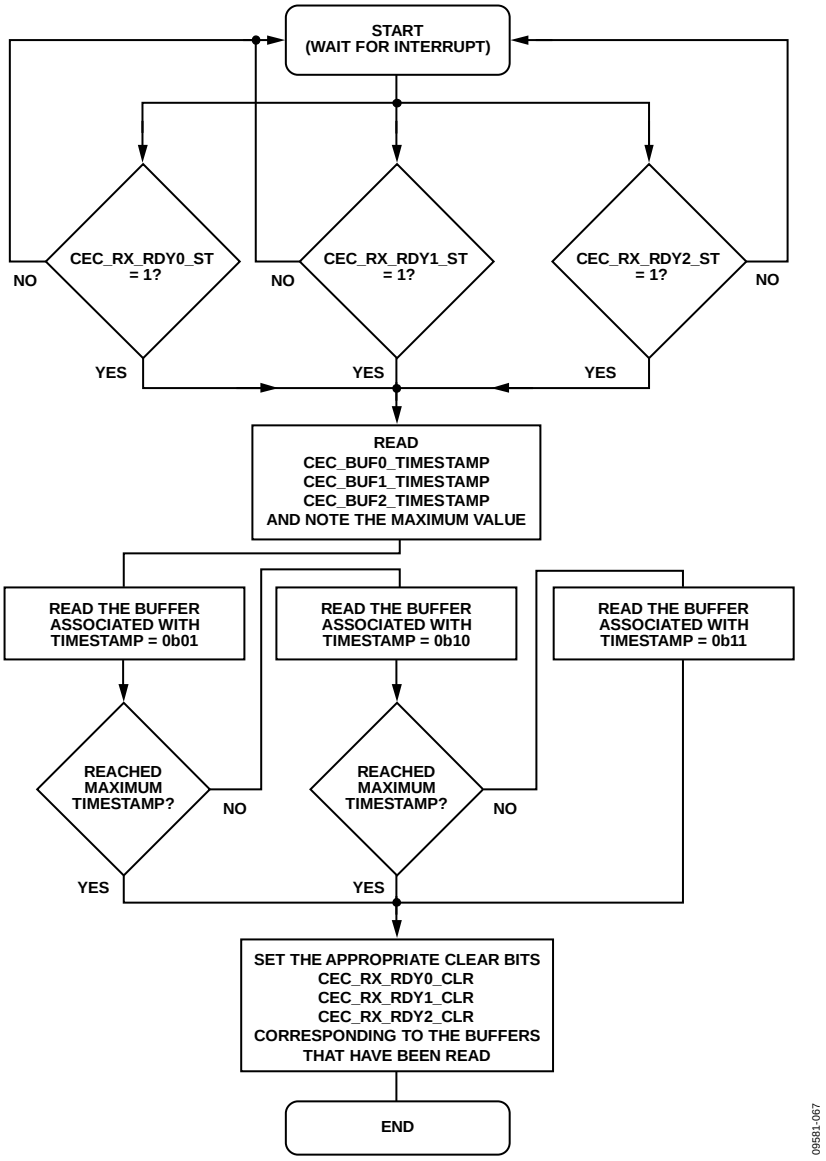


Figure 67. Using CEC Module as Follower

LOW POWER CEC MESSAGE MONITORING

The ADV7619 can be programmed to monitor the CEC line for messages that contain specific, user-programable opcodes. These are referred to as "WAKE_OPCODEs" as they allow the system to go into a low power or sleep mode and be woken up when an opcode of interest is received, without the host processor having to check each received message.

The default values of the wake_opcode registers are detailed in this section. All of these registers can be overwritten as required by the host processor.

For each of the 8 WAKE_OPCODE registers there is a corresponding raw flag, a status bit and a clear bit. If one of the WAKE_OPCODEs is received the corresponding raw flag will go high for a brief period of time. If the appropriate interrupt mask bit is set the status bit will go high and remain high until cleared by the clear bit, and an interrupt will also be generated.

CEC_WAKE_OPCODE0[7:0], Addr 80 (CEC), Address 0x78[7:0]

CEC_WAKE_OPCODE0

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE0[7:0]	Description
01101101 (default)	Power on
xxxxxxxx	User specified OPCODE to respond to

CEC_WAKE_OPCODE1[7:0], Addr 80 (CEC), Address 0x79[7:0]

CEC_WAKE_OPCODE1

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE1[7:0]	Description
10001111 (default)	Give power status
xxxxxxxx	User specified OPCODE to respond to

CEC_WAKE_OPCODE2[7:0], Addr 80 (CEC), Address 0x7A[7:0]

CEC_WAKE_OPCODE2

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE2[7:0]	Description
10000010 (default)	Active source
xxxxxxxx	User specified OPCODE to respond to

CEC_WAKE_OPCODE3[7:0], Addr 80 (CEC), Address 0x7B[7:0]

CEC_WAKE_OPCODE3

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE3[7:0]	Description
00000100 (default)	Image view on
xxxxxxxx	User specified OPCODE to respond to

CEC_WAKE_OPCODE4[7:0], Addr 80 (CEC), Address 0x7C[7:0]

CEC_WAKE_OPCODE4

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE4[7:0]	Description
00001101 (default)	TEXT VIEW ON
xxxxxxxx	User specified OPCODE to respond to

CEC_WAKE_OPCODE5[7:0], Addr 80 (CEC), Address 0x7D[7:0]

CEC_WAKE_OPCODE5

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE5[7:0]	Description
01110000 (default)	SYSTEM AUDIO MODE REQUEST
xxxxxxxx	User specified OPCODE to respond to

CEC_WAKE_OPCODE6[7:0], Addr 80 (CEC), Address 0x7E[7:0]

CEC_WAKE_OPCODE6

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE6[7:0]	Description
01000010 (default)	DECK CONTROL
xxxxxxxx	User specified OPCODE to respond to

CEC_WAKE_OPCODE7[7:0], Addr 80 (CEC), Address 0x7F[7:0]

CEC_WAKE_OPCODE7

This value can be set to a CEC opcode that requires a response. On receipt of this opcode the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE7[7:0]	Description
01000001 (default)	PLAY
xxxxxxxx	User specified OPCODE to respond to

INTERRUPTS

INTERRUPT ARCHITECTURE OVERVIEW

The ADV7619 interrupt architecture provides four different types of bits, namely

- Raw bits
- Status bits
- Interrupt mask bits
- Clear bits

Raw bits are defined as being either edge-sensitive or level-sensitive. The following example compares AVI_INFO_RAW and NEW_AVI_INFO_RAW to demonstrate the difference.

AVI_INFO_RAW, IO, Address 0x60[0] (Read Only)

Raw status of AVI InfoFrame detected signal. This bit is set to one when an AVI InfoFrame is received and is reset to zero if no AVI InfoFrame is received for more than 7 VSyncs (on the eighth VSync leading edge following the last received AVI InfoFrame), after an HDMI packet detection reset or upon writing to AVI_PACKET_ID.

Function

AVI_INFO_RAW	Description
0 (default)	No AVI InfoFrame has been received within the last seven VSyncs or since the last HDMI packet detection reset
1	An AVI InfoFrame has been received within the last seven VSyncs

NEW_AVI_INFO_RAW, IO, Address 0x79[0] (Read Only)

Status of the new AVI InfoFrame interrupt signal. When set to 1, it indicates that an AVI InfoFrame has been received with new contents. Once set, this bit will remain high until the interrupt is cleared via NEW_AVI_INFO_CLR.

Function

NEW_AVI_INFO_RAW	Description
0 (default)	No new AVI InfoFrame received
1	AVI InfoFrame with new content received

In the case of AVI_INFO_RAW this bit always represents the current status of whether or not the part is receiving AVI InfoFrames. It is not a latched bit and never requires to be cleared. This is the definition of a level-sensitive raw bit.

In the case of NEW_AVI_INFO_RAW the same strategy would not work. If the NEW_AVI_INFO_RAW bit were to behave in the same way as AVI_INFO_RAW it would go high at the instant the new InfoFrame was received, and would go low again some clock cycles afterwards. This is because a new InfoFrame is only new the instant it is received, and once received it it no longer new, so the event to set this bit only last for an instant and is then gone.

Having a raw bit that is only held high for an instant is not useful. Therefore, for these types of events, the raw bit is latched, and must be cleared by the corresponding clear bit. Accordingly, the raw bit does not truly represent the current status; instead it represents the status of an edge event that happened in the past. This is the definition of an edge-sensitive raw bit.

All raw bits, with the exceptions of INTRQ_RAW and INTRQ2_RAW, have corresponding status bits. The status bits always work in the same manner whether the raw bit is edge or level sensitive. Status bits have the following characteristics

- A status bit must be enabled by setting either or both of the corresponding interrupt mask bits
- Status bits are always latched, and must be cleared by the corresponding clear bit.

When either of the interrupt mask bits for a given interrupt is set, if that raw bit changes state the corresponding status bit goes high and an interrupt is generated on the INT1 or INT2 pin, depending on which interrupt mask bit was set. The status bit must be cleared using the appropriate clear bit. The status bits, interrupt mask bits, and clear bits for AVI_INFO and NEW_AVI_INFO are described here for completeness.

AVI_INFO_ST, IO, Address 0x61[0] (Read Only)

Latched status of AVI_INFO_RAW signal. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set, this bit will remain high until the interrupt is cleared via AVI_INFO_CLR.

Function

AVI_INFO_ST	Description
0 (default)	AVI_INFO_RAW has not changed state
1	AVI_INFO_RAW has changed state

NEW_AVI_INFO_ST, IO, Address 0x7A[0] (Read Only)

Latched status for the NEW_AVI_INFO_RAW. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit. Once set, this bit will remain high until the interrupt is cleared via NEW_AVI_INFO_CLR.

Function

NEW_AVI_INFO_ST	Description
0 (default)	NEW_AVI_INFO_RAW has not changed state
1	NEW_AVI_INFO_RAW has changed state

AVI_INFO_CLR, IO, Address 0x62[0] (Self-Clearing)

Clear bit for AVI_INFO_RAW and AVI_INFO_ST bits.

Function

AVI_INFO_CLR	Description
0 (default)	No function
1	Clear AVI_INFO_RAW and AVI_INFO_ST

NEW_AVI_INFO_CLR, IO, Address 0x7B[0] (Self-Clearing)

Clear bit for NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST bits.

Function

NEW_AVI_INFO_CLR	Description
0 (default)	No function
1	Clear NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST

AVI_INFO_MB1, IO, Address 0x64[0]

INT1 interrupt mask for AVI InfoFrame detection interrupt. When set an AVI InfoFrame detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT1.

Function

AVI_INFO_MB1	Description
0 (default)	Disables AVI Info frame detection interrupt for INT1
1	Enables AVI Info frame detection interrupt for INT1

AVI_INFO_MB2, IO, Address 0x63[0]

INT2 interrupt mask for AVI InfoFrame detection interrupt. When set an AVI InfoFrame detection event will cause AVI_INFO_ST to be set and an interrupt will be generated on INT2.

Function

AVI_INFO_MB2	Description
0 (default)	Disables AVI Info frame detection interrupt for INT2
1	Enables AVI Info frame detection interrupt for INT2

NEW_AVI_INFO_MB1, IO, Address 0x7D[0]

INT1 interrupt mask for new AVI InfoFrame detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT1.

Function

NEW_AVI_INFO_MB1	Description
0 (default)	Disables new AVI InfoFrame interrupt for INT1
1	Enables new AVI InfoFrame interrupt for INT1

NEW_AVI_INFO_MB2, IO, Address 0x7C[0]

INT2 interrupt mask for new AVI InfoFrame detection interrupt. When set a new AVI InfoFrame detection event will cause NEW_AVI_INFO_ST to be set and an interrupt will be generated on INT2.

Function

NEW_AVI_INFO_MB2	Description
0 (default)	Disables new SPD InfoFrame interrupt for INT2
1	Enables new SPD InfoFrame interrupt for INT2

See Figure 68 through Figure 70.

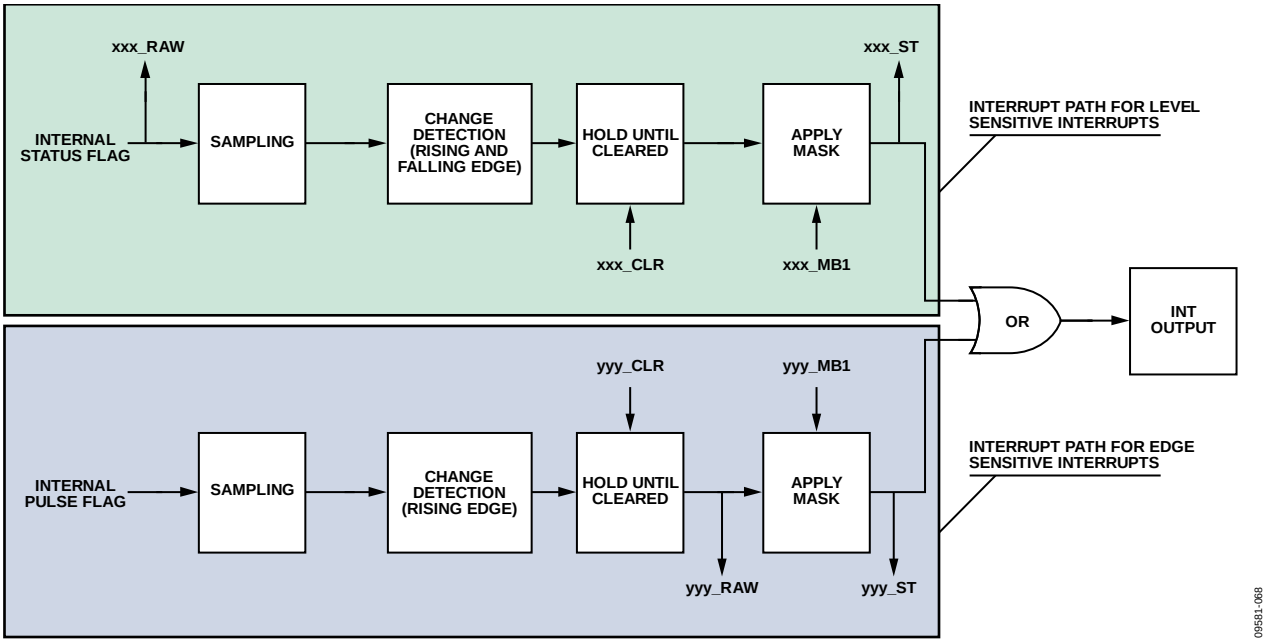


Figure 68. Level and Edge Sensitive Raw, Status and Interrupt Generation

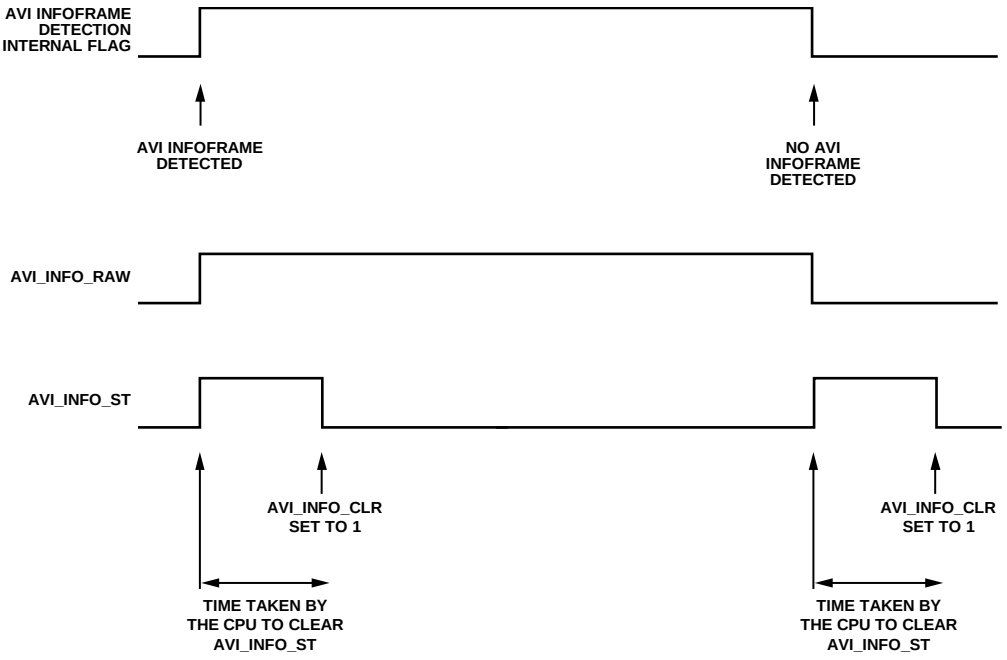


Figure 69. AVI_INFO_RAW and AVI_INFO_ST Timing

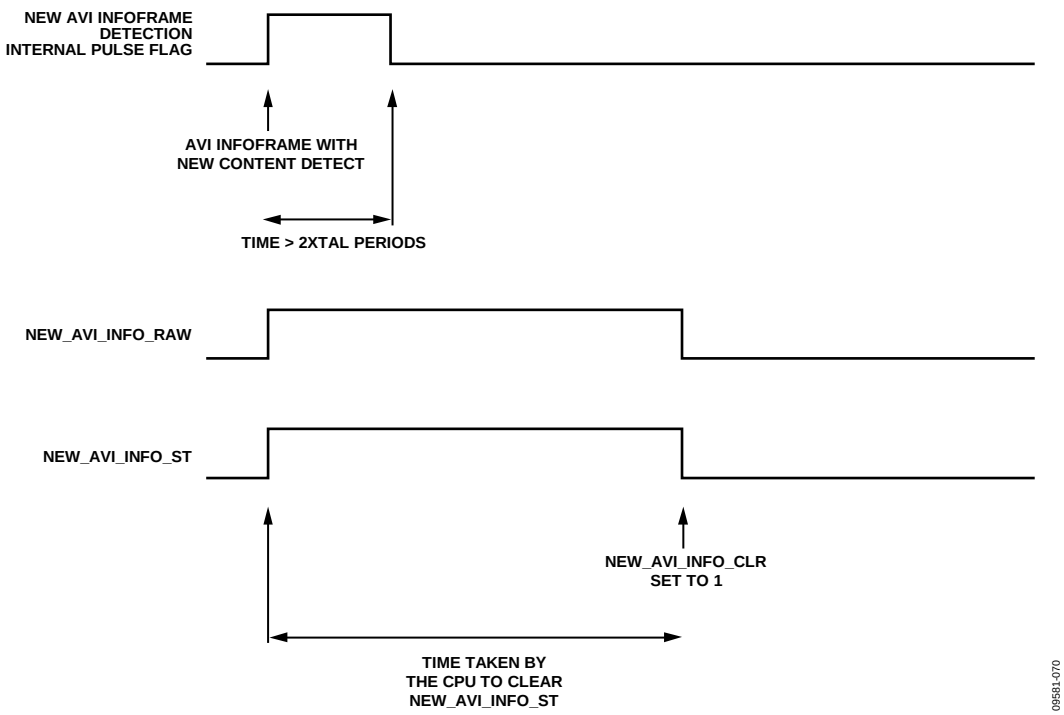


Figure 70. NEW_AVI_INFO_RAW and NEW_AVI_INFO_ST Timing

In this section, all raw bits are classified as being triggered by either level sensitive or edge sensitive events, with the following understanding of the terminology

- Level sensitive events are events that are generally either high or low and are not expected to change rapidly. The raw bit for level sensitive events is not latched and therefore always represents the true real-time status of the event in question.
- Edge sensitive events are events that only exist for an instant. The raw bits for edge sensitive events are latched and therefore represent the occurrence of an edge sensitive event that happened in the past. Raw bits for edge sensitive events must be cleared by the corresponding clear bit.

INTERRUPT PINS

The ADV7619 features two dedicated interrupt pins, INT1 and INT2. INT1 is always enabled, but INT2 is disabled by default and must be enabled using the following I²C control.

INTRQ2_MUX_SEL[1:0], IO, Address 0x41[1:0]

Interrupt signal configuration control for INT2

Function

INTRQ2_MUX_SEL[1:0]	Description
00 (default)	INT2 disabled
01	INT2 in MCLK/INT2 pin
10	INT2 in SCLK/INT2 pin
11	INT2 in HPA_A/INT2 pin

Notes

- INT1 is in a high impedance state after reset as the ADV7619 resets with open drain enabled on INT1.
- The ADV7619 resets with the INT2 disabled. The **INTRQ2_MUX_SEL[1:0]** bit in the IO map must be set in order to enable the INT2 function on the one of the pins: MCLK/INT2, SCLK/INT2, HPA_A/INT2.
- The ADV7619 resets with all interrupts masked off on INT1 and INT2.
- An interrupt is enabled for a specific event by masking the corresponding mask bit in the IO map.

Interrupt Duration

The interrupt duration can be programmed independently for INT1 and INT2. When an interrupt event occurs, the interrupt pin INT1 or INT2 becomes active with a programmable duration as described below.

INTRQ_DUR_SEL[1:0], IO, Address 0x40[7:6]

A control to select the interrupt signal duration for the interrupt signal on INT1.

Function

INTRQ_DUR_SEL[1:0]	Description
00 (default)	4 Xtal periods
01	16 Xtal periods
10	64 Xtal periods
11	Active until cleared

INTRQ2_DUR_SEL[1:0], IO, Address 0x41[7:6]

A control to select the interrupt signal duration for the interrupt signal on INT2.

Function

INTRQ2_DUR_SEL[1:0]	Description
00 (default)	4 Xtal periods
01	16 Xtal periods
10	64 Xtal periods
11	Active until cleared

Interrupt Drive Level

The drive level of INT1 and INT2 can be programmed as described below.

INTRQ_OP_SEL[1:0], IO, Address 0x40[1:0]

Interrupt signal configuration control for INT1.

Function

INTRQ_OP_SEL[1:0]	Description
00 (default)	Open drain
01	Drives low when active
10	Drives high when active
11	Disabled

INT2_POL, IO, Address 0x41[2]

INT2 polarity control.

Function

INT2_POL	Description
0 (default)	INT2 high when active
1	INT2 low when active

Interrupt Manual Assertion

It is possible to manually generate an interrupt on the INT1 and INT2 pins by setting MPU_STIM_INTRQ. This feature is designed for debug use and not intended for use in normal operation. The appropriate mask bit must be set to generate an interrupt at the pin.

MPU_STIM_INTRQ, IO, Address 0x40[2]

Manual interrupt set control. This feature should be used for test purposes only. Note that the appropriate mask bit must be set to generate an interrupt at the pin.

Function

MPU_STIM_INTRQ	Description
0 (default)	Disables manual interrupt mode
1	Enables manual interrupt mode

MPU_STIM_INTRQ_MB1, IO, Address 0x4B[7]

INT1 interrupt mask for manual forced interrupt signal. When set the manual forced interrupt will trigger the INT1 interrupt and MPU_STIM_INTRQ_ST will indicate the interrupt status.

Function

MPU_STIM_INTRQ_MB1	Description
0 (default)	Disables manual forced interrupt for INT1
1	Enables manual forced interrupt for INT1

MPU_STIM_INTRQ_MB2, IO, Address 0x4A[7]

INT2 interrupt mask for manual forced interrupt signal. When set the manual forced interrupt will trigger the INT2 interrupt and MPU_STIM_INTRQ_ST will indicate the interrupt status.

Function

MPU_STIM_INTRQ_MB2	Description
0 (default)	Disables manual forced interrupt for INT2
1	Enables manual forced interrupt for INT2

Multiple Interrupt Events

If an interrupt event occurs, and then a second interrupt event occurs before the system controller has cleared or masked the first interrupt event, the ADV7619 does not generate a second interrupt signal. The system controller should check all unmasked interrupt status bits as more than one may be active.

Table 72 lists the interrupt registers available and a brief description of their functions. For more details on the functionality of these interrupt registers, refer to the ADV7619 Software Manual. Refer to the IO map section of the ADV7619 Software Manual for details of the CP core interrupts and HDMI core interrupts.

Table 72. Interrupt Functions Available in ADV7619

Interrupt Register	Location	Description
Interrupt Status 1	IO Map, Address 0x43	CP interrupt status for STDI
Interrupt Status 2	IO Map, Address 0x48	CP interrupt status forces manual interrupt
Interrupt Status 6	IO Map, Address 0x5C	STDI channels interrupt status
HDMI Lvl Int Status 1	IO Map, Address 0x61	HDMI interrupt status for HDMI InfoFrame packets
HDMI Lvl Int Status 2	IO Map, Address 0x66	HDMI interrupt status for audio processing changes
HDMI Lvl Int Status 3	IO Map, Address 0x6B	HDMI interrupt status for HDMI video parameters and cable detection
HDMI Lvl Int Status 4	IO Map, Address 0x70	HDMI interrupt status for cable detection and encryption
HDMI Edg Int Status 1	IO Map, Address 0x7A	HDMI interrupt status for newly received HDMI InfoFrame packets
HDMI Edg Int Status 2	IO Map, Address 0x7F	HDMI interrupt status for audio FIFO, clock regeneration and packet errors
HDMI Edg Int Status 3	IO Map, Address 0x84	HDMI interrupt status for updates in deep color, video, AKSV, and audio
HDMI Edg Int Status 4	IO Map, Address 0x89	HDMI interrupt status for changes in InfoFrame checksum errors
HDMI Edg Int Status 5	IO Map, Address 0x8E	HDMI interrupt status for background measurements and changes in Inforframe checksum error

DESCRIPTION OF INTERRUPT BITS

This section lists all the raw bits in the IO map of the ADV7619 by category, and states whether the bit is an edge or level sensitive bit. A basic explanation for each bit is provided in the software manual and/or in the corresponding section of the hardware manual. For certain interrupts that require additional explanations, these are provided in the Additional Explanations section.

General Operation

- INTRQ_RAW (level sensitive event)
- INTRQ2_RAW (level sensitive event)
- MPU_STIM_INTRQ_RAW (edge sensitive event)

HDMI Video Mode

- STDI_DATA_VALID_RAW (edge/level sensitive event; programmable).
- STDI_DVALID_CH1_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7619 ES1.
- CP_UNLOCK_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7619 ES1.
- CP_UNLOCK_CH1_RAW (edge/level sensitive event; programmable). Edge sensitive event on ADV7619 ES1.
- CP_LOCK_RAW (edge/level sensitive event; programmable).Edge sensitive event on ADV7619 ES1.
- CP_LOCK_CH1_RAW (edge/level sensitive event; programmable).Edge sensitive event on ADV7619 ES1.

CEC

The following raw bits are all related to CEC operation and are all edge sensitive events; it is, therefore, necessary to clear these bits.

- CEC_RX_RDY2_RAW
- CEC_RX_RDY1_RAW
- CEC_RX_RDY0_RAW
- CEC_TX_RETRY_TIMEOUT_RAW
- CEC_TX_ARBITRATION_LOST_RAW
- CEC_TX_READY_RAW
- CEC_INTERRUPT_BYTE[7:0]

HDMI Only Mode

The following raw bits are all related to HDMI operation and are based on level sensitive events; it is, therefore, not necessary to clear these bits.

- ISRC2_PCKT_RAW
- ISRC1_PCKT_RAW
- ACP_PCKT_RAW
- VS_INFO_RAW
- MS_INFO_RAW
- SPD_INFO_RAW
- AUDIO_INFO_RAW
- AVI_INFO_RAW
- CS_DATA_VALID_RAW
- INTERNAL_MUTE_RAW
- AV_MUTE_RAW
- AUDIO_CH_MD_RAW
- HDMI_MODE_RAW
- GEN_CTL_PCKT_RAW
- AUDIO_C_PCKT_RAW
- GAMUT_MDATA_RAW
- TMDSPLL_LCK_A_RAW
- TMDSPLL_LCK_B_RAW
- TMDS_CLK_A_RAW
- TMDS_CLK_B_RAW
- HDMI_ENCRPT_A_RAW

- HDMI_ENCRPT_B_RAW
- CABLE_DET_A_RAW
- CABLE_DET_B_RAW
- V_LOCKED_RAW
- DE_REGEN_LCK_RAW
- VIDEO_3D_RAW
- RI_EXPIRED_A_RAW
- RI_EXPIRED_B_RAW

The following raw bits are all related to HDMI operation and are based on edge sensitive events; it is, therefore, necessary to clear these bits using the corresponding clear bit.

- NEW_ISRC2_PCKT_RAW
- NEW_ISRC1_PCKT_RAW
- NEW_ACP_PCKT_RAW
- NEW_VS_INFO_RAW
- NEW_MS_INFO_RAW
- NEW_SPD_INFO_RAW
- NEW_AUDIO_INFO_RAW
- NEW_AVI_INFO_RAW
- NEW_GAMUT_MDATA_RAW
- FIFO_NEAR_OVFL_RAW
- FIFO_NEAR_UFLO_RAW
- FIFO_UNDERFLO_RAW
- FIFO_OVERFLO_RAW
- CTS_PASS_THRSH_RAW
- CHANGE_N_RAW
- PACKET_ERROR_RAW
- AUDIO_PCKT_ERR_RAW
- DEEP_COLOR_CHNG_RAW
- VCLK_CHNG_RAW
- AUDIO_MODE_CHNG_RAW
- PARITY_ERROR_RAW
- NEW_SAMP_RT_RAW
- AUDIO_FLT_LINE_RAW
- NEW_TMDS_FRQ_RAW
- MS_INF_CKS_ERR_RAW
- SPD_INF_CKS_ERR_RAW
- AUD_INF_CKS_ERR_RAW
- AVI_INF_CKS_ERR_RAW
- AKSV_UPDATE_A_RAW
- AKSV_UPDATE_B_RAW
- BG_MEAS_DONE_RAW
- VS_INF_CKS_ERR_RAW

ADDITIONAL EXPLANATIONS

STDI_DATA_VALID_RAW

STDI_DATA_VALID_RAW is programmable as either an edge sensitive bit or a level sensitive bit using the following control. Note that this control also configures whether an interrupt is generated only on the rising edge of STDI_DATA_VALID_RAW or on both edges.

STDI_DATA_VALID_EDGE_SEL, IO, Address 0x41[4]

A control to configure the functionality of the STDI_DATA_VALID interrupt. The interrupt can be generated for the case when STDI changes to an STDI valid state. Alternatively, it can be generated to indicate a change in STDI_VALID status.

Function

STDI_DATA_VALID_EDGE_SEL	Description
0	Generate interrupt for a low to high change in STDI_VALID status
1 (default)	Generate interrupt for a low to high or a high to low change in STDI_VALID status

CP_LOCK, CP_UNLOCK

CP_UNLOCK_RAW is programmable as either an edge sensitive bit or a level sensitive bit using the following control. Note that this control also configures whether an interrupt is generated only on the rising edge of CP_UNLOCK_RAW, or on both edges.

CP_LOCK_UNLOCK_EDGE_SEL, IO, Address 0x41[5]

A control to configure the functionality of the CP_LOCK, CP_UNLOCK interrupts.

Function

CP_LOCK_UNLOCK_EDGE_SEL	Description
0	Generate interrupt for a low to high change in CP_LOCK,UNLOCK status for Ch1.
1 (default)	Generate interrupt for a low to high or a high to low change in CP_LOCK,UNLOCK status for Ch1.

CP_LOCK_ST, IO, Address 0x43[2] (Read Only)

For a detailed description of this function, see the entry in the List of Interrupt Status Registers section.

CP_UNLOCK_ST, IO, Address 0x43[3] (Read Only)

For a detailed description of this function, see the entry in the List of Interrupt Status Registers section.

HDMI Interrupts Validity Checking Process

All HDMI interrupts have a set of conditions that must be taken into account for validation in the display firmware. When the ADV7619 interrupts the display controller for an HDMI interrupt, the host must check that all validity conditions for that interrupt are met before processing that interrupt.

For simplicity, HDMI interrupts can be subdivided into three groups, as listed in the following sections.

Group 1 HDMI Interrupts

The interrupts listed in Table 73 are valid irrespective of the mode in which the ADV7619 is configured, that is: HDMI mode (PRIM_MODE set to values 0x05 or 0x06).

Table 73. HDMI Interrupts Group 1

Interrupts
TMDS_CLK_A
TMDS_CLK_B
CABLE_DET_A
CABLE_DET_B

Group 2 HDMI Interrupts

The interrupts listed in Table 74 are valid on the condition that the ADV7619 is configured in HMDI mode.

Table 74. HDMI Interrupts Group 2

Interrupts
INTERNAL_MUTE
VIDEO_PLL_LCK
AKSV_UPDATE

Group 3 HDMI Interrupts

The interrupts listed in Table 75 are valid under the following conditions:

- ADV7619 is configured in HMDI mode
- TMDS_CLK_A_RAW is set to 1 if Port A is the active HDMI port
- TMDS_CLK_B_RAW is set to 1 if Port B is the active HDMI port
- TMDSPLL_LCK_A_RAW is set to 1

Table 75. HDMI Interrupts Group 3

Interrupts
ISRC2_PCKT
ISRC1_PCKT
ACP_PCKT
VS_INFO
MS_INFO
SPD_INFO
AUDIO_INFO
AVI_INFO
CS_DATA_VALID
AV_MUTE
AUDIO_CH_MD
AUDIO_MODE_CHNG
GEN_CTL_PCKT
AUDIO_C_PCKT
GAMUT_MDATA
V_LOCKED
DE_REGEN_LCK
HDMI_MODE
HDMI_ENCRPT_A
HDMI_ENCRPT_B
NEW_ISRC2_PCKT
NEW_ISRC1_ PCKT
NEW_ACP_PCKT
NEW_VS_INFO
NEW_MS_INFO
NEW_SPD_INFO
NEW_AUDIO_INFO
NEW_AVI_INFO
FIFO_NEAR_OVFL
CTS_PASS_THRSH
CHANGE_N
PACKET_ERROR
AUDIO_PCKT_ERR
NEW_GAMUT_MDATA
DEEP_COLOR_CHNG
VCLK_CHNG
PARRITY_ERROR
NEW_SAMP_RT
AUDIO_FLT_LINE
NEW_TMDS_FRQ
FIFO_NEAR_UFLO
VIDEO_3D_RAW
RI_EXPIRED_B_RAW
RI_EXPIRED_A_RAW

Storing Masked Interrupts

STORE_UNMASKED_IRQS, IO, Address 0x40[4]

STORE_MASKED_IRQS allows the HDMI status flags for any HDMI interrupt to be triggered regardless of whether the mask bits are set. This bit allows a HDMI interrupt to trigger and allows this interrupt to be read back through the corresponding status bit without triggering an interrupt on the interrupt pin. The status is stored until the clear bit is used to clear the status register and allows another interrupt to occur.

Function

STORE_UNMASKED_IRQS	Description
0 (default)	Does not allow x_ST flag of any HDMI interrupt to be set independently of mask bits
1	Allows x_ST flag of any HDMI interrupt to be set independently of mask bits

List of Interrupt Status Registers

INTERRUPT_STATUS_1 register consists of fields: STDI_DATA_VALID_ST, CP_UNLOCK_ST, and CP_LOCK_ST.

STDI_DATA_VALID_ST, IO, Address 0x43[4] (Read Only)

Latched signal status of STDI valid interrupt signal. Once set, this bit will remain high until the interrupt is cleared via STDI_DATA_VALID_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

STDI_DATA_VALID_ST	Description
0 (default)	No STDI valid interrupt has occurred.
1	A STDI valid interrupt has occurred.

CP_UNLOCK_ST, IO, Address 0x43[3] (Read Only)

Latched signal status of CP Unlock interrupt signal. Once set, this bit will remain high until the interrupt is cleared via CP_UNLOCK_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

CP_UNLOCK_ST	Description
0 (default)	No CP UNLOCK interrupt event has occurred.
1	A CP UNLOCK interrupt event has occurred.

CP_LOCK_ST, IO, Address 0x43[2] (Read Only)

Latched signal status of the CP lock interrupt signal. Once set, this bit will remain high until the interrupt is cleared via CP_LOCK_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

CP_LOCK_ST	Description
0 (default)	No CP LOCK interrupt event has occurred.
1	A CP LOCK interrupt event has occurred.

INTERRUPT_STATUS_2 register consists of one field: MPU_STIM_INTRQ_ST.

MPU_STIM_INTRQ_ST, IO, Address 0x48[7] (Read Only)

Latched signal status of manual forced interrupt signal. Once set, this bit will remain high until the interrupt is cleared via MPU_STIM_INTRQ_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

MPU_STIM_INTRQ_ST	Description
0 (default)	Forced manual interrupt event has not occurred.
1	Force manual interrupt even has occurred.

INTERRUPT_STATUS_6 register consists of fields: CP_LOCK_CH1_ST, CP_UNLOCK_CH1_ST, and STDI_DVALID_CH1_ST.

CP_LOCK_CH1_ST, IO, Address 0x5C[3] (Read Only)

Function

CP_LOCK_CH1_ST	Description
0 (default)	No change. An interrupt has not been generated from this register.
1	Channel 1 CP input has caused the decoder to go from an unlocked state to a locked state.

CP_UNLOCK_CH1_ST, IO, Address 0x5C[2] (Read Only)

Function

CP_UNLOCK_CH1_ST	Description
0 (default)	No change. An interrupt has not been generated from this register.
1	Channel 1 CP input has changed from a locked state to an unlocked state and has triggered an interrupt.

STDI_DVALID_CH1_ST, IO, Address 0x5C[1] (Read Only)

Latched signal status of STDI valid for Sync Channel 1 interrupt signal. Once set, this bit will remain high until the interrupt is cleared via STDI_DATA_VALID_CH1_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

STDI_DVALID_CH1_ST	Description
0 (default)	No STDI valid for sync Channel 1 interrupt has occurred.
1	A STDI valid for sync Channel 1 interrupt has occurred.

HDMI Lvl INT Status 1 register consists of fields: ISRC2_PCKT_ST, ISRC1_PCKT_ST, ACP_PCKT_ST, VS_INFO_ST, MS_INFO_ST, SPD_INFO_ST, and AUDIO_INFO_ST.

ISRC2_PCKT_ST, IO, Address 0x61[7] (Read Only)

Latched status of ISRC2 packet detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via ISRC2_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

ISRC2_PCKT_ST	Description
0 (default)	No interrupt generated from this register.
1	ISRC2_PCKT_RAW has changed. Interrupt has been generated.

ISRC1_PCKT_ST, IO, Address 0x61[6] (Read Only)

Latched status of ISRC1 packet detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via ISRC1_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

ISRC1_PCKT_ST	Description
0 (default)	No interrupt generated from this register.
1	ISRC1_PCKT_RAW has changed. Interrupt has been generated.

ACP_PCKT_ST, IO, Address 0x61[5] (Read Only)

Latched status of audio content protection packet detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via ACP_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

ACP_PCKT_ST	Description
0 (default)	No interrupt generated from this register.
1	ACP_PCKT_RAW has changed. Interrupt has been generated.

VS_INFO_ST, IO, Address 0x61[4] (Read Only)

Latched status of vendor specific InfoFrame detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via VS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

VS_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	VS_INFO_RAW has changed. Interrupt has been generated.

MS_INFO_ST, IO, Address 0x61[3] (Read Only)

Latched status of MPEG source InfoFrame detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via MS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

MS_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	MS_INFO_RAW has changed. Interrupt has been generated.

SPD_INFO_ST, IO, Address 0x61[2] (Read Only)

Latched status of SPD InfoFrame detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via SPD_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

SPD_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	SPD_INFO_RAW has changed. Interrupt has been generated.

AUDIO_INFO_ST, IO, Address 0x61[1] (Read Only)

Latched status of audio InfoFrame detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via AUDIO_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AUDIO_INFO_ST	Description
0 (default)	No interrupt generated from this register.
1	AUDIO_INFO_RAW has changed. Interrupt has been generated.

AVI_INFO_ST, IO, Address 0x61[0] (Read Only*)*

For a detailed description, see the entry in the Interrupt Architecture Overview section.

HDMI Lvl INT Status 2 is an 8-bit register 0x66[7:0].

HDMI Lvl INT Status 2 register consists of fields: CS_DATA_VALID_ST, INTERNAL_MUTE_ST, AV_MUTE_ST, AUDIO_CH_MD_ST, HDMI_MODE_ST, GEN_CTL_PCKT_ST, AUDIO_C_PCKT_ST, and GAMUT_MDATA_ST.

CS_DATA_VALID_ST, IO, Address 0x66[7] (Read Only)

Latched status of channel status data valid interrupt signal. Once set, this bit will remain high until the interrupt is cleared via ICS_DATA_VALID_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

CS_DATA_VALID_ST	Description
0 (default)	CS_DATA_VALID_RAW has not changed. An interrupt has not been generated.
1	CS_DATA_VALID_RAW has changed. An interrupt has been generated.

INTERNAL_MUTE_ST, IO, Address 0x66[6] (Read Only)

Latched status of internal mute interrupt signal. Once set, this bit will remain high until the interrupt is cleared via INTERNAL_MUTE_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

INTERNAL_MUTE_ST	Description
0 (default)	INTERNAL_MUTE_RAW has not changed. An interrupt has not been generated.
1	INTERNAL_MUTE_RAW has changed. An interrupt has been generated.

AV_MUTE_ST, IO, Address 0x66[5] (Read Only)

Latched status of AV mute detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via AV_MUTE_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AV_MUTE_ST	Description
0 (default)	AV_MUTE_RAW has not changed. An interrupt has not been generated.
1	AV_MUTE_RAW has changed. An interrupt has been generated.

AUDIO_CH_MD_ST, IO, Address 0x66[4] (Read Only)

Latched status of audio channel mode interrupt signal. Once set, this bit will remain high until the interrupt is cleared via AUDIO_CH_MD_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AUDIO_CH_MD_ST	Description
0 (default)	AUDIO_CH_MD_RAW has not changed. An interrupt has not been generated.
1	AUDIO_MODE_CHNG_RAW has changed. An interrupt has been generated.

HDMI_MODE_ST, IO, Address 0x66[3] (Read Only)

Latched status of HDMI mode interrupt signal. Once set, this bit will remain high until the interrupt is cleared via HDMI_MODE_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

HDMI_MODE_ST	Description
0 (default)	HDMI_MODE_RAW has not changed. An interrupt has not been generated.
1	(No Suggestions) has changed. An interrupt has been generated.

GEN_CTL_PCKT_ST, IO, Address 0x66[2] (Read Only)

Latched status of general control packet interrupt signal. Once set, this bit will remain high until the interrupt is cleared via GEN_CTL_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

GEN_CTL_PCKT_ST	Description
0 (default)	GEN_CTL_PCKT_RAW has not changed. Interrupt has not been generated from this register.
1	GEN_CTL_PCKT_RAW has changed. Interrupt has been generated from this register.

AUDIO_C_PCKT_ST, IO, Address 0x66[1] (Read Only)

Latched status of audio clock regeneration packet interrupt signal. Once set, this bit will remain high until the interrupt is cleared via AUDIO_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AUDIO_C_PCKT_ST	Description
0 (default)	AUDIO_C_PCKT_RAW has not changed. Interrupt has not been generated from this register.
1	AUDIO_C_PCKT_RAW has changed. Interrupt has been generated from this register.

GAMUT_MDATA_ST, IO, Address 0x66[0] (Read Only)

Latched status of gamut metadata packet detected interrupt signal. Once set, this bit will remain high until the interrupt is cleared via GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

GAMUT_MDATA_ST	Description
0 (default)	GAMUT_MDATA_RAW has not changed. Interrupt has not been generated from this register.
1	GAMUT_MDATA_RAW has changed. Interrupt has been generated from this register.

HDMI Lvl INT Status 3 register consists of fields: CABLE_DET_B_ST, TMDSPLL_LCK_A_ST, TMDS_CLK_A_ST, VIDEO_3D_ST, V_LOCKED_ST, and DE_REGEN_LCK_ST.

CABLE_DET_B_ST, IO, Address 0x6B[7] (Read Only)

Latched status of Port B +5 V cable detection interrupt signal. Once set, this bit remains high until the interrupt has been cleared via CABLE_DET_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit.

Function

CABLE_DET_B_ST	Description
0 (default)	CABLE_DET_B_RAW has not changed. Interrupt has not been generated from this register.
1	CABLE_DET_B_RAW has changed. Interrupt has been generated from this register.

TMDSPLL_LCK_A_ST, IO, Address 0x6B[6] (Read Only)

Latched status of Port A TMDS PLL lock interrupt signal. Once set, this bit will remain high until the interrupt is cleared via TMDSPLL_LCK_A_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

TMDSPLL_LCK_A_ST	Description
0 (default)	TMDSPLL_LCK_A_RAW has not changed. An interrupt has not been generated.
1	TMDSPLL_LCK_A_RAW has changed. An interrupt has been generated.

TMDSPLL_LCK_B_ST, IO, *Address 0x6B[5] (Read Only)*

Latched status of Port B TMDS PLL lock interrupt signal. Once set this bit will remain high until the interrupt has been cleared via TMDSPLL_LCK_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit

Function

TMDS_CLK_B_ST	Description
0 (default)	TMDS_CLK_B_RAW has not changed. An interrupt has not been generated.
1	TMDS_CLK_B_RAW has changed. An interrupt has been generated.

TMDS_CLK_A_ST, IO, Address 0x6B[4] (Read Only)

Latched status of Port A TMDS clock detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via TMDS_CLK_A_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

TMDS_CLK_A_ST	Description
0 (default)	TMDS_CLK_A_RAW has not changed. An interrupt has not been generated.
1	TMDS_CLK_A_RAW has changed. An interrupt has been generated.

TMDS_CLK_B_ST, IO, Address 0x6B[3] (Read Only)

Latched status of Port B TMDS clock detection interrupt signal .Once set, this bit will remain high until the interrupt has been cleared via TMDS_CLK_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit

Function

TMDS_CLK_B_ST	Description
0 «	TMDS_CLK_B_RAW has not changed. An interrupt has not been generated.
1	TMDS_CLK_B_RAW has changed. An interrupt has been generated.

VIDEO_3D_ST, IO, Address 0x6B[2] (Read Only)

Latched status for the video 3D interrupt. Once set, this bit will remain high until the interrupt is cleared via VIDEO_3D_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

VIDEO_3D_ST	Description
0 (default)	VIDEO_3D_RAW has not changed. An interrupt has not been generated.
1	VIDEO_3D_RAW has changed. An interrupt has been generated.

V_LOCKED_ST, IO, Address 0x6B[1] (Read Only)

Latched status for the vertical sync filter locked interrupt. Once set, this bit will remain high until the interrupt is cleared via V_LOCKED_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

V_LOCKED_ST	Description
0 (default)	V_LOCKED_RAW has not changed. An interrupt has not been generated.
1	V_LOCKED_RAW has changed. An interrupt has been generated.

DE_REGEN_LCK_ST, IO, Address 0x6B[0] (Read Only)

Latched status for DE regeneration lock interrupt signal. Once set, this bit will remain high until the interrupt is cleared via DE_REGEN_LCK_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

DE_REGEN_LCK_ST	Description
0 (default)	DE_REGEN_LCK_RAW has not changed. An interrupt has not been generated.
1	DE_REGEN_LCK_RAW has changed. An interrupt has been generated.

HDMI Lvl INT Status 4 register consists of fields: HDMI_ENCRPT_A_ST and CABLE_DET_A_ST.

HDMI_ENCRPT_A_ST, IO, Address 0x70[2] (Read Only)

Latched status for Port A encryption detection interrupt signal. Once set, this bit will remain high until the interrupt is cleared via HDMI_ENCRPT_A_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

HDMI_ENCRPT_A_ST	Description
0 (default)	HDMI_ENCRPT_A_RAW has not changed. An interrupt has not been generated.
1	HDMI_ENCRPT_A_RAW has changed. An interrupt has been generated.

HDMI_ENCRPT_B_ST, IO, Address 0x70[1] (Read Only)

Latched status for Port B encryption detection interrupt signal. Once set, this bit will remain high until the interrupt is cleared via HDMI_ENCRPT_B_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

HDMI_ENCRPT_B_ST	Description
0 (default)	HDMI_ENCRPT_B_RAW has not changed. An interrupt has not been generated.
1	HDMI_ENCRPT_B_RAW has changed. An interrupt has been generated.

CABLE_DET_A_ST, IO, Address 0x70[0] (Read Only)

Latched status for Port A +5 V cable detection interrupt signal. Once set, this bit will remain high until the interrupt is cleared via CABLE_DET_A_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

CABLE_DET_A_ST	Description
0 (default)	CABLE_DET_A_RAW has not changed. Interrupt has not been generated from this register.
1	CABLE_DET_A_RAW has changed. Interrupt has been generated from this register.

HDMI Edg INT Status 1 register consists of fields: NEW_ISRC2_PCKT_ST, NEW_ISRC1_PCKT_ST, NEW_ACP_PCKT_ST, NEW_VS_INFO_ST, NEW_MS_INFO_ST, NEW_SPD_INFO_ST, and NEW_AUDIO_INFO_ST.

NEW_ISRC2_PCKT_ST, IO, Address 0x7A[7] (Read Only)

Latched status for the new ISRC2 packet interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_ISRC2_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_ISRC2_PCKT_ST	Description
0 (default)	No new ISRC2 packet received. An interrupt has not been generated.
1	ISRC2 packet with new content received. An interrupt has been generated.

NEW_ISRC1_PCKT_ST, IO, Address 0x7A[6] (Read Only)

Latched status for the new ISRC1 packet interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_ISRC1_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_ISRC1_PCKT_ST	Description
0 (default)	No new ISRC1 packet received. An interrupt has not been generated.
1	ISRC1 packet with new content received. An interrupt has been generated.

NEW_ACP_PCKT_ST, IO, Address 0x7A[5] (Read Only)

Latched status for the new ACP packet interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_ACP_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_ACP_PCKT_ST	Description
0 (default)	No new ACP packet received. An interrupt has not been generated.
1	ACP packet with new content received. An interrupt has been generated.

NEW_VS_INFO_ST, IO, Address 0x7A[4] (Read Only)

Latched status for the new vendor specific InfoFrame interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_VS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_VS_INFO_ST	Description
0 (default)	No new VS packet received. An interrupt has not been generated.
1	VS packet with new content received. An interrupt has been generated.

NEW_MS_INFO_ST, IO, Address 0x7A[3] (Read Only)

Latched status for the new MPEG source InfoFrame interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_MS_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_MS_INFO_ST	Description
0 (default)	No new MPEG Source InfoFrame received. Interrupt has not been generated.
1	MPEG Source InfoFrame with new content received. Interrupt has been generated.

NEW_SPD_INFO_ST, IO, Address 0x7A[2] (Read Only)

Latched status for the new source product descriptor InfoFrame interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_SPD_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_SPD_INFO_ST	Description
0 (default)	No new SPD InfoFrame received. Interrupt has not been generated.
1	SPD InfoFrame with new content received. Interrupt has been generated.

NEW_AUDIO_INFO_ST, IO, Address 0x7A[1] (Read Only)

Latched status for the new audio InfoFrame interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_AUDIO_INFO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_AUDIO_INFO_ST	Description
0 (default)	No new Audio InfoFrame received. Interrupt has not been generated.
1	Audio InfoFrame with new content received. Interrupt has been generated.

NEW_AVI_INFO_ST, IO, Address 0x7A[0] (Read Only)

A detailed description can be found for this function in the Interrupt Architecture Overview section.

HDMI Edg INT Status 2 register consists of fields: FIFO_NEAR_OVFL_ST, FIFO_UNDERFLO_ST, FIFO_OVERFLO_ST, CTS_PASS_THRSH_ST, CHANGE_N_ST, PACKET_ERROR_ST, AUDIO_PCKT_ERR_ST, and NEW_GAMUT_MDATA_ST.

FIFO_NEAR_OVFL_ST, IO, Address 0x7F[7] (Read Only)

Latched status for the audio FIFO near overflow interrupt. Once set, this bit will remain high until the interrupt is cleared via FIFO_OVFL_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

FIFO_NEAR_OVFL_ST	Description
0 (default)	Audio FIFO has not reached high threshold.
1	Audio FIFO has reached high threshold.

FIFO_UNDERFLO_ST, IO, Address 0x7F[6] (Read Only)

Latched status for the sudio FIFO underflow interrupt. Once set, this bit will remain high until the interrupt is cleared via FIFO_UNDERFLO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

FIFO_UNDERFLO_ST	Description
0 (default)	Audio FIFO has not underflowed.
1	Audio FIFO has underflowed.

FIFO_OVERFLO_ST, IO, Address 0x7F[5] (Read Only)

Latched status for the audio FIFO overflow interrupt. Once set, this bit will remain high until the interrupt is cleared via FIFO_OVERFLO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

FIFO_OVERFLO_ST	Description
0 (default)	Audio FIFO has not overflowed.
1	Audio FIFO has overflowed.

CTS_PASS_THRSH_ST, IO, Address 0x7F[4] (Read Only)

Latched status for the ACR CTS value exceed threshold interrupt. Once set, this bit will remain high until the interrupt is cleared via CTS_PASS_THRSH_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

CTS_PASS_THRSH_ST	Description
0 (default)	Audio clock regeneration CTS value has not passed the threshold.
1	Audio clock regeneration CTS value has changed more than threshold.

CHANGE_N_ST, IO, Address 0x7F[3] (Read Only)

Latched status for the ACR N value changed interrupt. Once set, this bit will remain high until the interrupt is cleared via CHANGE_N_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

CHANGE_N_ST	Description
0 (default)	Audio clock regeneration N value has not changed.
1	Audio clock regeneration N value has changed.

PACKET_ERROR_ST, IO, Address 0x7F[2] (Read Only)

Latched status for the packet error interrupt. Once set, this bit will remain high until the interrupt is cleared via PACKET_ERROR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function	
PACKET_ERROR_ST	Description
0 (default)	No uncorrectable error detected in packet header. An interrupt has not been generated.
1	Uncorrectable error detected in an unknown packet (in packet header). An interrupt has been generated.

AUDIO_PCKT_ERR_ST, IO, Address 0x7F[1] (Read Only)

Latched status for the audio packet error interrupt. Once set, this bit will remain high until the interrupt is cleared via AUDIO_PCKT_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AUDIO_PCKT_ERR_ST	Description
0 (default)	No uncorrectable error detected in audio packets. An interrupt has not been generated.
1	Uncorrectable error detected in an audio packet. An interrupt has been generated.

NEW_GAMUT_MDATA_ST, IO, Address 0x7F[0] (Read Only)

Latched status for the new gamut metadata packet interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_GAMUT_MDATA_PCKT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_GAMUT_MDATA_ST	Description
0 (default)	No new Gamut metadata packet received or no change has taken place. An interrupt has not been generated.
1	New Gamut metadata packet received. An interrupt has been generated.

HDMI Edg Int Status 3 register consists of fields: DEEP_COLOR_CHNG_ST, VCLK_CHNG_ST, AUDIO_MODE_CHNG_ST, PARITY_ERROR_ST, NEW_SAMP_RT_ST, AUDIO_FLT_LINE_ST, NEW_TMDS_FRQ_ST, and FIFO_NEAR_UFLO_ST.

DEEP_COLOR_CHNG_ST, IO, Address 0x84[7] (Read Only)

Latched status of deep color mode change interrupt. Once set, this bit will remain high until the interrupt is cleared via DEEP_COLOR_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

DEEP_COLOR_CHNG_ST	Description
0 (default)	Deep color mode has not changed.
1	Change in deep color has been detected.

VCLK_CHNG_ST, IO, Address 0x84[6] (Read Only)

Latched status of video clock change interrupt. Once set, this bit will remain high until the interrupt is cleared via VCLK_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

VCLK_CHNG_ST	Description
0 (default)	No irregular or missing pulse detected in TMDS clock
1	Irregular or missing pulses detected in TMDS clock

AUDIO_MODE_CHNG_ST, IO, Address 0x84[5] (Read Only)

Latched status of audio mode change interrupt. Once set, this bit will remain high until the interrupt is cleared via AUDIO_MODE_CHNG_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AUDIO_MODE_CHNG_ST	Description
0 (default)	Audio mode has not changed.
1	Audio mode has changed.

PARITY_ERROR_ST, IO, Address 0x84[4] (Read Only)

Latched status of parity error interrupt. Once set, this bit will remain high until the interrupt is cleared via PARITY_ERROR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

PARITY_ERROR_ST	Description
0 (default)	No parity error detected in audio packets
1	Parity error detected in an audio packet

NEW_SAMP_RT_ST, IO, Address 0x84[3] (Read Only)

Latched status of new sampling rate interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_SAMP_RT_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_SAMP_RT_ST	Description
0 (default)	Sampling rate bits of the channel status data on Audio Channel 0 have not changed.
1	Sampling rate bits of the channel status data on Audio Channel 0 have changed.

AUDIO_FLT_LINE_ST, IO, Address 0x84[2] (Read Only)

Latched status of new TMDS frequency interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AUDIO_FLT_LINE_ST	Description
0 (default)	Audio sample packet with flat line bit set has not been received.
1	Audio sample packet with flat line bit set has been received.

NEW_TMDS_FRQ_ST, IO, Address 0x84[1] (Read Only)

Latched status of new TMDS frequency interrupt. Once set, this bit will remain high until the interrupt is cleared via NEW_TMDS_FREQ_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

NEW_TMDS_FRQ_ST	Description
0 (default)	TMDS frequency has not changed by more than tolerance.
1	TMDS frequency has changed by more than tolerance.

FIFO_NEAR_UFLO_ST, IO, Address 0x84[0] (Read Only)

Latched status for the audio FIFO near underflow interrupt. Once set, this bit will remain high until the interrupt is cleared via FIFO_UFLO_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

FIFO_NEAR_UFLO_ST	Description
0 (default)	Audio FIFO has not reached low threshold.
1	Audio FIFO has reached low threshold.

HDMI Edg Status 4 register consists of fields: MS_INF_CKS_ERR_ST, SPD_INF_CKS_ERR_ST, AUD_INF_CKS_ERR_ST, AVI_INF_CKS_ERR_ST, RI_EXPIRED_A_ST, and AKSV_UPDATE_A_ST.

MS_INF_CKS_ERR_ST, IO, Address 0x89[7] (Read Only)

Latched status of MPEG source InfoFrame checksum error interrupt. Once set, this bit will remain high until the interrupt is cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

MS_INF_CKS_ERR_ST	Description
0 (default)	No change in MPEG source InfoFrame checksum error
1	An MPEG source InfoFrame checksum error has triggered this interrupt

SPD_INF_CKS_ERR_ST, IO, Address 0x89[6] (Read Only)

Latched status of SPD InfoFrame checksum error interrupt. Once set, this bit will remain high until the interrupt is cleared via SPD_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

SPD_INF_CKS_ERR_ST	Description
0 (default)	No change in SPD InfoFrame checksum error
1	An SPD InfoFrame checksum error has triggered this interrupt

AUD_INF_CKS_ERR_ST, IO, Address 0x89[5] (Read Only)

Latched status of audio InfoFrame checksum error interrupt. Once set, this bit will remain high until the interrupt is cleared via AUDIO_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AUD_INF_CKS_ERR_ST	Description
0 (default)	No change in audio InfoFrame checksum error
1	An audio InfoFrame checksum error has triggered this interrupt

AVI_INF_CKS_ERR_ST, IO, Address 0x89[4] (Read Only)

Latched status of AVI InfoFrame checksum error interrupt. Once set, this bit will remain high until the interrupt is cleared via AVI_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AVI_INF_CKS_ERR_ST	Description
0 (default)	No change in AVI InfoFrame checksum error
1	An AVI InfoFrame checksum error has triggered this interrupt

RI_EXPIRED_B_ST, IO, Address 0x89[3] (Read Only)

Latched status of Port B Ri expired Interrupt. Once set this bit will remain high until the interrupt has been cleared via RI_EXPIRED_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit

Function

RI_EXPIRED_B_ST	Description
0 (default)	No Ri expired on Port B
1	Ri expired on Port B

RI_EXPIRED_A_ST, IO, Address 0x89[2] (Read Only)

Latched status of Port A Ri expired interrupt. Once set, this bit will remain high until the interrupt is cleared via RI_EXPIRED_A_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

RI_EXPIRED_A_ST	Description
0 (default)	No Ri expired on Port A
1	Ri expired on Port A

AKSV_UPDATE_B_ST, IO, Address 0x89[1] (Read Only)

Latched status of Port B AKSV Update Interrupt. Once set this bit will remain high until the interrupt has been cleared via AKSV_UPDATE_B_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit

Function

AKSV_UPDATE_B_ST	Description
0 (default)	No AKSV updates on Port B
1	Detected a write access to the AKSV register on Port B

AKSV_UPDATE_A_ST, IO, Address 0x89[0] (Read Only)

Latched status of Port A AKSV update interrupt. Once set, this bit will remain high until the interrupt is cleared via AKSV_UPDATE_A_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

AKSV_UPDATE_A_ST	Description
0 (default)	No AKSV updates on Port A
1	Detected a write access to the AKSV register on Port A

HDMI Edg Int Status 5 register consists of the VS_INF_CKS_ERR_ST field.

BG_MEAS_DONE_ST, IO, Address 0x8E[1] (Read Only)

Latched status of background port measurement completed interrupt. Once set, this bit will remain high until the interrupt has been cleared via BG_MEAS_DONE_CLR. This bit is only valid if enabled via corresponding the INT1 or INT2 interrupt mask bit.

Function

BG_MEAS_DONE_ST	Description
0 (default)	Measurements of TMDS frequency and video parameters of background port not finished or not requested.
1	Measurements of TMDS frequency and video parameters of background port are ready

VS_INF_CKS_ERR_ST, IO, Address 0x8E[0] (Read Only)

Latched status of MPEG source InfoFrame checksum error interrupt. Once set, this bit will remain high until the interrupt is cleared via MS_INF_CKS_ERR_CLR. This bit is only valid if enabled via the corresponding INT1 or INT2 interrupt mask bit.

Function

VS_INF_CKS_ERR_ST	Description
0 (default)	No change in VS InfoFrame checksum error
1	A VS InfoFrame checksum error has triggered this interrupt

CEC_STATUS1_INT_STATUS register consists of fields:

- CEC_RX_RDY2_ST
- CEC_RX_RDY1_ST
- CEC_RX_RDY0_ST
- CEC_TX_RETRY_TIMEOUT_ST
- CEC_TX_ARBITRATION_LOST_ST
- CEC_TX_READY_ST

CEC_STATUS2_INT_STATUS register consists of the CEC_INTERRUPT_BYTE_ST[7:0] field.

CEC_INTERRUPT_BYTE_ST[7:0], IO, Address 0x98[7:0] (Read Only)

Function

CEC_INTERRUPT_BYTE_ST[7:0]	Description
0 (default)	No change
1	One of the 8 opcodes received

REGISTER ACCESS AND SERIAL PORTS DESCRIPTION

The ADV7619 has three 2-wire serial (I²C compatible) ports:

- One main I²C port, SDA/SCL, allows a system I²C master controller to control and configure the ADV7619
- Two I²C ports, DDC Port A and Port B allows an HDMI host to access the internal EDID and the HDCP registers

MAIN I²C PORT

Register Access

The ADV7619 has eight 256-byte maps that can be accessed via the main I²C ports, SDA and SCL. Each map has its own I²C address and acts as a standard slave device on the I²C bus.

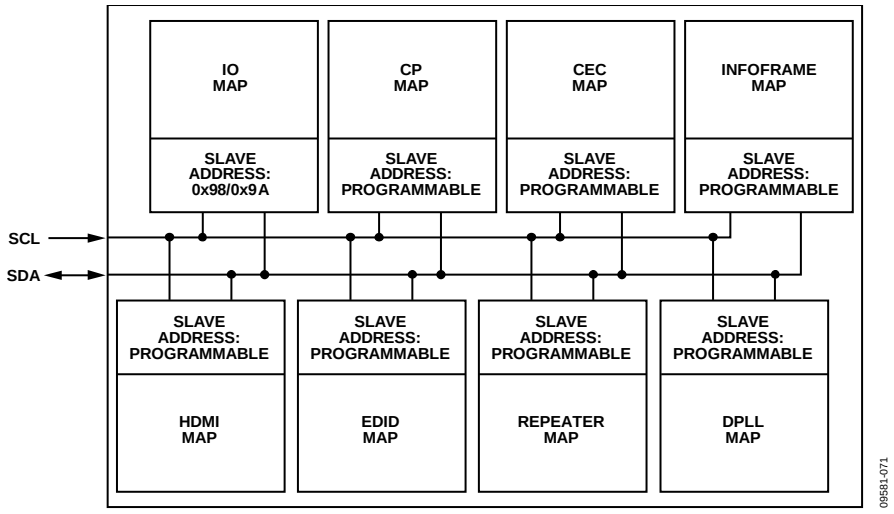


Figure 71. ADV7619 Register Map Access through Main I²C Port

Seven out of the eight maps have a programmable I²C address. This facilitates the integration of the ADV7619 in systems that have multiple slaves on the general I²C bus.

Table 76. Register Maps and I²C Addresses

Map	Default Address[2]	Programmable Address	Location at which Address can be Programmed
IO Map	0x98 or 0x9A[1]	Not programmable	Not applicable
CP Map	0x00 (disabled)	Programmable	IO Map Register 0xFD
HDMI Map	0x00 (disabled)	Programmable	IO Map Register 0xFB
Repeater Map	0x00 (disabled)	Programmable	IO Map Register 0xF9
EDID Map	0x00 (disabled)	Programmable	IO Map Register 0xFA
InfoFrame Map	0x00 (disabled)	Programmable	IO Map Register 0xF5
CEC Map	0x00 (disabled)	Programmable	IO Map Register 0xF4
DPLL Map	0x00 (disabled)	Programmable	IO Map Register 0xF8

[1] IO map address can be changed by pulling up or down VS/FIELD/ALSB pin.
[2] Map is disabled if its address is set to 0x00

IO I²C Map Address

It is possible to set the address of the IO map by using the VS/FIELD/ALSB pin. Follow these steps to set the address of IO map:

1. Pull up theVS/FIELD/ALSB pin with a 10 kΩ resistor to 3.3 V to set the IO map to 0x9A. It should be left floating for 0x98. If the line VS/FIELD/ALSB is not pulled up, the following steps will have no effect and the IO map will remain 0x98.
2. On power up, VS pin is tristated and the IO map will have an address of 0x98, regardless of the pull-up.
3. Set SAMPLE ALSB to 1; this causes the VS/FIELD/ALSB line to be sampled.
   a. If VS/FIELD/ALSB was pulled high with a 10 kΩ resistor to 3.3 V, the IO map address will become 0x9A.
   b. If VS/FIELD/ALSB was pulled low, or was left floating, the IO map address will remain 0x98.

This solution allows connecting two ADV7619 on the one I²C bus. One part should have a 10 kΩ resistor pull-up on the VS/FIELD/ALSB pin; Pin VS/FIELD/ALSB on the second part should be left floating. After reset, both parts will have Address 0x98. After sending an I²C

write command to IO 0x1B, SAMPLE_ALSB, one part (with VS/FIELD/ALSB left floating) will get Address 0x98 and the second part (with VS/FIELD/ALSB pulled high) will have an address of 0x9A.

SAMPLE_ALSB, IO, Address 0x1B[0]

When HIGH, VS/FIELD/ALSB pin is sampled to be used as ALSB value for IO map.

Function

SAMPLE_ALSB	Description
0 (default)	Use previously stored ALSB value
1	Sample new ALSB value

Addresses of Other Maps

CEC_SLAVE_ADDR[6:0], IO, Address 0xF4[7:1]

Programmable I²C slave address for CEC map

Function

CEC_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	CEC Map Slave address

INFOFRAME_SLAVE_ADDR[6:0], IO, Address 0xF5[7:1]

Programmable I²C slave address for InfoFrame map

Function

INFOFRAME_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	Infoframe Map Slave address

KSV_SLAVE_ADDR[6:0], IO, Address 0xF9[7:1]

Programmable I²C slave address for KSV (Repeater) map

Function

KSV_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	Repeater Map Slave address

EDID_SLAVE_ADDR[6:0], IO, Address 0xFA[7:1]

Programmable I²C slave address for EDID map

Function

EDID_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	EDID Map Slave address

HDMI_SLAVE_ADDR[6:0], IO, Address 0xFB[7:1]

Programmable I²C slave address for HDMI map

Function

HDMI_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	HDMI Map Slave address

CP_SLAVE_ADDR[6:0], IO, Address 0xFD[7:1]

Programmable I²C slave address for CP map

Function

CP_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	CP Map Slave address

DPLL_SLAVE_ADDR[6:0], IO, Address 0xF8[7:1]

Programmable I²C slave address for DPLL map

Function

DPLL_SLAVE_ADDR[6:0]	Description
0x00 (default)	Map not accessible
0xXX	DPLL Map Slave address

Protocol for Main I²C Port

The system controller initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCL remains high. This transition indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address and R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition.

In the idle condition, the device monitors the SDA and SCL lines for the start condition and the correct transmitted address. The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master will write information to the peripheral. A Logic 1 on the LSB of the first byte means that the master will read information from the peripheral.

Each of the ADV7619 maps acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/W bit. It interprets the first byte as the map address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, these cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7619 does not issue an acknowledge and returns to the idle condition.

If the user exceeds the highest subaddress in auto increment mode, the following actions are taken:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register. A no acknowledge is issued by the ADV7619 and the part returns to the idle condition.

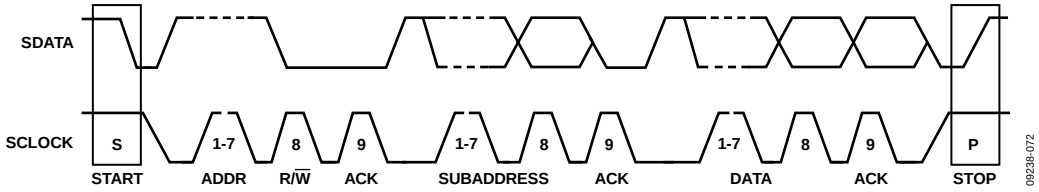


Figure 72. Bus Data Transfer

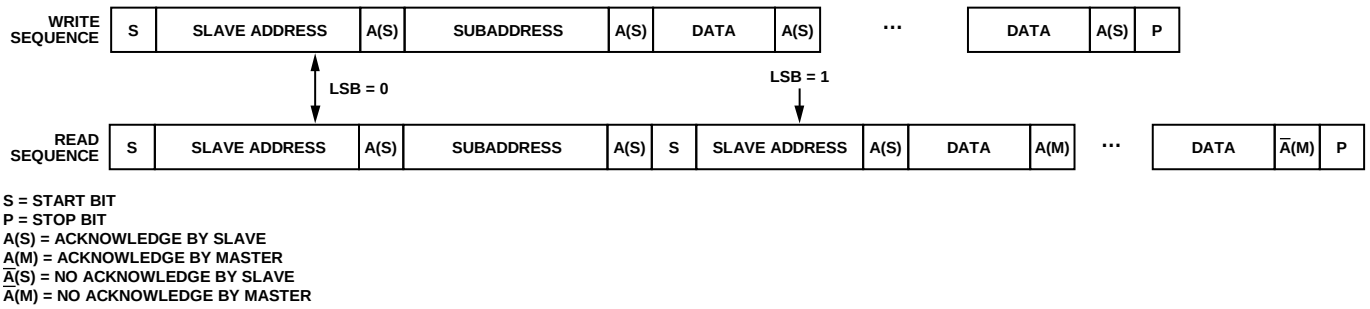


Figure 73. Read and Write Sequence

DDC PORTS

An I²C port, DDC Port A, allows HDMI hosts to access the internal E-EDID and the HDCP registers. Note that the DDC ports are 5 V tolerant, which simplifies the hardware between the HDMI connector and the ADV7619.

I²C Protocols for Access to the Internal EDID

An I²C master connected on a DDC port can access the internal EDID using the following protocol:

- Write sequence, as defined in the Protocol for Main I²C Port section
- Read sequence, as defined in the Protocol for Main I²C Port section
- Current address read sequence:
  Allows the master on the DDC port to read access internal E-EDID without specifying the subaddress that must be read. The ADV7619 stores an address counter for DDC port that maintains the value of the subaddress that was last accessed. The address counter is incremented by one every time a read or a write access is requested on the DDC port.

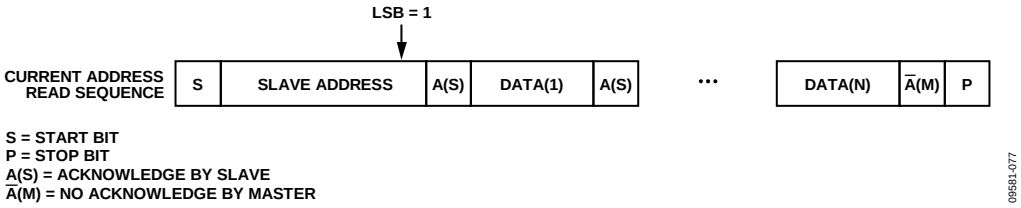


Figure 74. Current Address Read Sequence

I²C Protocols for Access to HDCP Registers

An I²C master connected on a DDC port can access the internal EDID using the following protocol:

- Write sequence, as defined in the Protocol for Main I²C Port section
- Read sequence, as defined in the Protocol for Main I²C Port section
- Short read format, as defined in the High-bandwidth Digital Content Protection (HDCP) System Specifications

DDC Port A

The DDC lines of the HDMI Port A comprise the DDCA_SCL and DDCA_SDA pins. An HDMI host connected to the DDC Port A accesses the internal E-EDID at address 0xA0 in read only mode, and the HDCP registers at address 0x74 in read/write mode (refer to Figure 75). The internal E-EDID for Port A is described in the Structure of Internal E-EDID section.

Refer to the High-bandwidth Digital Content Protection (HDCP) System specifications for detailed information on the HDCP registers.

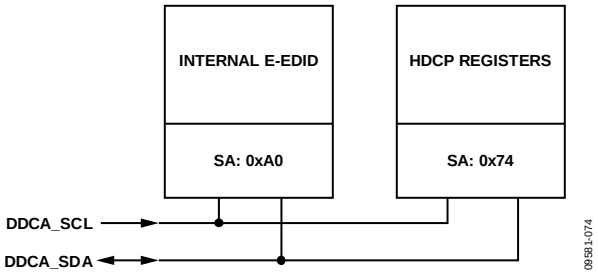


Figure 75. Internal E-EDID and HDCP Registers Access from Port A (SA = Slave Address)

DDC Port B

The DDC lines of the HDMI Port B comprise the DDCB_SCL and DDCB_SDA pins. An HDMI host connected to the DDC Port B accesses the internal E-EDID at Address 0xA0 in read-only mode, and the HDCP registers at Address 0x74 in read/write mode (refer to Figure 76). The internal E-EDID for Port B is described in Structure of Internal E-EDID for Port B section

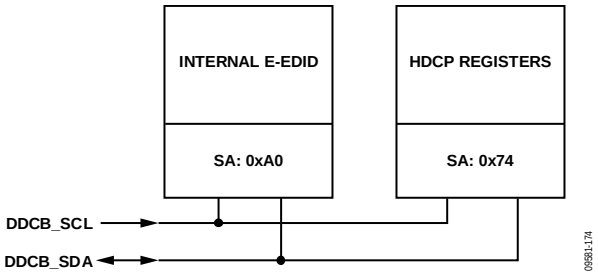


Figure 76.Internal E-EDID and HDCP Registers Access from Port B

Refer to the High-bandwidth Digital Content Protection (HDCP) System Specifications for detailed information on the HDCP registers.

APPENDIX A

PCB LAYOUT RECOMMENDATIONS

The ADV7619 is a high precision, high speed, mixed signal device. It is important to have a well laid out PCB board, in order to achieve the maximum performance from the part. The following sections are a guide for designing a board using the ADV7619.

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1 µF and a 10 nF capacitor where possible. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. The power connection should not be made between the capacitor and the power pin. Generally, the best approach is to place a via underneath the 100 nF capacitor pads down to the power plane (refer to Figure 77).

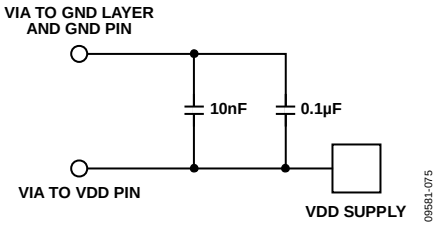


Figure 77. Recommended Power Supply Decoupling

It is particularly important to maintain low noise and good stability of the PVDD (the clock generator supply). Abrupt changes in the PVDD supply can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated or heavily filtered supplies for each of the analog circuitry groups (CVDD, TVDD, and PVDD).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical synchronization periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PVDD, from a different, cleaner, power source, for example, from a +12 V supply.

It is also recommended to use a single ground plane for the entire board. Repeatedly, experience has shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to place, at least, a single ground plane under the ADV7619. It is important to place components wisely because the current loops are much longer when using split ground planes as the current takes the path of least resistance.

Example of a Current Loop

Power plane → ADV7619 → digital output trace → digital data receiver→ digital ground plane → analog ground plane

DIGITAL OUTPUTS (DATA AND CLOCKS)

The trace length that the digital outputs have to drive should be minimized. Longer traces have higher capacitance, which requires more current that can cause more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor of value between 33 Ω to 200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside the ADV7619. If series resistors are used, they should be placed as close as possible to the ADV7619 pins and the trace impedance for these signals should match that of the termination resistors selected.

If possible, the capacitance that each of the digital outputs drives should be limited to is less than 15 pF. This can be accomplished easily by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7619, creating more digital noise on its power supplies.

DIGITAL INPUTS

The following digital inputs on the ADV7619 are 3.3 V inputs that are 5.0 V tolerant:

- DDCA_SCL
- DDCA_SDA
- DDCB_SCL
- DDCB_SDA

Any noise that gets onto the HS and VS inputs trace will add jitter to the system. Therefore, the trace length should be minimized; and digital or other high frequency traces should not be run near it.

XTAL AND LOAD CAP VALUE SELECTION

The ADV7619 can use a 24.000 MHz, 24.576 MHz, 27.000 MHz, or 28.6363 MHz crystal. Figure 78 shows an example of a reference clock circuit for the ADV7619. Special care must be taken when using a crystal circuit to generate the reference clock for the ADV7619. Small variations in reference clock frequency can cause auto detection issues and impair the ADV7619 performance.

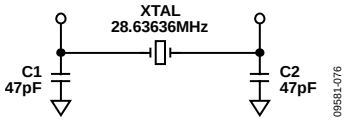


Figure 78. Crystal Circuit

These guidelines are followed to ensure correct operation:

- Use the correct frequency crystal, which is 28.6363 MHz. Tolerance should be 50 ppm or better.
- Know the C_{load} for the crystal part number selected. The value of capacitors C1 and C2 must be matched to the C_{load} for the specific crystal part number in the user's system.

To find C1 and C2, use the following formula:

$$C1 = C2 = 2(C_{load} - C_{stray}) - C_{pg}$$

where C_{stray} is usually 2 pF to 3 pF, depending on board traces and C_{pg} (pin-to-ground-capacitance) is 4 pF for the ADV7619.

Example

C_{load} = 30 pF, C1 = 50 pF, C2 = 50 pF (in this case, 47 pF is the nearest real-life cap value to 50 pF)

APPENDIX B

RECOMMENDED UNUSED PIN CONFIGURATIONS

Table 77. Recommended Configuration of Unused Pins

Pin No.	Mnemonic	Type	Recommended Configuration if Not Used
0	GND	Ground	Ground
1	GND	Ground	Ground
2	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V)
3	RXA_C-	HDMI Input	Float this pin
4	RXA_C+	HDMI Input	Float this pin
5	TVDD	Power	Terminator Supply Voltage (3.3 V)
6	RXA_0-	HDMI Input	Float this pin
7	RXA_0+	HDMI Input	Float this pin
8	TVDD	Power	Terminator Supply Voltage (3.3 V)
9	RXA_1-	HDMI Input	Float this pin
10	RXA_1+	HDMI input	Float this pin
11	TVDD	Power	Terminator Supply Voltage (3.3 V)
12	RXA_2-	HDMI Input	Float this pin
13	RXA_2+	HDMI Input	Float this pin
14	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V)
15	GND	Ground	Ground
16	TEST1	No Connect	Float this pin
17	DVDD	Power	Digital Core Supply Voltage (1.8 V)
18	TEST2	No Connect	Float this pin
19	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V)
20	RXB_C-	HDMI Input	Float this pin
21	RXB_C+	HDMI Input	Float this pin
22	TVDD	Power	Terminator Supply Voltage (3.3 V)
23	RXB_0-	HDMI Input	Float this pin
24	RXB_0+	HDMI Input	Float this pin
25	TVDD	Power	Terminator Supply Voltage (3.3 V)
26	RXB_1-	HDMI Input	Float this pin
27	RXB_1+	HDMI Input	Float this pin
28	TVDD	Power	Terminator Supply Voltage (3.3 V)
29	RXB_2-	HDMI Input	Float this pin
30	RXB_2+	HDMI Input	Float this pin
31	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V)
32	GND	Ground	Ground
33	NC	No Connect	Float this pin
34	DVDD	Power	Digital Core Supply Voltage (1.8 V)
35	P47	Digital Output	Float this pin
36	P46	Digital Output	Float this pin
37	P45	Digital Output	Float this pin
38	P44	Digital Output	Float this pin
39	P43	Digital Output	Float this pin
40	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V)
41	P42	Digital Output	Float this pin
42	P41	Digital Output	Float this pin
43	P40	Digital Output	Float this pin
44	P39	Digital Output	Float this pin
45	P38	Digital Output	Float this pin
46	P37	Digital Output	Float this pin
47	P36	Digital Output	Float this pin
48	P35	Digital Output	Float this pin

Pin No.	Mnemonic	Type	Recommended Configuration if Not Used
49	P34	Digital Output	Float this pin
50	P33	Digital Output	Float this pin
51	P32	Digital Output	Float this pin
52	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V)
53	DVDD	Power	Digital Core Supply Voltage (1.8 V)
54	P31	Digital Output	Float this pin
55	P30	Digital Output	Float this pin
56	P29	Digital Output	Float this pin
57	P28	Digital Output	Float this pin
58	P27	Digital Output	Float this pin
59	P26	Digital Output	Float this pin
60	P25	Digital Output	Float this pin
61	P24	Digital Output	Float this pin
62	LLC	Digital Output	This pin is always connected to the pixel clock input
63	DVDD	Power	Digital Core Supply Voltage (1.8 V)
64	DVDD	Power	Digital Core Supply Voltage (1.8 V)
65	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V)
66	P23	Digital Output	Float this pin
67	P22	Digital Output	Float this pin
68	P21	Digital Output	Float this pin
69	P20	Digital Output	Float this pin
70	P19	Digital Output	Float this pin
71	P18	Digital Output	Float this pin
72	P17	Digital Output	Float this pin
73	P16	Digital Output	Float this pin
74	P15	Digital Output	Float this pin
75	P14	Digital Output	Float this pin
76	P13	Digital Output	Float this pin
77	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V)
78	P12	Digital Output	Float this pin
79	DVDD	Power	Digital Core Supply Voltage (1.8 V)
80	P11	Digital Output	Float this pin
81	P10	Digital Output	Float this pin
82	P9	Digital Output	Float this pin
83	P8	Digital Output	Float this pin
84	P7	Digital Output	Float this pin
85	P6	Digital Output	Float this pin
86	P5	Digital Output	Float this pin
87	P4	Digital Output	Float this pin
88	P3	Digital Output	Float this pin
89	P2	Digital Output	Float this pin
90	P1	Digital Output	Float this pin
91	P0	Digital Output	Float this pin
92	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V)
93	DE	Digital Output	Float this pin
94	HS	Digital Output	Float this pin
95	VS/FIELD/ALSB	Digital I/O	Float this pin
96	NC	No connect	Float this pin
97	NC	No connect	Float this pin
98	NC	No connect	Float this pin
99	NC	No connect	Float this pin
100	AP0	Digital Output	Float this pin
101	AP1	Digital Output	Float this pin

Pin No.	Mnemonic	Type	Recommended Configuration if Not Used
102	AP2	Digital Output	Float this pin
103	AP3	Digital Output	Float this pin
104	AP4	Digital Output	Float this pin
105	SCLK/INT2	Digital Output	Float this pin
106	AP5	Digital Output	Float this pin
107	MCLK/INT2	Digital Output	Float this pin
108	DVDD	Power	Digital Core Supply Voltage (1.8 V)
109	SDA	Digital I/O	This pin is always connected to the I^2C data line of a control processor
110	SCL	Digital Input	This pin is always connected to the I^2C clock line of a control processor
111	INT1	Digital Output	Float this pin
112	$\overline{\text{RESET}}$	Digital Input	Level of this pin should be controlled by an external processor
113	$\overline{\text{CS}}$	Digital Input	Float this pin
114	PVDD	Power	PLL Supply Voltage (1.8V)
115	XTALP	Miscellaneous Analog	Input Pin for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7619
116	XTALN	Miscellaneous Analog	Crystal Input. Input pin for 28.63636 MHz crystal
117	DVDD	Power	Digital Core Supply Voltage (1.8 V)
118	CEC	Digital I/O	Float this pin
119	DDCB_SCL	Digital Input	Connect this pin to ground via a 10k ohm resistor
120	DDCB_SDA	Digital I/O	Float this pin
121	HPA_B	Digital Output	Float this pin
122	RXB_5V	Digital Input	If RXB_5V is not used, float RXB_5V and set DIS_CABLE_DET_RST to 0. In case where Port B is not used, RXB_5V can be left unconnected.
123	DDCA_SCL	Digital Input	Connect this pin to ground via a 10k ohm resistor
124	DDCA_SDA	Digital I/O	Float this pin
125	HPA_A/INT2	Digital Output	Float this pin
126	RXA_5V	Digital Input	If RXA_5V is not used, float RXA_5V and set DIS_CABLE_DET_RST to 0. In the case where Port A is not used, RXA_5V can be left unconnected.
127	NC	No connect	Float this pin
128	NC	No connect	Float this pin

APPENDIX C

PIXEL OUTPUT FORMATS

Table 78. SDR 4:2:2 Output Modes

	SDR 4:2:2				
OP_FORMAT_SEL[7:0]	**0x0 or 0x20[1]**	**0x1[1]**	**0x2[1]**	**0x6[1]**	**0x0A or 0x2A[1]**
Pixel Output	**8-Bit SDR ITU-R BT.656 Mode 0**	**10-Bit SDR ITU-R BT.656 Mode 0**	**12-Bit SDR ITU-R BT.656 Mode 0**	**12-Bit SDR ITU-R BT.656 Mode 1**	**12-Bit SDR ITU-R BT.656 Mode 2**
P47	High-Z	High-Z	High-Z	High-Z	High-Z
P46	High-Z	High-Z	High-Z	High-Z	High-Z
P45	High-Z	High-Z	High-Z	High-Z	High-Z
P44	High-Z	High-Z	High-Z	High-Z	High-Z
P43	High-Z	High-Z	High-Z	High-Z	High-Z
P42	High-Z	High-Z	High-Z	High-Z	High-Z
P41	High-Z	High-Z	High-Z	High-Z	High-Z
P40	High-Z	High-Z	High-Z	High-Z	High-Z
P39	High-Z	High-Z	High-Z	High-Z	High-Z
P38	High-Z	High-Z	High-Z	High-Z	High-Z
P37	High-Z	High-Z	High-Z	High-Z	High-Z
P36	High-Z	High-Z	High-Z	High-Z	High-Z
P35	High-Z	High-Z	High-Z	High-Z	Y3, Cb3, Cr3
P34	High-Z	High-Z	High-Z	High-Z	Y2, Cb2, Cr2
P33	High-Z	High-Z	High-Z	High-Z	Y1, Cb1, Cr1
P32	High-Z	High-Z	High-Z	High-Z	Y0, Cb0, Cr0
P31	High-Z	High-Z	High-Z	High-Z	High-Z
P30	High-Z	High-Z	High-Z	High-Z	High-Z
P29	High-Z	High-Z	High-Z	Y1, Cb1, Cr1	High-Z
P28	High-Z	High-Z	High-Z	Y0, Cb0, Cr0	High-Z
P27	High-Z	High-Z	High-Z	High-Z	High-Z
P26	High-Z	High-Z	High-Z	High-Z	High-Z
P25	High-Z	High-Z	High-Z	High-Z	High-Z
P24	High-Z	High-Z	High-Z	High-Z	High-Z
P23	Y7, Cb7, Cr7	Y9, Cb9, Cr9	Y11, Cb11, Cr11	Y11, Cb11, Cr11	Y11, Cb11, Cr11
P22	Y6, Cb6, Cr6	Y8, Cb8, Cr8	Y10, Cb10, Cr10	Y10, Cb10, Cr10	Y10, Cb10, Cr10
P21	Y5, Cb5, Cr5	Y7, Cb7, Cr7	Y9, Cb9, Cr9	Y9, Cb9, Cr9	Y9, Cb9, Cr9
P20	Y4, Cb4, Cr4	Y6, Cb6, Cr6	Y8, Cb8, Cr8	Y8, Cb8, Cr8	Y8, Cb8, Cr8
P19	Y3, Cb3, Cr3	Y5, Cb5, Cr5	Y7, Cb7, Cr7	Y7, Cb7, Cr7	Y7, Cb7, Cr7
P18	Y2, Cb2, Cr2	Y4, Cb4, Cr4	Y6, Cb6, Cr6	Y6, Cb6, Cr6	Y6, Cb6, Cr6
P17	Y1, Cb1, Cr1	Y3, Cb3, Cr3	Y5, Cb5, Cr5	Y5, Cb5, Cr5	Y5, Cb5, Cr5
P16	Y0, Cb0, Cr0	Y2, Cb2, Cr2	Y4, Cb4, Cr4	Y4, Cb4, Cr4	Y4, Cb4, Cr4
P15	High-Z	Y1, Cb1, Cr1	Y3, Cb3, Cr3	Y3, Cb3, Cr3	High-Z
P14	High-Z	Y0, Cb0, Cr0	Y2, Cb2, Cr2	Y2, Cb2, Cr2	High-Z
P13	High-Z	High-Z	Y1, Cb1, Cr1	High-Z	High-Z
P12	High-Z	High-Z	Y0, Cb0, Cr0	High-Z	High-Z
P11	High-Z	High-Z	High-Z	High-Z	High-Z
P10	High-Z	High-Z	High-Z	High-Z	High-Z
P09	High-Z	High-Z	High-Z	High-Z	High-Z
P08	High-Z	High-Z	High-Z	High-Z	High-Z
P07	High-Z	High-Z	High-Z	High-Z	High-Z
P06	High-Z	High-Z	High-Z	High-Z	High-Z
P05	High-Z	High-Z	High-Z	High-Z	High-Z
P04	High-Z	High-Z	High-Z	High-Z	High-Z
P03	High-Z	High-Z	High-Z	High-Z	High-Z
P02	High-Z	High-Z	High-Z	High-Z	High-Z
P01	High-Z	High-Z	High-Z	High-Z	High-Z
P00	High-Z	High-Z	High-Z	High-Z	High-Z

[1] Refer to the DLL Settings for 656, 8-/10-/12-Bit Modes section in chapter DLL on LLC Clock Path.

Table 79. SDR 4:2:2 Output Modes

	SDR 4:2:2				
OP_FORMAT_SEL[7:0]	**0x80**	**0x81**	**0x82**	**0x86**	**0x8A**
Pixel Output	**16-Bit SDR ITU-R BT.656 Mode 0**	**20-Bit SDR ITU-R BT.656 Mode 0**	**24-Bit SDR ITU-R BT.656 Mode 0**	**24-Bit SDR ITU-R BT.656 Mode 1**	**24-Bit SDR ITU-R BT.656 Mode 2**
P47	High-Z	High-Z	High-Z	High-Z	High-Z
P46	High-Z	High-Z	High-Z	High-Z	High-Z
P45	High-Z	High-Z	High-Z	High-Z	High-Z
P44	High-Z	High-Z	High-Z	High-Z	High-Z
P43	High-Z	High-Z	High-Z	High-Z	High-Z
P42	High-Z	High-Z	High-Z	High-Z	High-Z
P41	High-Z	High-Z	High-Z	High-Z	High-Z
P40	High-Z	High-Z	High-Z	High-Z	High-Z
P39	High-Z	High-Z	High-Z	High-Z	High-Z
P38	High-Z	High-Z	High-Z	High-Z	High-Z
P37	High-Z	High-Z	High-Z	High-Z	High-Z
P36	High-Z	High-Z	High-Z	High-Z	High-Z
P35	High-Z	High-Z	High-Z	High-Z	Y3
P34	High-Z	High-Z	High-Z	High-Z	Y2
P33	High-Z	High-Z	High-Z	Cb1, Cr1	Y1
P32	High-Z	High-Z	High-Z	Cb0, Cr0	Y0
P31	High-Z	High-Z	High-Z	High-Z	Cb3, Cr3
P30	High-Z	High-Z	High-Z	High-Z	Cb2, Cr2
P29	High-Z	High-Z	High-Z	Y1	Cb1, Cr1
P28	High-Z	High-Z	High-Z	Y0	Cb0, Cr0
P27	High-Z	High-Z	High-Z	High-Z	High-Z
P26	High-Z	High-Z	High-Z	High-Z	High-Z
P25	High-Z	High-Z	High-Z	High-Z	High-Z
P24	High-Z	High-Z	High-Z	High-Z	High-Z
P23	Y7	Y9	Y11	Y11	Y11
P22	Y6	Y8	Y10	Y10	Y10
P21	Y5	Y7	Y9	Y9	Y9
P20	Y4	Y6	Y8	Y8	Y8
P19	Y3	Y5	Y7	Y7	Y7
P18	Y2	Y4	Y6	Y6	Y6
P17	Y1	Y3	Y5	Y5	Y5
P16	Y0	Y2	Y4	Y4	Y4
P15	High-Z	Y1	Y3	Y3	High-Z
P14	High-Z	Y0	Y2	Y2	High-Z
P13	High-Z	High-Z	Y1	High-Z	High-Z
P12	High-Z	High-Z	Y0	High-Z	High-Z
P11	Cb7, Cr7	Cb9, Cr9	Cb11, Cr11	Cb11, Cr11	Cb11, Cr11
P10	Cb6, Cr6	Cb8, Cr8	Cb10, Cr10	Cb10, Cr10	Cb10, Cr10
P09	Cb5, Cr5	Cb7, Cr7	Cb9, Cr9	Cb9, Cr9	Cb9, Cr9
P08	Cb4, Cr4	Cb6, Cr6	Cb8, Cr8	Cb8, Cr8	Cb8, Cr8
P07	Cb3, Cr3	Cb5, Cr5	Cb7, Cr7	Cb7, Cr7	Cb7, Cr7
P06	Cb2, Cr2	Cb4, Cr4	Cb6, Cr6	Cb6, Cr6	Cb6, Cr6
P05	Cb1, Cr1	Cb3, Cr3	Cb5, Cr5	Cb5, Cr5	Cb5, Cr5
P04	Cb0, Cr0	Cb2, Cr2	Cb4, Cr4	Cb4, Cr4	Cb4, Cr4
P03	High-Z	Cb1, Cr1	Cb3, Cr3	Cb3, Cr3	High-Z
P02	High-Z	Cb0, Cr0	Cb2, Cr2	Cb2, Cr2	High-Z
P01	High-Z	High-Z	Cb1, Cr1	High-Z	High-Z
P00	High-Z	High-Z	Cb0, Cr0	High-Z	High-Z

Table 80. SDR 4:4:4 Output Modes

	SDR 4:4:4			
OP_FORMAT_SEL[7:0]	**0x40**	**0x41**	**0x42**	**0x46**
Pixel Output	**24-Bit SDR Mode 0**	**30-Bit SDR Mode 0**	**36-Bit SDR Mode 0**	**36-Bit SDR Mode 1**
P47	High-Z	High-Z	High-Z	High-Z
P46	High-Z	High-Z	High-Z	High-Z
P45	High-Z	High-Z	High-Z	High-Z
P44	High-Z	High-Z	High-Z	High-Z
P43	High-Z	High-Z	High-Z	High-Z
P42	High-Z	High-Z	High-Z	High-Z
P41	High-Z	High-Z	High-Z	High-Z
P40	High-Z	High-Z	High-Z	High-Z
P39	High-Z	High-Z	High-Z	High-Z
P38	High-Z	High-Z	High-Z	High-Z
P37	High-Z	High-Z	High-Z	High-Z
P36	High-Z	High-Z	High-Z	High-Z
P35	R7	R9	R11	R9
P34	R6	R8	R10	R8
P33	R5	R7	R9	R7
P32	R4	R6	R8	R6
P31	R3	R5	R7	R5
P30	R2	R4	R6	R4
P29	R1	R3	R5	R3
P28	R0	R2	R4	R2
P27	High-Z	R1	R3	R1
P26	High-Z	R0	R2	R0
P25	High-Z	High-Z	R1	G7
P24	High-Z	High-Z	R0	G6
P23	G7	G9	G11	G5
P22	G6	G8	G10	G4
P21	G5	G7	G9	G3
P20	G4	G6	G8	G2
P19	G3	G5	G7	G1
P18	G2	G4	G6	G0
P17	G1	G3	G5	B11
P16	G0	G2	G4	B10
P15	High-Z	G1	G3	B9
P14	High-Z	G0	G2	B8
P13	High-Z	High-Z	G1	G11
P12	High-Z	High-Z	G0	G10
P11	B7	B9	B11	B7
P10	B6	B8	B10	B6
P09	B5	B7	B9	B5
P08	B4	B6	B8	B4
P07	B3	B5	B7	B3
P06	B2	B4	B6	B2
P05	B1	B3	B5	B1
P04	B0	B2	B4	B0
P03	High-Z	B1	B3	R11
P02	High-Z	B0	B2	R10
P01	High-Z	High-Z	B1	G9
P00	High-Z	High-Z	B0	G8

Table 81. DDR 4:2:2 Output Modes

	DDR 4:2:2 Mode (Clock/2)					
OP_FORMAT_SEL[7:0]	**0x20**		**0x21**		**0x22**	
	8-Bit DDR ITU-656 Mode 0		**10-Bit DDR ITU-656 Mode 0**		**12-Bit DDR ITU-656 Mode 0**	
Pixel Output	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**
P47	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P46	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P45	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P44	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P43	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P42	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P41	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P40	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P39	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P38	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P37	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P36	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P35	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P34	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P33	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P32	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P31	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P30	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P29	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P28	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P27	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P26	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P25	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P24	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P23	Cb7, Cr7	Y7	Cb9, Cr9	Y9	Cb11, Cr11	Y11
P22	Cb6, Cr6	Y6	Cb8, Cr8	Y8	Cb10, Cr10	Y10
P21	Cb5, Cr5	Y5	Cb7, Cr7	Y7	Cb9, Cr9	Y9
P20	Cb4, Cr4	Y4	Cb6, Cr6	Y6	Cb8, Cr8	Y8
P19	Cb3, Cr3	Y3	Cb5, Cr5	Y5	Cb7, Cr7	Y7
P18	Cb2, Cr2	Y2	Cb4, Cr4	Y4	Cb6, Cr6	Y6
P17	Cb1, Cr1	Y1	Cb3, Cr3	Y3	Cb5, Cr5	Y5
P16	Cb0, Cr0	Y0	Cb2, Cr2	Y2	Cb4, Cr4	Y4
P15	High-Z	High-Z	Cb1, Cr1	Y1	Cb3, Cr3	Y3
P14	High-Z	High-Z	Cb0, Cr0	Y0	Cb2, Cr2	Y2
P13	High-Z	High-Z	High-Z	High-Z	Cb1, Cr1	Y1
P12	High-Z	High-Z	High-Z	High-Z	Cb0, Cr0	Y0
P11	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P10	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P09	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P08	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P07	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P06	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P05	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P04	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P03	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P02	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P01	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P00	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z

Table 82. DDR 4:4:4 Output Modes

	DDR 4:4:4 Mode (Clock/2)					
OP_FORMAT_SEL[7:0]	**0x60**		**0x61**		**0x62**	
	24-Bit DDR Mode 0		**30-Bit DDR Mode 0**		**36-Bit DDR Mode 0**	
Pixel Output	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**
P47	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P46	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P45	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P44	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P43	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P42	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P41	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P40	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P39	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P38	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P37	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P36	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P35	R7-0	R7-1	R9-0	R9-1	R11-0	R11-1
P34	R6-0	R6-1	R8-0	R8-1	R10-0	R10-1
P33	R5-0	R5-1	R7-0	R7-1	R9-0	R9-1
P32	R4-0	R4-1	R6-0	R6-1	R8-0	R8-1
P31	R3-0	R3-1	R5-0	R5-1	R7-0	R7-1
P30	R2-0	R2-1	R4-0	R4-1	R6-0	R6-1
P29	R1-0	R1-1	R3-0	R3-1	R5-0	R5-1
P28	R0-0	R0-1	R2-0	R2-1	R4-0	R4-1
P27	High-Z	High-Z	R1-0	R1-1	R3-0	R3-1
P26	High-Z	High-Z	R0-0	R0-1	R2-0	R2-1
P25	High-Z	High-Z	High-Z	High-Z	R1-0	R1-1
P24	High-Z	High-Z	High-Z	High-Z	R0-0	R0-1
P23	G7-0	G7-1	G9-0	G9-1	G11-0	G11-1
P22	G6-0	G6-1	G8-0	G8-1	G10-0	G10-1
P21	G5-0	G5-1	G7-0	G7-1	G9-0	G9-1
P20	G4-0	G4-1	G6-0	G6-1	G8-0	G8-1
P19	G3-0	G3-1	G5-0	G5-1	G7-0	G7-1
P18	G2-0	G2-1	G4-0	G4-1	G6-0	G6-1
P17	G1-0	G1-1	G3-0	G3-1	G5-0	G5-1
P16	G0-0	G0-1	G2-0	G2-1	G4-0	G4-1
P15	High-Z	High-Z	G1-0	G1-1	G3-0	G3-1
P14	High-Z	High-Z	G0-0	G0-1	G2-0	G2-1
P13	High-Z	High-Z	High-Z	High-Z	G1-0	G1-1
P12	High-Z	High-Z	High-Z	High-Z	G0-0	G0-1
P11	B7-0	B7-1	B9-0	B9-1	B11-0	B11-1
P10	B6-0	B6-1	B8-0	B8-1	B10-0	B10-1
P09	B5-0	B5-1	B7-0	B7-1	B9-0	B9-1
P08	B4-0	B4-1	B6-0	B6-1	B8-0	B8-1
P07	B3-0	B3-1	B5-0	B5-1	B7-0	B7-1
P06	B2-0	B2-1	B4-0	B4-1	B6-0	B6-1
P05	B1-0	B1-1	B3-0	B3-1	B5-0	B5-1
P04	B0-0	B0-1	B2-0	B2-1	B4-0	B4-1
P03	High-Z	High-Z	B1-0	B1-1	B3-0	B3-1
P02	High-Z	High-Z	B0-0	B0-1	B2-0	B2-1
P01	High-Z	High-Z	High-Z	High-Z	B1-0	B1-1
P00	High-Z	High-Z	High-Z	High-Z	B0-0	B0-1

Note that in Table 82, xxx-0 corresponds to odd samples and xxx-1 corresponds to even samples.

Table 83. Special SDR 4:2:2 and 4:4:4 Output Modes for Video with Pixel Clock Frequencies above 150 MHz

	2 x SDR 4:2:2 Interleaved			2 x SDR 4:4:4 Interleaved
OP_FORMAT_SEL[7:0]	**0x94**	**0x95**	**0x96**	**0x54**
Pixel Output	**2 × 16-Bits Mode 0[1]**	**2 × 20-Bits Mode 0[1]**	**2 × 24-Bits Mode 0[1]**	**2 × 24-Bits Mode 0[1]**
P47	Y7-0	Y9-0	Y11-0	G7-0
P46	Y6-0	Y8-0	Y10-0	G6-0
P45	Y5-0	Y7-0	Y9-0	G5-0
P44	Y4-0	Y6-0	Y8-0	G4-0
P43	Y3-0	Y5-0	Y7-0	G3-0
P42	Y2-0	Y4-0	Y6-0	G2-0
P41	Y1-0	Y3-0	Y5-0	G1-0
P40	Y0-0	Y2-0	Y4-0	G0-0
P39	High-Z	Y1-0	Y3-0	B7-0
P38	High-Z	Y0-0	Y2-0	B6-0
P37	High-Z	High-Z	Y1-0	B5-0
P36	High-Z	High-Z	Y0-0	B4-0
P35	Cb7-0	Cb9-0	Cb11-0	B3-0
P34	Cb6-0	Cb8-0	Cb10-0	B2-0
P33	Cb5-0	Cb7-0	Cb9-0	B1-0
P32	Cb4-0	Cb6-0	Cb8-0	B0-0
P31	Cb3-0	Cb5-0	Cb7-0	R7-0
P30	Cb2-0	Cb4-0	Cb6-0	R6-0
P29	Cb1-0	Cb3-0	Cb5-0	R5-0
P28	Cb0-0	Cb2-0	Cb4-0	R4-0
P27	High-Z	Cb1-0	Cb3-0	R3-0
P26	High-Z	Cb0-0	Cb2-0	R2-0
P25	High-Z	High-Z	Cb1-0	R1-0
P24	High-Z	High-Z	Cb0-0	R0-0
P23	Y7-1	Y9-1	Y11-1	G7-1
P22	Y6-1	Y8-1	Y10-1	G6-1
P21	Y5-1	Y7-1	Y9-1	G5-1
P20	Y4-1	Y6-1	Y8-1	G4-1
P19	Y3-1	Y5-1	Y7-1	G3-1
P18	Y2-1	Y4-1	Y6-1	G2-1
P17	Y1-1	Y3-1	Y5-1	G1-1
P16	Y0-1	Y2-1	Y4-1	G0-1
P15	High-Z	Y1-1	Y3-1	B7-1
P14	High-Z	Y0-1	Y2-1	B6-1
P13	High-Z	High-Z	Y1-1	B5-1
P12	High-Z	High-Z	Y0-1	B4-1
P11	Cr7-0	Cr9-0	Cr11-0	B3-1
P10	Cr6-0	Cr8-0	Cr10-0	B2-1
P09	Cr5-0	Cr7-0	Cr9-0	B1-1
P08	Cr4-0	Cr6-0	Cr8-0	B0-1
P07	Cr3-0	Cr5-0	Cr7-0	R7-1
P06	Cr2-0	Cr4-0	Cr6-0	R6-1
P05	Cr1-0	Cr3-0	Cr5-0	R5-1
P04	Cr0-0	Cr2-0	Cr4-0	R4-1
P03	High-Z	Cr1-0	Cr3-0	R3-1
P02	High-Z	Cr0-0	Cr2-0	R2-1
P01	High-Z	High-Z	Cr1-0	R1-1
P00	High-Z	High-Z	Cr0-0	R0-1

[1] The 0x54, 0x94, 0x95, 0x96 modes registers should be set as following:
DPLL Map, Register 0xC3 to Register 0x80
DPLL Map, Register 0xCF to Register 0x03.
IO Map, Register 0xDD to Register 0xA0.
IO Map, Register 0xBF[0] = 0 (CP_COMPLETE_BYPASS_IN_HDMI_MODES disabled).

Note that in Table 83, xxx-0 corresponds to odd samples and xxx-1 - corresponds to even samples.

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

UG09581-0-2/14(C)