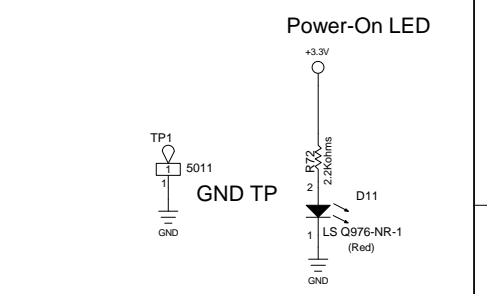
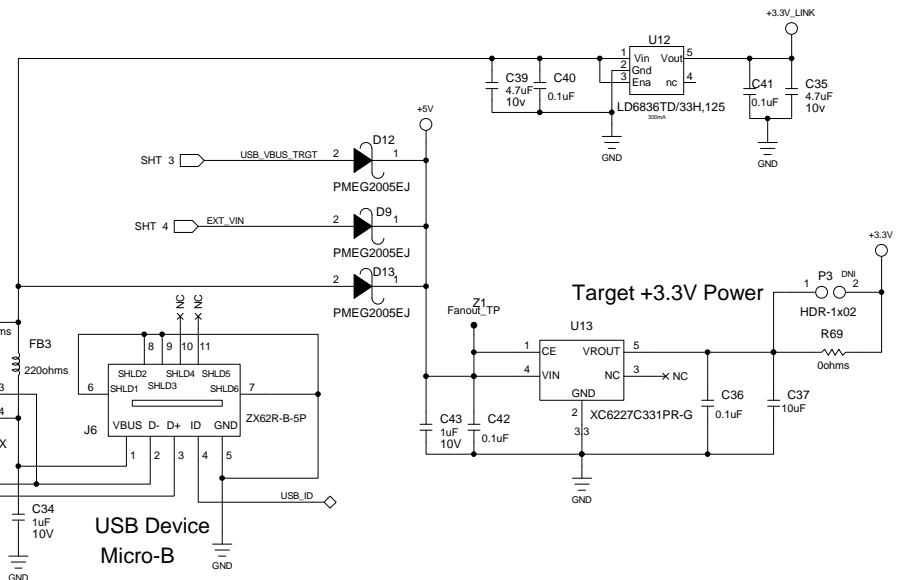
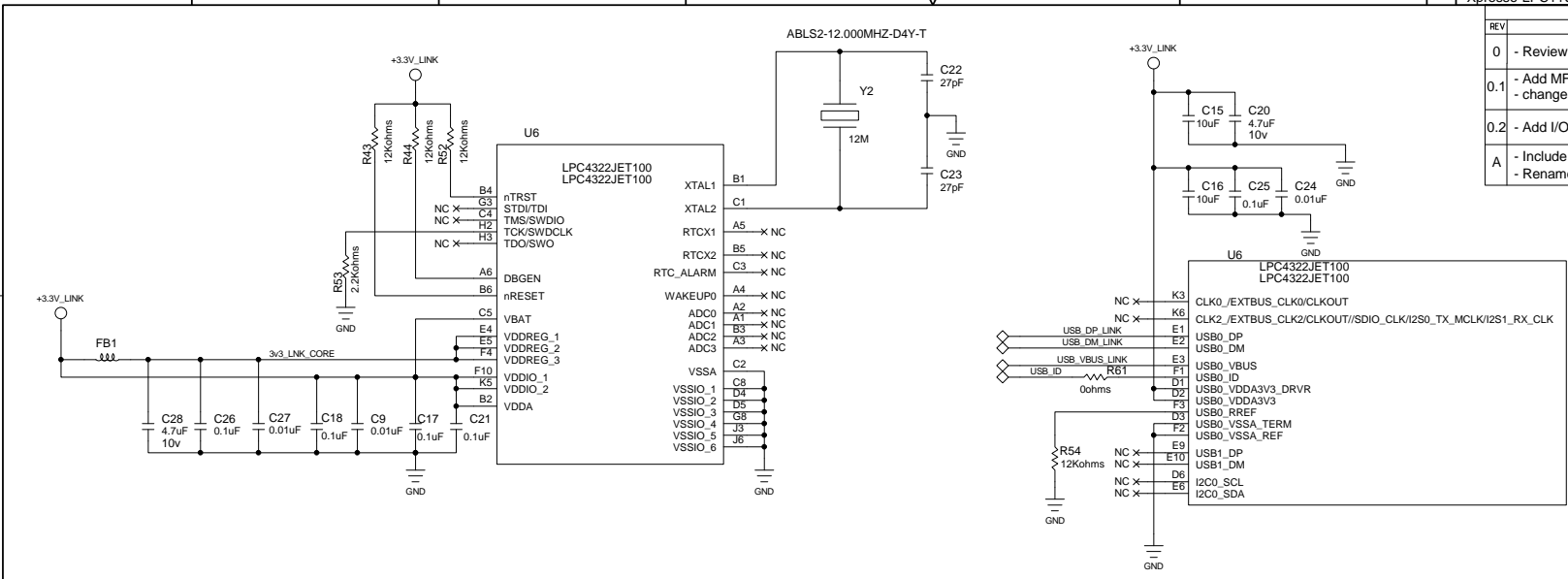


REV	DESCRIPTION	DATE	APPROVED
0	- Review	09/10/2013	
0.1	- Add MFA100 I2S support; - change Arduino connections	09/30/2013	
0.2	- Add I/OH Add-on brds (sht 6)	09/30/2013	
A	- Include review comments in design - Rename Refdes; Release to fab	10/02/2013	



CONTRACT NO.		LINK2 LPC4322	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio 10/14/2013	411 E. Plumeria Dr San Jose, CA 95134	
CHECKED		www.standards.nxp.com/microcontrollers/	
ISSUED	10/02/13	SIZE	FSCM NO.
		D	Xpresso-LPC11U37H
		SCALE	DWG. NO.
			1 OF 06

U6
LPC4322JET100
LPC4322JET100

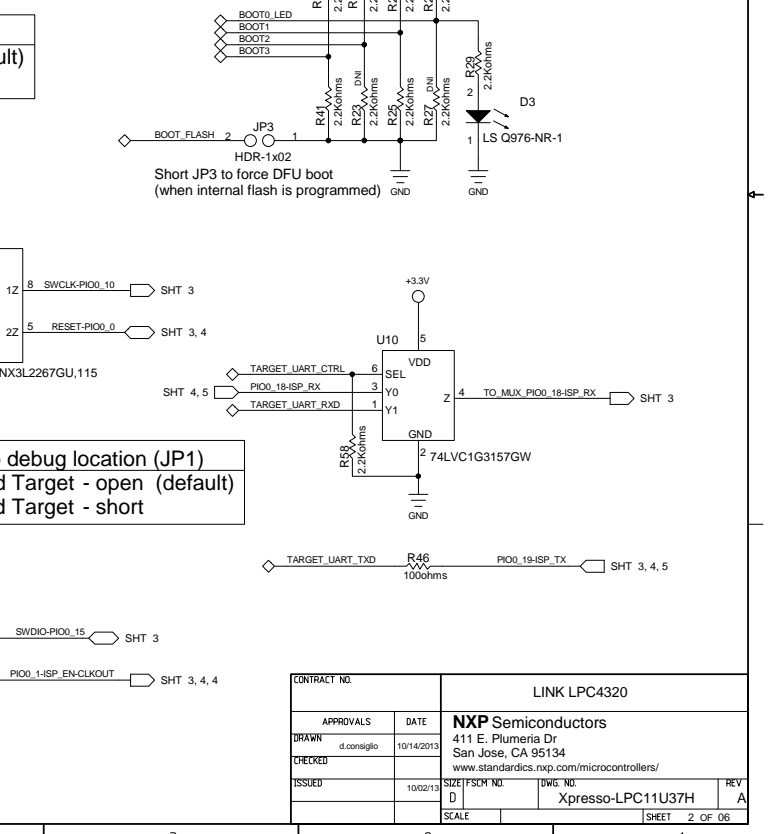
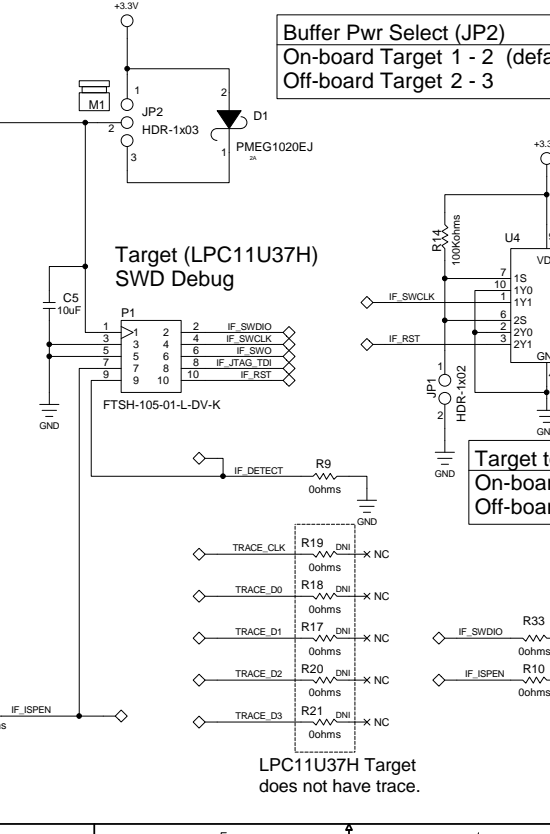
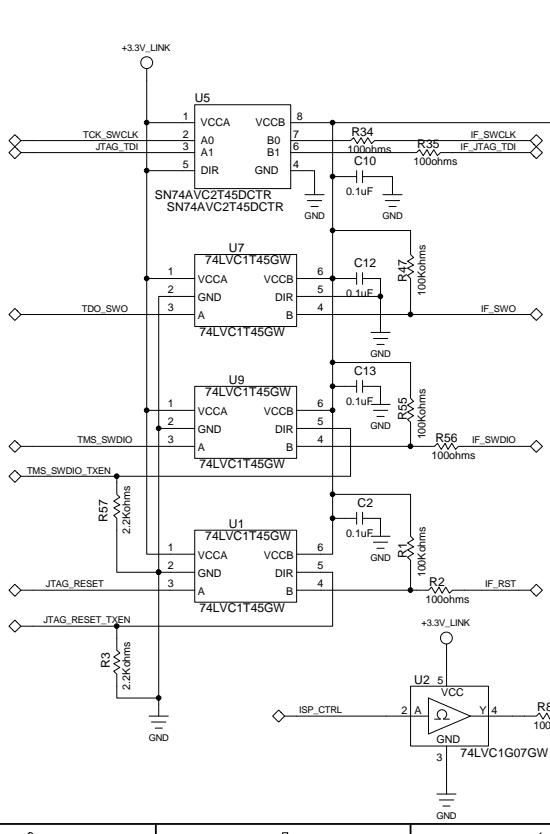
P0[0]_GPIO[0]SSP1_MISO/ENET_RXD1/SGPIO0	G2
P0[1]_GPIO[1]SSP1_MOSI/ENET_TXEN/SGPIO1	G1
P1[0]_GPIO[4]CTIN_3/EXTBUS_A5	H1
P1[1]_GPIO[8]C/OUT_7/EXTBUS_A6/SGPIO8	K2
P1[2]_GPIO[9]C/OUT_6/EXTBUS_A7/SGPIO9	K1
P1[3]_GPIO[10]C/OUT_8/SGPIO10/EXTBUS_OE	J1
P1[4]_GPIO[11]C/OUT_9/SGPIO11/EXTBUS_BLS0	J2
P1[5]_GPIO[18]C/OUT_10/NC/EXTBUS_CS0	J4
P1[6]_GPIO[19]CTIN_5/NC/EXTBUS_VE	K4
P1[7]_GPIO[9]U1_DSRC/OUT_13/EXTBUS_D0	G4
P1[8]_GPIO[1]U1_DTR/C/OUT_12/EXTBUS_D1	H5
P1[9]_GPIO[2]U1_RTS/C/OUT_11/EXTBUS_D2	J5
P1[10]_GPIO[3]U1_RI/C/OUT_14/EXTBUS_D3	H6
P1[11]_GPIO[14]U1_CTS/C/OUT_15/EXTBUS_D4	J7
P1[12]_GPIO[5]U1_DCD/NC/EXTBUS_D5	H7
P1[13]_GPIO[6]U1_TXD/NC/EXTBUS_D6	J8
P1[14]_GPIO[7]U1_RXD/NC/EXTBUS_D7	K8
P1[15]_GPIO[2]U2_TXD/S/SP02/ENET_RXD0	J9
P1[16]_GPIO[3]U2_RXD/S/SP03/ENET_RX_DV	H9
P1[17]_GPIO[12]U2_UCLK/NC/ENET_MDIO	J10
P1[18]_GPIO[13]U2_DIR/NC/ENET_TXD0	H10
P1[19]_ENET_TX_REF_CLK/SSP1_SCK/CLK/OUT/IZS1_RX_SCK	K9
P1[20]_GPIO[15]SSP1_SSEL/NC/ENET_TXD1	K10

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LPC4322JET100
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TARGET_UART_RXD	G10
TARGET_UART_TXD	G7
TARGET_UART_CTRL	F5
ISP_CTRL	D8
JTAG_RESET	D9
JTAG_RESET_TXEN	C9
BOOT_FLASH	C10
BOOT2	C6
BOOT3	B10
NC	A9
NC	A8
NC	B9
NC	A10
IF_DETECT	R22
NC	A8
NC	F7
NC	A7
NC	B8
NC	B7
NC	C7
NC	D7
NC	E7
P3[0]_I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK	A3
P3[1]_I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]	A4
P3[2]_I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]	A5
P3[3]_SPI_SCK/SSP0_SCK/SPIFI_SCK	A6
P3[4]_GPIO[14]//SPIFI_SIO3	A7
P3[5]_GPIO[15]//SPIFI_SIO2	A8
P3[6]_GPIO[6]SPI_MISO/SSP0_SSEL/SPIFI_MOSI	A9
P3[7]_SPI_MOSI/SSP0_MISO/SPIFI_MOSI	A10
P3[8]_SPI_SSEL/SSP0_MOSI/SPIFI_CS	A11

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LPC4322JET100
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NC	H7
NC	G5
NC	J9
NC	F6
NC	F9
NC	F8
NC	C9
NC	H4
P6[0]_I2S0_RX_MCLK/I2S0_RX_SCK	H7
P6[1]_GPIO[30]EXTBUS_nDVCYS1/U0_UCLK/I2S0_RX_WS	J9
P6[2]_GPIO[31]EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA	J9
P6[4]_GPIO[3]CTIN_6/U0_TXD/EXTBUS_nCAS	F6
P6[5]_GPIO[4]C/OUT_6/U0_RXD/EXTBUS_nRAS	F9
P6[9]_GPIO[5]NC/NC/EXTBUS_nDVCYS0	F8
P6[11]_GPIO[37]NC/NC/EXTBUS_CKEOUT0	C9
PF[4]_SSP1_SCK/SPIFI_CLKIN/TRACECLK/I2S_TX_MCLK/I2S_RX_MCLK	H4



Buffer Pwr Select (JP2)
On-board Target 1 - 2 (default)
Off-board Target 2 - 3

Target (LPC11U37H)
SWD Debug

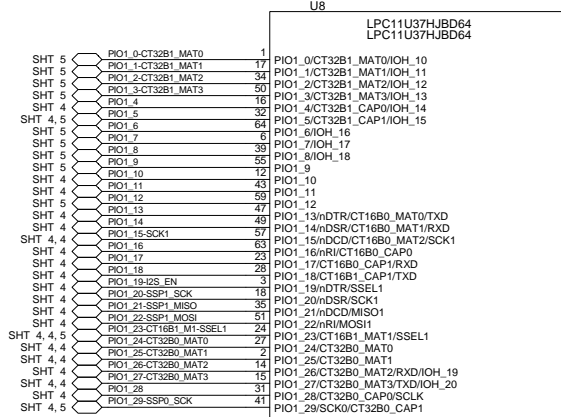
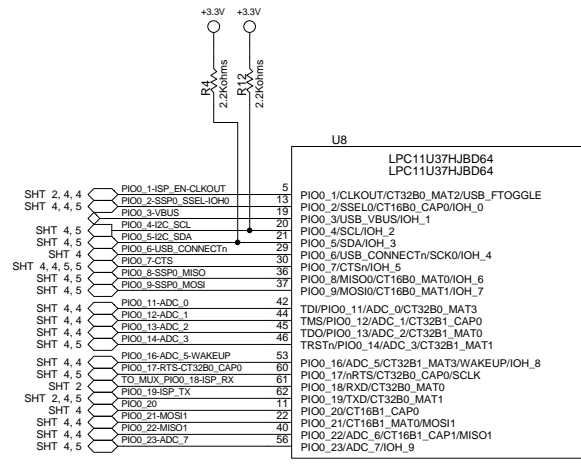
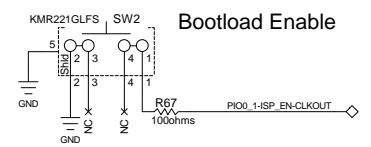
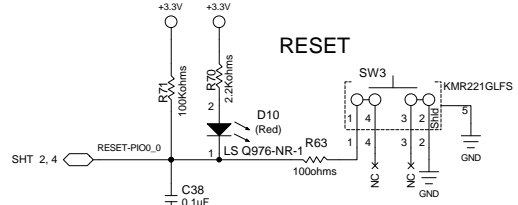
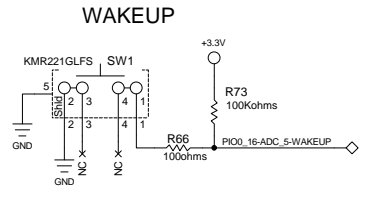
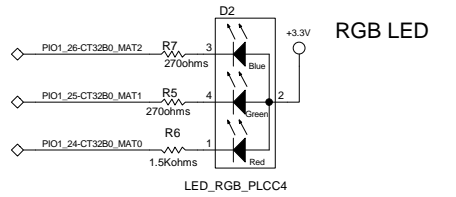
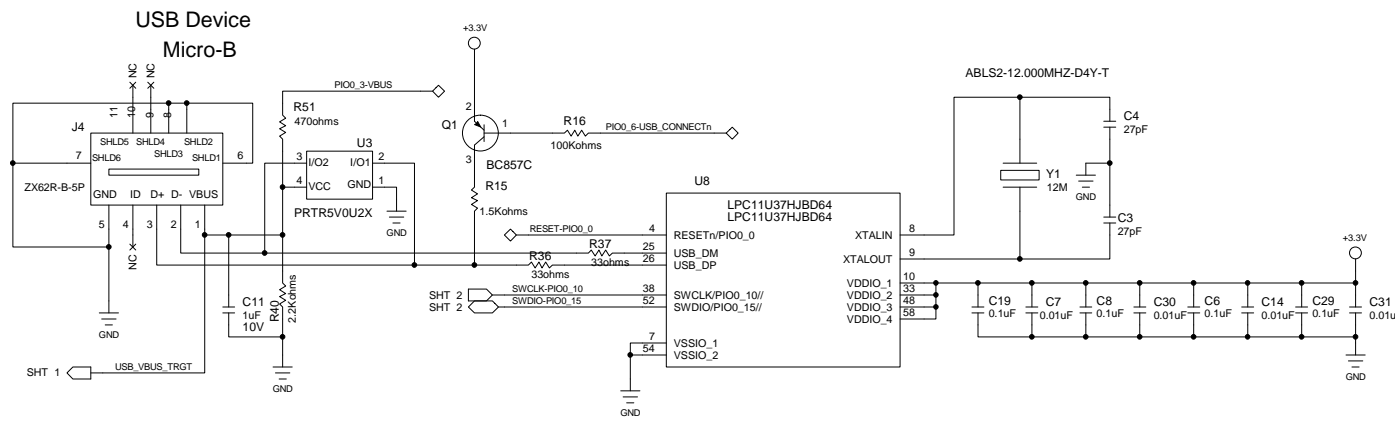
Target to debug location (JP1)
On-board Target - open (default)
Off-board Target - short

LPC4322 Boot mode
DFU USB0 = B3:0 = 0101

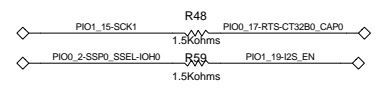
LPC11U37H Target
does not have trace.

CONTRACT NO.		LINK LPC4320	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	10/14/2013	San Jose, CA 95134	
ISSUED	10/02/13	www.standards.nxp.com/microcontrollers/	
SCALE		SIZE FSCM NO.	DWG NO.
		D	Xpresso-LPC11U37H
			REV A
			SHEET 2 OF 06

DWG. NO. Xpresso-LPC11U37H		SR. 3	REV. A
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

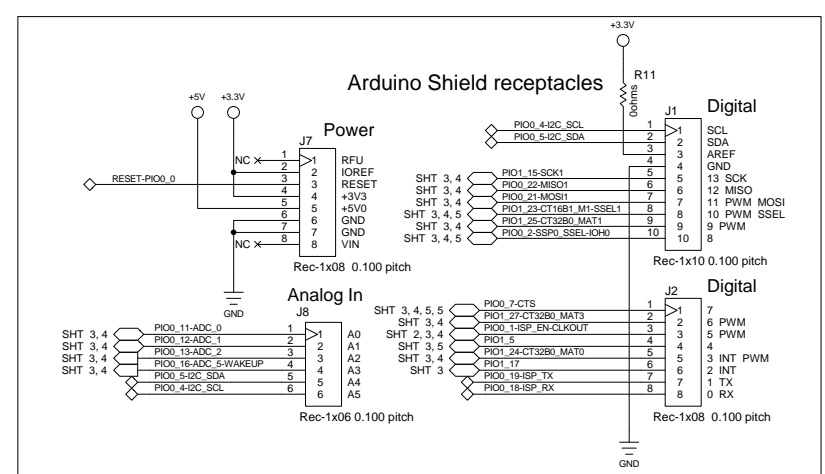
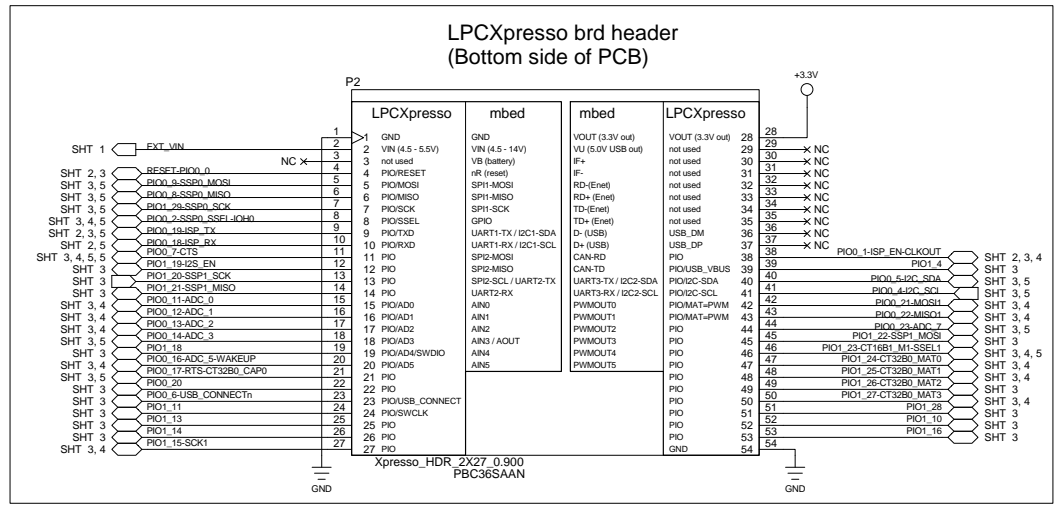


ISP Boot Modes		
Mode	PIO0_1	PIO0_3
No ISP (Flash)	high	X
USB	low	high
UART0	low	low

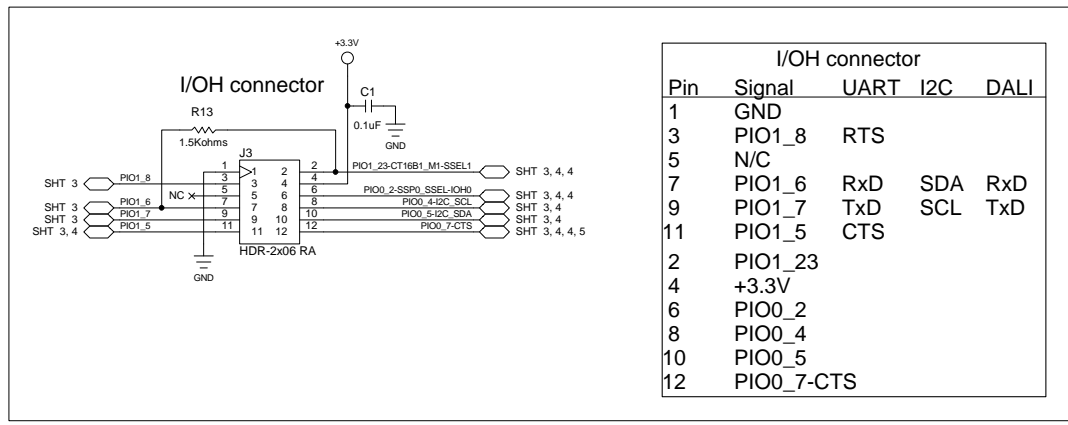


CONTRACT NO.		Target LPC11U37H	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	10/14/2013	San Jose, CA 95134	
ISSUED	10/02/13	www.standards.nxp.com/microcontrollers/	
SIZE FSC#	NO.	Xpresso-LPC11U37H	
D		REV A	
SCALE		SHEET 3 OF 06	

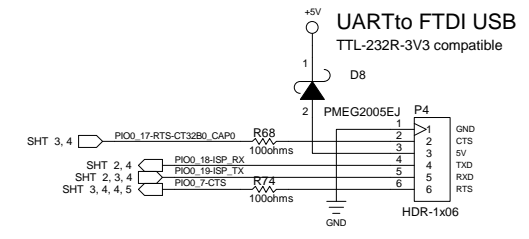
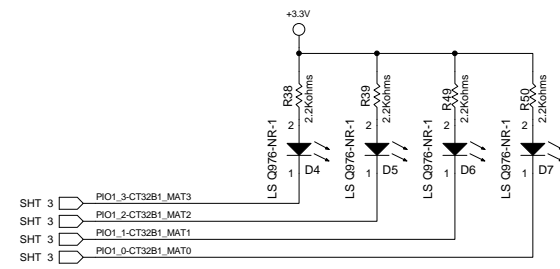
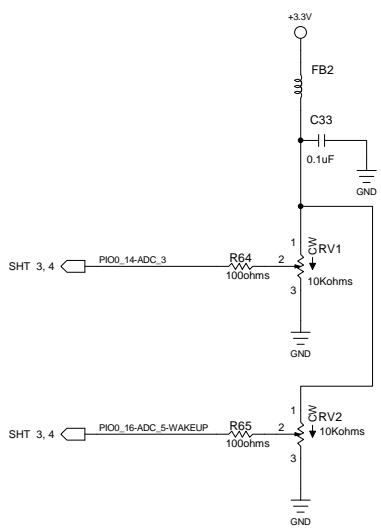
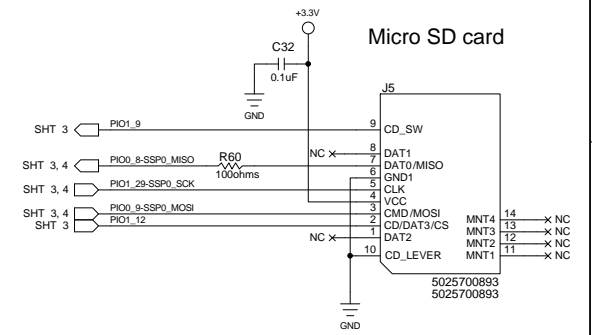
Pkg No		Rev		Rev	
Xpresso-LPC11U37H		4		A	
REVISIONS					
REV	DESCRIPTION	DATE	APPROVED		



CONTRACT NO.		Xpresso MC/Arduino headers	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	10/14/2013	San Jose, CA 95134	
ISSUED	10/02/13	www.standards.nxp.com/microcontrollers/	
SIZE	FSCM NO.	DWG. NO.	REV
D		Xpresso-LPC11U37H	A
SCALE		SHEET 4 OF 06	

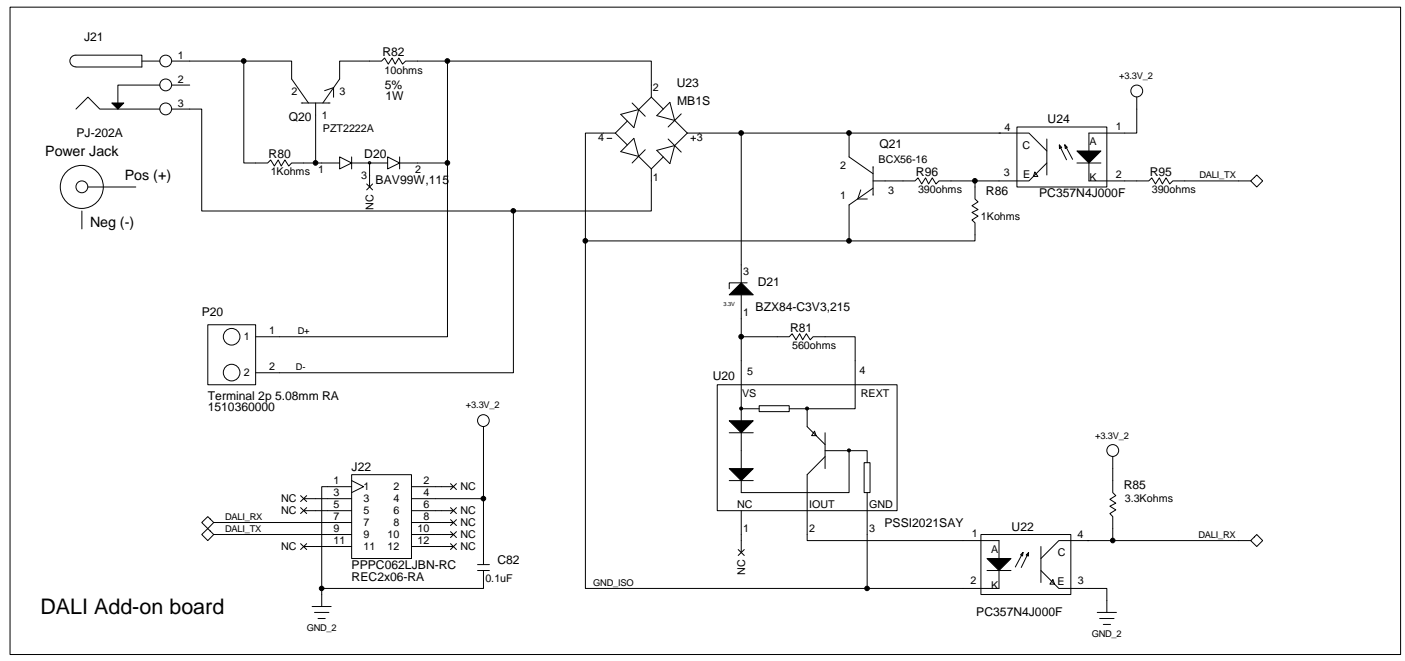
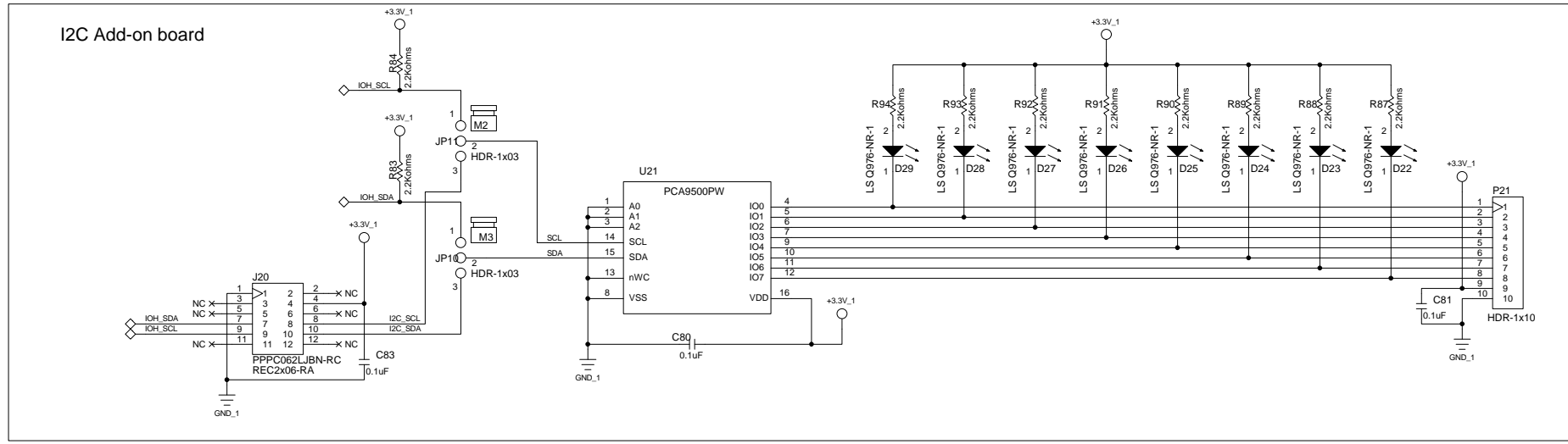


Pin	Signal	UART	I2C	DALI
1	GND			
3	PIO1_8	RTS		
5	N/C			
7	PIO1_6	RxD	SDA	RxD
9	PIO1_7	TxD	SCL	TxD
11	PIO1_5	CTS		
2	PIO1_23			
4	+3.3V			
6	PIO0_2			
8	PIO0_4			
10	PIO0_5			
12	PIO0_7-CTS			



CONTRACT NO.		IO/H, FTDI	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio 10/15/2013	411 E. Plumeria Dr	
CHECKED		San Jose, CA 95134	
		www.standards.nxp.com/microcontrollers/	
ISSUED	10/02/13	SIZE	DWG. NO.
		D	Xpresso-LPC11U37H
		SCALE	SHEET 5 OF 06

DWG. NO. Xpresso-LPC11U37H		REV. 6	REV. A
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		IO/H Add-on boards	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio 10/14/2013	411 E. Plumeria Dr San Jose, CA 95134 www.standards.nxp.com/microcontrollers/	
CHECKED		SIZE	DWG. NO.
ISSUED	10/02/13	D	Xpresso-LPC11U37H
SCALE		SHEET 6 OF 06	