ADRV9026 Quad-Channel, Wideband RF Transceiver Platform

200 MHz Bandwidth Integrated Radio Transceiver Solution

Smallest Size, Lowest Power Transceiver Solution for Base Transceiver Stations (BTS)

- Smallest size reduces footprint and enhances form factor flexibility
- 50% power consumption reduction over previous generation ADRV9009 for increased radio density
- Enables ORAN small cell designs with lowest system power and cost

Highly Integrated, High Performance Software-Defined Radio

- 2× integration over ADRV9009
- Supports up to 200 MHz bandwidth and covers all bands from 650 MHz to 6 GHz[1]

Common Platform Design for 3G/4G/5G Reduces Complexity, Development Costs, and Time to Market

- Single-chip FDD/TDD solution simplifies hardware and software development
- Common API across multiple applications
- Reduces product development cycles for band and power variants
- Enables modular architecture for scalable radio solutions

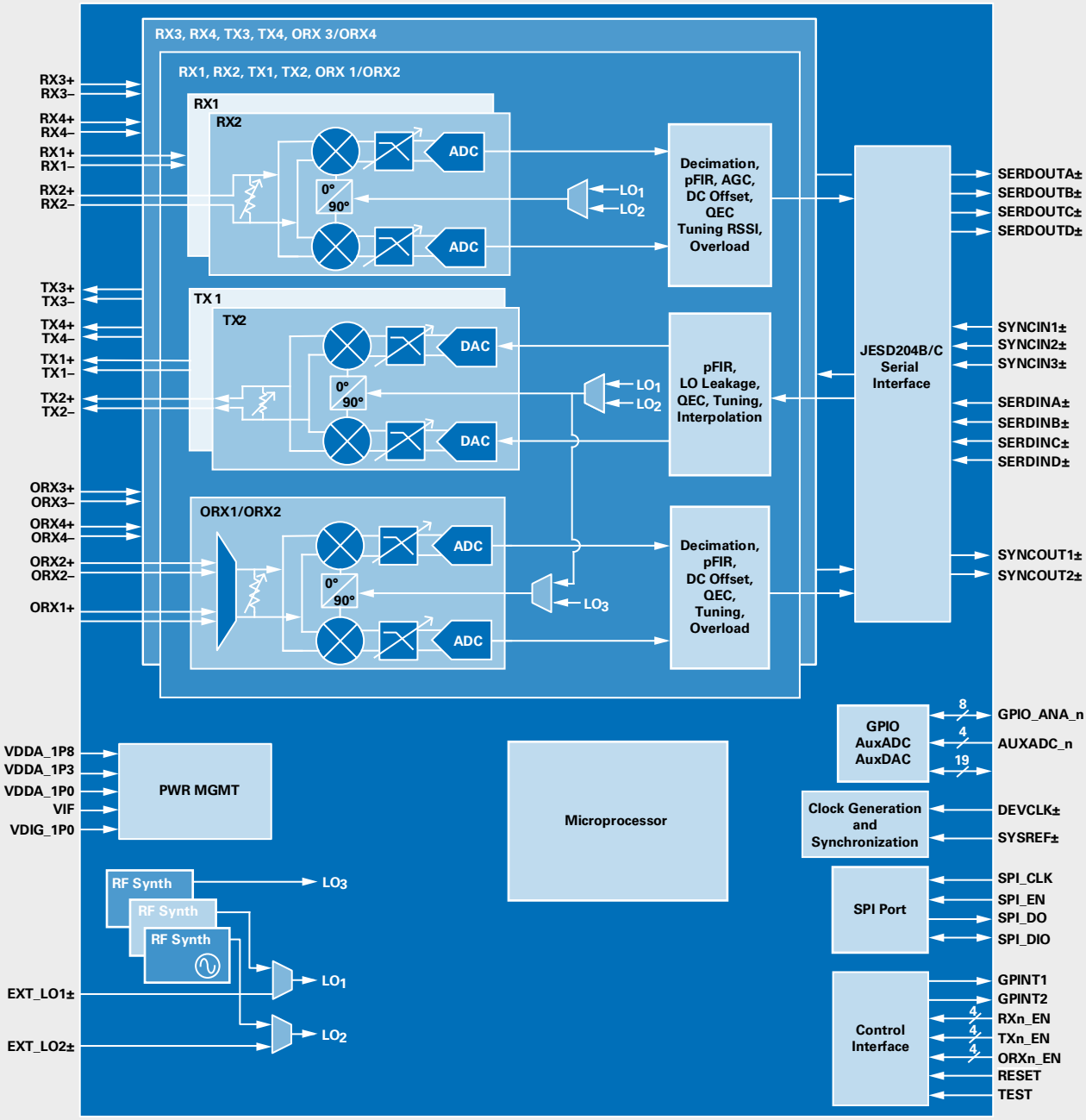
[1]See page 3 for future enhancements in the ADRV902x family roadmap

Applications

- Macro base stations
- Massive MIMO
- Small cell designs

VISIT ANALOG.COM

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™


RX3, RX4, TX3, TX4, ORX 3/ORX4
RX1, RX2, TX1, TX2, ORX 1/ORX2
RX1
RX2
RX3+
RX3–
RX4+
RX4–
RX1+
RX1–
RX2+
RX2–
ADC
0°
90°
LO1
LO2
Decimation, pFIR, AGC, DC Offset, QEC Tuning RSSI, Overload
TX 1
TX2
TX3+
TX3–
TX4+
TX4–
TX1+
TX1–
TX2+
TX2–
DAC
pFIR, LO Leakage, QEC, Tuning, Interpolation
ORX1/ORX2
ORX3+
ORX3–
ORX4+
ORX4–
ORX2+
ORX2–
ORX1+
LO3
Decimation, pFIR, DC Offset, QEC, Tuning, Overload
JESD204B/C Serial Interface
SERDOUTA±
SERDOUTB±
SERDOUTC±
SERDOUTD±
SYNCIN1±
SYNCIN2±
SYNCIN3±
SERDINA±
SERDINB±
SERDINC±
SERDIND±
SYNCOUT1±
SYNCOUT2±
VDDA_1P8
VDDA_1P3
VDDA_1P0
VIF
VDIG_1P0
PWR MGMT
Microprocessor
GPIO AuxADC AuxDAC
8
4
19
GPIO_ANA_n
AUXADC_n
Clock Generation and Synchronization
DEVCLK±
SYSREF±
SPI Port
SPI_CLK
SPI_EN
SPI_DO
SPI_DIO
RF Synth
RF Synth
RF Synth
LO3
LO1
LO2
EXT_LO1±
EXT_LO2±
Control Interface
GPINT1
GPINT2
RXn_EN
TXn_EN
ORXn_EN
RESET
TEST
4
4
4

ADRV9026 Overview

- Four differential transmitters
- Four differential receivers
- Two observation receivers with two inputs each
- Center frequency: 650 MHz to 6000 MHz
- Maximum receiver bandwidth: 200 MHz
- Maximum transmitter bandwidth: 200 MHz
- Maximum transmitter synthesis bandwidth: 450 MHz

See roadmap below for future enhancements

- Maximum observation receiver bandwidth: 450 MHz
- Fully integrated independent fractional-N radio frequency synthesizers
- Fully integrated clock synthesizer
- Multichip phase synchronization for all local oscillators and baseband clocks
- Support of TDD/FDD 3G/4G/5G applications
- 16 Gbps JESD204B/C digital interface

ADRV9026 Family Roadmap

Enhanced features and functions will be added to the ADRV9026 over time, including:

- 25 Gbps SERDES support
- Extending LO frequency range down to 75 MHz
- Support for an external LO
- Filter Wizard to generate custom profiles

An enhanced version from the ADRV902x family will be released in 2020 with integrated DPD and CFR, reducing FPGA requirements, as well as lowering total system power and cost.

RadioVerse Ecosystem and Partnerships

RadioVerse® is a design and technology ecosystem for advanced radio design and development. We offer market-leading integrated transceiver technology, software tools, evaluation and prototyping platforms, a range of reference designs, and radio solutions. RadioVerse is building up a global partnership network to provide customers all levels of design support. ADRV9026's partner network and reference design ecosystem will be launched on *analog.com/radioverse* in 2020.

ADI RadioVerse™

Evaluation System

The evaluation system comprises an FPGA carrier board ADS9-V2EBZ and a radio daughtercard, coming with two frequency bands of matching: –HB for 2.8 GHz to 6 GHz and –MB for 650 MHz to 2.8 GHz. Compatible evaluation software is provided for download, including API library, Windows GUI, and a binary image for FPGA configuration.

	Radio Cards	Carrier Boards	Software and Driver
Evaluation System	► ADRV902X-HB/PCBZ (for 2.8 GHz to 6 GHz) ► ADRV902X-MB/PCBZ (for 650 MHz to 2.8 GHz)	► ADS9-V2EBZ (FPGA motherboard with Xilinx® UltraScale+™)	► Operating system-agnostic API source in ANSI C ► Windows GUI for transceiver configuration and data capture ► Binary image for FPGA configuration

EngineerZone® Online Support Community

ADI EngineerZone™ SUPPORT COMMUNITY

Engage with the Analog Devices technology experts in our online support community. Ask your tough design questions, browse FAQs, or join a conversation.

Visit *ez.analog.com*

Circuits from the Lab Reference Designs

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are built and tested by ADI engineers with comprehensive documentation and factory-tested evaluation hardware.

Visit *analog.com/cftl*

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

VISIT ANALOG.COM

For regional headquarters, sales, and distributors or to contact customer service and technical support, visit analog.com/contact.

Ask our ADI technology experts tough questions, browse FAQs, or join a conversation at the EngineerZone Online Support Community. Visit ez.analog.com.

PH21775-11/19(A)