HITACHI®

SEMICONDUCTOR DEVICES FOR COMMUNICATION APPLICATIONS DATA BOOK

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- For Facsimile System Application
- Application for Data Communication System
- Application for Optical Fiber Communication System

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- Reliability
- Quality Assurance
- Reliability Test Methods and Test Results
- Notes on Using

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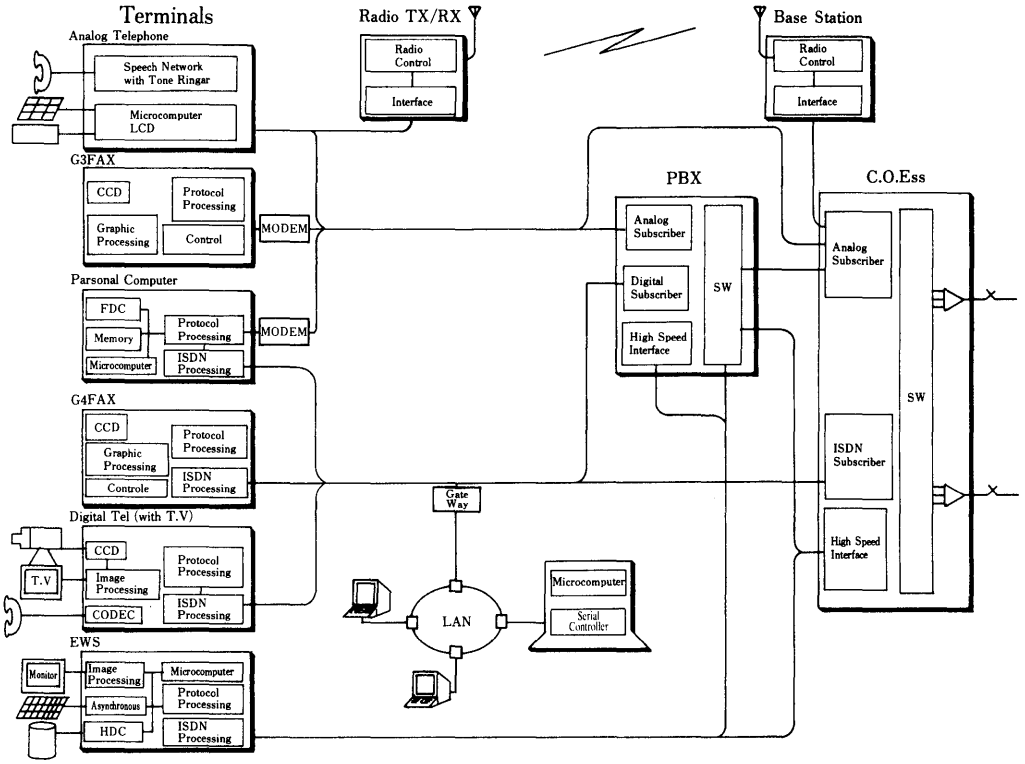
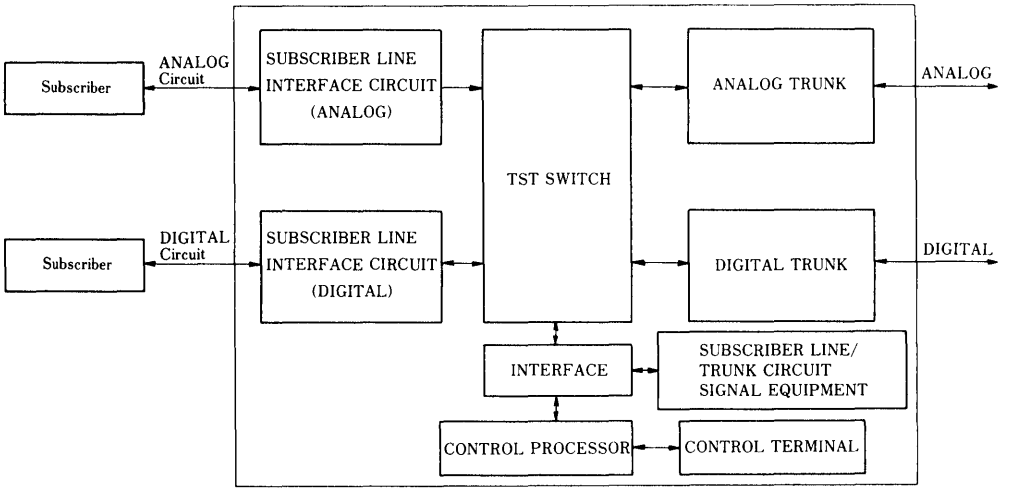
SELECTION GUIDES FOR APPLICATIONS

1. TELECOM NETWORK SYSTEM



2. FOR PABX (Private Auto Branch Exchange) APPLICATION

(1) For example structure of system

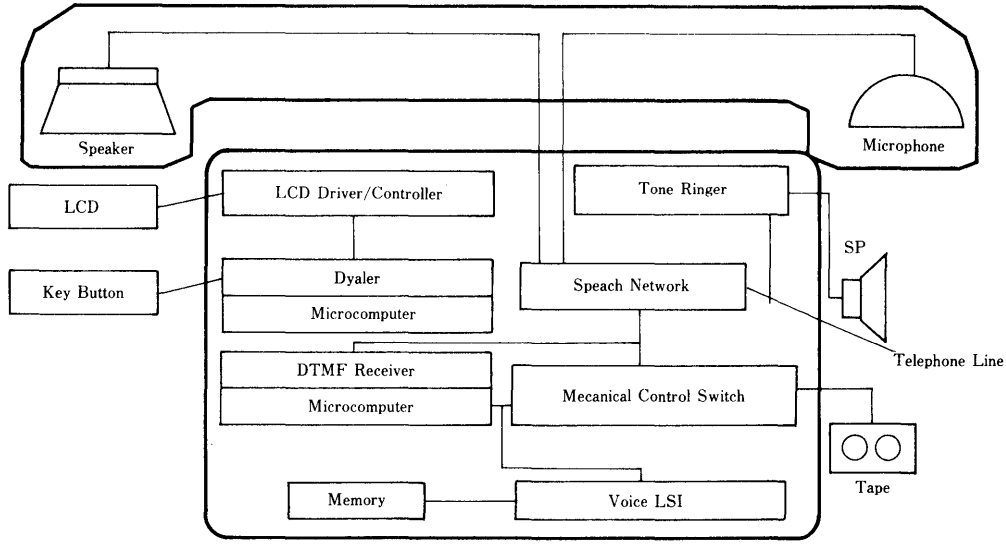


(2) Semiconductor lineup

	Used Semiconductor	Hitachi Product Lineup
Analog Subscriber	RT BSH CODEC MP GATE ARRAY	HA16811ANT/AMP HA16817NT/MP HD44230 SERIES HITACHI STANDARD IC
Digital Subscriber	FEED IC MP GATE ARRAY	HITACHI STANDARD IC
TST Switch	MP GATE ARRAY	HITACHI STANDARD IC
Analog Transmission	CODEC MP GATE ARRAY	HD44230 SERIES HITACHI STANDARD IC
Digital Transmission	X25 MP GATE ARRAY	HITACHI STANDARD IC
Subscriber Line/ Trunk Circuit Signal Equipment	MP AD/DA	HITACHI STANDARD IC HITACHI STANDARD IC
Control Processor	MP MEMORY GATE ARRAY	HITACHI STANDARD IC

3. FOR TELEPHONE SET APPLICATION

(1)-(A) For Example Structure of System (Feature phone/Answering Machine)

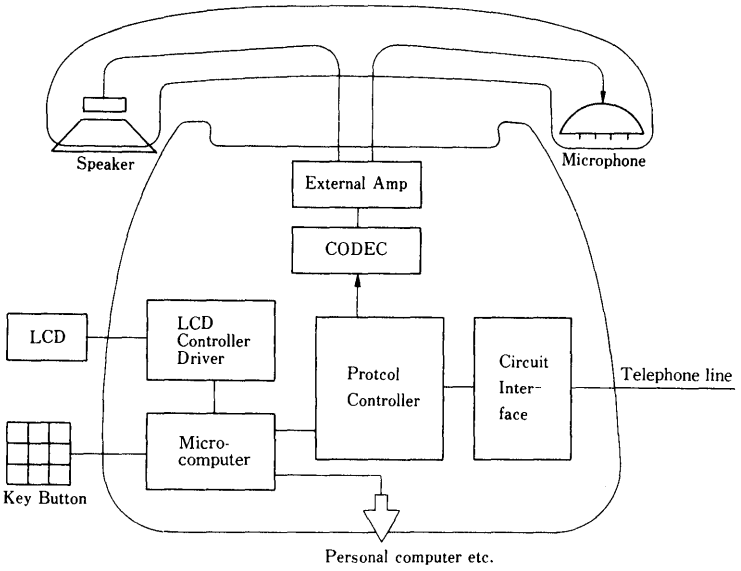


(2)-(A) Semiconductor line up

Function		Hitachi Products	
Tone ringer	Ringing signal detection	HA16802/4/5	
	Ringing sound generation		
Speech network	2W-4W conversion	HA16821	HA16808A
	AGC function	HA16822*	
Speaker amp	Loud speaker function	HA16820	
Dialer	DTMF signal transmission	HD61826	HMCS4608
	Dial pulse transmission	HD61825	
Display	LCD display	HD44780	HMCS4808
Repertory	Repertory dialing One louch dialing	HMCS404/414	
Microcomputer with DTMF receiver		HMCS4678	
Control switches for answering machine		HA12089/HA12189	
ADPCM for IC recording		HD81801/HD81802	

* Under development

(1)-(B) For example structure of system (Digital Telephone)

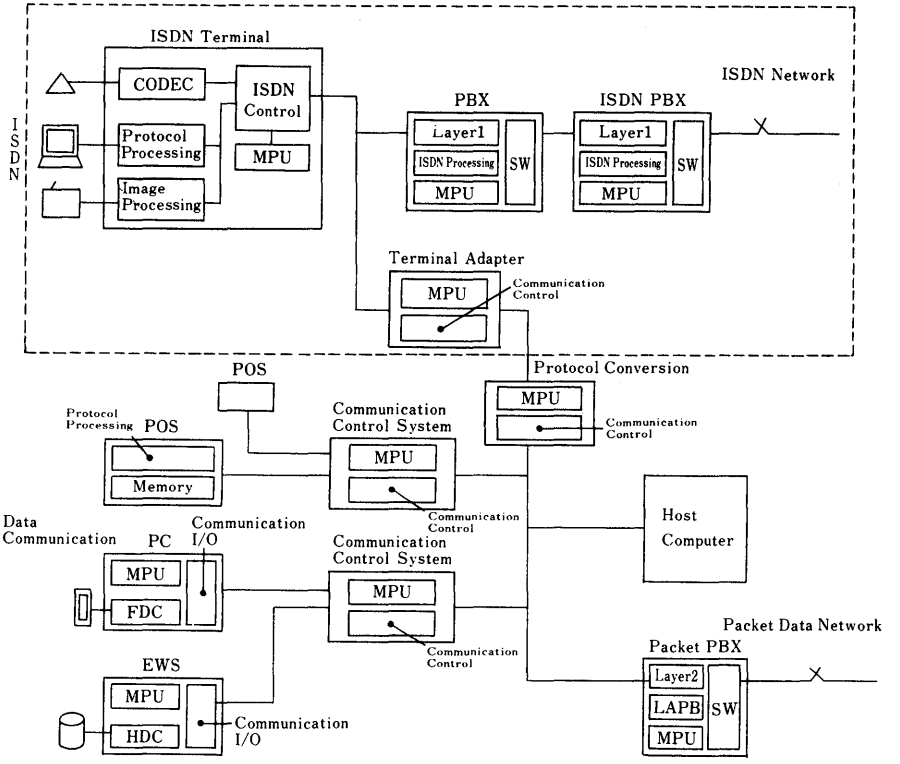


(2)-(B) Semiconductor line up

Function	Hitachi Products
CODEC	HD44230/240 Series HD44270 Series
Side tone adjustment	HD81019/20 Terminal CODEC
Speech network	Standard linear IC
Display	LCD driver HD44780
Microcomputer	General purpose microcomputer HD6301, HD64180 Microcomputer for telephones HMCS4608
Digital circuit interface	Gate Array

5. APPLICATION FOR DATA COMMUNICATION SYSTEM

(1) Application system



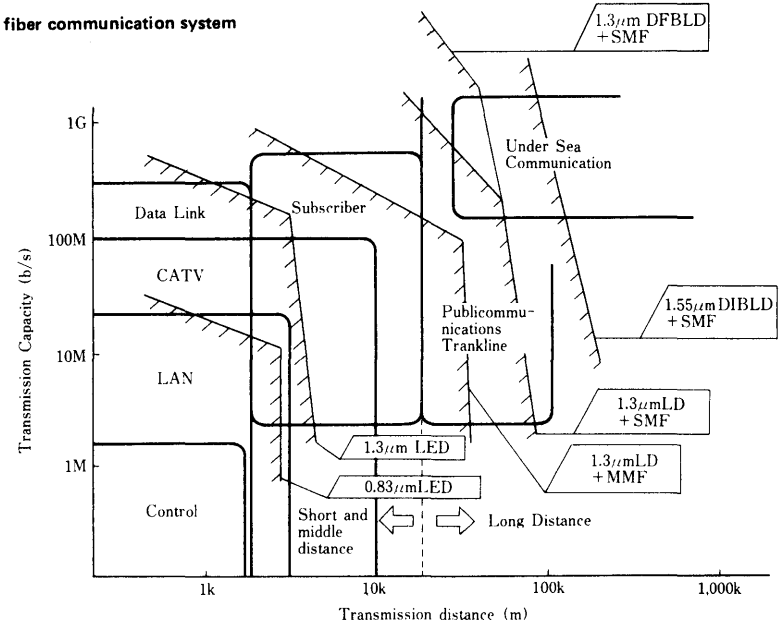
(2) Semiconductor lineup

	Application	Application Specific LSI	Standard LSI
ISDN	Digital Telephone	Call in for Information on ISDN Products	HD64180S
	G4 FAX		
	ISDN Terminal		
	ISDN PBX, PBX		
	Packet PBX		
Data Communication	Protocol Processing		HD64180S
	Communication Controller		HD64570
	Communication I/O		

* UNDER DEVELOPMENT

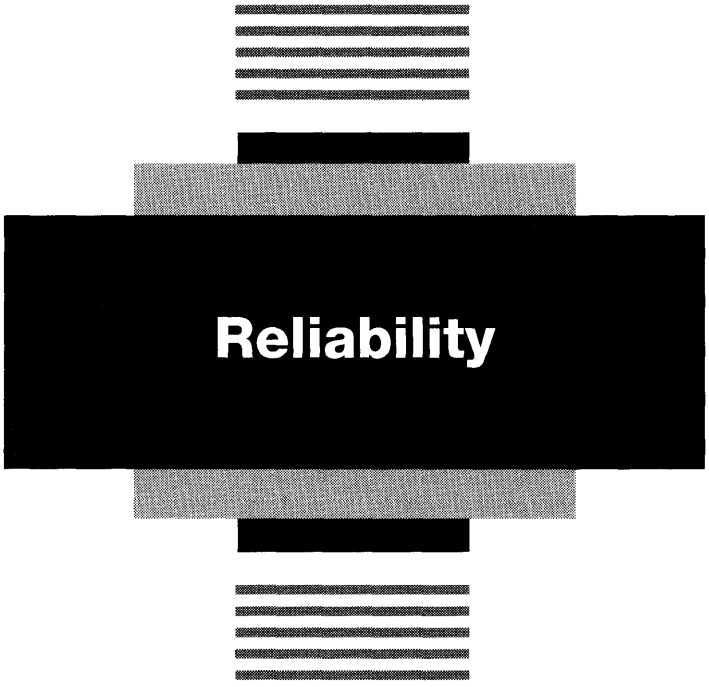
6. APPLICATION FOR OPTICAL FIBER COMMUNICATION SYSTEM

(1) Optical fiber communication system



(2) Hitach products line up

Transmission Rate (Mb/s)	Transmitter	Receiver
	Device Number	Device Number
32	HE8403TR/ HE8403R/ HE8403ML (0.84 μm IRED)	HR8102 (SI-PIN) HR8202TG (SI-APD)
140	HE1301TR/ HE1301ML (1.3 μm IRED) HE1301ML (1.3 μm IRED) HL1321DL (1.3 μm LD) HL1323TR/DM (1.3 μm LD)	HR1103TG/TR/CX (InGaAs-PIN) HR1104TG/CX (InGaAs-PIN) HR1105TG (InGaAs-PIN)
565	HL1321DL/BF (1.3 μm LD) HL1323TR/DM (1.3μm LD) HL1521A (1.55 μm LD)	HR1103TG/CX (In GaAs-PIN) HR1104TG/CX (In GaAs-PIN) HR1105TG (In GaAs-PIN) HR1201TG/CX
1500	HL1341A/AC/FG/BF/DL (1.3 μm DFB LD)	HR1201TG/CX (In GaAs-APD)
2400	HL1541A/AC/FG/BF/DL (1.55 μm DFBLD) HL1561A/AC (1.55 μm, 14 phase shifted DFB-LD)	HR1201TG/CX (In GaAs-APD)



Reliability

1. RELIABILITY

1.1 RELIABILITY CHARACTERISTICS FOR SEMICONDUCTOR DEVICES

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along proper emvironmental conditions. This section describes reliability characteristics, failure types and their mechanisms in terms of devices. First, semiconductor device characteristics are examined in light of their reliability.

(1) Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.

(2) Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

(3) Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.

(4) Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data thus cannot be used in some cases.

(5) Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.

(6) Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should be also reviewed when electrode and package materials are not suited for particular environmental conditions.

(7) Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

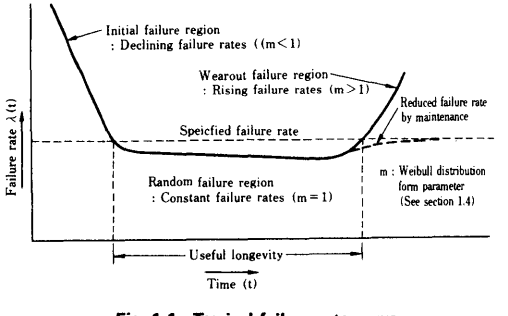


Fig. 1-1 Typical failure rate curve

Device reliability is generally represented by the failure rate. 'Failure' means that a device loses its function, including intermittent degradation as well as complete destruction. Failure criteria are defined in Chapter 3 Reliability Test. Under actual use, however, variations in failure detection sensitivity and operational margin should be considered.

Generally, the failure rate of electric components and equipment is represented by the bathtub curve shown in Fig. 1-1. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

1.2 FAILURE TYPES AND THEIR MECHANISMS

1.2.1 Failure physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering". It is used to examine the physical mechanism of failures in terms of atoms and molecules to improve device reliability. This physical approach was introduced to the reliability field with the demand for minimized development cost and period, as technology rapidly developed and system performance increased, requiring more complex and higher levels of reliability. These conditions derived from the development of solid state physics (semiconductor physics) after World War II and associated device development.

Failure physics have been employed to:

1) Detect failed devices as soon as possible
2) Establish models and equations used for failure prediction
3) Evaluate reliability for short periods by accelerated life tests

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage and usage by adding physics as a basic technology to conventional experimental and statistical approaches.

1.2.2 Failure types and their mechanisms

Device failures are physically discussed in this section. Semiconductor device failures are basically categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These failures and their causes are summarized in Table 1-1. Actual failures are shown in Photos 1-7 to 1-16. Typical failure mechanisms are reviewed next.

(1) Surface Deterioration

The pn junction has a charge density of $10^{14} - 10^{20}/cm^3$. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to a depletion layer, electrical characteristics of the junction tend to be easily varied. Although the surface of such devices as

planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model shown in section 3.3.

One example of recent failures is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS} by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 5 μm to 2 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have employed improved design and process techniques to prevent these problems. However, as processing becomes even finer, surface deterioration may possibly become a serious problem.

(2) Electrode-related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticable failures include electromigration and Al wiring corrosion in plastic sealed packages.

① Electromigration

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with current of about scattering electrons, an 'electron wind' is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

② Multi-metal line related failures

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

③ Al line corrosion and disconnection

When Plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Fig. 1-2). Under high-temperatures and high-humidity, corrosions are randomly generated over the element surface. However, after an extended period of time, the corrosions have not significantly increased. Accordingly, this failure is possibly due to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high-temperature, high-humidity condition, on the other hand, corrosions are generated in higher potential areas while in lower potential areas, grain corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Fig. 1-3.

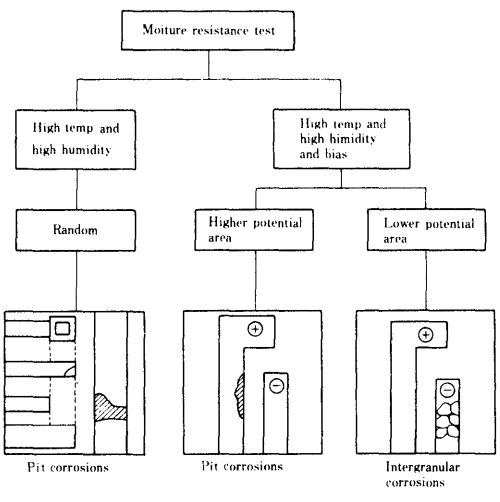


Fig. 1-2 Categorized Al corrosion mode

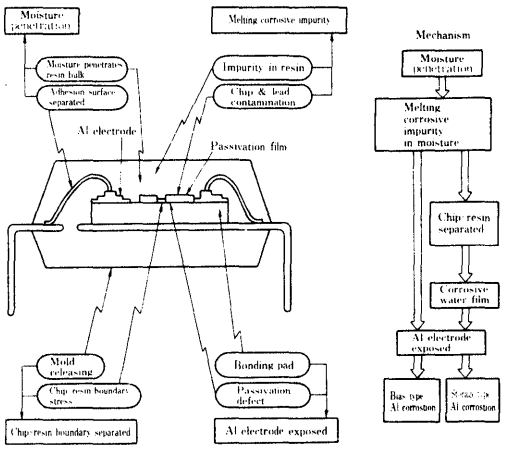


Fig. 1-3 Plastic package cross section and Al corrosion mechanism

(3) Bonding related failures

① Degradation caused by intermetallic formation

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

② Wire creep

Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding

under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

③ Chip crack

With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

④ Reduced maximum power dissipations

For power devices, heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance. This results in decreased maximum power dissipations.

(4) Sealing related failures

Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between the different ionized materials.
2. Intermittent moving foreign metals short
3. Al line corrosion due to extraneous H_2O caused by hermetic failure

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parastic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying.

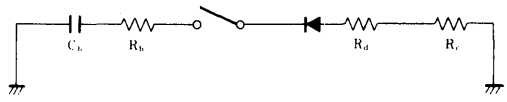
(5) Electrostatic discharge destruction

① Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure: the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Fig. 1-4. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged with 2000V, the dissipated energy is obtained by:

With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of



Cb – Human body capacity
Rb – Human body resistance
Rd – Device resistance
Rc – Resistance between device and ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} \text{ J}$$

Fig. 1-4 Equivalent circuit of human body model

this model is shown in Fig. 1-5. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction. 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high-frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

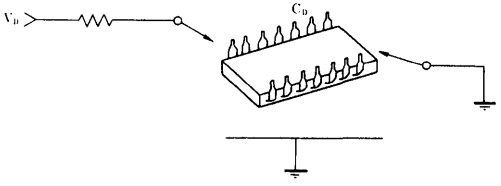


Fig. 1-5 Equivalent circuit of charging model

② Latch up

Latch up is a problem unique in CMOS devices. This problem is a thyristor phenomenon caused by a parastic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply and noise is applied, or when a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parastic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is off or the flowing current is forced to be reduced to a certain level. Once latch up occurs in an operating device, the device will be destroyed. Much effort should be made in designing circuits to prevent latch up. Latch up triggering input or output currents start to flow under the following conditions.

Vin > Vcc or Vin < GND for input level

Vout > Vcc or Vout < GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parastic diodes.

③ Soft errors

When α particles are generated from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating nodes, causing temporary soft errors. This pheno-

Table 1-1 Failure causes and mechanism

Failure related causes		Failure mechanisms	Failure modes	Example
Passivation	Surface oxide film, Insulating film between wires	Pin hole, Crack, Uneven thickness, Contamination, Surface inversion, Hot carrier injected	Withstanding voltage reduced, Short, Leak current increased, h_{FE} degraded, Threshold voltage variation, Noise	Fig. 1-7
Metallization	Interconnection, Contact, Through hole	Flaw, Void, Mechanical damage, Break due to uneven surface, Non-ohmic contact, Insufficient adhesion strength, Improper thickness, Electromigration, Corrosion	Open, Short, Resistance increased	Figs. 1-8, 1-16
Connection	Wire bonding, Ball bonding	Bonding runout, Compounds between metals, Bonding position mismatch, Bonding damaged	Open, Short Resistance increased	Fig. 1-9
Wire lead	Internal connection	Disconnection, Sagging, Short	Open, Short	Fig. 1-10
Diffusion, Junction	Junction diffusion, Isolation	Crystal defect, Crystallized impurity, Photo resist mismatching	Withstanding voltage reduced, Short	Fig. 1-11
Die bonding	Connection between die and package	Peeling chip, Crack	Open, Short, Unstable operation, Thermal resistance increased	Fig. 1-12
Package sheling	Packaging, Hermetic Seal, Lead plating, Hermetic package & plastic package, Filler gas	Integrity, moisture ingress, impurity gas, high temperature, surface contamination, lead rust, lead bend, break	Short, Leak current Increased, Open, Corrosion disconnection, Soldering failure	Fig. 1-13
Foreign matter	Foreign matter in package	Dirt, Conducting foreign matter, Organic carbide	Short, Leak current increased	Fig. 1-14
Input/output pin	Electrostatistics, Excessive Voltage, Surge	Electron destroyed	Short, Open, Fusing	Fig. 1-15
Disturbance	α particle	Electron hole generated	Soft error	
	High electric field	Surface inversion	Leak current increased	

menon is shown in Fig. 1-6. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases organic material, PIQ, is applied to the surface of the device.

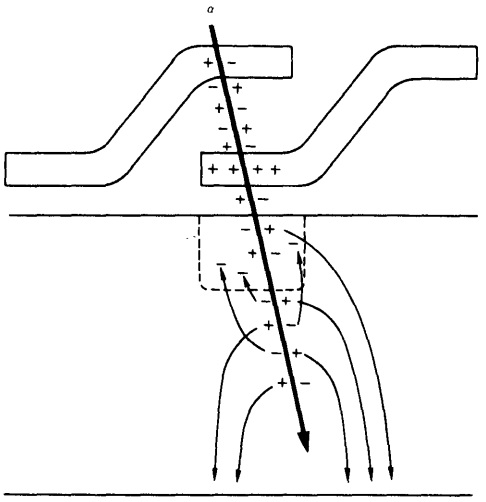


Fig. 1-6 Soft error caused by α particles in dynamic memory

(6) Fine geometry related problems

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 5 μm → 3 μm → 2 μm → 1.3 μm. However power supply has not been scaled down used for 5V, only line dimensions has been fined increasingly. Problems associated with finer geometry are shown in Table 1-2.

Table 1-2 Finer geometry related problems

Item	Problems	Countremasure
5V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering ◦ Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved ◦ Process improved
Vertical & horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

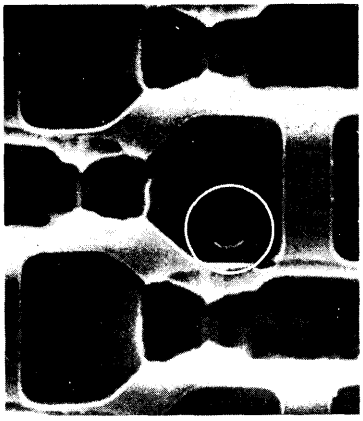


Fig. 1-7 Pin hole

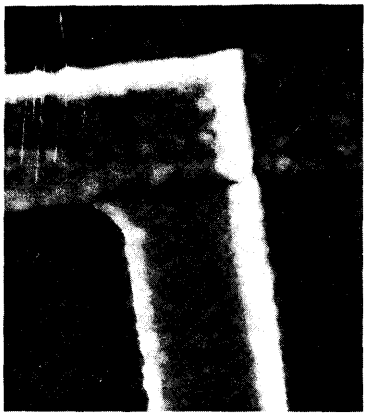


Fig. 1-8 Metallization break due to uneven surface

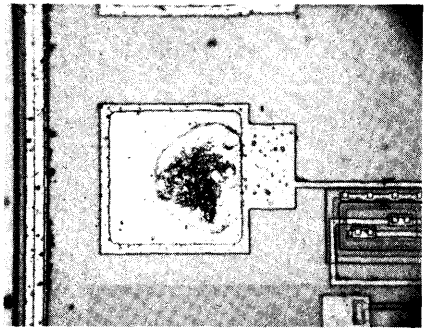


Fig. 1-9 Defect caused by bonding

Fig. 1-10 Bonding wire destruction by ultrasonic fatigue

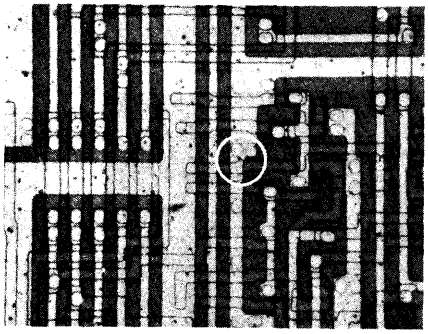


Fig. 1-11 Diffusion photo resist failure

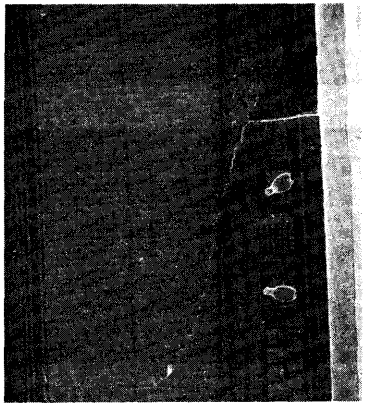


Fig. 1-12 Chip crack

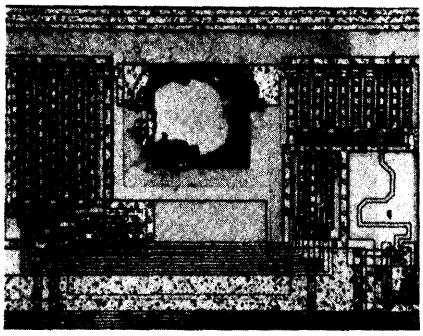


Fig. 1-13 Disconnection caused by bonding pad corrosion

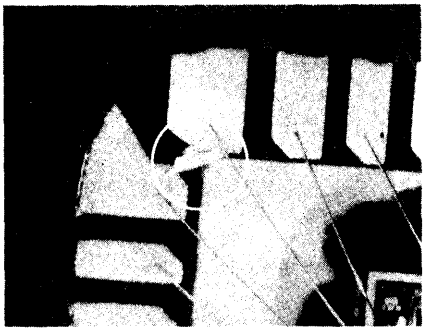


Fig. 1-14 Short caused by conducting foreign matter in a package

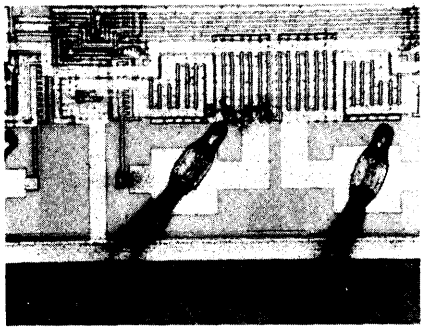
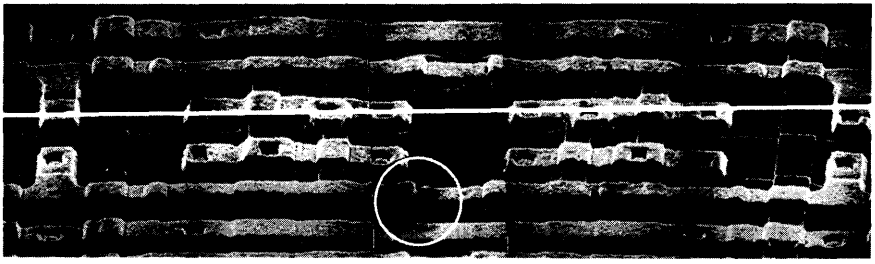
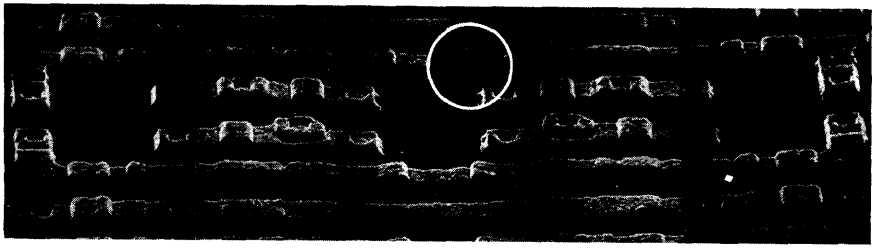


Fig. 1-15 Output pin destruction (open failure)



SEM photo of failure



The above part taken in opposite direction

Fig. 1-16 Al film break due to uneven surface

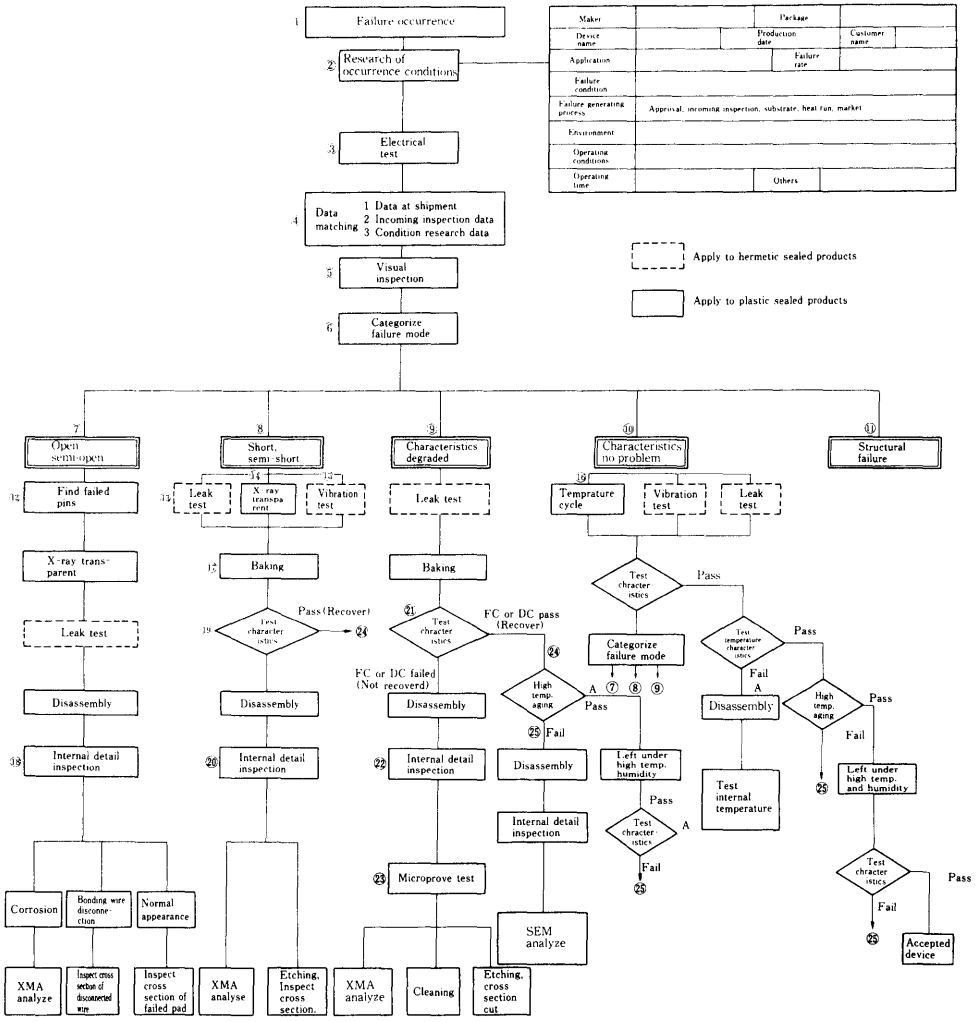


Fig. 1-17 Failure analysis flow

1.3 FAILURE ANALYSIS

Failures can occur during reliability testing or processing by users, or in the field. Analyzing the failures not only provides data on failure modes and failure mechanisms, but also contributes to device reliability improvement. Failure analysis should be carefully performed in a proper way. Please note the following failure analysis:

① Failure devices must be so analyzed as not to apply mechanical, electrical or thermal shocks. These shocks may alter the failure conditions.

② Equipment used for analysis should be suited for the purpose.

③ Proper failure analysis requires good knowledge of device design and manufacturing techniques.

④ Data concering stress applied under tests and use and failure histories are valuable for proper failure analysis.

⑤ Failure analysis results should be systematically recorded and accumulated.

A failure analysis procedure performed by semiconductor manufacturers is flowcharted in Fig. 1-17. Details of the procedure may vary depending on the failure mode and failure degree. Main equipment used for failure analysis are shown in Table 1-3.

Table 1-3 Equipment for failure analysis

For observation	Stereomicroscope Metal microscope Ultrasonic microscope Scanner electron microscope (SEM) Transparent electron microscope (TEM) Infrared microscope Scanner laser microscope X-ray transparent equipment Camera Scanner surface temperature measurement Others
For electrical characteristics measurement	Diode curve tracer Transistor curve tracer IC curve tracer Transistor tester IC tester LSI tester Function tester Oscilloscope Pulse generator DC power supply Ammeter, microammeter Voltmeter Noise measurement Small ohm-meter Insulating ohm-meter LCR meter Manipulator Others
For spectrum analyzing	Electron microscope X-ray microanalyzer (XMA) Fluorescence X-ray analyzer Auger electron spectral analyzer Auger electron microanalyzer
For analyzing	Ion microanalyzer (IMA) Laser microanalyzer Electron beam analyzer X-ray analyzer Infrared absorption spectral analyzer Emission spectral analyzer Atomic absorption photometer PH meter Electron spectral analyzer (ESCA) Nuclear magnetic resonance analyzer (NMR) He leak tester Bubble leak tester Ion chromatography Gas chromatography Mass spectrographer Differential thermal analyzer Others
For generating samples used for analyzing	Cutter Grinder Sander Epoxy mould Evaporation equipment Draft (foul solution, exhaust gas) Etchants Plastic decomposition Others
For various tests	PIND tester Thermostatic chamber Burn-in equipment Humidity generator Temperature cycling chamber Tension tester Others
Others	Chemical balance, Projector, Measuring micrometer, Micrometer, Caliper, Tarry step

Table 1-4 Screenings

Screening		Failure effective to screening	Effectivity	Remarks
Visual before sealing		Lead plating, wire bond metallization, contaminants, oxide film, corrosion, foreign material, substrate, die bond	Extremely effective	• Essential for highly reliable devices. • Cost depends on visual inspection.
Infrared-ray		Thermal resistance design	Very effective	• Used for design evaluation only.
X-ray		Die bond, sealing, lead, plating, package, foreign material, contaminants	Extremely effective for die bond, Effective for others	• Visual inspection after sealing. • X-ray can peneterate Al, Si, etc. • Cost is six times higher than visual before sealing.
High temp. storage		Electrical stability, Si (bulk), metallization, corrosion	Effective	• Highly recommended screening.
Thermal cycle		Package, wire bond, sealing, chip crack, die bond, thermally mismatching	Effective	• Effective for Al lead devices.
Thermal shock			Effective	• The same as for thermal cycling except for slightly larger stress level.
Constant acceleration		Lead plating, wire bond, die bond, chip crack	Effective	
Drop	No monitor	Wire bond, chip crack, die bond	Effective	• Inferior to constant acceleration screening.
	With monitor	Foreign materials, semi-short, semidisconnection	Inferior Slightly effective Slightly effective	• For foreign materials, inferior to visual and X-ray screenings.
Vibration fatigue		Lead plating, wire bond, package, substrate crack, die bond	Inferior	• Destruction possibility exists.
Variable frequency vibration	No monitor	Package, wire bond, die bond, substrate	Slightly effective	
	With monitor	Foreign materials, lead plating, semi-disconnection	Slightly effective Effective Effective	
Random vibration	No monitor	Package, wire bond, die bond, substrate	Effective	• More effective for space equipment than variable frequency vibration without monitor
	With monitor	Foreign materials, lead plating, semi-disconnection	Slightly effective	• Not recommended due to its high cost except for special cases.
He leak test		Package, sealing	Slightly effective	• Detect leak $10^{-6} \sim 10^{-10}$ atm cc/sec.
Radio isotope leak test		Package, sealing	Slightly effective	• Detect leak $10^{-8} \sim 10^{-12}$ atm cc/sec.
Phloro carbon leak test		Package, sealing	Slightly effective	• Detect leak 10^{-3} atm cc/sec on more.
Glycerol leak test		Package, sealing	Slightly effective	• Possibility of reliability deterioration.
High voltage test		Oxide film	Effective	
Insulating resistor		Lead plating, contaminants, metallization	Slightly effective	

(to be continued)

Screening	Failure effective to screening	Effectivity	Remarks
AC	Metallization, design, Si (bulk), parameter variation, oxide film, contaminants, inversion channel	Very effective	
DC	Metallization	Effective	
High temp. AC	AC operation	Extremely effective	• Temperature accelerates failures. • Most effective screening though most expensive.
High temp. inverse bias	Inversion channel	Effective	
Visual after sealing	Package crack, package sealing	Effective	
Power sequence	Parastic PNPN	Effective	Required for latch-up sensitive devices.

Table 1-5 Activation energy of deterioration in semiconductor devices

Area	Deterioration mechanism	Deterioration	Activation energy
Seal glass	Insulating resistance deteriorated (Pb^+ ion drift)	Conductivity	1.05 to 1.17 eV
Wire bonding	Au-Al alloy	Bonding tension strength	0.11
		Contact resistance	0.57, 1.04, 1.08
		Au-Al alloy film growth	0.69
Die bonding	Connection strength deteriorated	Au diffusion coefficient in Si	1.1
Contact	Contact disconnection (Si diffusion in Al)	Burn-out life (Pure Al)	0.55
		Burn-out life (Al containing Si)	0.31
		Contact resistance	0.89 (Tj > 210°C)
		Al diffusion in Si (Al bulk)	0.79
		Al diffusion in Si (1.8 Si-Al)	0.9
Metallization	Al electromigration	Burn-out life (small particle)	0.48
		Burn-out life (large particle)	0.84
		Burn-out life (SiO_2 coating)	1.2
		Al self-diffusion coeffecient	1.48
	Al moisture corrosion	Al surface film generation	1.17 (T > 60°C)
Resin	Al corrosion	Water diffusion coeffecient in resin	Approx. 0.4
Passivation	Surface resistance reduced	Conductivity (PSG)	0.8 0.5 (after moisture absorption)
		Conductivity (CVD SiO_2)	0.6
	Charge moving in PSG (Na^+ ion drift)	Na diffusion coefficient ([P] 4 mol %)	1.38
Field SiO_2	Surface resistance reduced (Adsorbed water film leak)	Surface conductivity	0.35 (> 80% RH) 0.65 (> 40% RH)
	Surface charge leak	Vth variation	1.0
	SiO_2 film alkaline moving	Na^+ diffusion constant	1.1 to 1.4
		Li^+ diffusion constant	1.0
		H^+ diffusion constant	0.31, 0.44
	SiO_2 NAPOX surface boundary resistance reduced	Surface boundary leak current	0.43 to 0.70
	SiO_2 film trap charge acquisition	Vth variation	1.3
	Hot electron SiO_2	Vth variation	1.06 0.97~2.0 (Actual device)
	Hot electron SiO_2		1.0

Table 1-6 Typical acceleration life tests

Stress applied	Characteristics	Example of tests	Acceleration factors	Failure modes
Constant stress	Inspects how stress affects devices	High & low temp storage	Temp	Surface deteriorated
		Operational lifetime	Junction temp, voltage	Surface deteriorated
		High temp & humidity storage	Temp, humidity	Corrosion, breakdown voltage reduced
		High temp & humidity bias	Temp, humidity, voltage	Corrosion, bridge between pins
Cyclic stress	Inspects how cyclic stress affect devices	Temp cycling (thermal shock)	Temp difference, duty	Disconnection, shorted
		Power cycling	Temp difference, duty	Disconnection thermal resistance reduced
		Humidity & Temp cycling	Temp difference, duty, humidity difference	Disconnection, shorts, corrosion
Step stress	Inspects limits of devices to stress	Operational lifetime	Junction temp, voltage	Element deteriorated
		High temp inverse bias	Junction temp, voltage	Element deteriorated
		Surge destruction	Electricity, voltage	Electrostatic destruction, element deteriorated
		Soldering resistance	Temp, time	Chip crack, element deteriorated

2. QUALITY ASSURANCE

2.1 RELIABILITY DESIGN AND PROCESS FEATURES OF HITACHI SEMICONDUCTOR DEVICES

The technology for designing and processing individual semiconductor devices, ICs, and LSIs is remarkably progressing towards more refined processing and higher reliability. Beginning overall with the setting of target specifications for reliability design of circuits and devices, higher integration and higher reliability can be accomplished by upgrading processing technology such as crystal processing, epitaxial growth, impurity diffusion, ion implantation, photo-etching surface stabilization, terminal forming, bonding, and sealing, as well as manufacturing process control technology, inspection, reliability evaluation, failure analysis, and so on.

The following describes reliability design and process features of Hitachi semiconductor devices.

2.1.1 Surface stabilization technology

There are mainly two reasons for surface degradation, one of the primary failure modes of semiconductor devices, according to the degradation parameter and mechanism.

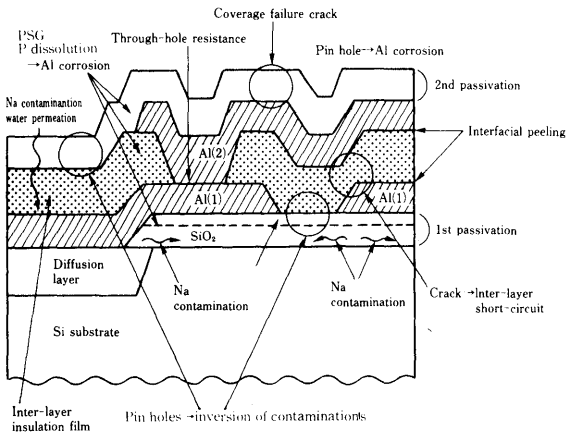


Fig. 2-1 Cross-section of surface protective films and the problems

One is due to the conductivity on the Si-SiO_2 surface layer such as backward pressure degradation at PN junction, threshold voltage (V_{TH}), a change on standing of mutual conductance, and the other is due to carrier reconnection on surface such as current amplification degradation and low-frequency noise degradation.

The following four factors are considered to cause surface degradation. (See Figure 2-1)

(1) Penetration of mobile ions (Na^+ etc.) into the first passivation film from manufacturing process and/or sealing material

(2) Surface charge (Qss) on surface level of the Si-SiO_2 surface layer

(3) Pin hole: failure of passivation film

(4) Leak charge onto the second passivation film from electrical fields

With the advances in device integration and performance, even a slight contamination of mobile ions can be a serious problem, and even a extremely partial contamination from passivation defects and the like can cause a fatal failure.

Therefore, to stabilize the Si surface, it is necessary to improve the "getter" effect for mobile ions in the first passivation film, to ensure surface stability by clean processes, to produce defect free films, and to have enough threshold voltage (V_{TH}) to resist leak charge. Additionally, to enhance the reliability of plastic sealing components (moisture resistance), the second passivation performs a significant role. The following features are required.

(1) Penetration prevention of external water molecules or contamination, and contaminated ions from the resin material itself

(2) Passivation film to resist thermal stress of the resin material

(3) Small defect density

From this point of view, Hitachi has enhanced reliability by developing and adopting first and second passivations, and a layer insulation film for various types of semiconductor devices. This section introduces a part of their development and adoption.

(1) Improve the second passivation to prevent external contamination, and to enhance moisture resistance

(2) Clean and defect free processes;

Cleanliness and defect free processes are particularly important for the first passivation. Hitachi is trying to achieve defect free processes by purifying process materials such as photoresist, cleaner, and evaporation Al, by cleaning oxidation furnace quartz pipes, by upgrading photomasks, by improving wafer handling methods, and by eliminating process dust. (See Figure 2-2)

(3) Leak charge countermeasure;

Threshold voltage (V_{TH}) can be made larger by forming a channel stopper layer using ion implantation technology, and by thickening passivation films.

(4) Process control;

For process control concerned with mobile ions, control of the implantation amount using specific MOS component, or automatic measurement of film thickness using optical methods at polysilicon film generation, is carried out as well as the BT (Bias-Temperature) method.

Moreover, Hitachi has developed technology for refined, higher-density, and multilayer line, and has adopted this technology to various semiconductor devices. The following describes some of them.

(1) Anisotropic dry etching using special gas is adopted (Figure 2-3), since conventional wet etching using chemicals cannot ensure enough dimension precision for refined processes.

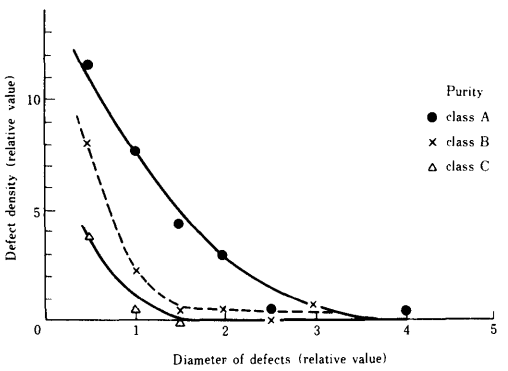


Fig. 2-2 Relationship between defect density in passivation films and the purity

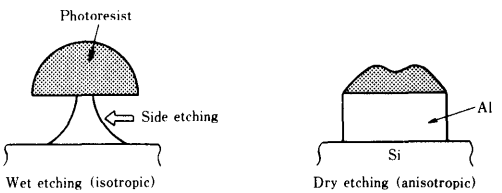


Fig. 2-3 Cross sections of devices during wiring process using the etching methods

(2) In the case of multilayer line, flow glass is applied or an etching method by sputtering is utilized.

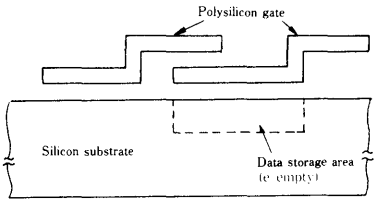
2.1.2 Soft error

(1) Soft error mechanism

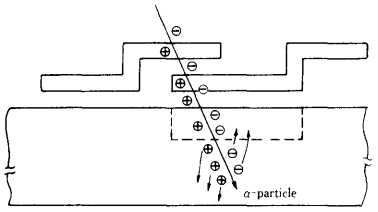
More and more refined IC memories are now being manufactured. This refinement implies a reduction in signal levels and accumulated charge in dynamic memories, as well as reduction of chip dimensions. The soft error problem interferes with this refinement. A "soft error" is a temporary failure which can be corrected by rewriting data into memory. The cause of it is α particle emitted by uranium and thorium (U, Th) which are slightly present in packaging material. A memory datum can be reversed when a memory chip is exposed to this α particle and subsequently many electron holes are generated on the Si substrate.

Figure 2-4 illustrates how an NMOS dynamic memory datum can be reversed by one of this α particle. In NMOS dynamic memory, only the electron cloud reverses information in a memory cell (data "1" → "0"), and the hole cloud is drawn by electric potential since a negative charge is formed onto the Si substrate. The failure mode shown in Figure 2-4 is defined as "memory cell mode" of a soft error and is distinguished from "bit line mode" to be described next.

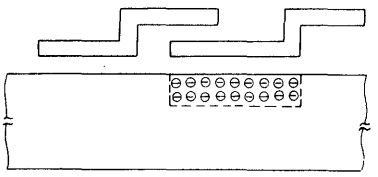
Figure 2-5 illustrates "bit line mode" of a soft error. When



a) A state in which memory data is "1"
(1-Transistor memory cell)

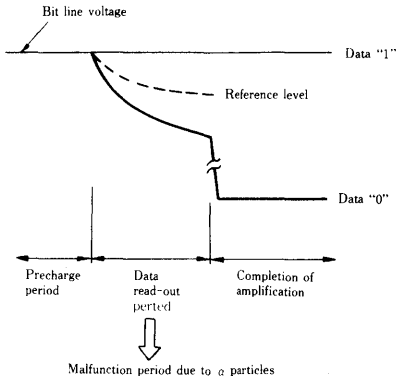


b) Entering α particle generates high volumes of electron-hole pairs.
The generated electrons go into the data storage area, and the holes are drawn to the substrate power supply.

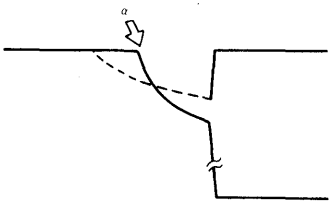


c) Reverse from memory data "1" to "0"

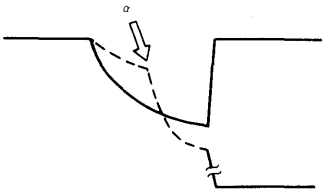
Fig. 2-4 Malfunction at the memory cell



a) Memory data read to the bit line



b) Malfunction due to data change from "1" to "0"



c) Malfunction due to data change from "0" to "1" (reference level is reduced)

Fig. 2-5 Malfunction on the bit line

the information stored in a memory cell is placed on the bit line, the electric potential of the bit line is altered due to this bit of information.

This charge is very small (hundreds mV), and the electric, potential is amplified by a sense amplifier, compared with the basic electric potential (electric potential read from dummy cell).

Datum reverse from "1" to "0" occurs if the bit line electric potential is below the basic electric potential due to the emission of α particle during the short period from data reading to amplification. The datum reverse from "0" to "1", on the other hand, occurs if the basic electric potential is lowered.

These are designated as "bit line mode", since errors occur through the emission of α particle onto the bit line in both cases. Figure 2-6 shows the relation between soft error occurrence ratio and cycle time.

Actual products are characterized by either cell mode or bit line mode soft errors, or their mixed mode.

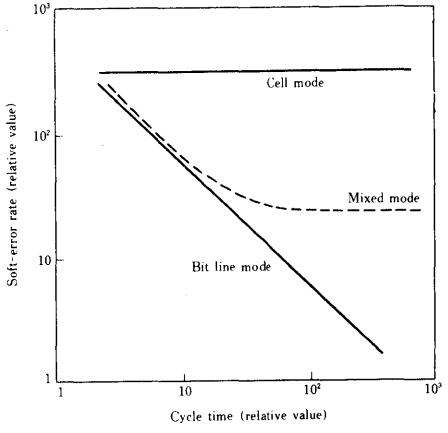


Fig. 2-6 The cycle-time dependency of soft error rate

(2) Countermeasures against soft errors

The error rate of 64 k DRAM is expected to exceed the target specification value according to forced irradiation test results. Consequently, the following countermeasures have been taken to reduce soft errors.

(a) Utilize package material emitting less α particle

(b) Utilize chip coating technology to prevent α particle peneteration

(c) Utilize circuit design and layout technology to withstand α particle penetration

Due to these countermeasures, soft errors in 64 k DRAM are not a problem any longer in practical use. Figure 2-7 shows an example of soft error reduction in 64 k DRAM. For masks 1 and 2, chip coating technology has been used to reduce soft errors. With the advance of layout technology (c), chip coating is not necessary for masks 3 and 4. The improved technology for 64 k DRAMs is also utilized for 256 k DRAMs to solve the soft error problem.

(3) Suggested countermeasures for system devices

As described so far, Hitachi has been taking various countermeasures against soft error to a satisfactory degree. The reliability of a system will be much more enhanced if the ECC function is added for large memory systems, and the parity bit for small systems.

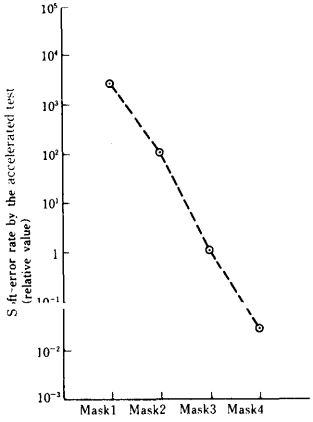


Fig. 2-7 Improvement in soft error rate of a 64K DRAM

2.1.3 Multilayer line technology using the resin insulation method

As one of the multilayer line technologies to raise the density of monolithic LSIs, Hitachi has developed a resin insulation method using polymeric resin for insulating material between line layers, and has been mass-producing LSIs for more than 10 years using this technology.

The process and materials used by this resin insulation method, particularly Polyimide Isoindro Quinazolinedione (PIQ), are originally Hitachi's technology.

Currently, LSIs with 3-layered line have been partially developed, but most LSIs still have 1- or 2-layered line. This structure, as shown in Figure 2-8, is configured by the repetition of 1-layered line processing. Using this method, the steps in the insulator layer and conductor layer are formed on top of each other, and these layers become thinner at either side of the steps. Consequently, short

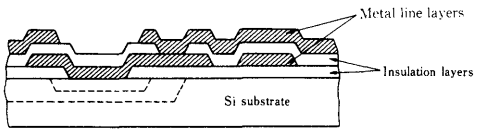


Fig. 2-8 A cross-section of the conventional 2-layer line structure

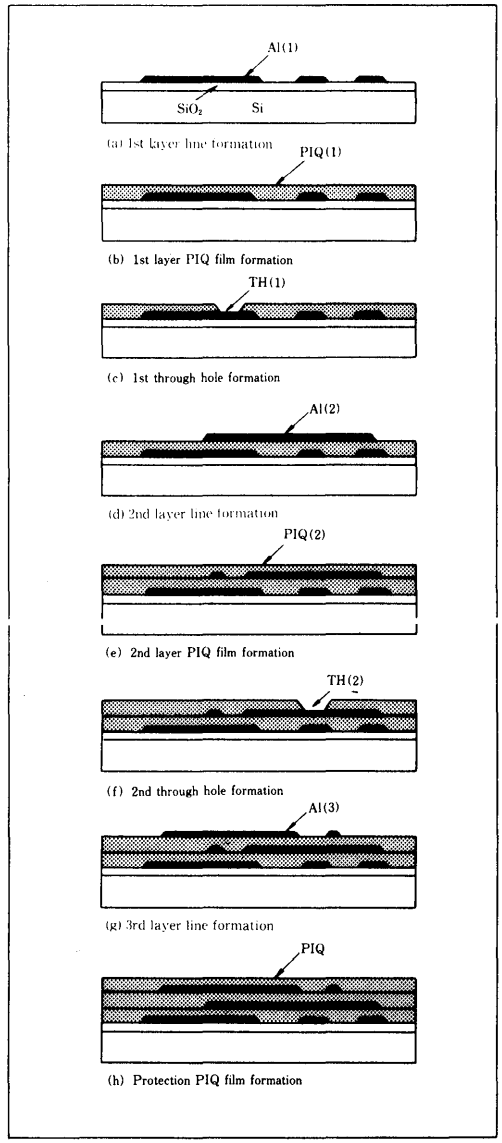


Fig. 2-9 PIQ layer process

circuits and disconnections in the conductor layer can easily occur at these points. Considering yield and reliability, up to 3-layered line can be allowed.

Accordingly, Hitachi, for the coming higher-integrated LSIs, has been trying to overcome failures in metal structure, and to develop new line technology to easily provide from 2- to 5-layered line. From among many trails for new metal line technology, Hitachi has developed a planar-type 2-layered line method, where thermosetting polymer resin is used for insulation film, and has mass produced LSIs using this method.

Additionally, for future VLSI devices, Hitachi has been developing ultra-fine processing and 3-layered line processing (Figure 2-9).

Scanning Electron Microscopy (SEM) photographs of the cross-section and surface of the 3-layered line structure are shown in Figures 2-10 and 2-11, respectively. These pictures show that the coverage of insulation film and metal line at the steps is extremely good and that there is no possibility of disconnection at these points.

Although the through hole is configured by ultra-fine processing, the taper is etched at an angle of 60° providing roundness. Disconnection, therefore, cannot occur since the coverage of Al line is satisfactory at this point.

Table 2-1 shows reliability test results of resin-sealed multilayer line LSIs using PIQ. The test results are satisfactory because of the stability of the component and corrosion protection effect for metal line, and the stability and higher reliability of the line structure itself.

The following describes the main features of PIQ.

(1) Good heat resistance: up to 450°C for 3 to 4 hrs.
(2) Good metal line coverage due to good flatness in multilayer line structure,
(3) Thick film formation on Si wafer: no cracks even at a film thickness of 10μ
(4) No cracks due to temperature change: no cracks from −196°C to +150°C of thermal shock.
(5) Good processability: processing by photoresist

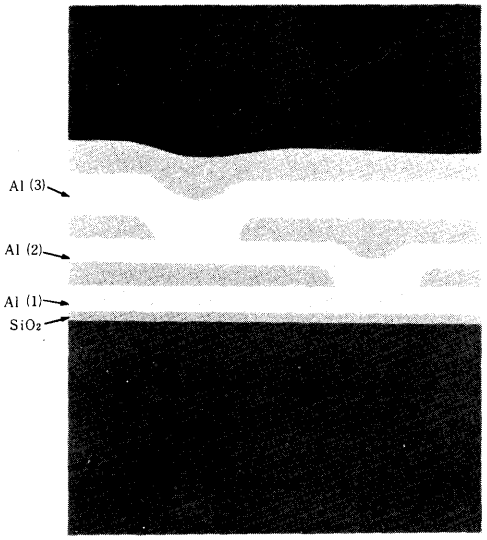


Fig. 2-10 A cross-section of three-layer lines

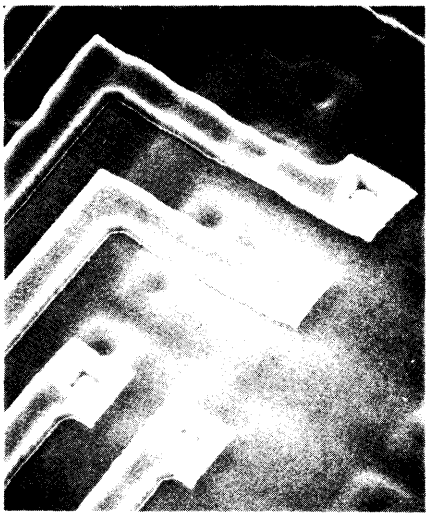


Fig. 2-11 The surface of a three-layer line LSI (by SEM)

2.1.4 Various types of breakdown protection circuits

Semiconductor devices may be damaged due to excessive stress caused by electrostatic discharge, surge, etc. Examples of improved circuits by installing protection circuits for electrostatic discharge, surge, and excessive load are described in the following.

2.1.4.1 Electrostatic breakdown protection circuit

Device breakdown by electrostatic discharge can generally be prevented by using the devices under moderate conditions following prescribed precautions. This is because a protection circuit is provided to strengthen the resistance against electrostatic breakdown as long as the performance of LSIs (operating speed, oscillation frequency, etc.) is not sacrificed. Figure 2-12 shows examples of electrostatic breakdown protection circuits; P-channel MOS IC (a), and bipolar IC (b). Each figure shows the equivalent circuit and cross-section. In the cross-section, the leak path of impressed electrostatic pulse is indicated by an arrow. Each protection circuit protects internal components from electrostatic damage by leaking static electricity to the IC board (GND) or power supply (Vcc) and by clamping the excessive input voltage at a constant voltage. Figure 2-13 shows electrostatic breakdown strength of typical Hitachi semiconductor devices.

Testing is carried out by the condenser discharge method, where a 200 pF condenser is used considering the capacitance of the human body. Generally, more than 200 V of breakdown strength is guaranteed except for ECL and the like, which require high-speed operation. Such types of LSIs cannot employ prevention circuit effectively.

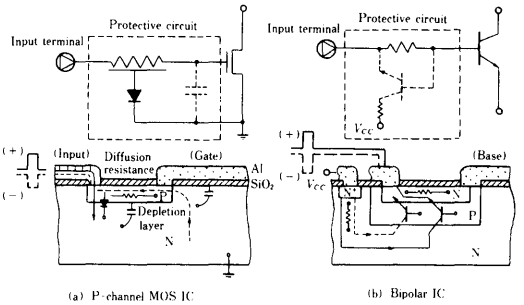


Fig. 2-12 Examples of protective circuits against electrostatic breakdown (Upper; Equivalent circuit, Lower; Cross-section)

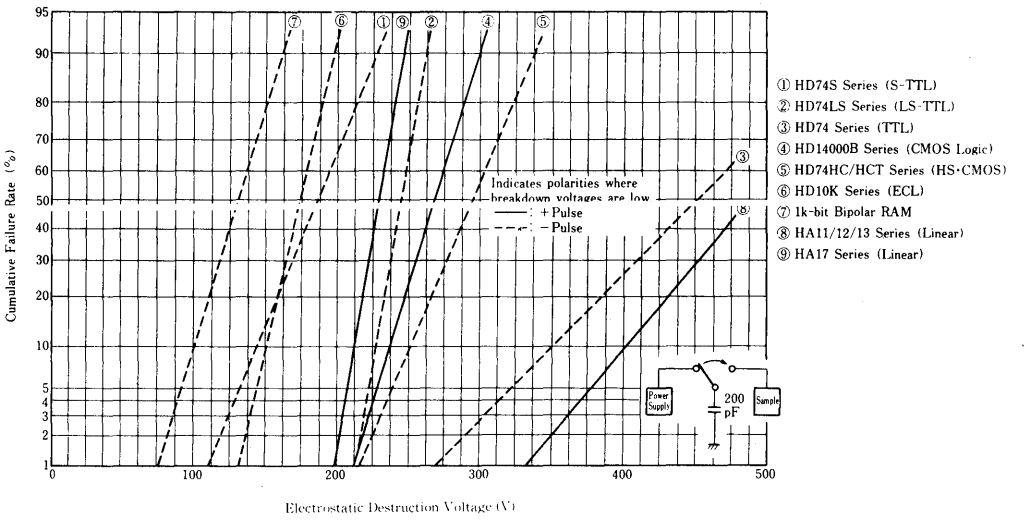


Fig. 2-13 An example of electrostatic breakdown voltages of ICs (1)

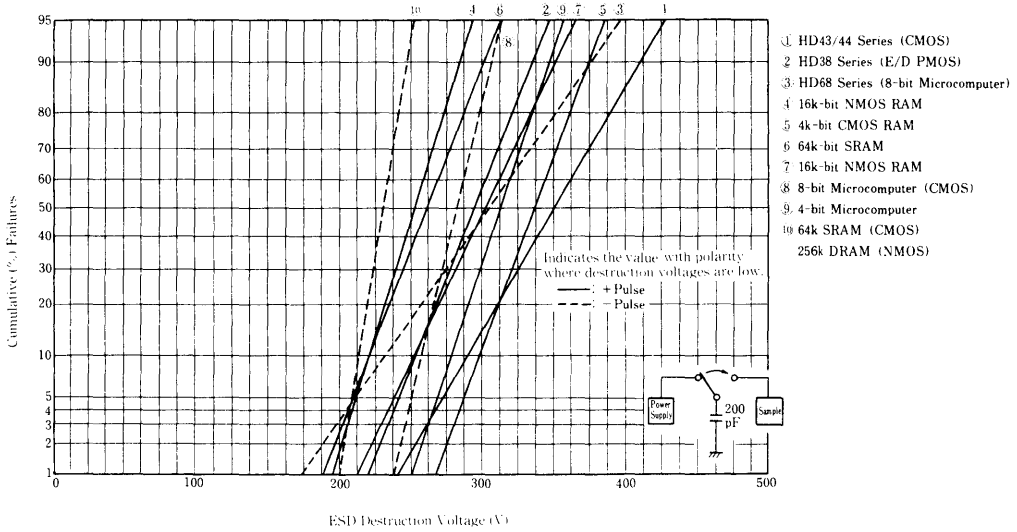


Fig. 2-13 An example of electrostatic breakdown voltage of ICs (2)

2.1.4.2 Protection circuit for power IC

Power ICs for output amplification, which are mainly mounted ICs, incorporate a thermal shutdown circuit and surge protection circuit. If junction temperature reaches about 150°C, the thermal shutdown circuit begins operation. The thermal shutdown circuit protects ICs from damage by automatically controlling output, restraining heat, and keeping junction temperature below 150°C, in spite of a continuous short circuit load. Another problem is the destruction of mounted devices caused by overlapped surge onto the Vcc line. The surge protection circuit is provided to solve this problem. ICs are protected from surge destruction by inverse voltage of transistors and stopping amplifier operation, when surge voltage is applied to the power supply pin of the power IC. For example, the HA13108 has been improved so as not to be destroyed if 0.2 sec surge voltage is applied to the power supply pin at 50 V of peak voltage. Currently, new ICs containing ASO protection circuit are being developed. Hitachi is trying to enhance reliability by increasing the destruction margin.

2.1.5 Assembly technology

The assembly process refers mainly to the die bonding process to attach a chip onto a package, and the wire bonding process to connect terminals of a chip to leads. The reliability is greatly affected depending on the level of assembly technology. The following describes the main failure modes which are likely to occur during the assembly process.

(1) Bonding open, intermittent, short circuits
(2) Chip cracks
(3) Resistance increase and open due to Au-Al compound
(4) Bonding wire open due to repetitive thermal stress

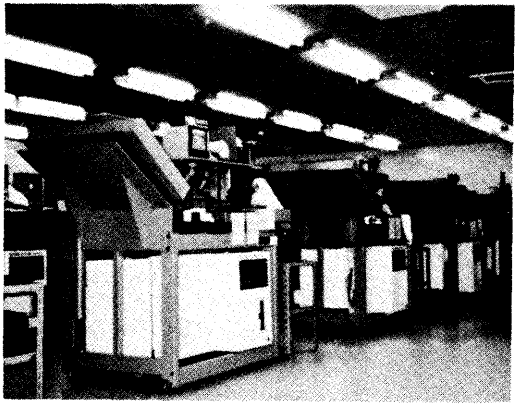


Fig. 2-14 Computerized automatic fabrication

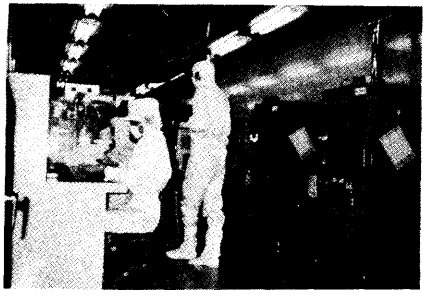


Fig. 2-15 Clean fabrication process

(5) Thermal resistance increase and chip peeling in soft solder type die bonding process

Hitachi is trying to enhance reliability by using appropriate designing and manufacturing technology to overcome these failures.

(1) Wafer dicing

Employing the diamond scribing method which has been widely used so far, cracks and chips on the pellet may occur. These failures are decreased by using the wafer dicing method where a wafer is diced by rapidly revolving a thin blade consisting of diamond powder congealed by a special metal.

(2) Automatic pellet bonding

There are several types of pellet bonding methods according to device characteristics.

(a) Au-Si eutectic alloying method

(b) Conductive adhesive method

(c) Soldering method

(d) Glass method, etc.

For each method, Hitachi adopts and automatic pellet bonding system on the mass-production line to upgrade quality and reliability of devices.

(3) Automatic wire bonding

Hitachi has developed and adopted an thermocompression automatic wire bonding system which can be controlled by computer (Figure 2-14). For quality control during processing, microwiring within a die is controlled by using SEM in addition to the usual visual inspection prior to sealing to upgrade device quality. Also, reliability is enhanced by keeping the assembly process clean (Figure 2-15).

2.1.6 Sealing technology

2.1.6.1 Plastic sealing technology

There are two types of sealing methods for semiconductor devices; one is an airtight sealing method using metal, ceramic or low fusion-point glass, and the other is a plastic sealing method using plastic material. As for airtight sealing, there is no peculiar problems concerning both material and technology. Airtightness is guaranteed through large and small leak tests. On the other hand, the plastic sealing method introduced to lower cost has enlarged the application field of semiconductor devices. Currently, devices completed by plastic sealing are very common among semiconductor products. This section describes reliability features of plastic-sealed devices.

There are mainly two types of failure modes for plastic-sealed devices; one is disconnection of electrode line due to aluminum line corrosion, and the other is wire bonding disconnection.

The former is caused by water molecules penetrating the boundary between plastic and lead frame or through the plastic material itself. These water molecules corrode electrode line and finally causes disconnection depending on impurity ions, voltage between electrode lines, and temperature.

The latter mode is caused by internal stress due to temperature change. Since the coefficient of thermal expansion and elastic modulus differs depending on component materials (Si chip, bonding wire, lead frame, plastic), the bonding wire, which is the weakest point, can be disconnected due to excessive internal stress caused by temperature change.

In addition to these failure modes, influence on electrical characteristics of other device types has been taken into

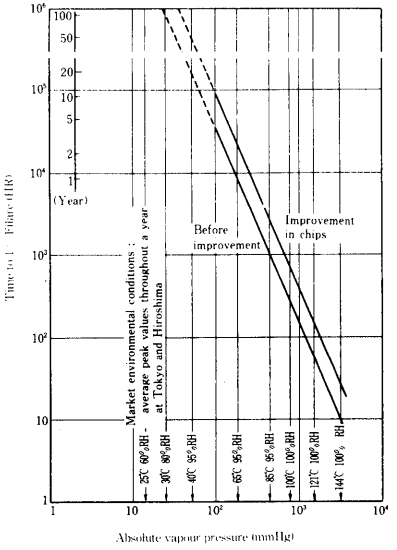


Fig. 2-16 Humidity dependency of a PIQ 2-layer metal line product and improvement

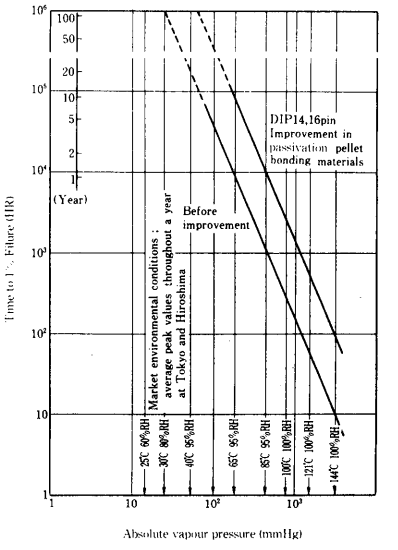


Fig. 2-17 Humidity dependency of a PIQ 1-layer line product and improvement

consideration. Considering all of these, Hitachi has systematically improved plastic material, molding technology, structure design, surface stabilization film of pellet bonding material, etc.

Figures 2-16 and 2-17 show improved moisture resistance of plastic-sealed ICs, taking PIQ 2-layered line products and 1-layered line products as examples.

2.1.6.2 Flameproofing of plastic-sealed devices

Resulting from the occurrence of TV fires, a UL (Underwriter's Lab. Inc.) standard has been established for plastic material in U.S.A. Hitachi finds flameproofing of plastic-sealed devices important to ensure product stability, and adopts the material with the highest flameproofing range V-0 defined by the UL94 standard. Table 2-2 shows flameproofing evaluation criteria of V-0 and HB (non-flameproofing).

2.1.7 Miscellaneous technology

Other than the technologies described above, Hitachi has improved such technologies as crystal processing, epitaxial growth, impurity diffusion, ion implantation, and photo etching.

Noise and leakage current of semiconductor devices result mainly from internal and surface defects or contamination of the crystal. Hitachi has tried various kinds of improved methods concerned with manufacturing, materials, equipment, and environment in the processes described above to eliminate these failures. For instance, product stability is ensured by adopting a method to decrease adverse effects due to surface polishing during crystal processing, a wafer rear face processing method to prevent lamination failure occurring at surface oxidation or diffusion, and an anneal method which is effective against lamination failure, and by improving materials used for photoresist and glassmask.

In addition, new automatic equipment for mask alignment or ion implantation has been utilized aiming at a full automation process. Hitachi has upgraded a variety of technologies pursuing cleanliness in the processing line, the first prerequisite in semiconductor manufacturing.

Table 2-2 UL94 Flameproofing Evaluation Criteria

V-0 (Vertical ignition 0 level)	HB (Horizontal ignition level)
A. Flaming within 10 sec after removing flame.	A. Burning rate below 1.5"/min when igniting the thickest specimen kept horizontally.
B. Flaming within 50 sec after applying flame to 1 set of 5 pieces 10 times.	
C. No flaming or glowing to pressure jig.	
D. No dropping of flaming grain ignition cotton below 12".	
E1. Glowing within 30 sec if removing flame ignited again after the procedure above.	
E2. Glowing but not igniting cotton after 10 sec have passed if removing flame ignited again after the procedure above.	

2.2 HITACHI'S PHILOSOPHY OF QUALITY AND RELIABILITY

Hitachi is always pursuing higher quality to meet individual users' and markets needs. User requested quality is clearly specified by contract in some cases, but is not very clear in other cases. Nevertheless, Hitachi is constantly trying to upgrade reliability so that all devices fully demonstrate their high performance in practical use.

To ensure better quality, Hitachi finds it important to establish quality control systems and to enhance quality consciousness in the manufacturing process. With the advance of device performance and expansion of application fields, the quality level needed by users is rising every year. Hitachi defines the following strategy to ensure better product quality.

(1) Consider fully reliability when developing new products
(2) Specify product quality at the beginning of the manufacturing process
(3) Strengthen inspection and reliability test of finished products
(4) Satisfy PPM target value by intensively pursuing failure potential from field data and test data

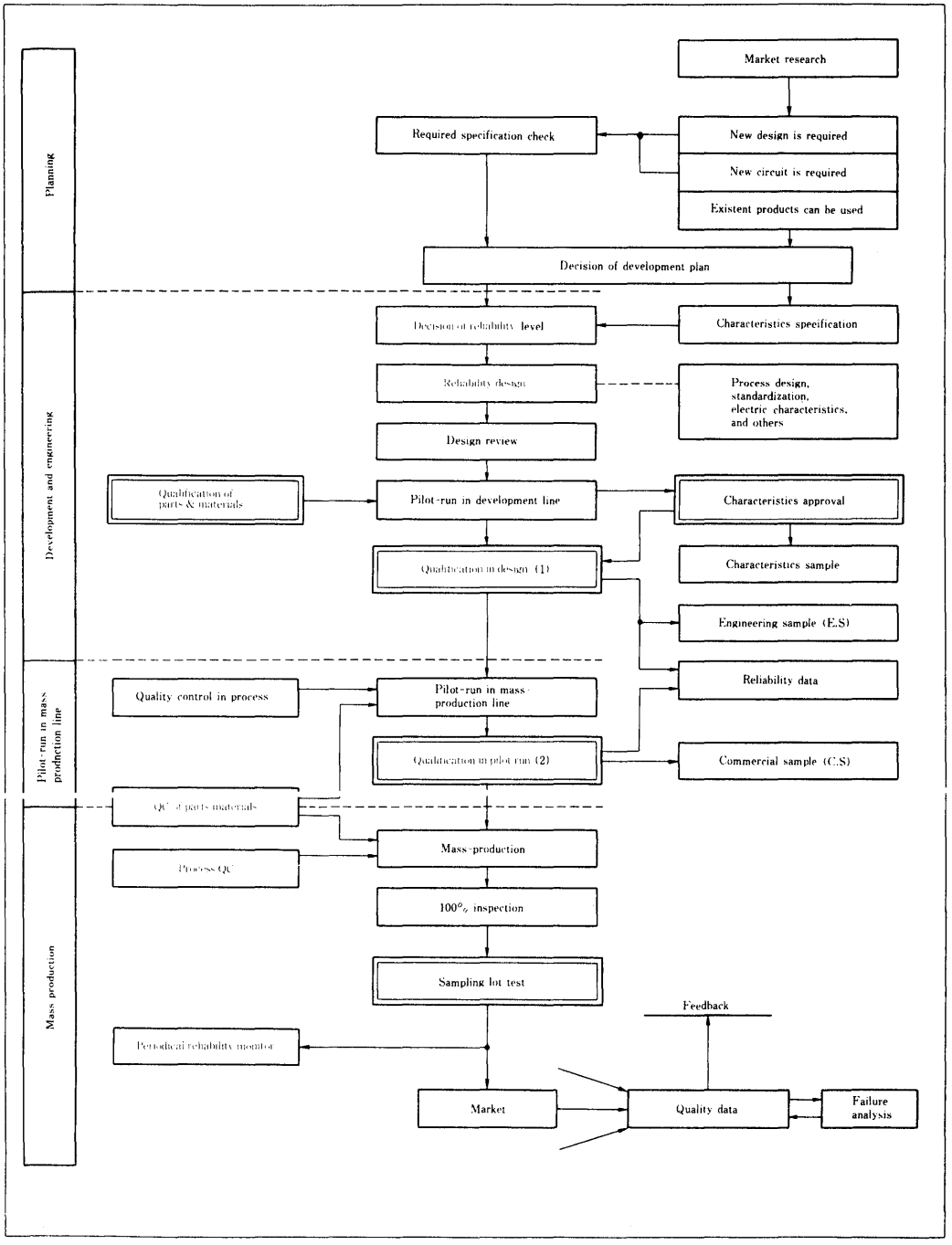
Table 2-3 shows an example of a reliability program. In this way, Hitachi is always trying to enhance the quality level and reliability of devices so as to fully satisfy users' needs.

2.3 RELIABILITY DESIGN FOR SEMICONDUCTOR DEVICES

2.3.1 Reliability target

Reliability target is an important item along with function and price when fabricating and marketing products. It is not practical to define a reliability target according to the failure ratio under a specific test condition. Hitachi, therefore, defines quality control at engineering, manufacturing, and processing sections, for screening, testing method, etc, depending on characteristics of each device by collectively considering environment where the device is used, target reliability of a system, derating, operating condition, maintenance, etc.

Table 2-3 An example of reliability programs



2.3.2 Reliability design

To satisfy requested reliability according to a reliability target, the following should carefully be examined and executed.

(1) Design standardization

To standardize device design, design rules must be defined, and parts, material, and processes standardized. For design rules, Hitachi always gives critical consideration on quality and reliability when defining rules for circuits, component, layout design, etc. Therefore, even for newly developed products, reliability is hardly affected as long as the standardized processes and materials are utilized.

(2) Device design

Collective device design is necessary in terms of circuit, layout, process and structure design. Especially when utilizing new processes or materials, Hitachi fully examines design technology prior to device development.

(3) Reliability evaluation by TEG

TEG (Test Element Group), sometimes called a test pattern, is an effective method to evaluate reliability of complicated IC and LSI design methods, and their manufacturing processes. It is also effective for transistors to raise their failure detection probability when applying new processes. The following describes TEG.

(a) Purpose of TEG

- ○ Define basic failure modes
- ○ Define relation between failure mode and manufacturing process conditions
- ○ Analyze failure mechanisms
- ○ Define QC points for manufacturing, etc.

(b) Evaluation of TEG effectiveness

- ○ Can evaluate common basic failure modes and failure mechanisms
- ○ Can make comparisons with actual user operations by identifying factors causing failure modes
- ○ Easily understood relations between cause of failures and process factors
- ○ Easily executable tests

As specific examples, types and pattern examples of TEG used in MOS IC are shown in Table 2-4 and Figure 2-18, respectively.

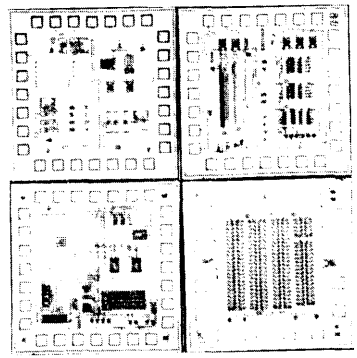


Fig. 2-18 An example of TEG pattern

Table 2-4 TEG types and check items

No.	Component		Check item
1	MOS transistor	Active MOS	Fluctuation in V_{TH}, and gm Fluctuation in junction voltage durability Fluctuation in leak current
2		Parasitic MOS	Fluctuation in field V_{TH} Fluctuation in junction voltage durability Fluctuation in leak current
3	Fundamental circuit	Unit cell	Fluctuation in operational margin Fluctuation in frequency characteristics Fluctuation in leak current
4	Contact		Degradation in ohmic characteristics Fluctuation in resistance value Fluctuation in leak current
5	Metal line		Fluctuation in resistance value

2.3.3 Design review

Design review is a systematic method to recognize whether or not the requested performance is fully satisfied, designing service is carried put in a specifies manner, technical improvement matters given by experiment data, field data, etc. are effectively taken into consideration. Also, design review is executed to enhance and ensure quality and reliability of products, in order to compete effectively with other developers.

Table 2-5 Design review standard

	Hitachi design review standard	NASA design review standard
Purpose	Reliability assurance required from the market	Guarantee for performance required by the space program
Definition	Promotion of systematic confirmation for various technical abilities	Systematic application of various technical abilities
Checking item	Correction of design failure	Correction of design failure
Checking subject	Specified products	Contracted projects
Period	Planning Intermediate design Final design	Preparation Before assembly Before issue
Organization Chairman of committee	Chief of designers	A person specified by the project manager
Members of committee	Manager in related dept., and a manager concerned with reliability	Manager or someone of upper rank and a manager concerned with reliability
Authorized limit of rights	Recommendation for improvement	Advise

Hitachi executes design review on new products as well as modified products from the stage of product planning.
This type of method is utilized in NASA. Table 2-5 shows comparison of design review criteria between Hitachi and NASA.
The items to be reviewed are as follows.
(1) Describe product according to design document
(2) Plan and execute subprograms such as calculations, experiments, or investigations, examining design document by specialists in various fields, if there is something unclear about design documents
(3) Determine reliability test contents and methods according to design document and drawings
(4) Check whether or not processability in the manufacturing workshop is sufficient to satisfy the design target
(5) Discuss production preparation
(6) Plan and execute subprograms such as tests, experiments, or calculations, to change device design following the suggestion of each specialist, or to determine such a change
(7) Review failure examples of similar products and determine preventive measures; plan and execute experimental programs to validate these measures
Hitachi performs the design review according to a check list specially defined for each product.

2.4 QUALITY ASSURANCE SYSTEM FOR SEMICONDUCTOR DEVICES

2.4.1 Quality assurance activity

This section describes Hitachi's general philosophy of quality assurance.

(1) Solve each process's problems; remove any potential failure factors in completed products
(2) Utilize feedback information to maintain good processability condition
(3) Ensure requested reliability and better quality by performing the above
The following sections describe quality control, reliability testing, etc.

2.4.2 Quality qualification

Hitachi executes quality qualification at sampling and mass-production to ensure requested quality and reliability, according to the reliability design described in section 2.3. The following shows the philosophy of quality qualification.
(1) Execute objective qualification from the customer's viewpoint
(2) Fully consider past failure specimens and field information
(3) Execute qualification also when design and process are changed
(4) Execute elaborate qualification for parts' materials and processes
(5) Determine control points at mass-production by examining processability and factors causing scatter
Hitachi executes the quality qualification shown in Figure 2-19, considering the above.

2.4.3 Quality and reliability control in mass-production

Hitachi controls product quality by effectively dividing the work between manufacturing section, inspection section, etc, as shown in Figure 2-20.

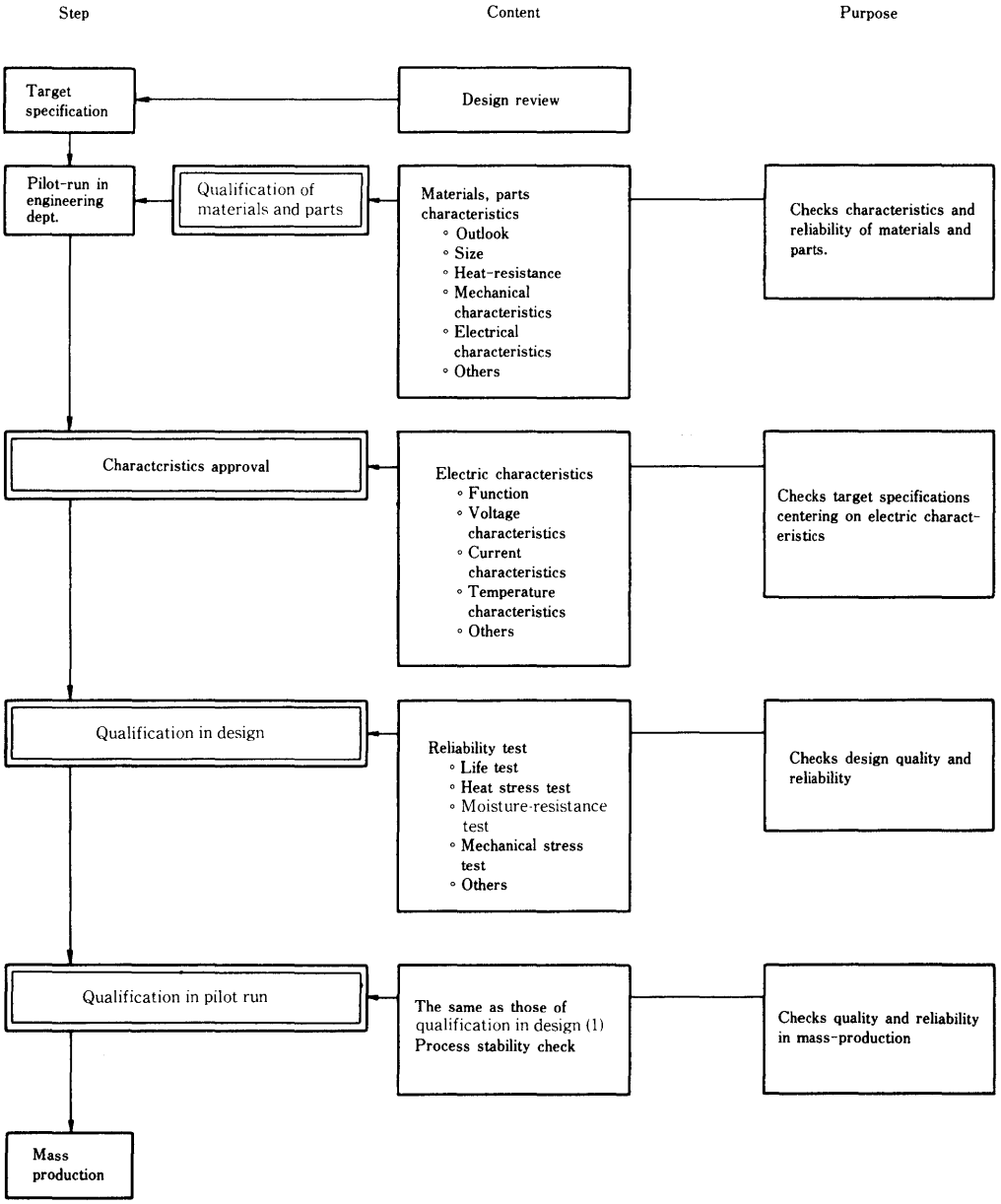


Fig. 2-19 Flowchart of quality authorization

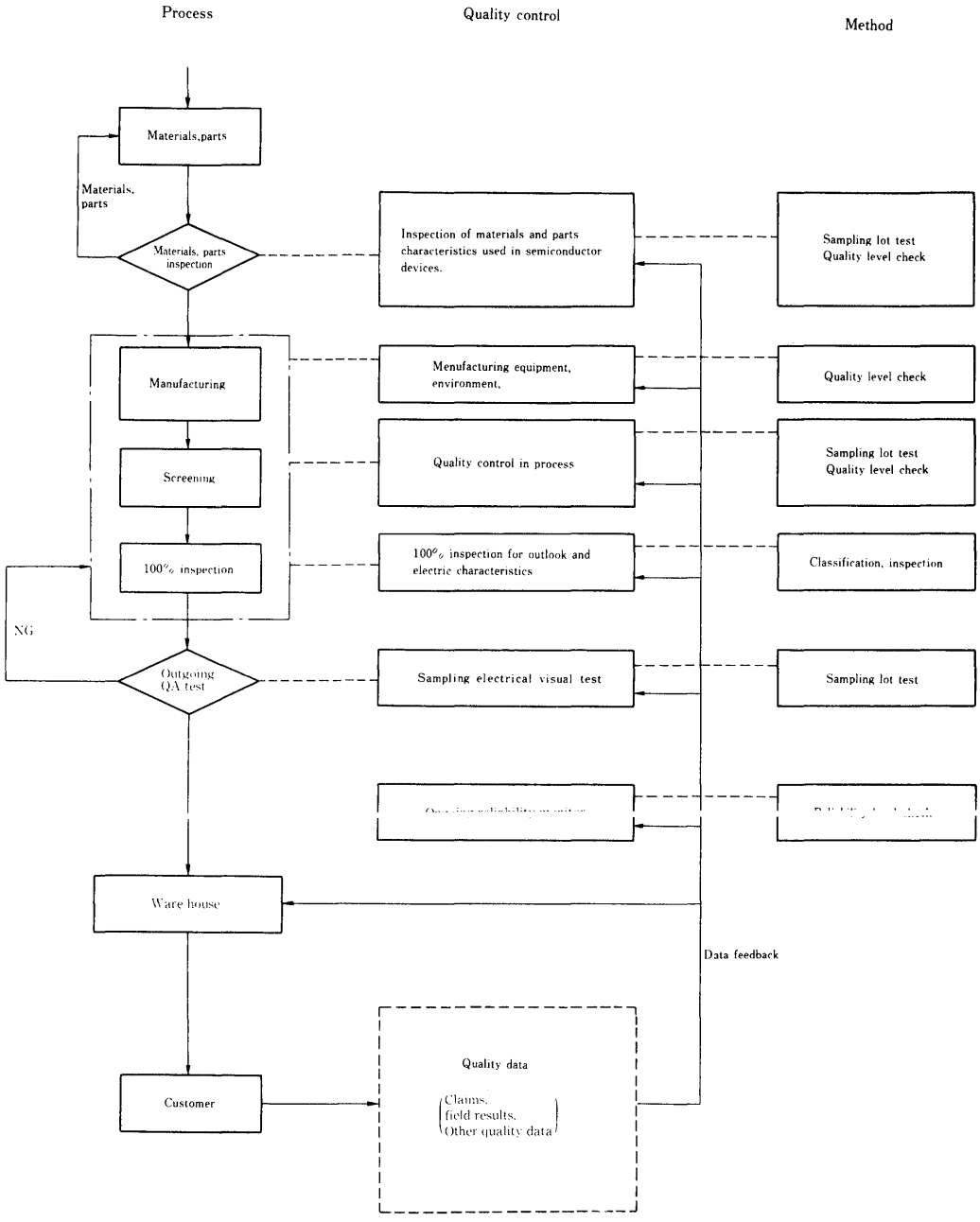


Fig 2-20 Flowchart of product control in manufacturing process

2.4.3.1 Quality control of materials and parts

With the advance in performance and reliability of semiconductor devices, quality control of materials and parts which are necessary to fabricate products, such as crystal, lead frame, bonding wire, package, etc, and of materials which are necessary in the manufacturing process such as mask patterns, chemicals, etc. is becoming more and more important. For quality control of materials and parts, incoming inspection is executed in addition to qualification of materials and parts. Sampling inspection following MIL-STD-105D is carried out for incoming inspection according to the incoming inspection standard defined by purchase specifications and drawings.

The following items are also carried out for quality control.

(1) Liaison meeting for purchasing external technology
(2) External order qualification, external order guidelines
(3) Physical and chemical analysis and testing

Table 2-6 lists the primary check points for materials and parts.

2.4.3.2 Internal process quality control

Internal process quality control is extremely important to ensure better quality of devices. The following describes how to control partially fabricated products, finished products, manufacturing equipment, measuring instrument, manufacturing environment, and sub-materials. Figure 2-21 shows an example of Internal process quality control.

(1) Quality control of partially fabricated products and finished products

Potential failure factors must be removed in the manufacturing process. Hitachi defines check points in each process and never delivers a product with a failure factor to the following process. Especially for high-reliability semiconductor devices, the manufacturing line is carefully selected, and precise quality control is executed for internal processes. Hitachi carefully checks each product lot in each process, executes 100% inspection in appropriate process to remove failure factors due to scattered manufacturing, and

Table 2-6 Check points for controlling materials and parts quality

Material/parts	Items to be controlled	Check items
Wafer	Appearance	Surface damage and contamination
	Size	Flatness
	Specific resistance	Resistance value
	Defect density	Number of defects
	Crystalline axis	
Mask	Appearance	Number of defects and flaws
	Size	Dimensional level
	Registration	
	Shading	Deviation in shading
Thin wire for wire-bonding	Appearance	Contamination, flaws, deflection, and twisting
	Size	
	Purity	Purity level
	Elongation ratio	Mechanical durability
Frame	Appearance	Contamination and flaws
	Size	Dimensional level
	Processing accuracy	
	Plating	Bondability and solderability
	Assembly characteristics	Heat resistance
Ceramic package	Appearance	Contamination and flaws
	Size	Dimensional level
	Air-tight leakage	Air-tightness
	Plating	Bondability and solderability
	Assembly characteristics	Heat resistance
	Electric characteristics	
	Mechanical durability	Mechanical durability
Plastic	Composition	Characteristics of materials
	Electrical characteristics	
	Heat characteristics	
	Moldability	Moldability
	Assembly characteristics	Assembly characteristics

Process	Control Points		Purposes
▽ Material purchase			
Wafer →	Wafer	Characteristics, Visual	Eliminate flaw and crystal defect
○ Surface oxidation	Oxidation		Ensure resistance value
□ Surface oxidation inspection		Appearance, Oxidation film thickness	Recognize pin-hole and flaw
○ Photoresist	Photoresist		
□ Photoresist inspection		Dimension, Visual	Recognize dimension level
—◇PQC level check			Check photoresist condition
○ Diffusion	Diffusion	Diffusion depth, Resistivity	Recognize diffusion condition
□ Diffusion inspection		Base width	Control basic characteristics (h_{FE} etc.)
—◇PQC level check		Oxidation film characteristics	Check cleanliness and V_{TH}
		Breakdown voltage	Check breakdown voltage level
○ Deposition			
□ Deposition inspection	Deposition	Deposition film thickness Flaw, Contamination	Ensure standard film thickness
—◇PQC level check			
□ Wafer inspection	Wafer	Wafer thickness	Reduction of voids, Scratches, discoloration
□ Chip electrical inspection	Chip	Electrical characteristics	
○ Chip scribing		Visual inspection	
□ Chip visual inspection			
—◇PQC lot acceptance		Visual after bonding	Check die bonding quality
Frame →			
Bonding → ○ Die bonding	Die bonding	Visual after bonding	Check wire bonding quality
○ Wire bonding	Wire bonding	Tensile strength, Application width shear strength	Prevent of wire short-circuit, Open-circuit
—◇PQC level check			
□ Inspection after assembly		Inspection after assembly	
—◇PQC lot acceptance			
Package →			
○ Sealing	Sealing	Visual inspection after sealing	Ensure appearance and dimension
○ Lead forming	Lead forming	Visual, Dimension	
○ Marking	Marking	Marking strength	
—◇PQC level check			
○ Final electrical inspection			
—◇Failure analysis		Failure analysis, Failure mode, mechanism	Feedback analysis information
□ Visual inspection			
△ Sampling inspection			
○ Register			
▼ Delivery			

Fig. 2-21 Example of Quality Control inside Process

Table 2-7 Examples of periodiac test for MOS memory

Test items	Testing conditions	Notes
Temperature Cycle test	−55°C−150°C 10 cycles	
High-temperature operation test	125°C, 48hrs	
	125°C, 1000hrs	
Humidity resistance	85°C 85%RH Bias 1000hrs	Plastic

performs necessary screening such as high-temperature aging, temperature cycle, etc.
The following lists the contents of internal process quality control.

- Control conditions for each piece of equipment and employee, and execute sampling inspection of partially fabricated products
- Propose and execute service improvement
- Educate employees
- Maintain and enhance yield
- Pick out problems on products and carry out countermeasures
- Communicate quality information

(2) Quality control of manufacturing equipment and measuring instruments

Manufacturing equipment is more and more advanced with higher-performance of devices and rationalization of production, and is extremely important to determine product quality and reliability. Hitachi promotes automation of manufacturing equipment to prevent manufacturing scatter, and controls each piece of high-performance equipment to operate and function appropriately.
Two types of checks are executed to control quality: daily check and periodic check. Every check point listed in the standard is thoroughly and carefully checked.
As for calibration of measuring instruments, calibration period is determined by defining custody no., specification, and calibration hysteresis. Measuring instruments are carefully checked according to the standard by using an officially qualified calibrator to ensure better quality.

(3) Quality control of manufacturing environment and submaterials

Quality and reliability of semiconductor devices greatly depends upon manufacturing processes. Hitachi fully controls the manufacturing environment such as temperature, moisture, dust, etc, and sub-materials such as gas and demineralized water. The following describes dust control.

Dust control is essential to realize higher-integration and higher-reliability. Hitachi maintains and promotes cleanliness in the workshop by periodically checking indoor floating dust, falling dust, floor soil, etc., paying attention to various points such as buildings, equipment, air-conditioning equipment, delivered goods, work clothes, service, etc.

(4) Control of changes

Hitachi defines procedures for any changes and determines product quality to maintain better quality and to prevent any failures after changes in manufacturing specification, working conditions, jigs, parts' materials, manufacturing section, etc.
For quality determination, Hitachi recognizes whether or not the requested quality and reliability is satisfied by executing qualification tests.
Depending on the contents of changes, customer's approval may be needed. In this case, Hitachi carries out discussions and coordinations between related sections prior to changes.

2.4.4 Failure management

If any failure is detected in a product after delivery, the product shall be returned to Hitachi by the request of customers or Hitachi. In this case, Hitachi's Marketing dept and Technical Marketing dept, together with Quality Assurance dept, should examine the product, conditions where it was used, period when it was used, conditions when the failure occurred, etc, and make appropriate response to the customers as soon as possible. Quality Assurance dept, in cooperation with engineering and manufacturing depts, should clarify the cause of failure and supply feedback to engineering and manufacturing depts, to prevent the failure from occurring again. Figure 2-22 shows how Hitachi manages failures.

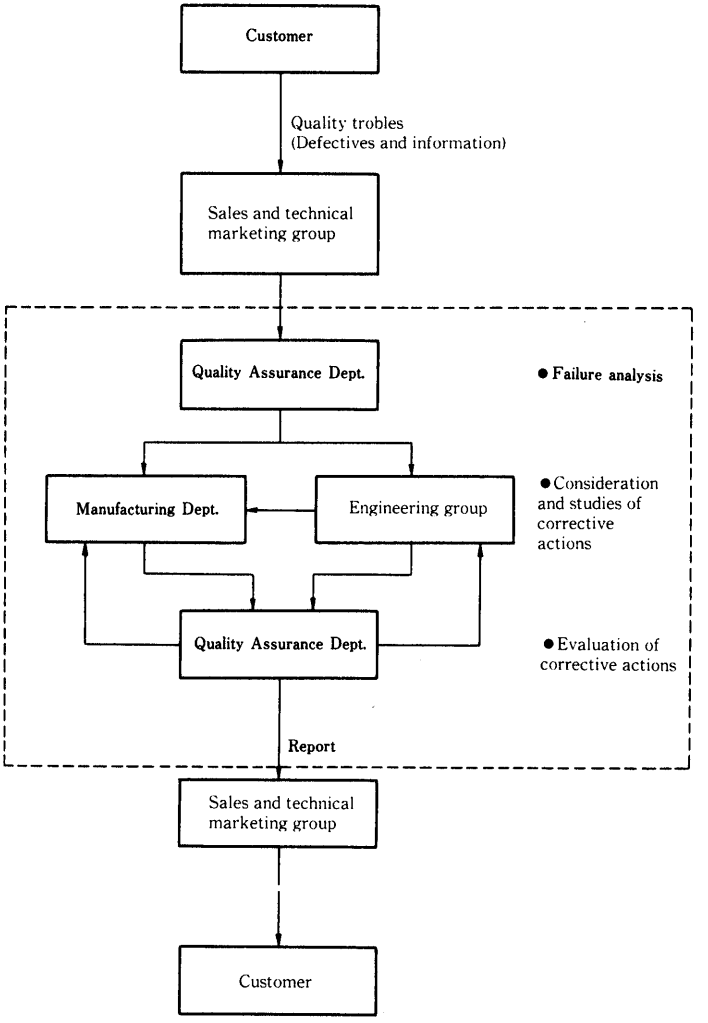


Fig. 2-22 A flowchart of transaction system for failures occurring customer sides

2.4.5 Reliability data collection

Hitachi estimates the field failure rate from process evaluation and reliability tests inside the company. This estimation is done by analyzing field data of similar products, or, in other words, quality information among users and markets. Figure 2-23 shows the failure rate trend of transistors, ICs, and LSIs used for components of large systems, as an example of field data. According to this figure, reliability of ICs and LSIs is being upgraded year by year. In this way, Hitachi pays careful attention to products after delivery, collects information from users, analyzes failures, and provides feedback quickly to engineering and manufacturing depts. The following describes field information and how it is used.

As for field data information,

- Early quality data on the device level
- Process data and early failure data on the sub-system level
- Debugging data such as burn-in on the system level
- Market data on the system level

are analyzed and effectively utilized to determine an attainable reliability target level, improve reliability design, process, acceleration tests, etc.

Field information is so important to ensure better reliability of products that it is directly collected from users through technical liaison meetings and the like.

In addition, Hitachi takes part in domestic and overseas data-exchange programs, and utilizes the obtained information to upgrade reliability.

As for data-exchange programs, the following are utilized.

- ? Reliability center for electronic components of Japan (RCJ) electronic parts reliability data-exchange program
- GIDEP (U.S.A.)
- EXACT (Europe)

Table 2-8 shows the RCJ field data sheet as an example.

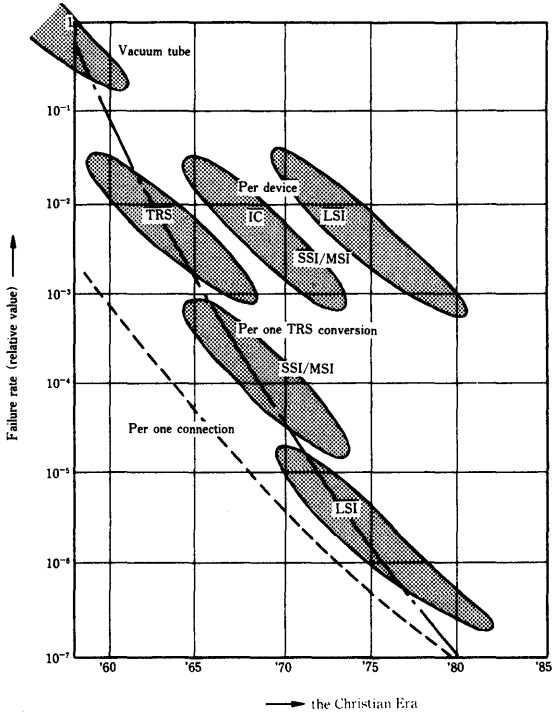


Fig. 23 The transition of the failure rate of semiconductor devices in a large-scale system

Table 2-8 Field Data Sheet

Prepared
Registered

① Company or Institute Name		Person in charge	Section
Address			Name Tel.
② Parts Code		⑤ Equipment Code	
Parts Name		Equipment Name	
STD No.		Parts structure, Ratings, Circuit Format, etc. (In case of no standard for similar products)	
Type No.			
③ Parts Supplier Name			
④ Installed Location	(a) Air-conditioned room (b) Ordinary room (c) Train (d) Automobile (e) Airplane (f) Ship (g) Portable (h) Outdoors (i)		

Conditions	⑥ (a) Used circuit	(1) Analog (2) Digital (3) Analog-Digital (4)
	⑦ (b) Ambient temperature Average (Max.)	(1) Below 0°C (2) 0 to 40°C (3) 40 to 60°C (4) 60 to 80°C (5) Above 80°C
	⑧ (c) Cooling method	(1) Natural cooling (2) Forced cooling (3) Other method ( )
	⑨ Ratings percentage (%)	(1) Below 20% (2) 20 to 50 (3) 50 to 80 (4) Above 80% of power, current, or voltage
	⑩ Operating Condition	(1) Continuous running (2) Average operating period/day (3) Average operating cycle
	⑪ Environment	(1) Heavy vibration (2) High dust (3) High moisture (4) Others ( )

⑫ Number of Units of Equipment		⑬ Number of Parts/ Equipment		⑭ Component Time T (10^4)	
Manufacturing Date		Running Start Date		Parts Component Time T (10^5) (Represented by numbers)	
⑮ Number of Failures	Breakdown maintenance		Total	⑯ Failure Rate fit (10^{-9} time) (Point estimation)	
	Preventive maintenance				

⑰ Number of Parts according to failure mode by breakdown maintenance:

Short circuit		Contamination	
Open circuit		Ambignous	
Breakage		Others	
Characteristics Value degradation			
Corrosion			

⑱ By preventive maintenance

(a) Individually check and exchange parts or sub-unit
(Write change rate to nominal value, if checking characteristics value of parts)

Parameter	Number of parts	Change rate (%)

(b) Periodically change parts or sub-unit.
(After hrs. have passed)

Comments by Parts Supplier

Code column

①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

⑭	⑮	⑯	⑰	⑱

(From RCJ)

3. RELIABILITY TEST METHODS AND TEST RESULTS

3.1 RELIABILITY TEST METHODS

3.1.1 For reliability testing, testing methods, testing conditions, and evaluation criteria should be appropriately selected depending on the product, its application, and test objectives. For example, the procedure for an endurance test is different from that of a test that checks whether or not device performance is passable under certain criterion.
Environmental factors (stress) are determined by taking device structures, processes, and operation conditions into account. There are many ways that stress can be applied; for example, single stress and combined stresses. Moreover, stress intensity and time-dependent stress should also be considered. In addition, we should check whether it is a screening or sampling test, and if a sampling test, sampling frequency should also be checked.
What is the most important factor in reliability testing is proper conjecture. At the same time, the test should contribute to improvement in device reliability. Accordingly, accumulation of actual reliability test results, failure analysis, and research on reliability improvement are required.

3.1.2 Reliability test methods

Standardized testing methods are required so as to obtain testing reappearance. These testing methods are determined by JIS standard, EIAJ standard, IEC standard, U.S. MIL standard, German DIN standard, and European CENELEC standard. Besides these, there are also standards registered by domestic government offices such as the Defence Agency, National Space Development Agency, NHK, and Japan Institute of Automobile Standards. From among these, generalized standards are shown in Table 3-1. Among these standards, JIS C7021 and C7022 are registered with the JIS standard based on EIAJ standards SD-121 and IC-121. Their summary is shown in Tables 3-2 and 3-3. ① Test objectives, ② Equipment and materials necessary for testing, ③ Testing method, and ④ Failure check method are described in the summary column of these tables. Notes from actual testing are described in the testing-points column. In the related-standard column, ⓐ to ⓓ indicates JIS C7021, IEC Pub. MIL-STD-750B, and MIL-STD-883C, respectively.

Table 3-1 Reliability testing standard

JIS standards
- JIS C 7030: Testing Methods for Transistors
- JIS C 7031: Testing Methods for Small Signal Diodes
- JIS C 7033: Testing Methods for Semiconductor Rectifier
- JIS C 7021: Environmental Testing Methods and Endurance Testing Methods for Discrete Semiconductor Devices
- JIS C 7210: General Rules for Reliability Assured Discrete Semiconductor Devices
- JIS C 5700: General Rules for Reliability Assured Electric Components
- JIS C 5020 General Rules of Basic Environmental Testing Procedure for Electronic Components
- JIS C 5003: General Test Procedure of Failure Rate for Electronic Components
- JIS C 7022: Environmental Testing Methods and Entrance Testing Methods for Semiconductor Integrated Circuits.
- JIS C 7310: General Rules for Reliability Assured Digital Semiconductor Integrated Circuit.

EIAJ standards
- EIAJ IC-121: Encironmental and Endurance Test Methods for Integrated Circuit
- EIAJ SD-121: Environmental and Endurance Test Methods for Discrete Semiconductor Devices.

IEC standards:
- Publication 68: Basic Environmental Testing Procedures.

CECC standards:
- CECC 50000: Generic Specification: Discrete Semiconductor Devices
- CECC 90000: Generic Specification: Monolithic Integrated Circuit

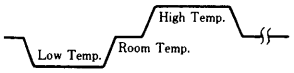
U S. MIL standards:
- MIL-STD-202E: Test Methods for Electronic and Electrical Component Parts
- MIL-STD-750B: Test Methods for Semiconductor Devices
- MIL-STD-883C: Test Methods and Procedures for Micro Electronics
- MIL-S-19500E: Semiconductor Devices, General Specification for
- MIL-M-38510C: Microcircuits General Specification for

Table 3-2 Summary of environment and weather resistance testing methods (JIS C 7022)

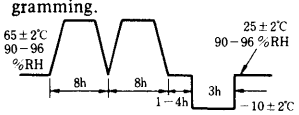
	Testing item	Summary	Notes on testing	Related standard (Note)
A-1	Soldering heat resistance test	① Checks heat resistance during soldering process. ② Solder component is Pb: Sn = 4:6 (H63A) ③ Dips device leads into solder of 260±5°C for 10±1 sec. as far as 1-1.5mm from the sample body. ④ Electrical characteristics	Dipping is performed one time	ⓐ A-1 ⓑ T ⓒ 2031.1

(Note) ⓐ JIS C 7021 ⓑ IEC Pub. 68. ⓒ MIL-STD-750B
ⓓ indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
A-2	Solderability test	① Checks the solderability of pins to be soldered. ② Solder component is Pb:Sn = 4:6 (H63A) Rosin isopropyl alcohol solution (25%) is used for flux. ③ Dips pins into solder bath of 230±5°C for 5±1 sec. after dipping them into flux. ④ Solder should be applied to more than 95% of the dipped portion. Pin holes or openings should not be concentrated on a certain portion, and their area should not exceed 5% of the total area.	Since a microscope of 10 to 20 magnification is used for this inspection and differences among individuals must be considered, it is recommended to prepare a limit sample.	ⓐ A-2 ⓑ 2-20 ⓒ 2026.2 ⓓ 2003
A-3	Thermal shock test	① Check device resistance against sudden temperature change. ② Two water baths of 100°C and 0°C. Pure water or supplied water (Condition A) ③ Method I: Devices are dipped in the hot bath for 15 sec. Next, they are transferred within 3 sec. and dipped in the cool bath. They are then transferred to the hot bath within 3 sec. after being dipped in the cool bath for at least 5 sec. This procedure is repeated 5 times. Method II: Devices are dipped in both baths alternately for 15 min., and the time for transfer is 10 sec, or less. ④ Electrical characteristics.	A temperature gradient is observed in a device, and stress strain occurs evenly with a uniform material. Measurement should be performed paying attention to bonding wire disconnections and pellet cracks. Fluorocarbon (FC-40, FC-77) is used in conditions B and C.	ⓐ A-3 ⓑ 2-14 ⓒ 1056.1 ⓓ 1011
	Temperature cycle test	① Checks device resistance against high and low temperatures and intermediate temperature changes. ② A high temperature bath and a low temperature bath having an air circulation system. ③ Example: low-temperature bath: 30 min. normal-temperature bath: 10 min. high-temperature bath: 30 min. normal temperature bath: 10 min. This procedure is repeated 5 times. ④ Wire breaks, short circuits, and electrical characteristics. 	Normally, Tstg max-min is selected. Since stress strain is generated in materials having different thermal expansion coefficients, care should be taken on the same points as the thermal shock test. Temperature change in each device differs depending on thermal capacity, thermal conductivity, and the number of devices. However, no special problem arises if the temperature changes in devices are within the range of Tstg max-min.	ⓐ A-4 ⓑ N ⓒ 1051.1 ⓓ 1010

(Note) ⓐ JIS C 7021 ⓑ IEC Pub. 68. ⓒ MIL-STD-750B (to be continued)
ⓓ indicates the testing method number of MIL-STD-883C.

	Testing item	Summary	Notes on testing	Related standard (Note)
A-5	Temperature-humidity cycle	① Checks stability in a high-temperature high-humidity condition. ② A bath in which temperature and humidity are controllable by programming.  ③ 1 cycle: 24 hr. 10 cycles are carried out. 5 cycles of the low-temperature (−10°C) should be carried out before 9-cycle. ④ Electrical characteristics	Temperature must be controlled so that the temperature does not reach 100%RH. Opening/closing of the door should be performed when the temperature in the bath is normal. Distilled water or deionized water. pH: 6.0 ~ 7.2 ρ: 50 kΩ·cm	ⓐ A-5 ⓑ D ⓒ 1021.1 ⓓ 1004
A-6	Seal test I (by He)	① Detection of slight leakage from a package. ② Puts a device in a closed vessel, and ③ He is pressurized at a prescribed time and pressure. Leakage detection is carried out by a mass analysis type leakage detector. Measurement is performed within 30 min. after the pressurization.	When leakage is great, a measurement error occurs because He escapes before the leak detection. It is recommended to check major leakage by performing the air-tightness test III (The reverse order is not possible).	ⓐ A-6 ⓑ Q_K ⓒ 1071.1 ⓓ 1014
	Seal test II (by Kr^{85})	① Detection of minor leakage. ② Puts a device in a closed vessel, and ③ Measures the amount of Kr35 entering the device by pressurization using a scintillation counter.	Since this method involves a radioactive pollution problem, it has become less and less used.	
	Seal test III (Test for major leakage by checking bubbles)	① Detection of major leakage in a package. ② Fluorocarbon (FC-48), silicon oil, or ethylene glycol. ③ Puts a device in the above solution heated at 125±5°C, and checks for bubbles appearing continuously from it. ④ If bubbles appear continuously from the same spot, it is considered that the device has a problem in air-tightness.	Since fluorocarbon evaporates at normal temperature, no washing is required after testing; however, it is quite expensive. In some cases, bubbles might be obserbed merely from an opening, strain, or surface absorption. Accordingly, this method requires some experience.	
A-7	Shock test	① Checks that devices can endure intense shock during transportation or actual use. ② A shock tester is used, whereby a prescribed half-sine wave acceleration can be applied. Normally, the prescribed acceleration can be obtained by raising a carriage (a device is fixed thereto) to a certain height, and then dropping it. ③ Selects among 100, 500, 1000, and 1500G. 3 shocks are applied per one direction to a device in the prescribed direction.	The acceleration should be selected by taking device materials and shapes into account. (Particular attention should be paid to ceramic packages).	ⓐ A-7 ⓑ Ea ⓒ 2016.2 ⓓ 2002

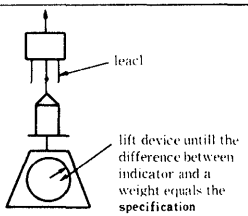
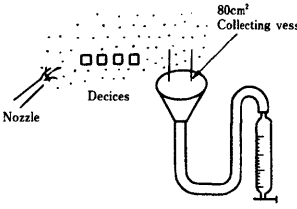
(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
	Natural drop test	① Checks that a device is durable against irregular shocks that might occur in normal handling. ② A flat maple board or equivalent (such as from a cherry) of 3cm or more thickness and 15 x 15 cm or more in size. ③ Drop a device naturally from a hight of 75 cm onto the maple board.	Care should be taken as to the drop direction according to the materials and shapes of devices. For example, when a large device is dropped leads first, the stem glass may sometimes break. This test is not applied for ceramic package.	ⓐ A-8 ⓑ Ed
A-9	Constant acceleration test	① Tests device durability against acceleration. ② A centrifugal accelerator. ③ Either 5000, 10000, or 20000G is applied in each X, Y, Z direction for one minute. ④ Electrical characteristics.	Tests mechanical durability of internal structures. Use a proper jig in which a package can be tightly fixed to the jig so that package deformity or destruction does not occur. Wire breaks are the main problem.	ⓐ A-9 ⓑ Ga ⓒ 2006 ⓓ 2001
A-10	Vibration test	① Tests how a device is influenced by vibration occurring during transportation and use. ② A vibration tester that can vary frequency. Wave shape: Sine wave ③ Fixes a package tightly to the vibrator using a jig. Vibration is applied to XYZ directions with equal testing times. 5 types of testing conditions are available. Two examples that are mainly used are shown below. Condition E: Freq. 60±20 Hz, Acceleration 20G, 96 Hr Condition D: Freq. 10-2000 Hz, 4 min./∞, 20G, 48 Hr ④ Electrical characteristics.	Since the size of semiconductor parts is small, the resonance frequency is high. Accordingly, condition D is more effective than condition E.	ⓐ A-10 ⓑ Fc ⓒ 2046.1 ⓓ 2005
A-11	Lead toughness test I (tensile test)	① Tests if a device is sufficiently durable against stress during attachment, wiring, or use. ② A tester, whereby a lead is pulled and the load can be measured. ③ Prescribed load is applied in the lead direction for 10±1 sec. Nominal cross-section area (mm^2) / Weight (kg) $0.05 < A \leqq 0.07$ / 0.25 $0.07 < A \leqq 0.2$ / 0.5 $0.2 < A \leqq 0.5$ / 1.0	Load should be applied gradually. When the tester is not provided, a prescribed weight may be hung at a lead. Another method can be employed in which a heavier weight is hung at the lead, and the weight is then put on an weighing machine. Adjust by lifting the device so that the difference between the pointer value of the machine and the weight becomes the prescribed value.	ⓐ A-11 ⓑ Ua ⓒ 2036.3 ⓓ 2004

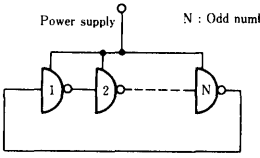
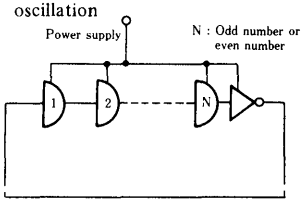
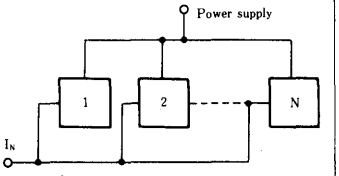
(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
		$0.5 < A \leqq 1.2$ 2.0 $1.2 < A$ 4.0	 Lifts a device so that the difference between load weight and the indicated value becomes the prescribed value.	
A-11	II	① ② Same as above. ③ A weight is hung at the tip of a lead. Next, the lead is bent 90° for within 5 sec., and then restored to its original position. Besides this test, torsion test and torque test for screw pins are available as pin toughness tests. (not described) Nominal cross-sectional area (mm^2) — Weight (kg) $0.05 < A \leqq 0.07$ — 0.125 $0.07 < A \leqq 0.2$ — 0.25 $0.2 < A \leqq 0.5$ — 0.5 $0.5 < A \leqq 1$ — 1.0 $1.2 < A$ — 2.0 ④ Relative shifts between leads and main body. Damage, and loosening.		ⓐ A-11 ⓑ Ub ⓒ 2036.3 ⓓ 2004
A-12	Salt atmosphere test	① Checks corrosion resistance and uniformity of a device surface. ② A temperature-controllable bath, whereby salt water is sprayed from a nozzle. ③ NaCl solution: 5% ± 1% (by weight) Temperature of salt water and bath is 35 ± 2°C. With respect to the spray amount, adjusts from 10-50 $g/m^2/d$. Unless specified, testing time is 24 ± 2 hr. Samples are washed by water at normal temperature after testing. ④ Unclear markings, peels, or pits on the surface are not acceptable. In addition, corrosion that results in a defective device is of course not acceptable.	 A bath from which no water drops form on devices should be prepared. In spite of such a bath, water drops are sometimes formed naturally, and can cause corrosion, making it difficult to judge. Accordingly, it is recommended to prepare a defective limit sample.	ⓐ A-12 ⓑ Ka ⓒ 1046.2 ⓓ 1009
A-13	Dip test	① Checks sealing effects. ② A hot water bath and a cold water bath. ③ One cycle is as follows: Dips into pure water at 65 ± 5°C for the specified time, and then dips		

(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
A-13		into pure water or saturated salt water at 25 ± 10°C for the specified time. 2 cycles are carried out. The dip time is 15 min. ④ Electrical characteristics.		
A-14	Solvent durability test	① Checks marking durability against solvent used for the removal of solder flux. ② A vessel made of materials non-reactive with the solvent. ③ A sample is dipped into a solvent selected from among isopropyl alcohol, trichloro ethylene, acetate-n-butyl, acetone, and tetrachloro-carbon at 25°C for 30 ± 5 sec. ④ Visual inspection to check markings.		ⓐ A-13
B-1	High-temperature ring oscillating operation test	(a) Inverter gate circuit ring oscillation.  (b) Non-inverter gate circuit ring oscillation  Ta = Topr max. 1000 times Applicable examples: Bipolar gate circuits and MOS gate circuits.	Check operation periodically or occasionally.	ⓐ 1015
	Hith-temperature alternate operating test	 A specified pulse is applied to the input; a specified load is connected to the output terminal. Ta = Topr max. 1000 times. Applicable example: Bipolar gate circuits MOS gate circuits Flip-flop circuits Bipolar memory circuits MOS shift register circuits	Check operation periodically or occasionally.	ⓓ 1015

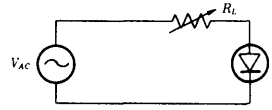
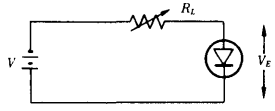
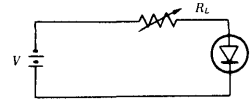
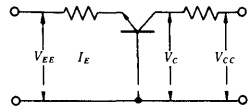
(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B (to be continued)
ⓓ Indicates the testing method number of MIL-STD-883C.

	Testing item	Summary	Notes on testing	Related standard (Note)
B-1	High-temperature direct current operation test	1) A specified voltage is supplied to the power supply terminal, and a specified voltage is supplied to the input, making the output either H or L. Applicable example: Bipolar and gate circuits, Flip-flop circuits, MOS gate circuits, and MOS memories. 2) Supply a specified voltage to the power supply terminal. Input voltage including application sequence is supplied so that a particular bit (only one) goes into a read out state. Applicable examples: Bipolar memories 3) A specified voltage is supplied to the power supply terminal. Connects the input to ground, and the output is left open. Applicable example: Operational amplifiers and comparators.		ⓓ 1015
B-2	Intermittent operation test	① Checks durability against change in electric or thermal stress when power is periodically applied in the way of ON-OFF. ②,③,④ The same as those of B-1 except for the method in which ON-OFF is periodically applied entirely or partially to input or power supply.		ⓐ B-6 B-7
B-3	High-temperature storage test	① Checks durability when a sample is stored at a high temperature for a long period of time. ② 1000 hr. at a maximum rated storage temperature. (Tstg Max) Under 125°C $^{+5°C}_{-3°C}$ More 125°C ±5°C	Oxidation on account of surface finish should be excluded from the evaluation. Remove stains using sandpaper when necessary so as to avoid contact failure due to oxidization of the terminals.	ⓐ B-10 ⓑ B ⓒ 1031.4 ⓓ 1008
B-4	Low-temperature storage test	① Checks durability when a sample is stored at a low-temperature for a long period of time. ③ Storage temperature: Maximum rated storage Tstg	If frost or water drops are present, remove them in advance.	ⓐ B-12 ⓑ C ⓒ 1021.1
B-5	Moisture resistance test	① Checks durability when a sample is used or stored in a highly humid atmosphere for a long period of time. ③ Conditions A 40 ± 2°C, 90 ± 5%RH B 60 ± 2°C, 90 ± 5%RH C 85 ± 2°C, 85 ± 5%RH	Deionized water is used. pH = 6.0-7 2 Temp.: 23°C Specific resistance: 50kohm·cm Care should be taken so that no water drops form on the device. In particular, apply bias after the inside of the bath becomes stable, and also after formed drops completely disappear.	ⓐ B-11 ⓑ A

(Note): ⓐ JIS C 7021 ⓑ IEC Pub. 68 ⓒ MIL-STD-750B
ⓓ Indicates the testing method number of MIL-STD-883C.

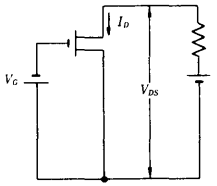
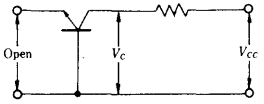
(to be continued)

Table 3-3 Summary of weather resistance testing method for transistors (JIS C 7021 except overlap of JIS C 7022)

	Testing item	Summary	Notes on testing	Related standard (Note)
B-1	Small-signal diode continuous operation test	 V_{AC} max = V_R max (50 or 60Hz) ±10% $R_L = V_{AC}(peak)/I_F$ (peak) Ta = 25 ± 5°C, 1000 hr		Ⓒ 1038
B-2	Zener diode, continuous operation test	 In the above circuit, an electric power of Pc max ± 5% is supplied. Ta = 25 ± 5°C 1000 hr	R_L should be such set so that the voltage drop at R_L is larger than V_Z.	Ⓒ 1038
B-3	Voltage variable capacitance diode, High-temp reverse bias test	 $V < V_R$ max. ±5% of the specific value Ta = Tj max 1000 hr	Monitoring method is recommended.	Ⓒ 1038
B-4	Transistor continuous operation test	 V_C = 0.4 to 0.6 x V_{CEO} max I_E is determined so that Pc = Pc max or Tj = Tj max. Both Vc and I_E should be within ±5% of the specified values. Ta = 25°C, 1000 hr	It's recommended to insert capacitances of 0.01 μF into E-B, C-B, and C-E to avoid oscillation.	Ⓒ 1039

(Note) Ⓒ Indicates the testing method number of MIL-STD-750B.

(to be continued)

	Testing item	Summary	Notes on testing	Related standard (Note)
B-5	Field effect transistor continuous operation test	 V_{DS} = 0.4 to 0.6 x V_{DS} max. I_D is determined so that P_T = P_T max. Both V_{DS} and I_D should be within ±5% of the specified value. Ta = 25°C, 1000 hr	If the gate turns on, in some cases, a large current may flow, destroying the device	Ⓒ 1036
B-6	Transistor intermittent operation test	Checks electrical-mechanical durability of a transistor against temperature change caused by ON-OFF.	Pay attention that no abnormal surge voltage is applied during the ON-OFF period.	Ⓒ 1036
B-7	Transistor intermittent operation test	The ON-OFF period is specified by the individual standards. Other conditions are the same as those of transistors and FET continuous operation test.		
B-8	Transistor high-temperature reverse bias test	 V_C = 0.7 to 0.8 x V_{CBO} max. V_C should be within ±5% of the specified value. Ta < Tj max, 1000 hr	When generated heat due to leak current is not negligible, decrease Ta or Vc so that Tj < Tj max.	Ⓒ 1036

(Note) Ⓒ Indicates the testing method number of MIL-STD-750B.

3.2 ACCELERATED LIFE TEST METHOD

The reliability of semiconductor devices are markedly influenced by the operational environment (e.g. junction temperature, temperature, humidity, voltage, and current conditions). Accordingly, the accelerated life test method has been normally employed as a means for estimating failure rate on the market.

The method of the accelerated life test is as follows:

Selecting a particular stress (e.g., voltage or junction stress) from actual stresses, a failure is investigated using the stress condition as a parameter, making it possible to estimate the failure ratio for actual operational conditions. This method is commonly used when new processes or devices are developed. In this section, the basic ideas of the accelerated life test are described.

3.2.1 Basic idea of the accelerated life test

When the accelerated test keeps a close relationship with failure physics, the test become effective. In other words, the test has been validated based on reaction kinetics; device failures occur as a result of physical-chemical reactions (crack generation, diffusion, or corrosion), and the reaction rate is determined by the stress factors.

An Arrhenius model, which is the most popular accelerated life model for semiconductor devices, and the Iring model, which is a modified model of the Arrhenius model, are described as follows:

(1) Arrhenius model

This model is commonly used when the accelerated test based on absolute temperature is carried out.

$$\ln L = A + E/R \cdot T$$

Where L is life time, A is a constant, E is activated energy [eV], T is absolute temperature [°K], and R is a gas constant.

Lifetimes L1 and L2 at temperatures of T1 and T2 can be represented as follows:

$$\log(L_1/L_2) = 5.009\ (1000/T_1 - 1000/T_2) \cdot E$$

The active energy of reaction, which is a scale of acceleration, can be determined using this formula. A conceptual figure of this model is shown in Fig. 3-4.

(2) Iring model

This model is commonly used when an acceleration based on stress is carried out, and is expressed as follows:

$$\ell n L = A - \alpha \ell n S$$

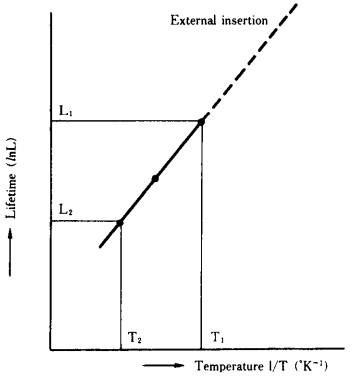


Fig. 3-1 A conceptual figure of Arrhenius model

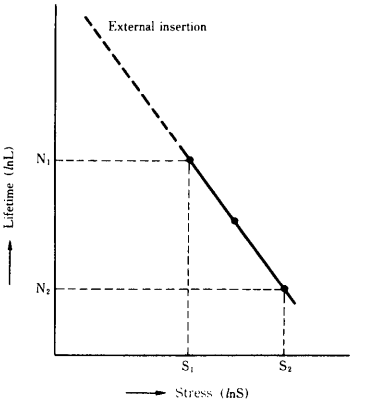


Fig. 3-2 A conceptual figure of Iring model

where L is lifetime, A and α are constants, and S is stress. In the case of material fatigue, alternating stress, and the number of repeated lifetimes N are employed. The relationship between repeated lifetimes N1 and N2 at the alternation stresses S1 and S2 is given by:

$$\ell n(N_1/N_2) = \alpha \ell n(S_1/S_2)$$

α, which represents the acceleration of this reaction, can be obtained using this formula. The conceptual drawing of this model is shown in Fig. 3-2. In JIS Z8115 (reliability terminology), the above acceleration life test is defined as "a test which is carried out in severer conditions than standard, and the object is to shorten testing time," and further defined as "failure mode and the cause should not be varied by acceleration so that the evaluation is valid."

Accordingly, the selection of acceleration factors and condition settings are key points.

When the accelerated life test is carried out, stress factors and conditions should be determined by assuming device manufacturing processes and the corresponding failure mechanism. Accordingly, the failure mechanism should be studied in advance through failure analysis of corresponding or similar devices. The accelerated life test can be classified according to stress application as shown in Table 3-4. The constant stress method is a technique in which the distribution of failure times is checked. On the other hand, the step stress method checks for the stress step where failure occurs by increasing stress step by step at constant time intervals (t_s).

Table 3-4 Classification of typical accelerated lifetime tests

Stress application method	Characteristics	Examples of accelerated test	Acceleration factor	Major failure mode
Constant stress application	Checks influence of stress on semiconductor device	High-temperature shelf test (Low-temperature shelf test)	Temperature	Surface degradation
		Operational lifetime	Junction temperature, Voltage	
		High-temperature high-humidity shelf test	Temperature, Humidity	Voltage durability degradation, Corrosion
		High-temperature high-humidity shelf test bias	Temperature, Humidity, Voltage	Corrosion, Inter-pin bridge
Cyclic stress application	Checks influence of repeated stress on semiconductor devices	Temperature cycle (Heat shock)	Temperature difference, duty	Wire break, short-circuit
		Power cycle	Temperature difference, duty	Wire break, Heat resistance degradation
		Temperature Humidity cycle	Temperature difference, Humidity difference	Wire break, short-circuit, Corrosion
Step stress application	Checks endurance limit of semiconductor device against stress	Operational lifetime	Junction temperature, Voltage	Device degradation
		High-temperature reverse bias	Junction temperature, Voltage	Device degradation
		Surge breakdown	Electricity amount, Voltage	Electrostatic breakdown, Device degradation
		Soldering heat resistance	Temperature, Time	Pellet cracks, Device degradation

3.3 RELIABILITY DATA FOR SEMICONDUCTOR DEVICES

Reliability data for Hitachi communication devices is described. Although current data is used, additional new data may be added because semiconductor devices are being developed in an innovative background. Since some devices are not mentioned in this section, refer to Hitachi's reliability data sheet for individual devices.

3.3.1 Reliability data for CODEC LSIs

Reliability test data for CODEC LSIs according to the reliability test methods described in the previous section are shown in this section. The results of high-temperature operation tests and high-temperature shelf tests are shown in Tables 3-5 and 3-6, and Table 3-7.
Thermal and mechanical environmental test results are shown in Table 3-8. Time-dependent fluctuation data of electrical characteristic parameters for CODEC LSIs obtained by high temperature operation tests are shown in Table 3-9.

Table 3-5 Reliability test result for CODEC LSI (1)

Testing item: High-temperature operation
Test condition: Ta = 125°C, V_{DD} = 5.5V, V_{SS} = −5.5V

Product name	Number of samples (pcs)	Total test time (hrs)	Number of defects	Failure rate* (1/hr)	Note
HD44231	294	3.60×10^4	0	2.5×10^{-5}	
HD44234	180	1.80×10^5	0	5.1×10^{-6}	
Total	474	2.16×10^5	0	4.3×10^{-6}	

* Confidence level: 60%

Table 3-6 Reliability test result for CODEC LSI (2)

Testing item: High-temperature operation
Test condition: Ta = 150°C V_{DD} = 5.5V, V_{SS} = −5.5V

Product name	Number of samples (pcs)	Total test time (hrs)	Number of defects	Failure rate* (1/hr)	Note
HD44231	503	5.30×10^5	2	5.8×10^{-6}	Oxidized film degradation
HD44232	48	8.40×10^4	0	1.1×10^{-5}	
HD44233	88	1.20×10^5	0	7.7×10^{-6}	
HD44234	268	1.50×10^5	0	6.1×10^{-6}	
HD44235	23	4.60×10^4	0	2.0×10^{-5}	
HD44236	24	4.80×10^4	0	1.9×10^{-5}	
HD44237	24	4.80×10^4	0	1.9×10^{-5}	
HD44238	109	2.20×10^5	0	4.2×10^{-6}	
Total	1087	1.25×10^6	2	2.5×10^{-6}	

* Confidence level: 60%

Table 3-7 Reliability test result for CODEC LSI (3)

Testing item: High-temperature operation
Test condition: Ta = 295°C

Product name	Number of samples (pcs)	Total test time (hrs)	Number of defects	Failure rate* (1/hr)	Note
HD44231	40	4.0×10^4	0	2.3×10^{-5}	
HD44233	15	1.5×10^4	0	6.1×10^{-5}	
HD44234	15	1.5×10^4	0	6.1×10^{-5}	
HD44238	19	1.5×10^4	0	4.8×10^{-5}	
Total	89	1.9×10^4	0	1.0×10^{-5}	

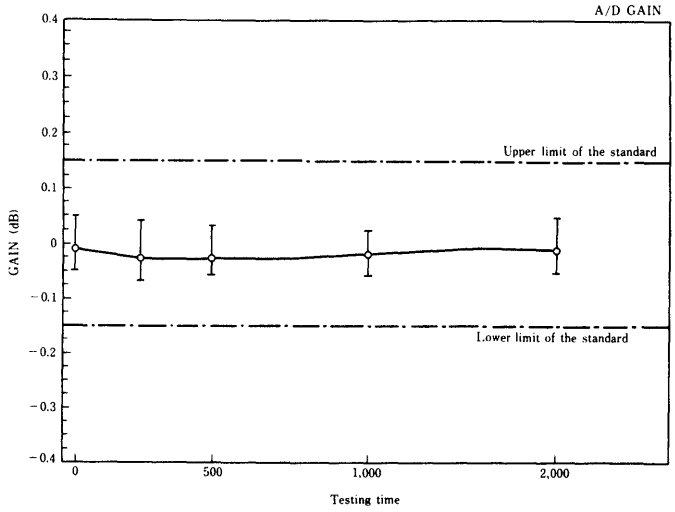
* Confidence level: 60%

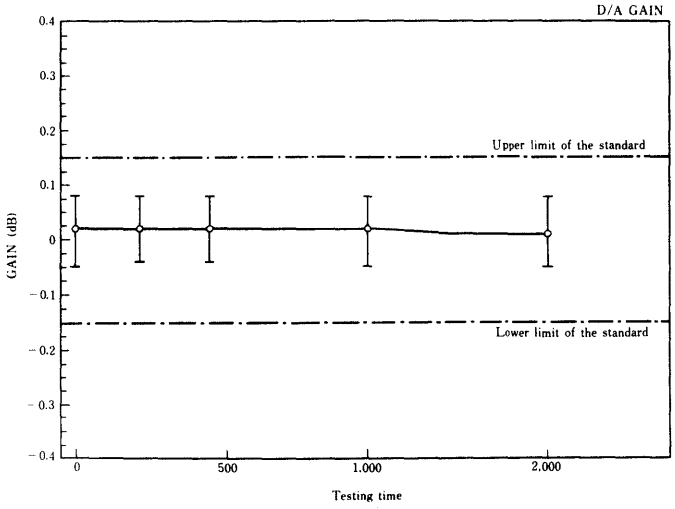
Table 3-8 Reliability test result for CODEC LSI (4)

Testing items	Test condition	Product name	Testing times	Number of samples	Number of defects
Temperature cycle (1)	−55°C to 150°C	HD44231	10 cycle	275	0
		HD44232		25	0
		HD44233		25	0
		HD44234		71	0
Temperature cycle (2)	−55°C to 150°C	HD44231	500 cycle	87	0
		HD44234		240	0
Heat shock	−65°C to 150°C	HD44231	30 cycle	30	0
		HD44234	15 cycle	15	0
Soldering heat resistance	260°C 10 sec	HD44231	–	13	0
		HD44234		44	0
Mechanical shock	1500G, 0.5msec, in each of X, Y and Z planes 3 times	HD44231		20	0
		HD44234		44	0
Variable frequency vibration	20 to 2000Hz, 20G, in each of X, Y and Z planes, 4 times	HD44231	–	20	0
		HD44234		44	0
Constant acceleration	20000G, in each of X, Y and Z planes, 1 minute	HD44231	–	20	0
		HD44234		44	0

Table 3-9 Fluctuation in characteristic for CODEC LSI

Fluctuation in characteristics		Time-dependent fluctuation in A/D and D/A gains according to lifetime testing for CODEC LSIs
Product name	HD44234B	
Testing condition	Ta = 150°C V_{DD} = +5.5V V_{SS} = −5.5V	
Number of samples	30 pieces	
Failure checking standard	A/D side Gain ±0.15dB D/A side Gain ±0.15dB	
Failure factor	V_{TH} shift due to such as surface degradation or contamination of gate oxidized films	





3.3.2 Reliability data for microcomputer LSIs

Reliability test data according to the reliability test methods described in the previous section are given in this section. Test data of 4-bit PMOS, 4-bit CMOS, 8-bit, and 16-bit NMOS LSIs are shown in Tables 3-10, 3-11, and 3-12.

(1) The distribution and fluctuation of both the A/D and D/A gains are within the standard with sufficient margin. No test results exceed the failure evaluation criterion.

Table 3-10 Reliability test results for microcomputer LSIs (1)

Test items	Test condition	4-bit microcomputer LSI Si-gate P channel plastic seal				4-bit microcomputer LSI Si-gate CMOS plastic seal			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
High-temperature operation lifetest	Ta = 125°C V_{DD} max	546	C.H. 5.6×10^{5}	1	3.6×10^{-6}	80	C.H. 0.8×10^{5}	0	1.2×10^{-5}
High-temperature shelf test	Ta = 150°C	43	0.2×10^{5}	0	–	53	0.2×10^{5}	0	–
Low-temperature shelf test	Ta = −55°C	90	0.4×10^{5}	0	–	–	–	–	–
High-temperature high-humidity lifetest	Ta = 65°C RH = 95%	1418	1.0×10^{6}	0	0.9×10^{-6}	80	0.6×10^{5}	0	–
	Ta = 85°C RH = 85% Bias application	45	0.2×10^{5}	0	–	–	–	–	–

* Confidence level: 60%

Table 3-11 Reliability test results for microcomputer LSIs (1)

Test item	Test condition	8-bit microcomputer LSI Si-gate N-channel ceramic seal				8-bit microcomputer LSI Si-gate CMOS plastic seal				16-bit microcomputer LSI Si-gate N-channel ceramic seal			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
High-temperature operation lifetest	Ta=125°C V_{DD} max	Pieces 1027	C.H. 9.4×10^{5}	1	2.1×10^{-6}	Pieces 331	C.H. 3.31×10^{5}	0	2.8×10^{-6}	Pieces 62	C.H. 0.62×10^{5}	0	1.5×10^{-5}
High-temperature shelf test	Ta=150°C	343	3.1×10^{5}	0	3.0×10^{-6}	–	–	–	–	42	0.42×10^{5}	0	–
Low-temperature shelf test	Ta=−55°C	66	0.7×10^{5}	0	–	–	–	–	–	42	0.42×10^{5}	0	–
High-temperature high-humidity lifetest	Ta=65°C RH=95%	90	0.9×10^{5}	0	–	176	1.39×10^{5}	0	6.6×10^{-6}	42	0.42×10^{5}	0	–
	Ta=85°C RH=85% Bias application	90 90	0.9×10^{5} 0.9	0	–	875	8.75×10^{5}	0	1.1×10^{-6}	42	0.42×10^{5}	0	–

* Confidence level: 60%

Table 3-12 Reliability test results for microcomputer LSIs (2)

Test item	Test condition	DIL plastic seal		QFP plastic seal		Ceramic seal (8-bit microcomputer LSI)		Ceramic seal (16-bit microcomputer LSI)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Heat shock	0°C to 100°C 10 cycles	150	0	100	0	76	0	44	0
Temperature cycle	−55°C to 150°C 10 cycles	1,637	0	1,514	0	397	0	42	0
Soldering heat resistance	260°C 10 sec.	140	0	160	0	88	0	22	0
Salt water spray	35°C NaCl 5% 24hr	20	0	20	0	22	0	22	0
Solderability	230°C 5 sec. Rosin flux	34	0	34	0	66	0	22	0
Natural drop	Used maple board 75cm, 3 times	24	0	20	0	76	0	44	0
Mechanical & shock	1,500G, 0.5ms in each of X, Y and Z planes, 3 times	–	–	–	–	66	0	44	0
Vibration fatigue	60Hz, 20G, in each of X, Y and Z planes 32hr.	120	0	20	0	66	0	44	0
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z planes, 4 times	–	–	–	–	66	0	44	0
Constant acceleration	20,000G, in each of X, Y and Z planes, 1 minute	–	–	–	–	66	0	44	0
Pin toughness	225g, 90°C bending test, 3 times for both sides	20	0	20	0	66	0	20	0

3.3.3 Reliability data for MOS memories

3 3.3.1 Reliability data of MOS dynamic and static RAMs

Lifetime test results for 1M DRAM (HM511000, HM514256), 256K SRAM (HM62256), and 1M SRAM (HM628128FP) sre shown in Tables 3-13 and 14. High-temperature and high-voltage lifetime tests are implemented so as to evaluate product reliability with few samples. Every failure occurring in the testing is due to faults in fabrication processes. These test results are reflected in the fabrication processes, enabling quality and reliability to be improved.

3.3.3.2 Reliability data for EPROMs

There are two types of EPROMs: one is the conventional type (a package with a window) in which written data is erasable by irradiating ultra-violet rays, and the other is the one-time writing type (OTP: one time EPROM). The latter is sealed into a plastic package.
Lifetime test results for 512K EPROMs (HN27512, HN27512P) and a 1M EPROM (HN27C101, HN27C301) are shown in Table 3-15.

The cause of the defects shown in Table 3-15 is data dissipation caused by a phenomenon in which charges (electrons) stored in memory cells escape from the floating gates out of a device by obtaining thermal energy. In this data dissipation phenomenon, although quite evident temperature dependency (activated energy: approximately 1.0 eV) is observed, no problems arise in actual use. The moisture resistance of plastic-sealed OTPs is quite favourable.

3.3.3.3 Reliability data for mask ROMs

Unlike EPROM/EEPROMs, since patterning is performed on mask ROMs in the manufacturing process according to the ROM data, no data dissipation occurs. The lifetime test results for 2M and 4M-bit mask ROMs are shown in Table 3-16.

3.3.3.4 Reliability data for MOS memories (environmental test results)

An example of environmental test results is shown in Table 3-17. Desirable results can be obtained without causing a failure even under severe environmental conditions.

Table 3-13 Reliability Data on 1M DRAM

Test item	Test condition	HM511000P/HM514256P Series (DIP)				HM511000JP/HM514256JP Series (SOP)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	125°C/5.5V	300	6.00×10^{5}	0	1.53×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	*1 Oxide film Failure x1
	125°C/7V	1252	4.50×10^{5}	1*	4.48×10^{-6}	3186	9.34×10^{5}	0	9.85×10^{-7}	
	150°C/7V	200	4.00×10^{5}	0	2.30×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	
Moisture endurance	85°C 85% RH 5.5V	420	8.40×10^{5}	0	1.10×10^{-6}	682	1.36×10^{6}	0	6.74×10^{-7}	
Pressure cooker	121°C/100% RH	150	4.50×10^{4}	0	2.04×10^{-5}	200	6.00×10^{4}	0	1.53×10^{-5}	

* Confidence level 60%

Table 3-14 Reliability Data on 256K and 1M SRAM

Test item	Test condition	HM62256FP (SOP)				HM628128FP (SOP)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	125°C/5.5V	3088	3.11×10^{6}	0	8.88×10^{-7}	1038	1.04×10^{6}	0	8.86×10^{-7}	*1 Foreign x 2 *2 Leak x 1
	125°C/7V	455	4.55×10^{5}	0	2.02×10^{-6}	951	5.33×10^{5}	1*1	3.79×10^{-6}	
	150°C/7V	103	1.00×10^{5}	1*1	2.02×10^{-5}	80	1.60×10^{5}	0	5.75×10^{-6}	
Moisture endurance	85°C/85% RH 7V	680	6.80×10^{5}	0	1.35×10^{-6}	127	2.54×10^{5}	0	3.62×10^{-6}	
Pressure cooker	121°C/100% RH	320	6.40×10^{4}	1*2	3.16×10^{-5}	90	2.70×10^{4}	0	3.41×10^{-5}	

* Confidence level 60%

Table 3-15 Reliability Data on 512K and 1M EPROM

Test item	Test condition	HN27512 (Cerdip/Plastic)				HN27C101/HN27C301				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature operation	125°C/5.5V	200	3.72×10^{5}	0	2.47×10^{-6}	180	3.24×10^{5}	0	2.84×10^{-6}	*1 Data dissipation x 49
	125°C/7V	530	7.95×10^{5}	0	1.16×10^{-6}	327	6.54×10^{5}	0	1.41×10^{-6}	
High-temperature bake	175°C	260	4.91×10^{5}	0	1.87×10^{-6}	150	7.5×10^{5}	0	1.23×10^{-6}	
	200°C	240	3.72×10^{5}	1*1	5.43×10^{-6}	130	6.49×10^{5}	1*1	3.11×10^{-6}	
	250°C	180	1.89×10^{5}	7*1	4.44×10^{-5}	110	3.07×10^{5}	40*1	1.30×40^{-4}	
Moisture endurance	85°C/85% RH 5.5V	290	5.22×10^{5}	0	1.76×10^{-6}	–	–	–	–	Data of 512K OTPROM
Pressure cooker	121°C/100% RH	50	0.10×10^{5}	0	9.20×10^{-5}	–	–	–	–	

* Confidence level 60%.

Table 3-16 Reliability Data on 2M and 4M MASK ROM

Test item	Test condition	HN62412P (Plastic)				HN62404P (Plastic)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total test time	Failures	Failure rate* (1/hr)	
High-temp. pulse operaton	125°C/5.5V	–	–	–	–	200	4.0×10^{5}	0	2.3×10^{-6}	
	125°C/7V	120	1.2×10^{5}	0	7.67×10^{-6}	300	3.0×10^{5}	0	3.0×10^{-6}	
Moisture endurance	85°C/85% RH 5.5V	120	1.2×10^{5}	0	7.67×10^{-6}	120	1.20×10^{5}	0	7.67×10^{-6}	
Pressure cooker	121°C/ 100% RH	45	2.3×10^{4}	0	4.1×10^{-5}	45	2.3×10^{4}	0	4.1×10^{-5}	

* Confidence level 60%.

Table 3-17 Reliability Data on MOS Memories

Test item	Test condition	HM511000P (DIP)		HM511000JP (SOJ)		HM62256FP (SOP)		HM628128FP (SOP)		EPROM (Cerdip)		Remarks
		Samples	Failure	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	–55°C to 150°C 10 cycle	3755	0	2786	0	3328	0	710	0	2790	0	
Temperature cycling	–55°C to 150°C 500 cycle	150	0	200	0	482	0	105	0	450	0	
Thermal shock	–65°C to 150°C 15 cycle	77	0	100	0	76	0	77	0	80	0	
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	22	0	22	0	
Mechanical shock	1,500G, 0.5ms	–	–	–	–	–	–	–	–	38	0	
Variable frequency	100 to 2,000Hz 20G	–	–	–	–	–	–	–	–	38	0	
Constant-acceleration	6000G	–	–	–	–	–	–	–	–	38	0	*6,000G

3.3.4 Reliability data for linear ICs

Reliability test data of an linear IC obtained according to the test method for semiconductor devices described in the previous section is shown in Table 3-18. As an example of characteristics fluctuation, input offset of an operation amplifier is shown in Table 3-19.

3.3.5 Reliability data for bipolar digital ICs

Test results according to the reliability evaluation test for semiconductor devices described in the previous section are described in this section. As an example of reliability test results for TTLs, a summary of standard TTL HD74 series is described in Tables 3-20 and 21. They are classified into plastic seal type and air-tight seal type. For more details on HD74 series products and reliability test results of other series products, refer to the reliability data book.

Table 3-18 Reliability test result for Linear IC

Test items	Test condition	Plastic moided type				Hermetic sealed type (Cerdip)			
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*
High-temperature operation	Ta = 125°C V_{CC} = V_{CC} max. (V_{CC} = V_{EE} max)	1,660	1,190,000	5	5.3×10^{-6}	2,345	2,424,600	0	3.8×10^{-7}
High-temperature shelf test	Ta = 150°c Ta = −55°C	829 509	793,000 509,000	0 0	1.2×10^{-6} 1.8×10^{-6}	485 –	463,700 –	0 –	2.0×10^{-6} –
Low-temperature shelf test	Ta = −65°C	–	–	–	–	376	376,000	0	2.4×10^{-6}
High-temperature high-humidity shelf test	Ta=65°C, 95%RH Ta=85°C, 85%RH	3,110	2,727,000	0	3.4×10^{-7}	–	–	–	–
High-temperature high-humidity operation	V_{CC}=V_{CC} max.	443	443,000	0	2.0×10^{-6}	–	–	–	–
Temperature cycle	−55°C to +150°C 10 cycles	10,043	–	0	–	2,198	–	0	–
Temperature cycle life-time	−55°C to +150°C 200 cycles	4,280	–	0	–	900	–	0	–
Heat shock	0°C to 100°C 10 cycles	398	–	0	–	311	–	0	–
Soldering heat resistance	260°C, 10 sec	404	–	0	–	305	–	0	–
Mechanical shock	1500G, 0.5ms., in each of X, Y and Z directions, 3 times	160	–	0	–	260	–	0	–
Vibration fatigue	60Hz, 20G, in each of X, Y and Z directions 32hrs.	160	–	0	–	260	–	0	–
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z directions, 3 times	160	–	0	–	260	–	0	–
Constant acceleration	20,000G, in each of X, Y and Z directions, 1 minute	160	–	0	–	260	–	0	–
PCT	Ta = 121°C, 2 atmospheric pressure, 60hrs	360	–	0	–	–	–	–	–
Solderability	230°C, 5 sec Rodin flux	160	–	0	–	300	–	0	–
Pin toughness	225g, 90° bending test, 3 times for both sides	90	–	0	–	45	–	0	–

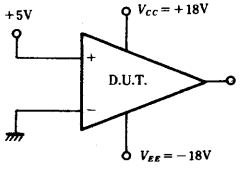
* Confidence level 60%

Table 3-19 Fluctuation in characteristics of Op-Amp. ICs

Fluctuation in characteristics	
Product	HA17747P (Plastic DIP)
Testing condition	Ta = 125°C, $V_{CC} = -V_{EE}$ = 18V continuous operation
Failure checking standard	V_{IO} = 9mV (Rs ≦ 10kΩ) V_{IO} = 300nA
Failure mechanism	Surface degradation, V_{BE} balance

Results:
1) Both V_{IO} and I_{IO} vary stably.
2) Both V_{IO} and I_{IO} are within the initial standard; neither exceeds the failure checking standard.

Note: Circuit diagram of operation test



Fluctuation in input offset voltage and current of Op-Amp. ICs.

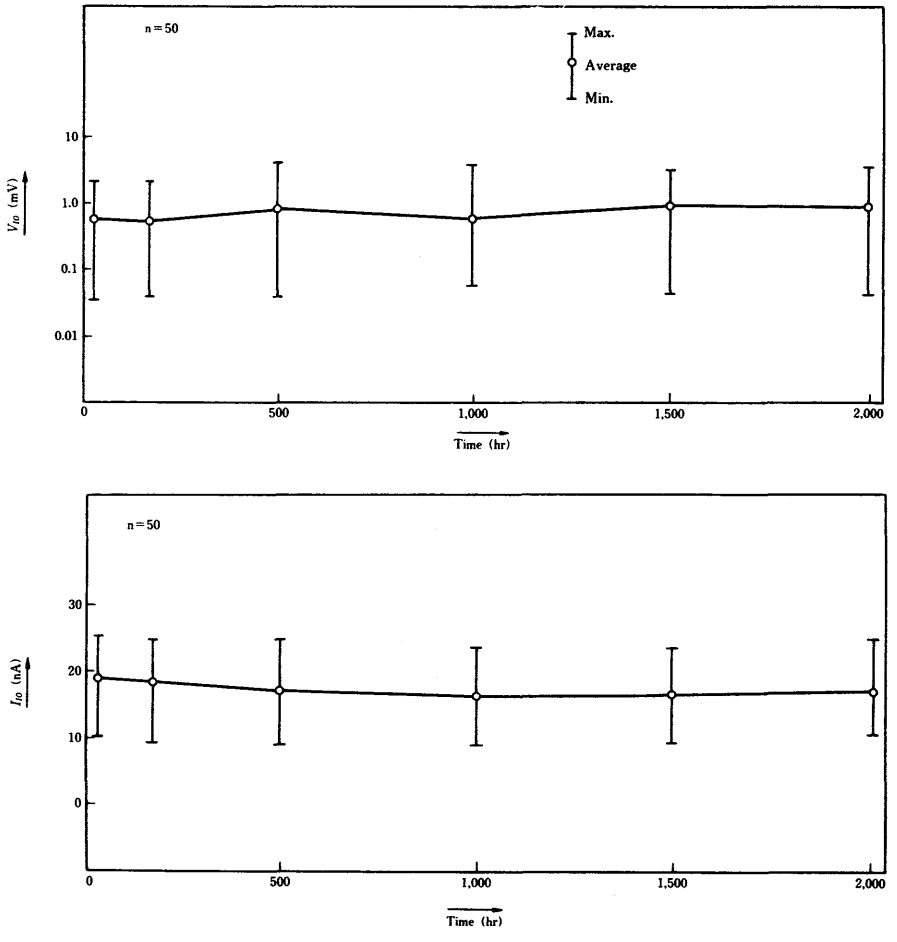


Table 3-20 Reliability test result for HD74 SERIES (1)

Test items	Test condition	Plastic DIP				Cerdip			
		Number of samples	Total test time	Number of defects	Failure rate (1/hr)*	Number of samples	Total test time	Number of defects	Failure rate (1/hr)*
High-temperature operation lifetime	Ta = 125°C V_{CC} = 5.5V	7,852	C.H. 7.3×10^6	2**	4.3×10^{-7}	3,390	C.H. 3.7×10^6	0	2.5×10^{-7}
	Ta = 150°C V_{CC} = 5.5V	–	–	–	–	3,771	3.3×10^6	0	2.8×10^{-7}
High-temperature shelf test lifetime	Ta = 150°C	1,488	6.4×10^6	0	1.4×10^{-7}	–	–	–	–
	Ta = 200°C	–	–	–	–	400	2.7×10^5	0	3.4×10^{-6}
Moisture-resistance lifetime	Stored at 65°C, 95%	11,312	1.1×10^7	1***	1.8×10^{-7}	600	6.0×10^5	0	1.5×10^{-6}
	Biased at 85°C, 85%	14,150	1.4×10^7	2***	2.2×10^{-7}	180	1.2×10^5	0	7.7×10^{-6}

* Reliability level 60% ** I_{IH} Large *** Al corrosion

Table 3-21 Reliability test results for HD74 SERIES (2)

Test item	Test condition	Plastic DIP		Cerdip	
		Number of samples	Number of defects	Number of samples	Number of defects
Nutural drop	Use maple board 75cm	Piece 334	Pieces 0	Pieces 480	Pieces 0
Mechanical shock	1500G, 0.5ms in each of X, Y and Z planes, 3 times	311	0	540	0
Vibration fatigue	60Hz, 20G, in each of X, Y and Z planes 32hr.	90	0	547	0
Variable frequency vibration	100 to 2000Hz, 20G in each of X, Y and Z planes, 4 times	90	0	409	0
Constant acceleration	20,000G in each of X, Y and Z planes once	160	0	480	0
Temperature cycle	–55°C to +150°C, 10 cycles	180,000	0	4,630	0
Heat shock	0°C to 100°C, 10 cycles	1,582	0	850	0
Soldering heat resistance	260°C, 10 sec.	653	0	835	0
Solderability	230°C, 5 sec., Rosin flax	1,333	0	950	0
Pin toughness	225g 90° bending, 3 times	99	0	60	0
Temperature cycle lifetime	–55°C to +150°C, 500 cycles	68,000	0	4,552	0

3.3.6 Reliability data for small signal transistors

Examples of lifetime and environmental test results are shown in Tables 3-22 and 23. For individual reliability test results, refer to reliability data for each product.

Table 3-22 Reliability test result for small signal transistors (1)

Testing item	2SC1707 Ⓗ type (NPN metal seal)					2SA537 Ⓗ type (PNP metal seal)					2SA1084 type (PNP plastic mold)				
	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate
		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr
Operation life-time	P_C= 200mW V_{CB}= 40V	1,000	1.0×10^6	0	0.92×10^{-6}	P_C= 0.75W V_{CB}= −50V	1,000	1.0×10^6	0	0.92×10^{-6}	Ta=25°C P_C= 400mW V_{CB}= −72V	200	2.0×10^5	0	0.46×10^{-5}
High-temperature reverse bias	Ta= 150°C V_{CES}= 400V	300	3.0×10^5	0	3.1×10^{-6}	Ta= 150°C V_{CES}= −50V	300	3.0×10^5	0	3.1×10^{-6}	Ta= 125°C V_{CES}= −90V	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 175°C	500	5.0×10^5	0	1.8×10^{-6}	Ta= 175°C	500	5.0×10^5	0	1.8×10^{-6}	–	–	–	–	–
High-temperature shelf test	–	–	–	–	–	–	–	–	–	–	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}

Testing item	2SC2468 type (FPAK)					3SK83 type (FPAK)					2SC2462 type (MPAK)				
	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate
		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr
Operation life-time	P_C= 200mW V_{CA}= 24V	200	2.0×10^5	0	0.46×10^{-5}	P_C= 200mW V_{DS}= 15V	200	2.0×10^5	0	0.46×10^{-5}	P_C= 150mW V_{CB}= 40V	200	2.0×10^5	0	0.46×10^{-5}
High-temperature reverse bias	Ta= 125°C V_{CES}= 30V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{DS}= 15V V_{G1S}= V_{G2S}= −5V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{CES}= 50V	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}

Testing item	2SD1368 type (UPAK)					3SK136 type (MPAK-4)					2SA1374 type (SPAK)				
	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate	Test condition	Number of samples	Total test time	Number of defects	Failure rate
		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr		Pieces	C.H.	Pieces	1/hr
Operation life-time	** P_C=1W V_{CB}= 100V	200	2.0×10^5	0	0.46×10^{-5}	Pch= 150mW V_{DS}= 20V	200	2.0×10^5	0	0.46×10^{-5}	P_C= 300mW V_{CB}= −55V	200	2.0×10^5	0	0.46×10^{-5}
High-temperature reverse bias	Ta= 150°C V_{CES}= 50V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{DS}= 20V V_{G1S}= V_{G2S}= −5V	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C V_{CES}= −55V	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 150°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}	Ta= 125°C	150	1.5×10^5	0	0.61×10^{-5}
High-temperature shelf test	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}	Ta= 85°C RH≧ 85%	300	3.0×10^5	0	0.31×10^{-5}

* Confidence level 60% ** Used specified heat sink

Table 3-23 Reliability test results for small signal transistors (2)

Test item	Test condition	2SC1775(Plastic mold)		2SC2468 (FPAK)		2SC2462 (MPAK)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Soldering heat resistance	260°C, 10 sec. 1.3mm from root	Pieces 120	Pieces 0	Pieces 120	Pieces 0	Pieces 120	Pieces 0
Heat shock	−196°C to +150°C, 5 minutes, 100 cycles	775	0	775	0	775	0
Temperature cycle	−55°C to 25°C to 150°C 10 cycles	4,500	0	4,500	0	4,500	0
MIL humidity resistance	−10°C to +65°C, RH≧90% 10 cycles	200	0	200	0	200	0
Mechanical shock	1,500G, 0.5msec. in each X, Y and Z directions, 3 times	80	0	80	0	80	0
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z planes, 4 minutes x 4 times	80	0	80	0	80	0
Vibration fatigue	60Hz, 20G in each of X, Y and Z planes 32hr.	80	0	80	0	80	0
Pin toughness (1)	450g, 90° bending test, 3 times for both sides	80	0	–	–	–	–
	225g, 90° bending test, once for both sides	–	–	80	0	80	0
Pin toughness (2)	450g, 10 sec.	80	0	80	0	80	0
Salt water spray	35°C, 5% salt water spraying test 48hr.	110	0	110	0	110	0

Test item	Test condition	3SK136 (MPAK-4)		2SD1368 (UPAK)		2SA1374 (SPAK)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Soldering heat resistance	260°C, 10 sec. 1.3mm from root	Pieces 120	Pieces 0	Pieces 120	Pieces 0	Pieces 120	Pieces 0
Heat shock	−196°C to +150°C, 5 minutes, 100 cycles	775	0	775	0	775	0
Temperature cycle	−55°C to 25°C to 150°C 10 cycles	5,600	0	4,500	0	4,500	0
MIL humidity resistance	−10°C to +65°C, RH≧90% 10 cycles	200	0	200	0	200	0
Mechanical shock	1,500G, 0.5msec. in each X, Y and Z directions, 3 times	80	0	80	0	80	0
Variable frequency vibration	100 to 2,000Hz, 20G, in each of X, Y and Z planes, 4 minutes x 4 times	80	0	80	0	80	0
Vibration fatigue	60Hz, 20G in each of X, Y and Z planes 32hr.	80	0	80	0	80	0
Pin toughness (1)	500g, 90° bending test, 2 times for both sides	80	0	–	–	–	–
	250g, 90° bending test, once for both sides	–	–	80	0	80	0
Pin toughness (2)	500g, 30 sec.	80	0	80	0	80	0
Salt water spray	35°C, 5% salt water spraying test 48hr.	110	0	110	0	110	0

Table 3-24 Fluctuation in characteristics of small signal transistors (1)

Fluctuation in characteristics (1)	
Product	2SC1707Ⓗ
Test condition	Ta = 125°C, V_{CES} = 50V
Failure checking standard	h_{FE} fluctuation ratio ± 10%
Failure mechanism	Surface degradation
Result: The fluctuation of h_{FE} which is highly sensitive to surface degradation of the emitter-base conjunction is evaluated. No or less fluctuation is observed as shown in the right figure.	
Note Air-tight seal	

h_{FE} Fluctuation (I_C = 100μA)

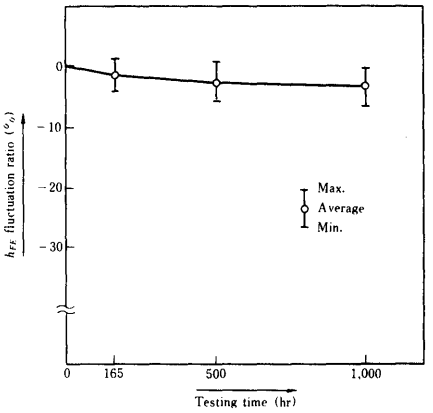
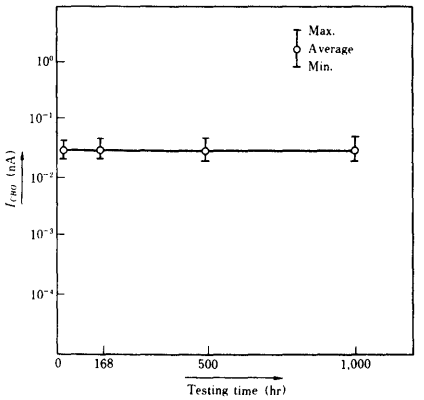


Table 3-25 Fluctuation in characteristics of small signal transistors (2)

Fluctuation in characteristics (2)	
Product	2SA1084
Test condition	High-temperature and high-humidity bias: Ta=85°C, RH=85%, V_{CES}=-90V
Failure checking standard	I_{CBO} initial standard value×2
Failure mechanism	Surface degradation due to water permeation
Result: The fluctuation of I_{CBO} which is highly sensitive to surface degradation of the collector-base junction is evaluated. No device has current leakage of 0.1 nA or more even after 100 hr. of testing.	
Note Plastic seal	

I_{CBO} fluctuation (V_{CB} = -60V)



3.3.7 Reliability data for power transistors

Examples of reliability test results for power transistors are shown in Tables 3-26 and 27. For individual reliability test results, refer to the reliability data for each product.
Checking characteristic fluctuation by the reliability test is very effective to grasp the reliability and quality level of products. In particular, with respect to characteristic items having no margin in circuit design, study of the characteristic fluctuation is required by taking operational conditions into account. In particular, with respect to high output device applications, this is very important since heat radiation design greatly influences the reliability. Examples of characteristic fluctuations are shown in Tables 3-28 to 30. During attachment, care should be taken that excessive force is not applied to devices. (tightening torque, foreign material between devices and heat sink plates, etc.)

Table 3-26 Reliability test result for Power transistors (1)

Test item	Test condition	2SB638Ⓗ/2SD628Ⓗ(TO-3)				2SK135(TO-3) power MOS FET				2SC3336 (TO-3P)			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
Operation lifetime	T_j=150°C	Piece 44	C.H. 4.4×10^4	Piece 0	1/hr 2.1×10^{-5}	Piece 80	C.H. 1.6×10^5	Piece 0	1/hr 5.8×10^{-6}	Piece 50	C.H. 5.0×10^4	Piece 0	1/hr 1.8×10^{-5}
High-temperature contrary bias	Ta=150°C $V_{CB}=V_{CB}$ max	50 V_{CB}=100V	5.0×10^4	0	1.8×10^{-5}	125 V_{DS}=160V V_{GS}=−10V	2.5×10^3	0	3.7×10^{-6}	50 V_{CB}=500V	5.0×10^4	0	1.8×10^{-5}
High-temperature shelf test	Ta=150°C	50	5.0×10^4	0	1.8×10^{-5}	80	1.6×10^5	0	5.8×10^{-6}	50	5.0×10^4	0	1.8×10^{-5}
High-temperature high-humidity shelf test	Ta=65°C RH≧95%	–	–	–	–	–	–	–	–	50	5.0×10^4	0	1.8×10^{-5}
Power cycle	ΔTc=90°C	50	Cycle 5.0×10^5	0	1.8×10^{-6} /cycle	50	Cycle 5.0×10^5	0	1.8×10^{-6} /cycle	50	Cycle 5.0×10^5	0	1.8×10^{-6} /cycle

Test item	Test condition	2SD768Ⓚ(TO-220)				2SC1514(TO-202)				2SD1081(DPAK)			
		Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate	Number of samples	Total test time	Number of defects	Failure* rate
Operation lifetime	with heat sink T_j=150°C	Piece 40	C.H. 4.0×10^4	Piece 0	1/hr 2.3×10^{-5}	–		–	–	–	–	–	–
	Free air T_j=150°C	40	4.0×10^4	0	2.3×10^{-5}	Piece 150	C.H. 1.5×10^5	Piece 0	1/hr 6.1×10^{-6}	Piece 150	C.H. 1.5×10^5	Piece 0	1/hr 6.1×10^{-6}
High-temperature contrary bias	Ta=150°C $V_{CB}=V_{CB}$ max	60 V_{CB}=120V	6.0×10^4	0	1.5×10^{-5}	120 V_{CB}=300V	1.2×10^5	0	7.6×10^{-6}	120 V_{CB}=180V	1.2×10^5	0	7.6×10^{-6}
High-temperature shelf test	Ta=150°C	76	7.6×10^4	0	1.2×10^{-5}	120	1.2×10^5	0	7.6×10^{-6}	120	1.2×10^5	0	7.6×10^{-6}
High-temperature high-humidity lifetime	Ta=65°C RH≧95%	40	4.0×10^4	0	2.3×10^{-6}	120	1.2×10^5	0	7.6×10^{-6}	120	1.2×10^5	0	7.6×10^{-6}
Power cycle	ΔTc=90°C	80	Cycle 8.0×10^5	0	1.2×10^{-6} /cycle	80	Cycle 8.0×10^5	0	1.2×10^{-6} /cycle	80	Cycle 8.0×10^5	0	1.2×10^{-6} /cycle

* Confidence level, 60%

Table 3-27 Reliability test result for power transistors (2)

Test item	Test condition	2SD628 Ⓗ (TO-3)		2SC3336 (TO-3P)		2SD768Ⓚ		2SC1514 (TO-202)		2SD1081 (DPAK)	
		Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects	Number of samples	Number of defects
Soldering heat resistance	260°C 1.5mm 10 sec.	Pieces 22	Pieces 0	Pieces 22	Pieces 0	Pieces 20	Pieces 0	Pieces 75	Pieces 0	Pieces 22	Pieces 0
Heat shock	0 to 100°C 5 cycles	44	0	44	0	75	0	75	0	75	0
Temperature cycle	−55 to +150°C 10 cycles	767	0	1,152	0	767	0	767	0	1,152	0
Mechanical shock	1500G, 0.5msec 3 directions 3 times each	44	0	44	0	45	0	67	0	45	0
Natural drop	Used maple board 75cmx3times	400	0	1,152	0	800	0	350	0	800	0
Vibration fatigue	60Hz, 20G 3 direction, 96hr	22	0	45	0	45	0	67	0	45	0
Pin toughness	Stretch test 24hr	22	0	22	0	20	0	67	0	22	0
Salt water spray	5% saltwater spraying test 24Hr	22	0	22	0	20	0	–	–	22	0

Table 3-28 Fluctuation in characteristic of Power Transistors

Fluctuation in characteristics (1)	
Product	2SD628Ⓗ
Test condition	$\Delta Tj = 105°C$*
Failure checking standard	ΔV_{BE} initial standard value x 1.2
Failure mechanism	Material fatigue

Result:
The fluctuation of V_{BE} having an evident correlation with θ_{jc} through the power cycle is plotted in the right figure. No or less fluctuation is observed at a range up to 30,000 cycles.

Note
*ΔTj: Temperature differences in functions

Fluctuation in ΔV_{BE} through the power cycle

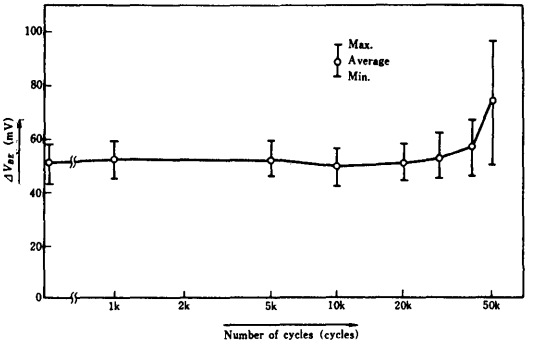


Table 3-29 Fluctuation characteristic of in Power-MOS FET

Fluctuation in characteristics (2)		Fluctuation in voltage durability and saturation voltage under high-temperature reverse bias conditions
Product	2SK135	
Test condition	Ta = 150°C V_{DS} = 160V, V_{GS} = −10V	
Failure checking standard	V_{DSX} initial standard value x 0.8 $V_{DS(sat)}$ initial standard value x 1.2	
Failure mechanism	Surface degradation	
Result: 1. No or less fluctuation in voltage durability is observed even after 2,000 hr. 2. With respect to the saturation voltage change, a slight increase is observed at the initial stage; however, all are completely saturated after 2,000 hr.		
Note:		

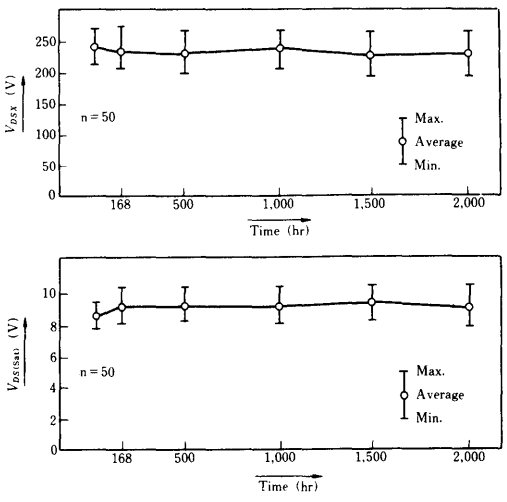
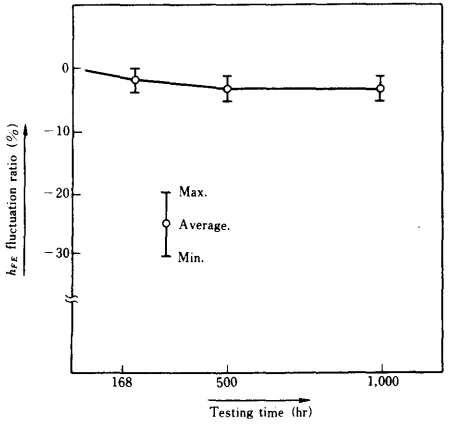


Table 3-30 Fluctuation in TO-3P transistors

Fluctuation in characteristics (3)		h_{FE} fluctuation (I_C = 1.0A)
Product	2SC3336	
Test condition	Ta = 150°C, V_{CES} = 500V	
Failure checking standard	h_{FE} fluctuation ratio ±20%	
Failure mechanism	Surface degradation	
Result: The fluctuation of h_{FE} which is highly sensitive to surface degradation of the emitter-base junction is evaluated. No or less fluctuation is observed as shown in the right figure.		
Note	Plastic molded type	



3.3.8 Reliability data for infrared LEDs

Examples of reliability data for infrared LEDs are described. Reliability test results of RG-type devices of HLP series are shown in Table 3-31.

(3) Characteristic fluctuation

Time-dependent variational data examples of light emitting power by operation lifetime tests for RG type devices in HLP series are shown in Table 3-32.

3.3.9 Reliability data for laser diodes

Examples of reliability data for laser diodes are described. Reliability test results of HL and HLP series devices are shown in Table 3-33. For individual reliability test results, refer to reliability data for each product.

Time-dependent characteristic variational data examples from operational lifetime tests for HL and HLP series are shown in Table 3-34.

Table 3-31 Reliability test results for infrared LEDs

Test item	Test condition	RG type (Air-tight sealing)		
		Number of samples (Piece)	Test time (hr)	Number of defects (Piece)
Operational lifetime	Ta = 25°C, I_F = 200mA, RG type: Free air	22	1,000	0
Intermittent operation lifetime	2 min. for ON, and 1 min. for OFF under the same conditions as the above	22	1,000	0
Temperature shelf test	Ta = 100°C	11	1,000	0
High-temperature high-humidity shelf test	Ta = 60°C, RH ≧ 90%	15	1,000	0
Low-temperature shelf test	Ta = −40°C	15	1,000	0
Temperature cycle	−40 to +100°C, 30 minutes each, 10 cycles	22	1,000	0
Vibrational fatigue	60Hz, 20G, 2 directions each 32hr.	15	–	0
Variable frequency vibration	100 to 2000Hz, 20G 4 minutes for both sides, 2 directions, 3 times each			
Mechanical shock	1500G, 0.5msec, 2 directions, 3 times each			
Lead bending	225g, 90° 3 times	11	–	0
Soldering heat resistance	260°C, 10sec.	11	–	0
Solderability	230°C, 5sec.	11	–	0

Table 3-32 Fluctuation in infrared LEDs

Fluctuation in characteristics	
Product	HLP30
Test condition	Ta = 25°C, IF = 200mA RG type: Free air
Failure checking standard	Initial standard value of light emitting power × 0.7
Failure mechanism	Crystalline failure

Result:
The fluctuation in outputs from forward-direction continuous operational test is shown in the right figure.
Since heat radiating conditions are different, decrease in the light emitting output of the RG package is slightly greater than others.

Fluctuation in light emitting power (I_F = 200mA)

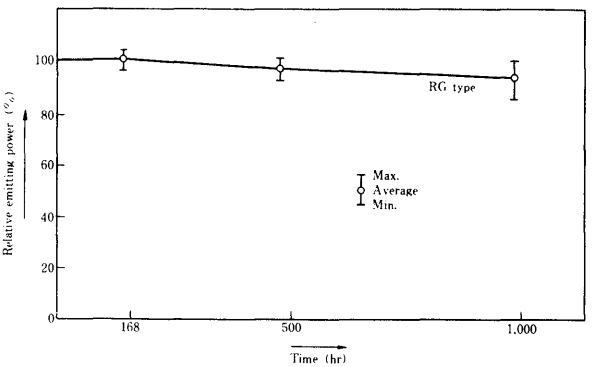


Table 33 Reliability test result for laser diodes

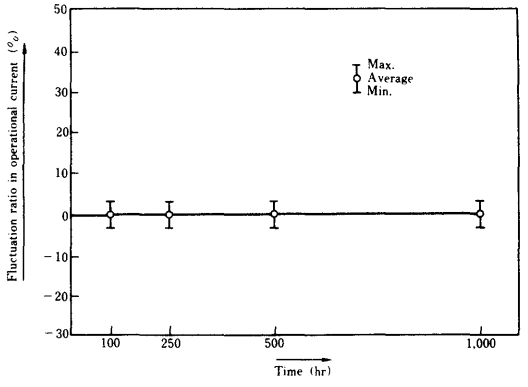
Test item	Test condition	Number of defects / Number of samples					
		HL7801E	HL7801G	HLP1500	HL8312E	HLP5400	HLP5500
Operation lifetime	50°C, N_2 atmosphere Po = 5mW, APC 1,000 times	0/100	0/100	0/20	0/50	0/50	0/20
Temperature cycle	−40 (30 min.) to 25(15 min.)to 70°C(30 min.) 10 cycles	0/50	0/50	0/45	0/50	–	0/20
Temperature cycle lifetime	−40 (30 min) to 25 (15 min.) to 70°C (30 min.), 100 cycles	0/20	0/20	0/10	0/20	–	0/10
Heat shock	0 (5 min.) to 100°C (5 min.), 10 cycles	0/10	0/10	0/5	0/10	–	0/5
Soldering heat resistance	260°C, 10 sec.	0/10	0/10	0/5	0/10	–	0/5
High-temperature shelf test	Ta = 70°C, 1,000 times	0/10	0/10	0/5	0/10	0/10	0/5
High-temperature high-humidity shelf test	Ta = 60°C RH ≧ 90%, 1,000 times	0/50	0/50	0/10	0/50	–	0/20
Low-temperature shelf test	Ta = −40°C, 1,000 times	0/10	0/10	0/5	0/10	–	0/5
Mechanical shock	1,500G, 0.5msec XYZ directions 3 times each	0/10*	0/10*	0/5*	0/10*	0/5*	0/5*
Vibration fatigue	60Hz 20G XYZ directions 3 times each						
Vibration frequency vibration	100 to 2,000Hz, 20G XYZ directions 3 times each						
Lead toughness	Bending durability 225g, 90°, 3 times for both sides	0/5	0/5	0/5	0/5	0/10	0/10
Solderability	230°C, 5sec., Rosin flux	0/5	0/5	0/5	0/5	0/10	0/10
Air-tighting	(1) Bubble leak 100°C, Fluorinert (2) He leak 5×10^{-7} atm cc/sec	0/100	0/100	0/100	0/300	–	0/50

* Series test

Table 3-35 Reliability result for laser diode

Fluctuation in characteristics	
Product	HLP5400
Test condition	Ta = 50°C, N_2 atmosphere with heatsink Po = 5mW APC
Failure checking standard	Fluctuation ratio in operational current $^{+50\%}_{-30\%}$
Failure mechanism	Nonradiative recombination current amplification
Result: Fluctuation in operation current from high temperature constant-light-emission tests is plotted. Stable operation is obtained even after 1,000 hr.	
Note 400 type: Open-air type	

Fluctuation in operational current (P_O = 5mW)



4. NOTES ON USING

4.1 MOUNTING ON A PRINTED CIRCUIT BOARD

Lead pins of packages are solder-coated or plated so as to be easily mounted on printed circuit boards. Normally, lead pins are soldered with eutectic solder. Typical mounting methods are explained below.

4.1.1 Mounting pin-insertion type packages

Pin-insertion package mounting consists of inserting lead pins of the package into the throughholes of about ϕ0.8mm on a printed circuit board and dipping them in the wave solder bath for soldering. This method can facilitate process up to solder immersion due to fixed lead pins, and realize automatic soldering easily. During soldering no wave solder should touch the package body. Solder touching might cause damage to the package.

4.1.2 Mounting surface mount packages

4.1.2.1 Basic mounting process flow

Fig. 4.1 flowcharts the basic process for mounting surface mount packages. First, soldering paste is applied to the footprint of a printed circuit board and an IC or LSI is placed on the board. Next, after the soldering paste dries, soldering is performed. Residual flux is then removed, followed by a visual inspection.

(1) Several types of solder pastes and fluxes are shown in Tables 4.1 and 4.2, respectively. To select a solder paste, composition, grain size, shape, flux content and viscosity should be considered to suit the application.

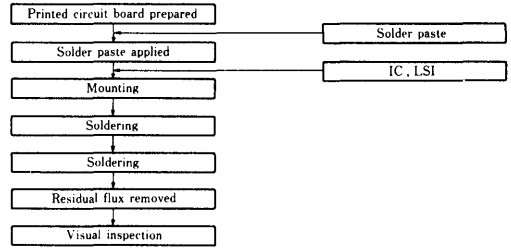


Fig. 4-1 Surface mount package mounting flow

Table 4-1 Typical Solder Paste Properties

Composition	Melting point	Grain size	Shape	Flux		Viscosity (at 25°C)	Remarks
				Content	Chlorine quantity		
Sn63/Pb37	183°C	250 mesh	Irregular Spherical	10Wt%	0.2Wt%	5×10^5 cp 3×10^5 cp	
Sn62/Pb36/Ag2	179°C	200 mesh	Spherical	15Wt%	0.2Wt%	2.5×10^5 cp	For Ag-soldered lead devices

Table 4-2 Types of Fluxes

I	Rosin-based flux 1 WW rosin (WW) 2 Activated rosin (RA) 3 Mild activated rosin (RMA)
II	Water-soluble flux (strongly activated mainly by organic acid)
III	Water-soluble rosin flux
IV	Synthetic rosin flux
V	Ester-based flux

(2) Application of solder paste

Solder paste is applied by screen printing or by discharge from a dispenser.
Screen printing . . . A screen is used as a mask, on which an appropriate amount of soldering paste is placed. Using a squeezer the thin screen is moved being pressed against the board surface to transfer or print the paste through the screen pattern onto the appropriate portion of the board surface.
Dispenser discharge technique . . . This technique involves discharging consistent quantities of solder paste through a needle by air pressure.

(3) Mounting

There are two ways of mounting a surface mount package on a board:
Vacuum pick-up and mechanical chuck. When a package is placed on a printed circuit board to fit the pattern of the package mounting area, it is roughly fixed by the flux's surface tension.

(4) Cleaning

Described in section 4.2.2.

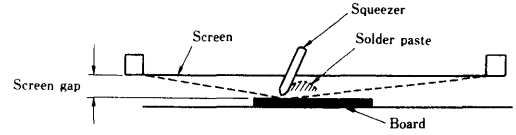


Fig. 4-2 Screen printing

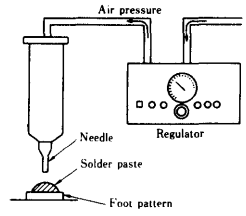


Fig. 4-3 Dispenser discharge

(5) Removal of residual flux

Any residual flux needs to be removed. Use a solvent such as alcohol, chloroethame or Freon. Note that for plastic packages, residual chlorine may deteriorate product reliability.

(6) Visual inspection

Soldered parts should be subjected to a visual inspection to insure good connection. Inspections by ultrasonic waves or laser are also available.

4.1.2 Soldering methods and their standard conditions

Main soldering methods for surface mount packages are shown in Table 4.3. These methods fall into two types: only the parts to be soldered are heated, or the entire device is heated.

Table 4-3 Methods for Soldering Surface Mount Packages

	Soldering method	Setup
Partial heat application	Iron	Soldering iron
	Pulse heater	Pulse current, Heater
	Hot air	Hot air blower
	Laser	Laser beam
Overall heat application	Infrared reflow	Infrared heater
	Vapor phase reflow	Cooling coil, Saturated vapor, Inert fluid, Heater
	Dipping	Wave solder (solder vessel for surface mounting)
	Furnace	Heater

(1) Infrared reflow soldering

Infrared light from a halogen lamp is concentrated using a reflecting mirror into a hot beam used for soldering. This method allows a large number of packages to be soldered at one time; it is suitable for high volume production. Reflow conditions depend on the package shape, board configuration and soldering equipment. Typical reflow conditions are shown in Fig. 4.4.

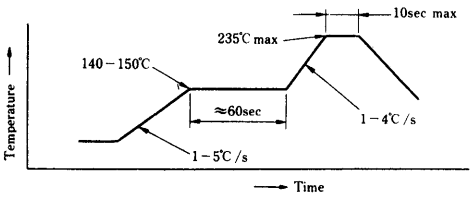


Fig. 4-4 Recommended reflow conditions

(2) Vapor phase reflow soldering

This technique utilizes the heat obtained from a fluorocarbon-type boiling point solvent. This method is advantageous in that soldering is performed independent of the device size and shape due to a constant temperature applied to the entire part (For example, 215°C for 3M company's Fluorinert FC5311). This feature reduces package damage caused by residuals on soldering parts and resulting uneven temperature. Examples of equipment and conditions are shown in Figs. 4.5 and 4.6, respectively.
The soldering methods described here are categorized with emphasis on thermal stress applied to parts and solderability, and do not consider productivity and cost.

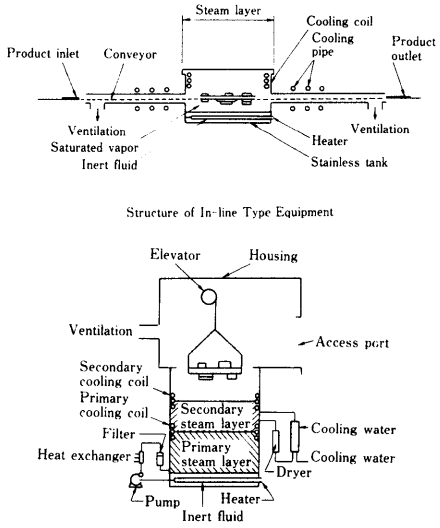


Fig. 4-5 Equipment for Vapor Phase Reflow Soldering (source: catalog from Japan Dynapart Co.)

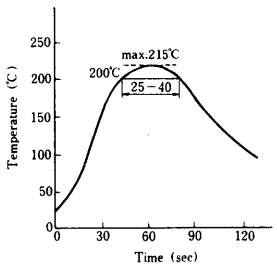


Fig. 4-6 Vapor phase reflow soldering conditions

4.3 APPLICABLE MOUNTING METHODS FOR EACH PACKAGE

Table 4.4 lists the applicable mounting methods for each package.

Table 4-4 Applicable Mounting Methods for Each Package

Mounting methods		IC/LSI packages					
		QFP	SOP	MSP	PLCC	FPG	LCC
Partial heat application	Iron soldering	O	O	O	O	O	X
	Pulse heater soldering	O	O	X	X	O	X
	Hot air soldering	O	O	O	O	O	O
	Laser soldering	O	O	O	O	O	X
Overall heat application	Infrared reflow soldering	O	O	O	O	O	O
	Vapor phase reflow soldering	O	O	O	O	O	O
	Dip-soldering	X	Note 1	O	X	X	X
	Furnace soldering	O	O	O	O	O	O

O : Applicable for mounting
X : Unapplicable for mounting
Note 1: Applicable for 20-pin or less SOPs, but unapplicable for 24- and 28-in SOPs.

4.2 NOTES ON DESIGNING CIRCUIT SYSTEMS

Reliable circuit systems can be designed considering the following:
Initial specifications are satisfied

- Design margin is insured considering characteristics variations.
- Derating is applied.

Other considerations for achieving reliable circuits include wiring related problems, extraneous surge voltage, reactance loading, noise margin, and area of safety operation (A.S.O), reverse bias fly-back pulse, static electricity and pulse stress.

4.2.1 General precautions

Reliable system design is examined for two cases below :

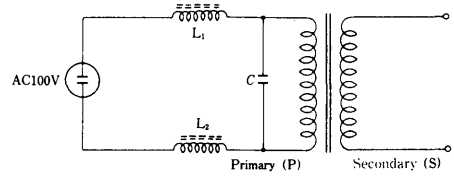
- A device is used in the range of specifications indicated in individual data sheets.
- A device is used in a special application such as digital ICs used in an analog circuit system (oscillator).

The former case allows derating based on parameters variations with time, used duty and temperature. Further, a failure rate can be predicted by simplified environmental factors.
The latter case includes applications such as TTLs driving loading capacitors or LEDs, or cases in which outputs are shorted. The following points should generally be noted when designing these systems.

(1) Ambient temperature should be kept as low as possible to keep semiconductor devices from becoming overheated.
(2) Supply voltages, input voltages and power dissipation should be maintained within rated values, considering derating.
(3) Excessive voltages caused by noise must not be applied to inputs/outputs and power supply pins.
(4) Plastic encapsulated semiconductor devices must be shielded from high electric fields. Devices exposed to a high electric field can cause polarization of plastic and the passivation film, which might result in malfunctions.
(5) No static electricity should appear during use.
(6) Since high speed devices employ fine processing, electrostatic pulses should be prevented by providing a protection circuit at the input stage.
(7) When turning power on/off, voltage must be applied constantly. If a voltage is applied to input and power supply pins with ground pins floated, excessive stress can be applied.
The above considerations are described using the following examples.

4.2.2 Noise and surge preventions

Surge voltage static electricity and noise are problems common to semiconductor devices.
Generally, electric devices are designed considering commercial power supply variations of about 10%. However, if devices are used near a machine generating a surge voltage, this surge can be superimposed on the power supply line causing malfunctions. Thunder may also induce an impulsive surge. This surge can be reduced by providing a filter as shown in Fig. 4-7 on the AC line.



$L_1 = L_2 = 2 - 10\text{mH}$, $C = 0.1 - 0.5\mu\text{H}$

Fig. 4-7 Surge absorber

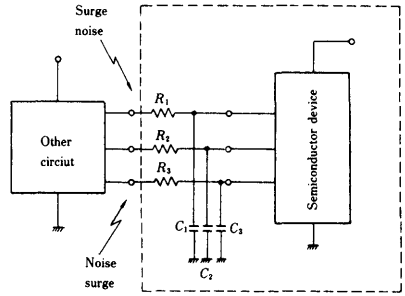
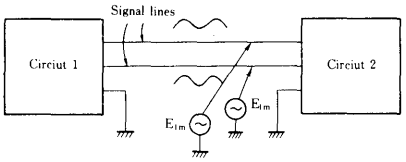


Fig. 4-21 Surge protection circuit

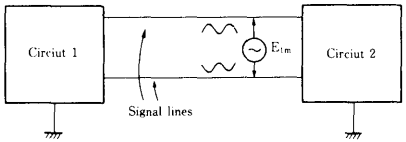
If surge or static electricity can possibly be directly applied to the semiconductor devices and other components on a board (not from the AC line), the device must be shielded. In this case, the impedance between the shield and ground must be low.
If there is a possibility of static electricity or surge pulses applied as noise, a protection circuit as shown in Fig. 4-8 is recommended. Time constants Ri and Ci should be determined so that surge pulses can be effectively absorbed without affecting device operation.

4.2.2.1 Types of noise

Noise is generated between earth and signal lines, or induced between signal lines (Fig. 4-9). The above cases have different effects on devices and require individual prevention techniques.



(a) Noise generated between grounds and signal



(b) Noise generated between signal lines

Fig. 4-9 Noise generation

4.2.2.2 Noise source and signal line coupling

Noise and signal line coupling is caused by:
(1) Conduction – leakage impedance exists between a noise source and signal lines
(2) Electrostatic induction – electrostatic coupling between a noise line and a signal line
(3) Electromagnetic induction – mutual conductance between a signal source and signal lines

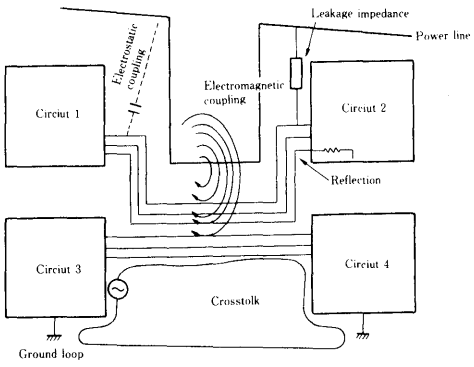


Fig. 4-10 Noise source and signal line coupling

(4) Cross talk – when two or more lines exist adjacently, electrostatic and electromagnetic induction cause one line to induce noise voltage on the other line.
(5) Ground loop – When both ends of a signal line are grounded, the potential difference between the two may cause noise.
(6) Reflection – Reflection caused by signal line impedance mismatching produces noise.
These couplings are illustrated in Fig. 4-10.

4.2.2.3 Countermeasures against noise

To construct a system which is not plagued by noise, the following should be considered.
- Eliminate or reduce the noise
- Pick up no noise
- Increase the noise margin
- Provide a compensation circuit

(1) Noise source

The most effective means of noise prevention is to control noise sources as described below.
- Insert diodes, resistors or capacitors in parallel into a relay coil to reduce surge voltage.
- Install a filter on the AC power line to prevent noise through the AC line.
- Shield equipment producing strong electric fields: these precautions eliminate the need for protecting the entire system from receiving noise. Another precaution is to place the device away from the noise source.

(2) Ground lines

Ground lines for circuits should be exclusively used and not commonly used with other ground systems to remove interference caused by currents flowing to ground. There must be only one connection and no closed loop between circuit systems and the frame (Fig. 4-11).

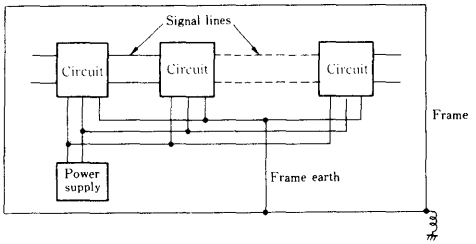
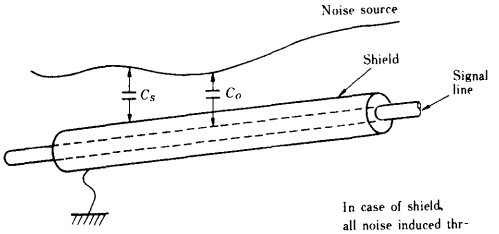


Fig. 4-11 Grounding of a circuit system

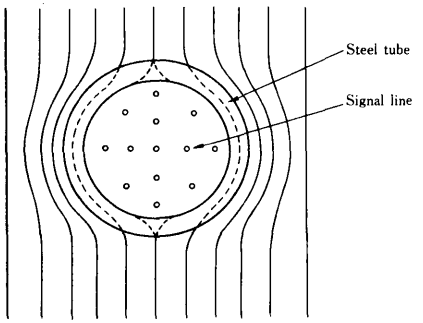
(3) Shields

It is recommended that signal lines or the entire system be shielded to reduce extraneous noise effects. A bond should be used to prevent noise due to electrostatic coupling. This permits noise on signal lines to be induced on the shield line and then to be bypassed to earth if there are no shields. The internal magnetic field of a system placed under a strong magnetic field can be attenuated by covering the system using magnetic material (Fig. 4-12). Steel tubes are usually used for the shield. Magnetic permeability materials are not employed due to their high price.



In case of shield, all noise induced through C_O is grounded via C_S.

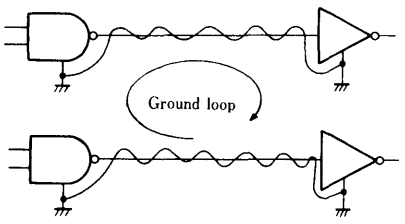
(a) Electrostatic shield



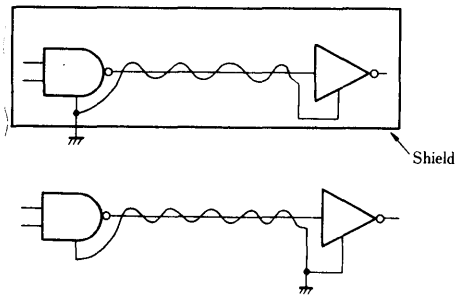
(b) Magnetic shield

Fig. 4-12 Shield example

Another shield type commonly used is twisted pair lines. Noise can be reduced by placing two signal lines symmetrically between receiver circuits, signal sources, ground and noise sources. Extraneous noise can be suppressed by reducing the twist pitch of signal lines in proportion to transmission distance. Further, if a shield is provided, protection against electromagnetic induction can also be obtained. Twisted pair lines may produce a ground loop, but this can be eliminated in the manner shown in Fig. 4-13.



(a) Ground loop is produced (bad example)



(b) No ground loop is produced (good example)

Fig. 4-13 Twisted pair line system

(4) Filters

Most power supply related noise originates from the AC line. This noise can be reduced by installing an AC line filter into the noise generating side or circuit system's AC supply side, which was illustrated in Fig. 4-7. Fig. 4-14 shows an example of the use of a switching regulator. This example reportedly accomplishes a noise voltage reduction of 0.3 to 20 MHz and approximately 20 dB.

From the point of view of circuit systems, power supply impedance should be lowered as much as possible. This can be achieved by placing capacitors at appropriate places on the power supply lines. In this case, it is desired to place in parallel a large capacitor as a bypass for lower frequencies and a small capacitor for higher frequencies.

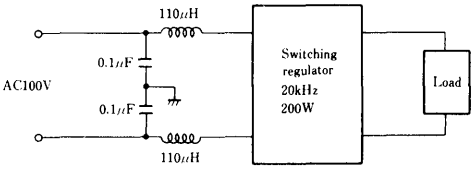
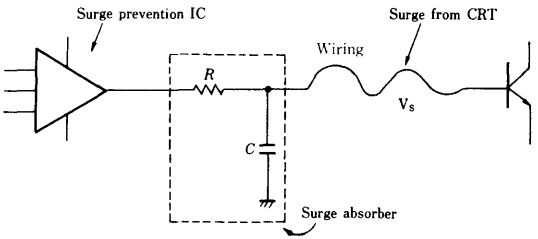


Fig. 4-14 AC line filter

4.2.2.4 Countermeasures against surge

For preventing voltage surges, surge incoming pins and paths should be determined and the following measures taken.

Surge voltage may be generated due to discharge when high voltage circuits are placed adjacent to each other such as when ICs and a CRT are incorporated in the same system. Various types of protection circuits against surge can be provided for an IC pin as shown in Figs. 4-15 to 4-17. Reliability improvement depends heavily on how much a surge voltage can be reduced. Fig. 4-15 illustrates a protection circuit placed at the output stage consisting of a capacitor and a resistor to reduce the surge induced on lead lines. Fig. 4-16 is a protection circuit placed at the input of a transistor used for a high frequency circuit. This circuit proves to be effective based on failure data from the field.



V_S : Surge voltage induced to wiring

Fig. 4-15 Absorber against surge from CRT

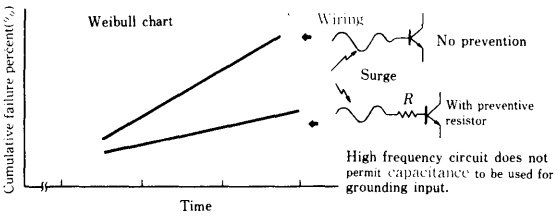


Fig. 4-16 Surge prevention for high frequency transistors

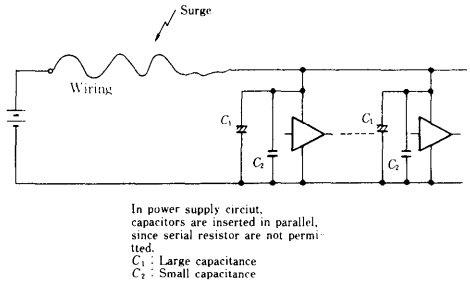


Fig. 4-17 Power line surge absorbtion

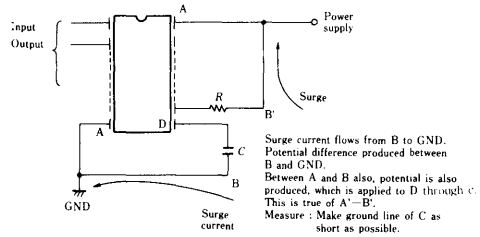


Fig. 4-18 Power line incoming surge prevention

Power supply lines at the same potential may induce a surge, producing a potential which may cause malfunction or destruction. In Fig. 4-18, surge produces potential between points A and B which were at the same potential. This surge can be prevented by employing a layout, wiring system and ground configuration that do not induce surge, or by providing a shield.

4.2.3 Characteristics parameters and reliability

Characteristic parameters of semiconductor devices are specified according to each device functions and application. The importance of each parameter depends on the application. For key parameters and ones having stringent system specifications, initial characteristic variation should be considered in designing systems and derating should be conducted. Since parameter variation is usually small under actual use, initial characteristic specifications may be used for most designs.

Parameters should be considered in terms of:

(1) The importance of the parameter: Is the parameter directly related to failures?
(2) Initial margin value of the parameter
(3) Whether parameter varies with age or not: is the variation in the direction having sufficient margin?
(4) Whether the margin permits the use of other devices or not.
(5) Whether redundant design is possible or not.
(6) Whether a statistical technique can be applied to the parameter design or not?

4.3 CHARACTERISTIC EVALUATION SOCKETS

4.3.1 Notes on handling sockets

(1) The lead spacing of the DIP except for the side brazed ceramic DIP is wider than standard ones of 300, 400, 600 and 900 mil. Therefore, you may have difficulty in inserting an IC in a socket since the lead tips do not match the socket taps. An appropriate jig should be used to insert and in particular to remove ICs.
(2) When soldering an IC inserted in a socket, an iron with high insulating resistance should be used; care should be taken so as to damage the IC by leakage current from the soldering iron.
(3) Use the IC socket within a heat resistance temperature of 125°C.

4.3.2 Socket purchasing

For details on each socket and their purchasing, please contact the agencies below.

(1) Yamaichi Denki Kogyo
Tel: 03(756)1191
(2) AUGAT
Tel 03(244)3788
(3) TEXTOOL
Tel: 044(711) 0022
(4) PLASTRONICS
Tel: 044(711)0022
(5) General Bussan
Tel. 03(383)1711

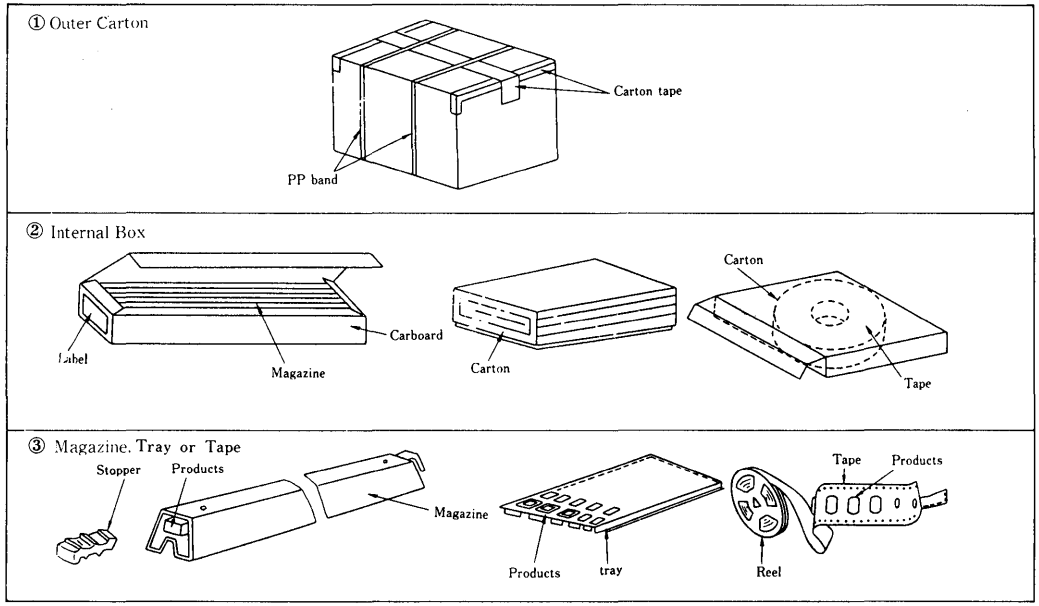
4.4 PACKAGE PACKING FORM

4.4.1 Unpacking cartons

LSIs are packed in magazines or trays in an internal box which is placed in an outer box as shown below. Unpack in the following order ① outer carton ② internal box. ③ magazine or tray. Be careful not to damage packages when unpacking from magazines, though the magazines or trays are designed to resist damage during shipment.

4.4.2 Precautions in handling magazines

(1) Outer cartons must not be subjected to any physical damage such as dropping.
(2) Magazines should be kept away from any water leakage. Do not leave them outdoors or store them under high temperature or humidity.
(3) Special care should be taken when handling the internal box. Dropping may jar the stopper causing devices to fall out of the magazine, resulting in deformed leads. Ceramic packages, if dropped, can be cracked, causing leakage failure.
(4) Though antistatic treatment is provided over the surface of transparent chloroethylene magazines, the following precautions should be taken:



① Adsorption of moisture removes the antistatic additives losing their effect.

② High temperature and high humidity make magazines sticky.

③ Storage period should not exceed six months, as antistatic additives deteriorate with time.

④ The transparent magazine with a surface resistance of less than $1 \times 10^{10}\ \Omega/\square$ is inferior to the black magazine with a resistance of less than $1 \times 10^{6}\ \Omega/\square$.

4.5 NOTES ON USING CODEC LSIs

– Latch up protection –

Since all Hitachi CODEC LSIs employ CMOS structure, general latch up protection is useful. In particular, the following protection procedures should be considered when using CODEC devices.

Latch up: A thristor phenomenon caused by parastic pnp or npn transistors unique in CMOS structure.

A CODEC has four power supply pins: AGND, DGND, V_{DD} and V_{SS}. Power should be applied to these pins in proper order. Voltage exceeding the absolute maximum rating may cause damage to the device.

4.5.1 Notes on inserting mounting boards

Special care should be taken when inserting or replacing a CODEC-mounted board with the system powered on. When the usual slow-starter power supply is turned on, voltages at each part of the board change slowly. Accordingly, a reverse current seldom exceeds the maximum rating. On the other hand, when a mounting board is inserted with the power on, a rapid voltage change can occur. This might cause element destruction, thermally disconnecting V_{DD} or V_{SS} on the device. In the case of V_{DD} disconnection, substrate bias is derived from I/O pins because of its CMOS characteristics resulting in unstable operation with the S/N ratio reduced. Thus, 'hot line insertion' is not recommended from the standpoint of reliability. If this is unavoidably required, the following must be considered.

Hitachi CODEC HD44230 and 240 series incorporate an inverse potential prevention circuit to prevent V_{SS} pin voltage from rising. This circuit can effectively prevent element destruction caused through hot line insertion. During power up sequence where a +5V V_{DD} pin is set up first, part of the negative supply current is dissipated to temporary activate the prevention circuit. Thus, ensure that the current capacity is high enough to set up the transition at power up.

When power must be applied to a large number of lines, the current capacity margin must set up a –5V at V_{SS} pin. After the power up sequence is completed, the current flowing in the prevention circuit is cut off. Accordingly, the current of rated input voltage is specified as a supply current in individual data sheets. In Hitachi CODECs, a sufficient current capacity is preserved at the negative power set up by simultaneously setting up two different types of slow-starter power supplies or by first setting up a –5V V_{SS} pin.

4.5.1.1 DGND and AGND connection on a mounting board

It is usually recommended that bypass capacitors are inserted between DGND and V_{DD} and between AGND and V_{SS}. However, CMOS structure is also formed between DGND and V_{DD}. If DGND and AGND are connected separately on a board, the impedance between V_{DD} and DGND becomes higher, which increases the possibility of latch up generated by noise during power up. The best way to prevent this is to connect DGND and V_{DD} pins together just before the CODEC. If the two lines are separately traced, they can be connected together just before the socket.

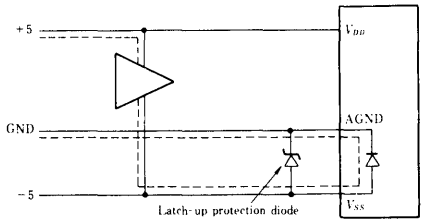


Fig. 4-19 Latch-up protection diode

4.5.1.2 Insertion of diodes against inverse voltage

If elements such as resistors and operational amps are inserted between V_{DD} and V_{SS}, current flows in the path of V_{DD}-V_{SS}-AGND/DGND through parastic diodes in the CODEC (Fig. 4-19). For eliminating this current, it is recommended that a diode such as a Shottky type be placed to suppress the voltage between AGND and V_{SS} to under 0.5V. The current capacity of the diode should be determined based on the amount of flowing from external circuits.

4.5.1.3 Currents flowing from other power supplies

Power supplies available on the CODEC board include ±12V, ±15V and –48V. These supplies may overdrive the +5V CODEC I/O pins. Usually, the current flowing through devices are not large enough to cause latch up, but care should be taken.

4.5.1.4 Bypass capacitors

When bypass capacitors are inserted between different power supplies, the potential may be inversed temporarily depending on the order in which the supplies are on. The following phenomenon can occur: 1) with capacitors placed between V_{DD}, V_{SS} and AGND pins, when V_{DD} and GND are powered with V_{SS} open, V_{SS} potential will rise to V_{DD} x C2/(C1 + C2), which may raise V_{SS} to a positive potential; actually, however, a fairly large capacity is required for potential inversion; and 2) in such an application that a –48V is applied with GND open, the GND potential may be pulled up to –48V and exceed V_{SS} (–5V).
The more power supplies are used, the more cases of inverse potential should be considered. Inverse potential can be prevented by providing larger bypass capacitors between V_{DD}-GND (=AGND=DGND) and between GND – V_{SS}.

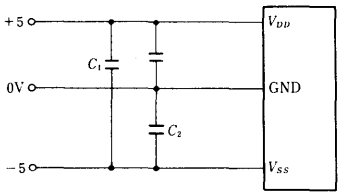


Fig. 4-20

4.5.2 Notes on inserting the CODEC into a socket

Power should be turned off before the CODEC is inserted into a socket. Insertion with power on may destroy the CODEC because the bypass capacitors have no effect.

4.5.3 Connection with a transformer, coil, etc.

Special care should be taken for connecting a transformer for a speech circuit with the CODEC. A voltage beyond the power supply voltage may be applied to the inputs when:

- rush currents are caused by intermittent currents through a telephone circuit.
- thunder surge leakage exist between coils.

and

- substrate potential has risen.

The circuit of Fig. 4-21 can be effectively used to prevent this problem. The peak voltage can be suppressed by a filter consisting of R1 and C (floating capacitance only is sufficient) and clamped by diodes. This prevents AOUT or AIN from being overdriven. Most cases does not require R2.
When long lines are connected to CODEC pins such as a microphone input and earphone output, these pins should be prevented from noise such as external spikes. When piezo elements are used for the microphone and earphone pins, these pins should also be prevented from the piezo effect when stress is applied.

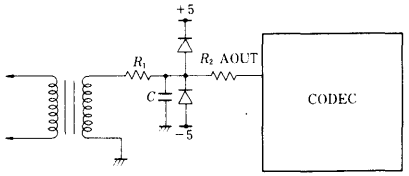


Fig. 4-21 Surge prevention circuit

4.5.4 Digital output

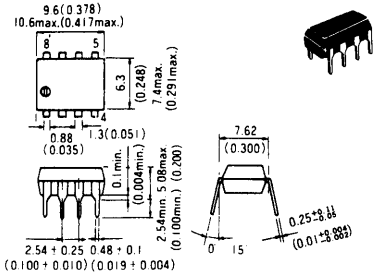
Digital output pins employ open drain structure, but its substrate (WELL) is connected to DGND. Accordingly, voltages below DGND (0V) at these pins may cause latch up. Additionally, loading capacitance and transmission reflection effects should be considered. Since a diode is provided between V_{DD} and digital outputs, pull up voltage must not exceed V_{DD}.

Package Information

■ Plastic DIP

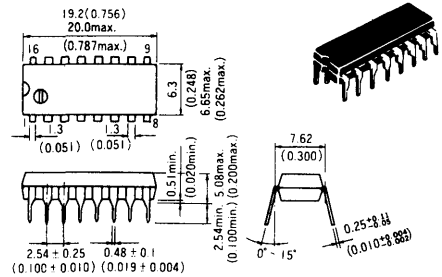
Unit: mm (inch), Scale: 1/1

DP-8



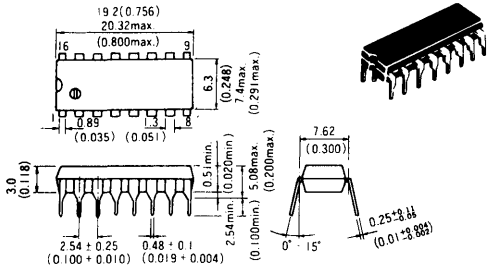
Hitachi Code	DP-8
EIAJ	SC-504-8C
JEDEC	MO-001AN

DP-16



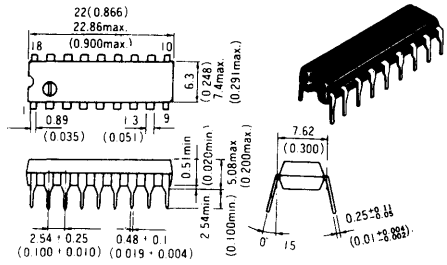
Hitachi Code	DP-16
EIAJ	SC-503-16A
JEDEC	MO-001AP

DP-16A



Hitachi Code	DP-16A
EIAJ	SC-503-16A
JEDEC	MO-001AP

DP-18



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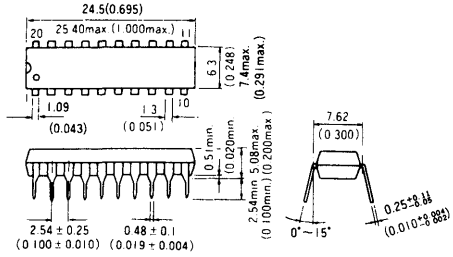
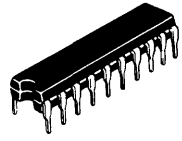
EIAJ	SC-505-18A
JEDEC	—

DP-20N

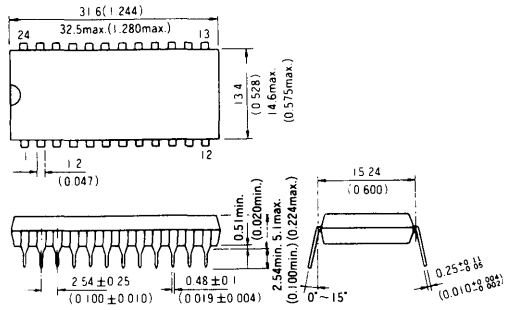


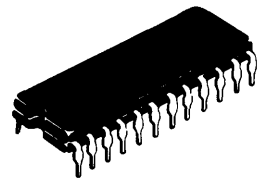


Hitachi Code	DP-20N
EIAJ	SC-541-20A
JEDEC	—

1

DP-24





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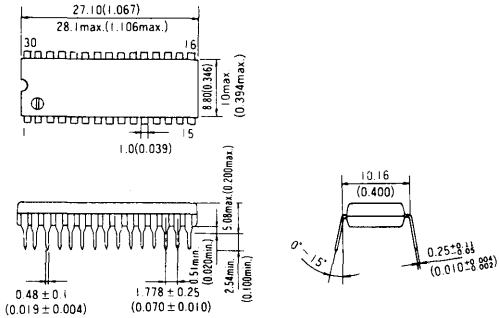
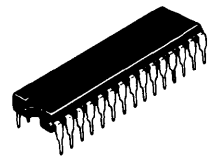
EIAJ	SC-509-24E
JEDEC	MO-015-AA

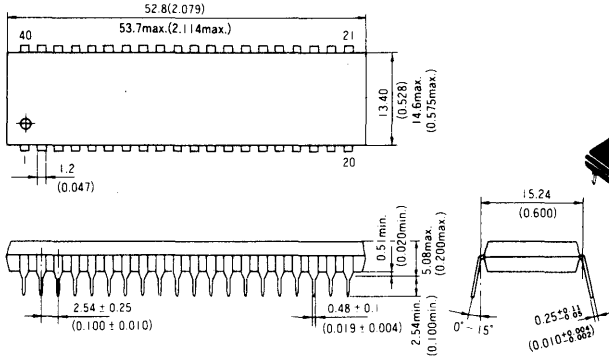
DP-30S

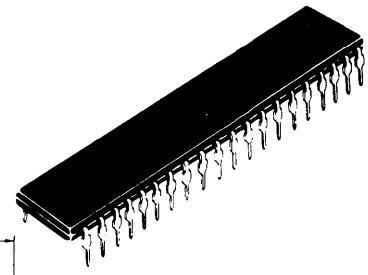




Hitachi Code	DP-30S
EIAJ	SC-549-30
JEDEC	——

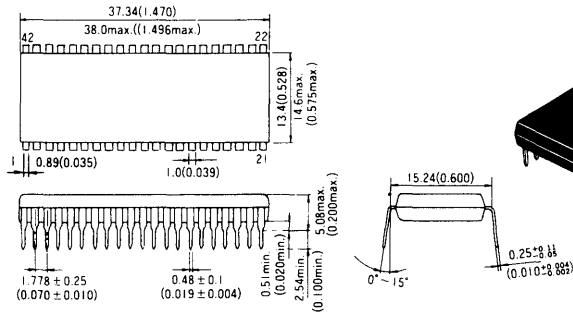
DP-40

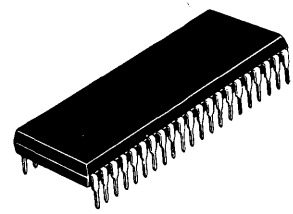




Hitachi Code	DP-40
EIAJ	SC-511-40D
JEDEC	MO-015J

DP-42SA

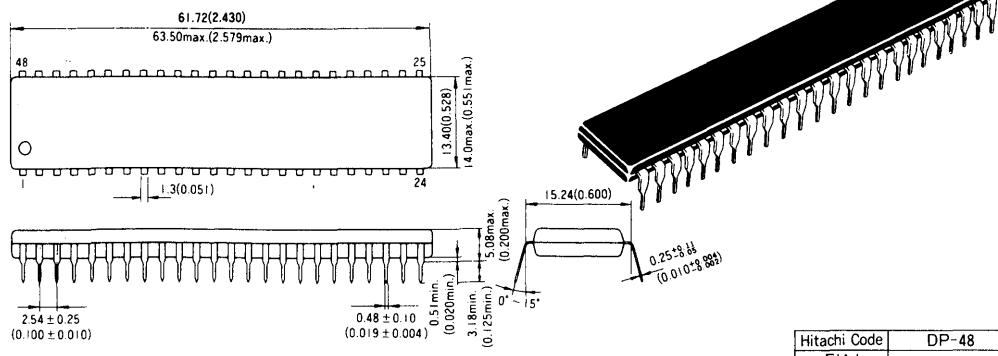




Hitachi Code	DP-42SA
EIAJ	SC-551-42
JEDEC	——

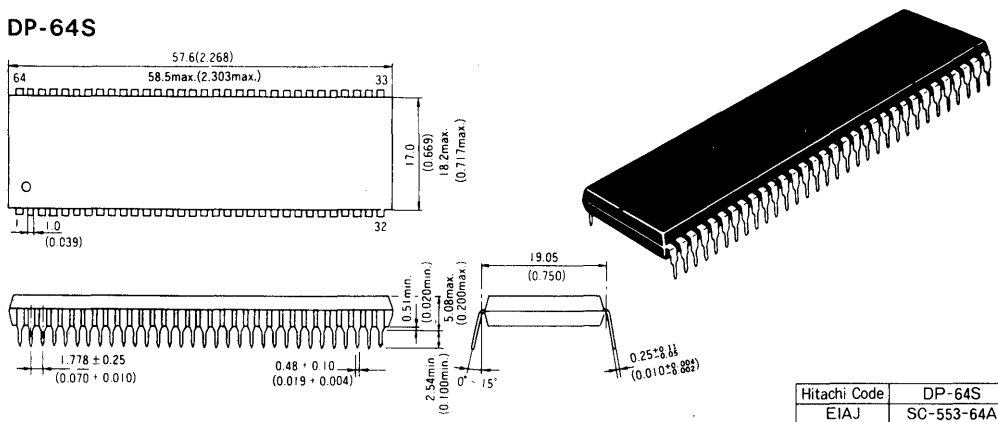
Unit: mm (inch) scale: 1/1

DP-48



Hitachi Code	DP-48
EIAJ	——
JEDEC	——

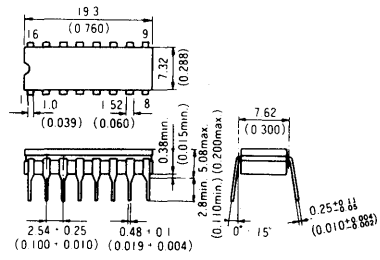
DP-64S

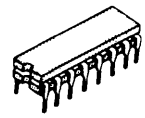


Hitachi Code	DP-64S
EIAJ	SC-553-64A
JEDEC	——

■ Cerdip

DG-16A



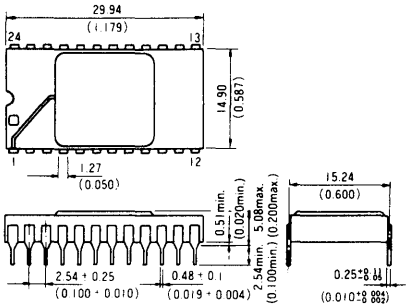


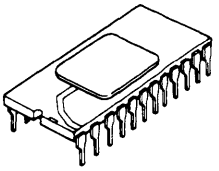
Hitachi Code	DG-16A
EIAJ	——
JEDEC	——

■ Ceramic DIP

Unit: mm (inch), scale: 1/1

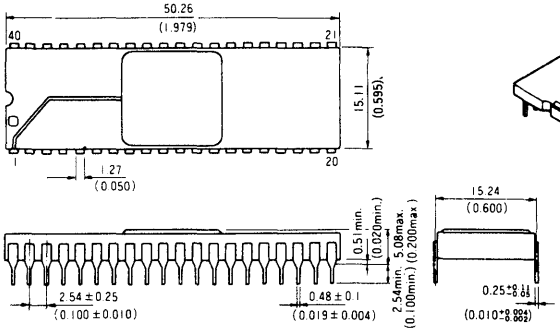
DC-24

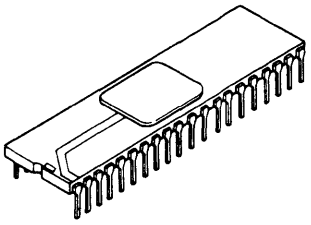




Hitachi Code	DC-24
EIAJ	——
JEDEC	——

DC-40



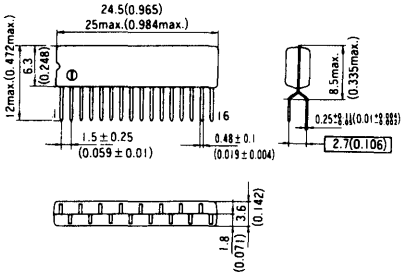


Hitachi Code	DC-40
EIAJ	——
JEDEC	——

■ Plastic SIP

Unit: mm (inch) scale: 1/1

SP-16

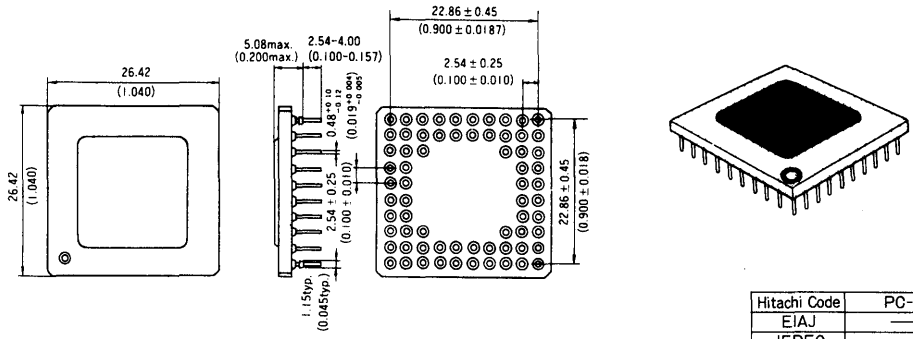


Hitachi Code	SP-16
EIAJ	——
JEDEC	——

■ **Pin Grid Array**

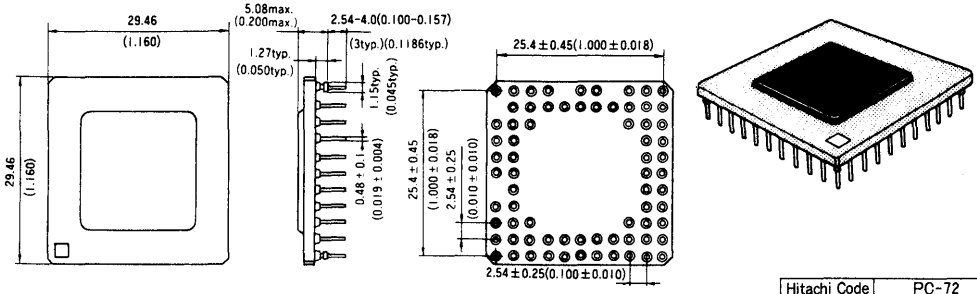
Unit: mm (inch), scale: 1/1

PC-68



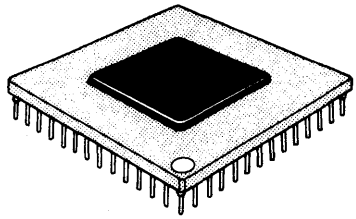
Hitachi Code	PC-68
EIAJ	—
JEDEC	—

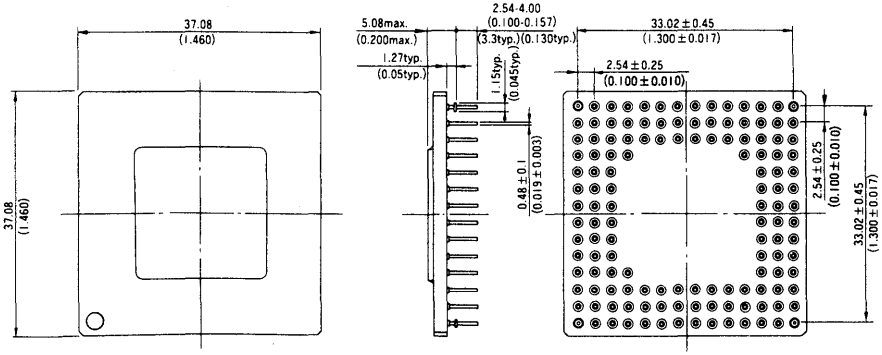
PC-72



Hitachi Code	PC-72
EIAJ	—
JEDEC	—

PC-135



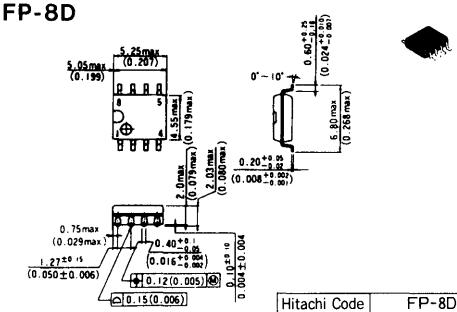


Hitachi Code	PC-135
EIAJ	—
JEDEC	—

■ Flat Package

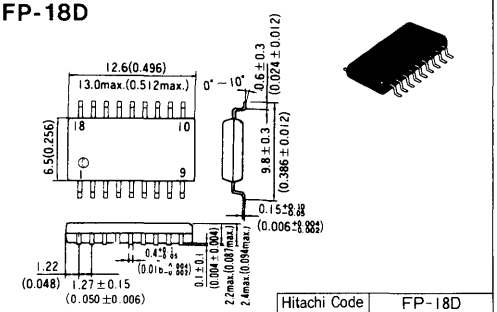
Unit. mm (inch) scale: 1⅛

FP-8D



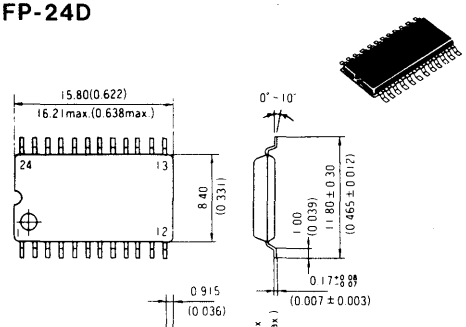
Hitachi Code	FP-8D
EIAJ	SC-527-8A
JEDEC	——

FP-18D



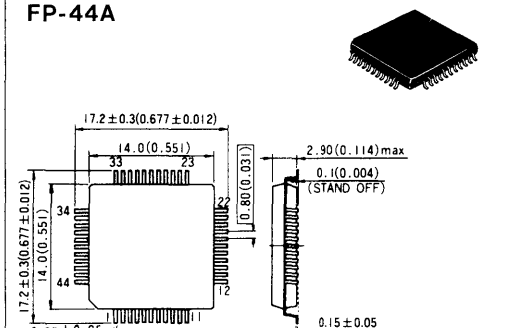
Hitachi Code	FP-18D
EIAJ	SC-556-18A
JEDEC	——

FP-24D



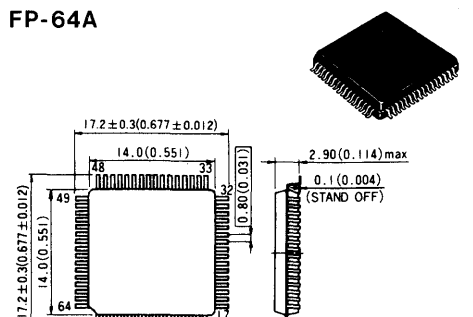
Hitachi Code	FP-24D
EIAJ	SC-532-24B
JEDEC	MO-059AA

FP-44A



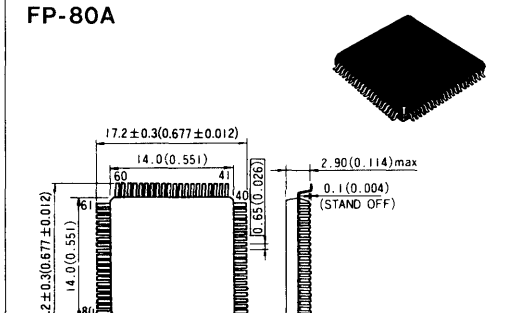
Hitachi Code	FP-44A
EIAJ	——
JEDEC	——

FP-64A



Hitachi Code	FP-64A
EIAJ	——
JEDEC	——

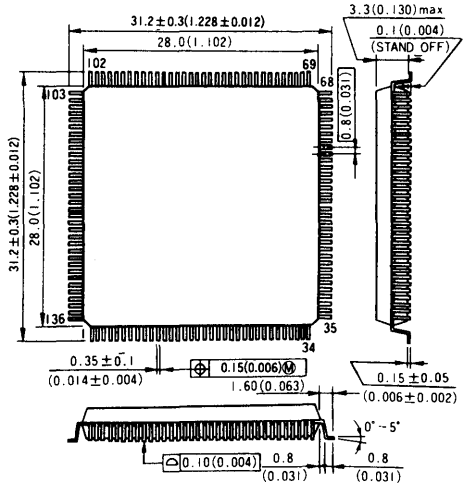
FP-80A

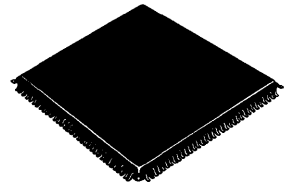


Hitachi Code	FP-80A
EIAJ	——
JEDEC	——

Unit: mm (inch), scale: 1½

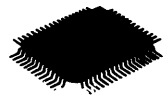
FP-136

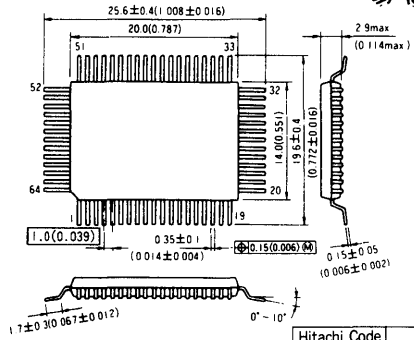




Hitachi Code	FP-136
EIAJ	—
JEDEC	—

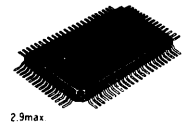
FP-64

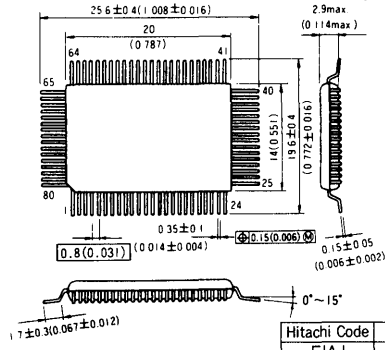




Hitachi Code	FP-64
EIAJ	—
JEDEC	—

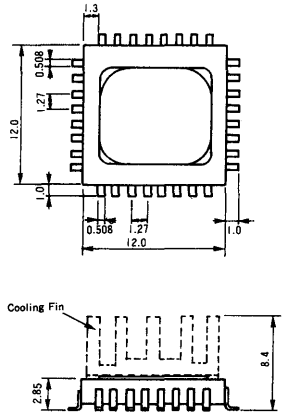
FP-80B





Hitachi Code	FP-80B
EIAJ	—
JEDEC	—

FG-32

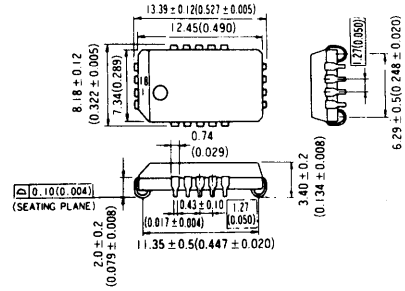


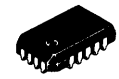
Hitachi Code	FG-32
EIAJ	—
JEDEC	—

■ **PLCC (QFJ)**

Unit: mm (inch), scale: 1½

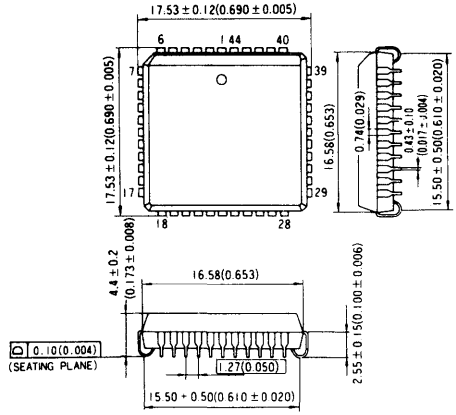
CP-18

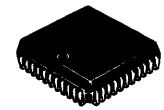




Hitachi Code	CP-18
EIAJ	——
JEDEC	MO-052AB

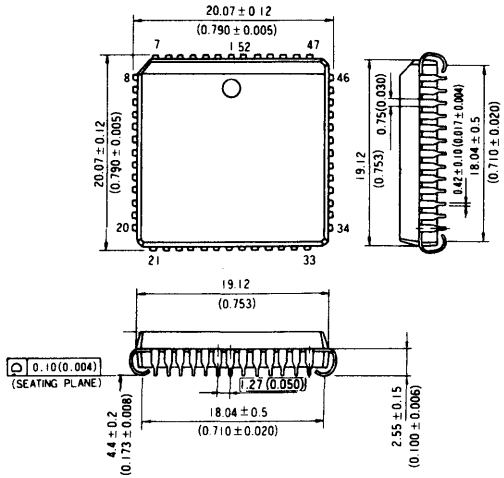
CP-44

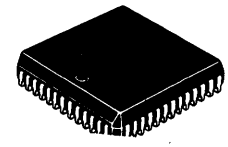




Hitachi Code	CP-44
EIAJ	——
JEDEC	MO-047AC

CP-52

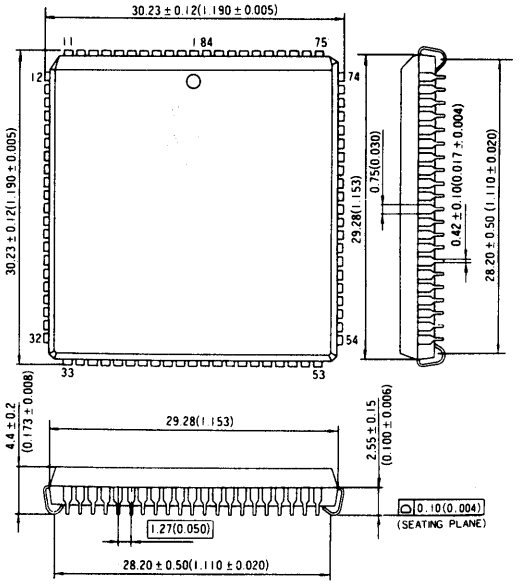


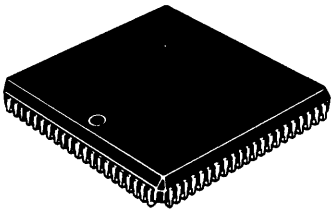


Hitachi Code	CP-52
EIAJ	——
JEDEC	MO-047AD

Unit: mm (inch), scale: 1½

CP-84

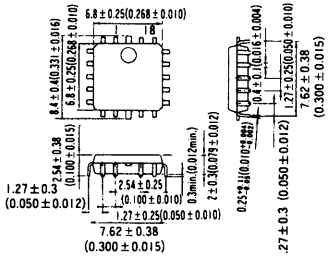




Hitachi Code	CP-84
EIAJ	—
JEDEC	MO-047AF

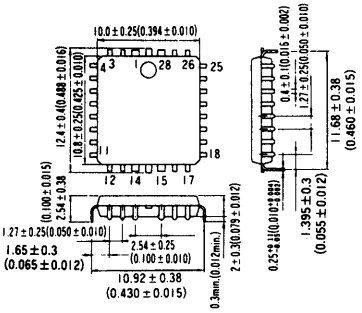
■ MSP

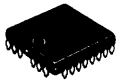
MP-18/18T



Hitachi Code	MP-18
EIAJ	—
JEDEC	—

MP-28

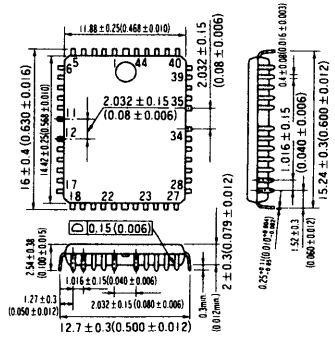


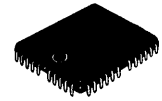


Hitachi Code	MP-28
EIAJ	—
JEDEC	—

Unit: mm (inch) scale: 1½

MP-44/44TA





Hitachi Code	MP-44
EIAJ	——
JEDEC	——

Section Two

Data Sheets

Devices for Telephone Applications

The absolute maximum ratings referenced in the data sheet sections of this manual are limiting values, to be applied individually and beyond which operation of the described circuits may be impaired. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the circuit's reliability.

The "Electrical Characteristics" of the circuits described in this manual are for reference only.

HA16802PS, HA16804PS, HA16805PS/F Series

Tone Ringer

■ DESCRIPTION

The HA16802, HA16804 and HA16805 are tone ringer monolithic IC's for telephone. These IC's have a built-in regulator power supply and produce electronic sound by directly driving external magnetic speaker or piezoelectric buzzer when call signal is detected. The HA16802, HA16804 and HA16805 each have different additional functions and control the functions by control terminal. (Type number: HD16805F)

HA16802PS/HA16804PS/
HA16805PS

(DP-8)

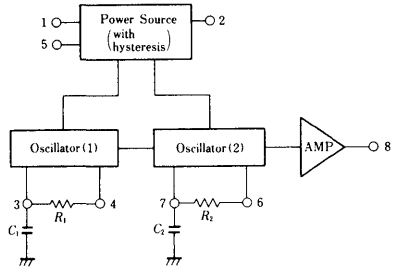
HA16805F

(FP-8D)

■ FEATURES

- Output frequency is variable.
- Low power dissipation.
- As it has a regulator power source with hysteresis, it can prevent a resonance which occurs in case of parallel connection (branch) of telephone.
- 2 levels of supply initiation voltage can be selected (HA16802PS).
- Supply initiation voltage is variable. (HA16804PS)
- Oscillation can be inhibited. (HA16804PS)
- Supply initiation current is variable. (HA16805PS/F)

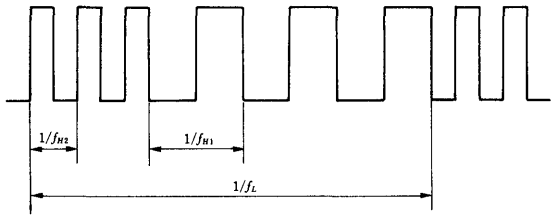
■BLOCK DIAGRAM



Note: R_1, R_2, C_1, C_2 are external parts

- Oscillator (1) operated at about 10 Hz (f_L) and modulates the frequency of Oscillator (2) at this cycle.
- Oscillator (2) operated at a high frequency and has two oscillation frequency; f_{H1}, f_{H2} by Oscillator (1).

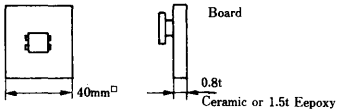
$$f_L = 1/1.25\ R_1C_1 \quad f_{H1} = 1/1.35\ R_2C_2 \quad f_{H2} = 1.24\ f_{H1}\ [Hz]$$



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	Vs	40	V
Output Current	Io	12	mA
Power Dissipation	P_T	625 (390)	mW*
Operating Temperature Range	Topr	−20 to +70	°C
Storage Temperature Range	Tstg	−55 to +125	°C

*P_T for HA16805F is 390 mW, the other 625 mW.
For HA16805F value at Ta ≦ 70°C, when Ta is more than 70°C, 7.14 mW/°C derating shall be performed. (Condition glass epoxy with 30% metallization density)



The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

■ELECTRICAL CHARACTERISTICS (Ta=25°C)

●HA16802PS

Item	Symbol	Condition	min.	typ.	max.	Unit	Remarks
Supply Initiation Voltage	Vsi	The contents within ( ) are the value at the time of changing (Trigger in=GND)	17 (21)	19 (23)	21 (25)	V	Selectable
Supply Initiation Current	Isi		0.6	1.2	2.5	mA	
Sustaining Voltage	Vsus		9	11	–	V	
Sustaining Current	Isus	Vs=15V	0.5	1.0	2.0	mA	
Output "H" Voltage	V_{OH}	Vs=24V, I_{OH}=−10mA	20	21.5	22.5	V	
Output "L" Voltage	V_{OL}	Vs=24V, I_{OL}=10mA	0	1.0	2.0	V	
Output Frequency	f_L	C_1=0.47μF, R_1=160kΩ	9.3	10.4	11.5	Hz	
	f_{H1}	C_2=6800pF	495	–	606	Hz	
	f_{H2}	R_2=200kΩ	610	–	752	Hz	

●HA16804PS

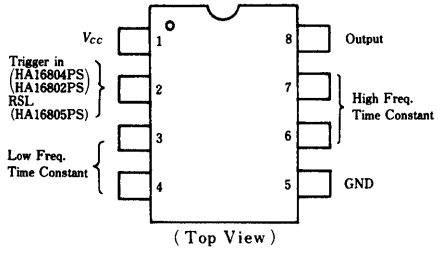
Item	Symbol	Condition	min.	typ.	max.	Unit
Supply Initiation Voltage	Vsi		17	19	21	V
Supply Initiation Current	Isi		1.5	3.1	6.2	mA
Sustaining Voltage	Vsus		9	11	–	V
Sustaining Current	Isus	Vs=15V	0.5	1.0	2.0	mA
Output "H" Voltage	V_{OH}	Vs=24V, I_{OH}=−10mA	20	21.5	22.5	V
Output "L" Voltage	V_{OL}	Vs=24V, I_{OL}=10mA	0	1.0	2.0	V
Output Frequency	f_L	C_1=0.47μF, R_1=160kΩ	9.3	10.4	11.5	Hz
	f_{H1}	C_2=6800pF	495	–	606	Hz
	f_{H2}	R_2=200kΩ	610	–	752	Hz

●HA16805PS/F

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply Initiation Voltage	Vsi	Connect with R_{SL}=20kΩ	26	28	30	V
Supply Initiation Current	Isi		0.7	1.5	3.0	mA
Sustaining Voltage	Vsus		9	11	–	V
Sustaining Current	Isus	Vs=15V, Connect with R_{SL}=20kΩ	0.5	1.0	2.0	mA
Output "H" Voltage	V_{OH}	Vs=36V, I_{OH}=−10mA	32	–	36	V
Output "L" Voltage	V_{OL}	Vs=36V, I_{OL}=10mA	0	1.0	2.0	V
Output Frequency	f_L	C_1=0.47μF, R_1=160kΩ	9.3	10.4	11.5	Hz
	f_{H1}	C_2=6800pF	495	–	606	Hz
	f_{H2}	R_2=200kΩ	610	–	752	Hz

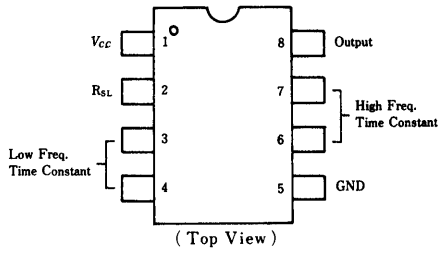
■PIN ARRANGEMENT

● HA16802PS, HA16804PS, HA16805PS



(Top View)

● HA16805F

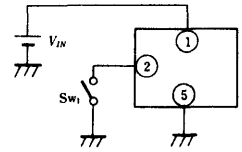
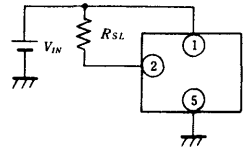
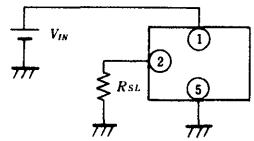


(Top View)

■PIN FUNCTION

Pin No.	Pin Name	Function	
1	Vcc	Positive Power Supply	
2	TRIGGER IN	HA16802PS HA16804PS	Shown below
	R_{SL}	HA16805PS/F	
3 4	LOW FREQ. TIME CONSTANT	Low Frequency Time Constant Setting	
5	GND	Negative Power Supply	
6 7	HIGH FREQ. TIME CONSTANT	High Frequency Time Constant Setting	
8	OUTPUT	Tone Output	

TRIGGER IN TERMINAL
R_{SL} } ② Pin Function Description

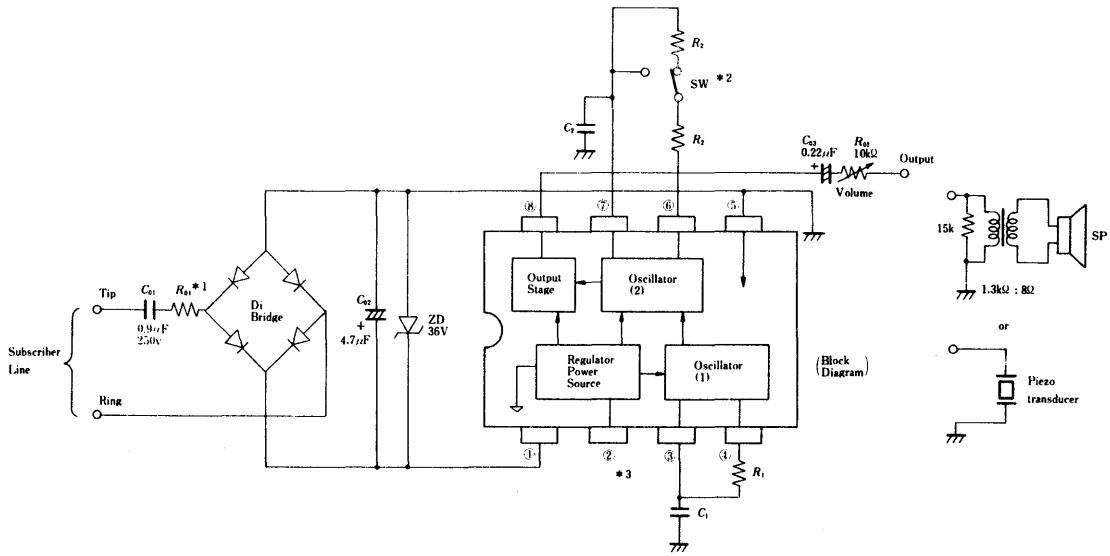
Type Name	Function	Description
HA16802PS	Supply Initiation Voltage Variable (Vsi)	
HA16804PS	Supply Initiation Voltage Variable	
HA16805PS/F	Supply Initiation Current Variable (Isi)	

② Pin Condition	Vsi
Open (Sel : OFF)	19V typ.
GND (Swl : ON)	23V typ.

R_{SL}	Vsi
Open	19V typ.
1MΩ	17V typ.
500kΩ	15V typ.

R_{SL}	Isi
6.3k	3.2mA typ.
13k	2mA typ.
20k	1.2mA typ.

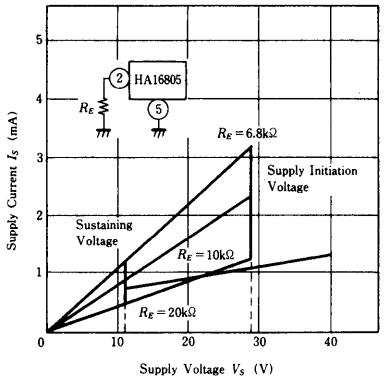
■APPLICATION



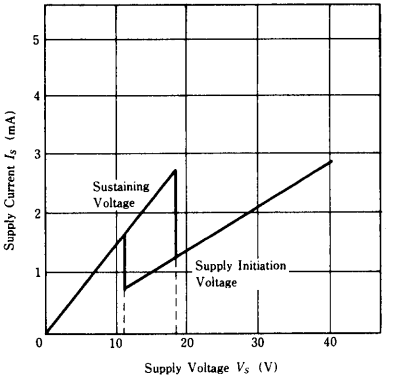
Note *1 HA16802PS, HA16805PS/F→10kΩ
HA16804PS → 2kΩ
*2 Possible timbre adjustment by changing the resistance value of R_2
*3 Additional function control terminal

Tone Ringer Application Circuit Example

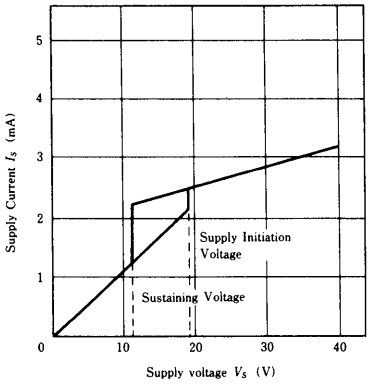
HA16805 Supply Voltage vs. Supply Current Characteristic.



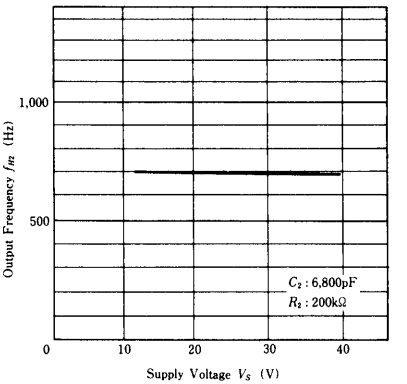
HA16804 (at Pin 2 Open) Supply Voltage vs. Supply Current Characteristic



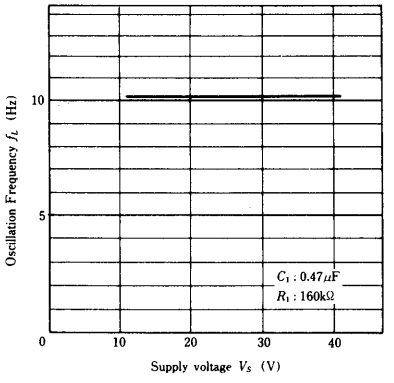
HA16802 (at Pin 2 Open) Supply Voltage vs. Supply Current Characteristic



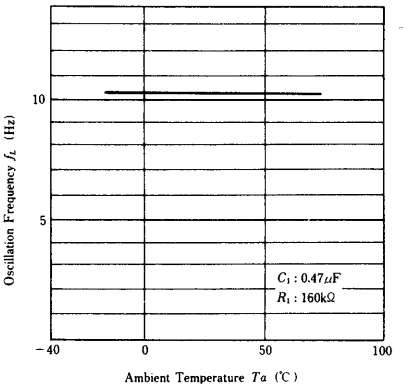
Output Frequency vs. Supply Voltage Characteristic



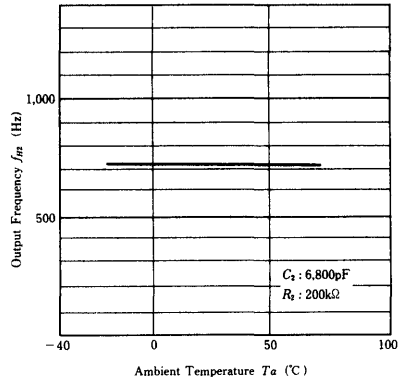
Oscillation Frequency vs. Supply Voltage Characteristic



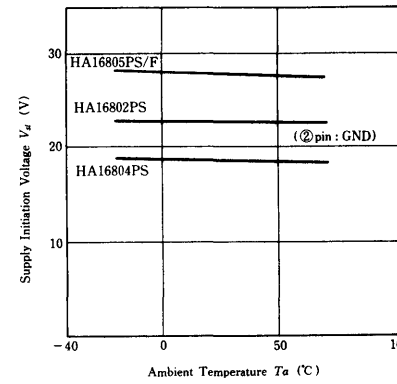
Oscillation Frequency vs. Ambient Temperature Characteristic



Output Frequency vs. Ambient Temperature Characteristic



Supply Initiation Voltage vs. Ambient Temperature Characteristic



2

HA16808ANT

Speech Network IC including Speaker Amp. for Telephone Set

Description

The HA16808ANT is a monolithic IC including speech network, tone ringer, and speaker amp. Therefore the telephone with speaker can be composed of HA16808ANT and dialer IC.

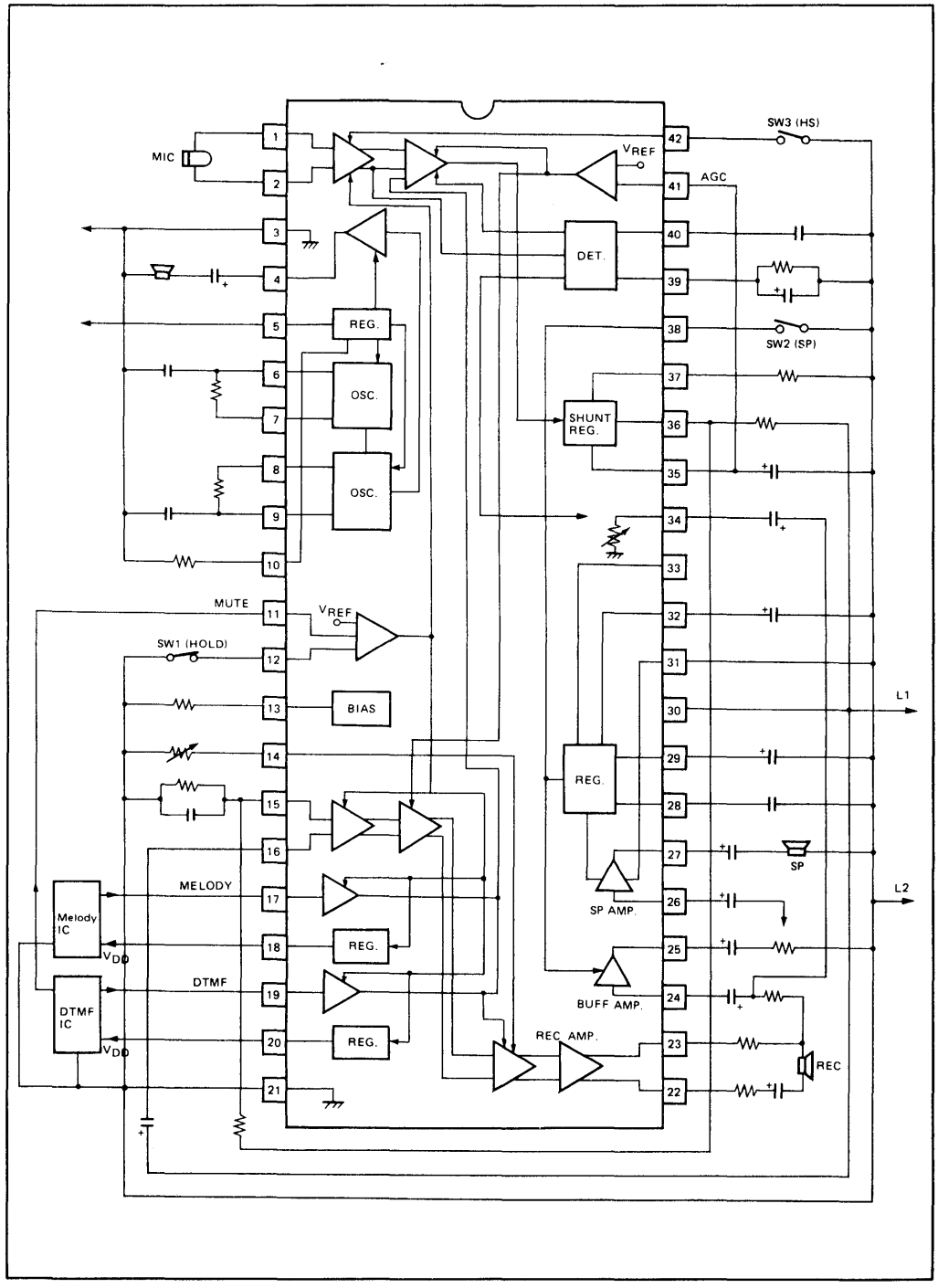
Features

- Low voltage operation ..... (1.8V)
- AGC according to the line current (Gains of sending, receiving, DTMF, and melody)
- Adjustable receiving gain by external resistor (0 to +10dB)
- Interface for DTMF (V_{DD}, MUTE, Sending amp. of DTMF signal)
- Interface for melody IC (V_{DD}, Sending amp. of melody signal)
- Noise suppression (No output for the input below noise level. The noise level can be controlled by external components.)
- Possible to dial under the on – hook condition (Included speaker amp.)
- Possible to receive by speaker (Also possible to send with handset in speaker mode.)
- At the time to send DTMF or melody, back-tone comes out from receiver or speaker.
- Variable oscillation freq. of ringer by external R, C.
- Variable supply initiation current.
- 42 pins shrink plastic DIP package (DP-42SA)

Pin Description

Pin No.	Symbol	Function	Function	Symbol	Pin No.
1	MIC 1	Mic. Input	Hook Switch	HS	42
2	MIC 2		AGC	AGC	41
3	GND	Tone Ringer	Voice SW Gain Adjustment (Noise Suppression)	VS3	40
4	OUTPUT				
5	V_{CC}		Decide the Suppression Level (Speaker Receive)	VS4	39
6	LOW FREQ.		On at Speaker Mode	SP SW	38
7	TIME CONSTANT		Detect the Line Current	ILDET	37
8	HIGH FREQ.		Bridge part 1	BRG1	36
9	TIME CONSTANT		Bridge part 2	BRG2	35
			Loss Pad on Speaker mode	ALC	34
10	R_{SL}		NC	NC	33
11	MUTE	DTMF Mode ($\geqq$ 1.6V)	Regulating Capacitor	BIPS	32
12	HOLD	On at Melody Mode	Speaker Amp. GND	GND 2	31
13	R_B	Decide IC Bias Current	Line	L1	30
14	GRCT	Adjust Receiving Gain	Speaker Part Regulator	V_{SP}	29
15	BRG3	Receiving Signal Input (one part of the bridge)	Compensating Capacitor	COMP1	28
16	BRG4		Speaker Amp. Output	SP OUT	27
17	MEL	Melody Input	Speaker Amp. Input	SP IN	26
18	V_{REF2}	Melody IC Supply Voltage	Buffer Amp. Output	BUFF OUT	25
19	DTMF	DTMF Input	Buffer Amp. Input	BUFF IN	24
20	V_{REF1}	DTMF IC Supply Voltage	Receiver Output	REC1	23
21	L2	Line (GND)		REC2	22

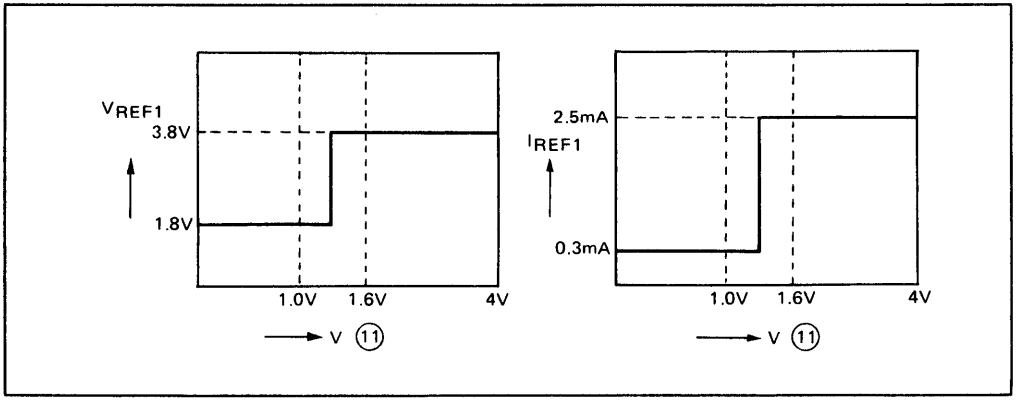
Block Diagram



Functional Description

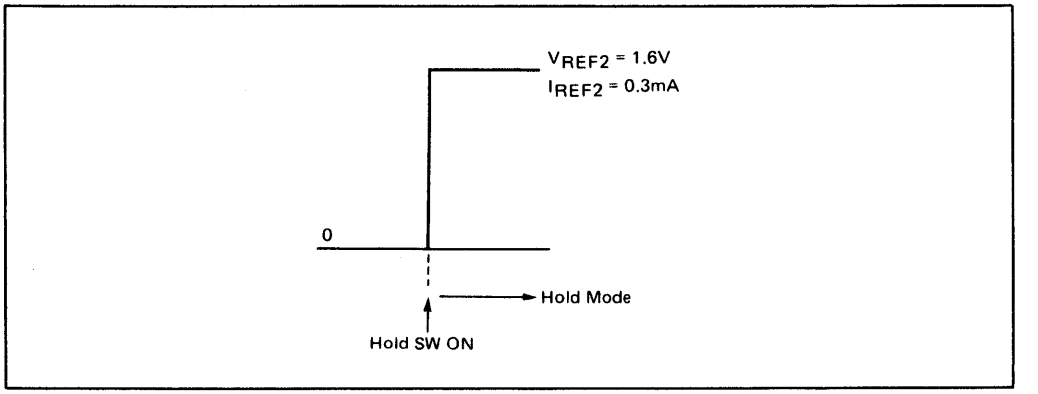
- **DTMF IF**

When 11 pin (MUTE) voltage V11 is 1.6V or more, IC becomes DTMF sending mode. (Threshold level is 1.3V typ). In this mode, the sending and receiving input amps are 'off' and DTMF sending amp. is 'on'.
Though DTMF signal is applied to 19 pin then, AC couple is needed (Cex16) because of bias of about 1V.
50 to 70mVrms input level is appropriate because the sending gain is a little over 20dB. As soon as DTMF signal is sent to line, backtone is produced from receiver. At speaker mode it is also from speaker. Also, DTMF IC supply voltage or current changes to V11 as figures.



- **Hold IF**

When 12 pin (HOLD) is connected to GND, IC becomes hold mode, and sending and receiving input amps are 'off', and melody sending amp. is 'on'. As the melody is applied to 17 pin, AC couple (Cex15) is needed because of bias of about 1V. 10 to 30mVrms input level is appropriate because of a little over 20dB.
As soon as the melody is sent to line, the backtone is produced from speaker. Then, the melody IC supply source becomes 'on' for the first time.

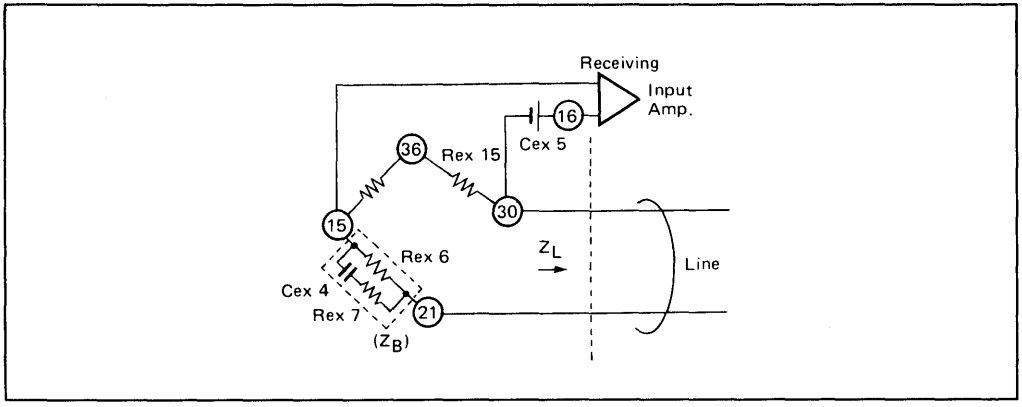


- **Circuit for suppression of sidetone**

The circuit for suppression of sidetone is constructed by resistance bridge. To control side tone Z_B is adjusted, in consideration of the line impedance Z_L.

$$\frac{Rex8}{Rex15} = \frac{Z_B}{Z_L}$$

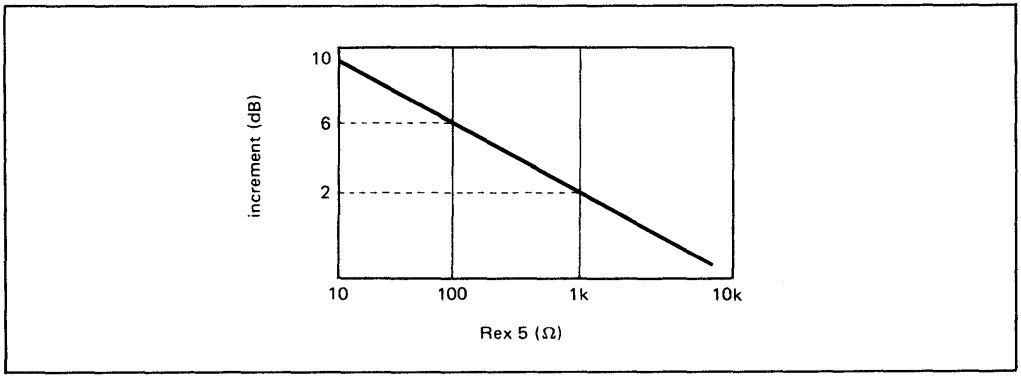
Cex5 is for AC couple.
When the resistance increases with keeping the ratio of Rex8/Rex15, the receiving gain increases. The receiving gain of Rex8/Rex15 = 330Ω/30Ω gets about 6dB larger than that of 110Ω/10Ω.



- **Receiving Gain Variable**

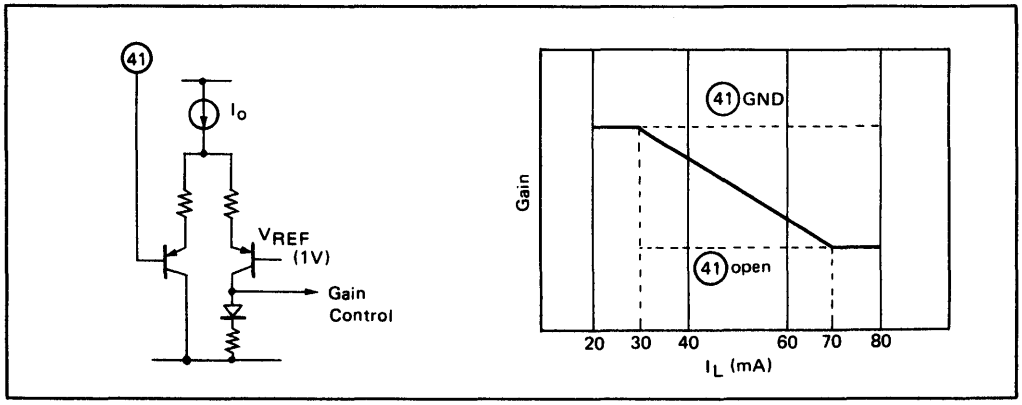
When the Rex5 decreases, the receiving gain increases while receiving (But Rex5≧560Ω). When Rex5 = 1kΩ to the condition of open of 14 pin, the receiving gain increases by about 8dB. Moreover, some modes are automatically 'off'.

Mode	Speaking		Dial (DTMF Sending)	Hold
	Hand Set	Speaker		
On ○	○	x	x	x
Off x				



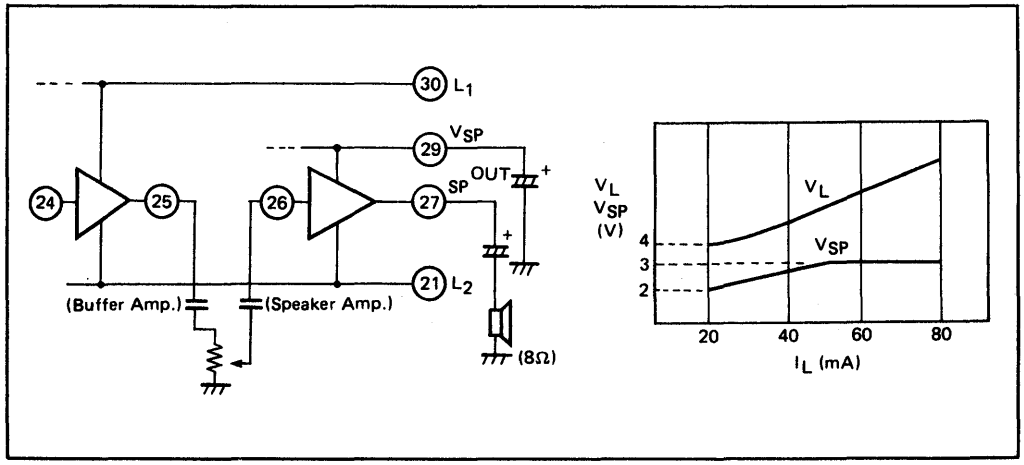
- **AGC Characteristics (Line Compensation)**

By connecting 41 pin with 35 pin, the sending and receiving gain, and the DTMF and Melody amp. are automatically adjusted to line current. When 41 pin applied voltage is fixed with apart-ing 41 pin from 35 pin, the gain becomes fixed,
High gain fix when $0V \leqq V41 \leqq 0.3V$
Low gain fix when V41 = V30 or open
In the case of $30mA \leqq I_L \leqq 70mA$, the gain changes.



- **Receiving by speaker**

When 38 pin (SPSW) is connected to GND, the IC becomes speaker mode, and in this mode, buffer–amp., speaker amp. and the regulator (Vsp) are 'on'. By inserting volume it is possible to adjust the volume of speaker output.
Voltage of Vsp changes the line current I_L and secures the dynamic range at line. (L1)
In $20mA \leqq I_L \leqq 50mA$, Vsp changes from 2V to 3V, in $I_L \geqq 50mA$ it keeps 3V. Also the line voltage is 1.5V higher than normal mode. (at $I_L = 20mA$).

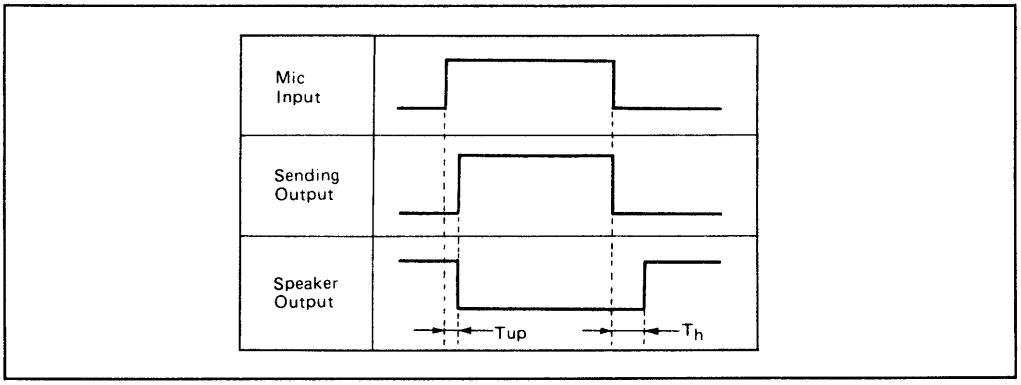


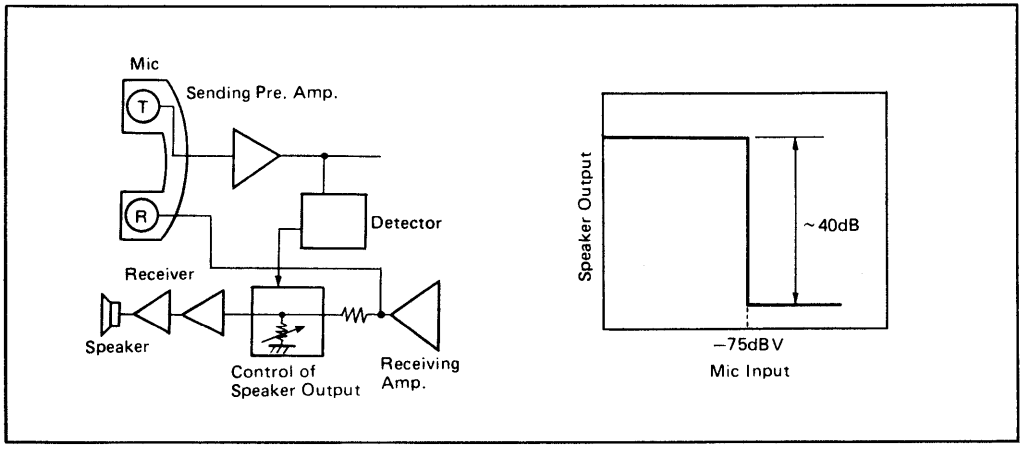
- **Speaking at speaker mode**

At speaker Mode it is possible to call under the holding Off–Hook. But when a signal enters from mike, speaker output attencates by about –40dB because of keeping away the oscillation of speaker and mike of hand set, what is called, the howling. So the sound of speaker disappears, but from the receiver of hand set, the sound can be normally heard. The threshold of mike input can be adjusted by Cex19 in the same way as noise suppression. The rising time Tup and the hang over time Th of the change of speaking and receiving are determined by Rex17 and Cex18 of 39 pin.

Tup = 13 Cex18 [ms]

Th = Cex18 · Rex17 [ms]



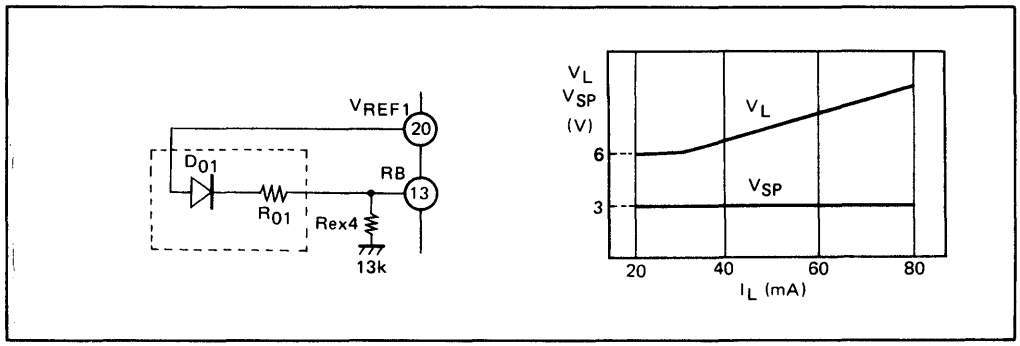


- **Hook Switch (HS)**

As 42 pin interlocks with the hook switch, in the case of GND the sending preamp. is 'on' and in the case of open it is 'off' and the signal from mike is not amplified.

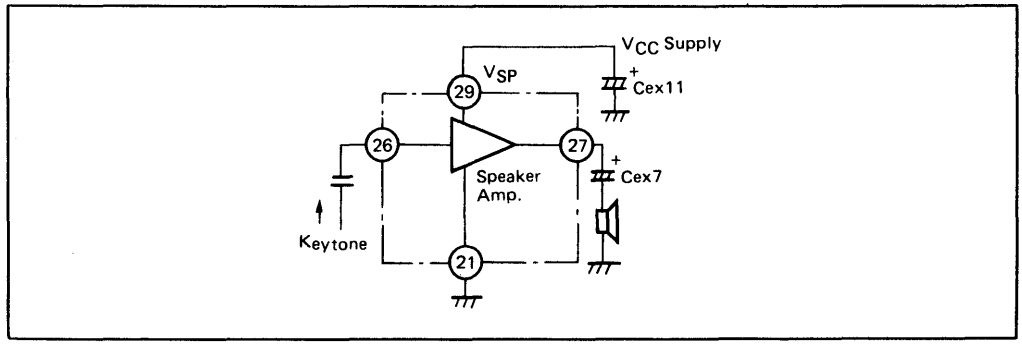
- **Backtone I_L margin Up**

While the on–hook dialing (speaker mode), the backtone is produced from speaker. Under the condition of $I_L \leqq 25mA$ the sound from speaker becomes little.
By using MUTE signal and adding a circuit, the margin increases. 13 pin is biased under the condition of 1V, the constant–current is determined by external Rex4. When MUTE becomes high level, $V_{REF}1$ changes from 1.8V typ. to 3.8V typ., constant–current decreases equivalently, and I_L margin increases.
Moreover, when 33 pin is set by 'L' level ($0.5V \leqq$), Vsp is fixed, and dynamic range of speaker amp. widens when dialing, that is, sending DTMF signal, Vsp can be fixed because of going the line voltage up to 6V.



- **Keytone Amp.**

In the case of using the pulse dialer keytone is produced as backtone as pushing dial. Then, the speaker amp. can be used as a keytone amp. When power supply is applied to Vsp (29 pin) by a zener diode, speaker amp. operates independent of other circuits.
The speaker amp. can operate under the condition of 1.5V or more. When the keytone signal is applied to 26 pin, the keytone is confirmed by speaker.



- **Line Current Detection**

The current in proportion to the Line current flows to Rex16 via 37 pin, and the line current is detected by this voltage. The voltage of 35 pin adds this voltage to +0.3V.

$V35 = V37 + 0.3V$

Moreover, the line matching impedance is proportioned to this Rex16. $Z_{IN} \propto$ Rex16

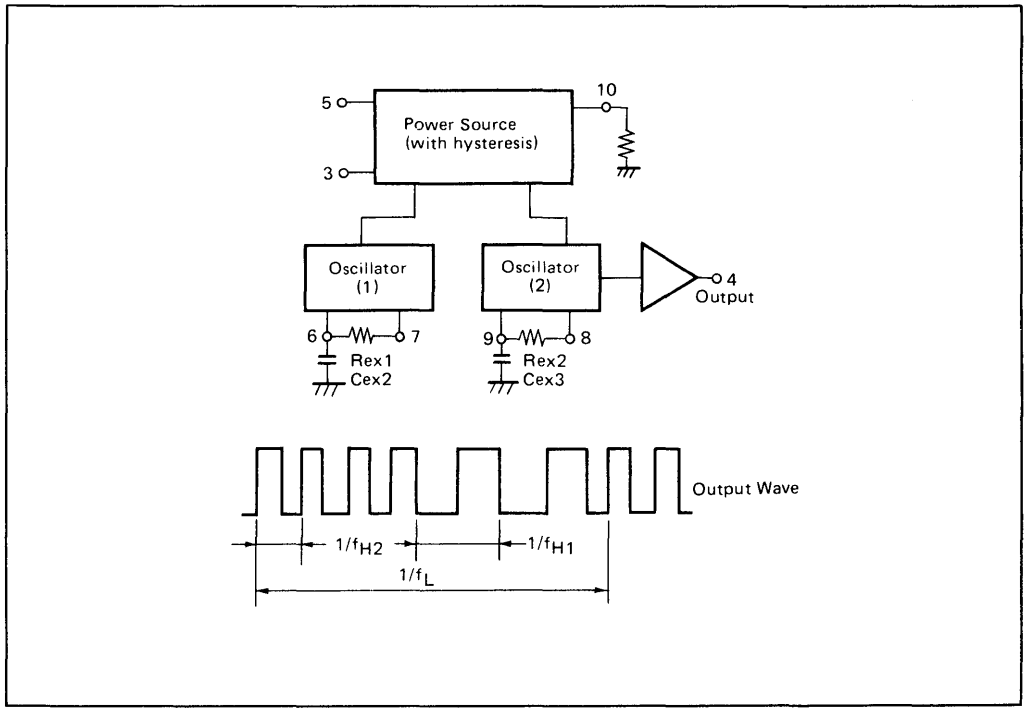
- **Tone Ringer Oscillation Frequency**

Constraction of toneringer system is same as that of the HA16805PS (toneringer). The oscillator (1) has low frequency oscillation of about 10Hz, and the oscillator (2) is demodulated by this frequency; f_L. The oscillator (2) has two oscillation frequency; f_{H1} and f_{H2} by the oscillator (1).

$f_L = 1/1.25 \cdot$ Rex1 Cex3

$f_{H1} = 1/1.35 \cdot$ Rex2 Cex3 (Hz)

$f_{H2} = 1.24\ f_{H1}$ (Hz)



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (OFF HOOK)	V_L*1	20	V
Supply Current (OFF HOOK)	I_L	120	mA
Supply Voltage (Tone Ringer)	V_{TR}	30	V
Power Dissipation	P_T	950	mW
Operating Temperature	T_{opr}	−20 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note) •1 3ms Pulse duration

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics

- **Handset Mode**

Item		Symbol	min.	typ.	max.	Unit	Test Condition I_L (mA)	
Supply Voltage	Speaking	V_L	2.3	2.6	2.8	V	20	
			5.0	6.5	8.0	V	80	
	Dialing		5.5	6.2	6.6	V	20	
			7.0	–	10.0	V	80	
Receiving Gain		G_R	−6.5	−5	−3.5	dB	30	f = 1kHz
			−12.5	−11	−9.5	dB	80	
	Up Mode		5	10	15	dB	30	R_{EXB_5} = 0Ω
Sending Gain		G_T	49.5	51	52.5	dB	30	f = 1kHz
			44	45.5	47	dB	80	
Side tone		G_{SID}	–	–	40	dB	30	f = 1kHz
DTMF Sending Gain		G_{MF}	20.5	22	23.5	dB	30	
			17	18.5	20	dB	80	
Sending Dynamic Range		DR_T	2.2	2.7	–	Vp−p	30	f = 1kHz
			4.5	6.0	–	Vp−p	80	
Receiving Dynamic Range		DR_R	0.4	0.6	–	Vp−p	20	f = 1kHz
			0.8	–	–	Vp−p	80	
DTMF Dynamic Range		DR_{MF}	2.8	4.0	–	Vp−p	20	
			3.0	–	–	Vp−p	80	
DTMF Supply Voltage	Stand-by	V_{DD}	1.6	1.8	–	V	20	
	Mute		3.5	3.8	–	V	20	
DTMF Supply Current	Stand-by	I_{DD}	200	–	–	μA	20	
	Mute		2	–	–	mA	20	
DTMF Backtone		BT_{MF}	60	85	110	mVp−p	80	V_{IN}= 170mVp−p
Line Matching Impedance		Z_{IN}	500	600	700	Ω	20, 80	f = 1kHz

• Speaker Mode

Item		Symbol	min.	typ.	max.	Unit	Test Condition I_L (mA)	
Supply Voltage	Speaking	V_{LSP}	3.9	4.35	4.7	V	20	
			6	–	9	V	80	
	Dialing		5.2	6.0	6.8	V	20	
			7	–	10	V	80	
Receiving Gain		G_{RSP}	–12.5	–10	–7.5	dB	30	f = 1kHz
			–17.5	–15	–12.5	dB	80	
Sending Gain		G_{TSP}	46	48	50	dB	30	f = 1kHz
			40	42	44	dB	80	
Side tone		G_{SIDSP}	–	–	45	dB	30	f = 1kHz
DTMF Sending Gain		G_{MFSP}	19.5	21.5	23.5	dB	30	
			16	18	20	dB	80	
Sending Dynamic Range		DR_{TSP}	2.3	–	–	Vp–p	50	f = 1kHz
Receiving (SP) Dynamic Range		DR_{SP}	0.8	–	–	Vp–p	50	Speaker Output
DTMF Dynamic Range		DR_{MFSP}	2.2	–	–	Vp–p	20	
DTMF Backtone	Receiver	BT_{MFSP}	40	65	90	mVp–p	25	Vin = 120mVp–p
	Speaker		400	550	700	mVp–p	50	
Line Matching Impedance		Z_{INSP}	270	–	700	Ω	20, 80	
Speaker Amp. Gain		G_{SP}	5	8.5	12	dB	30	

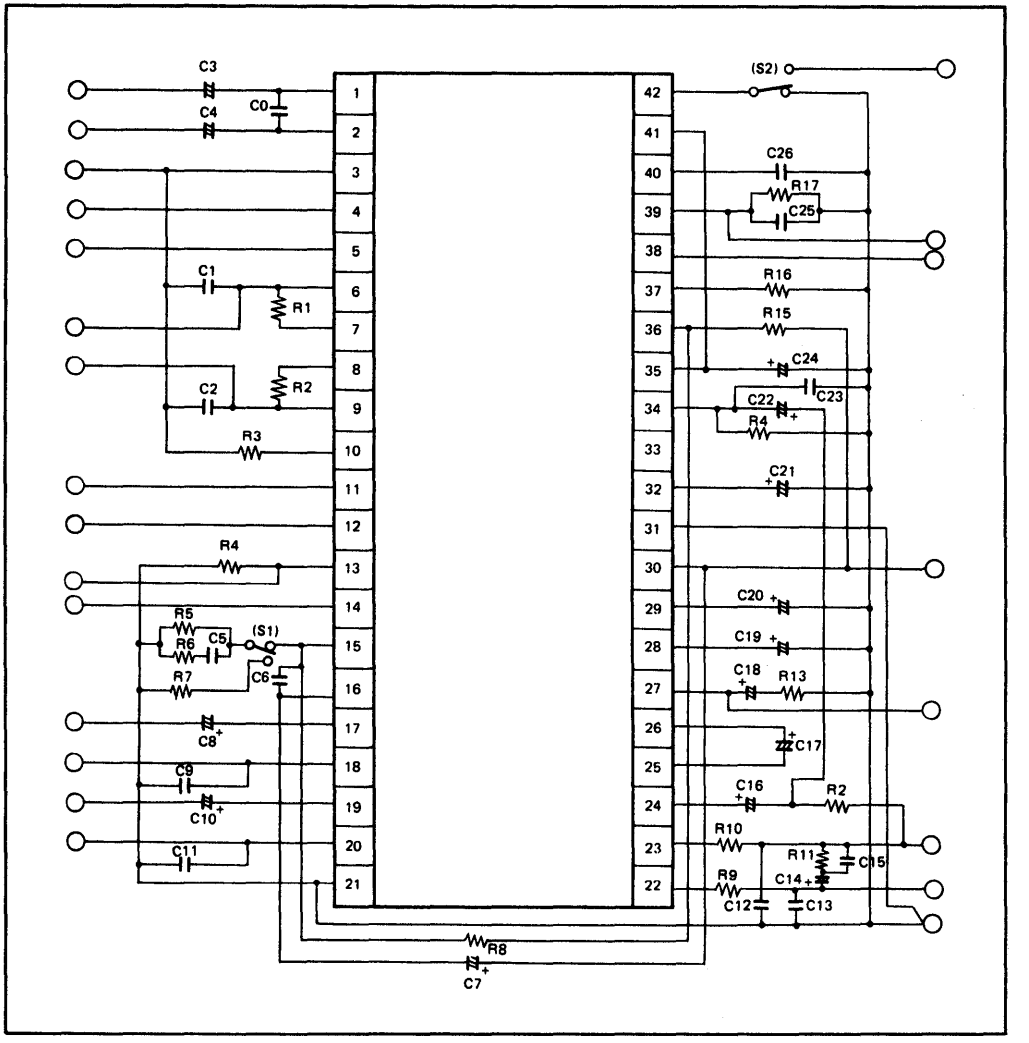
• Melody Mode

Item		Symbol	min.	typ.	max.	Unit	Test Condition I_L (mA)	
Supply Voltage		V_{LHD}	3.9	4.35	4.7	V	20	
			6	–	9	V	80	
Melody IC Supply	Voltage	V_{DH}	1.2	1.5	1.8	V	20	
	Current	I_{DH}	200	–	–	μA	20	
Melody Sending Gain		G_{HD}	22	24	26	dB	30	f = 1kHz
			19	21	23	dB	80	
Melody Sending Dynamic Range		DR_{HD}	2.2	–	–	Vp–p	30	
Melody Back tone	Receiver	BT_{HD}	30	60	90	mVp–p	30	f = 1kHz
	Speaker		350	450	550	mVp–p	30	Vin = 70mVp–p

• Tone Ringer

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Supply Initiation Voltage	V_{TH}	17	19	21	V	
Supply Initiation Current	I_{TH}	0.7	1.5	3.0	mA	
Sustaining Voltage	V_{SUS}	9	11	–	V	
Sustaining Current	I_{SUS}	0.5	1.0	2.0	mA	Vin = 15V
Output "H" Voltage	V_{OH}	20.0	21.5	22.5	V	Vin=24V, I_{OH}=–10mA
Output "L" Voltage	V_{OL}	0.7	1.0	2.0	V	Vin = 24 V, I_{OL} = 10mA
Output Frequency	f_L	9	10	11	Hz	R_1 = 165kΩ, C_1 = 0.47μF
	f_{H1}	460	510	565	Hz	R_2 = 190kΩ, C_2 = 6800pF
	f_{H2}	575	640	705	Hz	Vin = 24V

Test Circuit

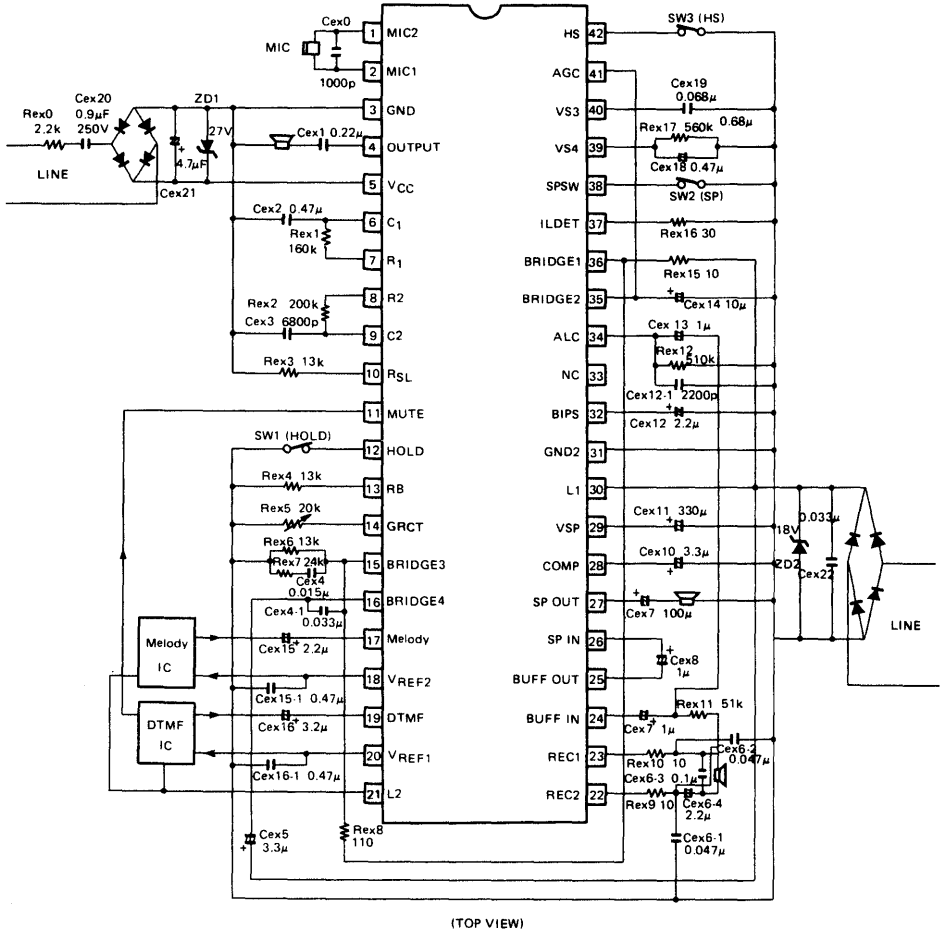


CNo.	C Value	CNo.	C Value	CNo.	C Value	CNo.	C Value	CNo.	C Value	CNo.	C Value
0	1000P	1	0.47μ	2	6800p	3	22μ	4	22μ	5	0.015μ
6	0.033μ	7	3.3μ	8	2.2μ	9	0.47μ	10	2.2μ	11	0.47μ
12	0.047μ	13	0.047μ	14	2.2μ	15	0.1μ	16	1μ	17	1μ
18	100μ	19	3.3μ	20	330μ	21	2.2μ	22	1μ	23	2200p
24	10μ	25	0.47μ	26	0.068μ						

RNo.	R Value	RNo.	R Value	RNo.	R Value	RNo.	R Value	RNo.	R Value	RNo.	R Value
1	165k	2	190k	3	13k	4	13k	5	13k	6	2.4k
7	12k	8	110	9	10	10	10	11	180	12	51k
13	8	14	510k	15	10	16	30	17	560k		

Unit R: Ω, C: F

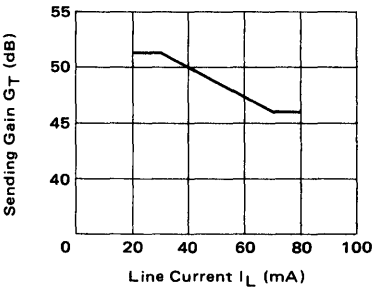
Connection Arrangement and Application Circuit



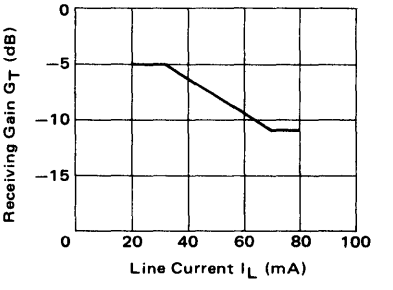
(TOP VIEW)

Note) Unit $\left(\begin{matrix} R\ (\Omega) \\ C\ (F) \end{matrix}\right)$

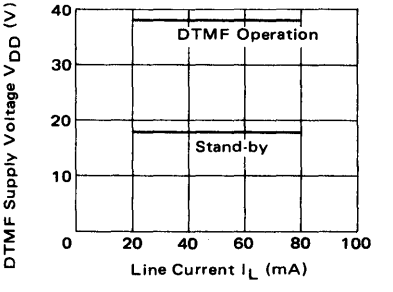
External Components are only for reference.



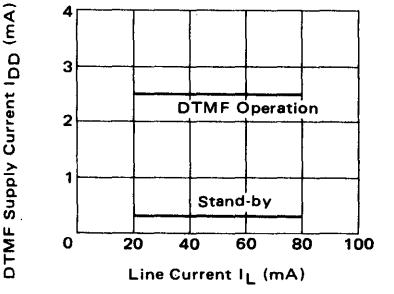
SENDING GAIN VS. LINE CURRENT



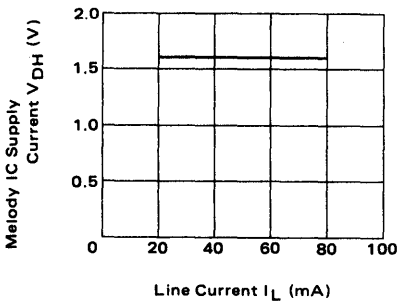
RECEIVING GAIN VS. LINE CURRENT



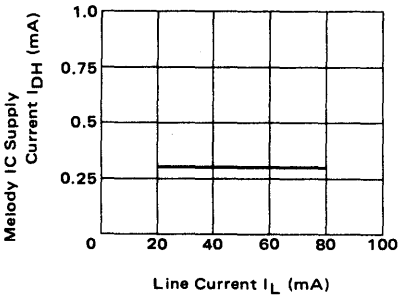
DTMF SUPPLY VOLTAGE VS. LINE CURRENT



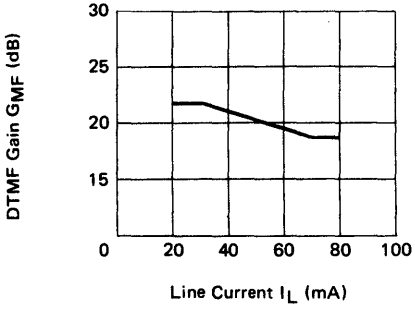
DTMF SUPPLY CURRENT VS. LINE CURRENT



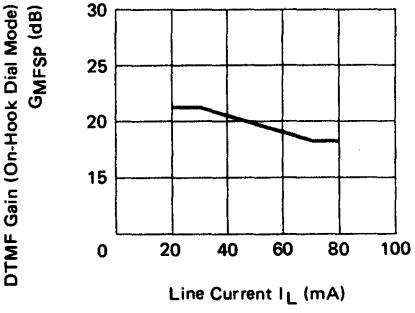
MELODY IC SUPPLY VOLTAGE VS. LINE CURRENT



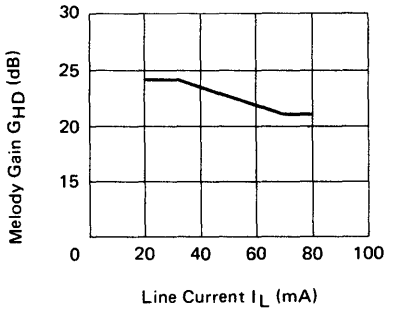
MELODY IC SUPPLY CURRENT VS. LINE CURRENT



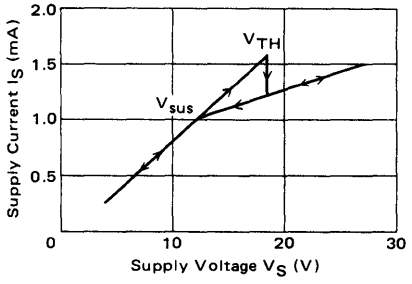
DTMF GAIN VS. LINE CURRENT



DTMF GAIN (ON-HOOK DIAL MODE) VS. LINE CURRENT



MELODY GAIN VS. LINE CURRENT



TONE RINGER SUPPLY VOLTAGE VS. SUPPLY CURRENT

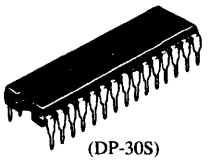
HA16820NT

Speech Network IC with Built-in Speaker Amp. for Telephone Sets (Speakerphone)

Description

The HA16820NT realizes an excellent branching performance by incorporating a speech network and speaker amplifier on one chip while achieving low current dissipation and low voltage operation. This IC well suited telephones with speaker.

HA16820NT

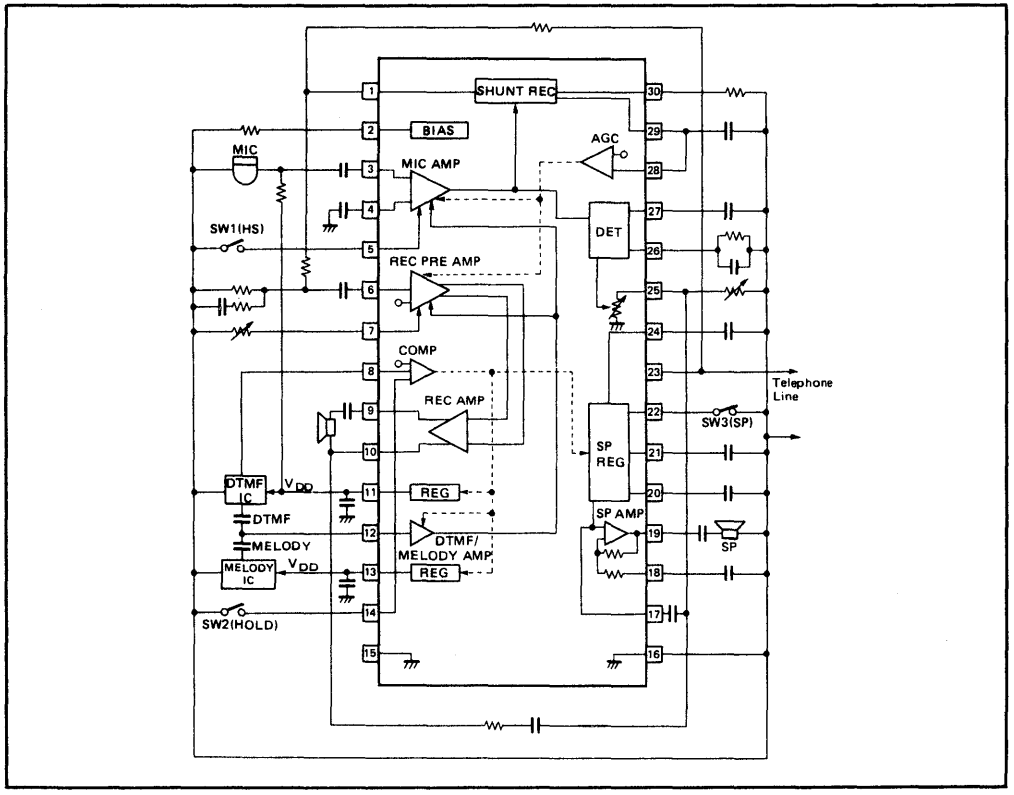


(DP-30S)

Features

- Low current dissipation, low voltage operation (5mA, 1.8V)
- Makes speaker amplified calls possible (Permits speech through handsets while receiving speaker amplified call)
- Prevents howing during speaker amplified call
- Directly drives 8Ω speaker
- Permits on-hook dialing by incorporating speaker amp. on chip
- Line compensation on chip (sending, receiving, DTMF sending, melody sending gain)
- DTMF sending interface on chip (power supply, MUTE, DTMF sending amp.)
- Melody sending interface on chip (power supply, melody sending amp.)
- Backtone can be output through either the receiver or speaker amp. during DTMF or melody sending
- 30 pins shrink plastic DIP package (DP-30S)

Block Diagram



Pin Description

Pin No.	Symbol	Pin description
1	BRG1	Bridge pin 1
2	R_B	IC bias current decision
3	MIC1	Mike input
4	MIC2	Mike input
5	HS	Hook switch
6	BRG2	Receiver amp. input (bridge pin)
7	GRCT	Receiver gain variable
8	MUTE	MUTE
9	REC1	Receiver output
10	REC2	Receiver output
11	V_{DD} 1	Regulator for DTMF IC
12	VIN	DTMF/melody input
13	V_{DD} 2	Regulator for melody IC
14	HOLD	ON when melody is being sending.
15	L2	Line (GND)
16	SP GND	GND (Speaker section)
17	SP IN1	Speaker amp. signal input
18	SP IN2	Speaker amp. input
19	SP OUT	Speaker amp. output
20	V_{SP}	Speaker regulator
21	BIPS1	AC bypass
22	SP SW	ON during speaker amp. mode
23	L1	Line
24	BIPS2	AC bypass
25	ATT	ATT pad on speaker amp. mode
26	VS1	Voice switch (on speaker amp. mode)
27	VS2	
28	AGC	AGC
29	VLDET	Line voltage detection
30	ILDET	Line current detection

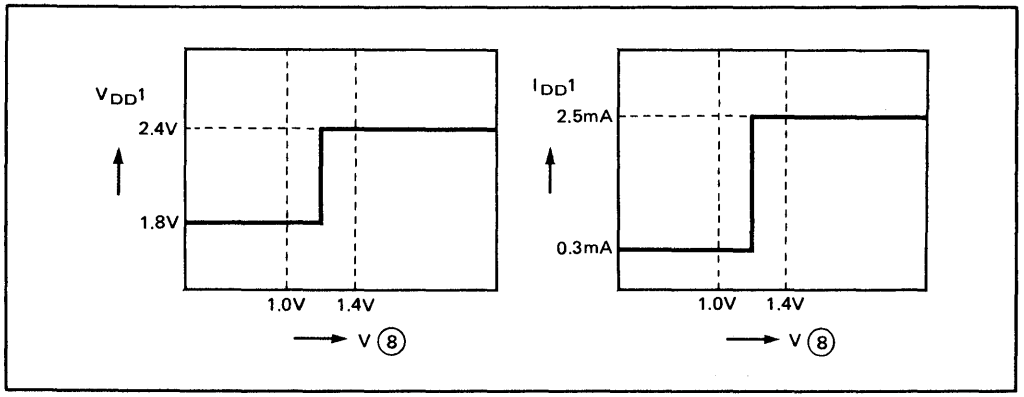
Functional Description

1. DTMF Interface

The DTMF sending mode is activated when pin (8). (MUTE) voltage (V (8)) becomes 1.6V or more (threshold is 1.2V typ.). In this mode, the sending and receiving input amp. are off and the DTMF sending amp. is on. The DTMF signal is input to pin (12). However, since it has a bias of about 1V, and AC couple (Cex8) is required.

An input level of from 50 to 70mVrms is appropriate since the sending gain is a little over 20dB. As soon as the DTMF signal is sent out the line, a backtone is generated from receiver, and during a speaker amp. call, it is also generated from speaker.

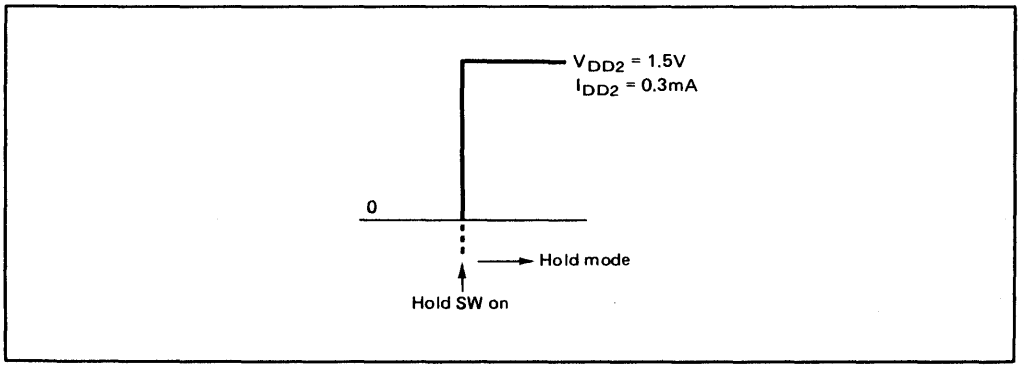
This IC is provided with a flexible power supply which changes the supply voltage and current (pin (11)) according to whether the device is in waiting or operating status.



2. Holding Interface

The holding interface mode is activated when pin (14) (HOLD) is connected to GND. In this mode, the sending and receiving amps. are off and the melody sending amp. is on. The melody is input to pin (12). However, since it has a bias of about 1V, an AC couple (Cex9) is required.

An input level of from 10 to 30mVrms is appropriate since the sending gain is a little over 20dB. As soon as the melody is sent to the line, backtone is generated from the speaker. At this time, the melody IC power supply is on for the first time.

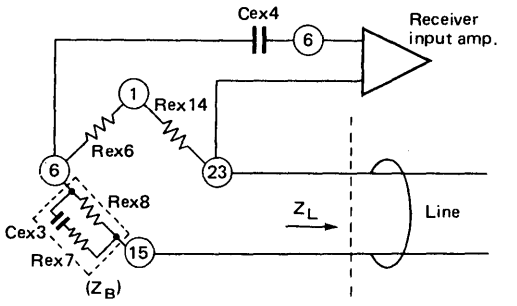


3. Sidetone Suppression Circuit

Sidetone suppression circuit is constructed with bridge-type resistance. To suppress sidetone, Z_B is adjusted by the following equation in response to line impedance Z_L.

$$\frac{Rex6}{Rex14} = \frac{Z_B}{Z_L}$$

Cex4 is for AC couple. Receiver gain is increased by increasing resistance while maintaining a Rex6/Rex14 ratio. For example, when Rex6/Rex14 = 330Ω/30Ω, receiver gain is increased by about 6dB over that when Rex6/Rex14 = 110Ω/10Ω.



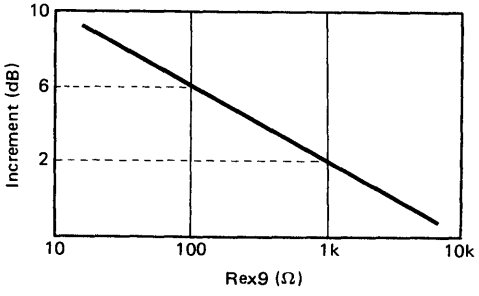
4. Receiving Gain Variable

Receiving gain is increased by lowering Rex9.

For example, when Rex9 = 100Ω, receiving gain is increased by about 6dB over that when pin (7) is open.

In some modes, receiving gain adjust function is automatically set to off.

Mode	Speech		Dialing	Holding
	Handset	Speaker	(DTMF Sending)	
On Off	On	Off	Off	Off

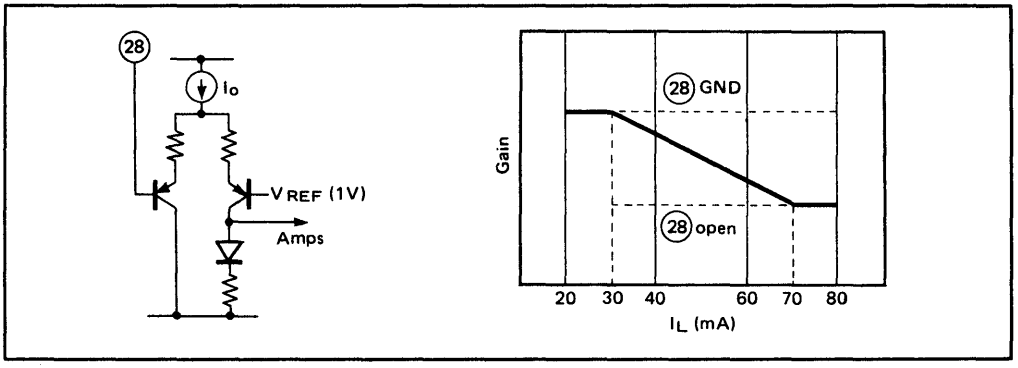


5. AGC Characteristics (Line Compensation)

By connecting pins (28) and (29) , sending and receiving gain, DTMF and melody sending gain are automatically adjust to coincide with line current.

The gain fixed mode is set by disconnecting pin (29) and applying a constant voltage to pin (28) .

High gain fixed when $0V \leqq V$ (28) $\leqq 0.3V$, Low gain fixed when V (28) = V (23) or open. However, gain changes when I_L is from 30mA to 70mA.

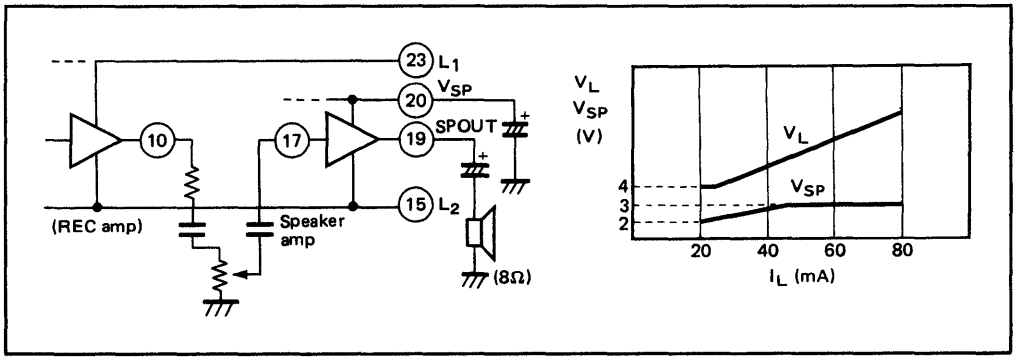


6. Speaker Amp.

The speaker amp. mode is activated when pin (22) (SPSW) is connected to GND. In this mode, the speaker amp. and speaker regulator (V_{SP}) comes on for the first time. Speaker output volume is adjusted by volume insertion.

The dynamic range of line L1 is assured by adjusting voltage V_{SP} to coincide with line current I_L.

V_{SP} changes from 2V to 3V, when $20mA \leqq I_L \leqq 50mA$, and V_{SP} is constant to 3V when $I_L \leqq 50mA$.



7. Speech in Speaker Amp. Mode (Handset Speaker Amp.)

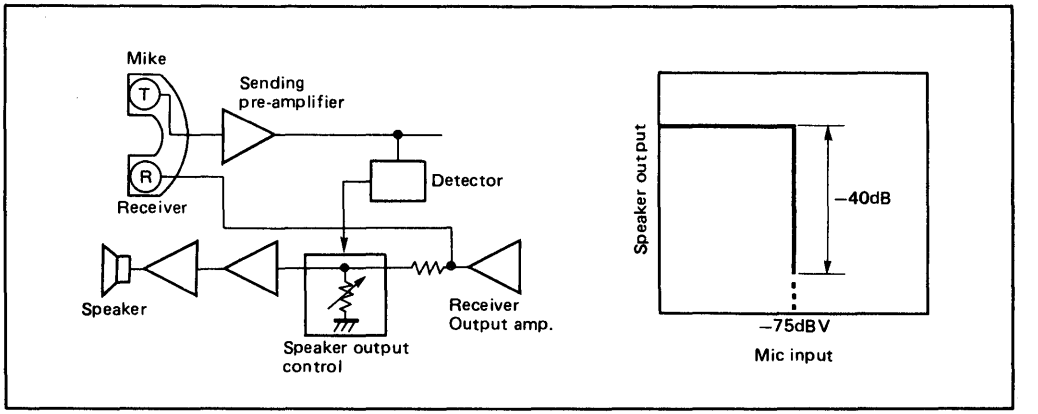
It's possible to talk holding handset in the speaker amp. mode. However, in order to prevent howing (that is resonance between the speaker and handset mike), a speaker output loss of about – 40dB is provided in cases when signals are input into the mike.

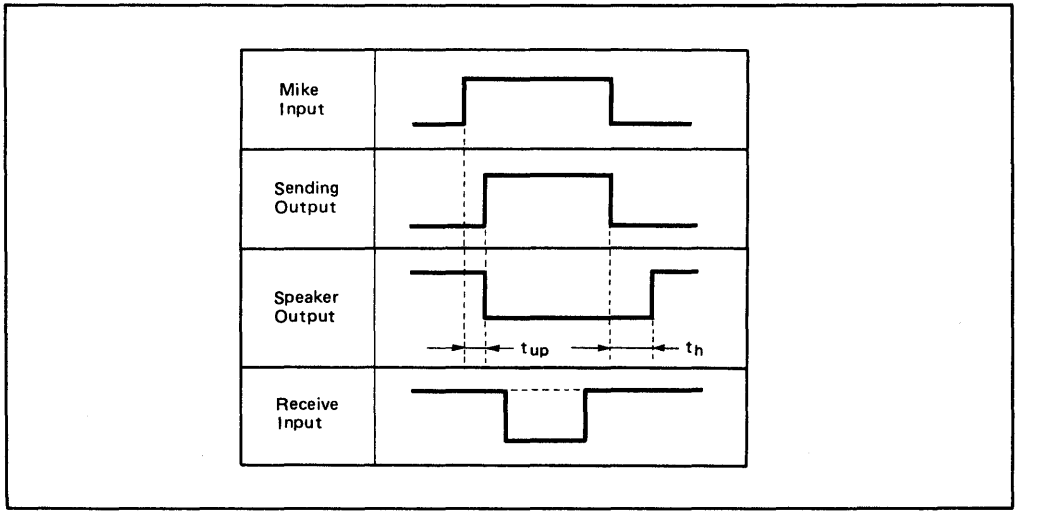
As a result, handset receiver output is heard normally while speaker output is eliminated. The mike input threshold is adjustable with Cex20.

Rise time t_{up} and hang – over time t_h are determined by Rex12 and Cex19 of pin (26) .

$t_{up} \fallingdotseq 13$ Cex19 (ms)

$t_h \fallingdotseq$ Cex19 · Rex12 (ms)





8. Hook Switch (HS)

Pin ⑤ is linked to the hook switch. The sending pre-amplifier is on when the pin is connected to GND, and off when it is open and the signal from the mike is not amplified.

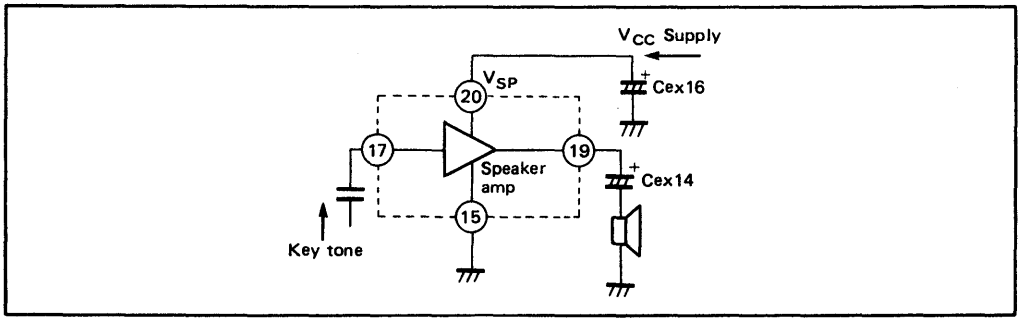
⑤	Pre-Amplifier
GND	ON
OPEN	OFF

9. Line Current Detection

Line current is detected by Rex13 of pin ㉚
The voltage of pin ㉙ is,
V ㉙ = V ㉚ + 0.3V
The line matching impedance is proportionate to the Rex13.
$Z_{IN} \propto$ Rex13

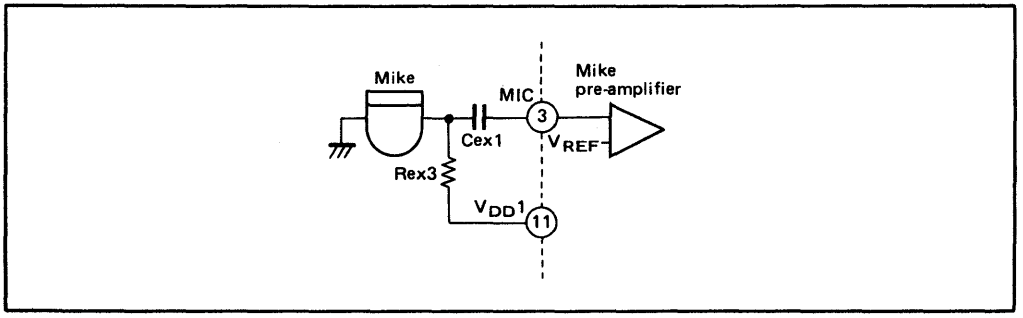
10. Key Tone Amplifier

The key tone is generated as the backtone when dialing with a pulse dialer. The speaker amp. can also be used as the key tone amp.
Voltage is applied to V_{SP} (pin ⑳), using a zener diode. The speaker amp. is activated when a voltage of 1.5V or more is applied. Generation of the key tone from the speaker can be verified by inputing the key tone in pin ⑰ .



11. Mike Bias

Mike bias is provided for capacitor mike. Pin ⑪ $V_{DD}1$ is used for mike bias source. This $V_{DD}1$ is 1.8V typ, and the Rex3 of which is determined by the type of mike used. The signal from the mike is input to mike pre-amplifier through Cex1.



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Supply Voltage*1	V_L	15	V
Supply Current	I_L	120	mA
Operating Temperature Range	Topr	−20 ~ +70	°C
Storage Temperature Range	Tstg	−55 ~ +125	°C
Power Dissipation	P_T	850	mW

Note) 1: 3ms Pulse duration (Keep the duration to be more than 3 sec.)

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics (Ta=25°C)

On Handset Mode:

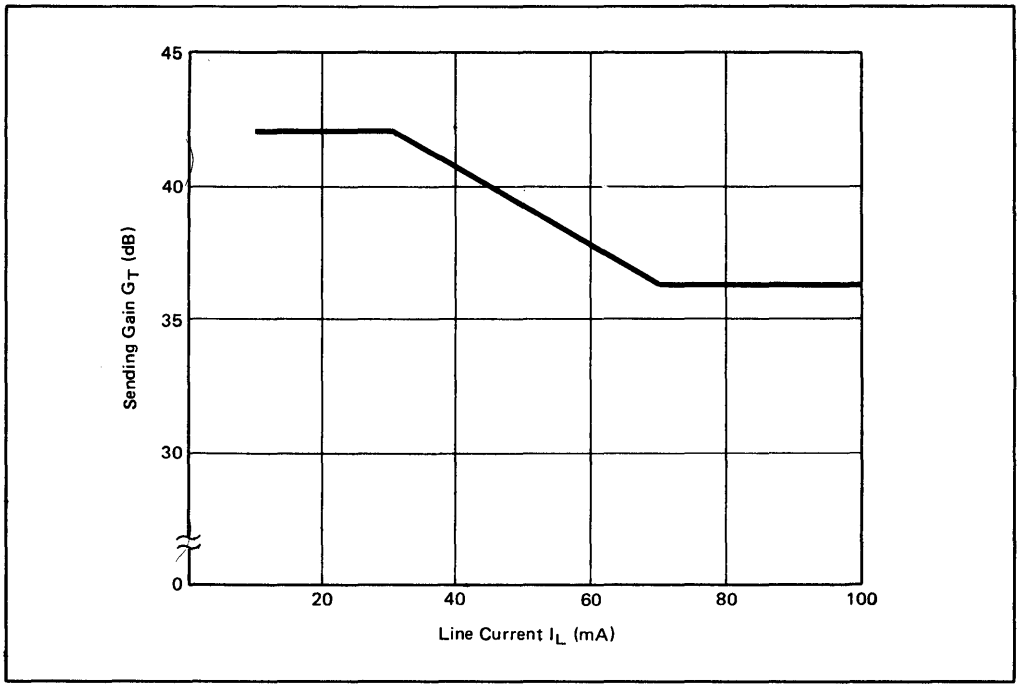
Item		Symbol	Min	Typ	Max	Unit	I_L mA	Test Conditions
Supply Voltage	Speaking	V_L	2.5	2.8	3.0	V	20	
			5.0	6.5	8.0	V	80	
	Dialing		3.6	4.0	4.4	V	20	
			6.5	8.0	9.5	V	80	
Receiver Gain		G_R	−6	−4	−2	dB	30	f=1kHz
			−11	−9	−7	dB	80	
	Up Mode		2.5	6.5	10.5	dB	30	Rex 9=0Ω
Sending Gain		G_T	39	41	43	dB	30	f=1kHz
			34	36	38	dB	80	
DTMF Sending Gain		G_{MF}	22	24	26	dB	30	f=1kHz
			19	21	23	dB	80	
Sending Dynamic Range		DR_T	2.5	3.5	–	Vp-p	30	f=1kHz, Distortion=5%
			3.5	4.5	–	Vp-p	80	
Receiving Dynamic Range		DR_R	0.7	1.0	–	Vp-p	30	f=1kHz, Distortion=5%
			0.8	1.1	–	Vp-p	80	
On Dialing Dynamic Range		DR_{MF}	2.5	4.0	–	Vp-p	30	f=1kHz, Distortion=5%
			2.5	4.0	–	Vp-p	80	
DTMF Supply Voltage	Stand-by	V_{DD1}	1.6	1.8	–	V	20	
	Mute		2.2	2.4	2.6	V	20	
DTMF Supply	Stand-by	I_{DD1}	220	–	–	μA	20	$V_{DD} \geqq 1.6V$
	Mute		2	–	–	mA	20	$V_{DD} \geqq 2.2V$
DTMF Backtone		BT_{MF}	−13	−8	−4	dB	30	V_{IN}=50mV, f=1kHz
Characteristics Impedance		Z_{IN}	480	600	720	Ω	30, 80	f=1kHz

On Speaker Amp. Mode:

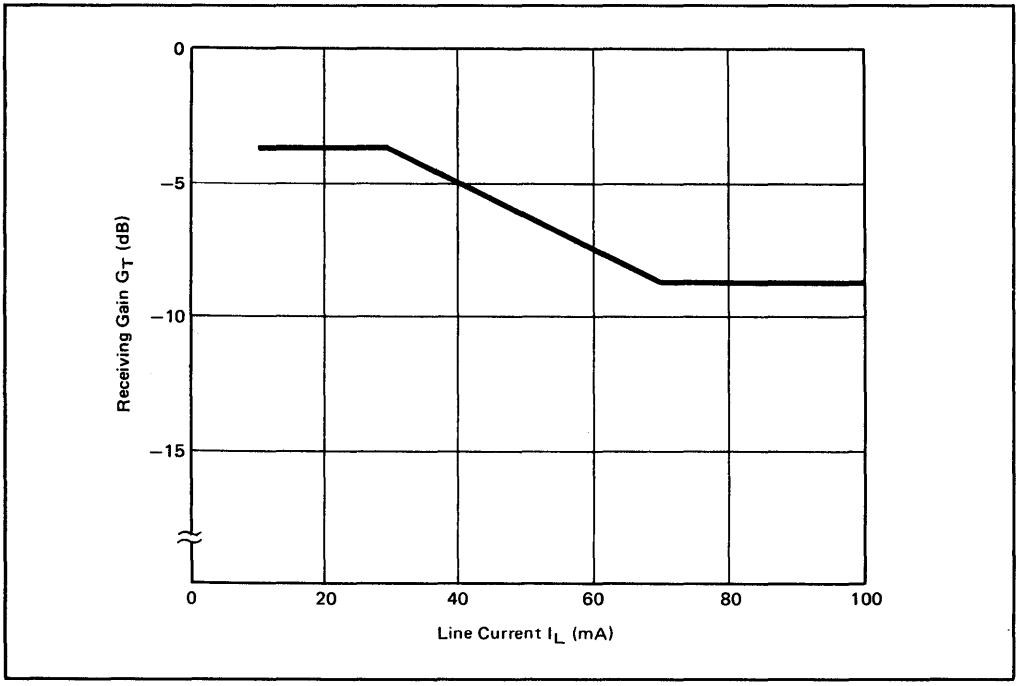
Item		Symbol	Min	Typ	Max	Unit	I_L mA	Test Conditions
Supply Voltage	Speaking	V_{LSP}	3.6	4.0	4.4	V	20	
			6.6	7.8	9.0	V	80	
	Dialing		3.5	3.9	4.3	V	20	
			6.6	7.8	9.0	V	80	
Receiving Gain		G_{RSP}	−6.5	−4.0	−1.5	dB	30	f=1kHz
			−12.0	−9.5	−7.0	dB	80	
Sending Gain		G_{TSP}	38.5	41	43.5	dB	30	f=1kHz
			33	35.5	38	dB	80	
DTMF Sending Gain		G_{MFSP}	21.5	24	26.5	dB	30	f=1kHz
			18.5	21	23.5	dB	80	
Sending Dynamic Range		DR_{TSP}	2.5	3.8	–	Vp-p	50	f=1kHz Distortion=5%
Receiving (SP) Dynamic Range		DR_{SP}	0.7	1.0	–	Vp-p	50	SP Output, f=1kHz, Distortion=5%
On Dialing Dynamic Range		DR_{MFSP}	2.5	3.5	–	Vp-p	50	f=1kHz, Distortion=5%
DTMF Backtone	Speaker	BT_{MFSP}	7	10	13	dB	50	Vin=50mV, f=1kHz
Line Matching Impedance		Z_{INSP}	450	600	750	Ω	30, 80	f=1kHz
Speaker Amp. Gain		G_{SP}	8	12	16	dB	30	f=1kHz

On Holding Mode :

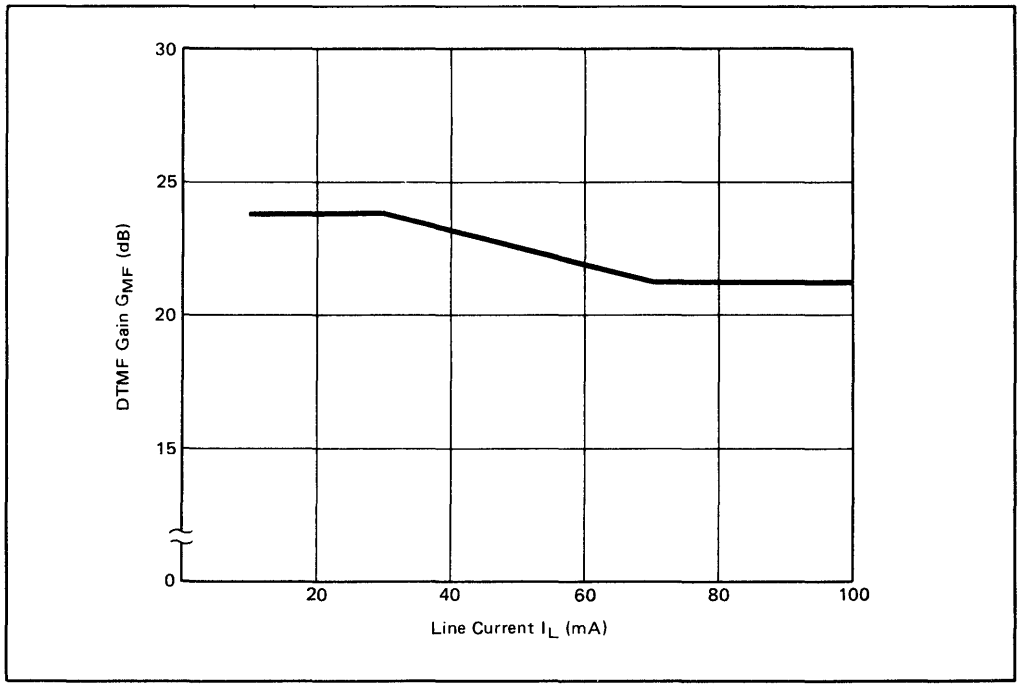
Item		Symbol	Min	Typ	Max	Unit	I_L mA	Test Conditions
Supply Voltage		V_{LHD}	3.6	4.0	4.4	V	20	
			6.5	7.7	8.9	V	80	
Melody IC	Voltage	V_{DD2}	1.2	1.5	1.8	V	20	
Supply	Current	I_{DD2}	200	300	–	μA	20	
Melody Sending Gain		G_{HD}	21.5	24	26.5	dB	30	f = 1kHz
			18.5	21	23.5	dB	80	
Melody Sending Dynamic Range		DR_{HD}	2.5	4.5	–	Vp-p	50	f = 1kHz, Distortion = 5%
Melody Backtone	Speaker	BT_{HD}	19	22	25	dB	50	f = 1kHz



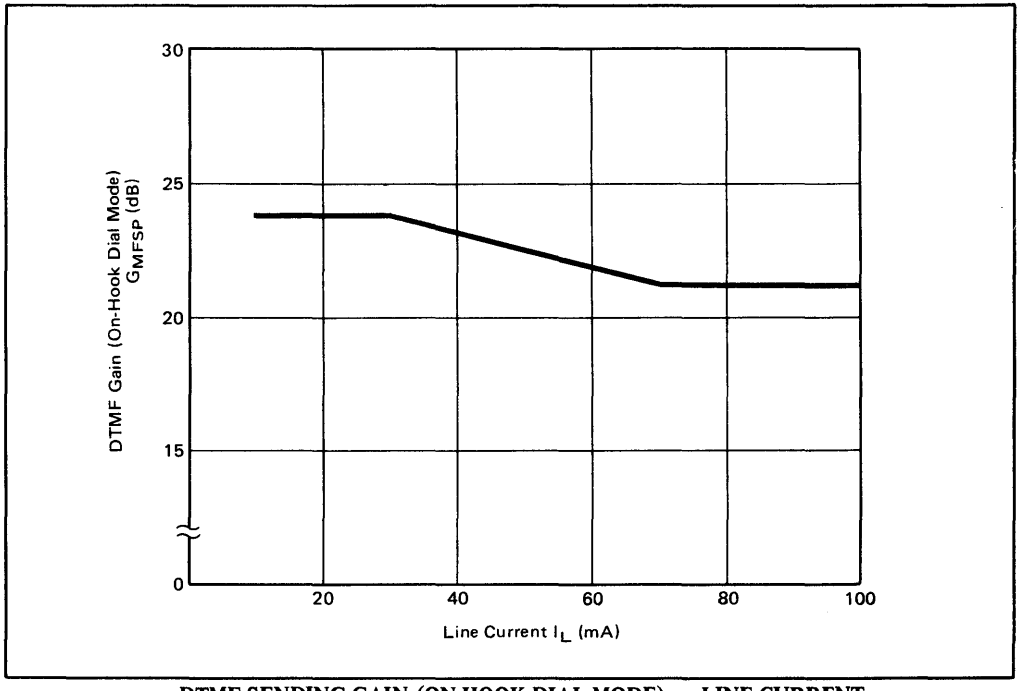
SENDING GAIN vs. LINE CURRENT



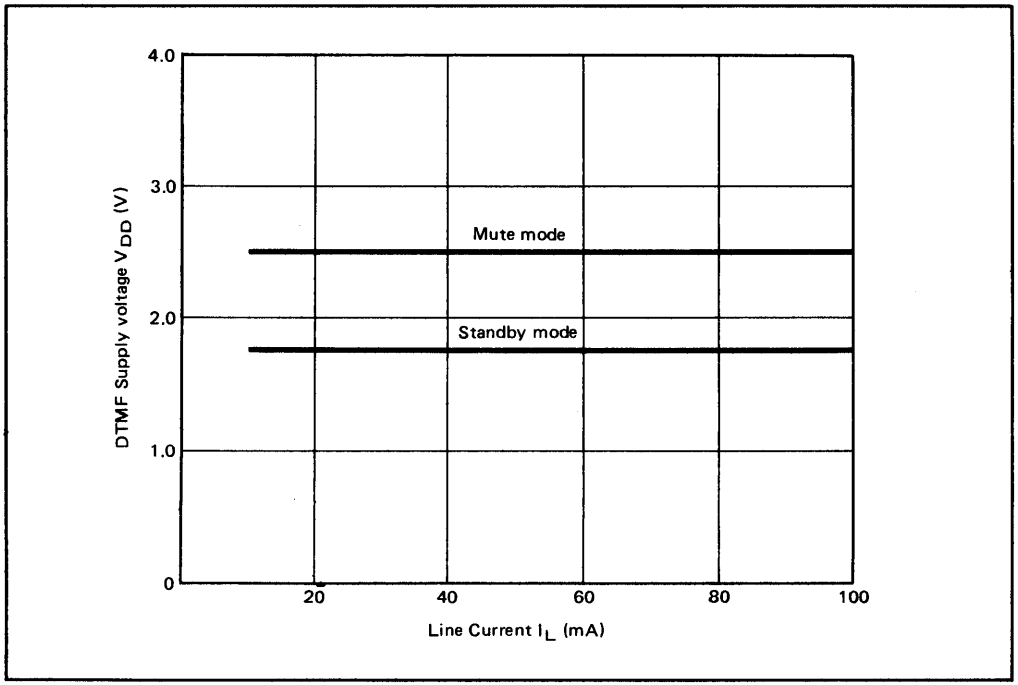
RECEIVING GAIN vs. LINE CURRENT



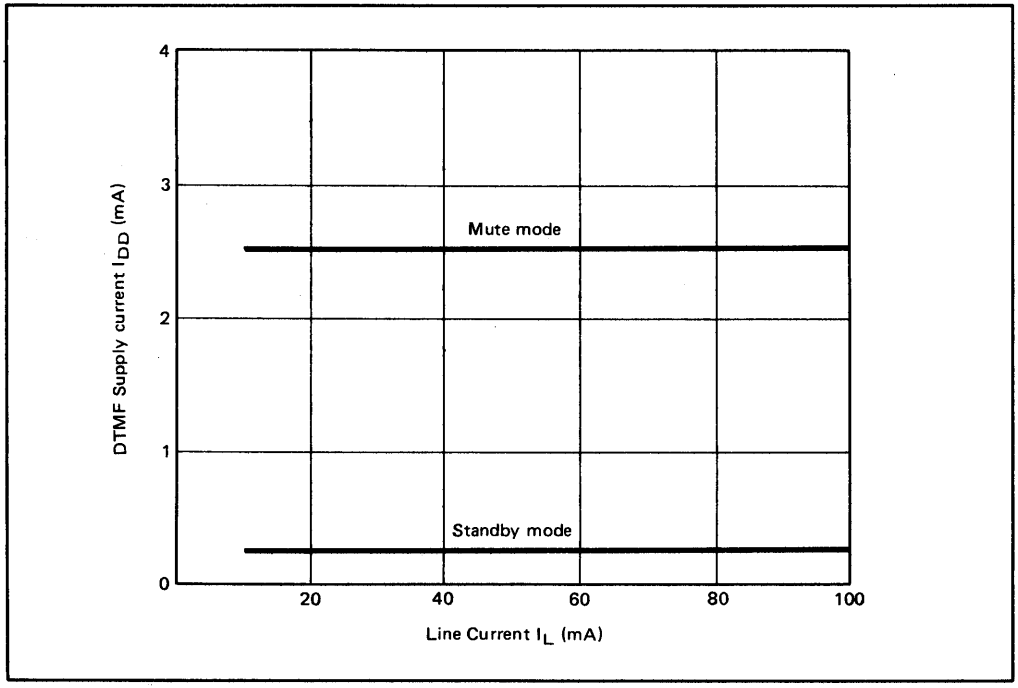
DTMF GAIN vs. LINE CURRENT



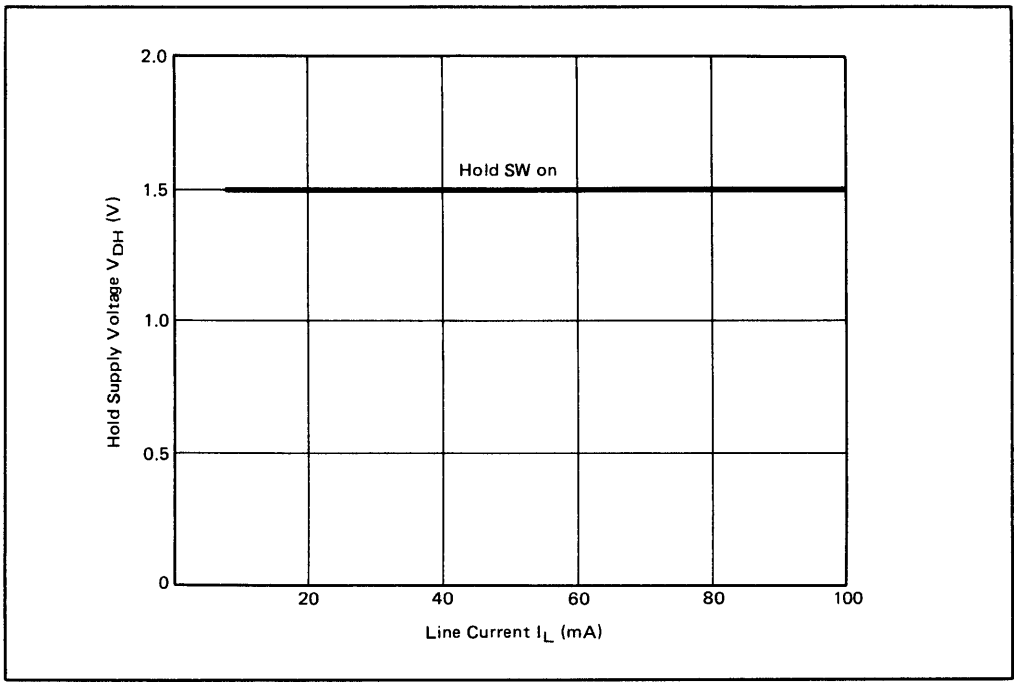
DTMF SENDING GAIN (ON-HOOK DIAL MODE) vs. LINE CURRENT



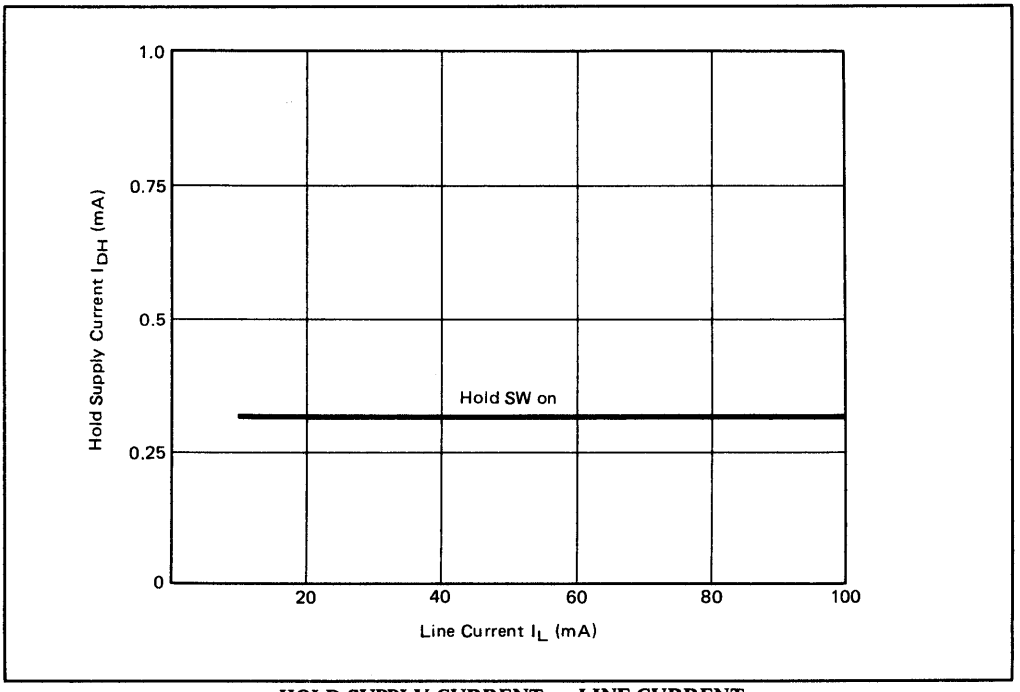
DTMF SUPPLY VOLTAGE vs. LINE CURRENT



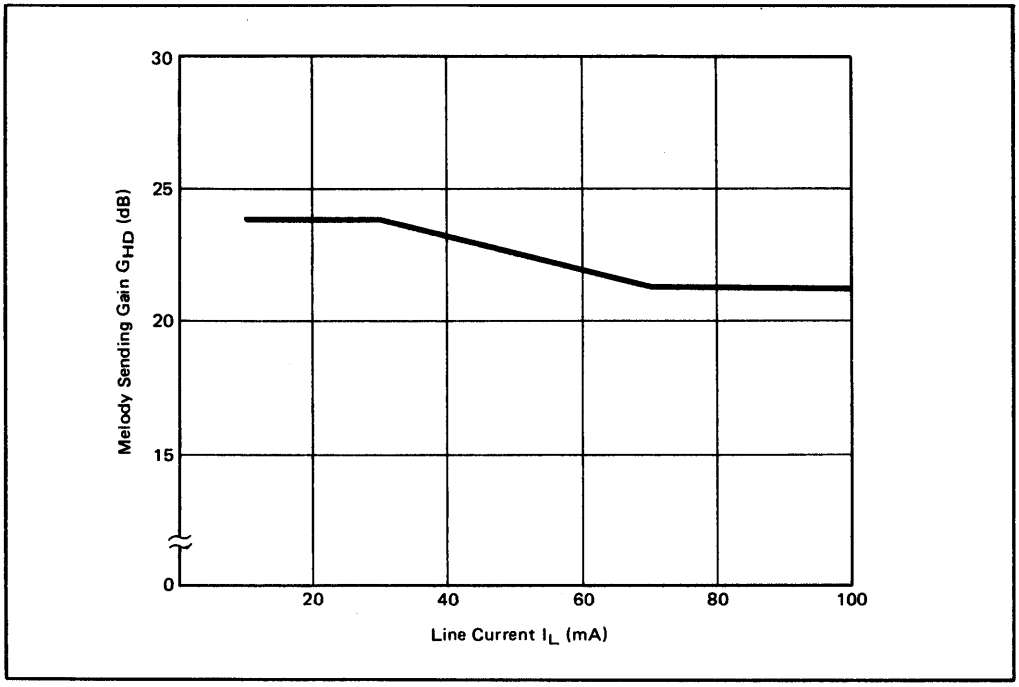
DTMF SUPPLY CURRENT vs. LINE CURRENT



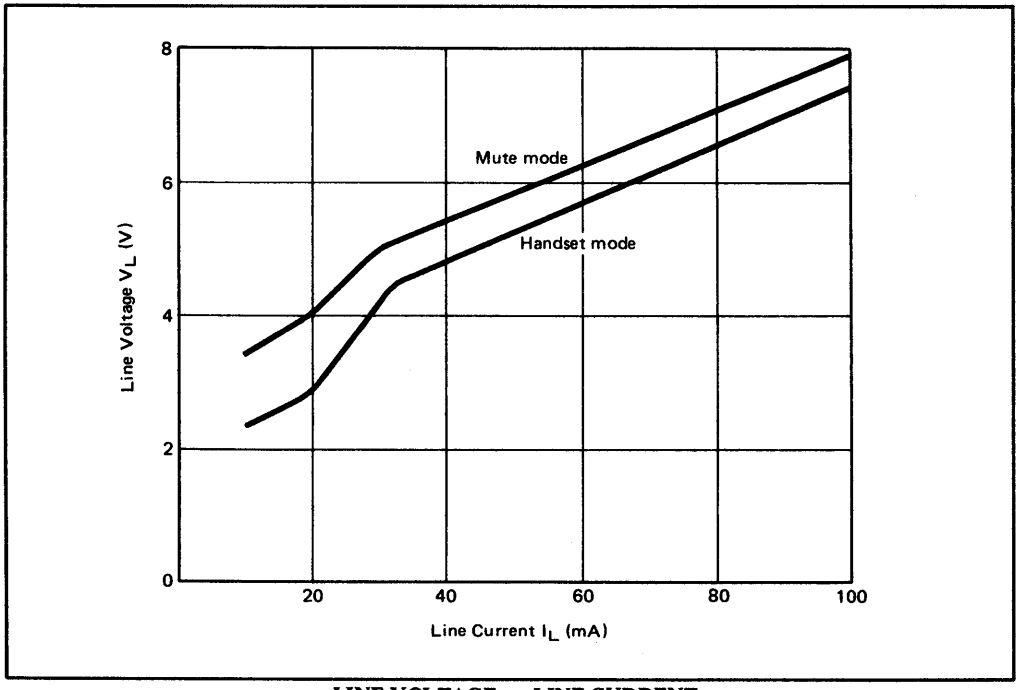
HOLD SUPPLY VOLTAGE vs. LINE CURRENT



HOLD SUPPLY CURRENT vs. LINE CURRENT

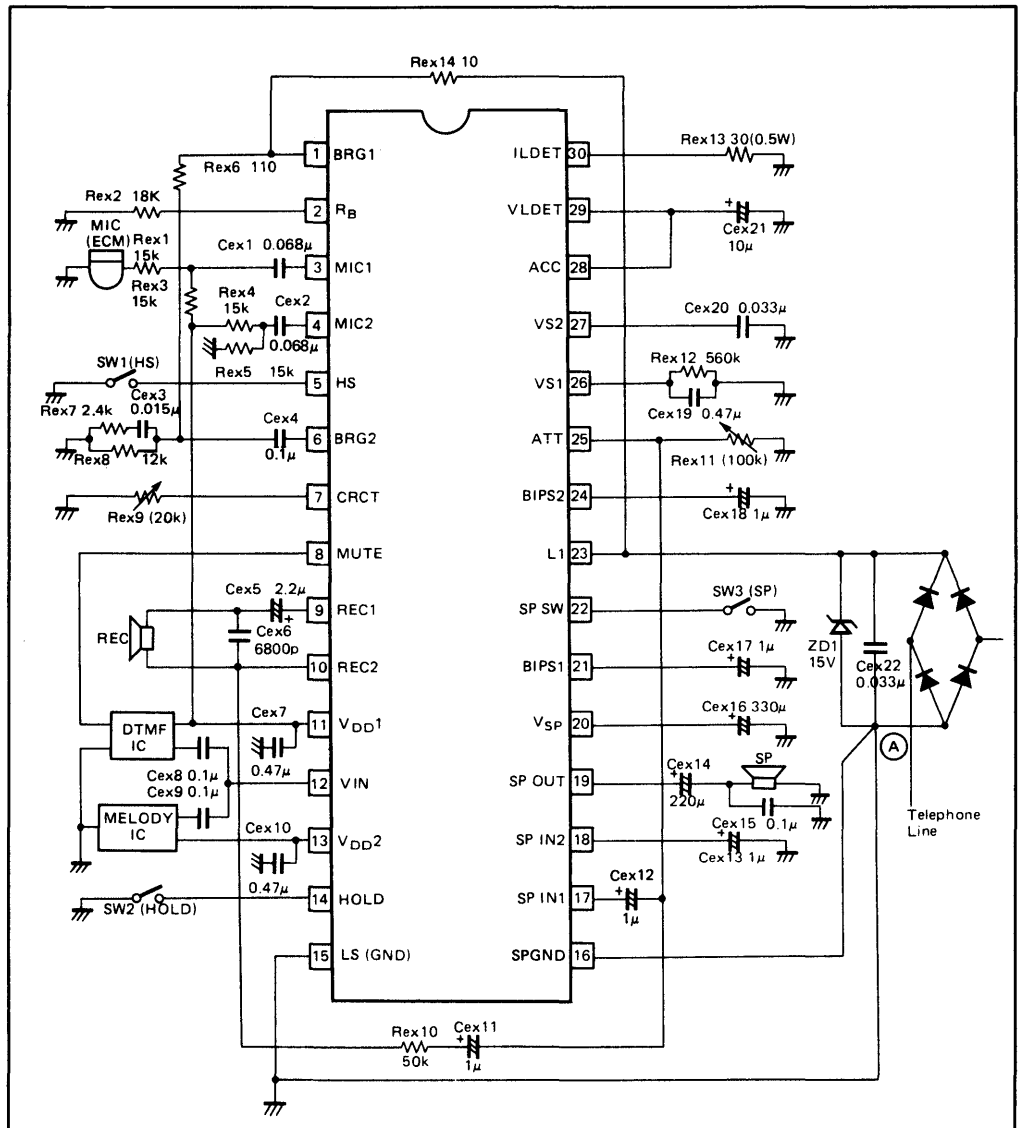


MELODY SENDING GAIN vs. LINE CURRENT



LINE VOLTAGE vs. LINE CURRENT

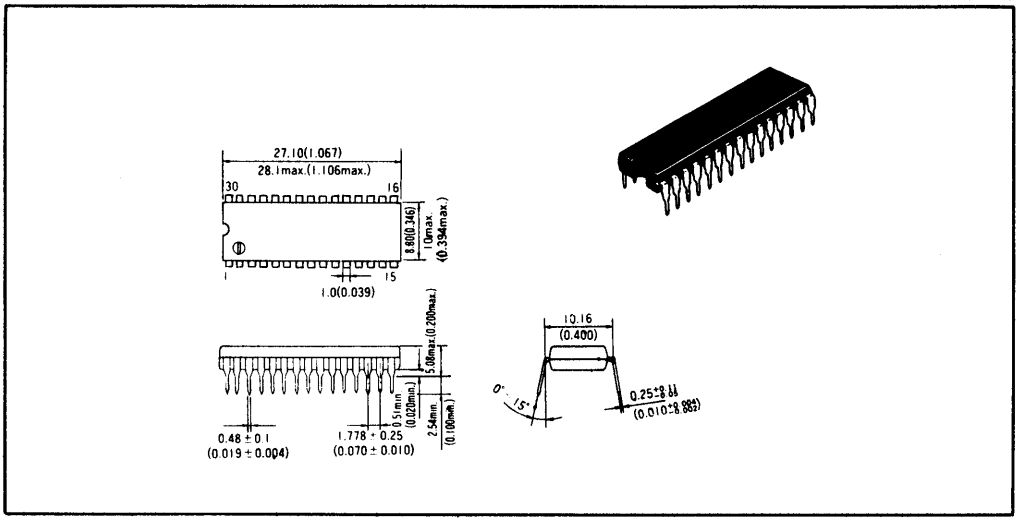
Circuit Example



Notes) 1. Externalized components are exmple, Unit R:Ω, C:F
2. SP GND shall be to connected to L2 at the near the TEL line.

Dimensional Outline

Unit: mm(inch)



HA16821P/HA16821MP/HA16821F — Preliminary

Speech Network IC for Telephone Sets

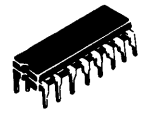
Description

The HA16821 realizes an excellent branching performance by achieving low current dissipation and low voltage operation as speech network IC. It is possible to send DTMF signal or backtone to line or receiver. Moreover there are three kinds of packages.

Features

- Low current dissipation, low voltage operation. (5 mA, 1.8 V)
- Possible of direct interface to light, low impedance receiver.
- Possible of auto gain control cope with line current. (AGC)
- DTMF signal can be send to line and backtone can be send to receiver.
- Built in regulator to bias of small ceramic transmitter.

HA16821P

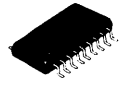


DP-16

HA16821MP

MP-18

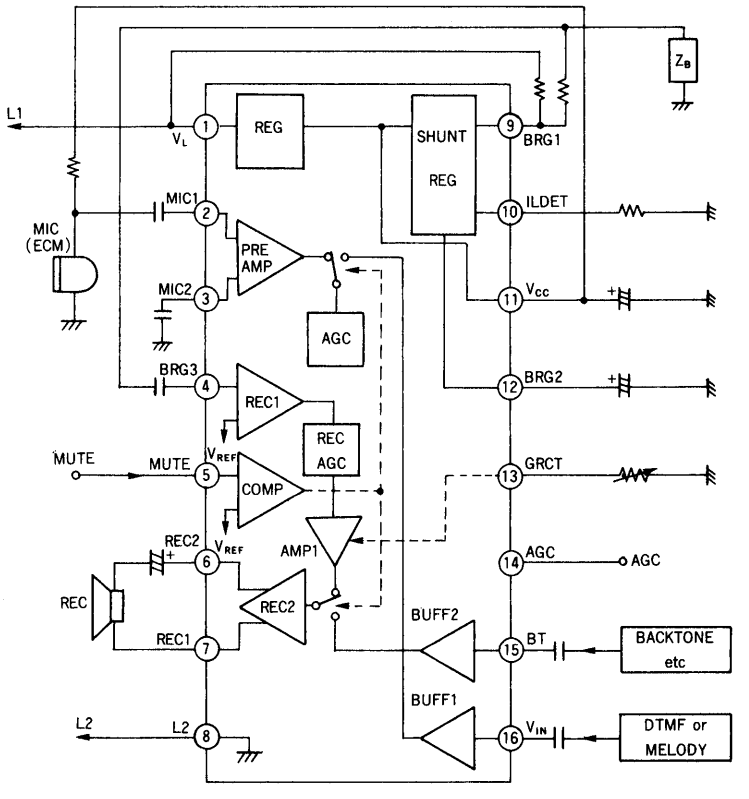
HA16821F



FP-18D

2

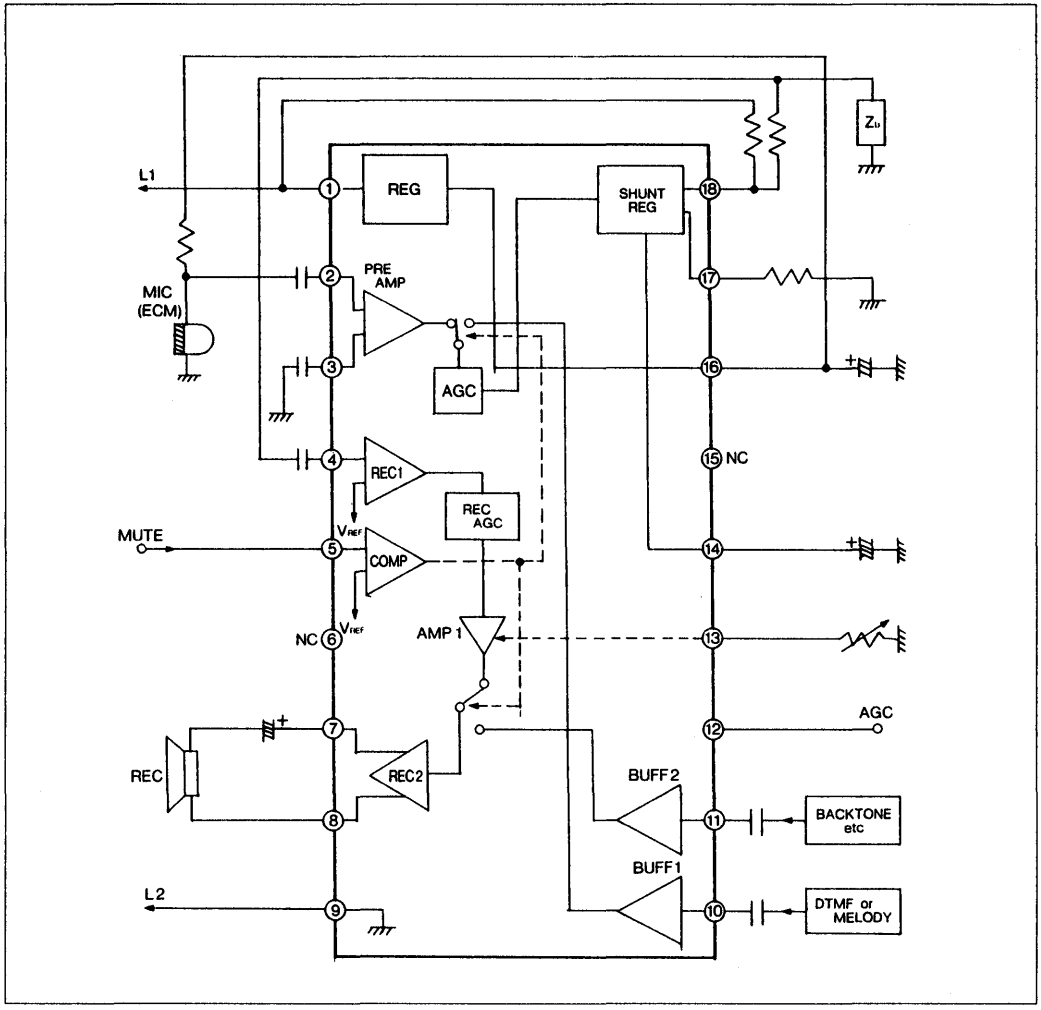
Block Diagram (HA16821P)



Pin Description (HA16821P)

Pin No.	Symbol	Pin Description	
1	V_L	Line Input	Connect with plus-output of diode bridge circuit.
2	MIC1	Mike Input	This pin is a signal-input pin from mike. Input impedance is 30 kΩ typ.
3	MIC2	Mike Input	This pin is input of mike pre-amplifier. Input impedance is 30 kΩ typ. To suppress oscillation, connect capacitor.
4	BRG3	Receiver Input	This pin is input of receiver pre-amplifier. Adjust balancing network Z_B to restrain from sidetone.
5	MUTE	MUTE	This IC becomes DTMF/HOLD mode when voltage of this pin is over 1.4 V.
6	REC2	Receiver Output	Connect to dynamic receiver.
7	REC1	Receiver Output	Connect to dynamic receiver.
8	L2	Line (GND)	Connect with minus-output of diode bridge circuit.
9	VIN	DTMF/HOLD Signal Input	The signal entered to this pin is send to line when voltage of this pin is over 1.4 V.
10	BT	Backtone Input	The signal entered to this pin is send to receiver when voltage of this pin is over 1.4 V.
11	AGC	AGC	When this pin is connected with pin ⑬, sending, receiver gain and sending gain of DTMF/HOLD are automatically adjusted to forward line current. And gain is fixed when voltage of this pin is constant.
12	GRCT	Receiver Gain Control	As resistance connected with this pin is smaller, receiver gain is larger.
13	BRG2	Line Voltage Detection	Voltage of this is proportional to line voltage.
14	Vcc	Reference	Connect with ceramic mike via a resistance.
15	ILDET	Line Current Detection	Current proportional to line current through this pin. So, power dissipation of resistance is needed over 1/2 W.
16	BRG1	Shunt Input	This pin is connected to L1 through resistance. Power dissipation of this resistance is needed over 1/2 W.

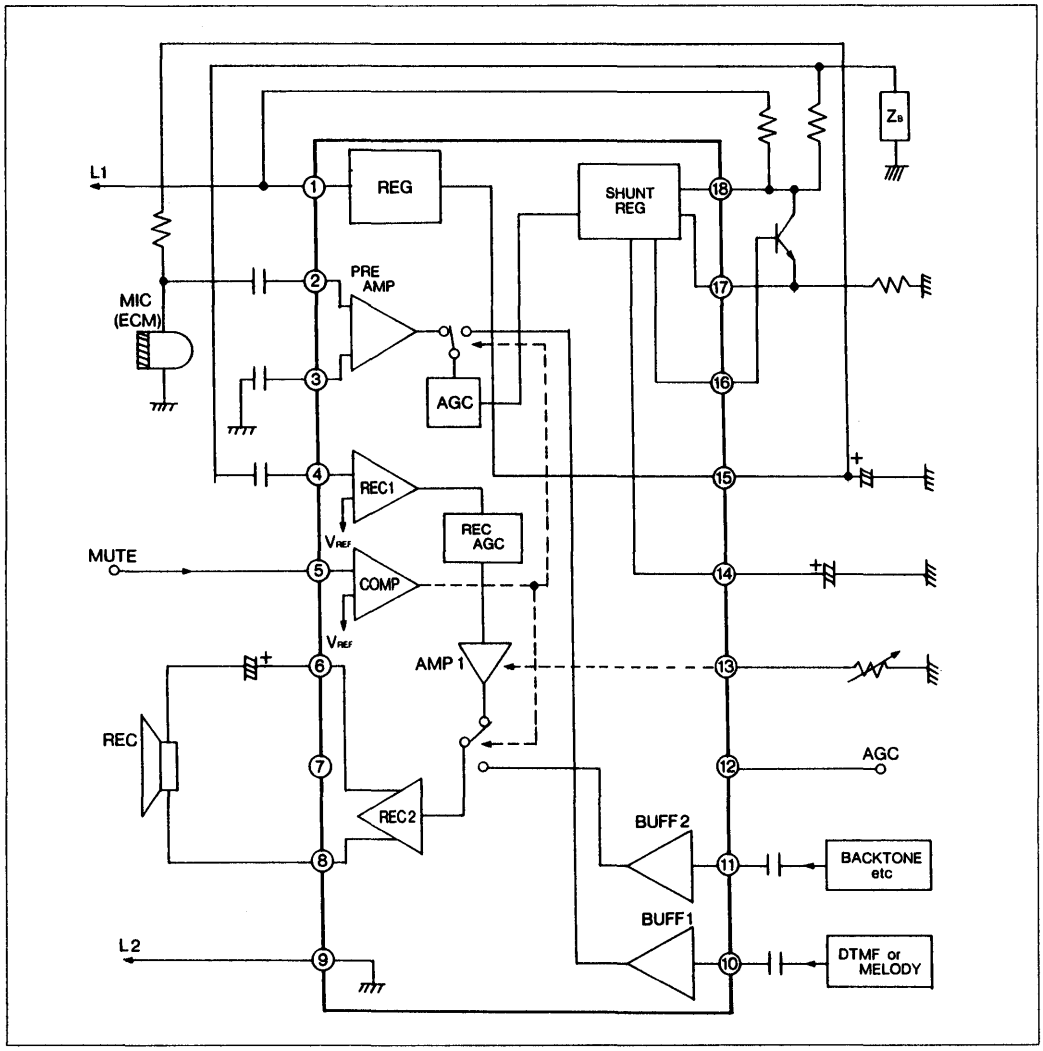
Block Diagram (HA16821MP)



Pin Description (HA16821MP)

Pin No.	Symbol	Pin Description	
1	V_L	Line Input	Connect with plus-output of diode bridge circuit.
2	MIC1	Mike Input	This pin is a signal-input pin from mike. Input impedance is 30 kΩ typ.
3	MIC2	Mike Input	This pin is input of mike pre-amplifier. Input impedance is 30 kΩ typ. To suppress oscillation, connect capacitor.
4	BRG3	Receiver Input	This pin is input of receiver pre-amplifier. Adjust balancing network Z_B to restrain from sidetone.
5	MUTE	MUTE	This IC becomes DTMF/HOLD mode when voltage of this pin is over 1.4 V.
6	NC	NC	No connect
7	REC2	Receiver Output	Connect to dynamic receiver.
8	REC1	Receiver Output	Connect to dynamic receiver.
9	L2	Line (GND)	Connect with minus-output of diode bridge circuit.
10	VIN	DTMF/HOLD Signal Input	The signal entered to this pin is send to line when voltage of this pin is over 1.4 V.
11	BT	Backtone Input	The signal entered to this pin is send to receiver when voltage of this pin is over 1.4 V.
12	AGC	AGC	When this pin is connected with pin ⑭, sending, receiver gain and sending gain of DTMF/HOLD are automatically adjusted to forward line current. And gain is fixed when voltage of this pin is constant.
13	GRCT	Receiver Gain Control	As resistance connected with this pin is smaller, receiver gain is larger.
14	BRG2	Line Voltage Detection	Voltage of this is proportional to line voltage.
15	NC	NC	No connect
16	Vcc	Reference	Connect with ceramic mike via a resistance.
17	ILDET	Line Current Detection	Current proportional to line current through this pin. So, power dissipation of resistance is needed over 1/2 W.
18	BRG1	Shunt Input	This pin is connected to L1 through resistance. Power dissipation of this resistance is needed over 1/2 W.

Block Diagram (HA16821F)



Pin Description (HA16821F)

Pin No.	Symbol	Pin Description	
1	V_L	Line Input	Connect with plus-output of diode bridge circuit.
2	MIC1	Mike Input	This pin is a signal-input pin from mike. Input impedance is 30 kΩ typ.
3	MIC2	Mike Input	This pin is input of mike pre-amplifier. Input impedance is 30 kΩ typ. To suppress oscillation, connect capacitor.
4	BRG3	Receiver Input	This pin is input of receiver pre-amplifier. Adjust balancing network Z_B to restrain from sidetone.
5	MUTE	MUTE	This IC becomes DTMF/HOLD mode when voltage of this pin is over 1.4 V.
6	REC2	Receiver Output	Connect to dynamic receiver.
7	NC	NC	No connect
8	REC1	Receiver Output	Connect to dynamic receiver.
9	L2	Line (GND)	Connect with minus-output of diode bridge circuit.
10	VIN	DTMF/HOLD Signal Input	The signal entered to this pin is send to line when voltage of this pin is over 1.4 V.
11	BT	Backtone Input	The signal entered to this pin is send to receiver when voltage of this pin is over 1.4 V.
12	AGC	AGC	When this pin is connected with pin ⑭, sending, receiver gain and sending gain of DTMF/HOLD are automatically adjusted to forward line current. And gain is fixed when voltage of this pin is constant.
13	GRCT	Receiver Gain Control	As resistance connected with this pin is smaller, receiver gain is larger.
14	BRG2	Line Voltage Detection	Voltage of this is proportional to line voltage.
15	Vcc	Reference	Connect with ceramic mike via a resistance.
16	SHTRS	Shunt Output	This is connected to base of external transistor. Almost of line current flow through this transistor.
17	ILDET	Line Current Detection	Current proportional to line current through this pin. So, power dissipation of resistance is needed over 1/2 W.
18	BRG1	Shunt Input	This pin is connected to L1 through resistance. Power dissipation of this resistance is needed over 1/2 W.

Functional Description

DTMD/HOLD Interface:

The DTMF/HOLD sending mode is activated when pin⑤becomes 1.4 V or more (threshold is 1.2 V typ.). In this mode, the sending and receiving input amp. are off and the buffer amp. 1, 2 are on and the DTMF/HOLD signal is sent out the line.

The DTMF/HOLD signal is input to pin⑨(⑩).

However, since it has a bias of about 1 V, and AC couple (Cex8) is required.

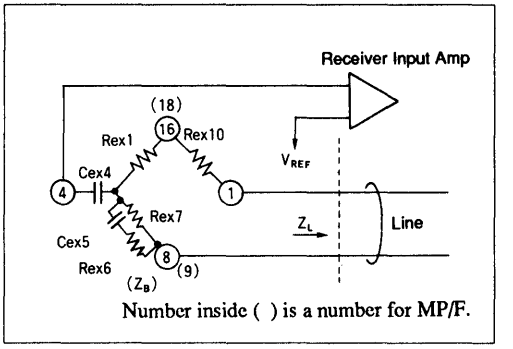
Input level of from 50 to 70mVrms is appropriate since the sending gain is a little over 20 dB. When DTMF/HOLD signal is input to pin ⑩ (⑪), backtone is generated from receiver.

Sidetone Suppression Circuit:

Sidetone suppression circuit is constructed with bridge-type resistance. To suppress sidetone Z_B is adjusted by the following equation in response to line impedance Z_L.

$$\frac{Rex1}{Rex10} = \frac{Z_B}{Z_L}$$

Receive gain is increased by increasing resistance while maintaining a Rex1/Rex10 ratio. For example, when Rex1/ Rex10 = 330Ω/30Ω, receiver gain is increased by about 6 dB over that when Rex1/Rex10 = 110Ω/10Ω.

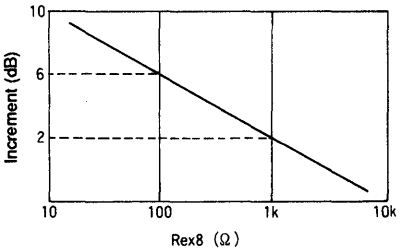


Number inside ( ) is a number for MP/F.

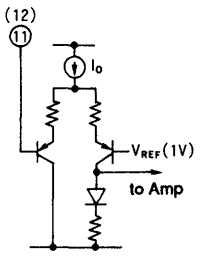
Receiving Gain Variable:

Receiving gain is increased by lowing Rex8.

For example, when Rex8 = 100Ω, receiving gain is increased by about 6 dB over that when pin ⑫ (⑬) is open. In some modes receiving gain adjust-function is automatically set to off.



Mode	Speech	Dialing (DTMF Sending)
On	On	Off
Off		



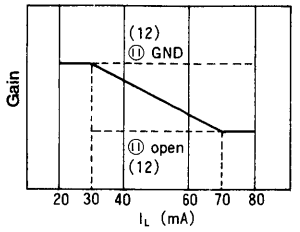
Number inside ( ) is a number for MP/F.

AGC Characteristics (line Compensation):

By connecting pin ⑪ (⑫) and ⑬ (⑭) sending and receiving gain, DTMF and melody sending gain are automatically adjust to coincide with line current.

The gain fixed mode is set by disconnecting pin ⑬ (⑭) and applying a constant voltage to pin ⑪ (⑫).

High gain fixed when $0V \leq V$ ⑪ (⑫) ≤ 0.3 V, low gain fixed when V ⑪ (⑫) = V ① or open. Gain changes when I_L is from 30 mA to 70 mA.



Number inside ( ) is a number for MP/F.

Line current Detection:

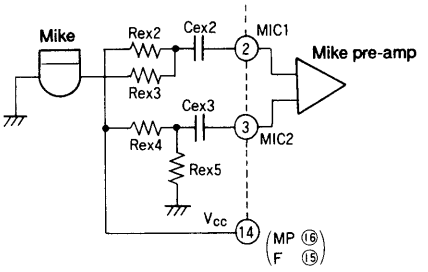
Line current is detected by Rex9 of pin ⑮ (⑰).

The voltage of pin ⑬ (⑭) is V ⑬ (⑭) = V ⑮ (⑰) +0.3 V.

The line matching impedance is proportional to the Rex9. $Z_{IN} \propto$ Rex9.

Mike Bias:

Mike bias is provided for capacitor mike. Pin ⑭ (MP: ⑯, F: ⑮) Vcc is used for mike bias source. This Vcc is 1.8 V typ. and the Rex2, 3, 4, 5 of which is determined by the type of mike used. This signal from the mike is input to mike pre-amplifier through Cex2.



Number inside ( ) is a number for MP/F.

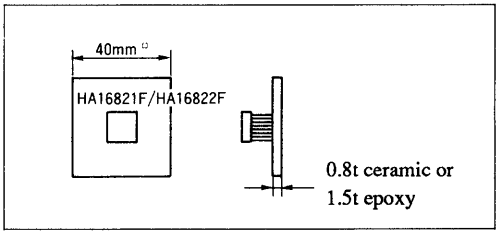
Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings			Unit	Notes
		HA16821P	HA16821MP	HA16821F		
Supply Voltage	V_L	15	15	15	V	1
Supply Current	I_L	120	120	120	mA	
Operating Temperature Range	Topr	–20 to +70	–20 to +70	–20 to +70	°C	
Storage Temperature Range	Tstg	–55 to +125	–55 to +125	–55 to +125	°C	
Power Dissipation	P_T	720	720	390	mW	2

Note 1) 3ms Pulse duration (Keep the duration to be more than 3 sec.)

Note 2) Value at Ta ≤ 70°C, when Ta is more than 70°C, 7.14 mW/°C derating shall be performed. (Condition: glass epoxy with 30% metallization density)

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

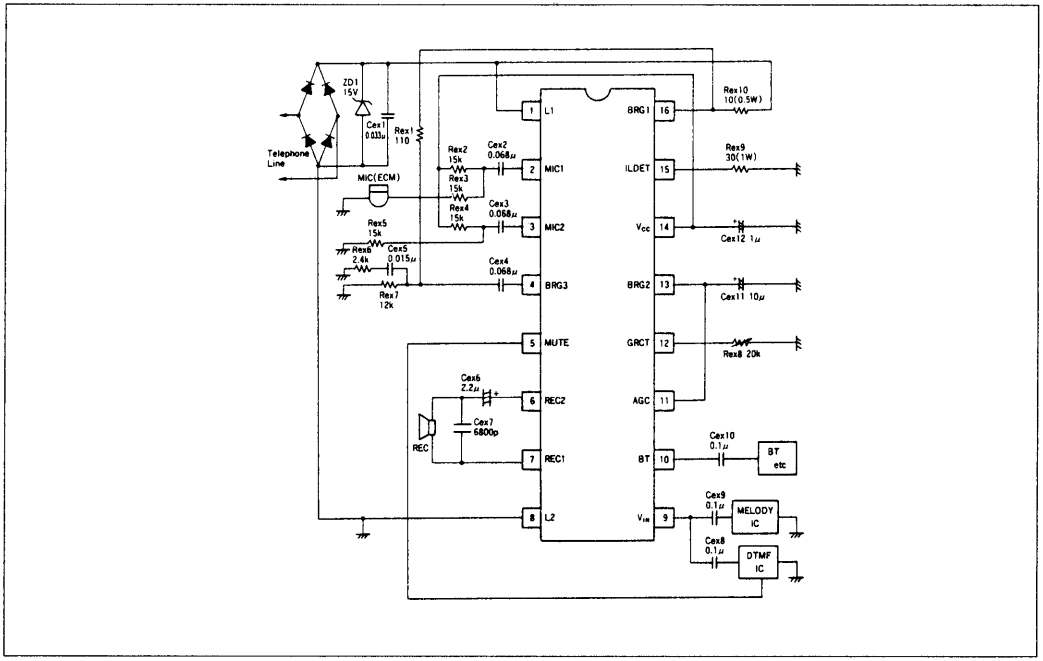


Electrical Characteristics (Ta = 25°C)

Item		Symbol	Test Conditions		Min	Typ	Max	Unit
			I_L mA					
Line Voltage	Speaking	V_L	20		2.5	2.85	3.3	V
			80		5.6	6.8	8.0	V
	Dialing		20		3.6	4.0	4.4	V
			80		6.8	8.0	9.2	V
Reference	Voltage	V_{DD}	20		1.6	1.8	2.0	V
	Current	I_{DD}	20	V_{DD} = 1.6 V	0.15	0.3		mA
Mute Current	Stand-by	I_M	20	V = 0.9 V	–5	0	5	µA
	Mute		20	V = 1.5 V		1	10	µA
Mute	Stand-by	V_{TH}	20				0.9	V
threshold	Mute		20		1.4			V
V_{IN} Input Impedance		Z_{VIN}	20		20k	30k		Ω
BT Input Impedance		Z_{BT}	20		20k	30k		Ω
MIC Input Impedance		Z_{MIC}	20		20k	30k		Ω
Line Matching Impedance		Z_{IN}	20	f = 1 kHz	480	600	720	Ω
			80		480	600	720	Ω
Sending Gain		G_T	30	f = 1 kHz	38	41	44	dB
			80		32	35	38	dB
Receiving Gain		G_R	30	f = 1 kHz	–7	–4	–1	dB
			80		–12	–9	–6	dB
DTMF/HOLD Sending Gain		G_{MF}	30	f = 1 kHz	21	24	27	dB
			80		18	21	24	dB
BT Sending Gain		G_{BT}	30	f = 1 kHz	–15	–11.5	–8	dB
			80		–15	–11.5	–8	dB
Sending Dynamic Range*		DR_T	30	f = 1 kHz	2.4			Vp-p
			80		3.5			Vp-p
Receiving Dynamic Range*		DR_R	30	f = 1 kHz	0.6			Vp-p
			80		0.7			Vp-p
DTMF/HOLD Dynamic		DR_{MF}	30	f = 1 kHz	2.5			Vp-p
Range*			80		3			Vp-p

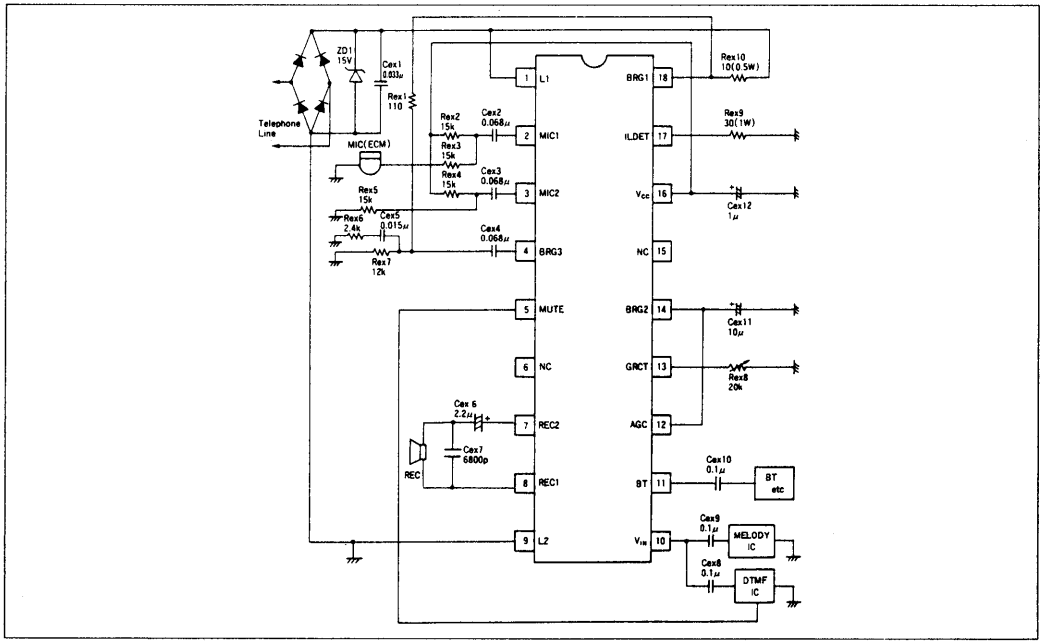
* Distortion ratio : 5%

Pin Arrangement and Application Circuit (HA16821P)



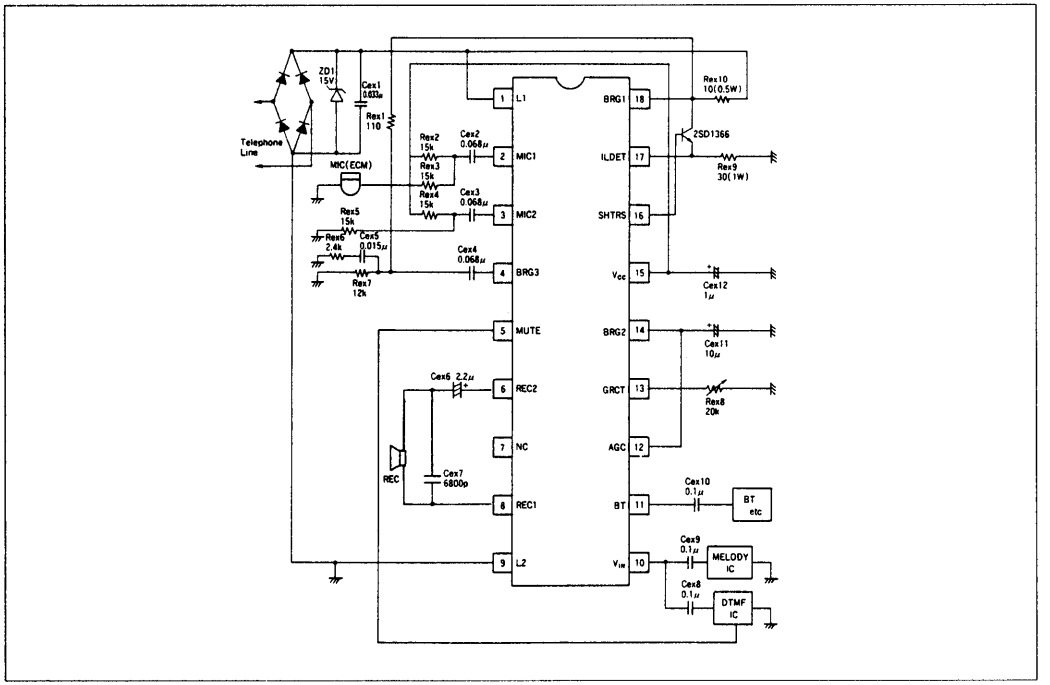
Note 1) Externalized components are example.
Unit: R; Ω, C; F

Pin Arrangement and Application Circuit (HA16821MP)



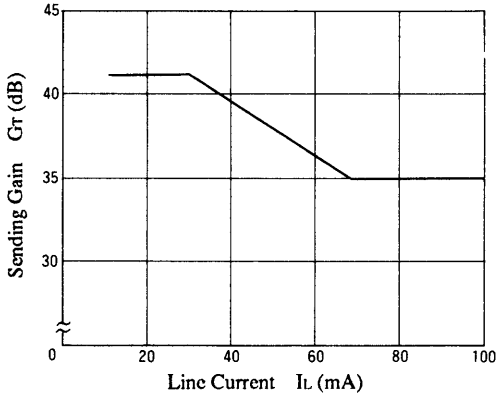
Note 1) Externalized components are example.
Unit : R; Ω, C; F

Pin Arrangement and Application Circuit (HA16821F)

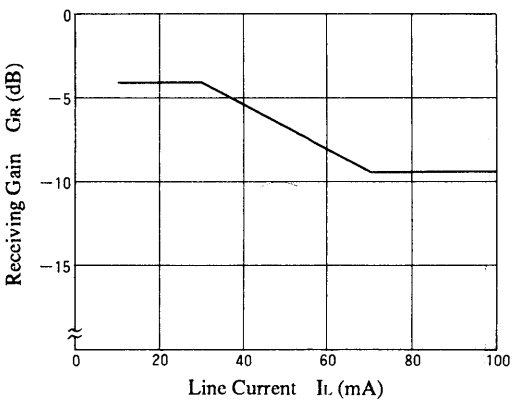


Note 1) Externalized components are example.
Unit: R; Ω, C; F

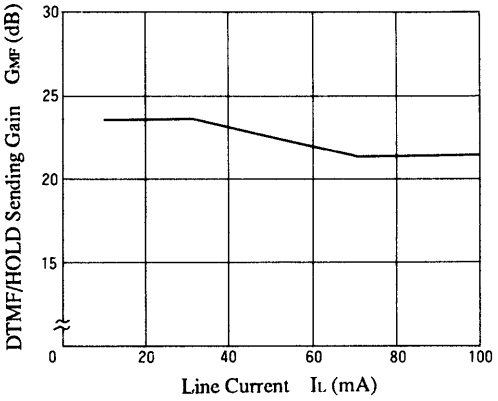
Sending Gain vs. Line Current



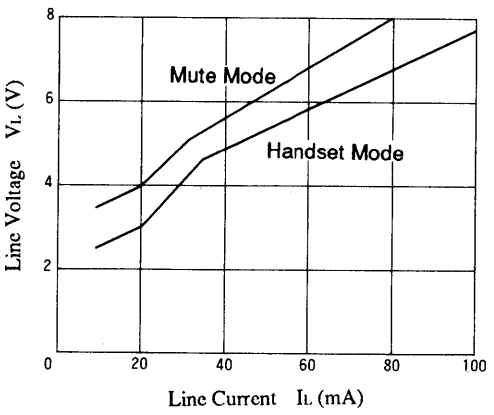
Receiving Gain vs. Line Current



DTMF/HOLD Sending Gain vs. Line Current



Line Voltage vs. Line Current



HA16822P/HA16822MP/HA16822F — Preliminary

Speech Network IC for Telephone Sets

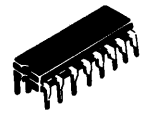
Description

The HA16822 realizes an excellent branching performance by achieving low current dissipation and low voltage operation as speech network IC. It is possible to send DTMF signal or backtone to line or receiver. Moreover there are three kinds of packages.

Features

- Low current dissipation, low voltage operation. (3 mA, 1.5 V)
- Possible of direct interface to light, small ceramic transmitter and receiver.
- Possible of auto gain control cope with line current. (AGC)
- DTMF signal can be send to line and backtone can be send to receiver.
- Built in regulator to bias of small ceramic transmitter.

HA16822P

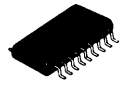


DP-16

HA16822MP

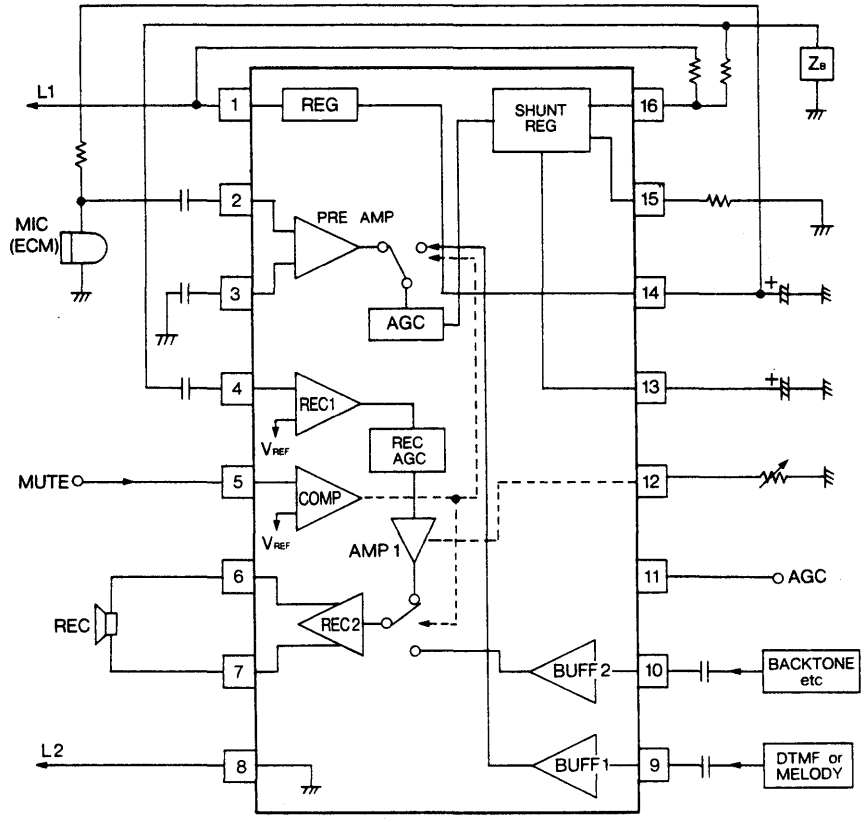
MP-18

HA16822F



FP-18D

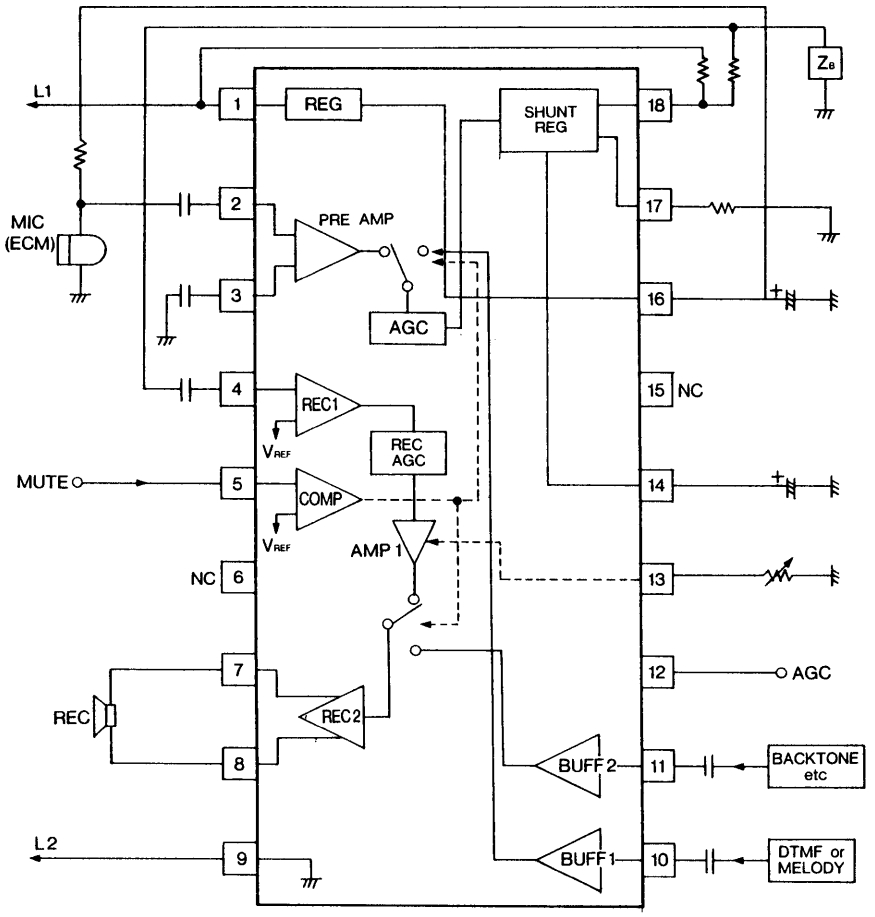
Block Diagram (HA16822P)



Pin Description (HA16822P)

Pin No.	Symbol	Pin Description	
1	V_L	Line Input	Connect with plus-output of diode bridge circuit.
2	MIC1	Mike Input	This pin is a signal-input pin from mike. Input impedance is 30 kΩ typ.
3	MIC2	Mike Input	This pin is input of mike pre-amplifier. Input impedance is 30 kΩ typ. To suppress oscillation, connect capacitor.
4	BRG3	Receiver Input	This pin is input of receiver pre-amplifier. Adjust balancing network Z_B to restrain from sidetone.
5	MUTE	MUTE	This IC becomes DTMF/HOLD mode when voltage of this pin is over 1.4 V.
6	REC2	Receiver Output	Connect directory to ceramic receiver.
7	REC1	Receiver Output	Connect directory to ceramic receiver.
8	L2	Line (GND)	Connect with minus-output of diode bridge circuit.
9	VIN	DTMF/HOLD Signal Input	The signal entered to this pin is send to line when voltage of this pin is over 1.4 V.
10	BT	Backtone Input	The signal entered to this pin is send to receiver when voltage of this pin is over 1.4 V.
11	AGC	AGC	When this pin is connected with pin ⑬, sending, receiver gain and sending gain of DTMF/HOLD are automatically adjusted to forward line current. And gain is fixed when voltage of this pin is constant.
12	GRCT	Receiver Gain Control	As resistance connected with this pin is smaller, receiver gain is larger.
13	BRG2	Line Voltage Detection	Voltage of this is proportional to line voltage.
14	Vcc	Reference	Connect with ceramic mike via a resistance.
15	ILDET	Line Current Detection	Current proportional to line current through this pin. So, power dissipation of resistance is needed over 1/2 W.
16	BRG1	Shunt Input	This pin is connected to L1 through resistance. Power dissipation of this resistance is needed over 1/2 W.

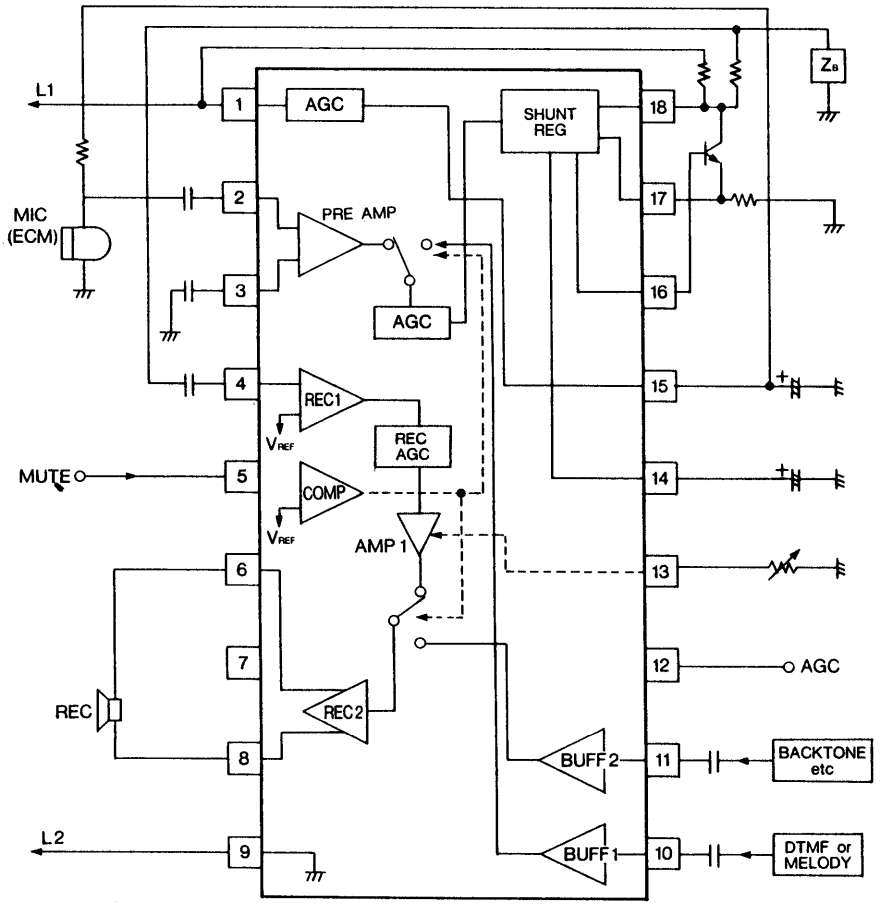
Block Diagram (HA16822MP)



Pin Description (HA16822MP)

Pin No.	Symbol	Pin Description	
1	V_L	Line Input	Connect with plus-output of diode bridge circuit.
2	MIC1	Mike Input	This pin is a signal-input pin from mike. Input impedance is 30 kΩ typ.
3	MIC2	Mike Input	This pin is input of mike pre-amplifier. Input impedance is 30 kΩ typ. To suppress oscillation, connect capacitor.
4	BRG3	Receiver Input	This pin is input of receiver pre-amplifier. Adjust balancing network Z_B to restrain from sidetone.
5	MUTE	MUTE	This IC becomes DTMF/HOLD mode when voltage of this pin is over 1.4 V.
6	NC	NC	No connect
7	REC2	Receiver Output	Connect directory to ceramic receiver.
8	REC1	Receiver Output	Connect directory to ceramic receiver.
9	L2	Line (GND)	Connect with minus-output of diode bridge circuit.
10	VIN	DTMF/HOLD Signal Input	The signal entered to this pin is send to line when voltage of this pin is over 1.4 V.
11	BT	Backtone Input	The signal entered to this pin is send to receiver when voltage of this pin is over 1.4 V.
12	AGC	AGC	When this pin is connected with pin ⑭, sending, receiver gain and sending gain of DTMF/HOLD are automatically adjusted to forward line current. And gain is fixed when voltage of this pin is constant.
13	GRCT	Receiver Gain Control	As resistance connected with this pin is smaller, receiver gain is larger.
14	BRG2	Line Voltage Detection	Voltage of this is proportional to line voltage.
15	NC	NC	No connect
16	Vcc	Reference	Connect with ceramic mike via a resistance.
17	ILDET	Line Current Detection	Current proportional to line current through this pin. So, power dissipation of resistance is needed over 1/2 W.
18	BRG1	Shunt Input	This pin is connected to L1 through resistance. Power dissipation of this resistance is needed over 1/2 W.

Block Diagram (HA16822F)



Pin Description (HA16822F)

Pin No.	Symbol	Pin Description	
1	V_L	Line Input	Connect with plus-output of diode bridge circuit.
2	MIC1	Mike Input	This pin is a signal-input pin from mike. Input impedance is 30 kΩ typ.
3	MIC2	Mike Input	This pin is input of mike pre-amplifier. Input impedance is 30 kΩ typ. To suppress oscillation, connect capacitor.
4	BRG3	Receiver Input	This pin is input of receiver pre-amplifier. Adjust balancing network Z_B to restrain from sidetone.
5	MUTE	MUTE	This IC becomes DTMF/HOLD mode when voltage of this pin is over 1.4 V.
6	REC2	Receiver Output	Connect directory to ceramic receiver.
7	NC	NC	No connect
8	REC1	Receiver Output	Connect directory to ceramic receiver.
9	L2	Line (GND)	Connect with minus-output of diode bridge circuit.
10	VIN	DTMF/HOLD Signal Input	The signal entered to this pin is send to line when voltage of this pin is over 1.4 V.
11	BT	Backtone Input	The signal entered to this pin is send to receiver when voltage of this pin is over 1.4 V.
12	AGC	AGC	When this pin is connected with pin ⑭, sending, receiver gain and sending gain of DTMF/HOLD are automatically adjusted to forward line current. And gain is fixed when voltage of this pin is constant.
13	GRCT	Receiver Gain Control	As resistance connected with this pin is smaller, receiver gain is larger.
14	BRG2	Line Voltage Detection	Voltage of this is proportional to line voltage.
15	Vcc	Reference	Connect with ceramic mike via a resistance.
16	SHTRS	Shunt Output	This is connected to base of external transistor. Almost of line current flow through this transistor.
17	ILDET	Line Current Detection	Current proportional to line current through this pin. So, power dissipation of resistance is needed over 1/2 W.
18	BRG1	Shunt Input	This pin is connected to L1 through resistance. Power dissipation of this resistance is needed over 1/2 W.

Functional Description

DTMF/HOLD Interface:

The DTMF/HOLD sending mode is activated when pin⑤becomes 1.4 V or more (threshold is 1.2 V typ.). In this mode, the sending and receiving input amp. are off and the buffer amp. 1, 2 are on and the DTMF/HOLD signal is sent out the line.

The DTMF/HOLD signal is input to pin ⑨ (⑩). However, since it has a bias of about 1 V, and AC couple (Cex8) is required.

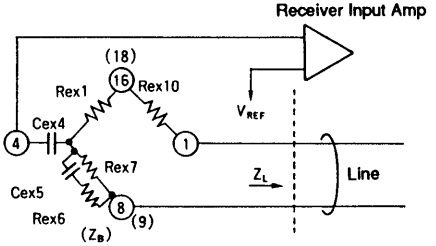
Input level of from 50 to 70mVrms is appropriate since the sending gain is a little over 20 dB. When DTMF/HOLD signal is input to pin ⑩ (⑪), backtone is generated from receiver.

Sidetone Suppression Circuit:

Sidetone suppression circuit is constructed with bridge-type resistance. To suppress sidetone Z_B is adjusted by the following equation in response to line impedance Z_L.

$$\frac{Rex1}{Rex10} = \frac{Z_B}{Z_L}$$

Receive gain is increased by increasing resistance while maintaining a Rex1/Rex10 ratio. For example, when Rex1/Rex10 = 330Ω/30Ω, receiver gain is increased by about 6 dB over that when Rex1/Rex10 = 110Ω/10Ω.

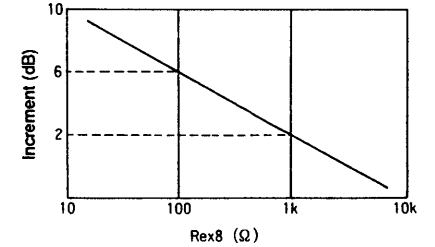


Number inside ( ) is a number for MP/F.

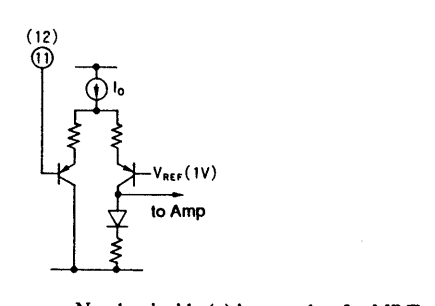
Receiving Gain Variable:

Receiving gain is increased by lowing Rex8.

For example, when Rex8 = 100Ω, receiving gain is increased by about 6 dB over that when pin ⑫ (⑬) is open. In some modes receiving gain adjust-function is automatically set to off.



Mode	Speech	Dialing (DTMF Sending)
On Off	On	Off



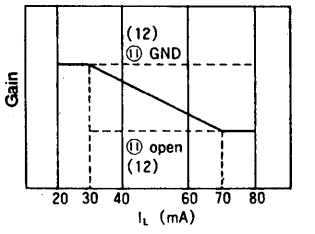
Number inside ( ) is a number for MP/F.

AGC Characteristics (line Compensation):

By connecting pin ⑪ (⑫) and ⑬ (⑭) sending and receiving gain, DTMF and melody sending gain are automatically adjust to coincide with line current.

The gain fixed mode is set by disconnecting pin ⑬ (⑭) and applying a constant voltage to pin ⑪ (⑫).

High gain fixed when $0V \leq V_{⑪\,(⑫)} \leq 0.3$ V, low gain fixed when $V_{⑪\,(⑫)} = V_{①}$ or open. Gain changes when I_L is from 30 mA to 70 mA.



Number inside ( ) is a number for MP/F.

Line current Detection:

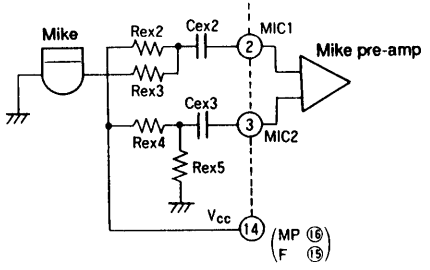
Line current is detected by Rex9 of pin ⑮ (⑰).

The voltage of pin ⑬ (⑭) is $V_{⑬\,(⑭)} = V_{⑮\,(⑰)} + 0.3$ V.

The line matching impedance is proportional to the Rex9. $Z_{IN} \propto$ Rex9.

Mike Bias:

Mike bias is provided for capacitor mike. Pin ⑭ (MP: ⑯, F: ⑮) V_{CC} is used for mike bias source. This V_{CC} is 1.2 V typ. and the Rex2, 3, 4, 5 of which is determined by the type of mike used. This signal from the mike is input to mike pre-amplifier through Cex2.



Number inside ( ) is a number for MP/F.

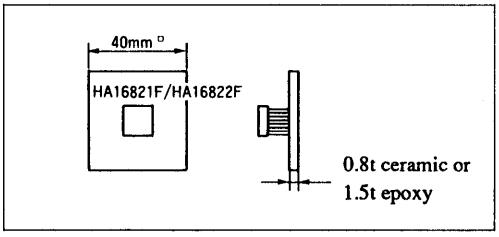
Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings			Unit	Notes
		HA16822P	HA16822MP	HA16822F		
Supply Voltage	V_L	15	15	15	V	1
Supply Current	I_L	120	120	120	mA	
Operating Temperature Range	Topr	–20 to +70	–20 to +70	–20 to +70	°C	
Storage Temperature Range	Tstg	–55 to +125	–55 to +125	–55 to +125	°C	
Power Dissipation	P_T	720	720	390	mW	2

Note 1) 3ms Pulse duration (Keep the duration to be more than 3 sec)

Note 2) Value at Ta ≤ 70°C, when Ta is more than 70°C, 7.14 mW/°C derating shall be performed. (Condition: glass epoxy with 30% metallization density)

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

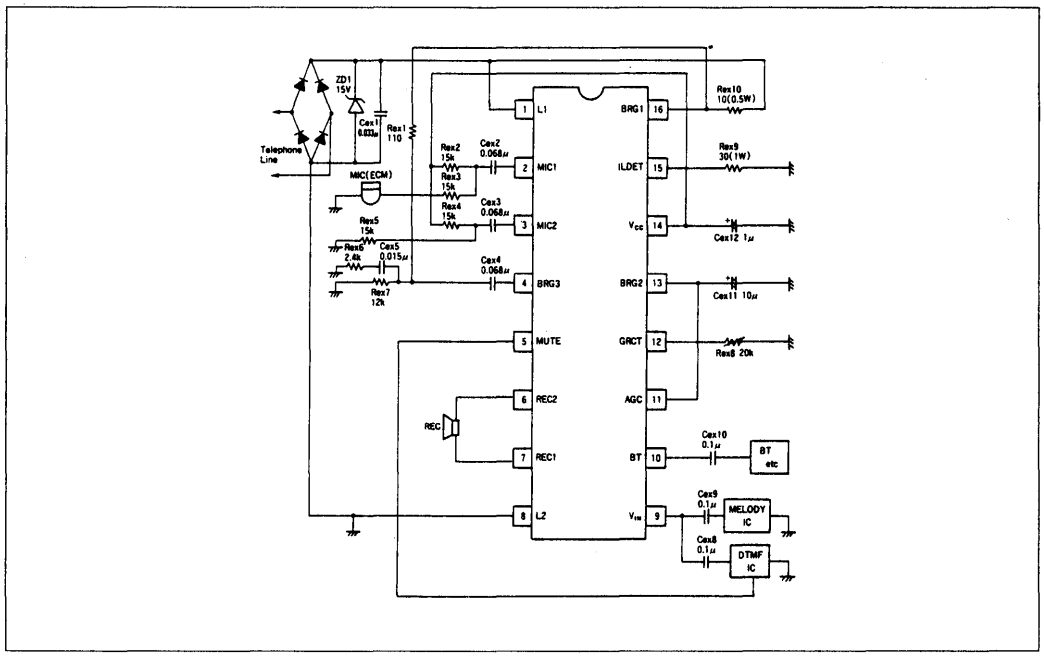


Electrical Characteristics (Ta = 25°C)

Item		Symbol	Test Conditions I_L mA		Min	Typ	Max	Unit
Line Voltage	Speaking	V_L	20		2.5	2.8	3.3	V
			80		5.6	6.8	8.0	V
	Dialing		20		3.6	4.0	4.4	V
			80		6.8	8.0	9.2	V
Reference	Voltage	V_{DD}	20		1.0	1.2	1.4	V
	Current	I_{DD}	20	V_{DD} = 1.2 V	0.2	0.3		mA
Mute Current	Stand-by	I_M	20	V = 0.9 V	–5	0	5	μA
	Mute		20	V = 1.5 V		1	10	μA
Mute threshold	Stand-by	V_{TH}	20				0.9	V
	Mute		20		1.4			V
V_{IN} Input Impedance		Z_{VIN}	20		20k	30k		Ω
BT Input Impedance		Z_{BT}	20		20k	30k		Ω
MIC Input Impedance		Z_{MIC}	20		20k	30k		Ω
Line Matching Impedance		Z_{IN}	20	f = 1 kHz	480	600	720	Ω
			80		480	600	720	Ω
Sending Gain		G_T	30	f = 1 kHz	38	41	44	dB
			80		32	35	38	dB
Receiving Gain		G_R	30	f = 1 kHz	9	12	15	dB
			80		4	7	10	dB
DTMF/HOLD Sending Gain		G_{MF}	30	f = 1 kHz	21	24	27	dB
			80		18	21	24	dB
BT Sending Gain		G_{BT}	30	f = 1 kHz	0.5	3.5	6.5	dB
			80		0.5	3.5	6.5	dB
Sending Dynamic Range*		DR_T	30	f = 1 kHz	2.4			Vp-p
			80		3.5			Vp-p
Receiving Dynamic Range*		DR_R	30	f = 1 kHz	3.5	4.5		Vp-p
			80		4	5		Vp-p
DTMF/HOLD Dynamic Range*		DR_{MF}	30	f = 1 kHz	2.5			Vp-p
			80		3			Vp-p

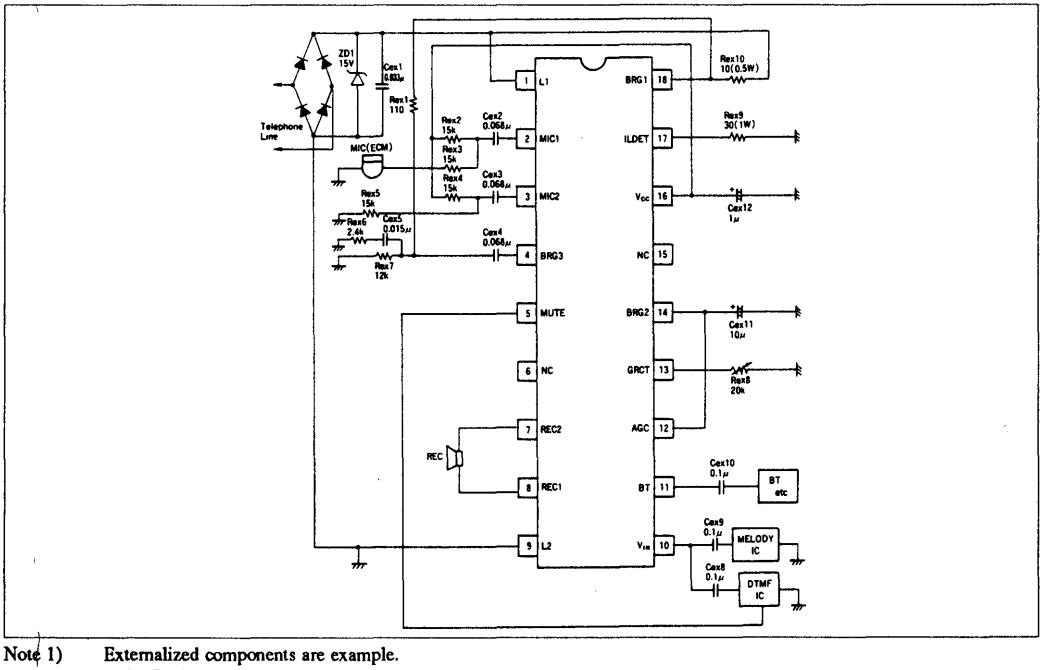
* Distortion ratio : 5%

Pin Arrangement and Application Circuit (HA16822P)



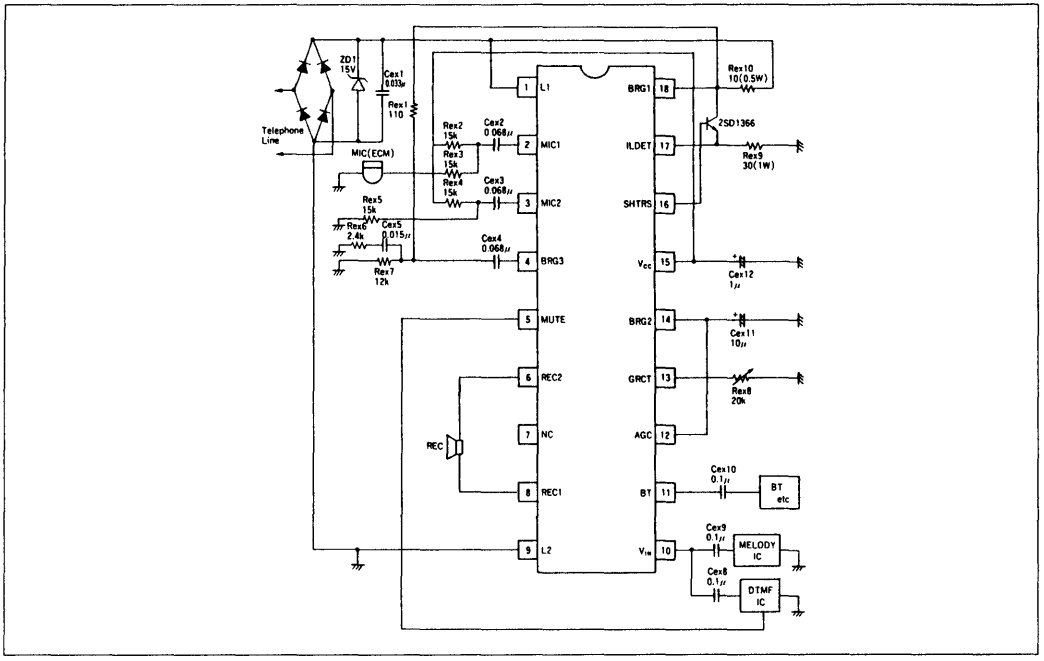
Note 1) Externalized components are example.
Unit: R; Ω, C; F

Pin Arrangement and Application Circuit (HA16822MP)



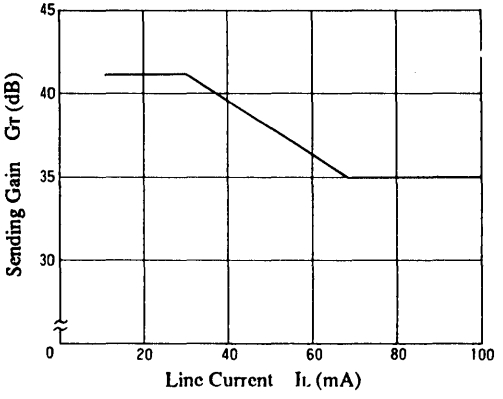
Note 1) Externalized components are example.
Unit: R; Ω, C; F

Pin Arrangement and Application Circuit (HA16822F)

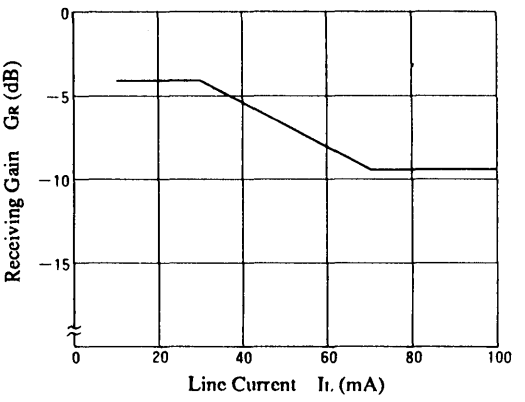


Note 1) Externalized components are example.
Unit : R; Ω, C; F

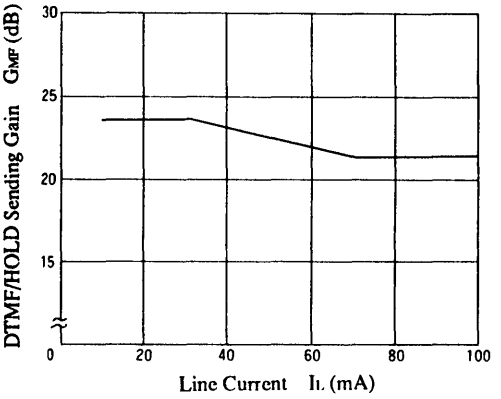
Sending Gain vs. Line Current



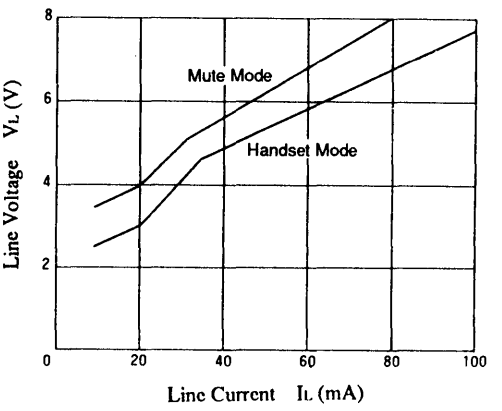
Receiving Gain vs. Line Current



DTMF/HOLD Sending Gain vs. Line Current



Line Voltage vs. Line Current

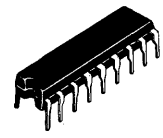


HD61825A/B Series

Pulse Dialer with Redial

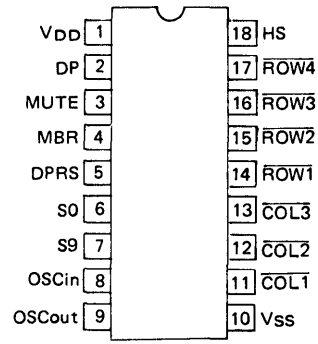
▪ FEATURES

- Direct telephone-line operation.
- Low power and low voltage operation by CMOS process.
- Uses either a standard 2-of-7 keyboard or the inexpensive matrix keyboard
- Stable operation by using ceramic resonator.
- Make/Break ratio pin-selectable
- 10 pps/20 pps pin-selectable
- Redial function (# key)
- Pause input (# key)
- Selectable of mute output
  - Mute (continuous) HD61825A
  - Mute (each digit) HD61825B
- 0 dialing in inhibition pin
  9 dialing in inhibition pin
- 23-digit dial memory
- Dial memory overflow protection (inhibit redial)
- On chip power supply voltage sense circuit
  - Reset voltage
  - Memory clear voltage



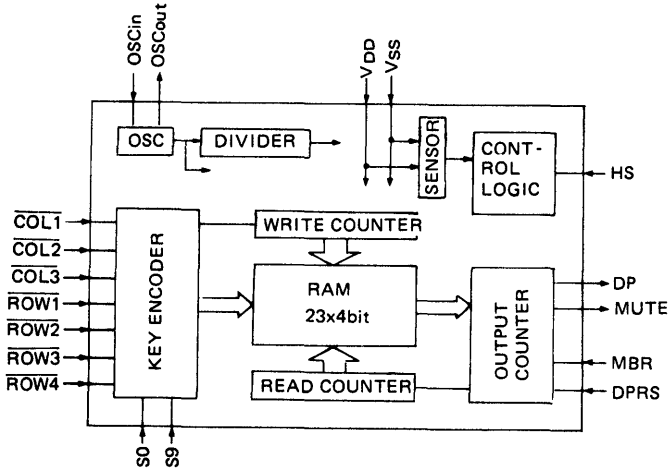
(DP-18)

▪ PIN ASSIGNMENT



(Top View)

▪ BLOCK DIAGRAM



▪ ABSOLUTE MAXIMUM RATINGS (Vss= 0V)

Item	Symbol	Value	Unit
Power supply voltage	V_{DD}	5.5	V
Terminal voltage	V_T	V_{SS} −0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage tmperature	Tstg	−55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

▪ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{SS}= 0V, V_{DD} = 2.0 to 5.0V, Ta = −20 to +75°C)

Item	Symbol	Test condition	min.	typ.*1	max.	Unit
Operating voltage	V_{DD}		1.7	–	5.0	V
Reset voltage	V_{DR}		–	1.5	–	V
Memory clear voltage	V_{DC}		–	1.15	–	V
Operating current	I_{DD}		–	170	–	μA
Memory hold (reset) current	I_{DR}		–	0.5	–	μA
Input High voltage	V_{IH}	except HS pin	80%V_{DD}	–	–	V
Input High voltage	V_{IH}	HS pin V_{DD} = 3.0 to 5.0V	90%V_{DD}	–	–	V
Input High voltage	V_{IH}	HS pin V_{DD} = 2.0 to 3.0V	V_{DD}−0.1	–	–	V
Input Low voltage	V_{IL}	HS pin V_{DD} = 2.0 to 5.0V	–	–	20%V_{DD}	V
Input Low voltage	V_{IL}		–	–	20%V_{DD}	V
Input leak current	$\|I_{IN}\|$	Pull up MOS off, V_{IN}=0 to V_{DD}	–	–	1	μA
Input Pull up MOS current	$-I_P$	V_{IN} = 0, ($\overline{MBR}$, DPRS, S0, S9, $\overline{ROW}$, $\overline{COW}$, HS)	–	10	–	μA
Output High voltage	V_{OH}	$-I_{OH}$ = 0.1 mA (DP, MUTE)	V_{DD}−0.5	–	–	V
Output Low voltage	V_{OL}	I_{OL} = 0.1 mA ($\overline{ROW}$, $\overline{COL}$)	–	–	0.3	V
Open drain output leak current	I_{OL}	V_{IN} = V_{DD} (DP, MUTE)	–	–	1	μA

• AC Characteristics (V_{SS} = 0V, V_{DD}= 2.0 to 5.0V, Ta = −20 to +75°C)

Item	Symbol	Test condition	min.	typ.*1	max.	Unit
Oscillation frequency	fosc		396	400	404	kHz
Oscillation start up time	t_{str}		–	5	–	ms

*1 Typ. value is the design value (the standard value at V_{DD} = 2.5V and Ta = 25°C)

▪ DESCRIPTION

HD61825 is a CMOS IC for button telephone and converts keyboard inputs into the dial pulse signal. Using low-voltage and low-power consumption CMOS process, it can operate directly from the telephone line and interfaces with the telephone line by loop-disconnect signal (DP output). Besides, it has MUTE output to mute the receiver during the sending pulses. In the HD61825, ON HOOK/OFF HOOK is detected by the HS pin.

Further, while the supply voltage is less than reset voltage, even if the HS is OFF HOOK, the HD61825 will be ON HOOK state of inhibition key input. When the power supply voltage is less than memory clear voltage, the internal memory data is cleared.

While the telephone is OFF-HOOK and the supply voltage is more than the reset voltage, the oscillator starts up with a key input and this key input is implemented with the key debounce circuit. In this case, if the first key after the reset (note 1) is other than # and * (note 2), the internal memory data is cleared, and then this input key is encoded and stored into the memory. Then the following keys are stored ordinal into the memory, and also at the same time these keys are converted into the output pulse.

The key input speed is same as that of DTMF telephone because the input data is stored in the memory. The internal memory capacity is 23 digits. When key input are more than 23 digits, the completed key code are cleared (FIFO type memory) and then the new keys are stored into the memory. However, considering the capacity, in the moment while the stored data reach 23 digits, the key input is temporarily neglected.

After dialing, once the HD61825 is reset (note 1) and then is redial mode with the first # key. However, if the 24 or more keys has been dialled previously or the memory has already cleared, it cannot be redial mode. During the redial, any key input is not accepted but after that it can be used as a usual dialer.

The pulse output (DP output) stops with the pause during the redial and the redial starts again with # key. # key is used to insert the pause data in the memory. In the normal dial mode, # key does not influence the output of pulse but is stored in the memory as one digit.

NOTES

1. In the HD61825, the reset means the clearing all logic (counter, etc.) except RAM. HD61825 is reset when the

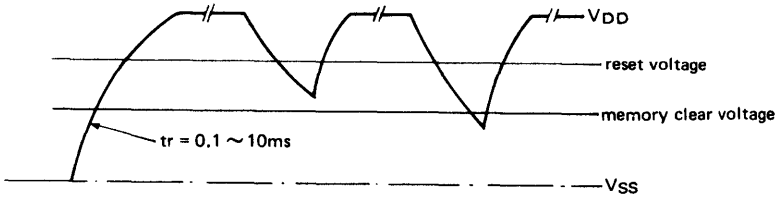
telephone is ON-HOOK or the supply voltage is less than the reset voltage.

2. *key is not used and always neglected in HD61825.

▪ PIN FUNCTIONS

• VDD (Pin 1)

This is a positive voltage supply pin which applies voltage on a basis of the VSS pin. HD61825 provides the internal sense circuit for the supply voltage. To make this circuit operate stable, the following rising time is necessary.

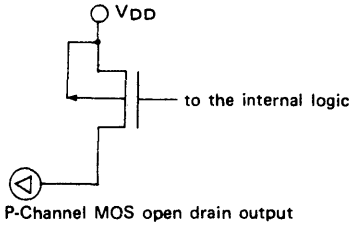


• DP (Pin 2) Dial Pulse

This is a pulse signal output pin for Loop Disconnect. Output circuit is P-Channel MOS open drain.

Break . . . . . High level
Make . . . . . Low level

While reset, the output voltage is held to the low level.

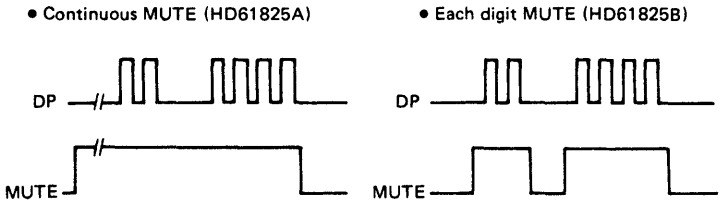


• MUTE (Pin 3)

This is a pin which mute the receiver. Output circuit is P-Channel MOS open drain.

Mute . . . . . High level

While reset, the output voltage is held to the low level. In the HD61825, the following two kinds of MUTE – continuous MUTE and each digit MUTE are selectable. (IC's are different.)

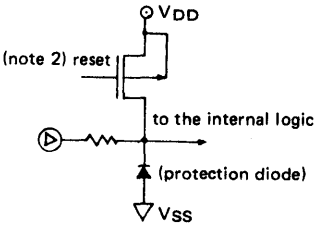


• MBR (Pin 4) Make/Break Ratio

This is a input pin with the pull up MOS to change the Make/Break ratio of DP output. To realize the low power dissipation on reset, the pull up MOS is turned off at the reset. (note 1)

MBR terminal	DP output	
	Make	Break
High (to V_{DD}) or open	33%	67%
Low (to V_{SS})	40%	60%

NOTES:
1. The input pins with the pull up MOS which is turned OFF at the reset, can be applied to MBR, DPRS, S0, S9 and HS.
2. The logic is positive. P MOS is ON with the low voltage and OFF with the high voltage.



Input Pin with Pull up MOS

- **DPRS (Pin 5) Dial Pulse Rate Selection**

This is a input pin to decide the pulse output speed (dial rate). It has a pull up MOS which is turned OFF at the reset.

DPRS terminal	Dial rate
High (to V_{DD}) or open	10 pps
Low (to V_{SS})	20 pps

- **S0, S9 (Pin 6, 7) Selection**

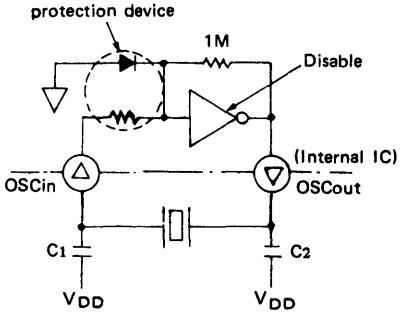
These are input pins to select functions and has pull up MOS which is turned OFF at the reset. The function of this terminal is to prevent the 0 dialing in and the 9 dialing in. When 0 or 9 is pushed after the reset, all the key inputs including the 0 or 9 key become invalid after then. In other words, the signals are not output to DP and MUTE. The telephone is initialized by the reset.

S0 terminal	S9 terminal	Function
High (to V_{DD}) or open	High (to V_{DD}) or open	Normal dialing mode
High (to V_{DD}) or open	Low (to V_{SS})	9 dialing in prevention mode
Low (to V_{SS})	High (to V_{DD}) or open	0 dialing in prevention mode
Low (to V_{SS})	Low (to V_{SS})	Test mode (for testing IC, Do not use.)

- **OSCin, OSCout (Pin 8, 9) Oscillation Input, Output**

These are input pins for the oscillator and constructs the inverter (with disable function to stop the oscillation). Using the ceramic resonator, the frequency is stable in the circuit. Moreover, the oscillator section needs two output capacitors externally. The ceramic oscillator should be 400 kHz and High Q.

Recommended ceramic oscillator
Kyoto Ceramic Co., Ltd. KBR-400H
Murata Co., Ltd. CSB-400
ex. ceramic oscillator KBR-400H
C_1 = 100 pF
C_2 = 470 pF



Oscillation Circuit

- **V_{SS} (Pin 10)**

Negative power supply pin

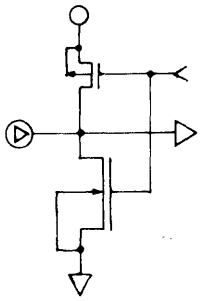
- **$\overline{COL1}$ to $\overline{COL3}$ (Pin 11 to 13) Column Input**
  $\overline{ROW1}$ to $\overline{ROW4}$ (Pin 14 to 17) Row Input

These are input/output pins for a key board which consists of PMOS pull up and NMOS driver. (As a matter of form, they are CMOS.)

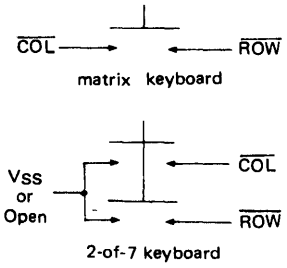
As the signals scan in Row side and Column side alternately, HD61825 can be connected both to the matrix-type keyboard and the 2-of-7 keyboard. While waiting the key input, Row is High level and Column is Low level. And in the reset condition, both Row and Column are Low level.

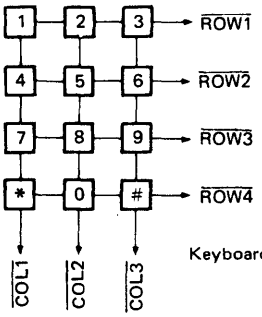
The hold time of the key should be more than 10 ms. (When the oscillation stops, the period for starting oscillation should be added.) (note 1)
The key debounce time is 20 ms.

NOTE:
1. The oscillation stops in HD61825;
   1. After the reset
   2. After the completion of DP output.
   3. On Pause



I/O Circuit for Keyboard Input/Output Pins





Keyboard Configuration

When two keys are pushed at the same time, the key of smaller number of ROW and COL is given priority and is input.

Ex. When typing [2] and [5] at the same time, [2] is input.

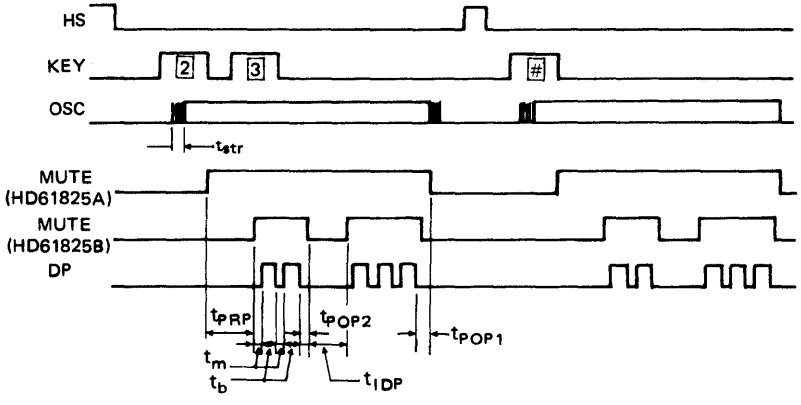
- **HS (PIN 18) HOOK SWITCH**

This is an input pin for detecting ON-HOOK/OFF-HOOK switch. It has a pull up MOS which is turned OFF at the reset.

ON HOOK . . . . . High (to V_{DD}) or open
OFF HOOK . . . . . Low (to V_{SS})

HD61825 is reset by making the HS terminal High level. If HS terminal is fixed to Low level, HD61825 is reset when the supply voltage falls less than the reset voltage. So, in this case, the HS pin is not used and the HD61825 controls the operation mode by the monitor of the supply voltage. However, as the pull up MOS is turned OFF with the reset signal, the current does not icnrease on reset.
An external capacitor must be provided between the HS pin and V_{SS} to prevent the noise from the switch.

• TIMING CHART



Item	Symbol	MBR	DPRS	min	typ	max	Unit
Pre-Digital pause	t_{PRP}	–	–	–	800	–	ms
Make time	t_m	33%	10PPS	–	33.3	–	ms
		40%	10PPS	–	39.7	–	ms
		33%	20PPS	–	16.6	–	ms
		40%	20PPS	–	20.5	–	ms
Breka time	t_b	33%	10PPS	–	66.7	–	ms
		40%	10PPS	–	60.2	–	ms
		33%	20PPS	–	33.3	–	ms
		40%	20PPS	–	29.4	–	ms
Inter-Digit Pause	t_{IDP}	–	10PPS	–	767	–	ms
		–	20PPS	–	500	–	ms
Post-Digital Pause	t_{POP1}	–	–	–	36	–	ms
	t_{POP2}	–	–	–	33	–	ms

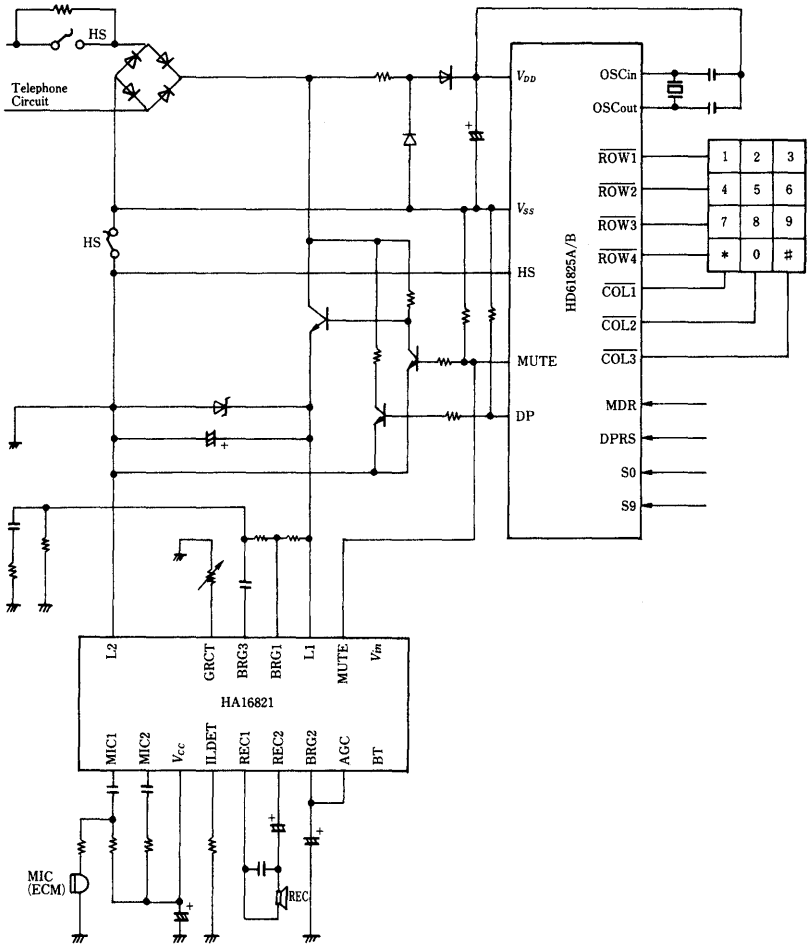
▪ AN EXAMPLE OF KEY OPERATION

	HOOK	KEY	DP
	ON		
Normal Dial	OFF	[0] [1] [2] [3] [4]	0–1–2–3–4
Dial after Pause		[5] [6]	5–6
	ON		
Redial	OFF	[#]	0–1–2–3–4–5–6
Dial after Redial		[7] [8]	7–8
	ON		
Redial	OFF	[#]	0–1–2–3–4–5–6–7–8
	ON		
Normal Dial	OFF	[9] [#] [1] [2]	9–1–2
(Pause Entry)	ON		
Redial	OFF	[#]	9
(Including Pause)		[#]	1–2
	ON		
Dial of 24 digits	OFF	[1] [1] . . . . . [1]	1–1 . . . . . –1
or more		24 times	24 times
	ON		
Prevention of Over Flow	OFF	[#]	
		[0] [1]	0–1

	HOOK	KEY	DP
(0 dialing in prevention mode with S0 = Low and S9 = High.)			
	ON OFF	[1] [2] [3] [0]	1–2–3–0
	ON OFF	[0] [4] [5] [6] [7]	
	ON OFF	[#]	1–2–3–0

NOTE:
After the output of pulse which corresponds to the each key operation are finished, Mute (also in HD61825A) is Low.

▪ APPLICATION CIRCUIT

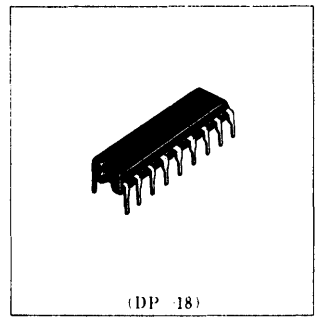


HD61826 Series

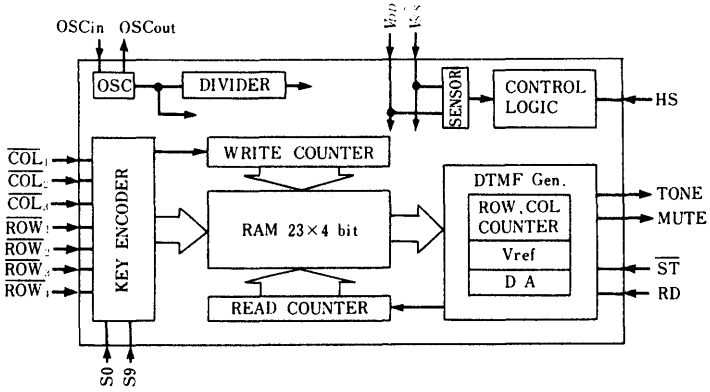
Tone Generator with Redial

■ FEATURES

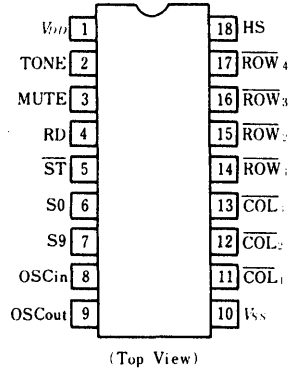
- Direct telephone-line operation
- CMOS process for low-power and low-voltage operation
- Uses either a standard 2-of-7 keyboard or the inexpensive matrix keyboard
- Stable operation by using ceramic resonator
- Redial function (# key)
- Pause input (# key)
- 0 or 9 dialing in inhibition pins for PABX system
- 23-digit redial memory
- Redial memory overflow protection (inhibit redial)
- On chip power supply voltage sense circuit
  - Memory clear voltage
  - Reset voltage
- Internal voltage reference circuit for stable Tone output
- Tone output with low distortion



■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



■ ABSOLUTE MAXIMUM RATINGS (Vss = 0V)

Item	Symbol	Value	Unit
Power supply voltage	V_{DD}	6.0	V
Terminal voltage	V_T	V_{SS} −0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{SS} = 0V, V_{DD} = 2.0 to 5.5V, T_a = −20 to +75°C)

Item	Symbol	Test Condition	min.	typ. *1	max.	Unit
Operating voltage (1)	V_{DD}	Tone Out Mode	2.5	–	5.5	V
Operating voltage (2)	V_{DD}	Non Tone Out Mode	1.7	–	5.5	V
Reset voltage	V_{DR}		–	1.5	–	V
Memory clear voltage	V_{DC}		–	1.15	–	V
Operating current	I_{DD}	Tone Out Mode, no load	–	300	–	μA
Memory retention (reset) current	I_{DR}		–	0.5	–	μA
Input High voltage	V_{IH}	except HS pin	80% V_{DD}	–	–	V
		HS pin V_{DD} = 3.0 to 5.5V	90% V_{DD}	–	–	
		HS pin V_{DD} = 2.0 to 3.0V	V_{DD}-0.1	–	–	
Input Low voltage	V_{IL}		–	–	20% V_{DD}	V
Input leak current	$\|I_{LI}\|$	Pull-up MOS off, V_{IN} = 0 to V_{DD}	–	–	1	μA
Input Pull-up MOS current	$-I_P$	V_{IN} = 0 (RD, ST, S0, S9, ROW, COL, HS)	–	10	–	μA
Output High voltage	V_{OH}	$-I_{OH}$ = 0.1mA (MUTE)	V_{DD}-0.5	–	–	V
Output Low voltage	V_{OL}	I_{OL} = 0.1mA (ROW, COL)	–	–	0.3	V
Output leak current	$\|I_{LO}\|$	Output MOS off, V_{IN} = 0 to V_{DD} (TONE MUTE)	–	–	1	μA

• **AC Characteristics** (V_{SS} = 0V, V_{DD} = 2.0 to 5.5V, T_a = −20 to +75°C)

Item		Symbol	Test Condition	min.	typ.*1	max.	Unit
Oscillation frequency		f_{osc}		–	400	–	kHz
Oscillation start up time		t_{str}		–	5	–	ms
Tone Out	ROW TONE	V_{OR}	Single Tone Mode, 600Ω to V_{SS}	200	245	290	mVrms
	COLUM TONE	V_{OC}	V_{DD} = 2.5 to 5.5V, T_a = 25°C	270	310	360	mVrms
Tone Out	ROW TONE	V_{OR}	Single Tone Mode, 10kΩ to V_{SS}	245	270	300	mVrms
	COLUM TONE	V_{OC}	V_{DD} = 2.5 to 5.5V, T_a = 25°C	310	340	370	mVrms
ROW/COLUM Tone Out ratio		dB_{CR}	V_{DD} = 2.5 to 5.5V	–	2	–	dB
Output distortion		D_{IS}	10kΩ to V_{SS}, V_{DD} = 2.5 to 5.5V	–	5	7	%

*1 Typ. value is the design value (the standard value at V_{DD} = 2.5V and T_a = 25°C)

■ Description

The HD61826 is specifically designed IC to implement a DTMF (Dual-Tone Multi Frequency) telephone dialing system. With low voltage and low-power consumption CMOS process, it can be operated directly from the telephone line. This IC generates each DTMF signal by digitally synthesizing the sinusoidal waveform for the individual frequencies, using a 400 kHz ceramic oscillation as frequency reference. The last dial numbers can be redialed by the simple key operation using an internal redial memory. The HD61826 can also be used as a normal DTMF dialer without the redial memory by mode select input.

In the HD61826, ON HOOK/OFF HOOK is detected by the HS pin. When the supply voltage is lower than reset voltage, the HD61826 does not accept any key inputs independent of the HS pin. When the power supply voltage is lower than memory clear voltage, the internal memory data is cleared.

While the telephone is in the OFF HOOK and the supply voltage is higher than the reset voltage, the oscillator is enabled by a key input and then this key input is implemented with the key debounce circuit, In this case, if the first key after the reset (note 1) is other than # and *, the internal memory data is cleared, and then this input key is encoded and stored into the memory. The following keys are in turn stored into the memory and converted into DTMF signal outputs. (note 2)

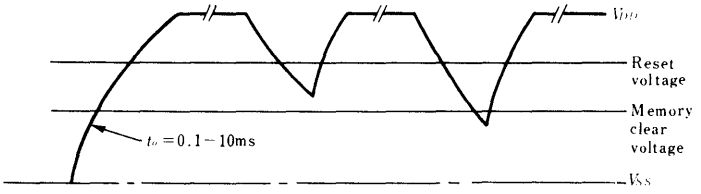
When the HD61826 is reset after dialing, it will be in the redial mode with the first # key. However, if the 24 or more keys have been dialed previously or the memory has already been cleared, it cannot be in the redial mode. During the redial mode, any key input is not accepted, but after the completion of redial, the HD61826 can be used as a usual dialer. The signal output will stop with the pause during the redial and the redial starts again with # key. # key is used to insert the pause data in the memory. In this case, # key does not influence the output of signal but is stored in the memory as one digit.

NOTES:
1. In the HD61826, the reset means the clearing of all logic (counter, etc.) except RAM. HD61826 is reset when the telephone is in the ON HOOK or the supply voltage is lower than the reset voltage.
2. While the key is pushed, the DTMF signal is kept generating.

■ PIN FUNCTION

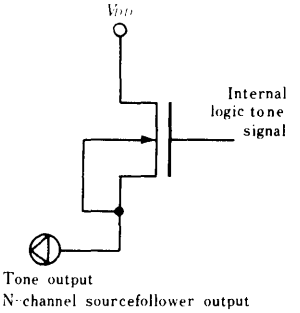
• V_{DD} (Pin 1)

This is a positive voltage supply pin which applies voltage to the basis of the V_{SS} pin. HD61826 provides the internal sense circuit for the supply voltage. To make this circuit operate stable, the following rising time is necessary.

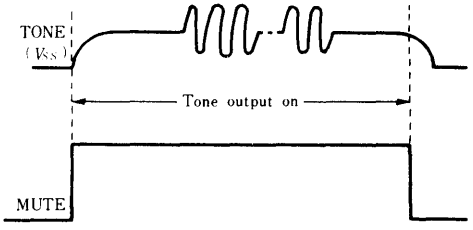


• TONE (Pin 2)

This is a Tone output (DTMF signal output) pin. Output circuit is N-Channel MOS source-follower and the resistor to V_{SS} is necessary. Further, to realize low power consumption in the standby mode, TONE output MOS and internal V_{ref} circuit are turned off after tone output completed. And this is synchronous with MUTE signal. DTMF signal is digitally synthesized by using the 400 kHz oscillation as frequency reference. Tone output frequency of HD61826 and its deviation from standard DTMF are as follows:



		Standard DTMF (Hz)	Tone Output Frequency Using 400 kHz Oscillation	% Deviation from Standard
ROW	f_1	697	694,44	−0.37
	f_2	770	769,23	−0.10
	f_3	852	851,06	−0.11
	f_4	941	938,97	−0.22
COL	f_5	1209	1212,12	0.26
	f_6	1336	1333,33	−0.20
	f_7	1477	1481,48	0.30



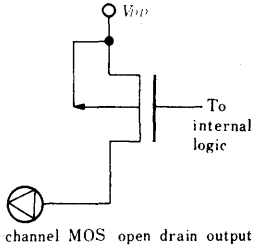
As the HD61826 contains an voltage reference (V_{ref}) circuit, it always generates stable Tone output amplitude even if supply voltage and temperature change.

• MUTE (Pin 3)

This is a pin which mutes the receiver and the transmitter. Output circuit is P-Channel MOS open drain.

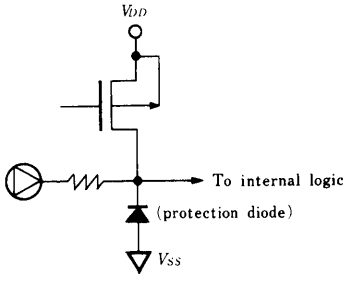
MUTE . . . High level

While reset, the output voltage is held to Low level.



- **RD (Pin 4) Redial Operation**

This is an input pin which selects HD61826 operations: a tone dialer with redial providing memory function, and a simple tone dialer in which only normal key input is converted into tone output. This pin is implemented with the pull-up MOS, and to realize the low power dissipation on reset, the pull-up MOS is turned off at the reset. (note 1)



RD pin	Operation Mode	Redial	Operation
High (to V_{DD}) or open	Tone Dialer with Redial	available	• no Tone out with * or # • Redial/Pause with #
Low (to V_{SS})	Simple Tone Dialer	not available	• Tone out with * or #

NOTES:
1. The input pins, with pull-up MOS which is turned off at the reset, can be applied to RD, $\overline{ST}$, S0, S9, HS.
2. The logic is positive. PMOS is ON with the low voltage and OFF with the high voltage.

- **$\overline{ST}$ (Pin 5) Single Tone Test**

This is an input pin to put HD61826 in the single tone mode for tone output test. This pin is implemented with the pull-up MOS which is turned off at the reset. Further, in the single tone mode, digital signal for test is output on MUTE. Usually $\overline{ST}$ pin should be fixed to High level or open.

$\overline{ST}$ pin	S0 pin	S9 pin	Operation Mode	Tone Output
High (to V_{DD}) or open	–	–	Dual Tone	DTMF Tone out
Low (to V_{SS})	Low	High	Single Tone	to ROW Single tone out
	High	Low		to COL Single tone out

NOTE: S0 and S9 pins should not be Low level at the same time.

- **S0, S9 (Pin 6, 7) Selection**

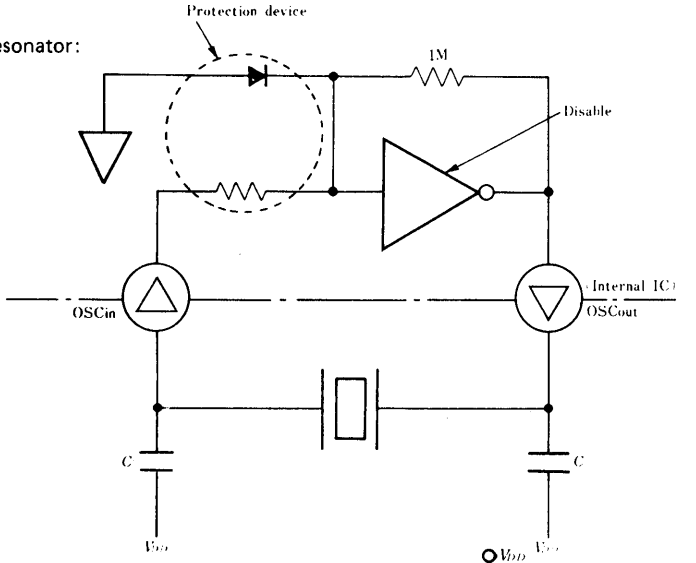
These are input pins to select functions and each of them has pull-up MOS which is turned OFF at the reset. The function of this terminal is to prevent the 0 dialing in and 9 dialing in, which is applied to the telephone subset under the PBX system. When the first key input after the reset is 0 or 9, all the key inputs including the 0 or 9 key become invalid after then. In other words, the signals are not output to TONE and MUTE. Then the telephone is initialized by the reset.

S0 Pin	S9 Pin	Function
High (to V_{DD}) or open	High (to V_{DD}) or open	Normal dialing mode
High (to V_{DD}) or open	Low (to V_{SS})	9 dialing in inhibition mode
Low (to V_{SS})	High (to V_{DD}) or open	0 dialing in inhibition mode
Low (to V_{SS})	Low (to V_{SS})	Test mode (for testing IC. Not use.)

- **OSCin, OSCout (Pin 8, 9) Oscillation Input, Output**

These are the input pins for the oscillator and construct the inverter (with disable function to stop the oscillation). The frequency is stable in the circuit by using the ceramic resonator. Then the oscillator section needs two external capacitors. The ceramic resonator should be 400 kHz and High Q.

Recommended ceramic resonator:
KYOCERA CO.
KBR-400H
ex. ceramic oscillation
C_1 = 100 pF
C_2 = 470 pF



Oscillation Circuit

When OSCout is open, a 400 kHz external pulse can be applied to OSCin.

- **V_{SS} (Pin 10)**

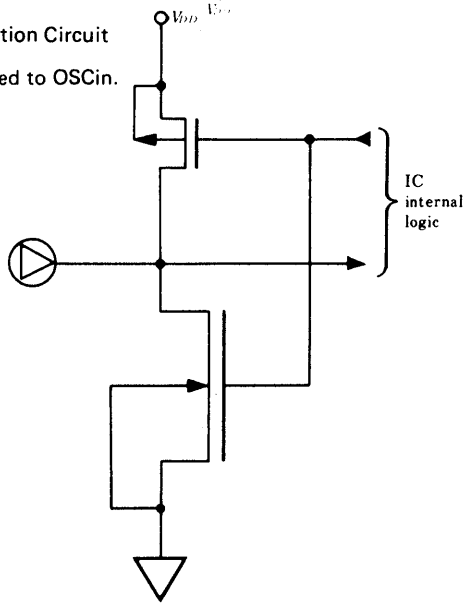
This is a negative power supply pin.

- **$\overline{COL_1}$ to $\overline{COL_3}$ (Pin 11 to 13) Colum Input**
  $\overline{ROW_1}$ to $\overline{ROW_4}$ (Pin 14 to 17) Row Input

These are input/output pins for a key board which consist of PMOS pull-up and NMOS driver. (As a matter of form, these are CMOS.)

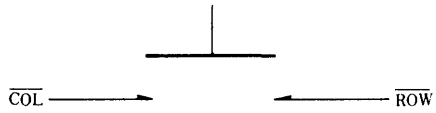
As the row and column are alternately scanned, the HD61826 can be connected both to the matrix-type keyboard and the 2-of-7 keyboard. While waiting for the key input, Rows are High level and Columns are Low level. And in the reset mode, both Row and Column are Low level.

The hold time of the key should be more than 10 ms. (While the oscillation stops, the period for starting oscillation should be added.) (note 1) The key debounce time is 20 ms. Tone is remaining while pushing the key (precisely speaking, after key operation, tone continues during the debounce time). But the key operation should meet the DTMF receiver specification.

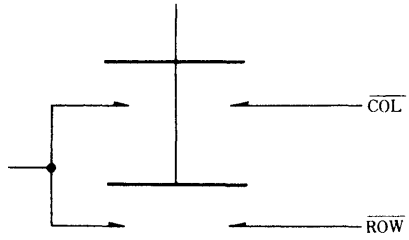


I/O Circuit for Keyboard

NOTES:
1. The oscillation stops in HD61826;
   1. After the reset
   2. After the completkon of Tone output
   3. On Pause



Matrix Keyboard



2–of–7 Keyboard

When two keys are pushed at the same time, the key of the smaller number of ROW and COL is given priority and is entered.

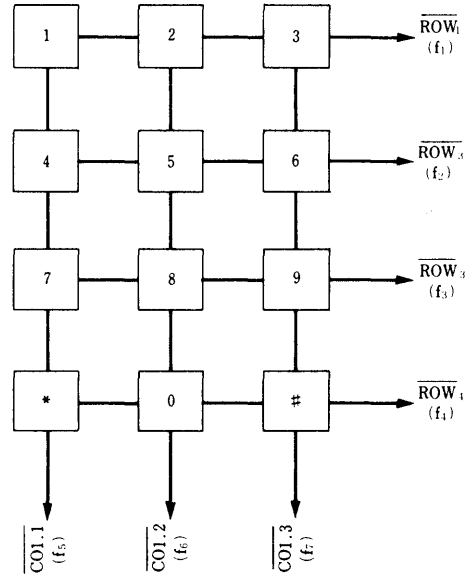
Ex. When 2 and 5 are pushed at the same time, 2 is accepted.

- **HS (Pin 18) Hook Switch**

This is an input pin for detecting ON-HOOK/OFF-HOOK switch. It has a pull-up MOS which is turned off at the reset.

ON HOOK . . . . High (to V_{DD}) or open

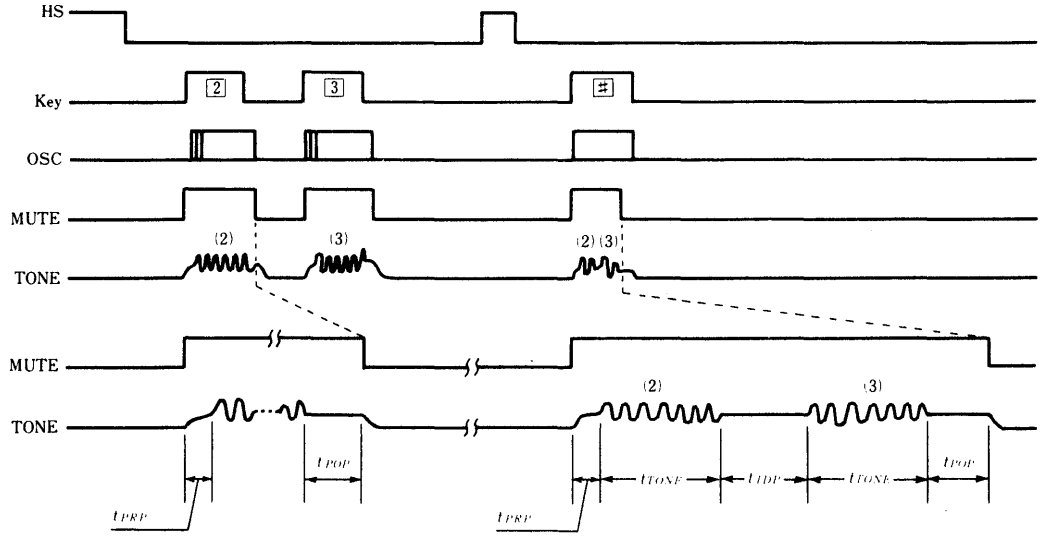
OFF HOOK . . . Low (to V_{SS})



Keyboard Configuration

HD61826 is reset by setting the HS terminal High level. Even if the HS terminal is fixed to Low level, the HD61826 is reset when supply voltage is lower than reset voltage. So without using the HS pin the HD61826 can control the operation mode by the monitor of supply voltage. Then, as the pull-up MOS is turned off with the reset signal, the current does not increase on reset. An external capacitor must be provided between the HS pin and V_{SS} to prevent the switch from chattering.

■ TIMING CHART



Mode	Item	Symbol	min.	typ.	max.	Unit
Normal Dial	Pre-Digital Pause	t_{PRP}	–	5	–	ms
	Post-Digital Pause	t_{POP}	–	44	–	ms
Redial	Pre-Digital Pause	t_{PRP}	–	5	–	ms
	Tone Output time	t_{TONE}	–	133	–	ms
	Inter-Digital Pause	t_{IDP}	–	87	–	ms
	Post-Digital Pause	t_{POP}	–	44	–	ms

■ AN EXAMPLE OF KEY OPERATION (RD = High)

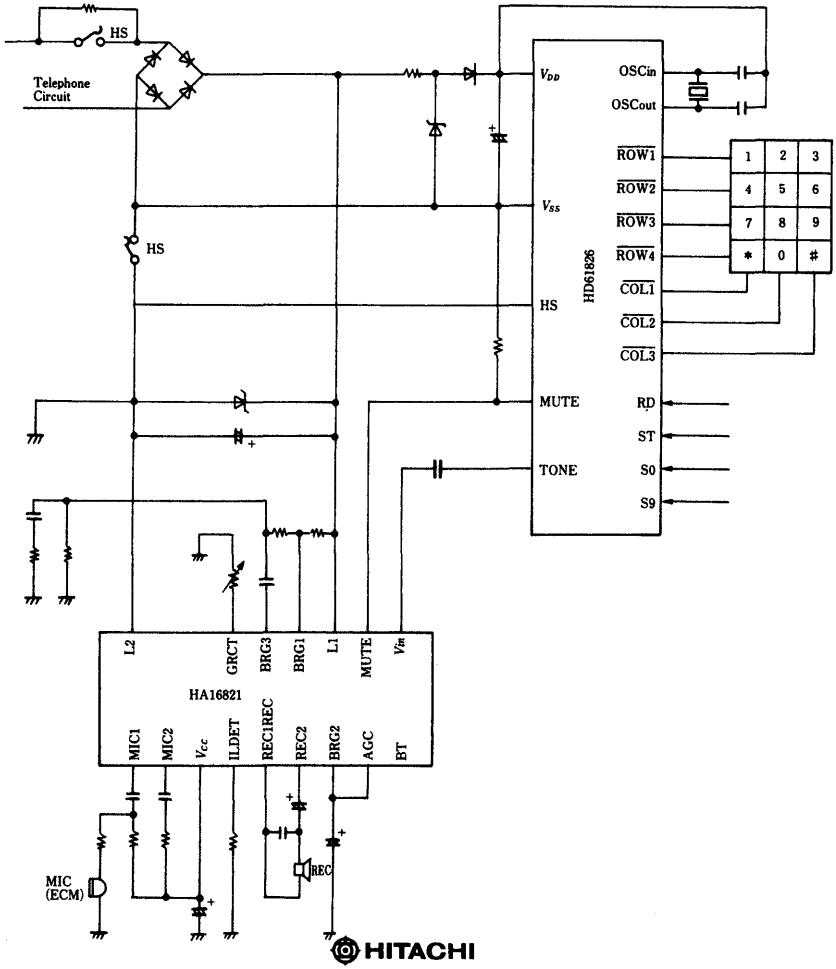
	HOOK	KEY	TONE
	ON		
Normal Dial	OFF	0 1 2 3 4 5 6	0, 1, 2, 3, 4, 5, 6, (note)
	ON		
Redial	OFF	#	0-1-2-3-4-5-6 (note)
Dial after Redial		7 8	7, 8,
	ON		
Redial	OFF	#	0-1-2-3-4-5-6-7-8
	ON		
Normal Dial	OFF	9 # 1 2	9, 1, 2,
(Pause Entry)	ON		
Redial	OFF	#	9,
(Including Pause)		#	1-2,
	ON		
Dial of 24 digits or more	OFF	1 1. . . . . 1 24 times	1, 1. . . . . 1, 24 times
	ON		
Prevention of Over Flow	OFF	# 0 1	0, 1

(0 dialing in inhibition mode with S0 = Low and S9 = High)

	ON	
	OFF	1 2 3 0
	ON	
	OFF	0 4 5 6 7 #
	ON	
	OFF	# 1 2 3 0

NOTE: , shows that after tone output Mute is Low level and - shows that Mute is High level.

■ APPLICATION CIRCUIT



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HA12089NT/MP

Sound Signal Processing IC for Automatic Telephone Answering System

Description

The HA12089 is the IC designed for sound signal processing for automatic telephone answering system. As the device builds mainly in fundamental features necessary to the automatic answering telephone, it can construct the sound signal processing needed for automatic answering telephone on 1 chip.

Features

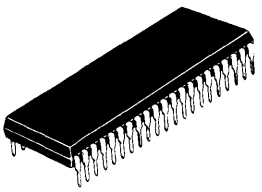
- Adjustable with frequency characteristic and each gain of LINE·REC·PB·Monitor series by external parts
- Possible to trim AC current flowing head by external resistance because of using current drive type for OGM/ICM head change
- High Integration
  (SW Part)
  - OGM/ICM Head Change SW Circuit
  - OGM/ICM Bias SW Circuit for Erase
  - MIC/LINE Input Change SW Circuit
  - PRE Amp Frequency Change Circuit

  (REC/PB Part)
  - PRE Amp·Buffer Amp·REC Amp
  - Power Amp·Power Mute Circuit
  - ALC Circuit·ATT Circuit when FF/REW

  (LINE Part)
  - Filter Amp·LINE Amp·ATT Circuit when FF/REW

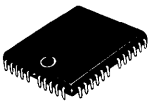
  (VOX Part)
  - VOX Amp·COMP Amp; (Detection Circuit)

HA12089NT



DP-42SA

HA12089MP



MP-44

2

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage *	Vcc (max)	7.0	V
Power Dissipation **	Pr	300	mW
Operating Temperature	Topr	–20 to +65	°C
Storage Temperature	Tstg	–55 to +125	°C

Note) * Standard Operating Voltage...Vcc 6.0 V ± 0.5 V
** Allowable Value under the condition of Ta = 65°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

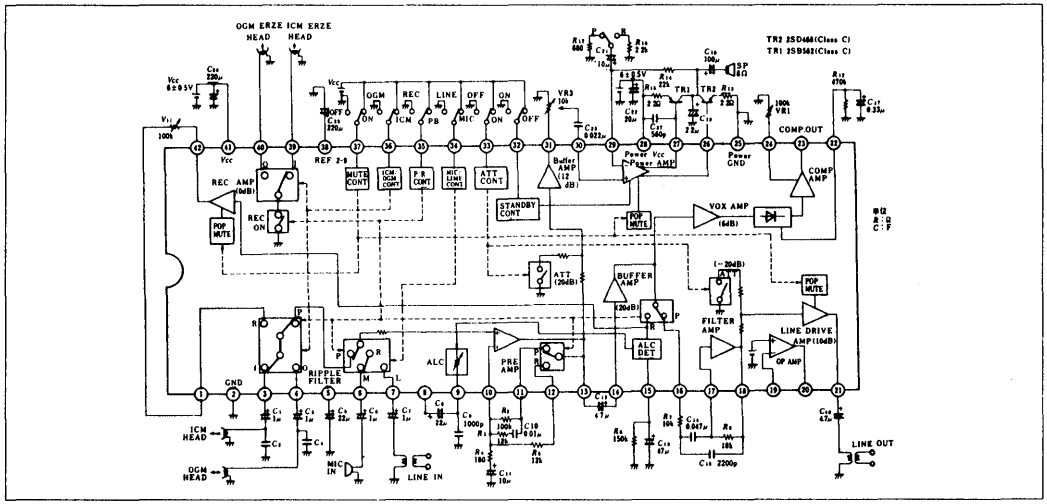


Figure 1-1 Standard External Circuit and Block Diagram (HA12089NT)

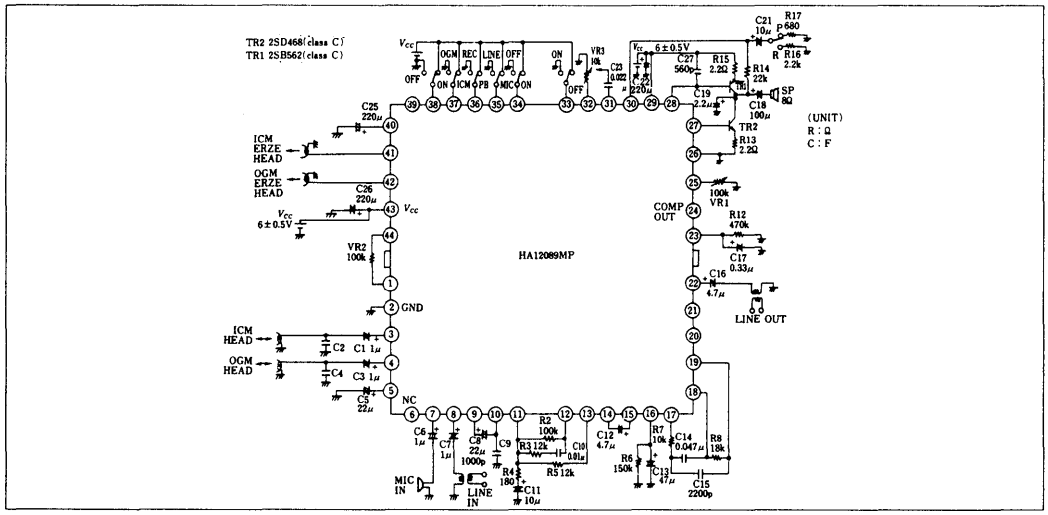


Figure 1-2 Standard External Circuit (HA12089MP)

Pin Description (HA12089NT)

Pin No.	Symbol	Description
1	REC-OUT1	REC Output
2	GND	GND (Small signal)
3	ICM	ICM Input/Output
4	OGM	OGM Input/Output
5	RIP-FIL	Ripple Filter
6	MIC-IN	Mic Input
7	LINE-IN	Line Input
8	ALC-DC-CUT	ALC DC Cut
9	ALC	ALC Input
10	PRE-IN	Pre Amp Input
11	PB-FB	Play Pre Amp Output
12	REC-FB	REC Pre Amp Output
13	PRE-OUT	Pre Amp Output
14	BUFF-IN	Buffer Amp Input
15	ALC-DET	ALC Detector
16	PB-BUFF-OUT	Play Buffer Amp Output
17	FIL-IN	Filter Amp Input
18	FIL-OUT	Filter Amp Output
19	AMP-IN	Attached Amp Input
20	AMP-OUT	Attached Amp Output
21	LINE-OUT	Line Amp Output
22	VOX-DET	Vox Detection
23	COMP-OUT	Comparator Output
24	COMP-ADJ	Comparative Level Adjustment
25	POWER-GND	GND (Power)
26	POWER-DR1	External Power Transistor Drive
27	POWER-DR2	External Power Transistor Drive
28	POWER-Vcc	Vcc (Power)
29	POWER-FB	Power Amp Feedback Input
30	POWER-IN	Power Amp Input
31	BUFF-OUT	Buffer Amp Output
32	STANDBY	Power Amp Standby Control *
33	ATT	Attenuator Control
34	MIC/LINE	MIC/LINE Input SW Control
35	PB/REC	PLAY/REC SW Control
36	ICM/OGM	ICM/OGM SW Control
37	MUTE	Mute Control
38	V_{REF}	Reference
39	ICM-ERS	ICM DC Erase
40	OGM-ERS	OGM DC Erase
41	Vcc	Vcc (Small signal)
42	REC-OOT2	REC output

* Consumption Current : 20 mA Typ → 1 mA Typ

Pin Function (HA12089MP)

Pin No.	Symbol	Description
1	REC-OUT1	REC output
2	GND	GND (Small signal)
3	ICM	ICM Input/Output
4	OGM	OGM Input/Output
5	RIP-FIL	Ripple Filter
6	NC	No Connect
7	MIC-IN	Mic Input
8	LINE-IN	Line Input
9	ALC-DC-CUT	ALC DC Cut
10	ALC	ALC Input
11	PRE-IN	Pre Amp Input
12	PB-FB	Play Pre Amp Output
13	REC-FB	REC Pre Amp Output
14	PRE-OUT	Pre Amp Output
15	BUFF-IN	Buffer Amp Input
16	ALC-DET	ALC Detector
17	PB-BUFF-OUT	Play Buffer Amp Output
18	FIL-IN	Filter Amp Input
19	FIL-OUT	Filter Amp Output
20	AMP-IN	Attached Amp Input
21	AMP-OUT	Attached Amp Output
22	LINE-OUT	Line Amp Output
23	VOX-DET	Vox Detection
24	COMP-OUT	Comparator Output
25	COMP-ADJ	Comparative Level Adjustment
26	POWER-GND	GND (Power)
27	POWER-DR1	External Power Transistor Drive
28	POWER-DR2	External Power Transistor Drive
29	POWER-Vcc	Vcc (Power)
30	POWER-FB	Power Amp Feedback Input
31	POWER-IN	Power Amp Input
32	BUFF-OUT	Buffer Amp Output
33	STANDBY	Power Amp Standby Control *
34	ATT	Attenuator Control
35	MIC/LINE	MIC/LINE Input SW Control
36	PB/REC	PLAY/REC SW Control
37	ICM/OGM	ICM/OGM SW Control
38	MUTE	Mute Control
39	NC	No Connect
40	V_{REF}	Reference
41	ICM-ERS	ICM DC Erase
42	OGM-ERS	OGM DC Erase
43	Vcc	Vcc (Small signal)
44	REC-OUT2	REC Output

* Consumption Current : 20 mA Typ → 1 mA Typ

Electrical Characteristics (Ta = 25°C, Vcc = 6 V)

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Application Terminal	Remark
Quiescent Current	I_Q	Pin㉟(㊱) = 5 V Non-signal	—	15	23	mA	㊶(㊸)	
PB Voltage Gain	Gv1	Vo = 0 dBm	71	74	77	dB	③→㉑(③→㉒)	
PB Maximum Output Voltage	Vom1	T.H.D = 10%	1.2	1.7	—	Vrms		
PB Distortion Ratio	THD1	Vo = 0 dBm	—	0.4	2.0	%		1
REC Voltage Gain	Gv2	Vin = –70 dBm	51	54	57	dB	⑥→③ (⑦→③)	
REC Maximum Input Voltage	Vim1	THD ≤ 2%	—	—	–30	dBm		
REC Distortion Ratio	THD2	Vin = –50 dBm	—	0.7	2.0	%		1
REC Cross Talk	C.T.1	Vin = –30 dBm	—	—	–60	dB	⑥→⑦(⑦→⑧)	1
REC Voltage When ALC Operating	Gv ALC	Vin = –50 dBm	–9	–6	–3	dBm	⑥→③(⑦→③)	
Power Voltage Gain	Gv3	PB Mode 10 dB ATT Vo = 0 dBm	68.5	71.5	74.5	dB	③→ Power Output	
Power Maximum Output Voltage	Vom2	PB Mode 10 dB ATT THD = 10%	1.2	1.7	—	Vrms		
Power Distortion	THD3	PB Mode 10 dB ATT Vo = 0 dBm	—	0.6	2.0	%		1
Power Mute Attenuation	ATT1	Vo = 0 dBm Pin㊲(㊳) = 5 V PB Mode	—	—	–50	dB		1
Comparator H Output Voltage	V_{OH}	Pin㉔(㉕) = 1.9 V REC Mode Vin = –60 dBm	3.8	—	5.0	V	㉓(㉔)	
Comparator L Output Voltage	V_{OL}	Pin㉔(㉕) = 1.9 V REC Mode	–0.3	—	0.5	V		
Control H Input Voltage	V_{IH}	Lo Mode → Hi Mode Change Voltage	3.8	—	Vcc	V	㉜~㊲(㉝~㊳)	
Control L Input Voltage	V_{IL}	Hi Mode → Lo Mode Change Voltage	0	—	0.5	V		

Remark 1) B.P.F in 400 Hz to 15 kHz

Number inside ( ) shows terminal pin number for HA12089MP.

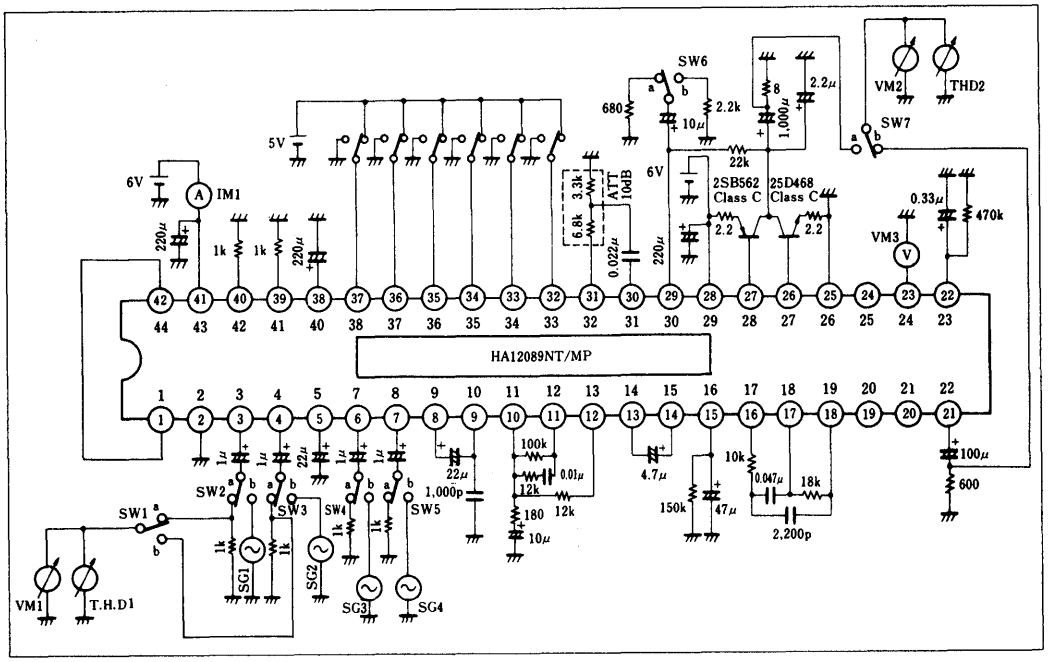
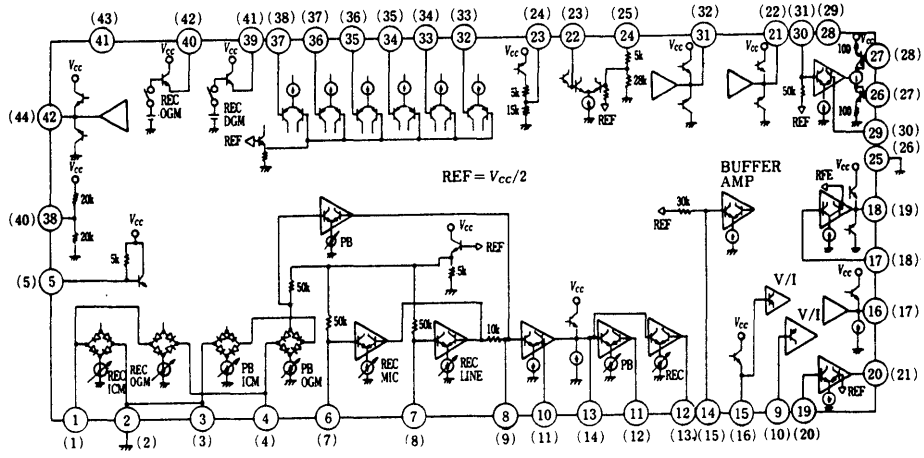


Figure 2 Test Circuit

Table 1. Switched Position Table

No.	Symbol	Control Terminal 32(33)	33(34)	34(35)	35(36)	36(37)	37(38)	SW Position SW1	SW2	SW3	SW4	SW5	SW6	SW7	Source Signal & Measurement
1	I_Q	L	L	L	H	L	L	a	a	a	a	a	a	a	IM1
2	Gv1	H	↓	↓	↓	H	↓	↓	b	↓	↓	↓	↓	b	SG1, VM2
3	Vom1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG1, VM2, THD2
4	THD1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
5	Gv2	↓	↓	H	L	↓	↓	↓	a	↓	b	↓	b	a	SG3, VM1
6	Vim1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG3, THD1
7	THD2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
8	C.T1	↓	↓	L	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG3, VM1
9	Gv ALC	↓	↓	H	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG3, THD1
10	Gv3	↓	↓	L	H	↓	↓	↓	b	↓	a	↓	a	↓	SG1, VM2
11	Vom2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG1, VM2, THD2
12	THD3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
13	ATT1	↓	↓	↓	↓	↓	H	↓	↓	↓	↓	↓	↓	↓	SG1, VM2
14	V_{OH}	↓	↓	H	L	↓	L	↓	a	↓	b	↓	b	↓	SG3, VM3
15	V_{OL}	↓	↓	↓	↓	↓	↓	↓	↓	↓	a	↓	↓	↓	↓
16	V_{IH}	↓	H	H	H	H	H	↓	↓	↓	↓	↓	↓	↓	—
17	V_{IL}	L	L	L	L	L	L	↓	↓	↓	↓	↓	↓	↓	—

H = 5 (V), L = 0 (V)



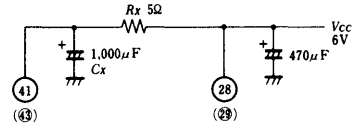
- Resistance value: Typ.
- Number inside ( ) shows terminal pin number for HA12089MP

Unit R: (Ω)

Figure 3 Input/Output Circuit

Note

1. This IC is two supply voltage pins; ㉘, ㊶ (㉙, ㊸) pin and two GND terminal pins; ②, ㉕ (②, ㉖) pin. Prevent signal from the supply sourse of another block by applying supply voltage to power ㉘ (㉙) pin and small signal ㊶ (㊸) pin respectively. Distortion ratio may become worse by the signal from the supply sourse of another block. In the case of single supply voltage of power and small signal, for example, avoid the signal from the supply sourse of power block to small signal one, by connecting wiring as shown below.



Take care of keeping 5.5 V or more of voltage of 41 (43) pin by reducing Rx as much as possible.

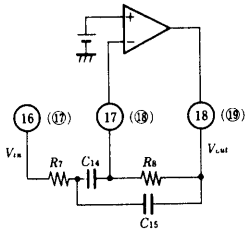
2. Determine the filter constant of ⑯, ⑰, ⑱ (⑰, ⑱, ⑲) pin as shown below.

$$\frac{Vout}{Vin} = T(S) = \frac{-\frac{1}{R7C15}S}{S^2 + \frac{1}{R8}\left(\frac{1}{C14} + \frac{1}{C15}\right)S + \frac{1}{C14C15R7R8}}$$

Cut-off frequency is shown below to use as a band path filter.

$$\omega_H = \frac{\frac{1}{C14} + \frac{1}{C15}}{2R8}\left(1 + \sqrt{1 - \frac{4R8}{R7\left(2 + \frac{C14}{C15} + \frac{C15}{C14}\right)}}\right)$$

$$\omega_L = \frac{\frac{1}{C14} + \frac{1}{C15}}{2R8}\left(1 - \sqrt{1 - \frac{4R8}{R7\left(2 + \frac{C14}{C15} + \frac{C15}{C14}\right)}}\right)$$

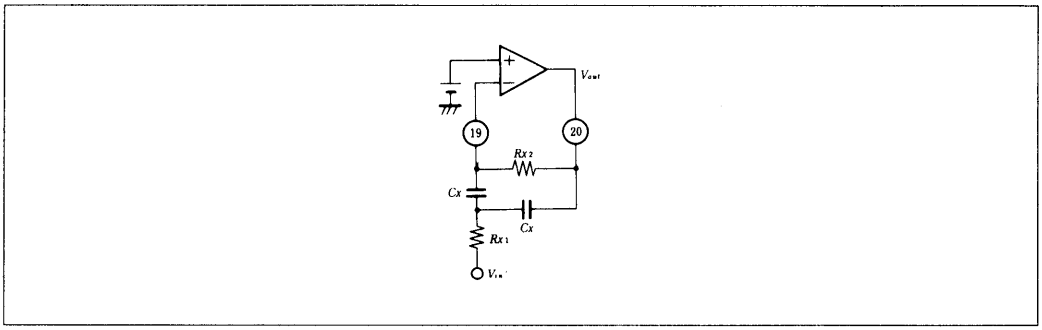


For example Cut-off frequency is f_H = 3.8 kHz, f_L = 350 Hz under the condition of R7 = 10 kΩ, R8 = 18 kΩ, C14 = 0.047 μF and C15 = 2200 pF.

Number inside (O) shows terminal pin number for HA12089MP.

3. Example of using ⑲, ⑳ (⑳, ㉑) additional Amp.

$$\frac{Vout'}{Vin'} = \frac{-\frac{1}{CxRx1}S}{S^2 + \frac{2}{CxRx2}S + \frac{1}{CxRx1Rx2}}$$



The resonance frequency; Wo, the band width; BW and the Q are shown below.

$$Wo = \frac{1}{Cx\sqrt{Rx1Rx2}}, \quad BW = \frac{Wo}{Q} = \frac{2}{CxRx2}, \quad Q = \frac{1}{2}\sqrt{\frac{Rx2}{Rx1}}$$

The gain under condition of the resonance frequency; Wo is shown below.

$$\left|\frac{Vout'}{Vin'}\right|_{S = jWo} = \frac{Rx2}{2Rx1}$$

For example, the following constant can be set to construct the resonance filter under the condition of Wo = 1kHz.

Cx = 0.0015μF Rx1 = 10kΩ Rx2 = 1MΩ

Q = 5BW = 200Hz Gv(f = 1kHz) = 50

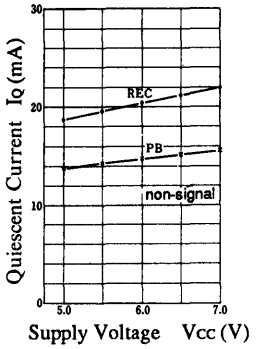
4. Power block is designed with our power transistor 2SD468, 2SB562C grade.
   Use the power transistor which has small deviation of V_{BE} to reduce the deviation of idling current.

External Component

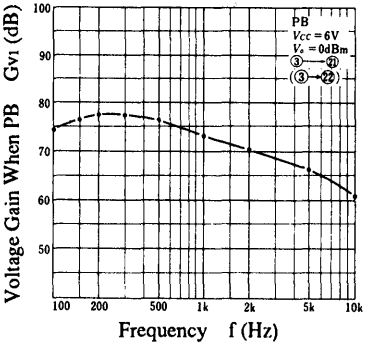
Part No.	Standard Value	Feature	Influence		Remarks
			Standard Value or less	Standard Vallue or more	
C1	1 μ	DC CUT	—	—	
C2					
C3	1 μ	DC CUT	—	—	
C4					
C5	22 μ	Ripple Filter	Ripple rejection ratio becomes worse	—	
C6	1 μ	DC CUT	—	—	
C7	1 μ	DC CUT	—	—	
C8	22 μ	DC CUT	Frequency characteristics become worse	Rising of AGC becomes slow	
C9	1000 pF	Oscillation Stop	ALC circuit oscillation	Frequency characteristics become worse	
C10	0.0 1μ	High Cut-off Frequency	Small cut-off frequency	Large cut-off frequency	
C11	10 μ	Low Cut-off Frequency	Large cut-off frequency	Small cut-off frequency	
C12	4.7 μ	DC CUT	Breaking off when attacking	—	
C13	47 μ	Constant when ALC	Distortion ratio becomes worse	Long attack recovery time	
C14	0.047 μ	Constant when filter	See Note.		
C15	2200 pF				
C16	4.7 μ	DC CUT	—	—	
C17	0.33 μ	Detection Circuit	Unstability of comparator operating	Delay of comparator response	
C18	100 μ	DC CUT	Frequency characteristics become worse	—	
C19	2.2 μ	Phase Compensation	Power amp oscillation	Frequency characteristics become worse	
C20	Missing	Number			
C21	10 μ	Low Cut-off	Small cut-off	Large cut-off	
C22	220 μ	Power Source Ripple Rejection	Ripple rejection ratio becomes worse.	—	
C23	0.022 μ	DC CUT	Small cut frequency	—	
C24	Missing	Number			
C25	220 μ	Ripple Filter	Ripple rejection ratio becomes worse	—	
C26	220 μ	Supply Voltage Ripple Rejection	Ripple rejection ratio becomes worse	—	
C27	560 pF	Stop of Oscillation	Power oscillation	Small cut-off frequency	

Part No.	Standard Value	Function	Influence		Remarks
			Standard Value or less	Standard Vallue or more	
R1	Missing Number				
R2	100 k	PB Gv	Small Gv	Large offset voltage of pin 31 (32)	
R3	12 k	PB Gv	Small Gv	Large Gv	
R4	180	Pre Amp Gv	Large Gv	Small Gv	
R5	12 k	REC Gv	Small Gv	Large Gv	
R6	150 k	Constant when ALC	Short attack recovery time	Long attack recovery time	
R7	10 k	Filter Amp Gv	Small Gv	Large Gv	
R8	18 k	Filter Amp Gv	Small Gv	Large off-set voltage of pin 21 (22)	
R9 to 11	Missing Number				
R12	470 k	Detection Circuit	Unstability of comparator operating	Delay of comparator response	
R13, 15	2.2 Ω	External Tr Idling Current	Large idling current	Small power output	
R14	22 k	Power Gv	Small Gv	Large off-set	
R16	2.2 k	REC Power Gv	Large Gv	Small Gv	
R17	680	PB Power Gv	Large Gv	Small Gv	

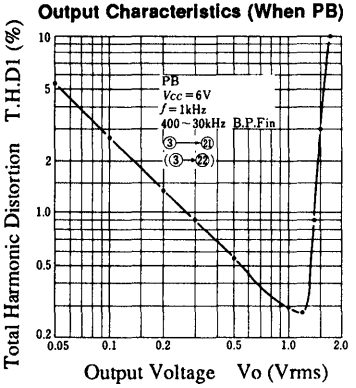
Quiescent Current vs. Supply Voltage Characteristics



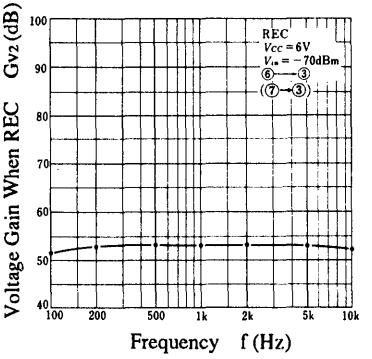
Voltage Gain vs. Frequency Characteristics (When PB)



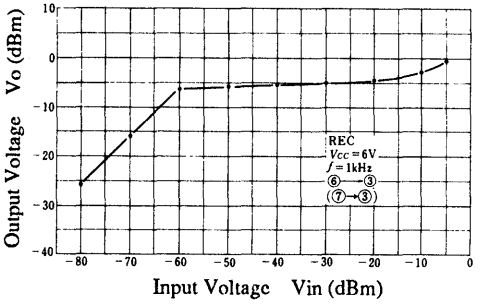
Total Harmonic Distortion vs. Output Characteristics (When PB)



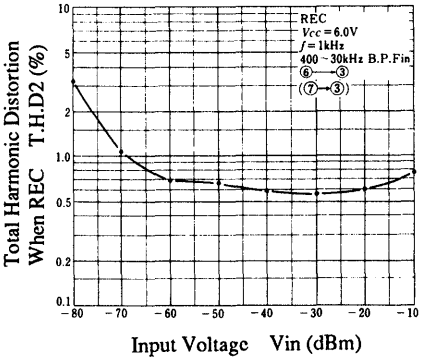
Voltage Gain vs. Frequency Characteristics (When REC)



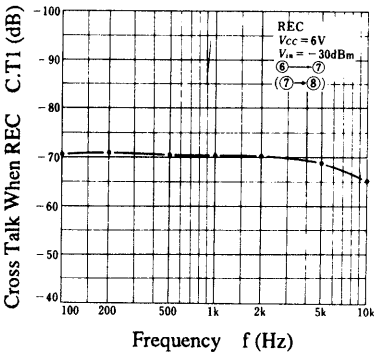
Input/Output Characteristics (When REC)



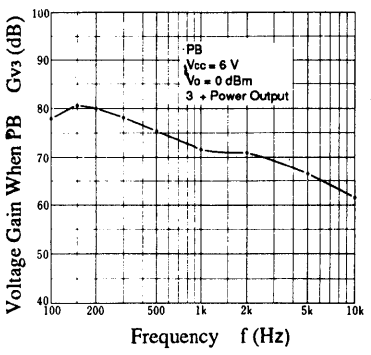
Total Harmonic Distortion vs. Input Voltage Characteristics (When REC)



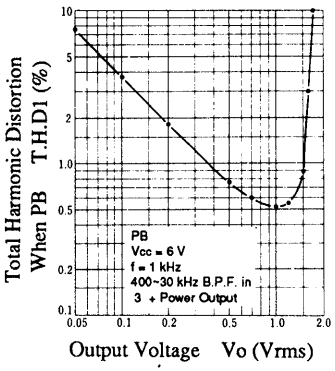
Cross Talk vs. Frequency (When REC)



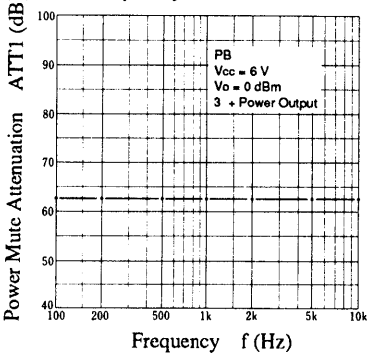
Voltage Gain vs. Frequency Characteristics (When PB)



Total Harmonic Distortion vs. Output Voltage Characteristics (When PB)



Power Mute Attenuation vs. Frequency Characteristics



HA12189NT/MP

Preliminary

Sound Signal Processing IC for Automatic Telephone Answering System

Description

The HA12189 is the IC designed for sound signal processing for automatic telephone answering system. As the device builds mainly in fundamental features, necessary to the automatic answering telephone, it can construct the sound signal processing easily, and is suitable for answering system that use cassette for ICM and IC memory for OGM.

Features

- Adjustable with frequency characteristic and each gain of LINE·REC·PB·Monitor series by external parts
- Suitable for answering system that use cassette for ICM and IC memory for OGM
- High Integration

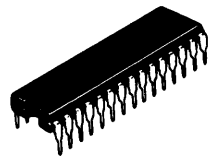
  (SW Part)
  - OGM/ICM Change SW Circuit
  - PLAY/REC Change SW Circuit
  - MIC/LINE Input Change SW Circuit
  - PRE Amp·Frequency Change Circuit
  - MUTE SW Circuit

  (REC/PB Part)
  - PRE Amp, Buffer Amp, REC Amp
  - ALC Circuit, MUTE Circuit

  (LINE Part)
  - LINE Amp, MUTE Circuit

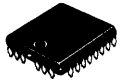
  (VOX Part)
  - VOX Amp, COMP Amp; (Detection Circuit)

HA12189NT



DP-30S

HA12189MP



MP-28

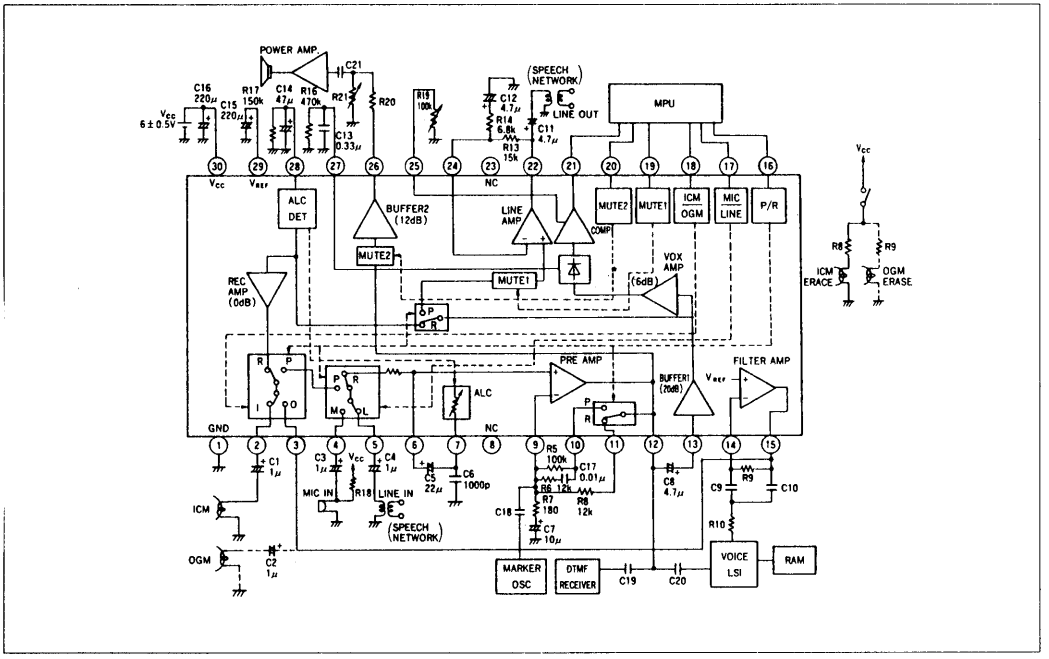


Figure 1-1 Standard External Circuit and Block Diagram. (HA12189NT)

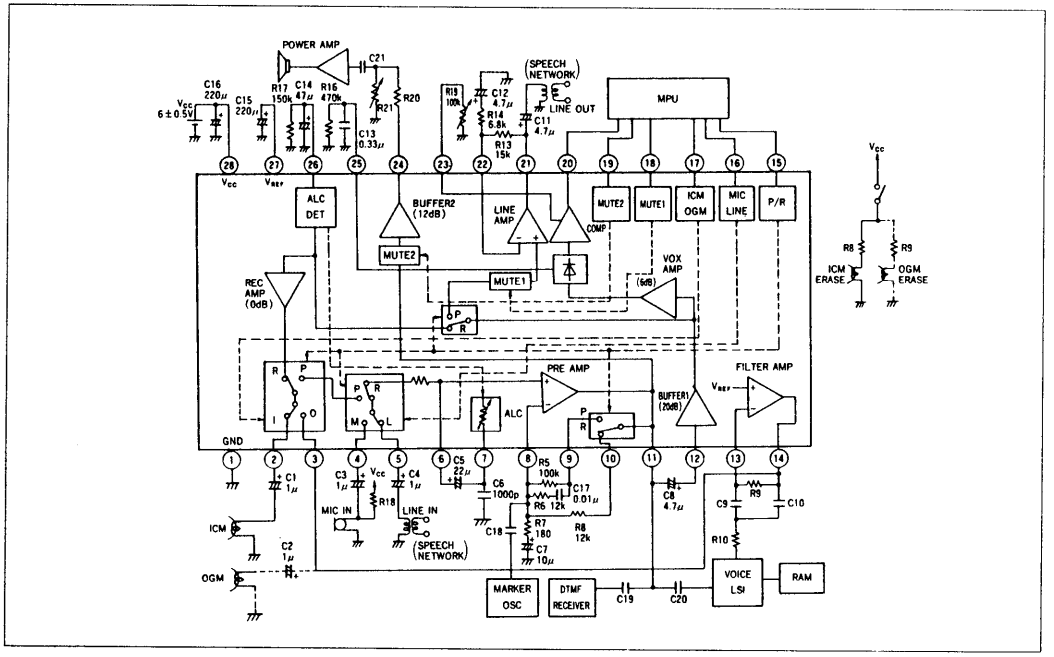


Figure 1-2 Standard External Circuit and Block Diagram. (HA12189MP)

Pin Function (HA12189NT)

Pin No.	Symbol	Description
1	GND	GND
2	ICM	ICM Input/Output
3	OGM	OGM Input/Output
4	MIC	MIC Input
5	LINE	Line Input
6	ALC-DC-CUT	ALC DC CUT
7	ALC	ALC Input
8	NC	No Connect
9	PRE-IN	Pre Amp Input
10	PB-FB	PLAY Pre Amp Output
11	REC-FB	REC Pre Amp Output
12	PRE-OUT	Pre Amp Output
13	BUFF-IN	Buffer Amp Input
14	FIL-IN	Filter Amp Input
15	FIL-OUT	Filter Amp Output
16	PB/REC	PLAY/REC SW Control
17	MIC/LINE	MIC/LINE Input SW Control
18	ICM/OGM	IGM/OGM SW Control
19	MUTE1	Line Mute Control
20	MUTE2	Buffer Output Mute Control
21	COMP-OUT	Comparator Output
22	LINE-OUT	Line Amp Output
23	NC	No Connect
24	LINE-IN	Line Amp Input
25	COMP-ADJ	Comparator Level Adjustment
26	BUFF-OUT	Buffer Amp Output
27	VOX-DET	VOX Detector
28	ALC-DET	ALC Detector
29	V_{REF}	Reference
30	V_{CC}	V_{CC}

Pin Function (HA12189MP)

Pin No.	Symbol	Description
1	GND	GND
2	ICM	ICM Input/Output
3	OGM	OGM Input/Output
4	MIC	MIC Input
5	LINE	LINE Input
6	ALC-DC-CUT	ALC DC CUT
7	ALC	ALC Input
8	PRE-IN	Pre Amp Input
9	PB-FB	PLAY Pre Amp Output
10	REC-FB	REC Pre Amp Output
11	PRE-OUT	Pre Amp Output
12	BUFF-IN	Buffer Amp Input
13	FIL-IN	Filter Amp Input
14	FIL-OUT	Filter Amp Output
15	PB/REC	PLAY/REC SW Control
16	MIC/LINE	MIC/Line Input SW Control
17	ICM/OGM	IGM/OGM SW Control
18	MUTE1	Line Mute Control
19	MUTE2	Buffer Output Mute Control
20	COMP-OUT	Comparator Output
21	LINE-OUT	Line Amp Output
22	LINE-IN	Line Amp Input
23	COMP-ADJ	Comparator Level Adjustment
24	BUFF-OUT	Buffer Amp Output
25	VOX-DET	VOX Detector
26	ALC-DET	ALC Detector
27	V_{REF}	Reference
28	Vcc	Vcc

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	Vcc (Max)	7.0	V	1
Power Dissipation	P_T (Max)	300	mW	
Operating Temperature	Topr	–20 to + 70	°C	
Storage Temperature	Tstg	–55 to + 125	°C	

Note 1) Standard Operating Voltage: Vcc = 6.0 V ± 0.5 V

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics (Ta = 25°C, Vcc = 6 V)

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Application Terminal	Remark
Quiescent Current	I_Q	No-signal Pin ⑯ (⑮) = 5 V	—	12	19	mA	㉚(㉘)	
PB Voltage Gain	Gv1	Vin = –74 dBm	69	72	75	dB	②→㉒ (②→㉑)	
PB Maximum Output Voltage	Vom1	THD = 10%	1.2	1.7	—	Vrms		
PB Distortion Ratio	T.H.D1	Vin = –74 dBm	—	0.5	2	%		1
REC Voltage Gain	Gv2	Vin = –70 dBm	48	51	54	dB	⑤→②	
REC Maximum Input Voltage	Vim1	THD ≤ 2%	—	—	–30	dBm		
REC Distortion Ratio	T.H.D2	Vin = –50 dBm	—	0.7	2	%		1
REC Voltage When ALC Operating	Gv ALC	Vin = –50 dBm	–9	–6	–3	dBm		
Buffer Voltage Gain	Gv3	PB Mode Vin = –74 dBm	52	55	58	dB	②→㉖ (②→㉔)	
Buffer Maximum Output Voltage	Vom2	PB Mode THD = 10%	0.7	1.0	—	Vrms		
Buffer Distortion Ratio	T.H.D3	PB Mode Vin = –74 dBm	—	0.6	2	%		1
Buffer Mute Attenuation	ATT1	Vo = 0 dBm PB Mode Pin ⑳(⑲) = 5 V	—	–65	–40	dB	②→㉖ (②→㉔)	1
PB Mute Attenuation	ATT2	Vo = 0 dBm PB Mode Pin ⑲(⑱) = 5 V	—	–65	–40	dB	②→㉒ (②→㉑)	1
Comparator H Output Voltage	V_{OH}	Pin25 (23) = 1.9 V REC Mode Vin = –60 dBm	3.8	4.5	5.0	V	㉑ (⑳)	
Comparator L Output Voltage	V_{OL}	Pin25 (23) = 1.9 V REC Mode No-Signal	–0.3	0	0.5	V		
Control H Input Voltage	V_{IH}	Lo Mode → Hi Mode Change Voltage	3.8	—	Vcc	V	⑯→⑳ (⑮→⑲)	
Control L Input Voltage	V_{IL}	Hi Mode → Lo Mode Change Voltage	0	—	0.5	V		

Remark 1) B.P.F in 400 Hz to 15 kHz

Number inside ( ) shows terminal pin number for HA12189MP.

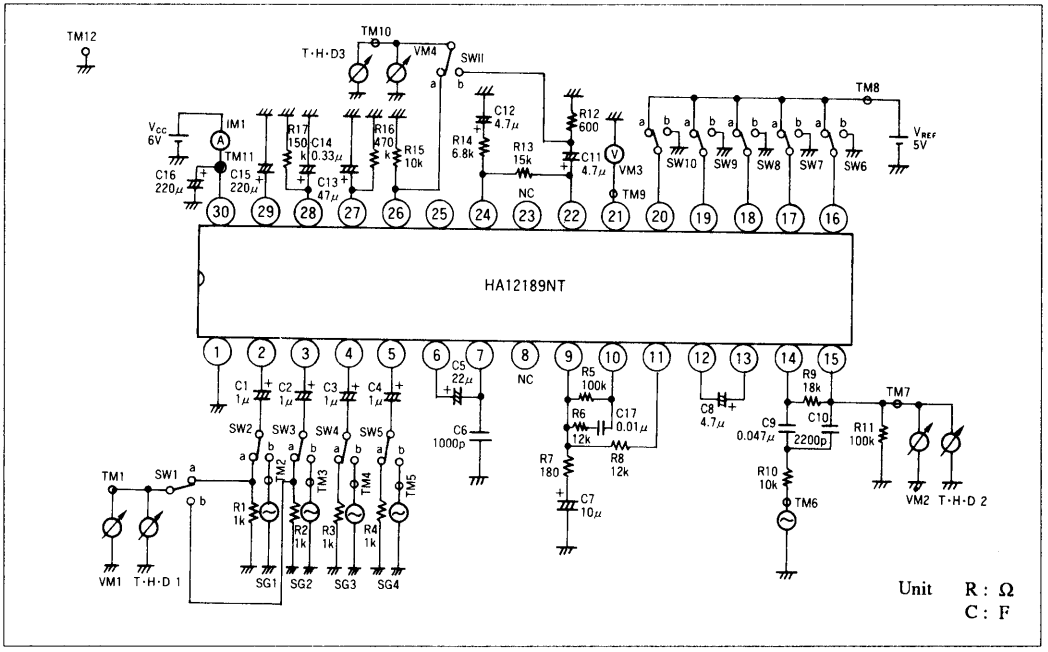


Figure 2-1 Test Circuit (HA12189NT)

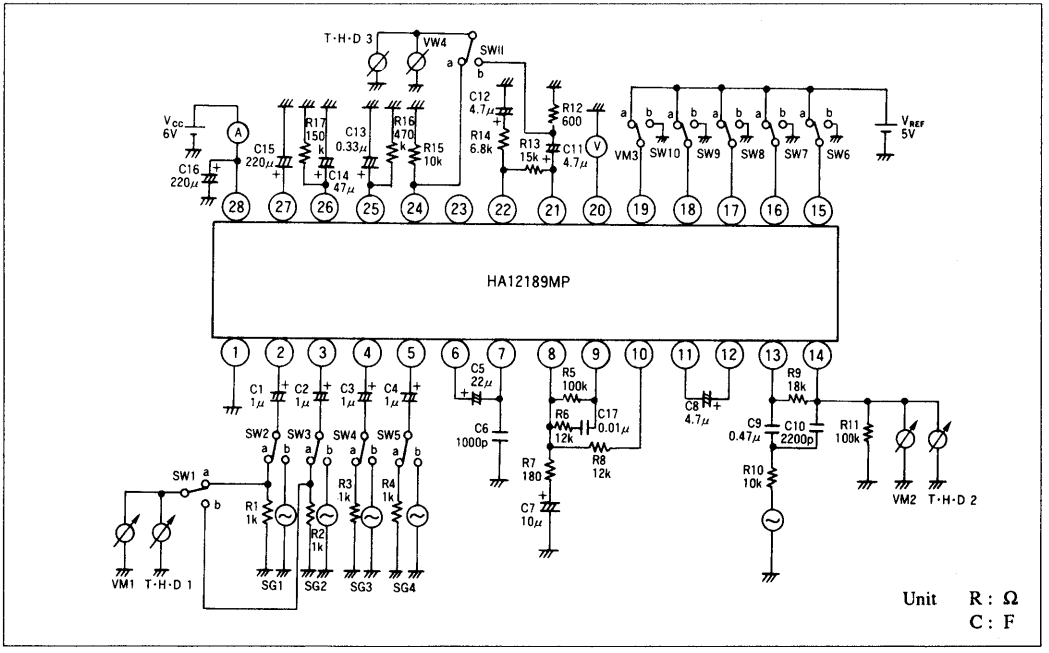


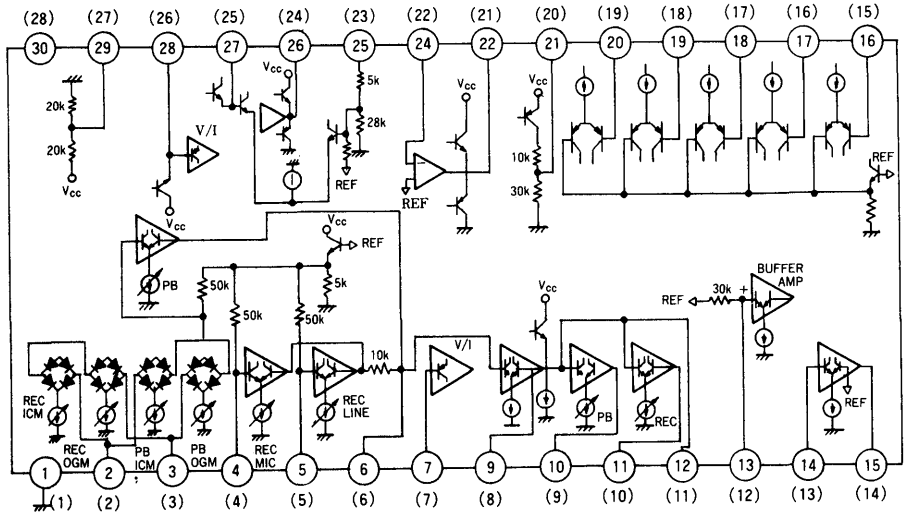
Figure 2-2 Test Circuit (HA12189MP)

Table 1. Switched Position Table

No.	Symbol	Control Terminal					SW Position						Source Signal Measurement
		16(15)	17(16)	18(17))	19(18)	20(19)	SW1	SW2	SW3	SW4	SW5	SW11	
1	Iq	H	L	L	L	L	a	a	a	a	a	a	IMI
2	Gv1	↓	↓	H	↓	↓	↓	b	↓	↓	↓	b	SG1, VM4
3	Vom1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG1, VM4, THD3
4	THD1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
5	Gv2	L	↓	↓	↓	↓	↓	a	↓	↓	b	a	SG4, VM1
6	Vim1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG4, VM1 THD1
7	THD2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
8	Gv ALC	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG4, VM1
9	Gv3	H	↓	↓	↓	↓	↓	b	↓	↓	a	↓	SG1, VM4
10	Vom2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SG1, VM4 THD3
11	THD3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
12	ATT1	↓	↓	↓	L	H	↓	↓	↓	↓	↓	↓	SG1, VM4
13	ATT2	↓	↓	↓	H	L	↓	↓	↓	↓	↓	b	
14	V_{OH}	L	↓	↓	L	↓	↓	a	↓	↓	b	↓	SG4, VM3
15	V_{OL}	↓	↓	↓	↓	↓	↓	↓	↓	↓	a	↓	
16	V_{IH}	H	H	↓	H	H	↓	↓	↓	↓	↓	↓	—
17	V_{IL}	L	L	L	L	L	↓	↓	↓	↓	↓	↓	—

*H = 5 (V), L = 0 (V)

Number inside ( ) shows terminal pin number for HA12189MP



- Resistance Value: Typ.
- Number inside ( ) shows terminal pin number for HA12189MP

Figure 3 Input/Output Circuit

Function Description (HA12189NT)

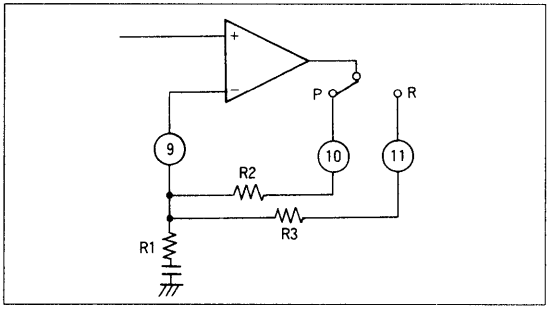
Signal-pass to Control SW (ex.)

Input	Output	⑯	⑰	⑱	Pass
MIC ④	VOICE LSI ⑫	L	H	L	④→(PRE AMP)→⑫→VOICE LSI
LINE ⑤	ICM HEAD ②	L	L	H	⑤→(PRE AMP)→(BUF1)→(PRE AMP)→② 20 dB 0 dB
ICM ②	Speaker BUFFER ㉖	H	*	H	②→(PRE AMP)→(BUF2)→㉖→SP 12 dB
OGM ③	LINE Output ㉒	H	*	L	③→(PRE AMP)→(BUF1)→(LINE AMP)→㉒ 20 dB 10 dB
VOICE LSI ⑮	LINE Output ㉒	H	*	L	VOICE →(FILTER AMP)→⑮→③→the same as LSI No. 4
LINE ⑤	OTMF Receiver ⑫	L	L	*	⑤→(PRE AMP)→⑫→DTMF Receiver
MARKER OSC ⑨	OGM ③	L	L	L	⑨→(PRE AMP)→(BUF1)→(REC AMP)→③ 0 dB 20 dB 0 dB

Control SW (Possible to be controlled by CPU)

Level	⑯	⑰	⑱	⑲	⑳
H	PLAY	MIC	ICM	ON	ON
L	REC	LINE	OGM	OFF	OFF

Pre Amp



SW	P	R
Gain	(1 + R2/R1)	(1 + R3/R1)

- Gain is controlled by voltage of Pin 16.

IGM/OGM

	ICM	OGM	PIN 2
1	cassette	cassette	a dotted line
2	cassette	VOICE LSI	a solid line

Function Description (HA12189MP)

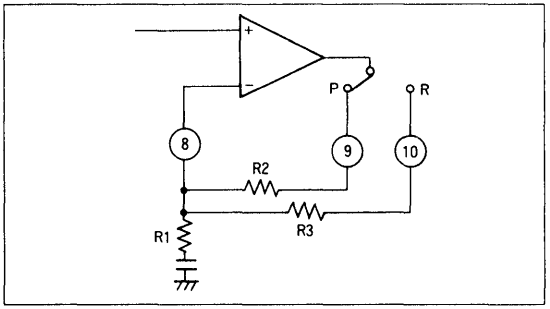
Signal-pass to Control SW (ex.)

No.	Input	Output	⑮	⑯	⑰	Pass
1	MIC ④	VOICE LSI ⑪	L	H	L	④→(PRE AMP)→⑪→VOICE LSI
2	LINE ⑤	ICM ② HEAD	L	L	H	⑤→(PRE AMP)→(BUF1)→(PRE AMP)→② 20 dB 0 dB
3	ICM ②	Speaker BUFFER ㉔	H	*	H	②→(PRE AMP)→(BUF2)→㉔→SP 12 dB
4	OGM ③	LINE ㉑ Output	H	*	L	③→(PRE AMP)→(BUF1)→(LINE AMP)→㉑ 20 dB 10 dB
5	VOICE LSI ⑭	LINE ㉑ Output	H	*	L	VOICE LSI →(FILTER AMP)→⑭→③→the same as No. 4
6	LINE ⑤	OTMF Receiver ⑪	L	L	*	⑤→(PRE AMP)→⑪→DTMF Receiver
7	MARKER OSC ⑧	OGM ③	L	L	L	⑧→(PRE AMP)→(BUF1)→(REC AMP)→③ 0 dB 20 dB 0 dB

Control SW (Possible to be controlled by CPU)

Level	⑮	⑯	⑰	⑱	⑲
H	PLAY	MIC	ICM	ON	ON
L	REC	LINE	OGM	OFF	OFF

Pre Amp



SW	P	R
Gain	(1 + R2/R1)	(1 + R3/R1)

- Gain is controlled by voltage of Pin ⑮.

IGM/OGM

	ICM	OGM	PIN 2
1	cassette	cassette	a dotted line
2	cassette	VOICE LSI	a solid line

External Component

Part No.	Standard Value	Function	Influence	
			Standard Value or less	Standard Vallue or more
C1	1 μ	DC Cut		
C2	1 μ	DC Cut		
C3	1 μ	DC Cut		
C4	1 μ	DC Cut		
C5	22 μ	DC Cut	Frequency characteristics becomes worse	Rising of AGC becomes slow
C6	1000p	Oscillation stop	ALC circuit oscillation	Frequency characteristics becomes worse
C7	10 μ	High Cut-off Frequency	Large cut-off frequency	Small cut-off frequency
C8	4.7 μ	DC Cut	Breaking off when attacking	
C9		Constant when filter		
C10				
C11	4.7 μ	DC Cut		
C12		Low cut-off Frequency	Small cut-off frequency	Large cut-off frequency
C13	0.33 μ	Detection circuit	Unstability of comparator operating	Delay of comparator response
C14	47 μ	Constant when ALC	Distortion ratio becomes worse	Long attack recovery time
C15	220 μ	Ripple Rejection	Ripple rejection ratio becomes worse	
C16	220 μ	Supply Voltage Ripple Rejection	Ripple rejection ratio becomes worse	
C17	0.01 μ	Low Cut-off Frequency	Small cut-off frequency	Large cut-off frequency
R5	100k	PB Gv	Small Gv	Large Offset Voltage of Pin ㉖ (㉔)
R6	12k	PB Gv	Small Gv	Large Gv
R7	180	Pre. Amp Gv	Large Gv	Small Gv
R8	12k	REC Gv	Small Gv	Large Gv
R9		Filter Amp Gv	Small Gv	Large Offset Voltage of Pin ⑮ (⑭)
R10		Filter Amp Gv	Large Gv	Small Gv
R13		Line Amp Gv	Small Gv	Large Gv
R14		Line Amp Gv	Large Gv	Small Gv
R16	470k	Detection Circuit	Unstability of Comparator Operating	Delay of Comparator response

Number inside ( ) shows terminal pin number for HA12189MP

HD4074008

HMCS400 Series ZTAT Microcomputer

Description

The HD4074008 is single chip microcomputer unit which includes 8K words of PROM and 512 digits of RAM.

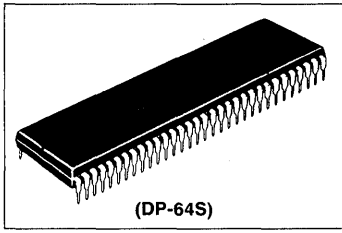
On chip PROM can be programmed by the same procedure as that of 27256 (Vpp = 12.5 V).

The HD4074008 is a member of the HMCS400 series with powerful and efficient programming architecture.

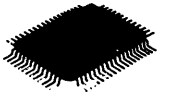
Features

- Instruction Set is compatible with HMCS402/404/408
- 8192 Words × 10 bit PROM
- 512 Digits × 4 bit RAM
- 58 I/O Pins, including 12 large current I/O pins (15 mA) [I/O Pin Circuit Type is all open drain]
- Two Timer/Counters
- Clock Synchronous 8 bit Serial Interface
- Five Interrupts
  - —External 2
  - —Internal 3
- Subroutine Stack
  - —Up to 16 levels including interrupts
- Two Low Power Dissipation Modes
  - —Standby Mode
  - —Stop Mode
- On chip oscillator
  - —External Connection of Crystal or Ceramic Filter (externally drivable)
- Minimum Instruction Execution Time 0.89 μs
- Operation Mode
  - —MCU Mode
  - —PROM Mode
- Package
  - —Shrink Type 64 pin Plastic DIP
  - —Shrink Type 64 pin Ceramic DIP with window
  - —64 pin Flat Plastic Package

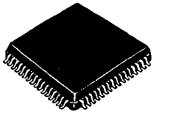
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



(DP-64S)



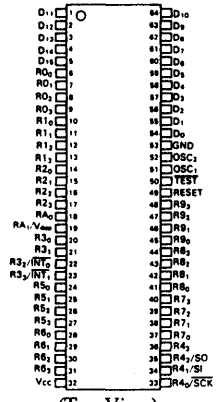
(FP-64)



(FP-64A)

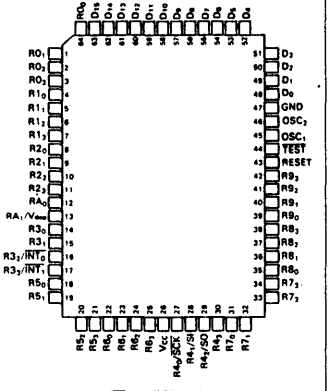
Pin Arrangement

DP-64S, DC-64S



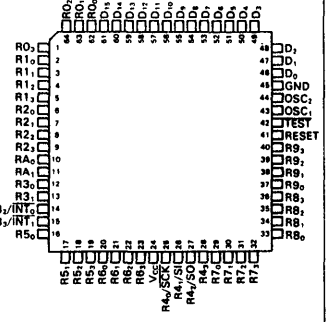
(Top View)

FP-64



(Top View)

FP-64A



(Top View)

HD404618/HD4074618

4-bit Single-Chip Microcomputer

Description

The MCU is a microcomputer unit which has the powerful and efficient architecture of the HMCS400 family. The MCU incorporates a high-precision dual-tone multi-frequency (DTMF) circuit, LCD driver/controller, voltage comparator, and 32-kHz watch oscillator circuit.

The HD4074618, incorporating PROM, is a ZTAT™ microcomputer that can dramatically shorten system development periods and smooth the process from debugging to mass production.

Features

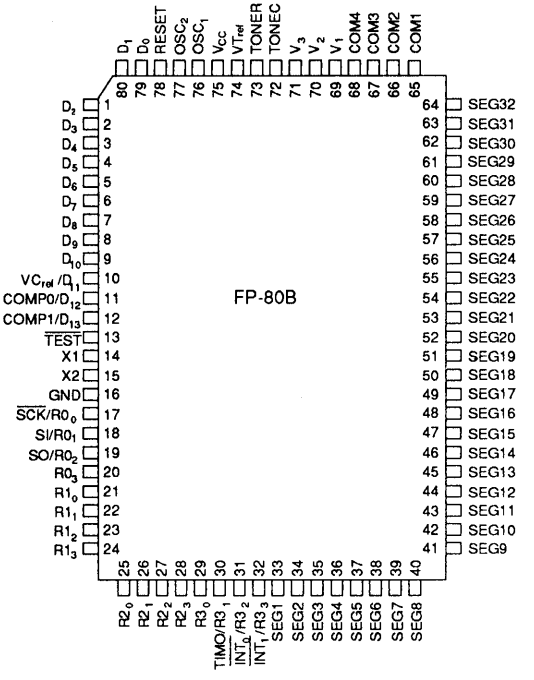
- 8192-word × 10-bit ROM
- 1184-digit × 4-bit RAM
- 30 I/O pins
  - — 10 high-current output pins
  - — CMOS I/O pin circuit configuration
  - — Input/output pull-up MOS can be selected by software
- On-chip DTMF generator
- 16-digit LCD driver
- Three timer/counters
- Clock-synchronous 8-bit serial interface
- Six interrupt sources
  - — Two external sources
  - — Four internal sources
- Subroutine stack
  - — Up to 16 levels, including interrupts
- Instruction cycle time
  - — 10 µs (f_{osc} = 400 kHz)
  - — 5 µs (f_{osc} = 800 kHz)
- Four low-power dissipation modes
  - — Stop mode
  - — Standby mode
  - — Watch mode
  - — Subactive mode (option)
- Built-in oscillator
  - — Crystal or ceramic filter (external clock also enabled)
- Voltage comparator (2 channels)
- Two operating modes
  - — MCU mode
  - — PROM mode (HD4074618)
- Package
  - — 80-pin plastic flat package (FP-80B) (FP-80A)

Ordering Information

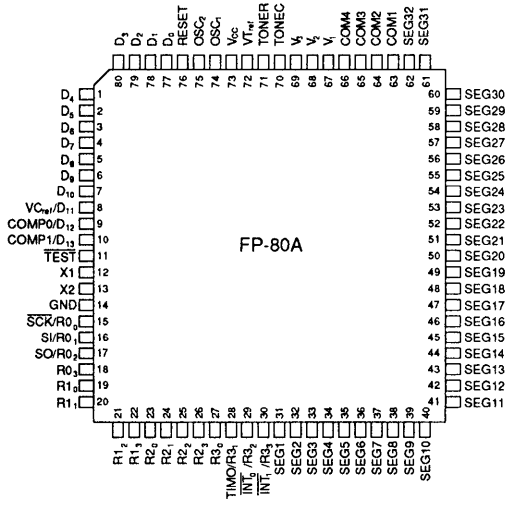
Type	Product Number	Clock Frequency (kHz)	Package
Mask ROM	HD404618FS	400/800	FP-80B
	HD404618H		FP-80A
ZTAT™	HD4074618FS	400/800	FP-80B
	HD4074618H		FP-80A

ZTAT™ is a registered trandemark of Hitachi Ltd.

Pin Arrangement



(Top View)



(Top View)

Pin Description

Pin Number				Pin Number			
FP-80B	FP-80A	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O
1	79	D_2	I/O	41	39	SEG9	O
2	80	D_3	I/O	42	40	SEG10	O
3	1	D_4	I/O	43	41	SEG11	O
4	2	D_5	I/O	44	42	SEG12	O
5	3	D_6	I/O	45	43	SEG13	O
6	4	D_7	I/O	46	44	SEG14	O
7	5	D_8	I/O	47	45	SEG15	O
8	6	D_9	I/O	48	46	SEG16	O
9	7	D_{10}	I	49	47	SEG17	O
10	8	D_{11}/VC_{ref}	I	50	48	SEG18	O
11	9	D_{12}/COMP0	I	51	49	SEG19	O
12	10	D_{13}/COMP1	I	52	50	SEG20	O
13	11	$\overline{TEST}$	I	53	51	SEG21	O
14	12	X1	I	54	52	SEG22	O
15	13	X2	O	55	53	SEG23	O
16	14	GND		56	54	SEG24	O
17	15	$R0_0/\overline{SCK}$	I/O	57	55	SEG25	O
18	16	$R0_1$/SI	I/O	58	56	SEG26	O
19	17	$R0_2$/SO	I/O	59	57	SEG27	O
20	18	$R0_3$	I/O	60	58	SEG28	O
21	19	$R1_0$	I/O	61	59	SEG29	O
22	20	$R1_1$	I/O	62	60	SEG30	O
23	21	$R1_2$	I/O	63	61	SEG31	O
24	22	$R1_3$	I/O	64	62	SEG32	O
25	23	$R2_0$	I/O	65	63	COM1	O
26	24	$R2_1$	I/O	66	64	COM2	O
27	25	$R2_2$	I/O	67	65	COM3	O
28	26	$R2_3$	I/O	68	66	COM4	O
29	27	$R3_0$	I/O	69	67	V_1	
30	28	$R3_1$/TIMO	I/O	70	68	V_2	
31	29	$R3_2/\overline{INT_0}$	I/O	71	69	V_3	
32	30	$R3_3/\overline{INT_1}$	I/O	72	70	TONEC	O
33	31	SEG1	O	73	71	TONER	O
34	32	SEG2	O	74	72	VT_{ref}	
35	33	SEG3	O	75	73	V_{CC}	
36	34	SEG4	O	76	74	OSC_1	I
37	35	SEG5	O	77	75	OSC_2	O
38	36	SEG6	O	78	76	RESET	I
39	37	SEG7	O	79	77	D_0	I/O
40	38	SEG8	O	80	78	D_1	I/O

Pin Functions

Power Supply

V_{CC}: Apply power voltage to this pin.

GND: Connect to ground.

$\overline{TEST}$: Used for test purposes only. Connect it to V_{CC}.

RESET: Resets the MCU.

Oscillators

OSC_1, OSC_2: Used as pins for the internal oscillator circuit. They can be connected to a ceramic filter resonator or to an external oscillator circuit.

X1, X2: Used for a 32.768-kHz crystal oscillator that acts as a clock.

Ports

D_0 – D_{13} (D Port): Input/output port addressable by individual bits. D_0 – D_9 are I/O pins and D_{10} – D_{13} are input pins. D_0 – D_9 are high current output pins (15 mA, max). D_{11} – D_{13} are also available as voltage comparators.

R0 – R3 (R Ports): Input/output ports addressable in 4-bit units. $R0_0$, $R0_1$, $R0_2$, $R3_1$, $R3_2$, and $R3_3$, are multiplexed with $\overline{SCK}$, SI, SO, TIMO, $\overline{INT_0}$, and $\overline{INT_1}$, respectively.

Interrupts

$\overline{INT_0}$, $\overline{INT_1}$: Input external interrupts to the MCU. $\overline{INT_1}$ is also used as an external event input for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$, respectively.

Serial Communications Interface

$\overline{SCK}$: Input/output SCI clock pin multiplexed with $R0_0$.

SI: SCI receive data input pin multiplexed with $R0_1$.

SO: SCI transmit data output pin multiplexed with $R0_2$.

Timer

TIMO: Outputs a variable-duty square wave. It is multiplexed with $R3_1$.

LCD Driver/Controller

V_1, V_2, V_3: Power supply pins for the LCD driver. Internal resistors provide the voltage level for each pin. The voltage condition is $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$.

COM1 – COM4: Common signal output pins for LCD display.

SEG1 – SEG32: Segment signal output pins for LCD display.

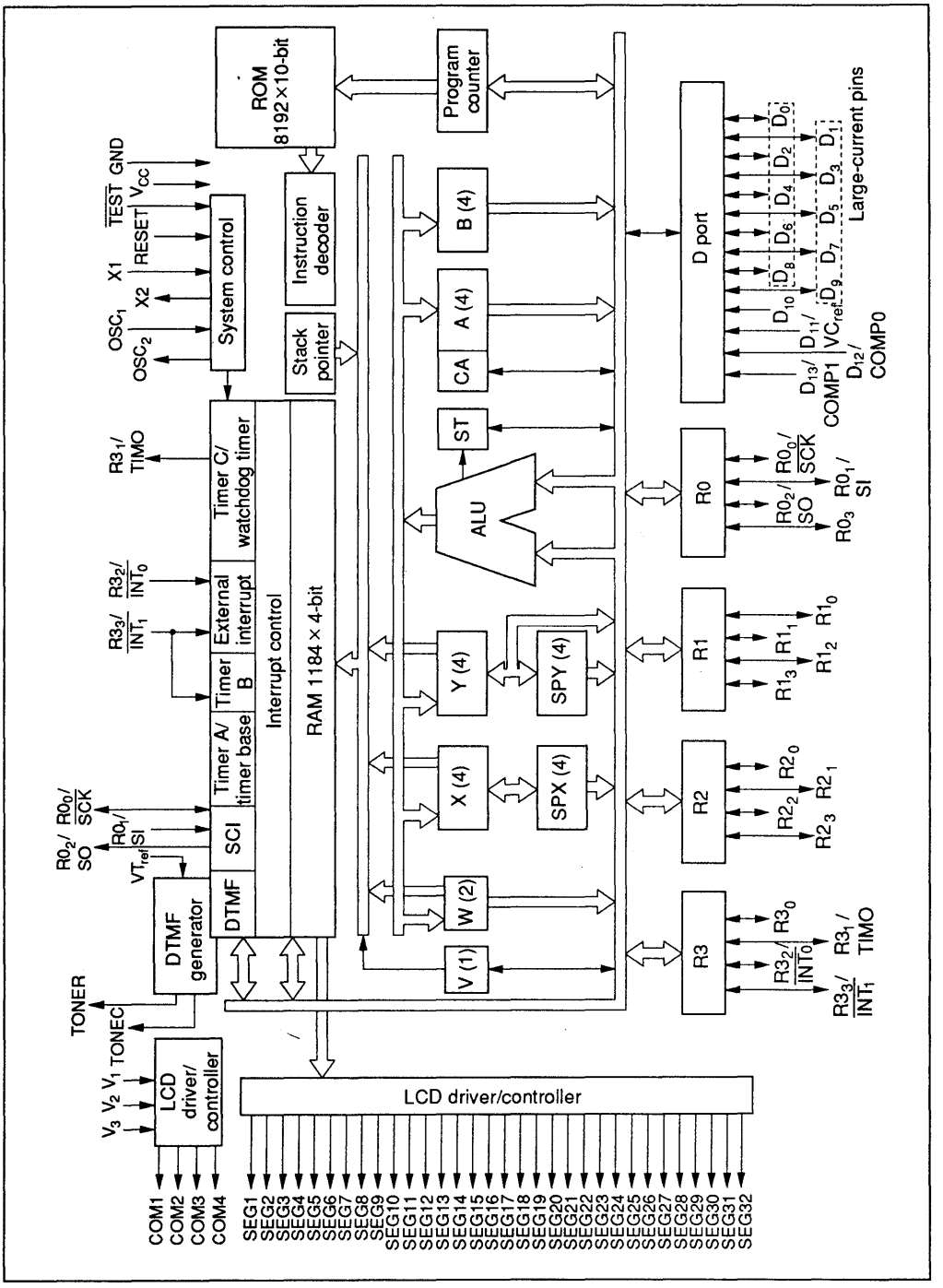
DTMF Generator

TONER, TONEC, VT_{ref}: DTMF signal output pins. TONER and TONEC transmit signals for ROW and COLUMN, respectively. VT_{ref} is a reference voltage for DTMF signals. Apply condition $V_{CC} \geq VT_{ref} \geq GND$ to VT_{ref}.

Voltage Comparator

COMP0, COMP1, VC_{ref}: COMP0 and COMP1 are analog inputs for the voltage comparator. VC_{ref} is a reference voltage pin that inputs the threshold voltage of the analog input pin.

Block Diagram



Memory Map

ROM Memory Map

The MCU contains a 8,192-word × 10-bit ROM. The ROM memory map is shown in figure 1, and the ROM is described below.

Vector Address Area ($0000 – $000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt service routines. After an MCU reset or interrupt execution, the program starts from the vector address.

Zero-Page Subroutine Area ($0000 – $003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000 – $0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000 – $1FFF): Used for program coding.

RAM Memory Map

The MCU contains a 1184-digit × 4-bit RAM area consisting of a data area and a stack area. In addition, interrupt control bits and special registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2 and described below.

Interrupt Control Bit Area ($000 – $003, $020 – $023): Used for interrupt control bits and the bit register (figure 3). The register flag area consists of LSON, WDON, TGSP, and DTON flags. Both areas can be accessed only by RAM bit manipulation instructions. In addition, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer.

Register Flag Area ($020 – $023): Consist of the LSON, WDON, TGSP, and DTON flags which are bit registers accessible by the RAM bit manipulation instruction.

The WDON flag can only be set, and only by the SEM/SEMD instruction.

The TGSP flag can be set and reset by the SEM/SEMD and REM/REMD instructions.

The DTON flag can be set, reset, and tested by the SEM/SEMD, REM/REMD, and TMD instructions. Note that the DTON flag is active only in subactive mode, and is normally reset in active mode.

Special Function Register Area ($004 – $01F, $024 – $03F): Used as mode or data registers for serial interface, timer/counters, LCD, and DTMF, and as data control registers for I/O ports. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2.

The SEM/REM, SEMD/REMD instructions can be used for the LCD control register (LCR), but RAM bit manipulation instructions cannot be used for other registers.

LCD Data Area ($050 – $06F): Used for storing LCD data which is automatically output to LCD segments as display data. Data 1 lights the corresponding LCD segment; data 0 extinguishes it. This area can be used as data area.

Data Area ($040 – $2CF, $100 – $2CF; Bank 0, 1): The memory register (MR), which is 16 digits ($040 – $04F) long, can be accessed by the LAMR and XMRA instructions (see figure 4). In the 464 digits from $100 – $2CF, a bank can be selected by the V register (see section on V register).

Stack Area ($3C0 – $3FF): Used for saving the contents of the program counter (PC), status (ST), and carry (CA) at subroutine call (CAL, CALL) and interrupt servicing. This area can be used as a 16-nesting-level subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 4.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

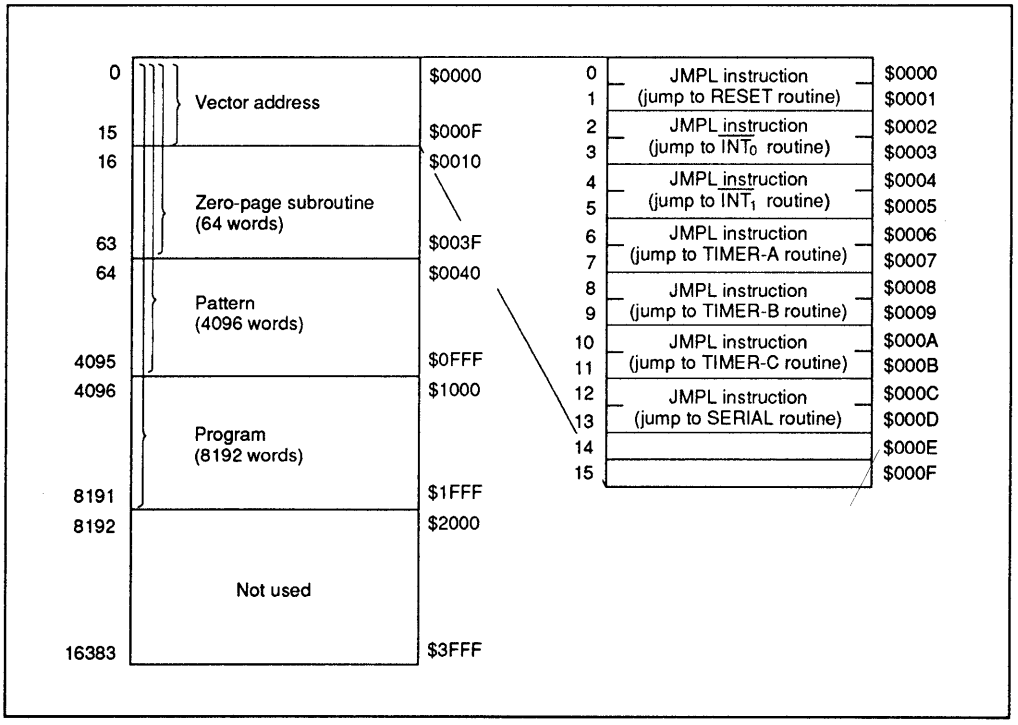


Figure 1 ROM Memory Map

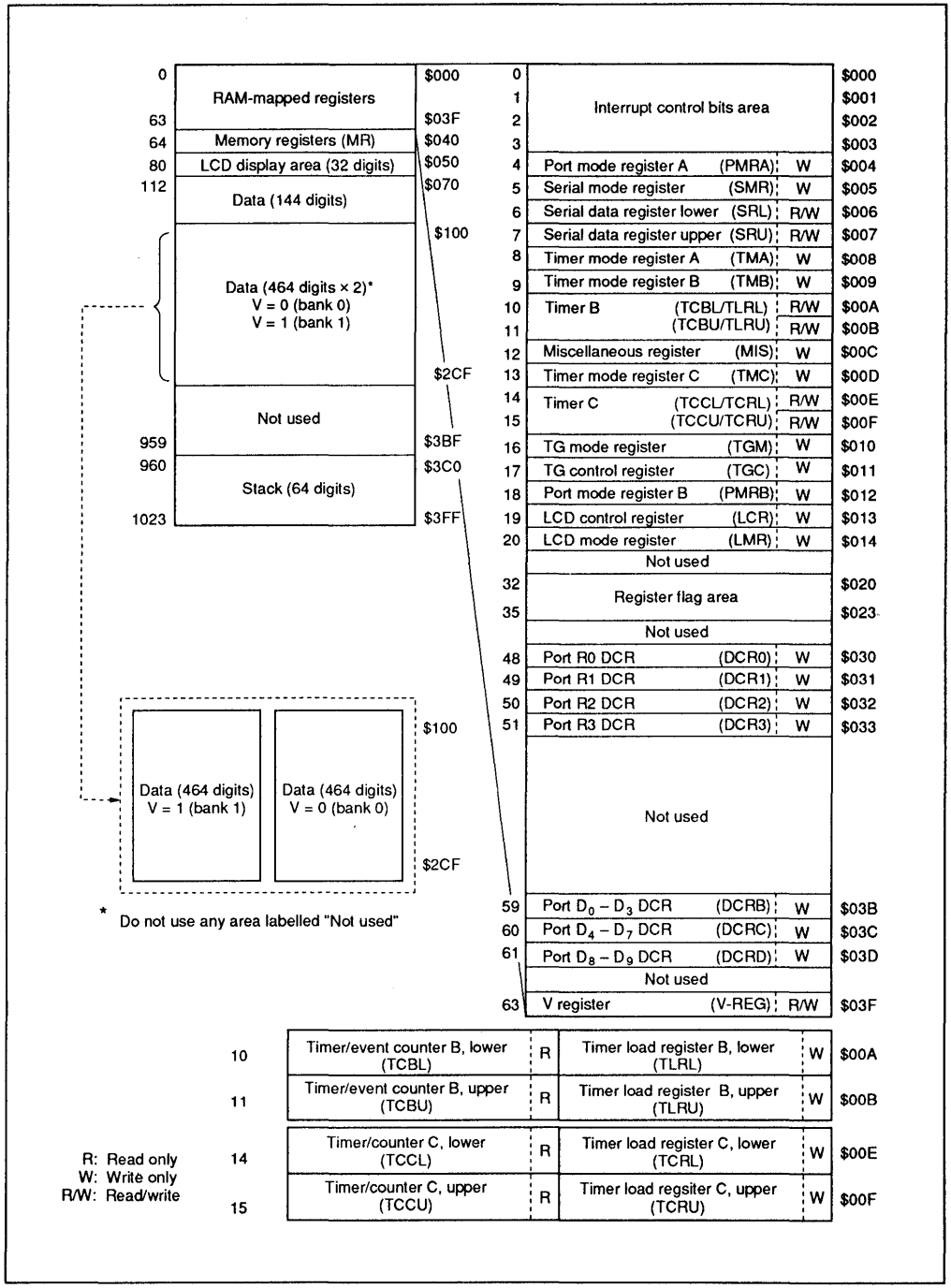


Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	I/E (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003
32	DTON Direct transfer on flag	TGSP (Tone generator speed flag)	WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
	Reserved				$021 to $023

IF: Interrupt request flag
IM: Interrupt mask
I/E: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bit area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM cr TMD instruction. Other instructions have no effect.
Note that the interrupt request flag cannot be set by the SEM or SEMD instruction.
If the RSP bit or a non-existent bit is tested by the TM or TMD instruction, its status is undefined.
The WDON flag can only be used by the SEM or SEMD instruction .
The TGSP flag can only be used by the SEM/SEMD and REM/SEMD instructions (It is reset only by MCU reset).

Figure 3 Configuration of Interrupt Control Bit and Register Flag Area

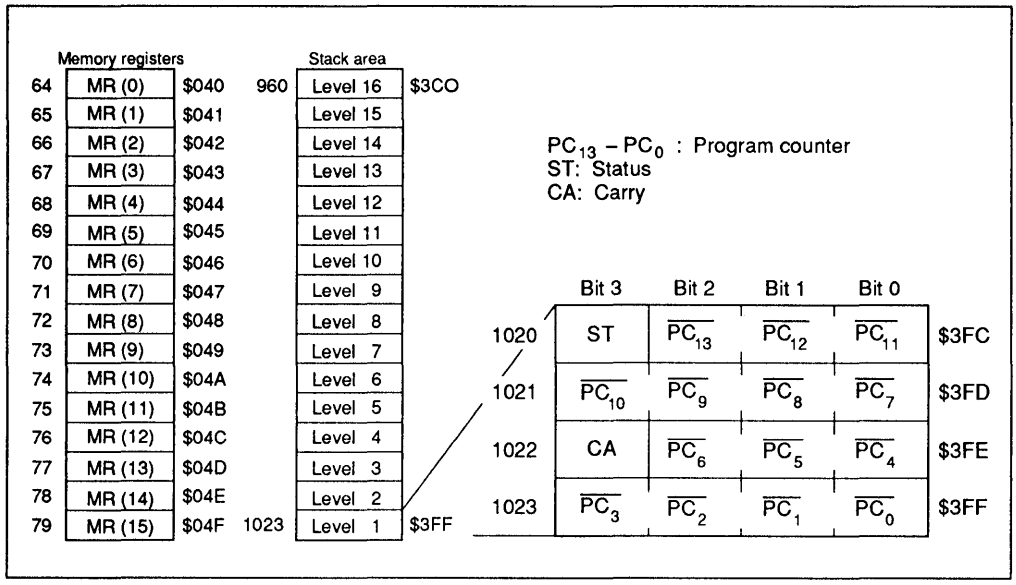


Figure 4 Configuration of Memory Register and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has ten registers and two flags for CPU operations. They are illustrated in figure 5 and described below.

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

V Register (V): Used for RAM address expansion and selecting the bank of RAM addresses $100 – $2CF (464 digits). Thus, when accessing locations $100 – $2CF, specify the value of the V register (V = $0 for bank 0, V = $1 for bank 1). Locations $000 – $00F and $300 – $3FF can be accessed independent of the V register. The V register is located at RAM address $03F.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. During interrupt servicing, a carry is pushed onto the stack and popped from the stack by the RTNI instruction–but not by the RTN instruction.

Status (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, or CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after a BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. During interrupt servicing, the contents of ST are pushed onto the stack and popped from the stack by the RTNI instruction, but not by the RTN instruction.

Program Counter (PC): 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top four bits of the SP are fixed at 1111, a stack of up to 16 levels can be used.

The SP can also be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

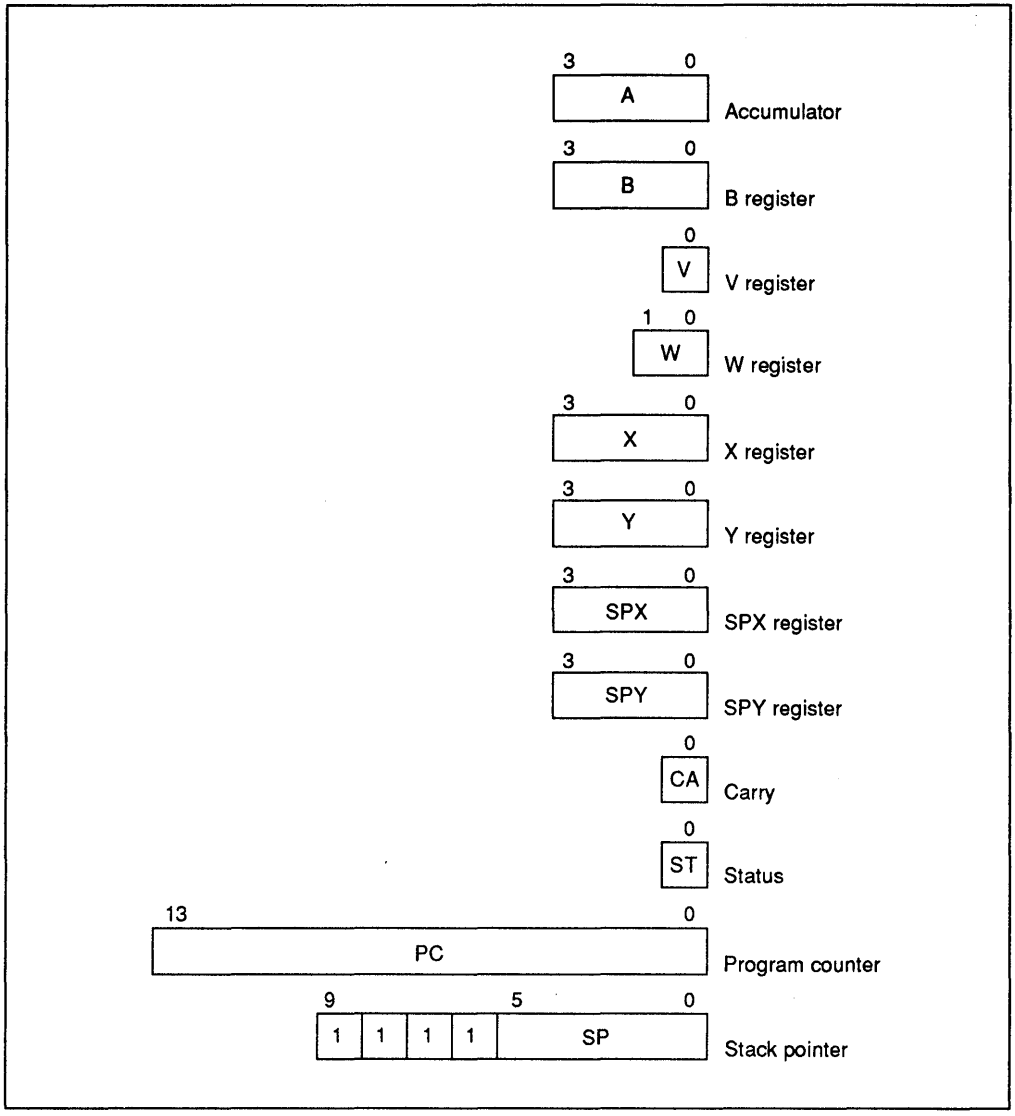


Figure 5 Registers and Flags

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Interrupts

The MCU has six interrupt sources: two external signals ($\overline{INT_0}$ and $\overline{INT_1}$), three timer/counters (timers A, B, and C), and serial interface (SERIAL).

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (I/E) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Servicing: Locations $000 through $003 in RAM space are reserved for interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (I/E) and the IF to 0 and the interrupt mask (IM) to 1.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 lists interrupt priorities and vector addresses, and table 2 lists the interrupt processing conditions for the six interrupt sources.

An interrupt request occurs when the IF is set to 1 and IM to 0. If the I/E is 1 at that point, the interrupt is serviced. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

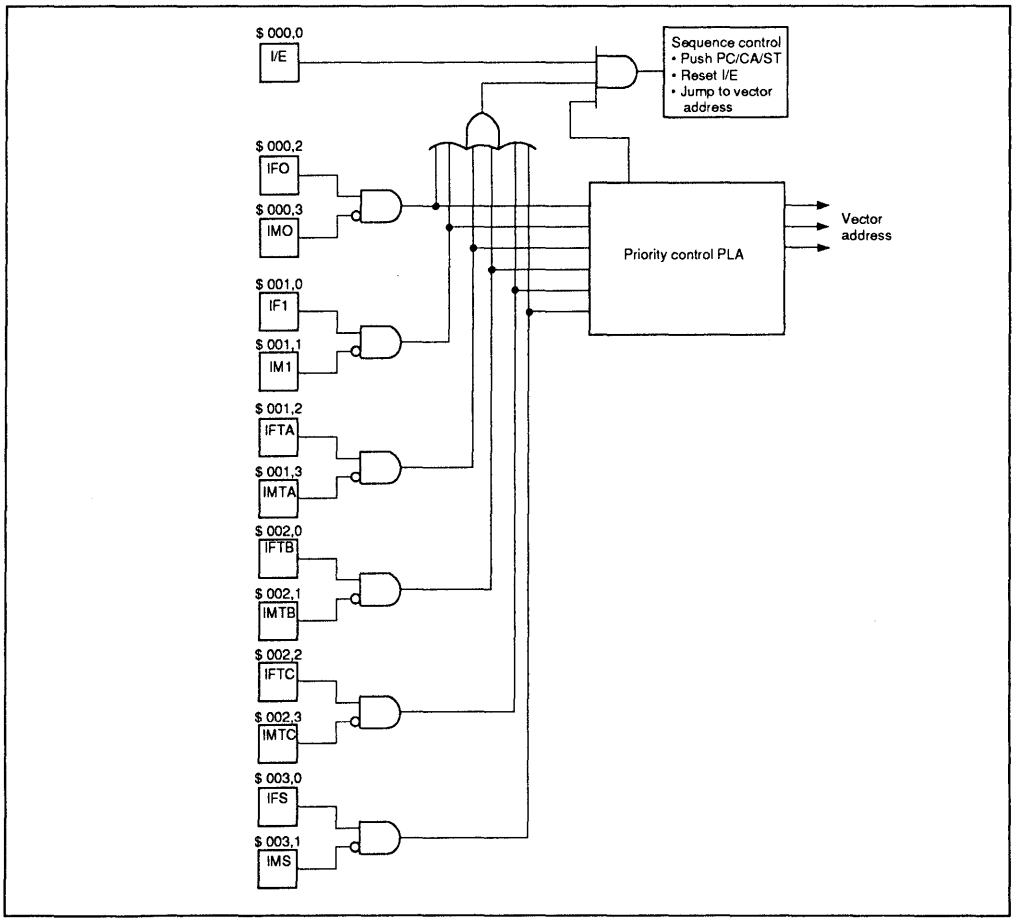


Figure 6 Block Diagram of Interrupt Control Circuit

Figure 7 shows the interrupt processing sequence, and figure 8 shows an interrupt processing flowchart. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The I/E is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program a JMPL instruction at each vector address to branch the program to the start address of the interrupt service program, and reset the IF by a software instruction within the interrupt service program.

Interrupt Enable Flag (I/E: $000, 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as shown in table 3.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): Specified by port mode register A (PMRA: $004).

Table 1 Vector Addresses and Interrupt Priorities

Reset, Interrupt	Priority	Vector Address
RESET		$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
SERIAL	6	$000C

Table 2 Interrupt Processing and Activation Conditions

	Interrupt Cause					
Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Timer C	SERIAL
I/E	1	1	1	1	1	1
IF0·$\overline{IM0}$	1	0	0	0	0	0
IF1·$\overline{IM1}$	*	1	0	0	0	0
IFTA·$\overline{IMTA}$	*	*	1	0	0	0
IFTB·$\overline{IMTB}$	*	*	*	1	0	0
IFTC·$\overline{IMTC}$	*	*	*	*	1	0
IFS·$\overline{IMS}$	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

The $\overline{INT_1}$ input can be used as a clock signal input to timer B. Timer B increments at each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as a timer B external event input, external interrupt mask IM1 must be set to prevent the $\overline{INT_1}$ interrupt request from being accepted (see table 5).

To detect the edge of $\overline{INT_0}$ or $\overline{INT_1}$, more than two instruction cycle times are required (2 t_{cyc} or 2 t_{SUBcyc}).

External Interrupt Request Flags (IF0: $000, 2; IF1: $001, 0): Set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, as shown in table 4.

External Interrupt Masks (IM0: $000, 3, IM1: $001, 1): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as shown in table 5.

Timer A Interrupt Request Flag (IFTA: $001, 2): Set by overflow output from timer A, as shown in table 6.

Timer A Interrupt Mask (IMTA: $001, 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag as shown in table 7.

Timer B Interrupt Request Flag (IFTB: $002, 0): Set by overflow output from timer B, as shown in table 8.

Timer B Interrupt Mask (IMTB: $002, 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as shown in table 9.

Timer C Interrupt Request Flag (IFTC: $002, 2): Set by overflow output from timer C, as shown in table 10.

Timer C Interrupt Mask (IMTC: $002, 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as shown in table 11.

Serial Interrupt Request Flag (IFS: $003, 0): Set when the octal counter counts the eighth transfer clock signal or when data transfer is discontinued by resetting the octal counter, as shown in table 12.

Serial Interrupt Mask (IMS: $003, 1): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as shown in table 13.

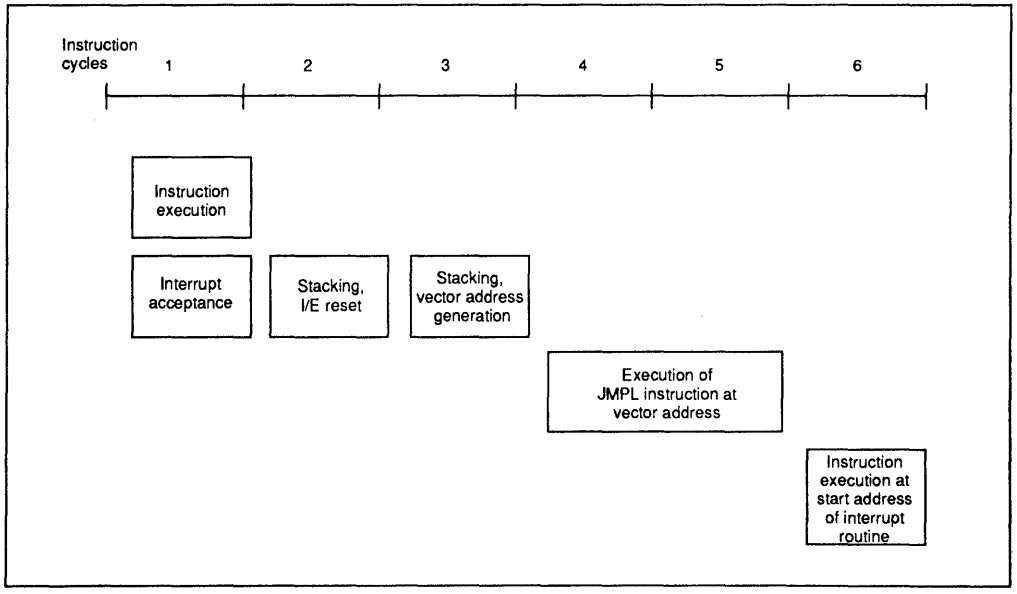


Figure 7 Interrupt Processing Sequence

Table 3 Interrupt Enable Flag

Interrupt Enable Flag (I/E)	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

Table 4 External Interrupt Request Flag

External Interrupt Request Flag (IF0, IF1)	Interrupt Request
0	No
1	Yes

Table 5 External Interrupt Masks

External Interrupt Mask (IM0, IM1)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 6 Timer A Interrupt Request Flag

Timer A Interrupt Request Flag (IFTA)	Interrupt Request
0	No
1	Yes

Table 7 Timer A Interrupt Mask

Timer A Interrupt Mask (IMTA)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 8 Timer B Interrupt Request Flag

Timer B Interrupt Request Flag (IFTB)	Interrupt Request
0	No
1	Yes

Table 9 Timer B Interrupt Mask

Timer B Interrupt Mask (IMTB)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 10 Timer C Interrupt Request Flag

Timer C Interrupt Request Flag (IFTC)	Interrupt Request
0	No
1	Yes

Table 11 Timer C Interrupt Mask

Timer C Interrupt Mask (IMTC)	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 12 Serial Interrupt Request Flag

Serial Interrupt Request Flag (IFS)	Interrupt Request
0	No
1	Yes

Table 13 Serial Interrupt Mask

Serial Interrupt Mask (IMS)	Interrupt Request
0	Enabled
1	Disabled (masked)

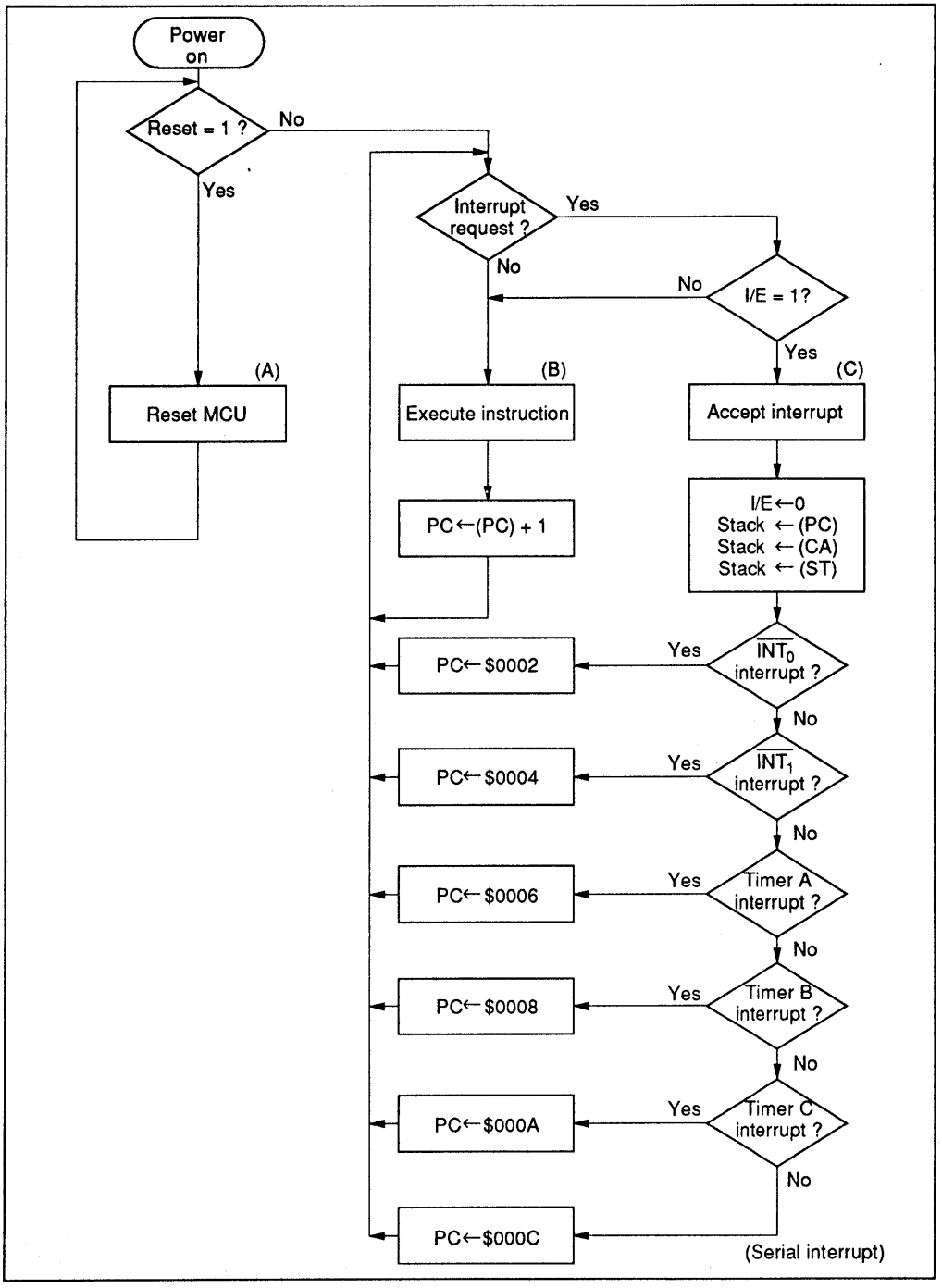


Figure 8 Interrupt Processing Flowchart

Serial Interface

The MCU has a clock-synchronous serial interface which transmits and receives 8-bit data.

The serial interface consists of a serial data register (SR), serial mode register (SMR), port mode register A (PMRA), octal counter, and multiplexers (see figure 9). The $R0_0/\overline{SCK}$ pin and the transmit clock are controlled by writing to the SMR. The transmit clock shifts the contents of the SR, which can be read and written to by software.

The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, starts counting at the falling edge of the transmit clock ($\overline{SCK}$), and it increments at the rising edge of the clock. A serial interrupt request flag is set when the eighth transmit clock signal is input (the serial interface is reset) or when serial transmission is discontinued (the octal counter is reset).

Serial Mode Register (SMR: $005): Four-bit write-only register that controls the $R0_0/\overline{SCK}$ pin, prescaler division ratio, and transmit clock source (table 14 and figure 10). Writing to this register initializes the serial interface.

A write signal input to the serial mode register discontinues the input of the transmit clock to the serial data register and octal counter. Therefore, if a write is performed during data transmission, the octal counter is reset to 000 to stop transmission, and at the same time, the serial interrupt request flag is set.

Write operations are valid from the second instruction execution cycle, so the STS instruction must be executed after at least two cycles have been executed. The serial mode register is initialized to $0 by MCU reset.

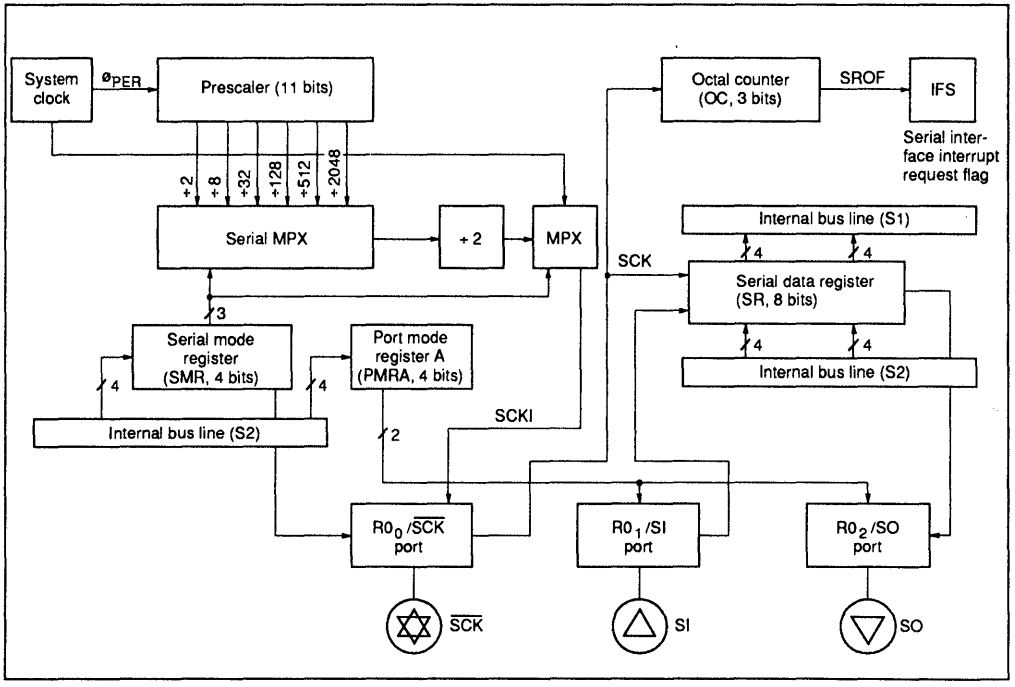


Figure 9 Serial Interface Block Diagram

Serial Data Register (SRL: $006, SRU: $007): Eight-bit read/write register separated into upper and lower digits located at sequential addresses.

Data in this register is output from the SO pin, LSB first, in synchronism with the falling edge of the transmit clock, and data is input LSB first through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 11.

Data cannot be read or written during serial data transmission. If a read/write occurs during transmission, the accuracy of the resultant data cannot be guaranteed.

Selecting and Changing Operating Mode: Table 15 lists the serial interface operating modes. To select an operating mode, use one of these combinations of PMR and SMR settings; to change the operating mode, always initialize the serial interface internally by writing to the SMR.

Serial Interface Operation: Three operating modes are provided for the serial interface; transitions between them are shown in figure 12.

In STS waiting state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed, the serial interface enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts the serial clock register, and activates serial transmission. However, note that if clock output mode is selected, the transmit clock is continuously output but data is not transmitted.

During transmission, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters transmit clock wait state. If the state changes from transmit to another state, the serial interrupt request flag is set by the octal counter reaching 000.

Table 14 Serial Mode Register

SMR	
Bit 3	**$R0_0/\overline{SCK}$ Pin**
0	$R0_0$ port input/output pin
1	SCK input/output pin

SMR			Transmit Clock			
Bit 2	**Bit 1**	**Bit 0**	**$R0_0/\overline{SCK}$ Pin**	**Clock Source**	**Prescaler Division Ratio**	**System Clock Division Ratio**
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
1	1	1	$\overline{SCK}$ input	External clock	—	—

In this state, if the internal clock has been selected, the transmit clock is output in answer to the execution of the STS instruction, but serial transmission is inhibited after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or during transmission, the serial mode register (SMR) must be written to, to initialize the serial interface. The serial interface then enters STS wait state.

If the serial interface shifts from transmission state to another state, the octal counter returns to 000, setting the serial interrupt request flag.

Table 15 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

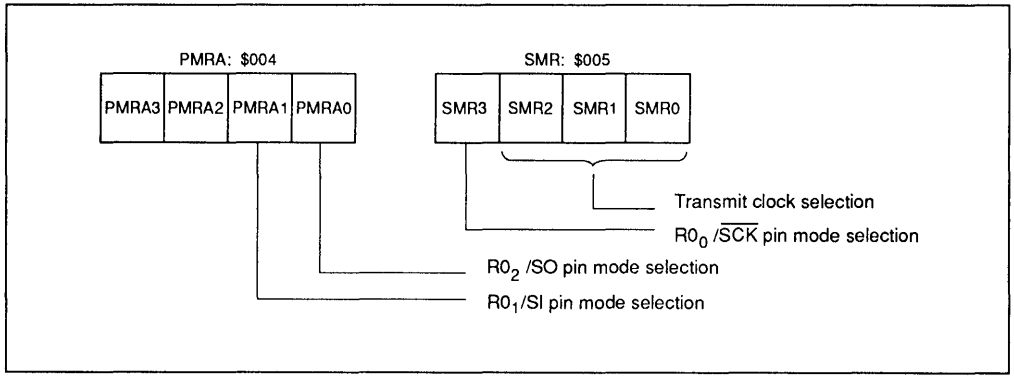


Figure 10 Configurations and Functions of the Mode Registers

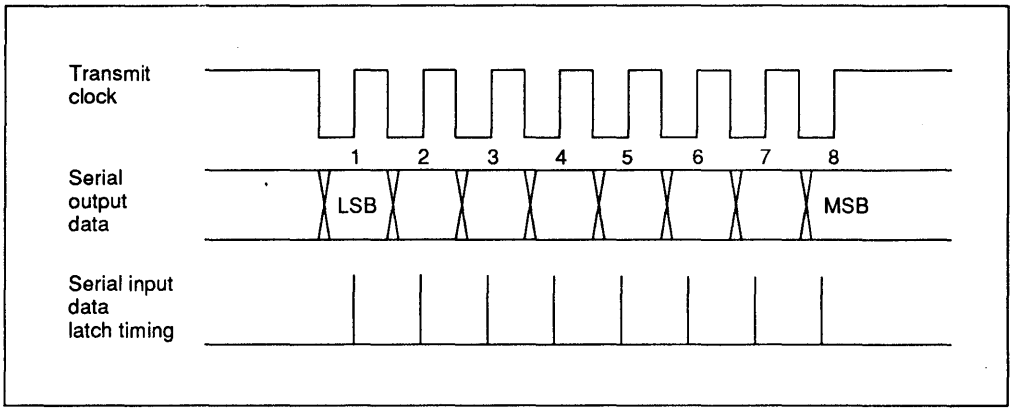


Figure 11 Serial Interface Timing

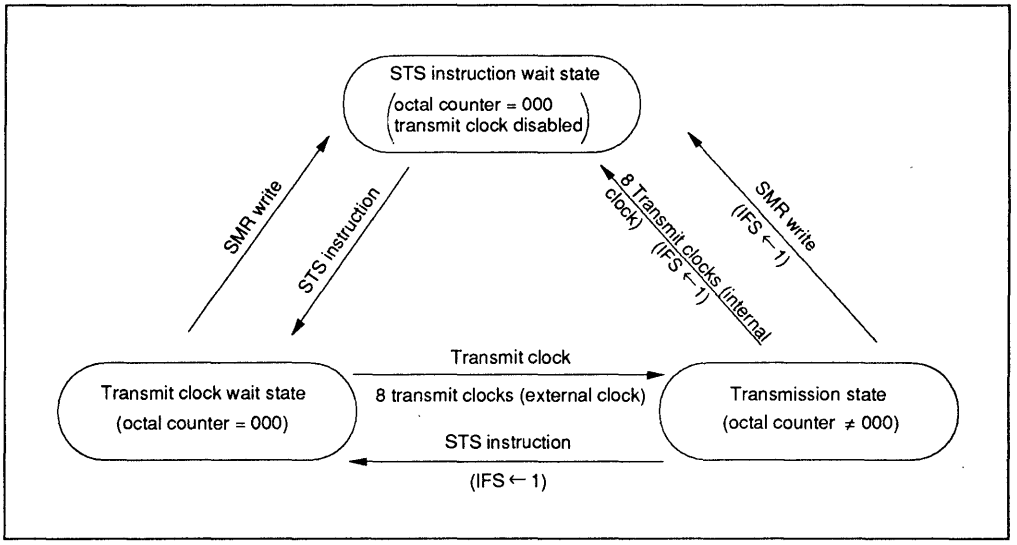


Figure 12 Serial Interface Mode Transitions

Transmit Clock Error Detection: The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error of this type can be detected as shown in figure 13.

If more than eight transmit clocks are input in transmit clock wait state, the serial interface state changes to transmission, transmit clock wait, then back to transmission.

If the serial interface is set to STS wait state by writing data to the SMR after the serial interrupt request flag has been reset, the flag is set again.

Note on Use: The serial interrupt request flag might not be set if the status is changed from transfer by the execution of an SMR write or STS instruction during the first period that the transmit clock is low. To prevent this, program a check that the SCK pin is at 1 (by executing an input instruction for the R1 port) before the execution of an SMR write or STS instruction, to ensure that the serial interrupt request flag is set.

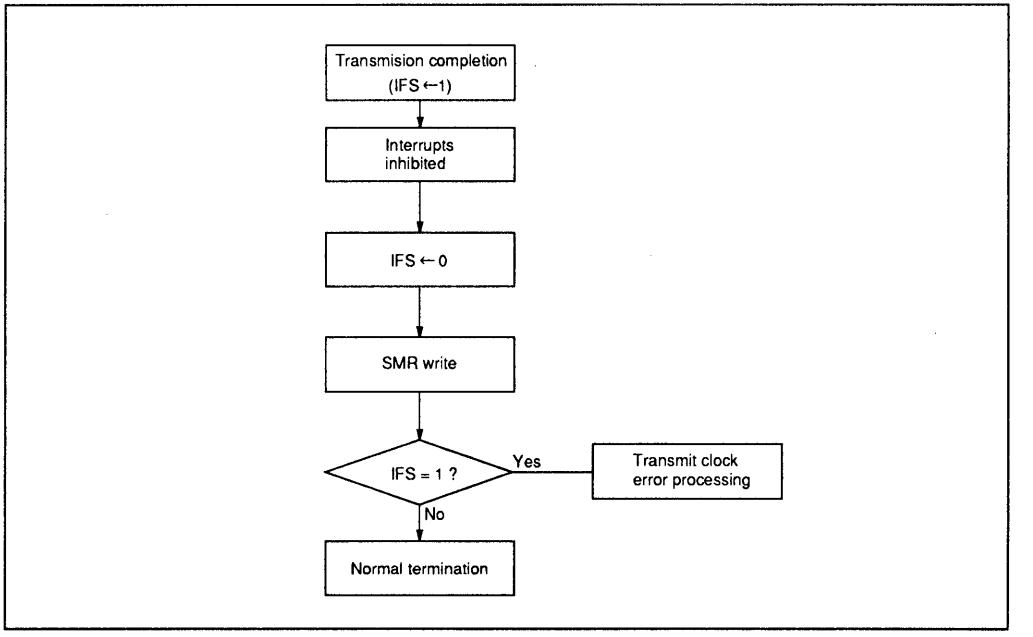


Figure 13 Transmit Clock Error Detection

Timers

The MCU has two prescalers (S and W) and three timer/counters (A, B, and C). Figures 14 and 15 show their diagrams.

Prescaler S: Eleven-bit counter that inputs a system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except at MCU reset and in the stop and watch modes. Of the prescaler S outputs, timer A input clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and the serial mode register (SMR).

Prescaler W: Five-bit counter that inputs the X1 input clock signal divided by eight. Prescaler W output can be selected as a timer A input clock by timer mode register A (TMA).

Timer A: Eight-bit timer that can be used as a clock time-base (figure 14). It is initialized to $00 and incremented at each clock input. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $001, 2) is generated, and timer A restarts from $00.

Timer A is used to generate regular interrupts (every 256 clocks) for measuring times between events. It can also be used as a clock time-base when bit 3 of timer mode register A (TMA) is set to 1. The timer is driven by the 32-kHz oscillator clock frequency divided by prescaler W, and the clock input to timer A is controlled by TMA. In this case, prescaler W and timer A can be initialized to $00 by software.

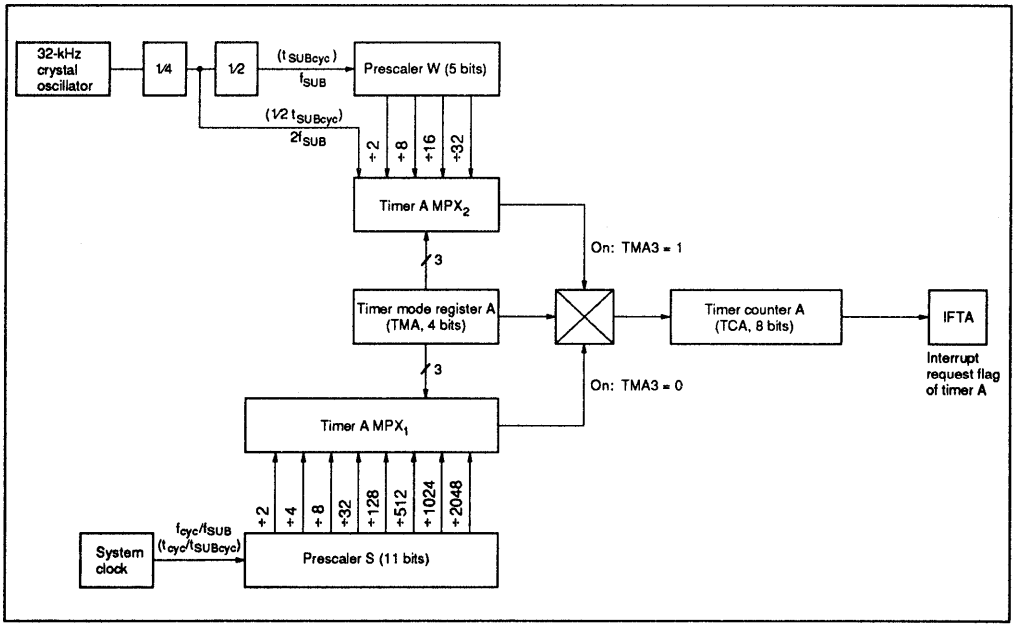


Figure 14 Block Diagram of Timer A

Timer B (TCBL and TLRL: $00A, TCBU and TLRU: $00B): Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer/counter (TCBL and TCBU) located at the same addresses. The eight-bit configuration consists of lower and upper 4-bit digits located at sequential addresses. A block diagram of timers B and C are shown in figure 15.

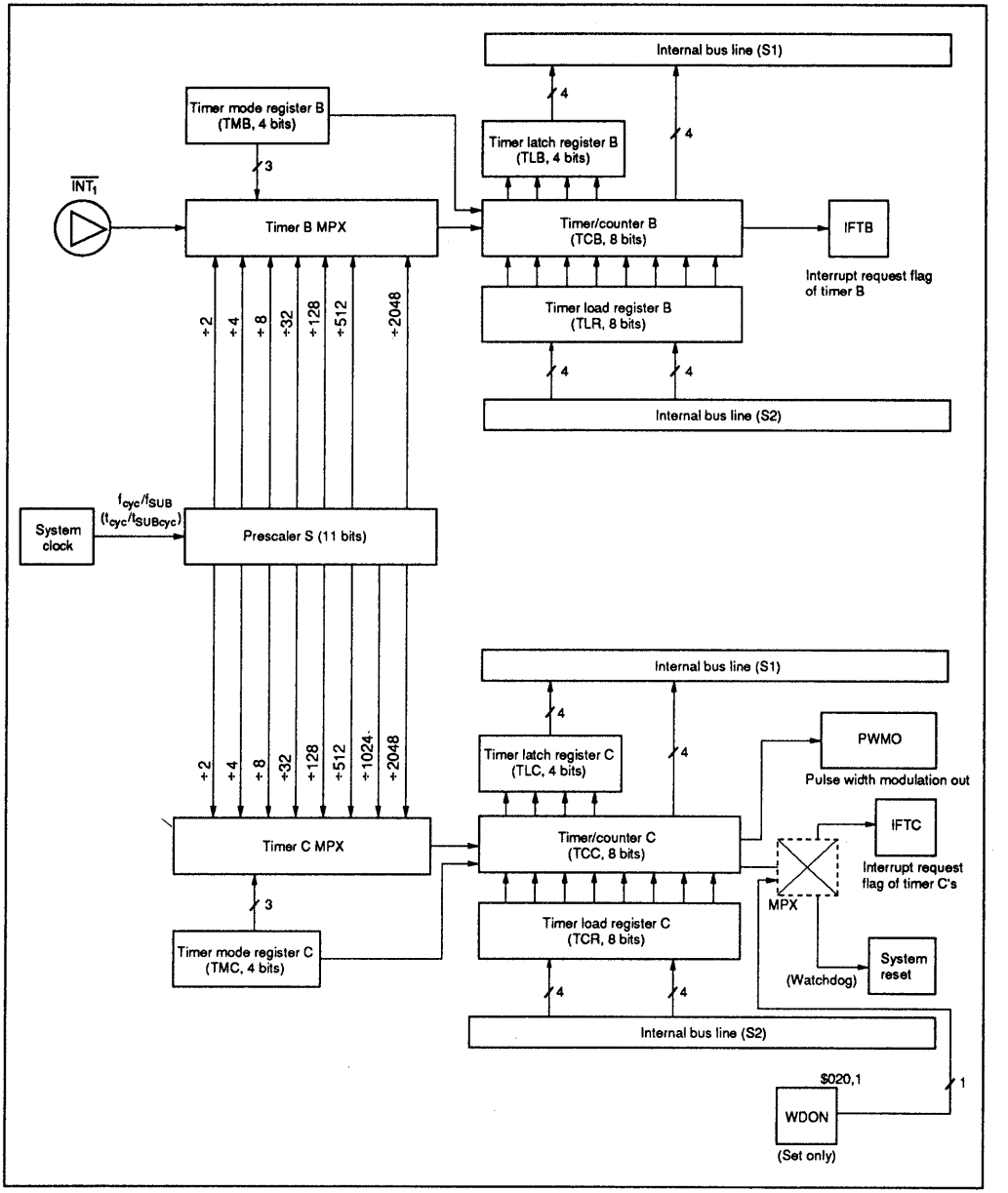


Figure 15 Block Diagram of Timers B and C

The timer/counter is initialized by writing to timer load register B (TLR). In this case, the lower digit must be written to first. The contents of TLR are loaded into the timer/counter at the same time the upper digit is written to, initializing the timer/counter. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading the timer/counter. In this case, the upper digit must be read first; the count is latched when the upper digit is read.

An auto-reload function, input clock source, and prescaler division ratio of timer B depend on the state of timer mode register B (TMB). When an external event input is used as the input clock source of TMB, the $R3_3/\overline{INT_1}$ pin must be set to $\overline{INT_1}$ by setting port mode register A (PMRA: $004).

Timer B is initialized to the value set in TMB by software, and is then incremented by one each clock input. If an input is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer B is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $002, 0).

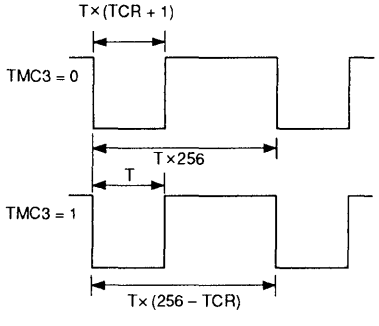
Timer C (TCCL and TCRL: $00E, TCCU and TCRU: $00F): Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer/counter (TCCL and TCCU) located at the same addresses. The eight-bit configuration consists of lower and upper 4-bit digits located at sequential addresses. The operation of timer C is basically the same as that of timer B.

The auto-reload function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in TMC by software, and is then incremented by one at each clock input. If an input is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer C is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $002, 2)

Timer C also functions as a watchdog timer. If a program routine runs out of control and an overflow is generated while the watchdog on (WDON) flag is set, the MCU is reset. This error can be detected by having the program control timer C reset before timer C reaches $FF.

The WDON can only have 1 written to it ; it is cleared to 0 only by MCU reset.

Timer Mode Register A (TMA: $008): Four-bit write-only register that controls timer A as shown in table 16.



T: Period of clock input to the counter (table 18)
TCR: Value of timer load register C (0 – 255)

Note: TMC3 is always fixed low when TCR = $FF.

Figure 16 Variable-Duty Pulse Output Waveform

Timer Mode Register B (TMB: $009): Four-bit write-only register that selects the auto-reload function, the prescaler division ratio, and input clock source as shown in table 17. Timer mode register B is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer B initialization set by writing to TMB must be done after a mode change becomes valid.

Timer Mode Register C (TMC: $00D): Four-bit write-only register that selects the auto-reload function and prescaler division ratio as shown in table 18. Timer mode register C is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer C initialization set by writing to TMC must be done after a mode change becomes valid.

Table 16 Timer Mode Register A

TMA				Source Prescaler, Input Clock Period,	
Bit 3	Bit 2	Bit 1	Bit 0	Operating Mode	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{SUBcyc}	Time-base mode
			1	PSW, 16 t_{SUBcyc}	
		1	0	PSW, 8 t_{SUBcyc}	
			1	PSW, 2 t_{SUBcyc}	
	1	0	0	PSW, 1/2 t_{SUBcyc}	
			1	Do not use	
		1	0	PSW, TCA reset	
			1		

Notes: 1. t_{SUBcyc} = 244.14 µs (when 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (s) = input clock period (s) × 256
3. If PSW or TCA reset is selected while the LCD is operating, LCD operation halts (power switch goes off).
   When LCD is connected for display, the PSW and TCA reset periods must be set in the program to the minimum.
4. In time base mode, the timer counter overflow output cycle must be greater than half of the interrupt frame period (T/2 = t_{RC}).
   If 1/2 t_{SUBcyc} is selected, t_{RC} must be 7.8125 ms ((MIS1, MIS0) = (0, 1), see figure 34).

Table 17 Timer Mode Register B

TMB	
Bit 3	Auto Reload Function
0	Disabled
1	Enabled

TMB			Prescaler Division Ratio,
Bit 2	Bit 1	Bit 0	Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (external event input)

Table 18 Timer Mode Register C

TMC	
Bit 3	Auto Reload Function
0	Disabled
1	Enabled

TMC			Prescaler Division Ratio,
Bit 2	Bit 1	Bit 0	Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

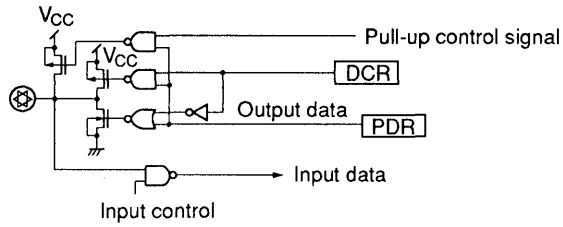
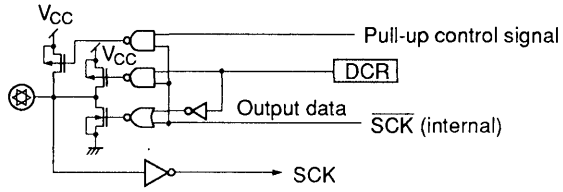
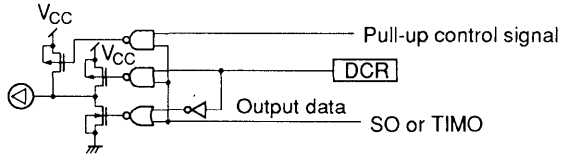
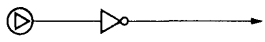
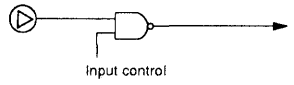
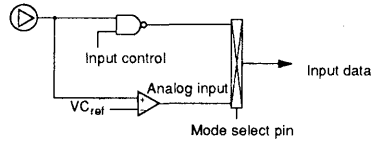
Input/Output

The MCU provides 26 input/output pins and 4 input pins, including 10 large-current pins (15 mA, max). A program-controlled pull-up MOS transistor is provided for each input/output pin.

The output buffer is turned on and off by the data control register (DCR) during input through an input/output pin.

I/O pin circuit types are shown in table 19.

Table 19 Circuit Configurations of I/O Pins

I/O Pin Type	Circuit	Applicable Pins
Common I/O pin (with pull-up MOS transistor)		$D_0 - D_9$ $R0_0 - R0_3$ $R1_0 - R1_3$ $R2_0 - R2_3$ $R3_0 - R3_3$
		$\overline{SCK}$
Output pin (with pull-up MOS transistor)		SO TIMO
Input pin		$\overline{INT_0}$ $\overline{INT_1}$ SI
		D_{10} D_{11}/VC_{ref}
		D_{12}/COMP0 D_{13}/COMP1 (multiplexed with analog inputs)

Note: Refer to table 20, note 3 concerning $R0_2$/SO.

D Ports (D_0 – D_{10}): Consist of ten 1-bit input/output pins and four input pins. Ports D_0 – D_9 are large-current I/O ports (15 mA, max). The sum current of the ports can go up to 100 mA. These ports are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions. Output data is stored in the port data register.

The on/off status of the output buffer is controlled by D port data control registers (DCRB, DCRC, and DCRD) that are mapped to memory address area. Pins D_{10} – D_{13} are input-only pins.

Two operating modes are available to pins D_{12} and D_{13}: digital input mode and analog input mode. The operating modes are set by bits 0 and 1 of port mode register B (PMRB). In the digital input mode, these pins can be used as input pins with the same input characteristics as the I/O pins. In the analog input mode, the result of a comparison with the reference voltage can be read as input data. The reference voltage is input by the D_{11}/VC_{ref} pin.

R Ports: Consist of sixteen 4-bit I/O ports. Data is input to these ports by LAR and LBR instructions and output from them by LRA and LRB instructions.

The on/off status of the output buffers of the R ports are controlled by R port data control registers (DCR0 – DCR3) that are mapped to memory addresses.

Pins $R0_0$, $R0_1$, and $R0_2$ are multiplexed with pins $\overline{SCK}$, SI, and SO, respectively.

Pins $R3_1$, $R3_2$, and $R3_3$ are multiplexed with TIMO, $\overline{INT_0}$, and $\overline{INT_1}$, respectively. Refer to figure 18.

Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin.

The on-off status of all these transistors is controlled by bit 3 of port mode register B (PMRB), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin. This enables on/off control of each individual pin. Refer to table 20.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up transistors or by resistors of about 100 kHz.

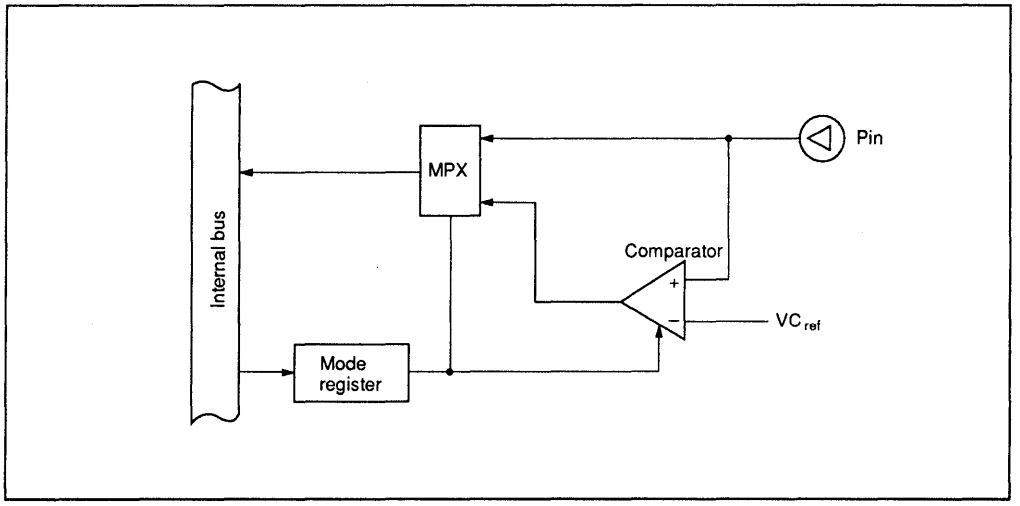


Figure 17 Configuration of D_{12} and D_{13}

Serial mode register: $005 (SMR)

3	2	1	0

$R0_0$ /$\overline{SCK}$ pin mode selection

SMR Bit 3	Port selection
0	$R0_0$
1	$\overline{SCK}$

Port mode register A: $004 (PMRA)

3	2	1	0

$R0_2$ /SO pin mode selection
$R0_1$ /SI pin mode selection
$R3_2$ /$\overline{INT_0}$ pin mode selection
$R3_3$ /$\overline{INT_1}$ pin mode selection

PMRA Bit 3	Port selection	PMRA Bit 2	Port selection	PMRA Bit 1	Port selection	PMRA Bit 0	Port selection
0	$R3_3$	0	$R3_1$	0	$R0_1$	0	$R0_2$
1	$\overline{INT_1}$	1	$\overline{INT_0}$	1	SI	1	SO

Port mode register B: $012 (PMRB)

3	2	1	0

D_{12} /COMP0 pin mode selection
D_{13} /COMP1 pin mode selection
$R3_1$ /TIMO pin mode selection
Pull-up MOS on/off selection

PMRB Bit 3	Pull-up MOS On/Off	PMRB Bit 2	Port selection	PMRB Bit 1	Port selection	PMRB Bit 0	Port selection
0	Off	0	$R3_1$	0	D_{13}	0	D_{12}
1	On	1	TIMO	1	COMP1	1	COMP0

Figure 18 I/O Switching Mode Registers

Table 20 Programmable I/O Circuits

PMRB Bit 3		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS	PMOS (A)	—	—	—	On	—	—	—	On
Buffer	NMOS (B)	—	—	On	—	—	—	On	—
Pull-up MOS Transistor		—	—	—	—	—	On	—	On

Notes: 1. —: Off

2. Various I/O methods can be selected by different combinations of settings of the above mode registers (PMRB3, DCR, PDR).
3. The PMOS (A) transistor of the $R1_2$/SO pin can be turned off by setting bit 2 of the miscellaneous register (MIS) to 1.

MIS	$R0_2$/SO Pin
Bit 2	PMOS (A)
0	On
1	Off

4. The relationships between DCRs and pins are as shown below.

DCR	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCRB	D3	D2	D1	D0
DCRC	D7	D6	D5	D4
DCRD	—	—	D9	D8

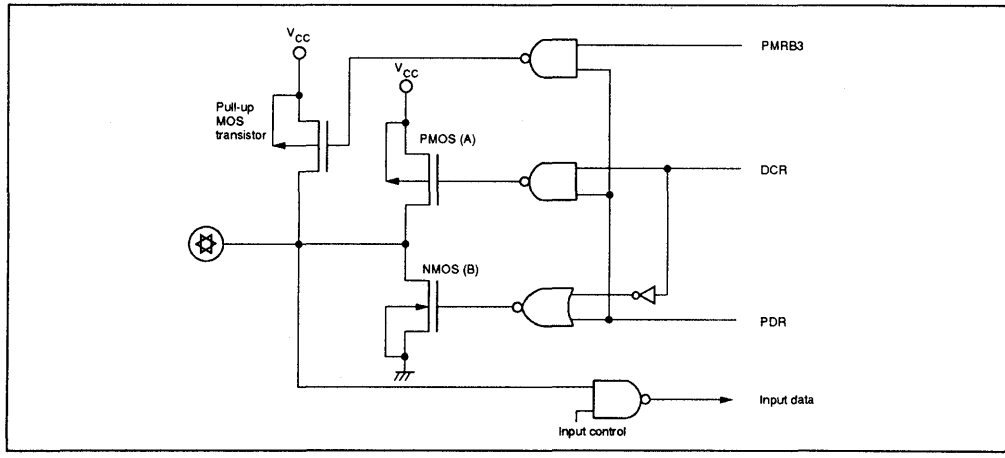


Figure 19 I/O Buffer Configuration

Reset

The MCU is reset by inputting a high-level voltage to the RESET pin. At power on and when stop mode is canceled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, RESET must be high for at least two instruction cycles.

Initial values after MCU reset are shown in table 21.

Table 21 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
V register (bank register)		(V)	0	Bank 0 (memory)
Interrupt flags/masks	Interrupt enable flag	(I/E)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt request
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
Timer/counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B	(TMB)	0000	Refer to description of timer mode register B
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S		$000	—
	Prescaler W		$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer load register B	(TLR)	$00	—
	Timer load register C	(TCR)	$00	—
	Octal counter		000	—

Table 21 Initial Values After MCU Reset (cont)

Item		Abbr.	Initial Value	Contents
LCD	LCD control register	(LCR)	000	Refer to description of LCD control register
	LCD mode register	(LMR)	0000	Refer to description of LCD duty cycle/clock control
DTMF generator	Tone generator control register	(TGC)	000	Refer to description of tone generator control register
	Tone generator mode register	(TGM)	0000	Refer to description of generator mode register
Bit register	Low speed on flag	(LSON)	0	Refer to description of low-power dissipation mode
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Tone generator speed flag	(TGSP)	0	Refer to description of DTMF generation circuit
	Direct transfer on flag	(DTON)	0	Refer to description of low-power dissipation mode
Miscellaneous register		(MIS)	000	—

Item	Abbr.	Status After Cancellation of Stop Mode by MCU Reset	Status After All Other Types of Reset
Carry	(CA)	Pre-MCU-reset values are	Pre-MCU-reset values are
Accumulator	(A)	not guaranteed; values must	not guaranteed; values must
B register	(B)	be initialized by program	be initialized by program
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SR)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retained	

Internal Oscillator Circuit

Figure 20 shows a block diagram of the internal oscillator circuit. A ceramic filter oscillator can be connected to OSC_1 and OSC_2 and a 32.768-kHz crystal oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock.

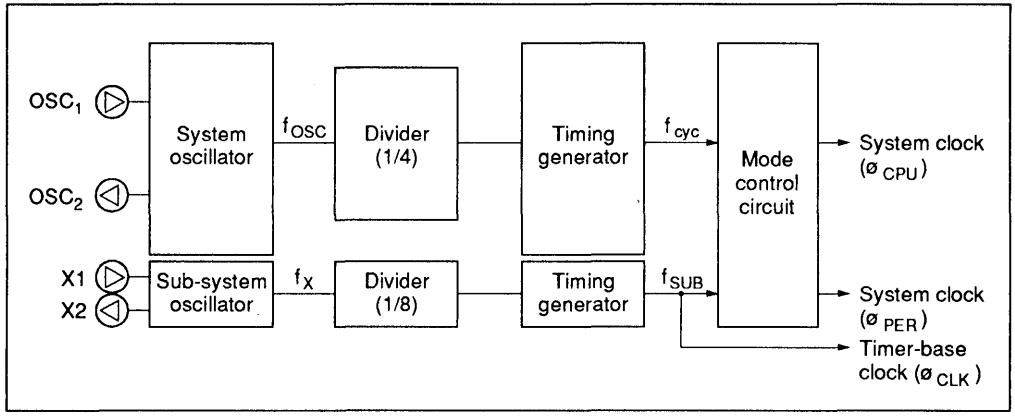


Figure 20 Internal Oscillator Circuit

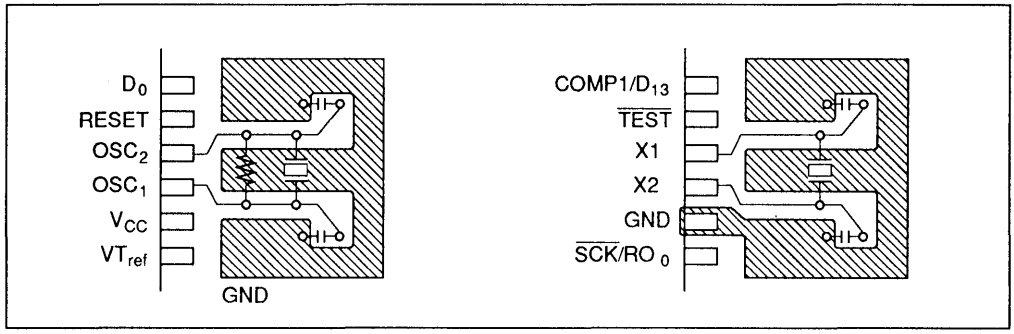
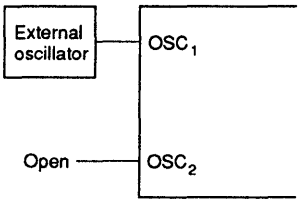
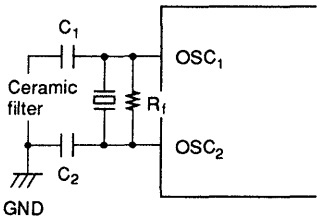
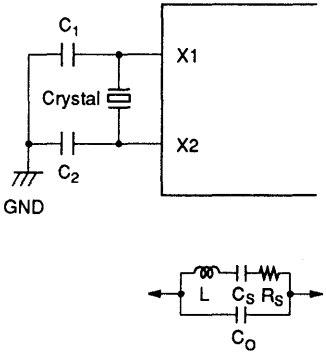


Figure 21 Layout of Crystal and Ceramic Filters

Table 22 Oscillator Circuit Examples

Circuit Configuration		Circuit Constants
External clock operation (OSC_1, OSC_2)		
Ceramic filter oscillator (OSC_1, OSC_2)		Ceramic filter: CSB400P22 (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5% Ceramic filter: CSB800J122 (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5%
Crystal oscillator		Crystal: 32.768 kHz: MX38T (Nippon Denpa Kogyo) R_s = 14 kΩ C_0 = 1.5 pF C_1 = 20 pF ± 20% C_2 = 20 pF ± 20%

Notes: 1. The circuit constants given above are recommended values provided by the oscillator manufacturer. Since they may be affected by stray capacitances from the oscillator or board, please consult the crystal or ceramic filter manufacturer to determine the actual circuit parameters required.

2. Wiring between the OSC_1/OSC_2 pins (X1, X2 pins) and other elements must be as short as possible, and must not cross other wiring. Refer to the recommended layout of the crystal and ceramic filter in figure 21.

3. If a 32.768-kHz crystal oscillator is not used, fix the X1 pin to V_{CC} and leave the X2 pin open.

Liquid Crystal Display (LCD)

The MCU has an LCD controller and driver which drive 4 common signal pins and 32 segment signal pins. The controller consists of a RAM area in which display data is stored, a display control register (LCR), and a duty/clock control register (LMR), as shown in figure 22.

Four duties and the LCD clock are program-controllable, and a built-in dual-port RAM ensures that display data can be automatically transmitted to the segment signal pins without program intervention. If a 32-kHz oscillation clock is selected as the LCD clock source, the LCD can be used even in watch mode, in which the system clock stops.

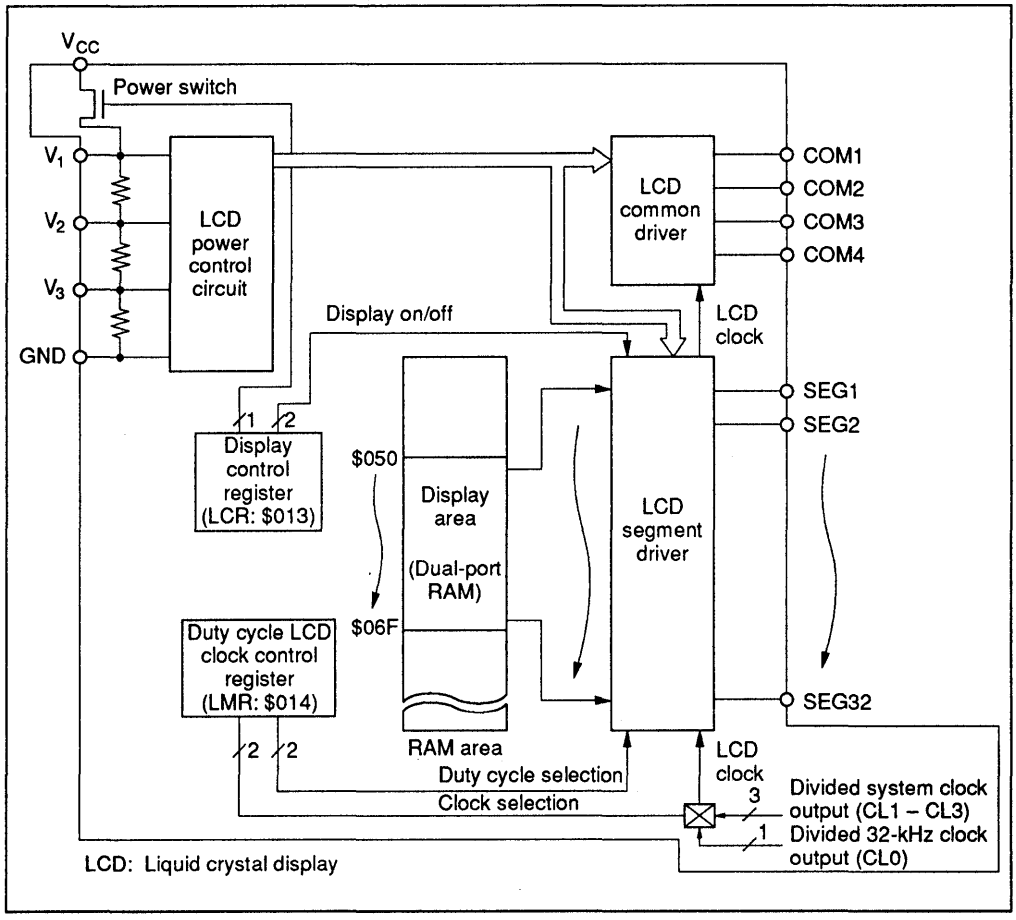


Figure 22 Block Diagram of Liquid Crystal Display

LCD Data Area and Segment Data ($050 – $06F): Figure 23 shows the configuration of LCD RAM area. Each bit of the storage area corresponds to one of four types of duties. If data is written to an area corresponding to a certain duty cycle, it is automatically output to the corresponding segments as display data.

LCD Control Register (LCR: $013): Three-bit write-only register which controls LCD blanking, the turning on and off of the LCD's power supply division resistor, and display in watch and subactive modes (see table 23).

Blank/display

Blank: Segment signals are turned off regardless of LCD RAM data setting.

Display: LCD RAM data is output as segment signals.

- Power switch on/off

  Off: The power switch is off.

  On: The power switch is on and V_1 is V_{CC}.

- Watch/subactive mode display

  Off: In watch and subactive modes, all common and segment pins are grounded and the liquid crystal power switch is turned off.

  On: In watch and subactive modes, LCD RAM data is output as segment signals.

LCD Duty/Clock Control Register (LMR: $014): Four-bit write-only register which selects the display duty and LCD clock source, as shown in table 24.

	Bit 3	Bit 2	Bit 1	Bit 0	
80	SEG1	SEG1	SEG1	SEG1	$050
81	SEG2	SEG2	SEG2	SEG2	$051
82	SEG3	SEG3	SEG3	SEG3	$052
83	SEG4	SEG4	SEG4	SEG4	$053
84	SEG5	SEG5	SEG5	SEG5	$054
85	SEG6	SEG6	SEG6	SEG6	$055
86	SEG7	SEG7	SEG7	SEG7	$056
87	SEG8	SEG8	SEG8	SEG8	$057
88	SEG9	SEG9	SEG9	SEG9	$058
89	SEG10	SEG10	SEG10	SEG10	$059
90	SEG11	SEG11	SEG11	SEG11	$05A
91	SEG12	SEG12	SEG12	SEG12	$05B
92	SEG13	SEG13	SEG13	SEG13	$05C
93	SEG14	SEG14	SEG14	SEG14	$05D
94	SEG15	SEG15	SEG15	SEG15	$05E
95	SEG16	SEG16	SEG16	SEG16	$05F
	COM 4	COM 3	COM 2	COM 1	

	Bit 3	Bit 2	Bit 1	Bit 0	
96	SEG17	SEG17	SEG17	SEG17	$060
97	SEG18	SEG18	SEG18	SEG18	$061
98	SEG19	SEG19	SEG19	SEG19	$062
99	SEG20	SEG20	SEG20	SEG20	$063
100	SEG21	SEG21	SEG21	SEG21	$064
101	SEG22	SEG22	SEG22	SEG22	$065
102	SEG23	SEG23	SEG23	SEG23	$066
103	SEG24	SEG24	SEG24	SEG24	$067
104	SEG25	SEG25	SEG25	SEG25	$068
105	SEG26	SEG26	SEG26	SEG26	$069
106	SEG27	SEG27	SEG27	SEG27	$06A
107	SEG28	SEG28	SEG28	SEG28	$06B
108	SEG29	SEG29	SEG29	SEG29	$06C
109	SEG30	SEG30	SEG30	SEG30	$06D
110	SEG31	SEG31	SEG31	SEG31	$06E
111	SEG32	SEG32	SEG32	SEG32	$06F
	COM 4	COM 3	COM 2	COM 1	

Figure 23 Configuration of LCD RAM Area

Table 23 LCD Control Register

LCR Bit 2	Display in Watch Mode or Subactive Mode	LCR Bit 1	Power Switch On/Off	LCR Bit 0	Blank/Display
0	Off	0	Off	0	Blank
1	On	1	On	1	Display

Note: When using an LCD in watch mode or subactive mode, use the divided output of a 32-kHz oscillator as the LCD clock and set bit 2 of the LCR to 1. If using the divided output of the system clock as the LCD clock, always set bit 2 of the LCR to 0.

Table 24 LCD Duty/Clock Control Register

LMR				
Bit 3	Bit 2	Bit 1	Bit 0	Duty Selection/Input Clock Selection
		0	0	1/4 duty cycle
		0	1	1/3 duty cycle
		1	0	1/2 duty cycle
		1	1	Static
0	0			CL0 (32.768/64 kHz when using 32.768-kHz oscillator)
0	1			CL1 (f_{cyc}/256)
1	0			CL2 (f_{cyc}/2048)
1	1			CL3 (refer to table 25)

Note: f_{cyc} is the divided system clock output.

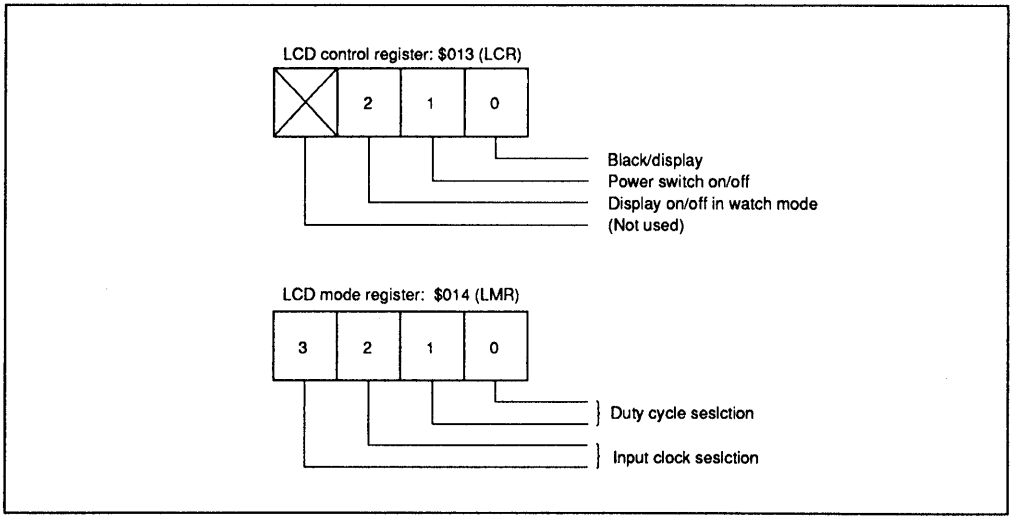


Figure 24 LCD Control Register

Table 25 LCD Frame Periods for Different Duties

Static Duty

Instruction cycle time	LMR Bit 3 / Bit 2 = 0 0 (CL0)	LMR Bit 3 / Bit 2 = 0 1 (CL1)	LMR Bit 3 / Bit 2 = 1 0 (CL2)	LMR Bit 3 / Bit 2 = 1 1 (CL3(Note))
10 µs	512 Hz	390.6 Hz	48.8 Hz	24.4 Hz/64 Hz
5 µs	512 Hz	781.2 Hz	97.6 Hz	48.8 Hz/64 Hz

1/2 Duty

Instruction cycle time	LMR Bit 3 / Bit 2 = 0 0 (CL0)	LMR Bit 3 / Bit 2 = 0 1 (CL1)	LMR Bit 3 / Bit 2 = 1 0 (CL2)	LMR Bit 3 / Bit 2 = 1 1 (CL3(Note))
10 µs	256 Hz	195.3 Hz	24.4 Hz	12.2 Hz/32 Hz
5 µs	256 Hz	390.6 Hz	48.8 Hz	24.4 Hz/32 Hz

1/3 Duty

Instruction cycle time	LMR Bit 3 / Bit 2 = 0 0 (CL0)	LMR Bit 3 / Bit 2 = 0 1 (CL1)	LMR Bit 3 / Bit 2 = 1 0 (CL2)	LMR Bit 3 / Bit 2 = 1 1 (CL3(Note))
10 µs	170.6 Hz	130.2 Hz	16.3 Hz	8.1 Hz/21.3 Hz
5 µs	170.6 Hz	260.4 Hz	32.6 Hz	16.2 Hz/21.3 Hz

1/4 Duty

Instruction cycle time	LMR Bit 3 / Bit 2 = 0 0 (CL0)	LMR Bit 3 / Bit 2 = 0 1 (CL1)	LMR Bit 3 / Bit 2 = 1 0 (CL2)	LMR Bit 3 / Bit 2 = 1 1 (CL3(Note))
10 µs	128 Hz	97.7 Hz	12.2 Hz	6.1 Hz/16 Hz
5 µs	128 Hz	195.4 Hz	24.4 Hz	12.2 Hz/16 Hz

Note: The division ratio depends on the value of bit 3 of timer mode register A (TMA3): The first value is for TMA3 = 0 and the second is for TMA3 = 1.
When TMA3 = 0, CL3 = f_{cyc}/4096.
When TMA3 = 1, CL3 = 32.768 kHz/512

Large Liquid-Crystal Panel Drive and V_{LCD}: To drive a large-capacity LCD, decrease the resistance of the built-in division resistors by attaching external resistors in parallel, as shown in figure 25.

The size of these resistors cannot be simply calculated from the LCD load capacitance because the matrix configuration of the LCD complicates the paths of charge/discharge currents flowing through the capacitors. The resistance will also vary with lighting conditions. This size must be determined by trial and error, taking into account the power dissipation of the device using the LCD, but a resistance of 1 to 10 kΩ would usually be suitable. (Another effective method is to attach capacitors of 0.1 to 0.3 µF.)

Always turn off the power switch (set bit 1 of the LCR to 0) before changing the liquid crystal drive voltage (V_{LCD}).

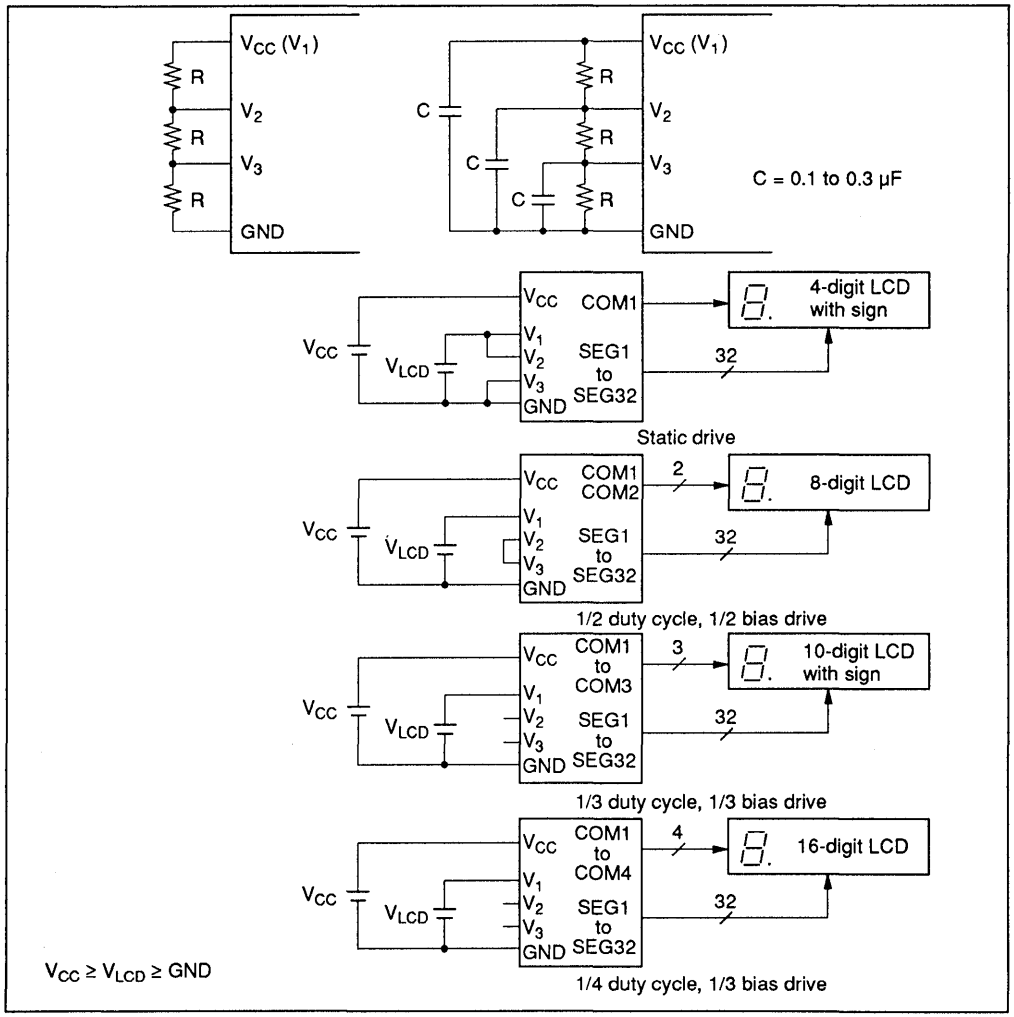


Figure 25 LCD Connection Examples

DTMF Generation Circuit

The MCU has a dual-tone multi-frequency (DTMF) generation circuit.

The DTMF signal consists of two sine waves to access the switching system.

Figure 26 shows the DTMF keypad and frequencies. Pressing a key generates a tone corresponding to its frequency. Figure 27 shows a block diagram of the DTMF circuit.

The MCU uses an oscillation frequency reduced to 400 kHz, an eighth of the conventionally used frequency, for low-power consumption. This, however, causes a potential frequency deviation. The MCU provides transformed programmable dividers in addition to sine wave counters and a control register to reduce frequency deviation.

The DTMF generation circuit is controlled by the following three registers.

Tone Generator Mode Register (TGM: $010): Four-bit write-only register which controls output frequencies (see table 26). It is cleared to $0 by MCU reset.

Tone Generator Control Register (TGC: $011): Three-bit write-only register which controls the start and stop of DTMF signal output (see table 27). It is cleared to $0 by MCU reset.

Tone Generator Speed Flag (TGSP: $020, 2): One-bit register which can be set and reset by the SEM/REM and SEMD/REMD instructions. The DTMF generation circuit generates output frequencies with a 400-kHz clock (table 26). With an 800-kHz clock the DTMF generation circuit generates these same frequencies by pulling the TGSP flag high.

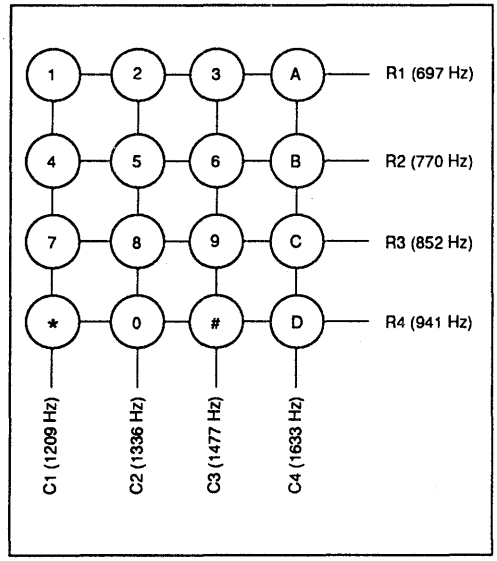


Figure 26 DTMF Keypad and Frequencies

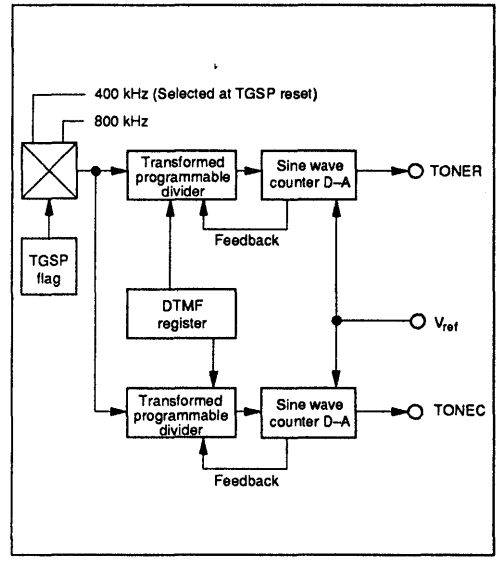


Figure 27 Block Diagram of DTMF Circuit

Table 26 Tone Generator Mode Register

TGM					
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Output Frequencies**	
Option (TONER output is not affected)		0	0	f_{R1} (697 Hz)	Output through TONER pin
		0	1	f_{R2} (770 Hz)	
		1	0	f_{R3} (852 Hz)	
		1	1	f_{R4} (941 Hz)	
0	0	Option (TONEC output is not affected)		f_{C1} (1,209 Hz)	Output through TONEC pin
0	1			f_{C2} (1,336 Hz)	
1	0			f_{C3} (1,477 Hz)	
1	1			f_{C4} (1,633 Hz)	

Table 27 Tone Generator Control Register

TGC Bit 1	DTMF Enable Bit
0	DTMF disabled
1	DTMF enabled

TGC Bit 2	TONER Output Control (Row)
0	Stopped
1	TONER output (active)

TGC Bit 3	TONEC Output Control (Column)
0	Stopped
1	TONEC output (active)

DTMF Output: The sine waves of the row-group and column-group are individually converted from digital to analog in the D/A conversion circuit, which provides high precision ladder resistance. The DTMF output pins, TONER and TONEC, transmit the sine waves of the row-group and column-group, respectively. Figure 28 shows the Tone output equivalent circuit. Figure 29 shows the output waveform. One cycle of this wave consists of 32 time slots, making the output waveform stable with little distortion. Table 28 lists the frequency deviation of the MCU from standard DTMF signals.

2

Table 28 Frequency Deviation of the MCU from Standard DTMF Signals

Standard	DTMF (Hz)	MCU (Hz)	Deviation from Standard (%)
R1	697	694.44	–0.37
R2	770	769.23	–0.10
R3	852	851.06	–0.11
R4	941	938.97	–0.22
C1	1,209	1,212.12	0.26
C2	1,336	1,333.33	–0.20
C3	1,477	1,481.48	0.30
C4	1,633	1,639.34	0.39

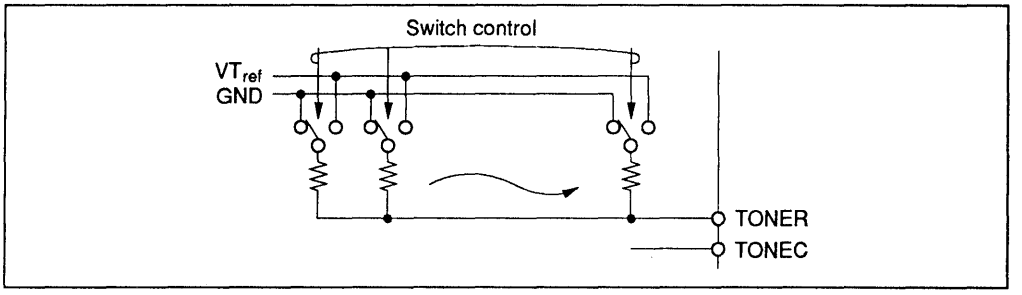


Figure 28 Tone Output Equivalent Circuit

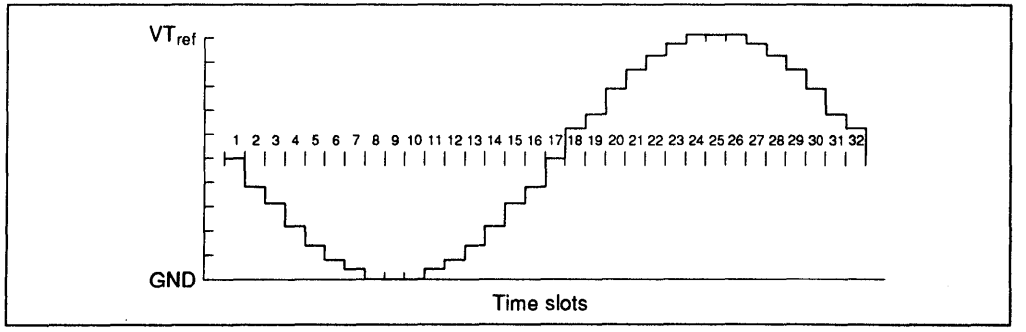


Figure 29 Waveform of Tone Output

Operating Modes

The MCU has five operating modes that are specified by how the clock is used. The functions available in each mode are listed in table 29, and operations are shown in table 31. Transitions between operating modes are shown in figure 30. Table 30 provides additional information for table 29.

Active Mode: The MCU operates according to the clock generated by the system oscillators OSC_1 and OSC_2.

Table 29 Functions Available in Each Operating Mode

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*4**
Activation method		RESET cancellation, interrupt request	SBY instruction	TMA3 = 0, STOP instruction	TMA3 = 1, STOP instruction	$\overline{INT_0}$ or timer A interrupt request from watch mode
Status	System oscillator	Operating	Operating	Stopped	Stopped	Stopped
	Subsystem oscillator	Operating	Operating	Operating*1	Operating	Operating
	Instruction execution (Φ_{CPU})	Operating	Stopped	Stopped	Stopped	Operating
	Interrupt function interrupt (Φ_{PER})	Operating	Operating	Stopped	Stopped	Operating
	Clock function interrupt (Φ_{CLK})	Operating	Operating	Stopped	Operating*2	Operating*2
	RAM	Operating	Retained	Retained	Retained	Operating
	Registers/flags	Operating	Retained	Reset	Retained	Operating
	I/O	Operating	Retained	High impedance*3	Retained*3	Operating*3
Cancellation method		RESET input, STOP/SBY instruction	RESET input, interrupt request	RESET input	RESET input, $\overline{INT_0}$ or timer A interrupt request	RESET input, STOP/SBY instruction

Notes: 1. To reduce current dissipation, stop all oscillation in external circuits.
2. Refer to the Interrupt frame section for details.
3. Refer to table 30.
4. Subactive mode is an optional function specified it on the function option list.
5. In the watch and subactive modes, the MCU requires a 32.768-kHz crystal oscillator.

	System Clock (Φ_{CPU})		
		Operating	**Stopped**
Non-timebase peripheral function clock (Φ_{PER})	Operating	Active mode	Standby mode
		Subactive mode	
	Stopped	—	Watch mode (TMA3 = 1)
			Watch mode (TMA3 = 0)

Standby Mode: The MCU enters standby mode when a SBY instruction is executed from active mode. In this mode, the oscillators, interrupts, timer/counters, and serial interface continue to operate, but all instruction execution-related clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and resumes, executing the next instruction after the SBY instruction. If the interrupt enable flag is 1, that interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 31.

Stop Mode: The MCU enters stop mode if a STOP instruction is executed in active mode when TMA3 = 0. In this mode, the system oscillator stops, which stops all MCU functions as well.

Stop mode is terminated by a RESET input as shown in figure 32. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is canceled, all RAM contents are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

Watch Mode: The MCU enters watch mode if a STOP instruction is executed in active mode when TMA3 = 1, or if a STOP or SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input or a timer A/$\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer A/$\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0, or subactive mode if LSON is 1. Any interrupt request generated during the transition to active mode is delayed for half the interrupt frame period (t_{RC}), to give the oscillation time to stabilize, as shown in figure 33.

Table 30 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby Mode, Watch Mode	Stop Mode	Active Mode, Subactive Mode
$D_0 - D_9$	Retained	High impedance	Input enabled
$D_{10} - D_{13}$			Input enabled
R0 – R3	Retained	High impedance	Input enabled

Table 31 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode	Standby Mode	Subactive Mode*3
CPU	Reset	Retained	Retained	
RAM	Retained	Retained	Retained	
Timer A	Reset			
Timer B	Reset	Stopped		
Timer C	Reset	Stopped		
Serial interface	Reset	Stopped*4		
LCD	Reset			
DTMF	Reset	Reset	Stopped	Reset
I/O	Reset*1	Retained	Retained	

Notes: 1. Output pins are at high impedance.
2. Shading means operating.
3. Subactive mode is an optional function specified on the function option list.
4. Transmission/reception is activated if a clock is input in external clock mode. (However, interrupts stop.)

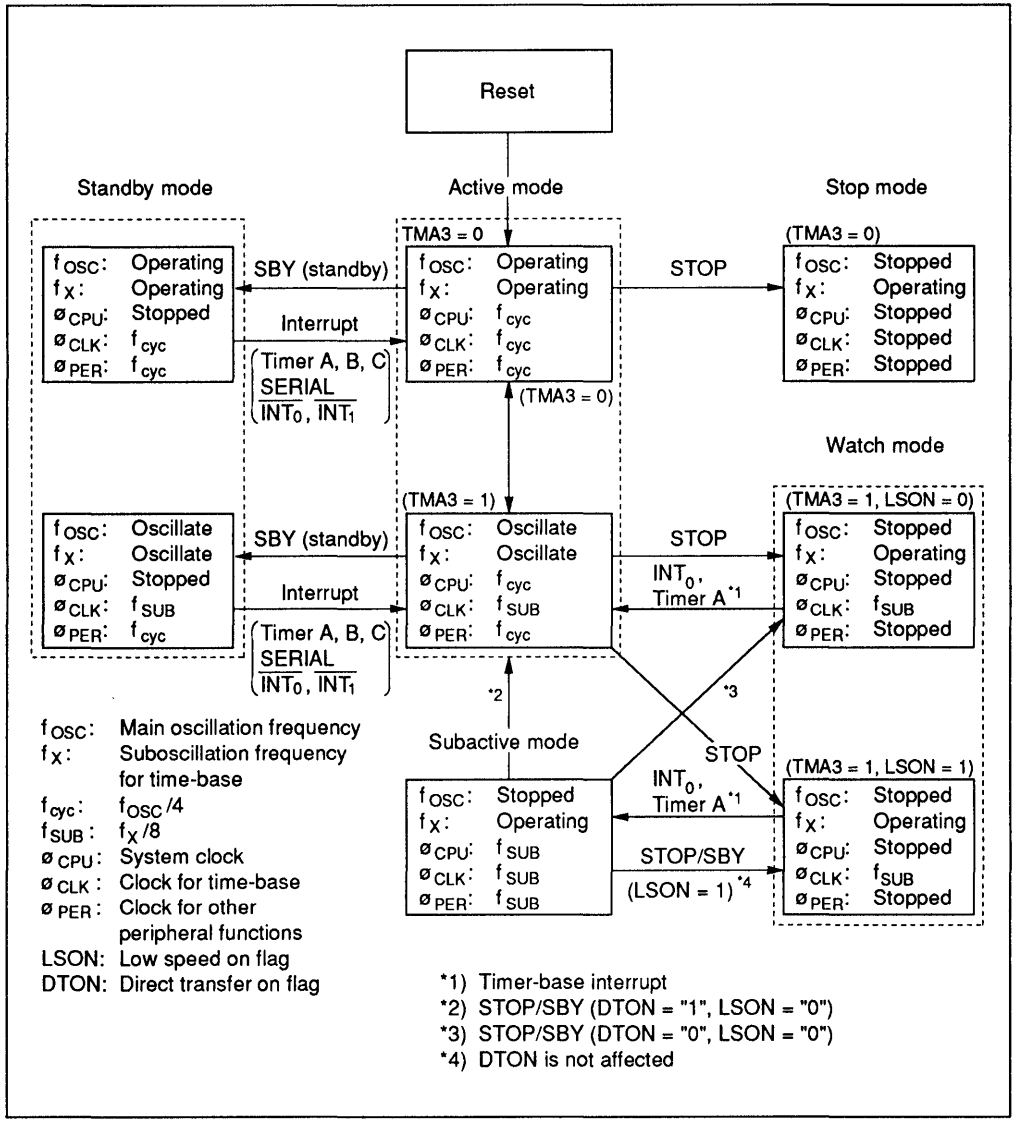


Figure 30 MCU Status Transitions

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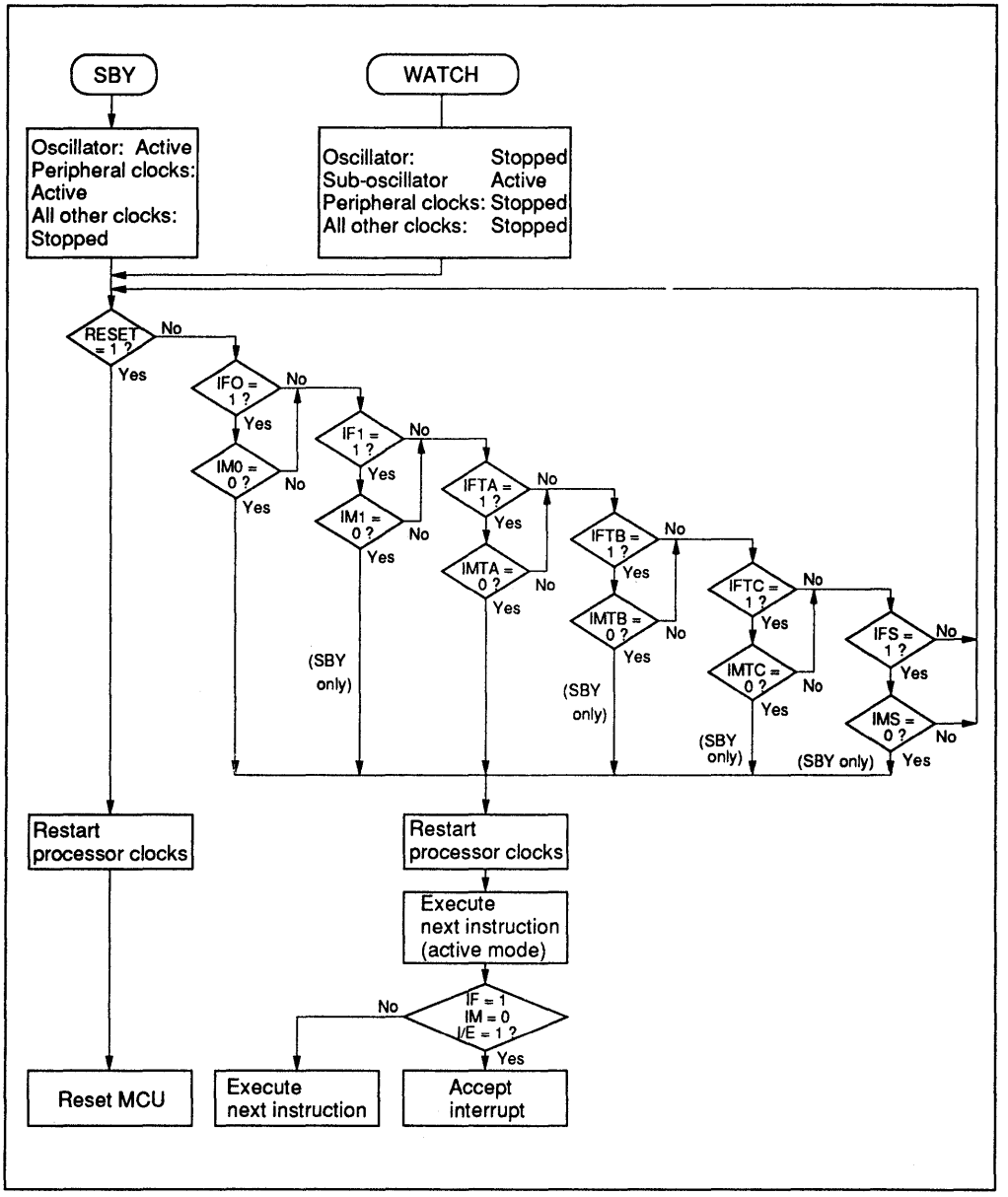


Figure 31 MCU Operation Flowchart

Operation during mode transition is the same as that at standby mode cancellation (figure 31).

Subactive Mode: The CPU operates with a clock generated by the X1 and X2 oscillation circuits. Functions that can operate in subactive mode are listed in table 31. When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of LSON and DTON. The DTON flag can only be set in subactive mode; it is automatically reset after a transition to active mode.

Subactive mode is an optional function that the user must specify on the function option list.

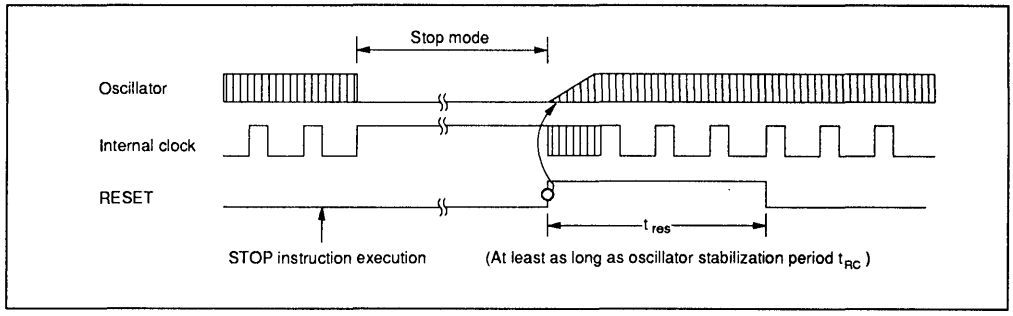


Figure 32 Timing of Stop Mode Cancellation

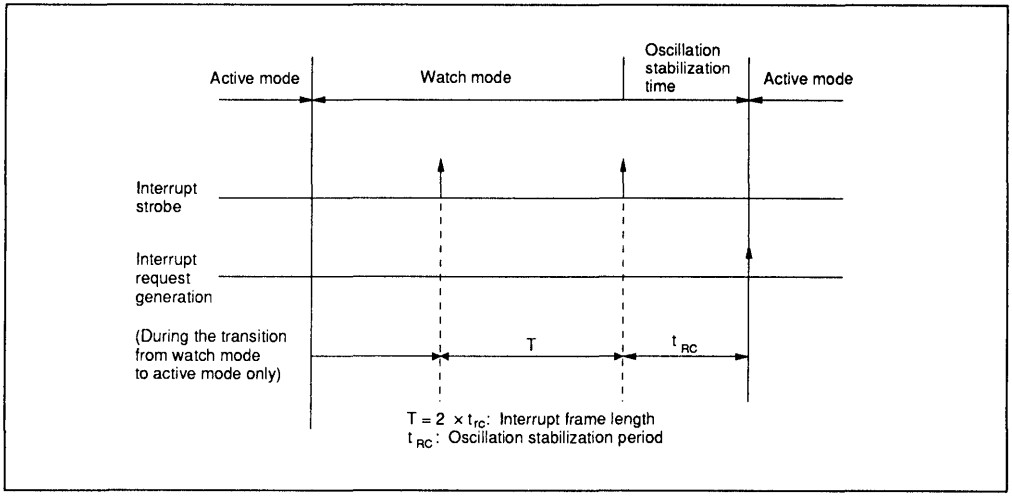
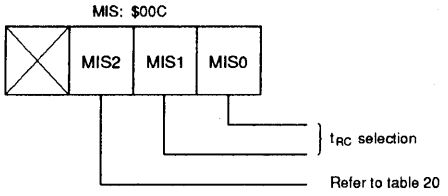


Figure 33 Interrupt Frame

Interrupt Frame: In watch and subactive modes, Φ_{CLK} is supplied for timer A and the $\overline{INT_0}$ circuit. Prescaler W and timer A operate as time bases to generate interrupt frame timing. Three interrupt frame cycles (T) can be selected by the settings of the miscellaneous register, as shown in figure 34.

In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. An interrupt request is generated at the interrupt strobe timing, except when the MCU enters active mode from watch mode. The $\overline{INT_0}$ falling edge is acknowledged regardless of the interrupt frame, but the interrupt is executed simultaneously with the next interrupt strobe. Timer A generates an overflow and interrupt request at the timing of an interrupt strobe.



MIS		T Note1	t_{RC} Note1	Oscillation circuit condition
1 Bit	0 Bit			
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms Note2	
0	1	15.625 ms	7.8125 ms	400/800-kHz ceramic filter
1	0	62.5 ms	31.25 ms	
1	1	Not used		—

Notes: 1. The value of t_{RC} applies only when using a 32.768-kHz oscillator.
2. Only direct transfer.

Figure 34 Miscellaneous Register

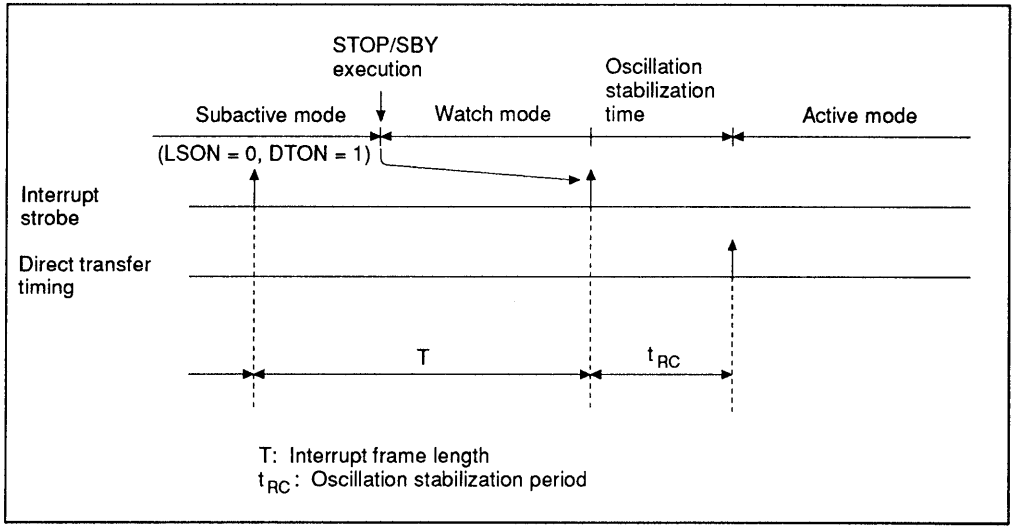


Figure 35 Direct Transfer Timing

Direct Transfer: A special flag, DTON (direct transfer on flag) has been newly added to enable a direct transfer from subactive to active mode. The detailed procedure is as follows:

- Set the DTON flag in subactive mode while LSON = 0.
- Execute the STOP or SBY instruction.
- After the oscillation stabilization time (a fixed value), the MCU will move automatically from subactive to active mode.

Note that DTON ($020, bit 3) is valid only in subactive mode. When the MCU is in active mode, this flag is always at reset.

The transition time (t_D) from subactive to active mode is $t_{rc} < t_D < T + t_{RC}$.

MCU Operating Sequence: The MCU operates in the sequence shown in figures 36 to 38. It is reset by an asynchronous RESET input, regardless of its state.

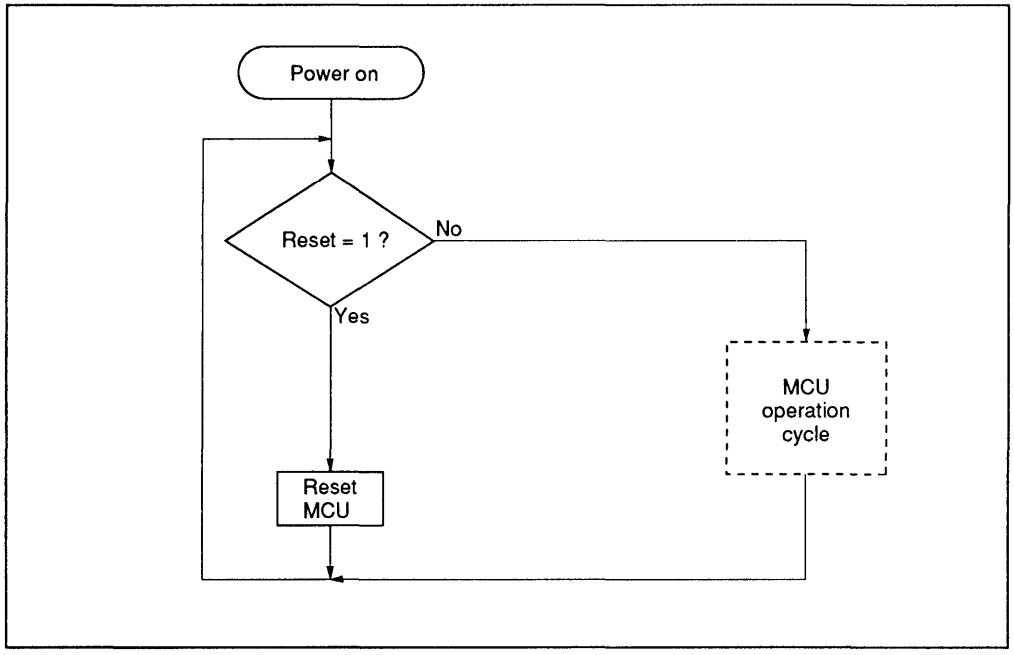


Figure 36 MCU Operating Sequence (power on)

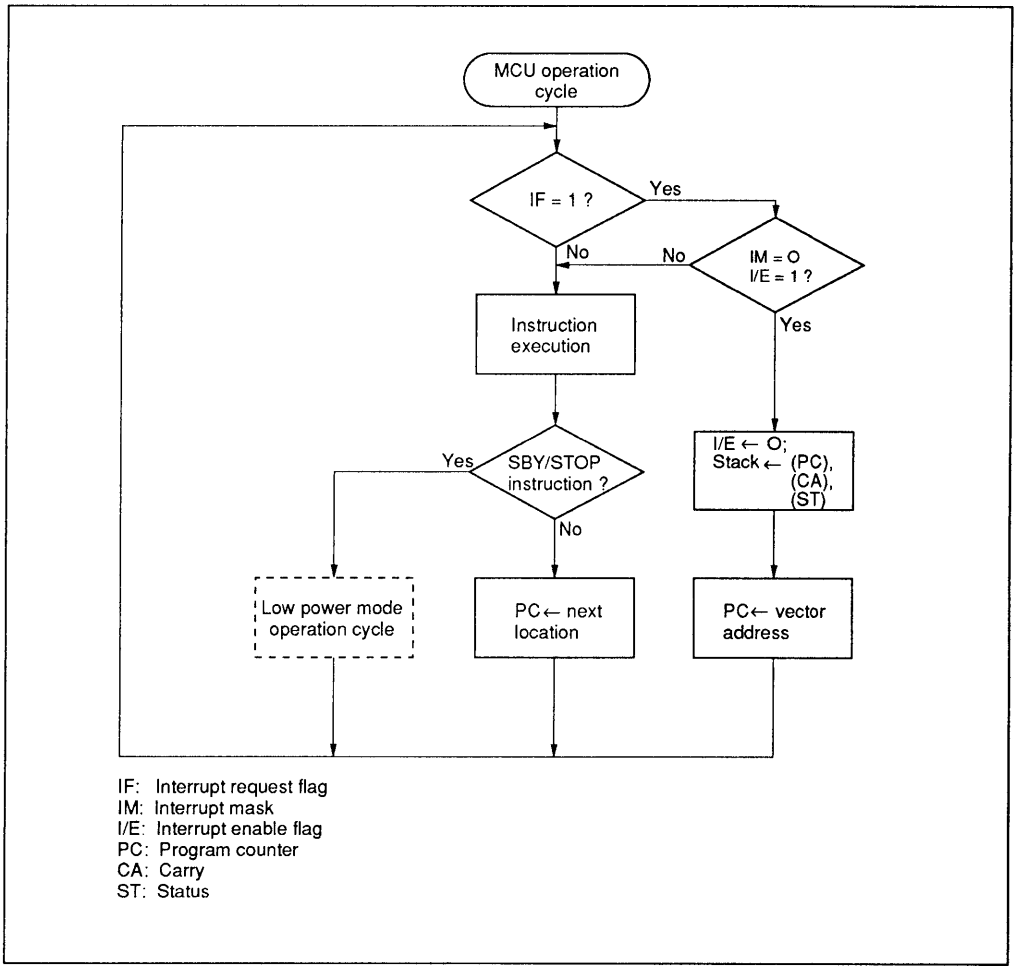


Figure 37 MCU Operating Sequence (MCU operation cycle)

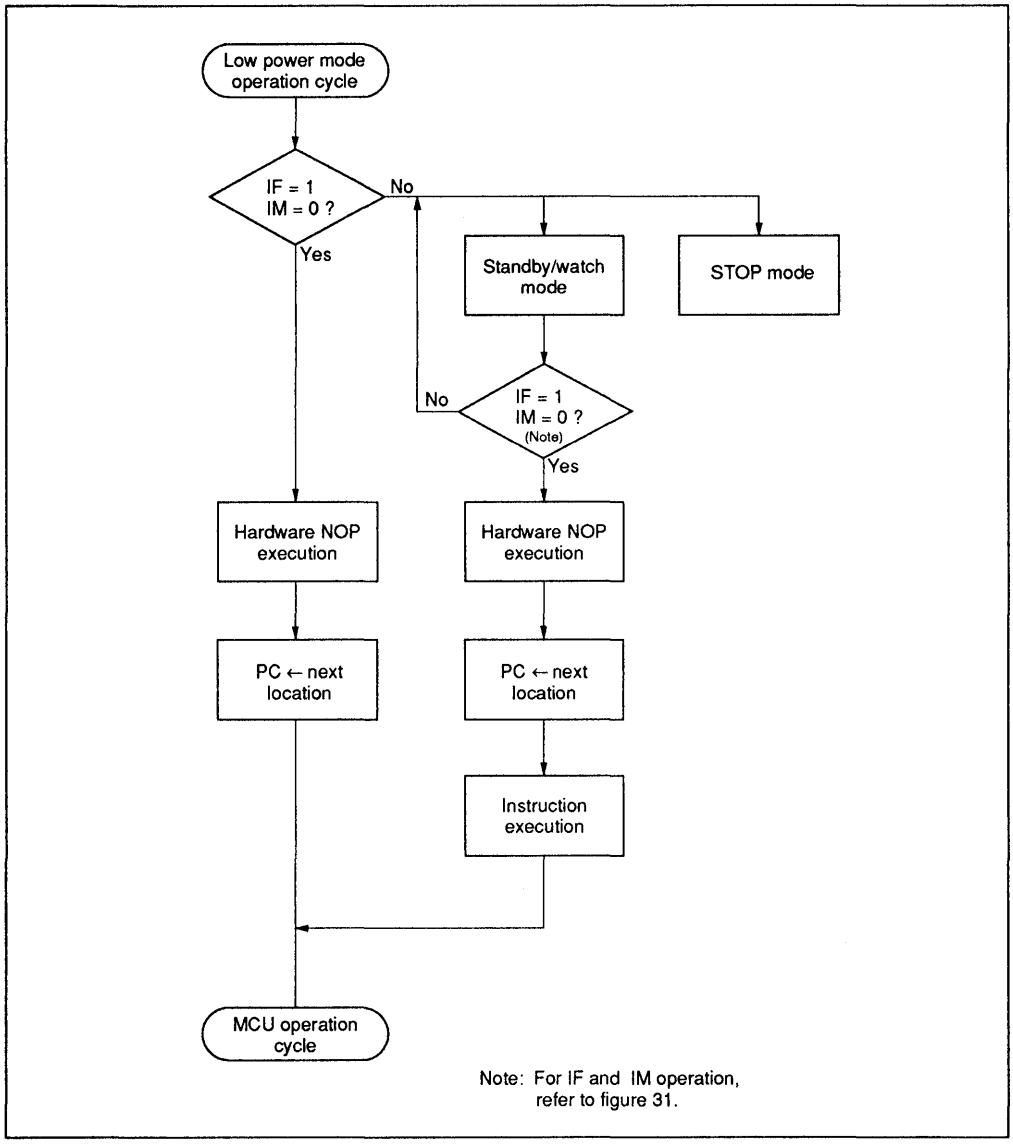


Figure 38 MCU Operating Sequence (low power mode operation)

Programmable ROM

The HD4074618 is a ZTAT™ microcomputer with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
1	79	D_2	I/O	O_2	I/O	41	39	SEG9	O		
2	80	D_3	I/O	O_3	I/O	42	40	SEG10	O		
3	1	D_4	I/O	O_4	I/O	43	41	SEG11	O		
4	2	D_5	I/O	O_5	I/O	44	42	SEG12	O		
5	3	D_6	I/O	O_6	I/O	45	43	SEG13	O		
6	4	D_7	I/O	O_7	I/O	46	44	SEG14	O		
7	5	D_8	I/O			47	45	SEG15	O		
8	6	D_9	I/O			48	46	SEG16	O		
9	7	D_{10}	I	V_{PP}		49	47	SEG17	O		
10	8	D_{11}/VC_{ref}	I	A_9	I	50	48	SEG18	O		
11	9	D_{12}/COMP0	I	$\overline{M0}$	I	51	49	SEG19	O		
12	10	D_{13}/COMP1	I	$\overline{M1}$	I	52	50	SEG20	O		
13	11	$\overline{TEST}$	I	$\overline{TEST}$	I	53	51	SEG21	O		
14	12	X1	I	GND		54	52	SEG22	O		
15	13	X2	O			55	53	SEG23	O		
16	14	GND		GND		56	54	SEG24	O		
17	15	$R0_0/\overline{SCK}$	I/O	A_1	I	57	55	SEG25	O		
18	16	$R0_1$/SI	I/O	A_2	I	58	56	SEG26	O		
19	17	$R0_2$/SO	I/O	A_3	I	59	57	SEG27	O		
20	18	$R0_3$	I/O	A_4	I	60	58	SEG28	O		
21	19	$R1_0$	I/O	A_5	I	61	59	SEG29	O		
22	20	$R1_1$	I/O	A_6	I	62	60	SEG30	O		
23	21	$R1_2$	I/O	A_7	I	63	61	SEG31	O		
24	22	$R1_3$	I/O	A_8	I	64	62	SEG32	O		
25	23	$R2_0$	I/O	A_0	I	65	63	COM1	O		
26	24	$R2_1$	I/O	A_{10}	I	66	64	COM2	O		
27	25	$R2_2$	I/O	A_{11}	I	67	65	COM3	O		
28	26	$R2_3$	I/O	A_{12}	I	68	66	COM4	O		
29	27	$R3_0$	I/O	A_{13}	I	69	67	V_1			
30	28	$R3_1$/TIMO	I/O	A_{14}	I	70	68	V_2			
31	29	$R3_2/\overline{INT_0}$	I/O	$\overline{CE}$	I	71	69	V_3		V_{CC}	
32	30	$R3_3/\overline{INT_1}$	I/O	$\overline{OE}$	I	72	70	TONEC	O		
33	31	SEG1	O			73	71	TONER	O		
34	32	SEG2	O			74	72	VT_{ref}		V_{CC}	
35	33	SEG3	O			75	73	V_{CC}		V_{CC}	
36	34	SEG4	O			76	74	OSC_1	I	V_{CC}	
37	35	SEG5	O			77	75	OSC_2	O		
38	36	SEG6	O			78	76	RESET	I	RESET	I
39	37	SEG7	O			79	77	D_0	I/O	O_0	I/O
40	38	SEG8	O			80	78	D_1	I/O	O_1	I/O

PROM Mode Pin Functions

Vpp: Applies the programming voltage (12.5 V ± 0.3 V) to the built-in PROM.

$\overline{CE}$: Inputs a control signal to enable PROM programming and verification.

$\overline{OE}$: Inputs a data output control signal for verification.

$A_0 - A_{14}$: Act as address input pins of the built-in PROM.

$O_0 - O_7$: Act as data bus I/O pins of the built-in PROM.

$\overline{M_0}$, $\overline{M_1}$: Used to set PROM mode. The MCU is set to the PROM mode by pulling $\overline{M_0}$, $\overline{M_1}$, and $\overline{TEST}$ low, and RESET high.

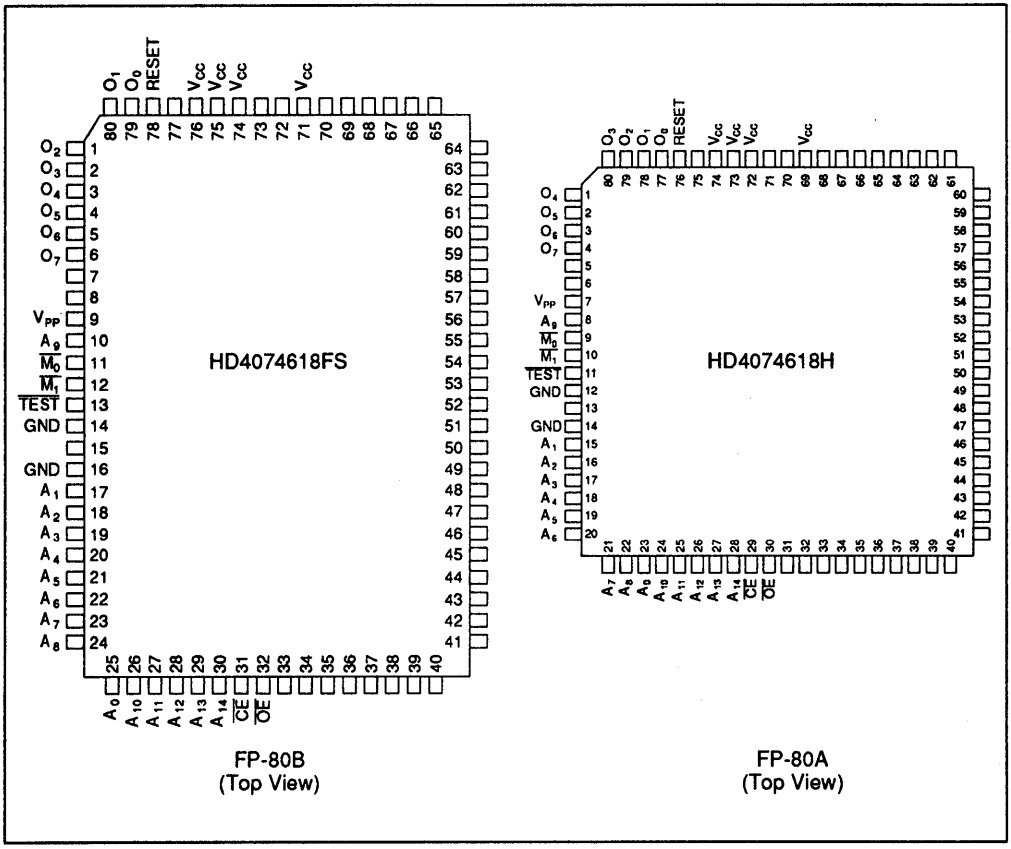


Figure 39 Pin Arrangement in PROM Mode

Programming the Built-in PROM

The MCU's built-in PROM is programmed in PROM mode which is set by pulling TEST, $\overline{M_0}$, and $\overline{M_1}$ low, and RESET high as shown in figure 40. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256 EPROM using a standard PROM programmer and a 80-to-28-pin socket adaptor. Recommended PROM programmers and socket adapters are listed in table 33.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower 5 bits and an upper 5 bits that are read from or written to consecutive addresses, as shown in figure 41. This means that if, for example, 8 Kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 16-Kbyte address space ($0000-$3FFF) must be specified.

Programming and Verification: The built-in PROM of the MCU can be programmed at high speed programming sequence without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 32, the memory map in PROM mode is shown in figure 41, the programming flowchart is shown in figure 42, and a timing chart of PROM programming and verification is shown in figure 43.

For details of PROM programming, refer to the notes on PROM Programming section.

Warnings

1. Always specify addresses $0000 to $3FFF when programming with a PROM programmer. If address $4000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed, but the ceramic window-package version can be reprogrammed after being exposed to ultraviolet light.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed in the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Table 32 PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0–O_7
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibition	High	High	V_{PP}	High impedance

Table 33 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Manufacturer**	**Model Name**	**Package**
DATA I/O Corp.	121B	Hitachi	HS460ESF01H	FP-80B
	29B		HS460ESH03H	FP-80A
AVAL Corp.	PKW-1000	Hitachi	HS460ESF01H	FP-80B
			HS460ESH03H	FP-80A

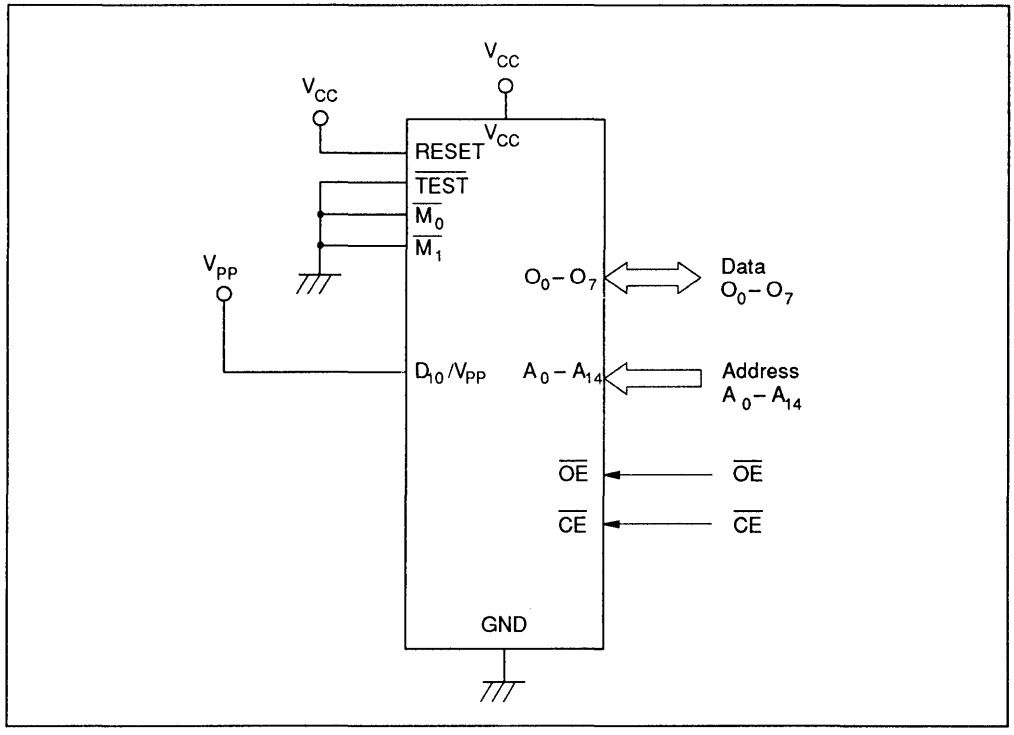


Figure 40 Connections in PROM Mode

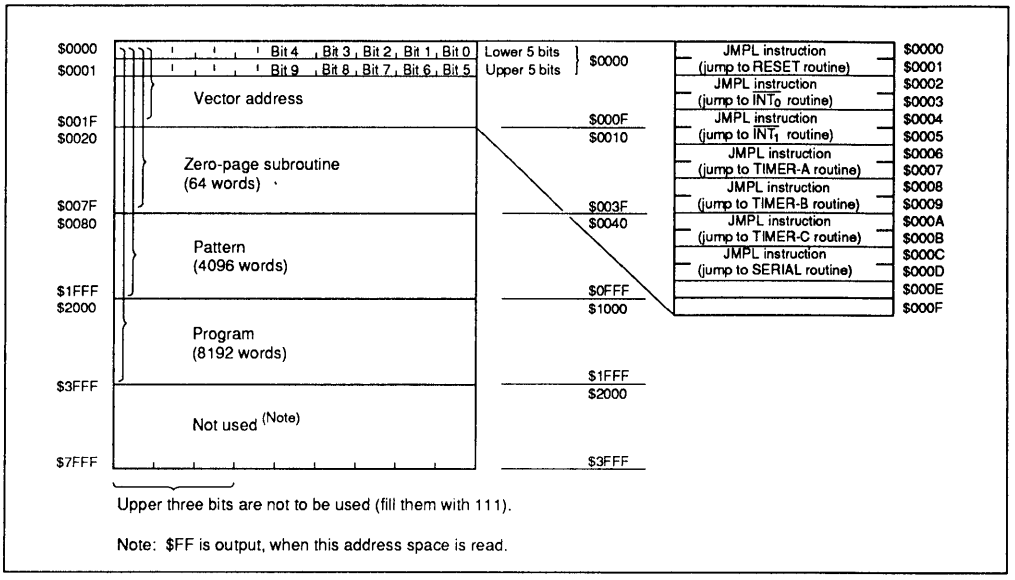


Figure 41 Memory Map in PROM Mode

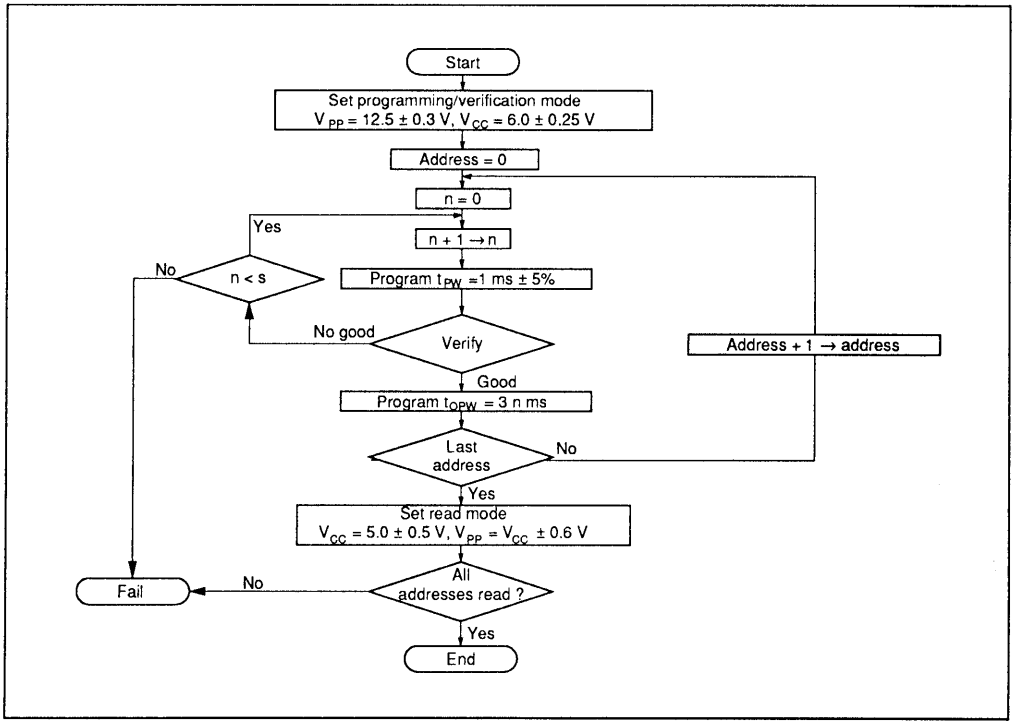


Figure 42 Flowchart of High-Speed Programming

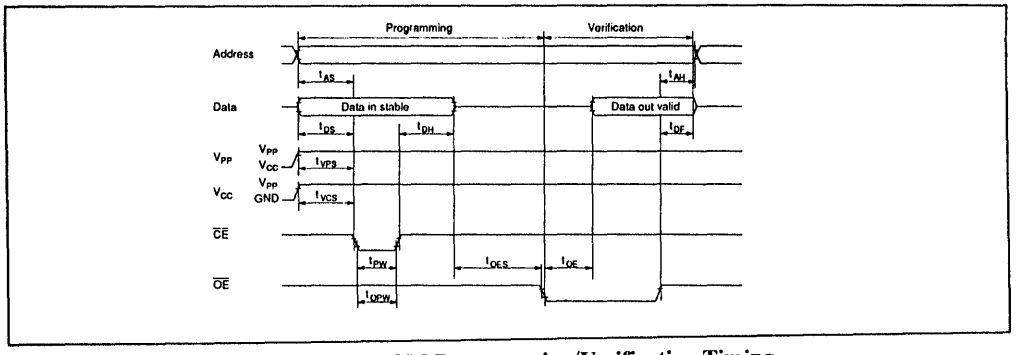


Figure 43 PROM Programming/Verification Timing

Programming and Verifying Electrical Characteristics

DC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, GND = 0.0 V, T_a = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	2.2	—	V_{CC} +0.3	V	
Input low voltage	V_{IL}	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	–0.3	—	0.8	V	
Output high voltage	V_{OH}	O_0–O_7	2.4	—	—	V	I_{OH} = –200 µA
Output low voltage	V_{OL}	O_0–O_7	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\|I_{LI}\|$	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	—	—	2	µA	V_{in} = 5.25 V/0.5 V
V_{CC} current	I_{CC}		—	—	30	mA	
V_{PP} current	I_{PP}		—	—	40	mA	

AC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, GND = 0.0 V, T_a = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	Refer to figure 42(Note)
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Output disable delay time	t_{DF}	—	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width during overprogramming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	500	ns	

Note: Input pulse level: 0.8 V to 2.2 V
Input rise/fall time: ≤ 20 ns
Input timing reference levels: 1.0 V, 2.0 V
Output timing reference levels: 0.8 V, 2.0 V

Notes on PROM Programming

Principles of Programming/Erasure: A memory cell in a ZTAT™ microcomputer is the same as an EPROM cell: it is programmed by applying a high voltage between its control gate and drain to inject hot electrons into its floating gate. These electrons are stable, surrounded by an energy barrier formed by an SiO_2 film. The change in threshold voltage of a memory cell with a charged floating gate makes the corresponding bit appear as 0; a cell whose floating gate is not charged appears as a 1 bit (figure 44).

The charge in a memory cell may decrease with time. This decrease is usually due to one of the following causes:

- Ultraviolet light excites electrons, allowing them to escape. This effect is the basis of the erasure principle.
- Heat excites trapped electrons, allowing them to escape.
- High voltages between control gate and drain may erase electrons.

If the oxide film covering a floating gate is defective, the electron erasure rate will be greater. However, electron erasure does not often occur because defective devices are detected and removed at the testing stage.

PROM Programming: EPROM memory cells must be programmed under specific voltage and timing conditions. The higher the programming voltage V_{PP} and the longer the programming pulse t_{pw} is applied, the more electrons are injected into the floating gates. However, if V_{PP} exceeds specifications, the p-n junctions may be permanently damaged. Pay particular attention to overshooting in the PROM programmer. In addition, note that negative voltage noise will produce a parasitic transistor effect that may reduce breakdown voltages.

The ZTAT™ microcomputer is electrically connected to the PROM programmer by a socket adapter. Therefore, note the following points:

- Check that the socket adapter is firmly mounted on the PROM programmer.
- Do not touch the socket adapter or the LSI during the programming. Touching them may affect the quality of the contacts, which will cause programming errors.

PROM Reliability After Programming: In general, semiconductor devices retain their reliability, provided that some initial defects can be excluded. These initial defects can be detected and rejected by screening. Baking devices under high-temperature conditions is one method of screening that can rapidly eliminate data-hold defects in memory cells. (Refer to the Principles of Programmings Erasure section.)

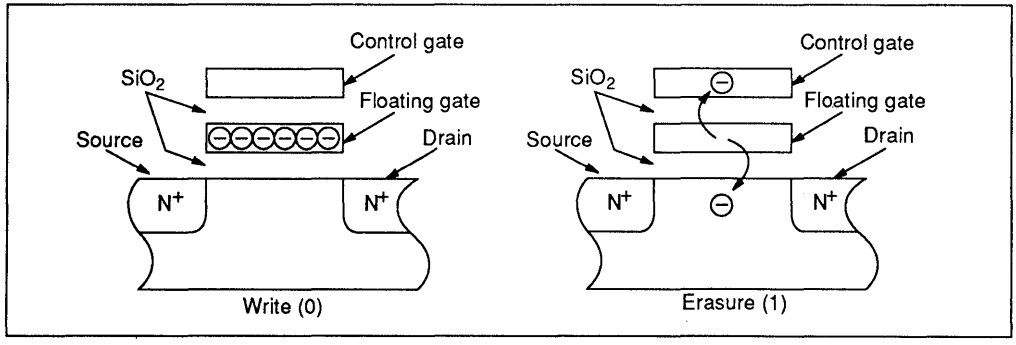


Figure 44 Cross-Sections through EPROM Cell

ZTAT™ microcomputer devices are extremely reliable because they have been subjected to such a screening method during the wafer fabrication process, but Hitachi recommends that each device is exposed to 150°C at one atmosphere for at least 48 hours after it is programmed, to ensure its best performance. The recommended screening process is shown in figure 45.

Note: If programming errors occur continuously during PROM programming, suspend programming and check for problems in the PROM programmer or socket adapter if using the window-package-type of EPROM. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi.

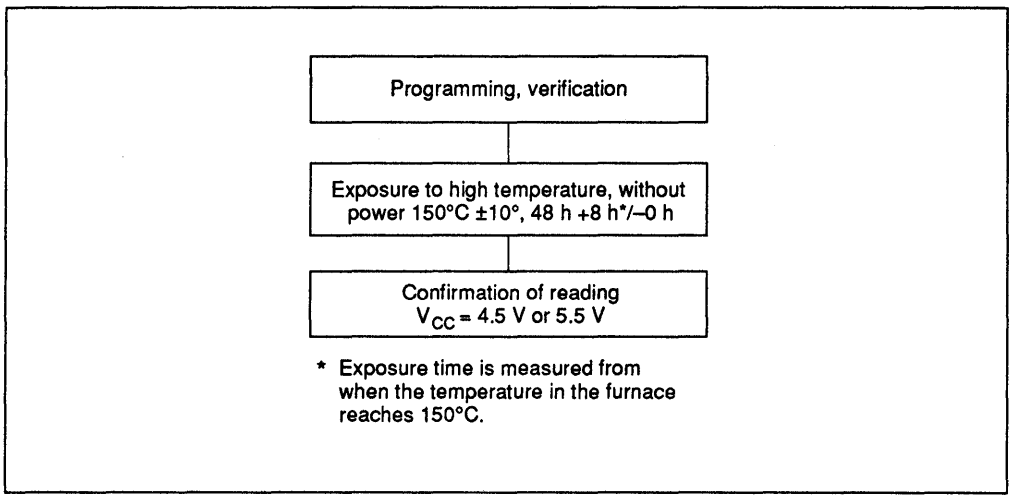


Figure 45 Recommended Screening Procedure

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 46 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory register (MR), which consists of 16 addresses from $040 to $04F, is accessed with the LAMR and XMRA instructions.

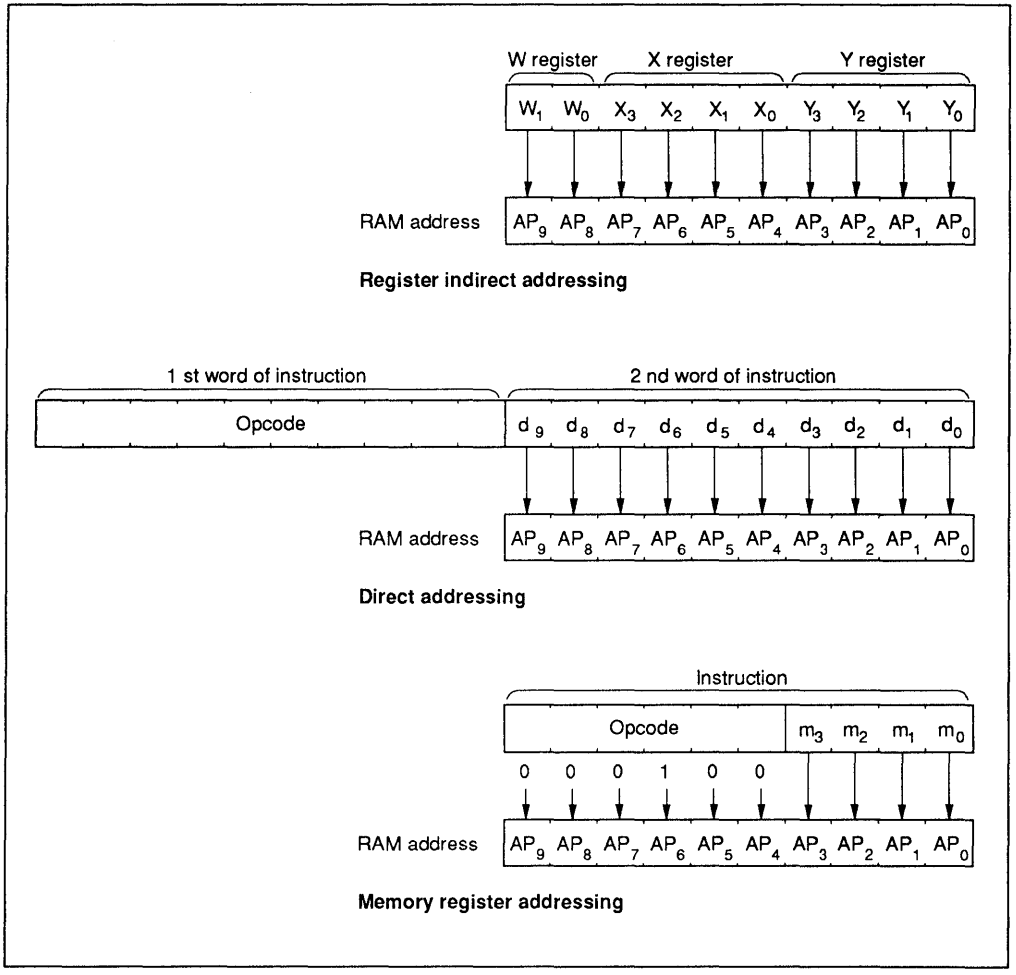


Figure 46 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 47 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 32 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 48. This means that the execution of a BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macro assembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 49. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output register. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

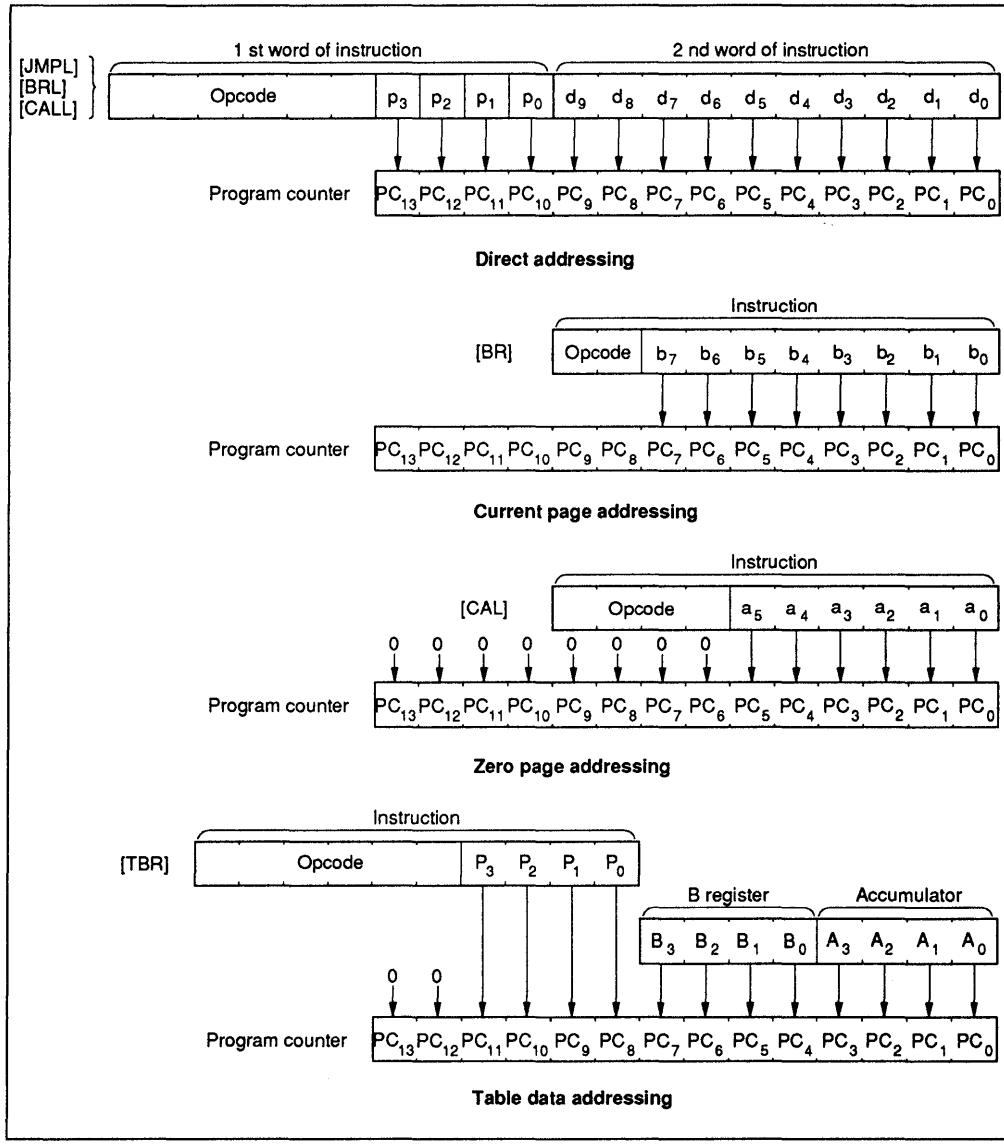


Figure 47 ROM Addressing Modes

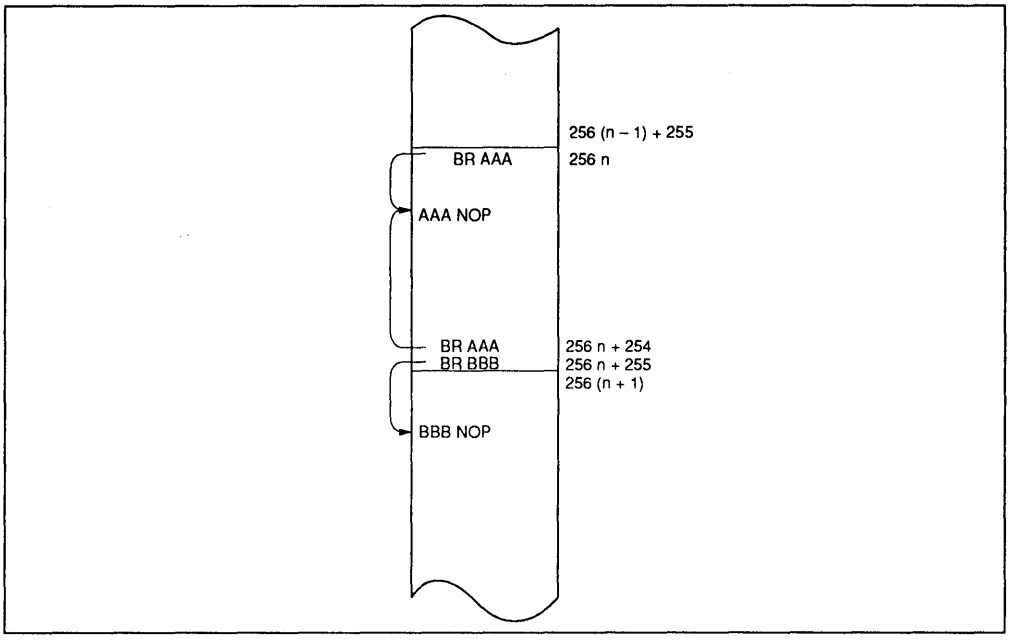


Figure 48 Branching when Branch Destination is on Page Boundary

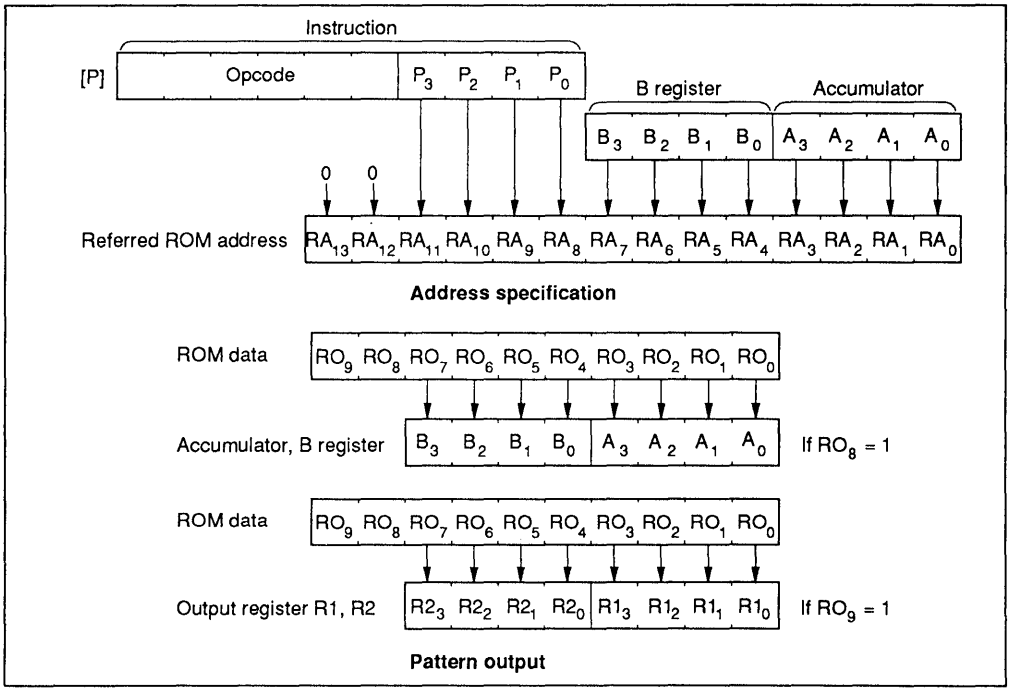


Figure 49 P Instruction

Instruction Set

The HD404618 and HD4074618 each have 101 instructions, classified into 10 groups as follows:

- Immediate instructions
- Register-to-register instructions
- RAM address instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM address instructions
- Input/output instructions
- Control instructions

The functions of these instructions are listed in tables 38 to 47, and an opcode map is shown in table 48.

Table 34 Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i → A		1/1
Load B from immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i → B		1/1
Load memory from immediate	LMID i, d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i → M		2/2
Load memory from immediate, increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i → M, Y + 1 → Y	NZ	1/1

Table 35 Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2(Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m) → A		1/1

Note: The assembler automatically provides an operand for the second word of the LAW instruction.

Table 36 RAM Address Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load W from immediate	LWI i	0	0	1	1	1	1	0	0	i_1	i_0	i → W		1/1
Load X from immediate	LXI i	1	0	0	0	1	0	i_3	i_2	i_1	i_0	i → X		1/1
Load Y from immediate	LYI i	1	0	0	0	0	1	i_3	i_2	i_1	i_0	i → Y		1/1
Load W from A	LWA	0	1	0	0	0	1	0	0	0	0	A → W		2/2(Note)
		0	0	0	0	0	0	0	0	0	0			
Load X from A	LXA	0	0	1	1	1	0	1	0	0	0	A → X		1/1
Load Y from A	LYA	0	0	1	1	0	1	1	0	0	0	A → Y		1/1
Increment Y	IY	0	0	0	1	0	1	1	1	0	0	Y + 1 → Y	NZ	1/1
Decrement Y	DY	0	0	1	1	0	1	1	1	1	1	Y − 1 → Y	NB	1/1
Add A to Y	AYY	0	0	0	1	0	1	0	1	0	0	Y + A → Y	OVF	1/1
Subtract A from Y	SYY	0	0	1	1	0	1	0	1	0	0	Y − A → Y	NB	1/1
Exchange X and SPX	XSPX	0	0	0	0	0	0	0	0	0	1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0	0	0	0	0	0	0	0	1	0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0	0	0	0	0	0	0	0	1	1	X ↔ SPX, Y ↔ SPY		1/1

Note: The assembler automatically provides an operand for the second word of the LWA instruction.

Table 37 RAM Register Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load A from memory	LAM (XY)	0	0	1	0	0	1	0	0	y	x	M → A, (X ′ SPX, Y ↔ SPY)		1/1
Load A from memory	LAMD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	0 d_1	0 d_0	M → A		2/2
Load B from memory	LBM (XY)	0	0	0	1	0	0	0	0	y	x	M → B, (X ↔ SPX, Y ↔ SPY)		1/1
Load memory from A	LMA (XY)	0	0	1	0	0	1	0	1	y	x	A → M, (X ↔ SPX, Y ↔ SPY)		1/1
Load memory from A	LMAD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	0 d_3	1 d_2	0 d_1	0 d_0	A → M		2/2
Load memory from A, increment Y	LMAIY (X)	0	0	0	1	0	1	0	0	0	x	A → M, Y + 1 → Y (X ↔ SPX)	NZ	1/1
Load memory from A decrement Y	LMADY(X)	0	0	1	1	0	1	0	0	0	x	A → M, Y − 1 → Y (X ↔ SPX)	NB	1/1
Exchange memory and A	XMA(XY)	0	0	1	0	0	0	0	0	y	x	M ↔ A, (X ↔ SPX, Y ↔ SPY)		1/1
Exchange memory and A	XMA(Dd)	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	0 d_1	0 d_0	M ↔ A		2/2
Exchange memory and B	XMB(XY)	0	0	1	1	0	0	0	0	y	x	M ↔ B, (X ↔ SPX, Y ↔ SPX)		1/1

Note: The meanings of (XY) and (X) are as follows:

Each instruction marked with (XY) has 4 mnemonics, each with different object codes.
For example, different values of X and Y of the opcode of the LAM (XY) instruction are given below.

Mnemonic	Y	X	Function
LAM	0	0	None
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

Each instruction marked with (X) has 2 mnemonics, each with different object codes. For example, different values of X of the opcode of the LMAIY(X) instruction are given below.

Mnemonic	X	Function
LAMIY	0	None
LAMIYX	1	X ↔ SPX

Table 38 Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	$A + i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B + 1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B - 1 \rightarrow B$	NB	1/1
Decimal adjust for addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal adjust for subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A} + 1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B} \rightarrow B$		1/1
Rotate right A with carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate left A with carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to memory	AM	0 0 0 0 0 0 1 0 0 0	$M + A \rightarrow A$	OVF	1/1
Add A to memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$M + A \rightarrow A$	OVF	2/2
Add A to memory with carry	AMC	0 0 0 0 0 1 1 0 0 0	$M + A + CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to memory with carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$M + A + \overline{CA} \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from memory with carry	SMC	0 0 1 0 0 1 1 0 0 0	$M - A - \overline{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from memory with carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$M - A - \overline{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \cap M \rightarrow A$	NZ	2/2
OR memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \cup M \rightarrow A$	NZ	2/2
EOR memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \oplus M \rightarrow A$	NZ	2/2

Note: $\cap$: Logical AND
$\cup$: Logical OR
$\oplus$: Exclusive OR

Table 39 Compare Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Immediate not equal to memory	INEM i	0	0	0	0	1	0	i_3	i_2	i_1	i_0	$i \neq M$	NZ	1/1
Immediate not equal to memory	INEMD i, d	0 d_9	1 d_8	0 d_7	0 d_6	1 d_5	0 d_4	i_3 d_3	i_2 d_2	i_1 d_1	i_0 d_0	$i \neq M$	NZ	2/2
A not equal to memory	ANEM	0	0	0	0	0	0	0	1	0	0	$A \neq M$	NZ	1/1
A not equal to memory	AMEMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	1 d_2	0 d_1	0 d_0	$A \neq M$	NZ	2/2
B not equal to memory	BNEM	0	0	0	1	0	0	0	1	0	0	$B \neq M$	NZ	1/1
Y not equal to immediate	YNEI i	0	0	0	1	1	1	i_3	i_2	i_1	i_0	$Y \neq i$	NZ	1/1
Immediate less or equal to memory	ILEM i	0	0	0	0	1	1	i_3	i_2	i_1	i_0	$i \leq M$	NB	1/1
Immediate less or equal to memory	ILEMD i, d	0 d_9	1 d_8	0 d_7	0 d_6	1 d_5	1 d_4	i_3 d_3	i_2 d_2	i_1 d_1	i_0 d_0	$i \leq M$	NB	2/2
A less or equal to memory	ALEM	0	0	0	0	0	1	0	1	0	0	$A \leq M$	NB	1/1
A less or equal to memory	ALEMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	1 d_2	0 d_1	0 d_0	$A \leq M$	NB	2/2
B less or equal to memory	BLEM	0	0	1	1	0	0	0	1	0	0	$B \leq M$	NB	1/1
A less or equal to immediate	ALEI i	1	0	1	0	1	1	i_3	i_2	i_1	i_0	$A \leq i$	NB	1/1

Table 40 RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Set memory bit	SEM n	0	0	1	0	0	0	0	1	n_1	n_0	$1 \rightarrow M(n)$		1/1
Set memory bit	SEMD n, d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	0 d_4	0 d_3	1 d_2	n_1 d_1	n_0 d_0	$1 \rightarrow M(n)$		2/2
Reset memory bit	REM n	0	0	1	0	0	0	1	0	n_1	n_0	$0 \rightarrow M(n)$		1/1
Reset memory bit	REMD n, d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	n_1 d_1	n_0 d_0	$0 \rightarrow M(n)$		2/2
Test memory bit	TM n	0	0	1	0	0	0	1	1	n_1	n_0		M(n)	1/1
Test memory bit	TMD n, d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	1 d_2	n_1 d_1	n_0 d_0		M(n)	2/2

Table 41 ROM Address Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Branch on status 1	BR b	1	1	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0		1	1/1
Long branch on status 1	BRL u	0	1	0	1	1	1	p_3	p_2	p_1	p_0		1	2/2
		d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
Long jump unconditionally	JMPL u	0	1	0	1	0	1	p_3	p_2	p_1	p_0			2/2
		d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
Subroutine jump on status 1	CAL a	0	1	1	1	a_5	a_4	a_3	a_2	a_1	a_0		1	1/2
Long subroutine jump on status 1	CALL u	0	1	0	1	1	0	p_3	p_2	p_1	p_0		1	2/2
		d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
Table branch	TBR p	0	0	1	0	1	1	p_3	p_2	p_1	p_0			1/1
Return from subroutine	RTN	0	0	0	0	0	1	0	0	0	0			1/3
Return from interrupt	RTNI	0	0	0	0	0	1	0	0	0	1	1 → I/E, carry restored	ST	1/3

Table 42 Input/Output Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Set discrete I/O latch	SED	0	0	1	1	1	0	0	1	0	0	1 → D(Y)		1/1
Set discrete I/O latch direct	SEDD m	1	0	1	1	1	0	m_3	m_2	m_1	m_0	1 → D(m)		1/1
Reset discrete I/O latch	RED	0	0	0	1	1	0	0	1	0	0	0 → D(Y)		1/1
Reset discrete I/O latch direct	REDD m	1	0	0	1	1	0	m_3	m_2	m_1	m_0	0 → D(m)		1/1
Test discrete I/O latch	TD	0	0	1	1	1	0	0	0	0	0		D(Y)	1/1
Test discrete I/O latch direct	TDD m	1	0	1	0	1	0	m_3	m_2	m_1	m_0		D(m)	1/1
Load A from R-port register	LAR m	1	0	0	1	0	1	m_3	m_2	m_1	m_0	R(m) → A		1/1
Load B from R-port register	LBR m	1	0	0	1	0	0	m_3	m_2	m_1	m_0	R(m) → B		1/1
Load R-port register from A	LRA m	1	0	1	1	0	1	m_3	m_2	m_1	m_0	A → R(m)		1/1
Load R-port register from B	LRB m	1	0	1	1	0	0	m_3	m_2	m_1	m_0	B → R(m)		1/1
Pattern generation	P p	0	1	1	0	1	1	p_3	p_2	p_1	p_0			1/2

Table 43 Control Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
No operation	NOP	0	0	0	0	0	0	0	0	0	0			1/1
Start serial	STS	0	1	0	1	0	0	1	0	0	0			1/1
Standby mode/watch mode(Note)	SBY	0	1	0	1	0	0	1	1	0	0			1/1
Stop mode/watch mode	STOP	0	1	0	1	0	0	1	1	0	1			1/1

Note: Only when shifted from sub-active mode.

Table 44 Opcode Map

R9 H \ R8 L	0																1													
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSPX	XSPY	XSP XY	AN EM				AM			ORM				LAW				ANE MD				AMD				OR MD			
	1	RTN	RT NI			AL EM				AMC			EO RM				LWA				ALE MD				AM CD				EOR MD			
	2	INEM i(4)															INEMD i(4)															
	3	ILEM i(4)															ILEMD i(4)															
	4	LBM(XY)				BN EM				LAB			IB				CO MB				OR				STS				SBY	STOP		
	5	LMAIY(X)				AYY				LAS PY			IY				JMPL p(4)															
	6	NE GA				RED				LAS PX						TC	CALL p(4)															
	7	YNEI i(4)															BRL p(4)															
	8	XMA(XY)				SEM n(2)				REM n(2)				TM n(2)			XM AD				SEMD n(2)				REMD n(2)				TMD n(2)			
	9	LAM(XY)				LMA(XY)				SMC			ANM				LA MD				LM AD				SM CD				AN MD			
	A	RO TR	RO TL						DAA				DAS			LAY	LMID i(4)															
	B	TBR p(4)															P p(4)															
	C	XMB(XY)				BL EM				LBA						DB	CAL a(6)															
	D	LMADY(X)				SYY				LYA						DY																
	E	TD				SED				LXA			REC			SEC																
	F	LWI i(2)																														
1	0	LBI i(4)															BR b(8)															
	1	LYI i(4)																														
	2	LXI i(4)																														
	3	LAI i(4)																														
	4	LBR m(4)																														
	5	LAR m(4)																														
	6	REDD m(4)																														
	7	LAMR m(4)																														
	8	AI i(4)																														
	9	LMIIY i(4)																														
	A	TDD m(4)																														
	B	ALEI i(4)																														
	C	LRB m(4)																														
	D	LRA m(4)																														
	E	SEDD m(4)																														
	F	XMRA m(4)																														

1-word/2-cycle instruction

1-word/3-cycle instruction

RAM direct address instruction (2-word/2-cycle)

2-word/2-cycle instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	2
Pin voltage	V_T	–0.3 to (V_{CC} + 0.3)	V	
Total permissible input current	ΣI_O	100	mA	3
Total permissible output current	$-\Sigma I_O$	50	mA	4
Maximum input current	I_O	4	mA	5, 6
		30	mA	5, 7
Maximum output current	$-I_O$	4	mA	8, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	
Storage temperature (bias)	T_{bias}	–25 to +80	°C	

Note: 1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in Electrical Characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
2. D_{10} (V_{PP}) of the HD4074618.
3. Total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
4. Total permissible output current is the total of output current simultaneously flowing out from V_{CC} to all I/O pins.
5. The maximum input current is the maximum current flowing from any I/O pin to ground.
6. Applies to R0–R3
7. Applies to D_0–D_9
8. The maximum output current is the maximum current flowing from V_{CC} to any I/O pin.
9. Applies to D_0–D_9, R0–R3

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics

DC Characteristics

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0.0 V, T_a = –20 to +75 °C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	0.9 V_{CC}		V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3		V_{CC} + 0.3	V	External clock operation	
		SI	0.9 V_{CC}		V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	–0.3		0.1 V_{CC}	V		
		OSC_1	– 0.3		0.3	V	External clock operation	
		SI	–0.3		0.1 V_{CC}	V		
Output high voltage	V_{OH}	$\overline{SCK}$, TIMO SO	V_{CC} – 1.0			V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, TIMO SO			0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$ SI, SO, TIMO, OSC_1			1	µA	V_{in} = 0 to V_{CC}	1
Stop mode retain voltage	V_{STOP}	V_{CC}	2			V	No 32-kHz oscillator	7

Notes: 1. Output buffer current is excluded.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: RESET, $\overline{TEST}$ at V_{CC}
3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: D_{12}, D_{13} in digital input mode
   DTMF in operation (excludes current flowing from VT_{ref} to GND)
4. Pins D_{12} and D_{13} are in analog input mode and I/O current is not flowing.
   Test conditions: VC_{ref}/D_{11}, COMP0/D_{12}, COMP1/D_{13} at GND
   DTMF stopped
5. Timer is in operation and I/O current is not flowing.
   Test conditions: MCU in standby mode
   I/O in reset state
   Serial interface stopped
   D_{12}, D_{13} in digital input mode
   DTMF stopped
   RESET at GND
   $\overline{TEST}$ at V_{CC}
6. Applies only to HD404618.
7. RAM data retention.

DC Characteristics

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0.0 V, T_a = −20 to +75 °C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Conditions	Notes
Current dissipation in active mode	I_{CC1}	V_{CC}		400	1000	µA	V_{CC} = 3 V f_{OSC} = 400 kHz	2
	I_{CC2}	V_{CC}		500	1500	µA	V_{CC} = 3 V DTMF: active f_{OSC} = 400 kHz	3
	I_{CC3}	V_{CC}		1	2	mA	V_{CC} = 3 V f_{OSC} = 400 kHz D_{12}, D_{13} analog input mode	4
Current dissipation in standby mode	I_{SBY}	V_{CC}		200	500	µA	V_{CC} = 3 V LCD on f_{OSC} = 400 kHz	5
Current dissipation in stop mode	I_{STOP}	V_{CC}		1	10	µA	V_{CC} = 3 V No 32-kHz oscillator	
Current dissipation in subactive mode	I_{SUB}	V_{CC}		50	100	µA	V_{CC} = 3 V	
				35	70	µA	LCD on	6
Current dissipation in watch mode (1)	I_{WTC1}	V_{CC}		5	15	µA	V_{CC} = 3 V LCD off	
Current dissipation in watch mode (2)	I_{WTC2}	V_{CC}		15	35	µA	V_{CC} = 3 V LCD on	

Notes: 1. Output buffer current is excluded.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: RESET, $\overline{TEST}$ at V_{CC}

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: D_{12}, D_{13} in digital input mode
   DTMF in operation (excludes current flowing from VT_{ref} to GND)

4. Pins D_{12} and D_{13} are in analog input mode and I/O current is not flowing.
   Test conditions: VC_{ref}/D_{11}, $COMP0/D_{12}$, $COMP1/D_{13}$ at GND
   DTMF stopped

5. Timer is in operation and I/O current is not flowing.
   Test conditions: MCU in standby mode
   I/O in reset state
   Serial interface stopped
   D_{12}, D_{13} in digital input mode
   DTMF stopped
   RESET at GND
   $\overline{TEST}$ at V_{CC}

6. Applies only to HD404618.

7. RAM data retention.

I/O Characteristics for Standard Pins

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0.0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Input high voltage	V_{IH}	D_{10} – D_{13}, R0 – R3	0.7 V_{CC}	—	V_{CC} + 0.3		V	
Input low voltage	V_{IL}	D_{10} – D_{13}, R0 – R3	– 0.3	—	0.3 V_{CC}		V	
Output high voltage	V_{OH}	R0 – R3	V_{CC} – 1.0	—		$-I_{OH}$ = 0.5 mA	V	
Pull-up MOS current	$-I_P$	R0 – R3	5	40	90	V_{CC} = 3 V, V_{in} = 0 V	µA	
Output low voltage	V_{OL}	R0 – R3	—	—	0.4	I_{OL} = 0.4 mA	V	
I/O leakage current	$\|I_{IL}\|$	D_{10}	—	—	20	V_{in} = 0 to V_{CC}	µA	2
		R0 – R3 D_{11} – D_{13}	—	—	1			1
Input high voltage	V_{IHA}	D_{12}, D_{13} (analog compare mode)	VC_{ref} + 0.1	—			V	
Input low voltage	V_{ILA}	D_{12}, D_{13} (analog compare mode)	—	—	VC_{ref} – 0.1		V	
Analog input Reference voltage scope	VC_{ref}	VC_{ref}	0	—	V_{CC} – 1.2		V	

Notes: 1. Output buffer current is excluded.
2. Maximum current for HD404618 is 1 µA.

I/O Characteristics for Large-current Pins

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Input high voltage	V_{IH}	D_0 – D_9	0.7 V_{CC}	—	V_{CC} + 0.3		V	
Input low voltage	V_{IL}	D_0 – D_9	–0.3	—	0.3 V_{CC}		V	
Output high voltage	V_{OH}	D_0 – D_9	V_{CC} – 1.0	—		$-I_{OH}$ = 0.5 mA	V	
Pull-up MOS current	$-I_P$	D_0 – D_9	5	40	90	V_{CC} = 3 V, V_{in} = 0 V	µA	
Output low voltage	V_{OL}	D_0 – D_9	—	—	2.0	I_{OL} = 15 mA V_{CC} = 4.5 V to 6 V	V	
			—	—	0.4	I_{OL} = 0.4 mA		
I/O leakage current	$\|I_{IL}\|$	D_0 – D_9	—	—	1	V_{in} = 0 to V_{CC}	µA	1

Note: Output buffer current is excluded.

LCD Circuit Characteristics

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Segment driver voltage drop	V_{ds}	SEG1 – SEG32	—	—	0.6	I_d = 3 µA	V	1
Common driver voltage drop	V_{dc}	COM1 – COM4	—	—	0.3	I_d = 3 µA	V	1
LCD power supply division resistor	R_{well}		100	300	900	Between V_1 and GND	kΩ	
LCD voltage	V_{LCD}	V_1		—	V_{CC}		V	2, 3

Notes: 1. V_{ds} and V_{dc} are the voltage drops from power supply pins V_1, V_2, and V_3, and GND to each segment pin and each common pin.
2. When V_{LCD} is supplied from an external source, the following relations must be retained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$
3. The minimum value of V_{LCD} in the HD404618 is 2.7 V.
The minimum value of V_{LCD} in the HD4074618 is 3.0 V.

DTMF Characteristics

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
TONE output voltage (1)	V_{OR}	TONER	500	660	—	VT_{ref} – GND = 2.0 V, R_L = 100 kΩ	mVrms	1
TONE output voltage (2)	V_{OC}	TONEC	520	690	—	VT_{ref} – GND = 2.0 V, R_L = 100 kΩ	mVrms	1
TONE output distortion	$\%_{DIS}$		—	3	7	Short circuit between TONER and TONEC, R_L = 100 kΩ	%	2
TONE output ratio	dB_{CR}		—	2.5	—	Short circuit between TONER and TONEC, R_L = 100 kΩ	dB	2

Notes: 1. See figure 50.
2. See figure 51.

AC Characteristics

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	—	400	—	1/4 division	kHz	
			—	800	—		kHz	
		X1, X2	—	32.768	—		kHz	
Instruction cycle time	t_{cyc}		—	10	—	f_{osc} = 400 kHz	µs	
			—	5	—	f_{osc} = 800 kHz	µs	
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	7.5	f_{osc} = 400 kHz	ms	1
			—	—	7.5	f_{osc} = 800 kHz	ms	1
		X1, X2	—	—	3	T_a = –10 to +60°C	S	2
External clock frequency	f_{CP}	OSC_1	—	400	—		kHz	
			—	800	—		kHz	
External clock high width	t_{CPH}	OSC_1	1100	—	—	f_{CP} = 400 kHz	ns	3
			550	—	—	f_{CP} = 800 kHz	ns	3
External clock low width	t_{CPL}	OSC_1	1100	—	—	f_{CP} = 400 kHz	ns	3
			550	—	—	f_{CP} = 800 kHz	ns	3
External clock rise time	t_{CPr}	OSC_1	—	—	150	f_{CP} = 400 kHz	ns	3
			—	—	75	f_{CP} = 800 kHz	ns	3
External clock fall time	t_{CPf}	OSC_1	—	—	150	f_{CP} = 400 kHz	ns	3
			—	—	75	f_{CP} = 800 kHz	ns	3

Notes: 1. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for HD4074618) at power-on or after RESET input goes high after stop mode is canceled. At power-on and when stop mode is canceled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, contact the manufacturer when designing a RESET circuit.

2. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for HD4074618) at power-on. The oscillation stabilization time (t_{RC}) must be ensured. If using a crystal oscillator, contact the manufacturer to determine what oscillation stabilization time is required, since it depends on the circuit constants end stray capacitances.
3. See figure 52.
4. See figure 53. The unit t_{cyc} applies when the MCU is in standby mode or active mode.
5. See figure 54.
6. See figure 53. The unit t_{SUBcyc} applies when the MCU is in watch mode or subactive mode. t_{SUBcyc} = 244.14 µs (32.768-kHz crystal oscillator)
7. The analog comparator stabilization time is the time required for the oscillator to stabilize and for correct data to be read after D_{12}/D_{13} enter analog input mode.
8. The maximum value for HD404618 is 15 pF.

AC Characteristics

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2	—	—		t_{cyc}/ t_{SUBcyc}	4, 6
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2	—	—		t_{cyc}/ t_{SUBcyc}	4, 6
$\overline{INT_1}$ high width	t_{I1H}	$\overline{INT_1}$	2	—	—		t_{cyc}	4
$\overline{INT_1}$ low width	t_{I1L}	$\overline{INT_1}$	2	—	—		t_{cyc}	4
RESET high width	t_{RSTH}	RESET	2	—	—		t_{cyc}	5
Input capacitance	C_{in}	D_{10}	—	—	90	f = 1 MHz, V_{in} = 0 V	pF	8
		All pins except D_{10}	—	—	15	f = 1 MHz, V_{in} = 0 V	pF	
RESET fall time	t_{RSTf}		—	—	20		ms	5
Analog comparator stabilization time	t_{CSTB}	D_{12}, D_{13} (analog input mode)	—	—	2		t_{cyc}	7

Notes: 1. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for HD4074618) at power-on or after RESET input goes high after stop mode is canceled. At power-on and when stop mode is canceled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, contact the manufacturer when designing a RESET circuit.

2. The oscillation stabilization time is the time required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for HD4074618) at power-on. The oscillation stabilization time (t_{RC}) must be ensured. If using a crystal oscillator, contact the manufacturer to determine what oscillation stabilization time is required, since it depends on the circuit constants end stray capacitances.
3. See figure 52.
4. See figure 53. The unit t_{cyc} applies when the MCU is in standby mode or active mode.
5. See figure 54.
6. See figure 53. The unit t_{SUBcyc} applies when the MCU is in watch mode or subactive mode. t_{SUBcyc} = 244.14 µs (32.768-kHz crystal oscillator)
7. The analog comparator stabilization time is the time required for the oscillator to stabilize and for correct data to be read after D_{12}/D_{13} enter analog input mode.
8. The maximum value for HD404618 is 15 pF.

Serial Interface Timing Characteristics

(HD404618: V_{CC} = 2.7 V to 6.0 V, HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—		t_{cyc}/ t_{SUBcyc}	1, 2, 4
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—		t_{Scyc}	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—		t_{Scyc}	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	200		ns	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	200		ns	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	500		ns	1, 2
Serial input data setup time	t_{SSI}	SI	300	—	—		ns	1
Serial input data hold time	t_{HSI}	SI	300	—	—		ns	1

During Transmit Clock Input

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—		t_{cyc}/ t_{SUBcyc}	1, 4
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—		t_{Scyc}	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—		t_{Scyc}	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	200		ns	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	200		ns	1
Serial output data delay time	t_{DSO}	SO	—	—	500		ns	1, 2
Serial input data setup time	t_{SSI}	SI	300	—	—		ns	1
Serial input data hold time	t_{HSI}	SI	300	—	—		ns	1
Transmit clock completion detect time	t_{SCKHD}	$\overline{SCK}$	1	—	—		t_{cyc}/ t_{SUBcyc}	1, 2, 3, 4

Notes: 1. See figure 55.
2. See figure 56.
3. The transmit clock completion detect time is the period at high after eight transmit clock pulses have been input. The SCI interrupt request flag is not set if the next transmit clock is input before the transmit clock completion detect time has passed.
4. The unit t_{SUBcyc} applies when the MCU is in subactive mode.
t_{SUBcyc} = 244.14 µs (32.168-kHz crystal oscillator).

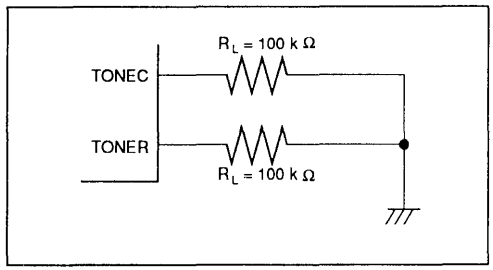


Figure 50 TONE Output Load Circuit

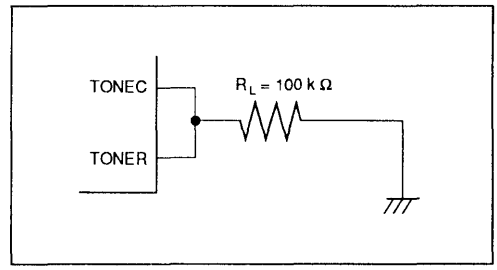


Figure 51 Distortion and dB_{CR} Load Circuit

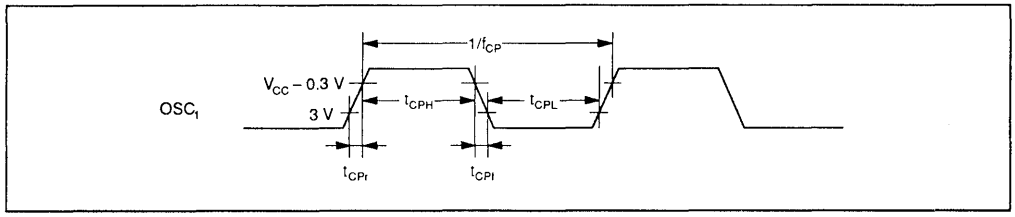


Figure 52 External Clock Timing

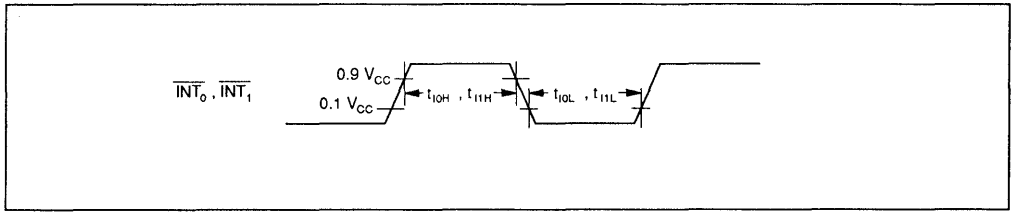


Figure 53 Interrupt Timing

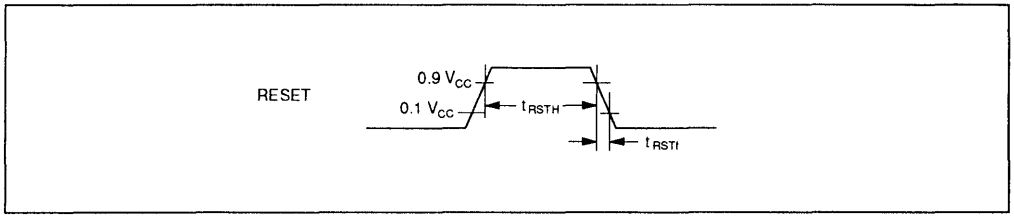
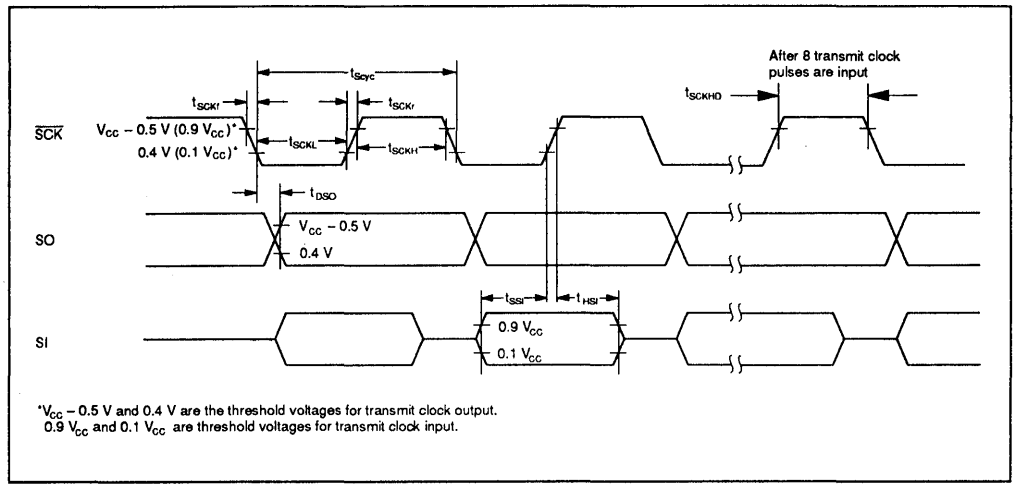


Figure 54 Reset Timing



*V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output.
0.9 V_{CC} and 0.1 V_{CC} are threshold voltages for transmit clock input.

Figure 55 Serial Interface Timing

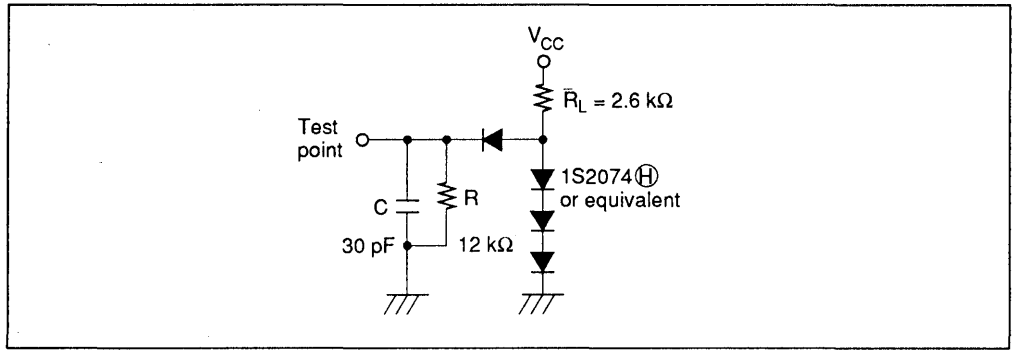


Figure 56 Timing Load Circuit

HD404618
Option List

Please enter check marks (■, ×, √) in boxes by applicable items.

Date of order	
Customer	
Department	
ROM code name	
LSI number (to be filled in by Hitachi)	

Optional functions

❒	With 32-kHz CPU operation, with time-base for clock
❒	Without 32-kHz CPU operation, with time-base for clock
❒	Without 32-kHz CPU operation, without time-base

Package type

❒	FP-80A
❒	FP-80B

ROM Code Media

ROM Code Media	
■	EPROM On-package microcomputer type

Usage Conditions Check

OSC_1 and OSC_2 Oscillator

❒	Ceramic filter	f =	kHz
❒	External clock	f =	kHz

X1 and X2 Oscillator

❒	Not used	—
❒	Crystal	f = 32.768 kHz

HD404678

4-Bit Single Chip Micro computer

Description

The HD404678 is a 4-bit single-chip HMCS400-series microcomputer for telephone applications which is designed to increase program productivity and incorporates a high-precision dual tone multi-frequency (DTMF) receiver that is especially suitable for answering machines.

HD404678

(FP-64A)

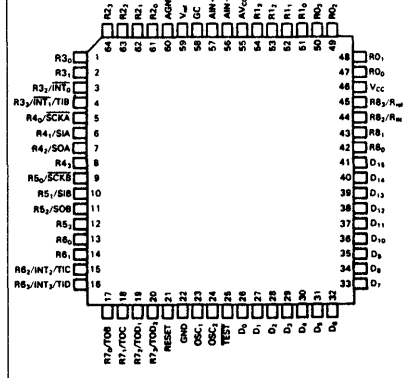
2

Features

- 8192 word x 10 bit ROM
- 512 digit x 4 bit RAM
- 48 I/O pins and 4 dedicated input pins
  - 16 large current output pins: Ten 15 mA Sinks (Maximum of 7 pins can be used at the same time) and six 10 mA Sources
- Four timer/counters
  - One 8-bit free-running timer
  - Three 8-bit reload-timer/event-counter/timer-output circuits
- Built-in 2-channel clock synchronous 8-bit serial interface
- Built-in DTMF receiver
- Built-in reset voltage variable function
- 11 interrupt sources
  - External sources: 4
  - Timer/counter: 4
  - Serial interface: 2
  - DTMF receiver: 1
- Subroutine stack: up to 16 levels including interrupts
- Instruction cycle time: 2 µs
- Two low-power dissipation modes
  - Standby mode
  - Stop mode
- Package
  - 64-pin flat plastic package (FP-64A)

Pin Arrangement

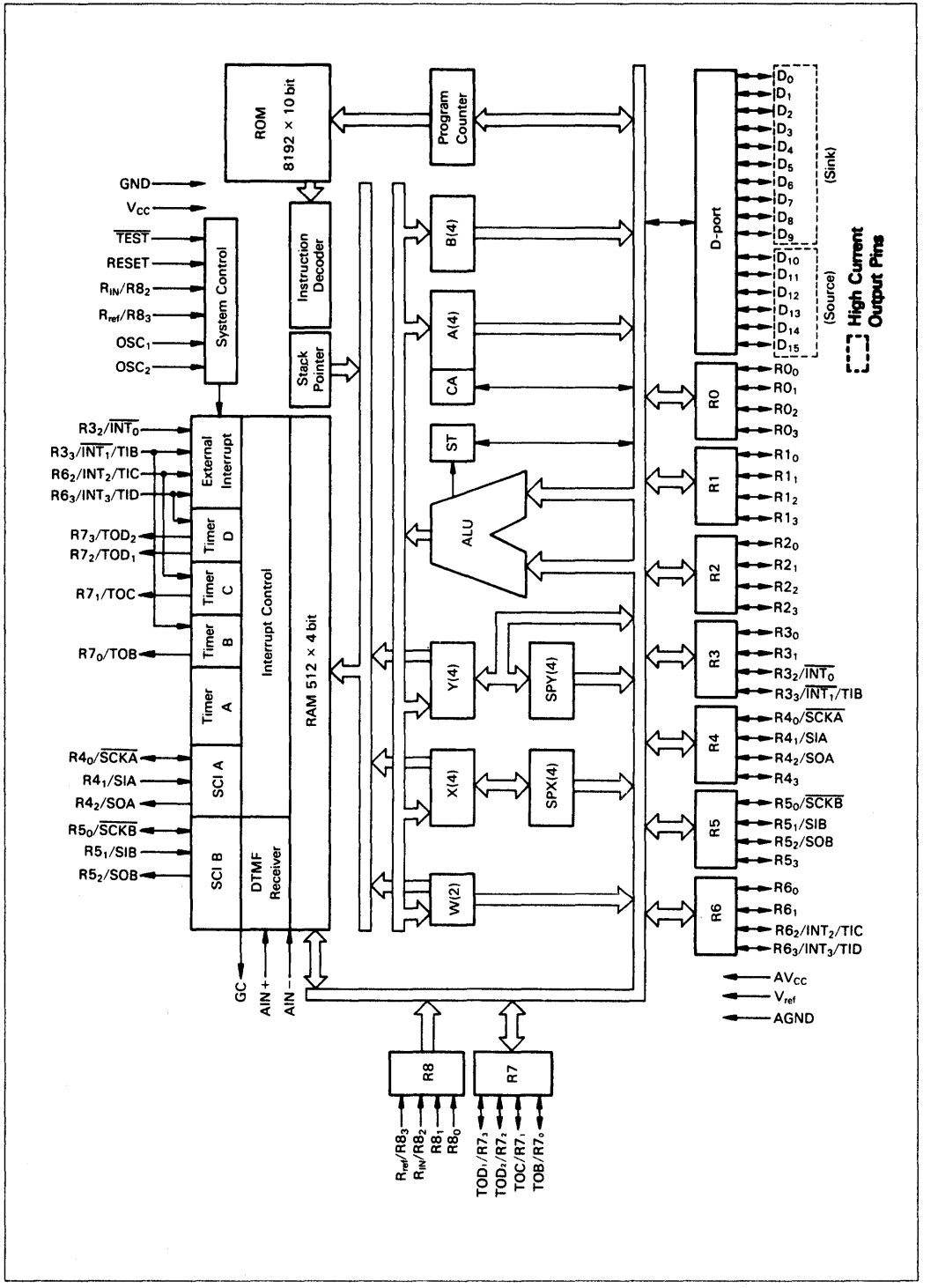
FP-64A



(Top View)

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Block Diagram



Pin Description

Function	Symbol	Pin No.	I/O	
Power	Vcc	46		Power supply voltage (5 V ± 10%)
	GND	22		Connected to the ground
Test	$\overline{\text{TEST}}$	25		Used for factory tests Connected to the Vcc
Reset	RESET	21	I	Resets the MCU
Oscillator	OSC1, OSC2	23, 24	I	Input pins for the internal oscillator circuit. Connected to the crystal oscillator or external oscillation circuit. External oscillation circuit can be connected to OSC1.
Port	D0-D9	26-35	I/O	Input/output ports. All bits can be accessed separately. Port pins are large current sink pins with pull-up MOS.
	D10-D15	36-41	I/O	Input/output ports. All bits can be accessed separately. Port pins are large current source pins with pull-down MOS.
	R00-R73	1-20, 47-54, 61-64	I/O	Input/output ports accessed with 4-bit-wide nibbles. Pins R00-R53 are standard pins with pull-up MOS while R60-R80 each has a pull-down MOS.
	R80-R83	42-45	I	An input port accessed with 4-bit-wide nibbles. Port pins are standard pins with pull-down MOS.
Interrupt	INT0-INT3	3, 4, 15, 16	I	External interrupts. These pins are multiplexed with R32, R33/TIB, R62/TIC, and R63/TID, respectively.
Serial Communication Interface	SCKA, SCKB	5, 9	I/O	Transfer clock input/output pins for SCIA, SCIB.
	SIA, SIB	6, 10	I	Receive data input pins for SCIA, SCIB.
	SOA, SOB	7, 11	O	Transmit data output pins for SCIA, SCIB.
Timer	TIB, TIC, TID	4, 15, 16	I	External clock input pins for Timers B, C, and D. These pins are multiplexed with R33/$\overline{\text{INT1}}$, R62/INT2, and R63/INT3, respectively.
	TOB, TOC, TOD1, TOD2	17-20	O	Timer output pins for Timers B, C, and D. These pins are multiplexed with R70, R71, R72, and R73, respectively.
DTMF	AVcc	55		Power supply pin for the DTMF receiver analog block. Connect it as close as possible to the power supply to set AVcc at the same potential as Vcc. Stabilized power supply must be applied.
	AGND	60		Power supply pin for the DTMF receiver analog block. Connect it as close as possible to the power supply to put AGND to the same potential as GND.
	Vref	59		DTMF receiver analog block reference voltage. A stabilized voltage AVcc/2 must be applied.
	AIN+, AIN–	57, 56	I	DTMF signal input pins for the DTMF receiver.
	GC	58	O	DTMF receiver gain control pin.
Reset Voltage Variable Circuit	Rref	45	I	A reference voltage input pin for threshold voltage of the reset voltage variable circuitry. Rref is multiplexed with R83.
	R_{IN}	44	I	An analog input pin of the reset voltage variable circuit. R_{IN} is multiplexed with R82.

HD40L4808/HD407L4808

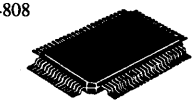
4-Bit Single Chip Microcomputer Unit

Description

The MCU is a 4-bit single chip HMCS400 series microcomputer providing high program productivity. It incorporates large size memory, LCD driver/controller, voltage comparator, and 32 kHz watch oscillator circuit.

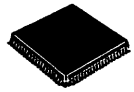
The HD407L4808, incorporating PROM, is a ZTAT microcomputer which can dramatically shorten system development period and smoothly proceed from debugging to mass production.

HD407L4808



(FP-80B)

HD40L4808



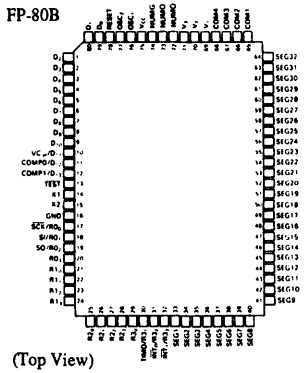
(FP-80A)

Features

- 8192 words of 10-bit ROM
- 1184 digits of 4-bit RAM
- 30 I/O pins:
  - Including 10 high-current output pins.
  - I/O pin circuit configuration
  - Input/output pull-up MOS can be selected by software
- 16-digit LCD driver
- Three timers/counters
- Clock synchronous 8-bit serial interface
- Six interrupt sources
  - External: 2
  - Internal: 4
- Subroutine stack
  - Up to 16 levels including interrupts
- Instruction cycle time:
  - 5 µs (fosc = 800 kHz for HD40L4808/HD407L4808)
- Four low power dissipation modes
  - Standby mode
  - Stop mode
  - Watch mode
  - Subactive mode (Functional Option)
- Internal oscillator:
  - Crystal or ceramic filter
  - External clock is available
- Voltage comparator (2 channels)
- Operation modes:
  - MCU mode
  - PROM mode (HD4074808/HD407L4808)
- Package
  - 80-pin flat plastic package (FP-80B) (FP-80A)

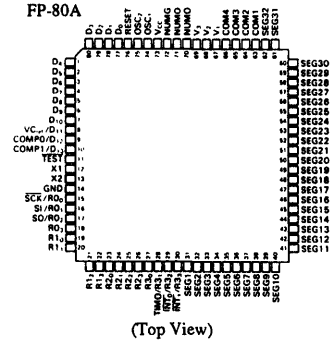
Pin Arrangement

FP-80B



(Top View)

FP-80A



(Top View)

Ordering Information

Mask ROM type

Part No.	Clock Freq. (MHz)	Package
HD40L4808FS	0.8	FP-80B
HD40L4808H		FP-80A

ZTAT type

Part No.	Clock Freq. (MHz)	Package
HD407L4808FS	0.8	FP-80B
HD407L4808H		FP-80A

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Section Three

Devices for Digital Phones, PBXs and Central Office Applications

The absolute maximum ratings referenced in the data sheet sections of this manual are limiting values, to be applied individually and beyond which operation of the described circuits may be impaired. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the circuit's reliability.

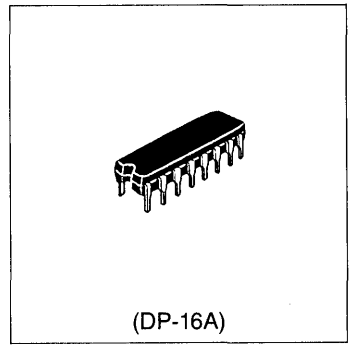
The "Electrical Characteristics" of the circuits described in this manual are for reference only.

HD44230P, HD44240P Series

Single Chip CODEC/Filter Combo LSI

Common Features

- COMBO-CODEC;
  The complete function of CODEC with filters is provided in a single chip LSI.
- CMOS Structure;
  The structure and the power down mode to reduce the CODEC power dissipation during the on-hook or nonselected channel reduce the system power requirement.
- Conventional Power Supply Requirement;
  ±5V power line operation provides the analog interface on the system ground level without DC decoupling capacitor, and the TTL level interface of digital signals. The digital ground and the analog ground is separated completely and are assigned to the respective pins, to minimize the system noise problem.
- CCITT-followed companding law;
  A-law or μ-law is selected by the metallization mask option using same base chip to assemble as the different LSI. This method is our approach to reduce both the wafer fabrication and the testing cost. And the precise A/D or D/A converters are achieved by the circuits which consist of the capacitor array for segments of companding law, and the resistor string for steps.
- Excellent Voltage Reference;
  The 2.5V reference voltage to determine the A/D conversion or D/A conversion is provided on chip. The CMOS band gap reference is stabilized using circuit techniques to the power supply voltage and the ambient temperature. The level of the reference is also adjusted internally during wafer-sort process using poly-Si fusing techniques to achieve the system gain tolerance requirement.
- Offset Cancelled Encoder;
  The internal sign-bit integration circuit with no external component compensates the offset for the small signal level or idle channel state into the first step of the companding law. The idle channel noise of A-law device is squelched by the sign-bit fixation technique.



(DP-16A)

- Switched Capacitor Filter;
  The filters conform the band pass filter for transmit side, and the low pass filter to compensate the aperture degradation for the receive side. Their clock frequencies are designed as 128 kHz for low pass filtering and 8 kHz for high pass filtering as the best approach to reduce the die size and cost. To protect the folding effect at 128 kHz clock at the analog input, 128 kHz filter cosine filter and 20 kHz (typ.) roll-off analog filter is provided on chip (antialiasing filters).
- Analog Input Gain Adjustment;
  The operational amplifier is provided to adjust the analog interface level in the range of 0-15dB.
- Open Drain Output of PCM Data;
  This provides the wired-or connection of 2 to 8 channel PCM data outputs using only one pull-up resistor, and reduce the difficulty of noise coupling to analog part through power supply line for the tri-state approach of the pin.

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

- Master Clock Generator;
  The 128 kHz master clock to determine the A/D, D/A conversion timing and to operate the switched capacitor filter is provided internally by the counter circuit to divide the bit-shift clock, or the PLL circuit to multiply the 8kHz synchronization clock, for the respective types of CODEC.
- Small/Standard Package;
  The CODEC is assembled in the small/standard 16 pin Dual-in-line ceramic package (CERDIP).

■ LINEUP & SELECTION GUIDE

The HD442030C series are revised version of HD44231B/232B/233B/234B/235/236/237/238. They have better characteristics of PSRR, absolute delay, gain stability, and analog output drivability than B series. And the CR filter of analog input is separated completely to provide the flexible analog interface configuration and to reduce the noise from negative input. They have upward and pin to pin compatibility with B series. The HD44240C series have the push/pull type of analog output to provide the large output swing for the transformer interface, despite the slightly larger power dissipation. Other configuration and characteristics are just same as HD44237C/HD44238C.

3

HITACHI SINGLE CHIP CODEC/FILTER LINEUP

Series	Type	Comp. Law	Power (Typ.)	Clock			Decoder Shift	Input Amp	Output Amp	
				Internal Clock	Sync/Async Operation	PCM Bit Clock Rate			Type	Min Load
44230P	HD44231P	A	50mW	Divider Included	Sync only	1536/ 1544/ 2048kHz	–	Fully Uncommitted OP-AMP	Single Ended	600Ω
	HD44232P	μ								
	HD44233P	A	50mW	Divider Included	Both		–			
	HD44234P	μ								
	HD44237P	A		PLL Included	Both	64- 2048kHz	–			
	HD44238P	μ					√			
44240P	HD44247P	A	70mW	PLL Included	Both	64- 2048kHz	–	Same as above	Push-Pull	600Ω
	HD44248P	μ					√			

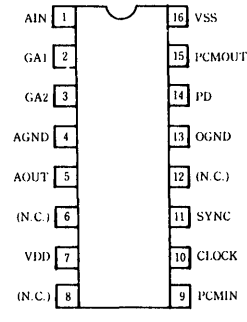
HD44231P, HD44232P, HD44233P, HD44234P

Single Chip CODEC with Filters (COMBO)

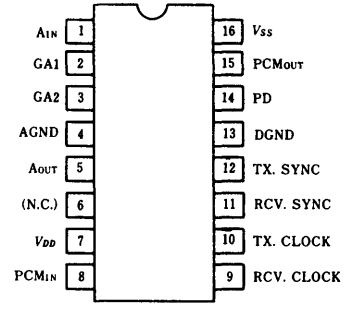
Features

- Single Chip CMOS CODEC with Filter In 16-pins DIL Package
- Power Supply Voltage ± 5 V ± 5%, Low Power Dissipation (50 mW Typ)
- Follows A-Law (HD44231P, HD44233P)
- Follows μ-Law (HD44232P, HD44234P)
- Exceeds CCITT Specifications & D4
- Synchronous (All Devices)/Asynchronous (HD44233P, HD44234P Only) Operation for 2048/1544/1536 kHz PCM Rate
- Internal Clock Generator
- Anti-Aliasing Filter (2nd order CR Active Filter)
- Voltage Reference (Internal-Trimmed)
- Input Amplifier
- Auto-Zero Cancel Circuit Without External Component

Pin Configuration



HD44231P, HD44232P



HD44233P, HD44234P

(Top View)

Figure 1 Pin Assignment

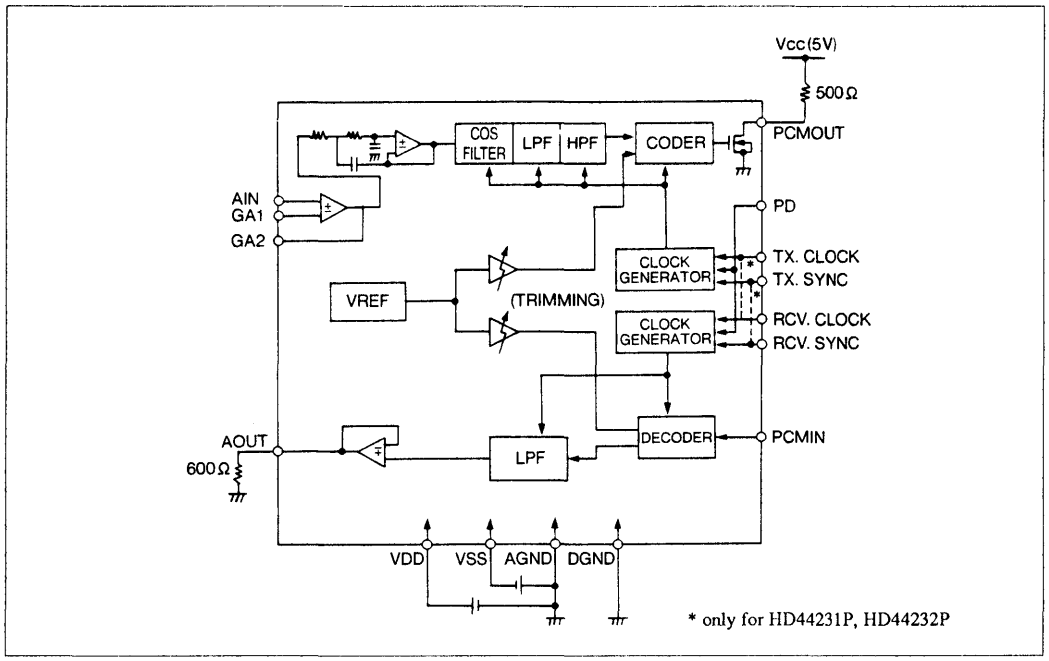


Figure 2 Block Diagram

Table 1. Pin Descriptions

HD44231P / HD44232P		HD44233P / HD44234P		Function	Remarks
No.	Symbol	No.	Symbol		
1	AIN	1	AIN	Analog Input	
2	GA1	2	GA1	Gain Adjust 1	Feed-Back Input
3	GA2	3	GA2	Gain Adjust 2	10 kΩ ≤ R_L C_L ≤ 100 pF
4	AGND	4	AGND	Analog Ground	
5	AOUT	5	AOUT	Analog Output	R_L ≥ 600 Ω, C_L ≤ 100 pF
6	N.C.	6	N.C.		Open
7	VDD	7	VDD	Positive Pow.Sup.	5 V ± 5%
9	PCMIN	8	PCMIN	PCM Data Input	(TTL)
10	CLOCK	9	RCV. CLK	PCM Bit Clock	(TTL) 2048/1544/1536 kHz
		10	TX. CLK		
11	SYNC	11	RCV. SYNC	Synchronization	(TTL) 8 kHz
		12	TX.SYNC		
13	DGND	13	DGND	Digital Ground	
14	PD	14	PD	Power Down	(TTL) "0" = down
15	PCMOUT	15	PCMOUT	PCM Data Output	Open Drain
16	VSS	16	VSS	Negative POW.SUP.	–5 V ± 5%
8	N.C				Open
12	N.C				Open

General Description

The HD44231P, HD44232P, HD44233P, HD44234P are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-law or μ-Law companding characteristic.

HD44231P and HD44233P are A-Law. HD44232P and HD44234P are μ-Law.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ± 5 V.

For a sampling rate of 8 kHz, PCM input/output data rate can be selected from 1536/1544/2048 kHz in synchronous or asynchronous (HD44233, HD44234 only) operation.

Functional Description

Figure 2 shows the simplified block diagram of the HD44231P, HD44232P, HD44233P and HD44234P. The dotted lines are connected internally to get the synchronous devices (HD44231P, HD44232P). The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44231P and HD44233P, Table 2 for HD44232P and HD44234P respectively.

A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

Transmit Section

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0 dB or 0 level in the system. This amplifier also operates as the 2 nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32 dB (typ) at 256 kHz and 40 dB (typ) at 512 kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128 kHz, followed by a 3rd Order High-Pass Filter clocked at 8 kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8 kHz. The 8-bit PCM data is clocked out by the shift clock at one of 1536/1544/2048 kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44231P and HD44233P is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A shift clock, at one of 1536/1544/2048 kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128 kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 600 Ω.

Companding Law

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 table

1 or Table 2, corresponding to their companding law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOUT is connected to AGND for about 1 ms to avoid the power-on noise.

Voltage Reference Circuit

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of ± 0.1 dB at the nominal power supply voltage and the room temperature.

Timing Requirements

The CODECs do not require that the 8 kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe, forcing the PCM output in a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8 kHz and shift clock is synchronized to it. The clock rate can be selected from 1536/1544/2048 kHz.

System Clock

The basic timing of the Codecs is provided by the shift clock.

This 1.536/1.544/2.048 MHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. No external control signal for the selection is required.

Pin/Function Descriptions

Pin	No	Descriptions
* CLOCK	10	One of 1.536, 1.544, 2.048 MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks.
**TX.CLOCK RCV.CLOCK	9 10	These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the SYNC, TX.SYNC/RCV.SYNC respectively.
* SYNC	11	These TTL compatible pulse inputs (Typ 8 kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK, TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the CLOCK, TX.CLOCK/ RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
**TX.SYNC RCV.SYNC	11 12	
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 Codecs is required.
* PCMIN	9	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK, RCV.CLOCK.
**PCMIN	8	
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10 kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 ohms. C_L should be less than 100 pF.
V_{DD} Vss AGND DGND	7 16 4 13	These are power supply pins. V_{DD} and Vss are positive and negative supply pins respectively (Typ + 5 V, –5 V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	When this TTL compatible input is held low, the chip is put into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect. This pin should be pulled-up to V_{DD} to keep the device active or to control On/Off with strobes.

* : for HD44231P, HD44232P
** : for HD44233P, HD44234P

Absolute Maximum Ratings

Item	Rating
V_{DD}	–0.3 to +7 V
V_{SS}	+0.3 to –7 V
Storage Temperature	–55°C to +125°C
Power Dissipation	0.5 W
Digital Input/Output Voltage	$-0.3\ V < V_{IN} < V_{DD} + 0.3$
Analog Input/Output Voltage	$V_{SS} - 0.3\ V < V_{IN} < V_{DD} + 0.3$

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics

Static Characteristics (V_{DD} = 5 ± 0.25 V, V_{SS} = –5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0–70°C)

Symbol	Pin HD44231P HD44232P	Pin HD44233P HD44234P	Descriptions	Min	Typ	Max	Unit	Note/Conditions
I_{DD}	7	7	V_{DD} Current (OPE.)		5.5	10	mA	Note 1)
I_{SS}	16	16	Vss Current (OPE.)	–10	–4.5			AIN = 0 V
I_{DDST}	7	7	V_{DD} Current (St.By.)		0.3	1		PCMIN = +0 CODE
I_{SSST}	16	16	Vss Current (St.By.)	–0.2				R_L(GA2) = 10 kΩ
								R_L(AOUT) = 600 kΩ
I_L	1, 2, 9, 10, 14	1, 2, 8, 9, 10, 14	Leak Current	–10.0		10.0	µA	V_M = 0.8 V
				–10.0		10.0	µA	V_M = 2.0 V
						10.0	µA	$V_{DD} = V_M$ = 5.25 V
I_{PL}	11	11, 12	Pull Up Current	–100		0	µA	
I_{DL}	15	15	Leak Current			10.0	µA	$V_{DD} = V_M$ = 5.25 V
C_{AIN2}	1, 2	1, 2	Analog Input Cap.			10	pF	at 1 MHz Vbias = 0
C_{DIN}	9, 10, 11, 14	8, 9, 10, 11, 12, 14	Input Capacitance			10	pF	at 1 MHz Vbias = 0
R_{OUTA}	5	5	AOUT Resistance		1	10	Ω	
R_{OUTG}	3	3	GA2 Resistance			30	Ω	Note 1
V_{GSW}			GA2 Output Swing	–3.0		3.0	V	R_L = 10 kΩ
V_{OFFIN}			Analog Offset Input	–500		500	mV	Note 1
V_{OFFG}			GA2 Offset Output	–50		50	mV	Note 1
V_{OFFA}			AOUT Offset Output	–50		50	mV	PCMIN = +0 – Code
C_{DOUT}	15	15	PCMOUT Capacitance			15.0	pF	at 1 MHz Vbias = 0 V
V_{OL}	15	15	PCMOUT Low Voltage			0.4	V	R_L = 500 Ω
								$+I_{OL}$ = 0.8 mA
V_{OH}	15	15	PCMOUT High Voltage	V_{CC}–0.3			V	I_{OH} = –150 mA
V_{IH}	10, 11, 9, 14	8, 10, 11, 9, 12, 14	Digital Input High Voltage	2.0			V	
V_{IL}	10,11 9,14	8, 10, 11, 9, 12, 14	Digital Input Low Voltage			0.8	V	

Note 1) Analog Input Amplifier Gain = 0 dB (Ga1 is connected to GA2)

Dynamic-Characteristics (V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, Vcc = 5 ± 0.25 V, Ta = 0 to +70°C)

Sym.	Descriptions	Min	Typ	Max	Unit	Note
FS	Synchronization Rate		8		kHz	
FC	PCM Bit Clock Rate		1536/ 1544/ 2048		kHz	
twc	Clock Pulse Width	200			ns	
twSH	SYNC Pulse High Width	200			ns	
twSL	SYNC Pulse Low Width	8			µs	
tr	Logic Input Rise Time	5		50	ns	
tf	Logic Input Fall Time	5		50	ns	
t_{BCS}	Previous Clock To SYNC Delay	40			ns	Note 1
tcs	Clock To SYNC Delay			100	ns	Note 1, 3
tcd1	Clock To PCM MSB Delay			170	ns	Note 1, 2, 4
tsd	SYNC To PCM MSB Delay			170	ns	Note 1, 2, 4
tcd	Clock To PCMOUT Delay			180	ns	Note 1, 2, 5
tsu	PCMIN Setup Time	65			ns	Note 1
thd	PCMIN Hold Time	120			ns	Note 1

Notes
1) tr, tf of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT Load Condition: 500 Ω + 165 pF + two LS-TTL Equivalent (I_{IL} = 0.8 mA, I_{IH} = –150 µA) Threshold Level (V_{OH} = 2.4 V, V_{OL} = 0.4 V)
3) Positive value shows SYNC delay from CLOCK.
4) tcd1, tsd are specified by CLOCK or SYNC which has slower rise time.
5) tcd specification is valid for the data except MSB.

System Related Characteristics (V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, Vcc = 5 ± 0.25 V, Ta = 0 to +70°C, Input Amplifier Gain = 0 dB, VREF-pin remains open GA2 Load = 10 kΩ, Aout Load = 600 Ω, Synchronous operation. FC (PCM Bit Clock) = 2048 kHz)

For HD44231P, HD44233P

Sym	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist (A to A)	820 Hz tone	–45 dBm0	25			dB	p-wgt
			–40	30			dB	
			–30 to +3	35			dB	
SNA	Signal to Dist	Noise	–55 dBm0	14			dB	
			–40	29			dB	
			–34	34			dB	
			–27 to –6	36			dB	
			–3	28			dB	
SDX	Signal to Dist (A to D)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	
SNX	Signal to Dist (A to D)	Noise	–55 dBm0	15			dB	
			–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
SDR	Signal to Dist (D to A)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	

(con'd)

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SNR	Signal to Dist	Noise	–55 dBm0	15			dB	
	(D to A)		–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
GTA	Gain Track	820 Hz tone	–55 to –50	–1.0		1.0	dB	
	(A to A)	Relative to	dBm0					
		–10 dBm0	–50 to –40	–0.5		0.5	dB	
			–40 to +3	–0.3		0.3		
GNA	Gain Track	Noise Relative	–60 to	–0.8		0.8	dB	
	(A to A)	to –10 dBm0	–55 dBm0					
			–55 to –10	–0.4		0.4	dB	
GTX	Gain Track	820 Hz tone	–55 to –50	–0.8		0.8	dB	
	(A to D)	Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to	–0.2		0.2	dB	
			+3 dBm0					
GNX	Gain Track	Noise	–60 to	–0.6		0.6	dB	
	(A to D)	Relative to	–55 dBm0					
		–10 dBm0	–55 to –40	–0.4		0.4	dB	
			–40 to –10	–0.2		0.2	dB	
GTR	Gain Track	820 Hz tone	–55 to –50	–0.8		0.8	dB	
	(D to A)	Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to	–0.2		0.2	dB	
			+3 dBm0					
GNR	Gain Track	Noise	–60 to	–0.4		0.4	dB	
	(D to A)	Relative to	–55 dBm0					
		–10 dBm0	–55 to –10	–0.2		0.2	dB	
FRX	Freq.Response	Relative to	0.06 kHz	24			dB	
	(A to D)	820 Hz	0.2	0		2.0		
	(Loss)	0dBm0	0.3 to 3	–0.15		0.15		
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
FRR	Freq. Response	Relative	0 to 3 kHz	–0.15		0.15	dB	
	(D to A)	to 820 Hz	3.18	–0.15		0.65		
	(Loss)	0 dBm0	3.4	0		0.8		
			3.78	6.5				
AIL	Analog Input	820 Hz	25°C	1.217	1.231	1.246	Vrms	
	Level	0 dBm0	nom.P.S.					
AOL	Analog Output	820 Hz	25°C	1.217	1.231	1.246	Vrms	
	Level	0 dBm0	nom. P.S.					
ICNA	Idle Ch. Noise	A to A	AIN = AGND			–78	dBmOP	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			–80	dBmOP	
ICNR	Idle Ch. Noise	D to A	PCMIN =			–81	dBmOP	
			+0–CODE					
XTKA	AIN to AOUT	820 Hz	0 dBm0			–65	dB	
	Crosstalk							
XTKD	PCMIN to	820 Hz	0 dBm0			–65	dB	
	PCMOUT							

For HD44232P, HD44234P

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist (A to A)	1020 Hz tone	–45 dBm0	25			dB	c-wgt
			–40	30			dB	
			–30 to +3	35			dB	
SDX	Signal to Dist (A to D)	1020Hz tone	–45 dBm0	26			dB	c-wgt
			–40	31			dB	
			–30 to +3	36			dB	
SDR	Signal to Dist (D to A)	1020 Hz tone	–45 dBm0	26			dB	c-wgt
			–40	31			dB	
			–30 to +3	36			dB	
GTA	Gain Tracking (A to A)	1020 Hz tone	–55 to –50 dBm0	–1.0		1.0	dB	
			–50 to –40	–0.5		0.5	dB	
			–40 to +3	–0.3		0.3	dB	
GTX	Gain Tracking (A to D)	1020 Hz tone Relative to –10 dBm0	–55 to –50	–0.8		0.8	dB	
			–50 to –40	–0.4		0.4	dB	
			–40 to +3 dBm0	–0.2		0.2	dB	
GTR	Gain Tracking (D to A)	1020 Hz tone Relative to –10 dBm0	–55 to –50	–0.8		0.8	dB	
			–50 to –40	–0.4		0.4	dB	
			–40 to +3 dBm0	–0.2		0.2	dB	
FRX	Freq.Response A to D Loss	Relative to 1020 Hz 0 dBm0	0.06 kHz	24			dB	
			0.2	0		2.0		
			0.3 to 3	–0.15		0.15		
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
FRR	Freq.Response (D to A) (Loss)	Relative to 1020 Hz 0 dBm0	0 to 3 kHz	–0.15		0.15	dB	
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
AIL	Analog Input Level	1020 Hz 0 dBm0	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
AOL	Analog Output Level	1020 Hz 0 dBm0	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
ICNA	Idle Ch. Noise	A to A	AIN = AGND			15	dBrnCO	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			15	dBrnCO	
ICNR	Idle Ch. Noise	D to A	PCMIN = +0–Code			9	dBrnCO	
XTKA	AIN to AOUT Crosstalk	1020Hz 0 dBm0				–65	dB	
XTKD	PCMIN to PCMOUT	1020 Hz 0 dBm0				–65	dB	

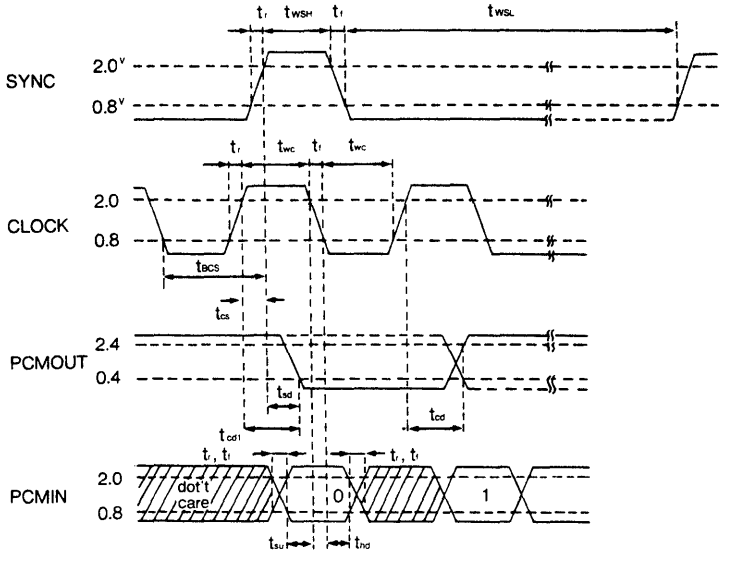
For HD44231P, HD44232P, HD44233P, HD44234P

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
AT	AIL, AOL Variation with temp.	Relative to 25°C nominal P.S.		±20			ppm/°C	
AP	AIL,AOL Variation with P.S.	25°C, Supplies ± 5%			± 0.01		dB	
ALS	Gain Variation over Temp. P.S.	A to D D to A	Initial	–0.2		–0.2	dB	Note 1)
AIP	Peak Analog Input			3.0			V	
AOP	Peak Analog Output			2.5			V	
PDL	Propagation Delay	A to A	0 dBm0		450	480	µs	
DD	Delay Distortion	A to A 0 dBm0	0.5 to 0.6 kHz			1.4		
			0.6 to 1.0			0.7	ms	rel. to min. delay
			1.0 to 2.6			0.2		
			2.6 to 2.8			1.4		
PSRR	PSRR	A to A AIN = AGND 0.3 – 50 kHz	V_{DD} Mod. = +5 V + 100 mVop	30			dB	
			Vss Mod. = –5 V + 100 mVop	30				
IM1	Intermodulation	A to A(2a-b) a; 0.47 kHz, –4 dBm0 b; 0.32, –4				–38	dB	
IM2	Intermodulation	A to A(a-b) a; 1.02 kHz, –4 dBm0 b; 0.05, –23				–52	dB	
ICS	Single Freq.Noise	A to A AIN = AGND	8,16,24, 32,40 kHz			–50	dBm0	
DIS	Discrimination	A to A 0 dBm0	4.6 to 200 kHz	30			dB	

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 to + 70° C, V_{DD}/V_{SS} = ± 5V ± 5%)

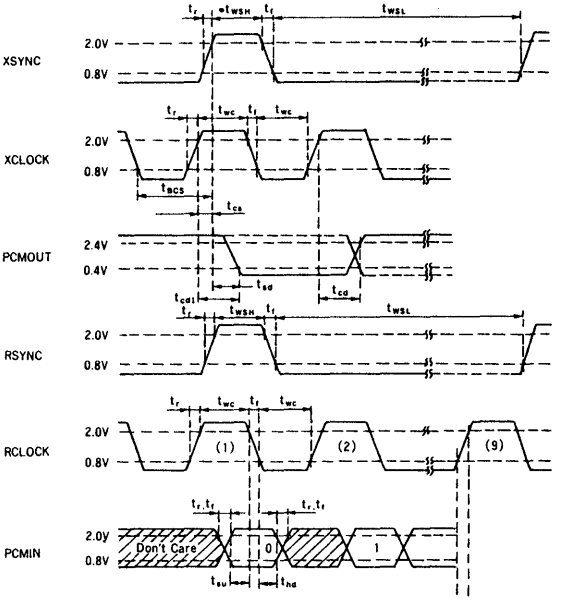
For HD44231P, HD44232P

Timing Chart



For HD44233P, HD44234P

Timing Chart



HD44237P, HD44238P

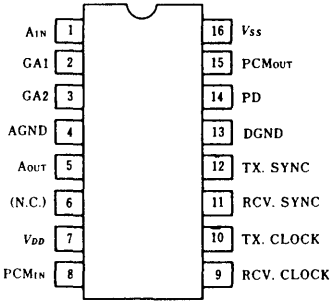
Single Chip CODEC with Filters (COMBO)

Features

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package
- Power Supply Voltage ± 5 V ± 5%, Low Power Dissipation (50 mW typ.)
- Follows A-Law (HD44237P)/μ-law(HD44238P)
- Exceeds CCITT and D4 Specifications
- Synchronous/Asynchronous Operation
- Internal Clock Generator Operation for 64 kHz to 2048 kHz PCM Rate as PLL Circuit
- Anti-Aliasing Filter (2nd order CR Active Filter)
- Voltage Reference (Internal-Trimmed)
- Input Amplifier with Uncommitted Plus/Minus Terminals
- Auto-Zero Cancel Circuit without External Component

3

Pin Configuration



(Top View)

Figure 1 Pin Assignment

Table 1. Pin Descriptions

HD44237P HD44238P No.	Symbol	Function	Remarks
1	A_{IN}	Analog Input	
2	G_{A1}	Gain Adjust 1	Feed-Back Input
3	G_{A2}	Gain Adjust 2	10 kΩ ≤ R_L C_L ≤ 100 pF
4	AGND	Analog Ground	
5	A_{OUT}	Analog Output	R_L ≥ 600 Ω, C_L ≤ 100 pF
6	N.C.		Open
7	V_{DD}	Positive Pow.Sup.	5 V ± 5%
8	PCM_{IN}	PCM Data Input	(TTL)
9	RCV.CLK	PCM Bit Clock	(TTL) 64 to 2048 kHz
10	TX.CLK		
11	RCV.SYNC	Synchronization	(TTL) 8 kHz
12	TX.SYNC		
13	DGND	Digital Ground	
14	P_D	Power Down	(TTL) "0" = down
15	PCM_{OUT}	PCM Data Output	Open Drain
16	Vss	Negative Pow.Sup.	–5 V ± 5%

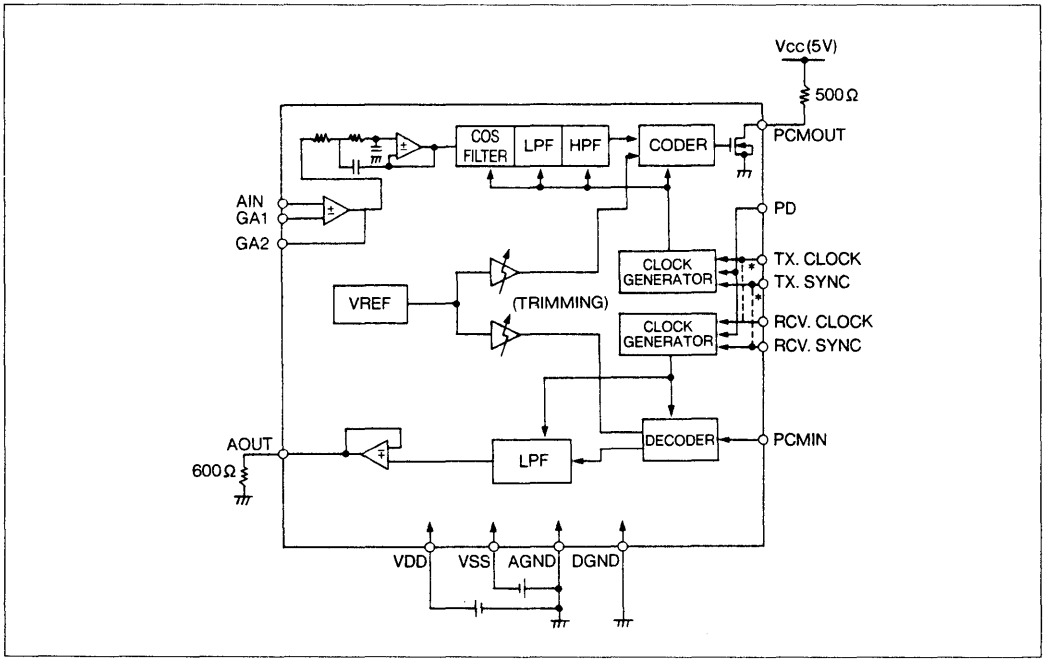


Figure 2 Block Diagram

General Description

The HD44237P, HD44238P are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-Law or μ-Law companding characteristic.

HD44237P is A-Law. HD44238P is μ-Law.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ± 5 V.

For a sampling rate of 8 kHz, PCM input/output data rate can be selected from 64 kHz to 2048 kHz in synchronous or asynchronous operation. Internal PLL circuits generate the internal clock from the 8 kHz synchronization clock.

Functional Description

Figure 2 shows the simplified block diagram of the HD44237P, HD44238P. The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44237P Table 2 for HD44238P respectively. A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

Transmit Section

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0 dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32 dB (typ) at 256 kHz and 40 dB (typ) at 512 kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128 kHz, followed by a 3rd Order High-Pass Filter clocked at 8 kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8 kHz. The 8-bit PCM data is clocked out by the shift clock at one of 64 kHz to 2048 kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44237P is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A shift clock, from 64 kHz to 2048 kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128 kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic or transformer directly as long as the impedance is greater than 600 Ω.

Companding Law

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 Table 1 or Table 2, corresponding to their companding law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The SYNC input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOUT is connected to AGND for about 1 ms to avoid the power-on noise.

Voltage Reference Circuit

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of $\pm$ 0.1 dB at the nominal power supply voltage and the room temperature.

Timing Requirements

The CODECs do not require that the 8 kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe. The PCM output goes into a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8 kHz and shift clock is synchronized to it. The clock rate can be selected from 64 kHz to 2048 kHz.

System Clock

The basic timing of the Codecs is provided by the internally generated clock from synchronization. The internal PLL (Phase Locked Loop) circuits generate 128 kHz clocks. These features make it possible that the clock rate of PCM bit shifting may be free in the range from 64 kHz to 2.048 MHz.

Bit Steal Control (HD44238P only)

For the bit steal period, the decoder output of μ-law CODEC should be shifted as half-bit of steps. For the CODECs, the power down control pin provides this function. If the low state of PD pin is less than 6 frames (0.75 ms), the device is not deactivated and the decoder output corresponding to the frame of the rising and falling edge of the pin is shifted as half-bit. And, if the low state is longer than 1.0 ms, the device is deactivated.

Pin/Function Descriptions

Pin	No	Descriptions
TX.CLOCK RCV.CLOCK	9 10	Any of 64 kHz to 2.048 MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the SYNC, TX.SYNC/RCV.SYNC respectively.
TX.SYNC RCV.SYNC	11 12	These TTL compatible pulse inputs (typ. 8 kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK, TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the CLOCK, TX.CLOCK/RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 Codecs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK, RCV.CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10 kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 ohms. C_L should be less than 100 pF.
V_{DD} Vss AGND DGND	7 16 4 13	These are power supply pins. V_{DD} and Vss are positive and negative supply pins respectively (typ. +5 V, –5 V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	When this TTL compatible input is held low, the chip is put into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect. This pin should be pulled-up to V_{DD} to keep the device active or to control On/Off with strobes. For the μ-law devices, this pin also provides the half-bit decoder shift for the bit-steal frame according to alternating the state of the input.

Absolute Maximum Ratings

Item	Rating
V_{DD}	–0.3 to +7 V
V_{SS}	+0.3 to –7 V
Storage Temperature	–55°C to 125°C
Power Dissipation	0.5 W
Digital Input/Output Voltage	$-0.3\ V < V_{IN} < V_{DD} + 0.3$
Analog Input/Output Voltage	$V_{SS} - 0.3\ V < V_{IN} < V_{DD} + 0.3$

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics

Static Characteristics ($V_{DD} = 5 \pm 0.25$ V, $V_{SS} = -5 \pm 0.25$ V, $V_{CC} = 5 \pm 0.25$ V, Ta = 0 to + 70° C)

Sym.	Pin No.	Descriptions	Min	Typ	Max	Unit	Note/Conditions
I_{DD}	7	V_{DD} Current (OPE.)		5.5	10	mA	Note 1
Iss	16	Vss Current (OPE.)	–10	–4.5			AIN = 0 V
IDDST	7	V_{DD} Current (St.By.)		0.3	1		PCMIN = +0 CODE
ISSST	16	Vss Current (St.By.)	–0.2				R_L(GA2) = 10 kΩ
							R_L(AOUT) = 600 Ω
IL	1, 2, 8,	Leak Current	–10.0		10.0	μA	V_M = 0.8 V
	9, 10, 14		–10.0		10.0	μA	V_M = 2.0 V
					10.0	μA	$V_{DD} = V_M$ = 5.25 V
IPL	11, 12	Pull Up Current	–100		0	μA	
IDL	15	Leak Current			10.0	μA	$V_{DD} = V_M$ = 5.25 V
CAIN2	1, 2	Analog Input Cap.			10	pF	at 1 MHz Vbias = 0
CDIN	8, 9, 10,	Input Capacitance			10	pF	at 1 MHz Vbias = 0
	11, 12, 14						
ROUTA	5	AOUT Resistance		1	10	Ω	
ROUTG	3	GA2 Resistance			30	Ω	Note 1
VGSW	3	GA2 Output Swing	–3.0		3.0	V	R_L = 10 kΩ
VOFFIN	1	Analog Offset Input	–500		500	mV	Note 1
VOFFG	3	GA2 Offset Output	–50		50	mV	Note 1
VOFFA	5	AOUT Offset Output	–50		50	mV	PCMIN = +0 – Code
CDOUT	15	PCMOUT Capacitance			15.0	pF	at 1 MHz Vbias = 0 V
V_{OL}	15	PCMOUT Low Voltage			0.4	V	R_L = 500 Ω
							$+I_{OL}$ = 0.8 mA
V_{OH}	15	PCMOUT High Voltage	Vcc–0.3			V	I_{OH} = –150 μA
V_{IH}	8, 10, 11,	Digital Input High	2.0			V	
	9, 12, 14	Voltage					
V_{IL}	8, 10, 11,	Digital Input Low Voltage			0.8	V	
	9, 12, 14						

Note 1) Analog Input Amplifier Gain = 0 dB (Ga1 is connected to GA2)

Dynamic-Characteristics (V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, Vcc = 5 ± 0.25 V, Ta = 0 to +70°C)

Sym.	Descriptions	Min	Typ	Max	Unit	Note
FS	Synchronization Rate		8		kHz	
FC	PCM Bit Clock Rate	64		2048	kHz	
twc	Clock Pulse Width	200			ns	
twSH	SYNC Pulse High Width	200			ns	
twSL	SYNC Pulse Low Width	8			µs	
tr	Logic Input Rise Time	5		50	ns	
tf	Logic Input Fall Time	5		50	ns	
tBCS	Previous Clock To SYNC Delay	40			ns	Note 1
tcs	Clock To SYNC Delay			100	ns	Note 1, 3
tcd1	Clock To PCM MSB Delay			170	ns	Note 1, 2, 4
tsd	SYNC To PCM MSB Delay			170	ns	Note 1, 2, 4
tcd	Clock To PCMOUT Delay			180	ns	Note 1, 2, 5
tsu	PCMIN Setup Time	65			ns	Note 1
thd	PCMIN Hold Time	120			ns	Note 1
tbs	PD (bit-steal) Setup	200			ns	Note 1, 6
tbh	PD (bit-steal) Hold	200			ns	Note 1, 6

Notes 1) tr, tf of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT Load Condition: 500 Ω+165 pF+ two LS-TTL Equivalent (I_{IL} = 0.8 mA, I_{IH} = –150 µA) Threshold Level (V_{OH} = 2.4 V, V_{OL} = 0.4 V)
3) Positive value shows SYNC delay from CLOCK.
4) tcd1, tsd are specified by CLOCK or SYNC which has slower rise time.
5) tcd specification is valid for the data except MSB.
6) Applicable HD44238P

System Related Characteristics (V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, Vcc = 5 ± 0.25 V, Ta = 0 to +70°C, Input Amplifier Gain = 0 dB, GA2 Load = 10 kΩ, Aout Load = 600 Ω, Synchronous operation. FC (PCM Bit Clock) = 2048 kHz)

For HD44237P

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist. (A to A)	820 Hz tone	–45 dBm0	25			dB	p-wgt
			–40	30			dB	
			–30 to +3	35			dB	
SNA	Signal to Dist. (A to A)	Noise	–55 dBm0	14			dB	
			–40	29			dB	
			–34	34			dB	
			–27 to –6	36			dB	
			–3	28			dB	
SDX	Signal to Dist. (A to D)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	
SNX	Signal to Dist. (A to D)	Noise	–55 dBm0	15			dB	
			–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
SDR	Signal to Dist. (D to A)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	

(con'd)

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SNR	Signal to Dist (D to A)	Noise	–55 dBm0	15			dB	
			–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
GTA	Gain Track (A to A)	820 Hz tone	–55 to –50 dBm0	–1.0		1.0	dB	
		Relative to	–50 to –40	–0.5		0.5	dB	
		–10 dBm0	–40 to +3	–0.3		0.3	dB	
GNA	Gain Track (A to A)	Noise	–60 to –55 dBm0	–0.8		0.8	dB	
		Relative to	–55 to –10	–0.4		0.4	dB	
		–10 dBm0						
GTX	Gain Track (A to D)	820 Hz tone	–55 to –50	–0.8		0.8	dB	
		Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
GNX	Gain Track (A to D)	Noise	–60 to –55 dBm0	–0.6		0.6	dB	
		Relative to	–55 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to –10	–0.2		0.2	dB	
GTR	Gain Track (D to A)	820 Hz tone	–55 to –50	–0.8		0.8	dB	
		Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
GNR	Gain Track (D to A)	Noise	–60 to –55 dBm0	–0.4		0.4	dB	
		Relative to	–55 to –10	–0.2		0.2	dB	
		–10 dBm0						
FRX	Freq.Response (A to D) (Loss)	Relative to 820 Hz 0 dBm0	0.06 kHz	24			dB	
			0.2	0		2.0		
			0.3 to 3	–0.15		0.15		
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
FRR	Freq.Response (D to A) (Loss)	Relative to 820 Hz 0 dBm0	0 to 3 kHz	–0.15		0.15	dB	
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
AIL	Analog Input Level	820 Hz 0 dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
AOL	Analog Output Level	820 Hz 0 dBm0	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
ICNA	Idle Ch. Noise	A to A	AIN = AGND			–78	dBmOP	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			–80	dBmOP	
ICNR	Idle Ch. Noise	D to A	PCMIN = +0–CODE			–80	dBmOP	
XTKA	AIN to AOUT Crosstalk	820 Hz	0 dBm0			–65	dB	
XTKD	PCMIN to PCMOUT	820 Hz	0 dBm0			–65	dB	

For HD44238P

Sym	Pin No.	Descriptions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist. (A to A)	1020 Hz tone	–45 dBm0	25			dB	c-wgt
			–40	30			dB	
			–30 to +3	35			dB	
SDX	Signal to Dist. (A to D)	1020Hz tone	–45 dBm0	26			dB	c-wgt
			–40	31			dB	
			–30 to +3	36			dB	
SDR	Signal to Dist. (D to A)	1020 Hz tone	–45 dBm0	26			dB	c-wgt
			–40	31			dB	
			–30 to +3	36			dB	
GTA	Gain Tracking (A to A)	1020 Hz tone Relative to 10 dBm0	–55 to –50 dBm0	–1.0		1.0	dB	
			–50 to –40	–0.5		0.5	dB	
			–40 to +3	–0.3		0.3	dB	
GTX	Gain Tracking (A to D)	1020 Hz tone Relative to –10 dBm0	–55 to –50	–0.8		0.8	dB	
			–50 to –40	–0.4		0.4	dB	
			–40 to +3 dBm0	–0.2		0.2	dB	
GTR	Gain Tracking (D to A)	1020 Hz tone Relative to –10 dBm0	–55 to –50	–0.8		0.8	dB	
			–50 to –40	–0.4		0.4	dB	
			–40 to +3 dBm0	–0.2		0.2	dB	
FRX	Freq.Response (A to D) (Loss)	Relative to 1020 Hz 0 dBm0	0.06 kHz	24			dB	
			0.2	0		2.0	dB	
			0.3 to 3	–0.15		0.15	dB	
			3.18	–0.15		0.65	dB	
			3.4	0		0.8	dB	
			3.78	6.5			dB	
FRR	Freq.Response (D to A) (Loss)	Relative to 1020 Hz 0 dBm0	0 to 3 kHz	–0.15		0.15	dB	
			3.18	–0.15		0.65	dB	
			3.4	0		0.8	dB	
			3.78	6.5			dB	
AIL	Analog Input Level	1020 Hz 0 dBm0	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
AOL	Analog Output Level	1020 Hz 0 dBm0	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
ICNA	Idle Ch. Noise	A to A	AIN = AGND			16	dBrnCO	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			16	dBrnCO	
ICNR	Idle Ch. Noise	D to A	PCMIN = +0–Code			10	dBrnCO	
XTKA	AIN to AOUT Crosstalk	1020Hz 0 dBm0				–65	dB	
XTKD	PCMIN to PCMOUT	1020 Hz 0 dBm0				–65	dB	

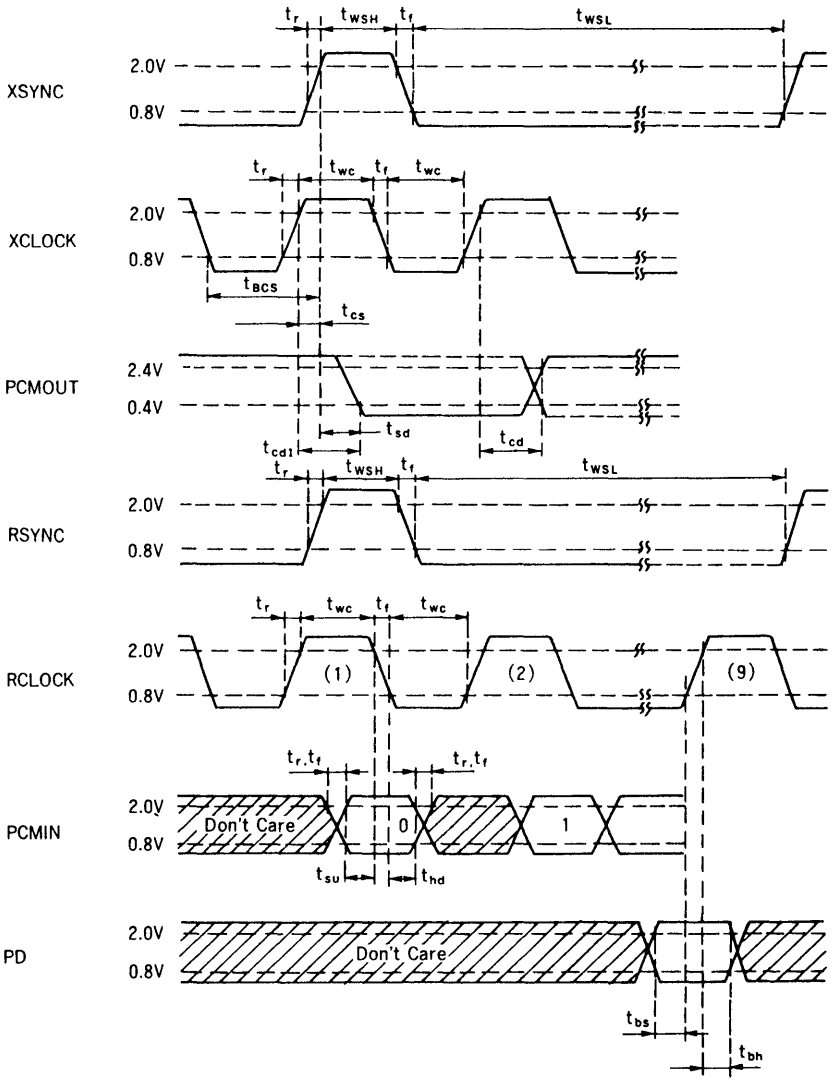
3

For HD44237P, HD44238P

Sym.	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
AT	AIL, AOL Variation with temp.	Relative to 25°C nominal P.S.			±20		ppm/°C	
AP	AIL,AOL Variation with P.S.	25°C, Supplies ± 5%			± 0.01		dB	
ALS	GAIN Variation over Temp. P.S.	A to D D to A	Initial	–0.2		–0.2	dB	Note 1)
AIP	Peak Analog Input			3.0			V	
AOP	Peak Analog Output			2.5			V	
PDL	Propagation Delay	A to A	0 dBm0		450	480	µs	
DD	Delay Distortion	A to A 0 dBm0	0.5 to 0.6 kHz			1.4	ms	
			0.6 to 1.0			0.7		rel. to min. delay
			1.0 to 2.6			0.2		
			2.6 to 2.8			1.4		
PSRR	PSRR	A to A AIN = AGND 0.3 – 50 kHz	V_{DD} Mod. = +5 V + 100 mVop	30			dB	
			Vss Mod. = –5 V + 100 mVop	30				
IM1	Intermodulation	A to A(2a-b) a; 0.47 kHz, –4 dBm0 b; 0.32, –4				–38	dB	
IM2	Intermodulation	A to A(a-b) a; 1.02 kHz, –4 dBm0 b; 0.05, –23				–52	dB	
ICS	Single Freq.Noise	A to A AIN = AGND	8,16,24, 32,40 kHz			–50	dBm0	
DIS	Discrimination	A to A 0 dBm0	4.6 to 200 kHz	30			dB	

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 to +70°C, V_{DD}/Vss = ± 5 V ± 5%)

Timing Chart



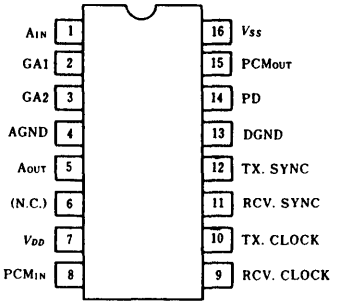
HD44247P, HD44248P

Single Chip CODEC with Filters (COMBO)

Features

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package
- Power Supply Voltage ± 5 V ± 5%, Low Power Dissipation
- Follows μ-Law (HD44248P) or A-Law (HD44247P)
- Exceeds CCITT and D4 Specifications
- Asynchronous and Synchronous Operation
- Internal Clock Generator for 64 kHz to 2048 kHz PCM Rate As PLL Circuit
- Anti-Aliasing Filter (2nd order CR Active Filter)
- Voltage Reference (Internal-Trimmed)
- Input Amplifier with Uncommitted Plus/Minus Terminals
- Auto-Zero Cancel Circuit Without External Component
- Push/Pull Analog Output

Pin Configuration



(Top View)

Figure 1 Pin Assignment

Table 1. Pin Descriptions

No.	Symbol	Function	Remarks
1	A_{IN}	Analog Input	
2	G_{A1}	Gain Adjust 1	Feed-Back Input
3	G_{A2}	Gain Adjust 2	10 kΩ ≤ R_L C_L ≤ 100 pF
4	AGND	Analog Ground	
5	A_{OUT} (+)	Analog Output	R_L ≥ 600 Ω, CL < 100 pF
6	A_{OUT} (–)		R_L ≥ 600 Ω, CL ≤ 100 pF
7	V_{DD}	Positive Pow.Sup.	5 V ± 5%
8	PCM_{IN}	PCM Data Input	(TTL)
9	RCV.CLK	PCM Bit Clock	(TTL) 64 kHz to 2048 kHz
10	TX.CLK		
11	RCV.SYNC	Synchronization	(TTL) 8 kHz
12	TX.SYNC		
13	DGND	Digital Ground	
14	PD	Power Down	(TTL) "0" = down
15	PCM_{OUT}	PCM Data Output	Open Drain
16	Vss	Negative Pow.Sup.	–5 V ± 5%

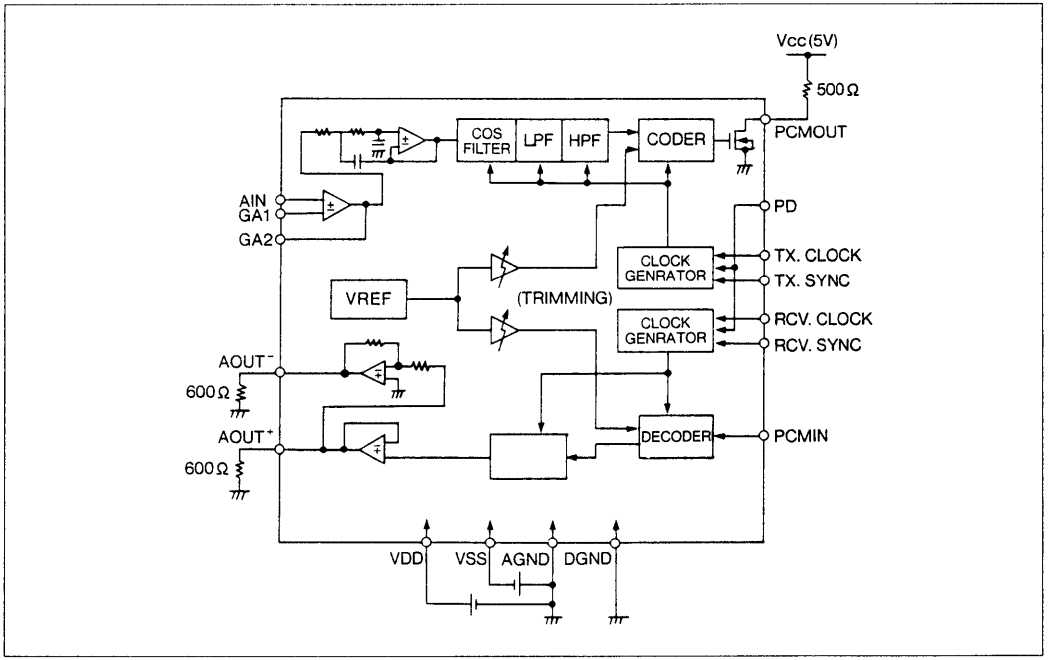


Figure 2 Block Diagram

General Description

The HD44247P and HD44248P are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-Law or μ-Law companding characteristic.

HD44247P is A-Law device and HD44248P is μ-Law device.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ± 5 V.

For a sampling rate of 8 kHz, PCM input/output data rate can be selected from 64 kHz to 2048 kHz in synchronous or asynchronous operation. The inverted analog output is provided for the balanced transformer interface.

Functional Description

Figure 2 shows the simplified block diagram of the HD44247P and HD44248P. The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44247P, Table 2 for HD44248P respectively. A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

Transmit Section

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0 dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32 dB (Typ) at 256 kHz and 40 dB (Typ) at 512 kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128 kHz, followed by a 3rd Order High-Pass Filter clocked at 8 kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8 kHz. The 8-bit PCM data is clocked out by the shift clock at one of from 64 kHz to 2048 kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44247P is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A shift clock, from 64 kHz to 2048 kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128 kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic or transformer directly as long as the impedance is greater than 600 Ω.

Companding Law

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 Table 1 or Table 2, corresponding to their companding law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The SYNC input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOUT is connected to AGND for about 1 ms to avoid the power-on noise.

Voltage Reference Circuit

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of ± 0.1 dB at the nominal power supply voltage and the room temperature.

Timing Requirements

The CODECs do not require that the 8 kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe. The PCM output goes into a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8 kHz and shift clock is synchronized to it. The clock rate can be selected from 64 to 2048 kHz.

System Clock

The basic timing of the Codecs is provided by the internally generated clock from synchronization. The internal PLL (Phase Locked Loop) circuits generate 128 kHz clocks. These features make it possible that the clock rate of PCM bit shifting may be free in the range from 64 kHz to 2.048 MHz.

Bit Steal Control (HD44248P only)

For the bit steal period, the decoder output of μ-law CODEC should be shifted as half-bit of steps. For the CODECs, the power down control pin provides this function. If the low state of PD pin is less than 6 frames (0.75 msec), the device is not deactivated and the decoder output corresponding to the frame of the rising and falling edge of the pin is shifted as half-bit. And, if the low state is longer than 1.0 ms, the device is deactivated.

Push-Pull Analog Output

The CODECs have the inverted output ($AOUT^-$) of the buffered filters output of receive side ($AOUT^+$). So, the CODECs can be interfaced directly to the balanced transformer to get the larger output level using the conventional power supply voltage (± 5 V).

Pin/Function Descriptions

Pin	No.	Descriptions
TX.CLOCK RCV.CLOCK	9 10	Any of 64 kHz to 2.048 MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX.SYNC/RCV.SYNC respectively.
TX.SYNC RCV.SYNC	11 12	These TTL compatible pulse inputs (Typ. 8 kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV.CLOCK.
AIN GA1 GA2	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10 kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT(+)	5	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100 pF.
V_{DD} Vss AGND DGND	7 16 4 13	These are power supply pins. V_{DD} and Vss are positive and negative supply pins respectively (Typ. +5 V, –5 V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect. This pin should be pulled-up to V_{DD} to keep the device active or to control On/Off with strobes. For the μ-law devices, this pin also provides the half-bit decoder shift for the bit-steal frame according to alternating the state of the input.
AOUT(–)	6	This is the inverted output of pin 5 signal output to drive the 600 Ω transformer as the push-pull operation. $R_L \geq 600\ \Omega$, $C_L \leq 100$ pF

Absolute Maximum Ratings

Item	Rating
V_{DD}	–0.3 to +7 V
V_{SS}	+0.3 to –7 V
Storage Temperature	–55°C to +125°C
Power Dissipation	0.5 W
Digital Input/Output Voltage	$-0.3\ V < V_{IN} < V_{DD} + 0.3$
Analog Input/Output Voltage	$V_{SS} - 0.3\ V < V_{IN} < V_{DD} + 0.3$

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

3

Electrical Characteristics

Static Characteristics ($V_{DD} = 5 \pm 0.25$ V, $V_{SS} = -5 \pm 0.25$ V, $V_{CC} = 5 \pm 0.25$ V, Ta = 0–70°C)

Symbol	Pin	Descriptions	Min	Typ	Max	Unit	Note/Conditions
I_{DD}	7	V_{DD} Current (OPE.)		8.0	13.5	mA	Note 1)
I_{SS}	16	V_{SS} Current (OPE.)	–13.0	–7.5			AIN = 0 V
I_{DDST}	7	V_{DD} Current (St.By.)		0.4	1.0		PCMIN = +0 CODE
I_{SSST}	16	V_{SS} Current (St.By.)	–0.2				R_L(GA2) = 10 kΩ
							R_L(AOUT) = 600 kΩ
I_L	1, 2, 8,	Leak Current	–10.0		10.0	µA	V_M = 0.8 V
	9, 10, 14		–10.0		10.0	µA	V_M = 2.0 V
					10.0	µA	$V_{DD} = V_M$ = 5.25 V
I_{PL}	11, 12	Pull Up Current	–100		0	µA	
I_{DL}	15	Leak Current			10.0	µA	$V_{DD} = V_M$ = 5.25 V
C_{AIN1}	1	Analog Input Cap.			10	pF	at 1 MHz Vbias = 0V
C_{AIN2}	2						
C_{DIN}	8, 9, 10,	Input Capacitance			10	pF	at 1 MHz Vbias = 0V
	11, 12, 14						
R_{OUTA}	5, 6	AOUT Resistance		1	10	Ω	
R_{OUTG}	3	GA2 Resistance			30	Ω	Note 1
V_{GSW}	3	GA2 Output Swing	–3.0		3.0	V	R_L = 10 kΩ
V_{OFFIN}	1	Analog Offset Input	–500		500	mV	Note 1
V_{OFFG}	3	GA2 Offset Output	–50		50	mV	Note 1
V_{OFFA}	5, 6	AOUT Offset Output	–50		50	mV	PCMIN = +0 – Code
C_{DOUT}	15	PCMOUT Capacitance			15.0	pF	at 1 MHz Vbias = 0 V
V_{OL}	15	PCMOUT Low Voltage			0.4	V	R_L = 500 Ω
							$+I_{OL}$ = 0.8 mA
V_{OH}	15	PCMOUT High Voltage	V_{CC}–0.3			V	I_{OH} = –150 µA
V_{IH}	8, 10, 11,	Digital Input High	2.0			V	
	9, 12, 14	Voltage					
V_{IL}	8, 10, 11,	Digital Input Low Voltage			0.8	V	
	9, 12, 14						

Note 1) Analog Input Amplifier Gain = 0 dB (Ga1 is connected to GA2)

Dynamic-Characteristics (V_{DD} = 5 ± 0.25 V, V_{SS} = –5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0–70°C)

Symbol	Descriptions	Min	Typ	Max	Unit	Note
FS	Synchronization Rate		8		kHz	
FC	PCM Bit Clock Rate	64		2048	kHz	
twc	Clock Pulse Width	200			ns	
twSH	SYNC Pulse High Width	200			ns	
twSL	SYNC Pulse Low Width	8			µs	
tr	Logic Input Rise Time	5		50	ns	
tf	Logic Input Fall Time	5		50	ns	
tBCS	Previous Clock To SYNC Delay	40			ns	Note 1
tcs	Clock To SYNC Delay			100	ns	Note 1, 3
tcd1	Clock To PCM MSB Delay			170	ns	Note 1, 2, 4
tsd	SYNC To PCM MSB Delay			170	ns	Note 1, 2, 4
tcd	Clock To PCMOUT Delay			180	ns	Note 1, 2, 5
tsu	PCMIN Setup Time	65			ns	Note 1
thd	PCMIN Hold Time	120			ns	Note 1
tbs	PD (bit-steal) Setup	200			ns	Note 1, 6
tbh	PD (bit-steal) Hold	200			ns	Note 1, 6

Notes
1) tr, tf of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT Load Condition: 500 Ω+165 pF+ two LS-TTL Equivalent (I_{IL} = 0.8 mA, I_{IH} = –150 µA) Threshold Level (V_{OH} = 2.4 V, V_{OL} = 0.4 V)
3) Positive value shows SYNC delay from CLOCK.
4) tcd1, tsd are specified by CLOCK or SYNC which has slower rise time.
5) tcd specification is valid for the data except MSB.
6) Applicable HD44248P

System Related Characteristics (V_{DD} = 5 ± 0.25 V, V_{SS} = –5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0 to +70°C, Input Amplifier Gain = 0 dB, Analog Output = Aout (–), GA2 Load = 10 kΩ, Aout Load = 600 Ω, Synchronous operation. FC (PCM Bit Clock) = 2048 kHz)

For HD44247P

Symbol	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist (A to A)	820 Hz tone	–45 dBm0	25			dB	p-wgt
			–40	30			dB	
			–30 to +3	35			dB	
SNA	Signal to Dist (A to A)	Noise	–55 dBm0	14			dB	
			–40	29			dB	
			–34	34			dB	
			–27 to –6	36			dB	
			–3	28			dB	
SDX	Signal to Dist (A to D)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	
SNX	Signal to Dist (A to D)	Noise	–55 dBm0	15			dB	
			–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
SDR	Signal to Dist (D to A)	820 Hz tone	–45 dBm0	26			dB	p-wgt
			–40	31			dB	
			–30 to +3	36			dB	

(con'd)

Symbol	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SNR	Signal to Dist.	Noise	–55 dBm0	15			dB	
	(D to A)		–40	30			dB	
			–34	35			dB	
			–27 to –6	37			dB	
GTA	Gain Track. (A to A)	820 Hz tone	–55 to –50 dBm0	–1.0		1.0	dB	
		Relative to	–50 to –40	–0.5		0.5	dB	
		–10 dBm0	–40 to +3	–0.3		0.3	dB	
GNA	Gain Track. (A to A)	Noise	–60 to –55 dBm0	–0.8		0.8	dB	
		Relative to	–55 to –10	–0.4		0.4	dB	
		–10 dBm0						
GTX	Gain Track. (A to D)	820 Hz tone	–55 to –50	–0.8		0.8	dB	
		Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
GNX	Gain Track. (D to A)	Noise	–60 to –55 dBm0	–0.6		0.6	dB	
		Relative to	–55 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to –10	–0.2		0.2	dB	
GTR	Gain Track. (A to D)	820 Hz tone	–55 to –50	–0.8		0.8	dB	
		Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
GNR	Gain Track. (D to A)	Noise	–60 to –55 dBm0	–0.4		0.4	dB	
		Relative to	–55 to –10	–0.2		0.2	dB	
		–10 dBm0						
FRX	Freq.Response	Relative to	0.06 kHz	24			dB	
	(A to D) (Loss)	820 Hz	0.2	0		2.0		
		0 dBm0	0.3 to 3	–0.15		0.15		
			3.18	–0.15		0.65		
			3.4	0		0.8		
			3.78	6.5				
FRR	Freq.Response	Relative to	0 to 3 kHz	–0.15		0.15	dB	
	(D to A) (Loss)	820 Hz	3.18	–0.15		0.65		
		0 dBm0	3.4	0		0.8		
			3.78	6.5				
AIL	Analog Input Level	820 Hz	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
		0 dBm0						
AOL	Analog Output Level	820 Hz	25°C nom.P.S.	1.217	1.231	1.246	Vrms	
		0 dBm0						
ICNA	Idle Ch. Noise	A to A	AIN = AGND			–78	dBm0P	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			–80	dBm0P	
ICNR	Idle Ch. Noise	D to A	PCMIN =			–80	dBm0P	
			+0–CODE					
XTKA	AIN to AOUT	820 Hz	0 dBm0			–65	dB	
	Crosstalk							
XTKD	PCMIN to PCMOUT	820 Hz	0 dBm0			–65	dB	

3

For HD44248P

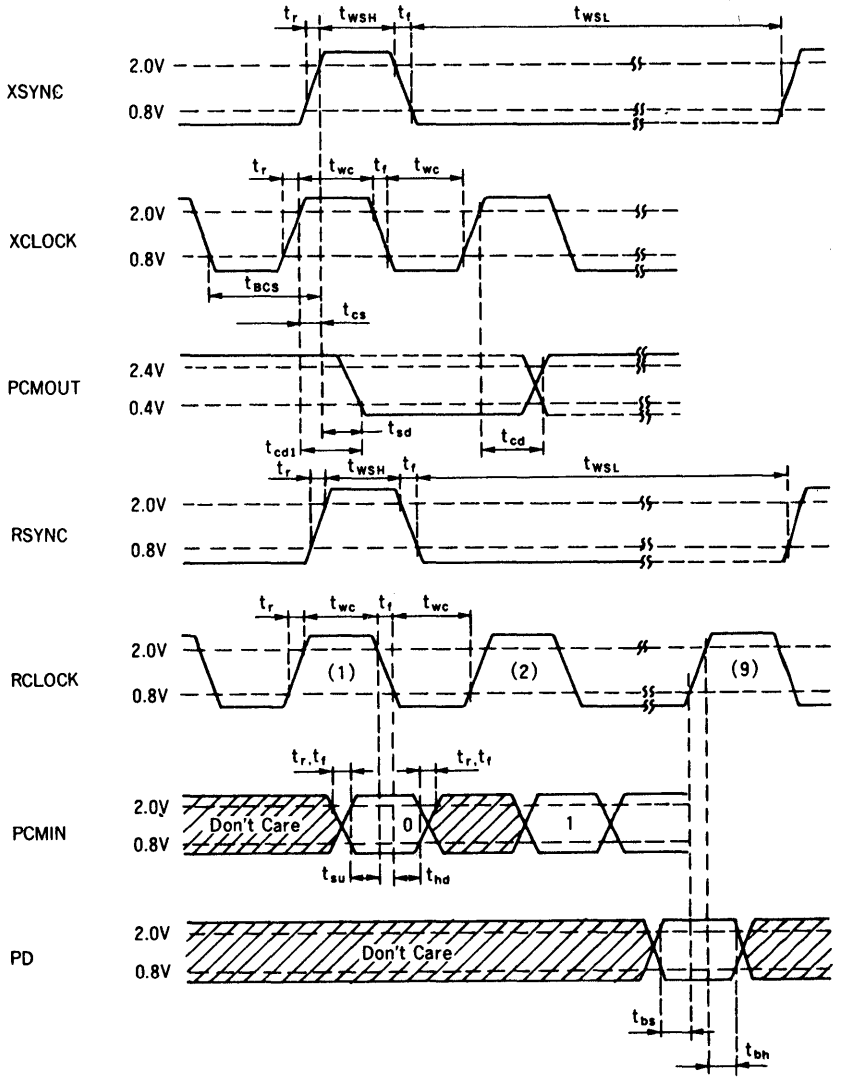
Symbol	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Dist.	1020 Hz tone	–45 dBm0	25			dB	c-wgt
	(A to A)		–40	30			dB	
			–30 to +3	35			dB	
SDX	Signal to Dist.	1020Hz tone	–45 dBm0	26			dB	c-wgt
	(A to D)		–40	31			dB	
			–30 to +3	36			dB	
SDR	Signal to Dist.	1020 Hz tone	–45 dBm0	26			dB	c-wgt
	(D to A)		–40	31			dB	
			–30 to +3	36			dB	
GTA	Gain Tracking	1020 Hz tone	–55 to –50 dBm0	–1.0		1.0	dB	
	(A to A)	Relative to	–50 to –40	–0.5		0.5	dB	
		10 dBm0	–40 to +3	–0.3		0.3	dB	
GTX	Gain Tracking	1020 Hz tone	–55 to –50	–0.8		0.8	dB	
	(A to D)	Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
GTR	Gain Tracking	1020 Hz tone	–55 to –50	–0.8		0.8	dB	
	(D to A)	Relative to	–50 to –40	–0.4		0.4	dB	
		–10 dBm0	–40 to +3 dBm0	–0.2		0.2	dB	
FRX	Freq.Response	Relative to	0.06 kHz	24			dB	
	(A to D) (Loss)	1020 Hz	0.2	0		2.0	dB	
		0 dBm0	0.3 to 3	–0.15		0.15	dB	
			3.18	–0.15		0.65	dB	
			3.4	0		0.8	dB	
			3.78	6.5			dB	
FRR	Freq.Response	Relative to	0 to 3 kHz	–0.15		0.15	dB	
	(D to A) (Loss)	1020 Hz	3.18	–0.15		0.65	dB	
		0 dBm0	3.4	0		0.8	dB	
			3.78	6.5			dB	
AIL	Analog Input	1020 Hz	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
	Level	0 dBm0						
AOL	Analog Output	1020 Hz	25°C nom. P.S.	1.213	1.227	1.241	Vrms	
	Level	0 dBm0						
ICNA	Idle Ch. Noise	A to A	AIN = AGND			16	dBmC0	
ICNX	Idle Ch. Noise	A to D	AIN = AGND			16	dBmC0	
ICNR	Idle Ch. Noise	D to A	PCMIN = +0 - Code			10	dBmC0	
XTKA	AIN to AOUT Crosstalk	1020Hz 0 dBm0				–65	dB	
XTKD	PCMIN to PCMOUT	1020 Hz 0 dBm0				–65	dB	

For HD44247P, HD44248P

Symbol	Descriptions	Test Conditions		Min	Typ	Max	Unit	Note
AT	AIL, AOL Variation with temp.	Relative to 25°C nominal P.S.			±20		ppm/°C	
AP	AIL,AOL Variation with P.S.	25°C, Supplies ± 5%			± 0.01		dB	
ALS	Gain Variation over Temp. P.S.	A to D D to A	Initial	–0.2		0.2	dB	Note 1)
AIP	Peak Analog Input			3.0			V	
AOP	Peak Analog Output			2.5			V	
PDL	Propagation Delay	A to A	0 dBm0		450	480	µs	
DD	Delay Distortion	A to A 0 dBm0	0.5 to 0.6 kHz			1.4	ms	
			0.6 to 1.0			0.7		rel. to min. delay
			1.0 to 2.6			0.2		
			2.6 to 2.8			1.4		
PSRR	PSRR	A to A AIN = AGND 0.3 – 50 kHz	V_{DD} Mod. = +5 V + 100 mVop	30			dB	
			Vss Mod. = –5 V + 100 mVop	30				
IM1	Intermodulation	A to A(2a-b) a; 0.47 kHz, –4 dBm0 b; 0.32, –4				–38	dB	
IM2	Intermodulation	A to A(a-b) a; 1.02 kHz, –4 dBm0 b; 0.05, –23				–52	dB	
ICS	Single Freq.Noise	A to A AIN = AGND	8,16,24, 32,40 kHz			–50	dBm0	
DIS	Discrimination	A to A 0 dBm0	4.6 to 200 kHz	30			dB	

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 to +70°C, V_{DD}/Vss = ± 5 V ± 5%)

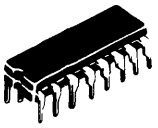
Timing Chart



HD44270P/CP Series

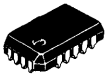
Single Chip CODEC/Filter Combo LSI (Plastic Versions)

HD44271P HD44272P



(DP-16A)

HD44271CP HD44272CP



(CP-18)

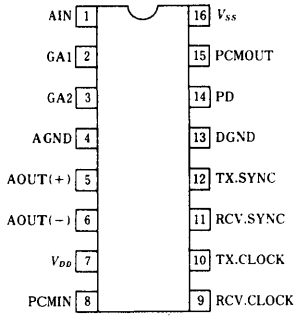
■FEATURES

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package and 18-pins PLCC package.
- Power Supply Voltage ±5V±5%, Low Power Dissipation.
- Follows μ-Law (HD44272P) or A-Law (HD44271P).
- Extremely Low Cost for the Digital PBX Terminal or Digital Handset Application.
- Internal Clock Generator.
- Anti-Aliasing Filter (2nd order CR Active Filter).
- Voltage Reference (Internal-Trimmed).
- Input Amplifier with Uncommitted Plus/Minus Terminals.
- Auto-Zero Cancel Circuit without External Component.
- Push/Pull Analog Output.

Type	Original Versions	Comp. Law	Power (Typ.)	Clock			Input Amp	Output Amp	
				Internal clock	Sync Async Operation	PCM bit clock rate		Type	Min load
HD44271P	HD44247C	A	70mW	PLL Included	Both	64-2048kHz	Fully Uncommited Op-amp	Push-Pull	600Ω
HD44272P	HD44248C	μ	70mW						
HD44273P	HD44233C	A	50mW	Divider Included		1536 1544 2048 kHz		Single Ended	
HD44274P	HD44234C	μ	50mW						
HD44277P	HD44237C	A	50mW	PLL Included		64-2048kHz			
HD44278P	HD44238C	μ	50mW						

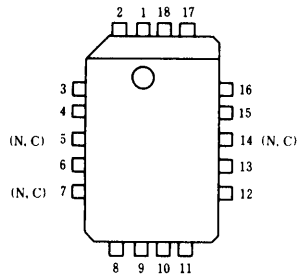
■ PIN ARRANGEMENT

● HD44271P/272P



(Top View)

● HD44271CP/272CP



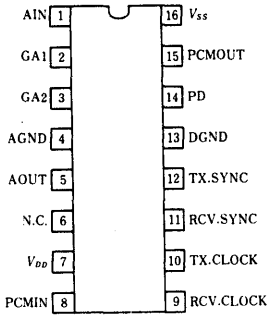
(Top View)

■ PIN DESCRIPTIONS

No. P	No. CP	Symbol	Function	Remarks
1	1	AIN	Analog input	
2	2	GAI	Gain adjust 1	Feed-back input
3	3	GA2	Gain adjust 2	10kΩ < R_L, C_L < 100pF
4	4	AGND	Analog ground	
5	6	AOUT(+)	Analog output	R_L > 600Ω, C_L < 100pF
6	7	AOUT(−)		R_L > 600Ω, C_L < 100pF
7	8	V_{DD}	Positive pow. sup.	5V ± 5%
8	9	PCMIN	PCM data input	(TTL)
9	10	RCV. CLK	PCM bit clock	(TTL) 64kHz to 2048kHz
10	11	TX. CLK		
11	12	RCV. SYNC	Synchronization	(TTL) 8kHz
12	13	TX. SYNC		
13	15	DGND	Digital ground	
14	16	PD	Power down	(TTL) "0" = down
15	17	PCMOUT	PCM data output	Open drain
16	18	V_{SS}	Negative pow. sup.	−5V ± 5%
—	5, 14	N.C.	—	Open

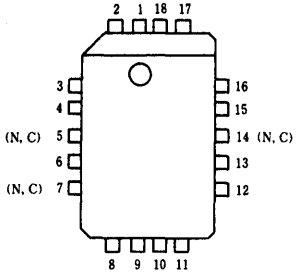
■PIN ARRANGEMENT

● HD44273P/274P



(Top View)

● HD44273CP/274CP

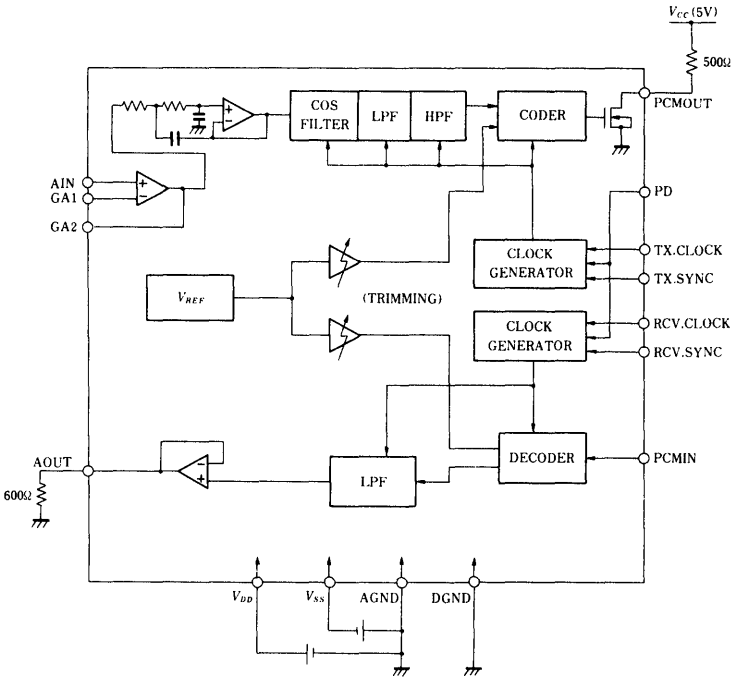


(Top View)

■PIN DESCRIPTIONS

No.		Symbol	Function	Remarks
P	CP			
1	1	AIN	Analog input	
2	2	GA1	Gain adjust 1	Feed-back input
3	3	GA2	Gain adjust 2	10kΩ < R_L C_L < 100pF
4	4	AGND	Analog ground	
5	6	AOUT	Analog output	R_L > 600Ω, C_L < 100pF
7	8	V_{DD}	Positive pow. sup.	5V ± 5%
8	9	PCMIN	PCM data imput	(TTL)
9	10	RCV. CLK	PCM bit clock	(TTL) 2048/1544/ 1536kHz
10	11	TX. CLK		
11	12	RCV. SYNC	Synchronization	(TTL) 8kHz
12	13	TX. SYNC		
13	15	DGND	Digital ground	
14	16	PD	Power down	(TTL) "0" = down
15	17	PCMOUT	PCM data output	Open drain
16	18	V_{SS}	Negative pow. sup.	−5V ± 5%
6	5, 7, 14	N.C.	—	Open

■BLOCK DIAGRAM



*ONLY FOR HD44271, 272P/CP

■PIN/FUNCTION DESCRIPTIONS

HD44271P/CP, HD44272P/CP, HD44277P/CP, HD44278P/CP

Pin	No		Descriptions
	P	CP	
TX. CLOCK RCV. CLOCK	9 10	10 11	Any of 64kHz to 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	12 13	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK 'RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	17	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK 'RCV.CLOCK signal following a positive edge on the SYNC, TX 'SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT(+)	5	6	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.
V_{DD} V_{SS} AGND DGND	7 16 4 13	8 18 4 15	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	16	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
AOUT(−)*	6	7	This is the inverted output of pin 5 signal output to drive the 600 Ω transformer as the push-pull operation. $R_L < 600\Omega$, $C_L < 100$pF.

*ONLY FOR HD44271, 272P/CP

■PIN/FUNCTION DESCRIPTIONS

HD44273P/CP, HD44274P/CP

Pin	No P	No CP	Descriptions
TX. CLOCK RCV. CLOCK	9 10	10 11	One of 1.536, 1.544 and 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC/RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	12 13	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	17	This is a LS-TTL compatible open-drain output. It is active only during transmisson of PCM output for 8 bit periods of CLOCK. TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC. TX/SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	9	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT	5	6	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.
V_{DD} V_{SS} AGND DGND	7 16 4 13	8 18 4 15	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	16	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.

■ABSOLUTE MAXIMUM RATINGS

Item	Rating
V_{DD}	−0.3 to +7V
V_{SS}	+0.3 to −7V
Storage temperature	−55°C to +125°C
Power dissipation	0.5W
Digital input output voltage	$-0.3V < V_{IN} < V_{DD}+0.3V$
Analog input output voltage	$V_{SS}-0.3V < V_{IN} < V_{DD}+0.3V$

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

3

■ELECTRICAL CHARACTERISTICS

●STATIC CHARACTERISTICS ($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to $+70°C$)

Descriptions	Symbol	Pin	min	typ	max	Note/conditions	Unit
V_{DD} current (ope.)	I_{DD}	7	–	8.0	13.5	Note 1 AIN = 0V PCMIN = +0 code R_L (GA2) = 10kΩ R_L (AOUT) = 600Ω	mA
V_{SS} current (ope.)	I_{SS}	16	−13.0	−7.5	–		
V_{DD} current (st.by.)	I_{DDST}	7	–	0.4	1.0		
V_{SS} current (st.by.)	I_{SSST}	16	−0.2	–	–		
Leak current	I_L	1, 2, 8	−10.0	–	10.0	$V_M=0.8V$	μA
		9, 10	−10.0	–	10.0	$V_M=2.0V$	μA
		14	–	–	10.0	$V_{DD}=V_M=5.25V$	μA
Pull up current	I_{PL}	11, 12	−100	–	0		μA
Leak current	I_{OL}	15	–	–	10.0	$V_{DD}=V_M=5.25V$	μA
Analog input cap.	C_{AIN1}	1	–	–	10	at 1MHz Vbias = 0	pF
Analog input cap.	C_{AIN2}	2	–	–	10	at 1MHz Vbias = 0	pF
Input capacitance	C_{DIN}	8,9,10,11,12,14	–	–	10	at 1MHz Vbias = 0	pF
AOUT resistance	R_{OUTA}	5, 6	–	1	20		Ω
GA2 resistance	R_{OUTG}	3	–	–	50	Note 1	Ω
GA2 output swing	V_{GSW}	3	−3.0	–	3.0	$R_L=10k\Omega$	V
Analog offset input	V_{OFFIN}	1	−200	–	200	Note 1	mV
GA2 offset output	V_{OFFG}	3	−50	–	50	Note 1	mV
AOUT offset output	V_{OFFA}	5, 6	−100	–	100	PCMIN = +0−code	mV
PCMOUT capacitance	C_{DOUT}	15	–	–	15.0	at 1MHz, Vbias = 0V	pF
PCMOUT low voltage	V_{OL}	15	–	–	0.4	$R_L=500\Omega$, $+I_{OL}=0.8mA$	V
PCMOUT high voltage	V_{OH}	15	$V_{CC}-0.3$	–	–	$I_{OH}=-150\mu A$	V
Digital input high voltage	V_{IH}	8,9,10,11,12,14	2.0	–	–		V
Digital input low voltage	V_{IL}	8,9,10,11,12,14	–	–	0.8		V

Note 1) Analog input amplifier gain = 0 dB (GA1 is connected to GA2)

( ): Only for HD44271, 272P/CP

●DYNAMIC-CHARACTERISTICS (V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C)

Descriptions	Symbol	Note	min	typ	max	Unit
Synchronization rate	F_S		–	8	–	kHz
PCM bit clock rate	F_C		64	–	2048	kHz
Clock pulse width	t_{wc}		200	–	–	ns
Sync pulse high width	t_{wSH}		200	–	–	ns
Sync pulse low width	t_{wSL}		8	–	–	ns
Logic input rise time	t_r		5	–	50	ns
Logic input fall time	t_f		5	–	50	ns
Previous clock to Sync delay	t_{hCS}	Note 1	40	–	–	ns
Clock to sync delay	t_{cs}	Note 1, 3	–	–	100	ns
Clock to PCM MSB delay	t_{cdd}	Note 1, 2, 4	–	–	170	ns
Sync to PCM MSB delay	t_{sd}	Note 1, 2, 4	–	–	170	ns
Clock to PCM OUT delay	t_{cd}	Note 1, 2, 5	–	–	180	ns
PCMIN setup time	t_{su}	Note 1	65	–	–	ns
PCMIN hold time	t_{hd}	Note 1	120	–	–	ns

Note 1) t_r, t_f of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT load condition: 500Ω + 165pF + two LS-TTL Equivalent (I_{OL} = 0.8mA, I_{OH} = −150μA) Threshold level (V_{OH} = 2.4V, V_{OL} = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) t_{cdd}, t_{sd} are specified by CLOCK or SYNC which has slower rise time.
5) t_{cd} specification is valid for the data except MSB.

●SYSTEM RELATED CHARACTERISTICS

(V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C, INPUT AMPLIFIER GAIN = 0dB, ANALOG OUT PUT = AOUT(−), GA2 LOAD = 10kΩ, AOUT LOAD = 600Ω, Synchronous operation. F_C (PCM BIT CLOCK) = 2048kHz)

A-law (HD44271P/CP, HD44273P/CP, HD44277P/CP)

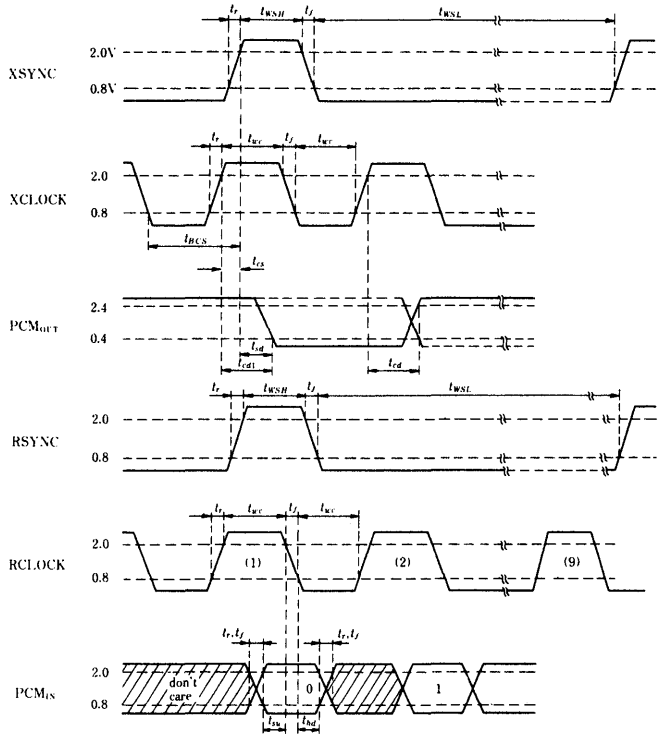
Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	820Hz tone	−45dBm0	23	–	–	dB	p-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain track. (A to A)	GTA	820Hz tone Relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq. response. (A to D)(Loss)	FRX	Relative to 820Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq. response.(D to A)(Loss)	FRR	Relative to 820Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level variation	AIL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN +0−Code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0dBm0	–	–	−65	dB	
PCMIN to PCMOUT	XTKD	820Hz	0dBm0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0 dBm 0	–	–	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	820Hz	0 dBm 0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

μ-law (HD44272P/CP, HD44274P/CP, HD44278P/CP)

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	1020Hz tone	−45dBm0	23	–	–	dB	c-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain Tracking(A to A)	GTA	1020Hz tone relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq.Response.(A to D)(Loss)	FRX	Relative to 1020Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq.Response.(D to A)(Loss)	FRR	Relative to 1020Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level	AIL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	16	dBrnC0	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	–	–	10	dBrnC0	
AIN to AOUT crosstalk	XTKA	1020Hz 0dBm0		–	–	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	1020Hz 0dBm0		–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

■TIMING CHART



HD81019/020

Terminal CODEC For Digital Telephones

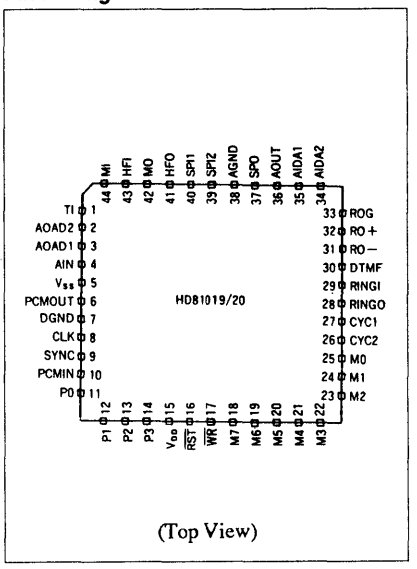
Description

HD81019/20 is a single chip CODEC specified for digital telephone. This LSI contains the function of CODEC with filters (corresponding to HD44270P series) and also includes analog input/output for Hands Free, input pin for DTMF signal, moreover Tone Ringer circuit and analog Gain Control circuit. All controls are available by microcomputer interface.

Features

- Single chip CMOS CODEC for digital telephone
  HD81019 : A-law
  HD81020 : μ-law
- Power Supply Voltage: ±5 V±5%, Low power dissipation: 300 mW max.
- Analog input/output for hand set/hands free
- Gain control for analog signals
- Ringing signal generator
  1, 2 and 3 tone are available.
  One of rectangle, steps and envelope wave is selectable.
- Input amplifier for addition of DTMF signal
- Microcomputer interface (8 bits parallel inputs)
- QFP (Quad flat package) 44 pin package

Pin Arrangement



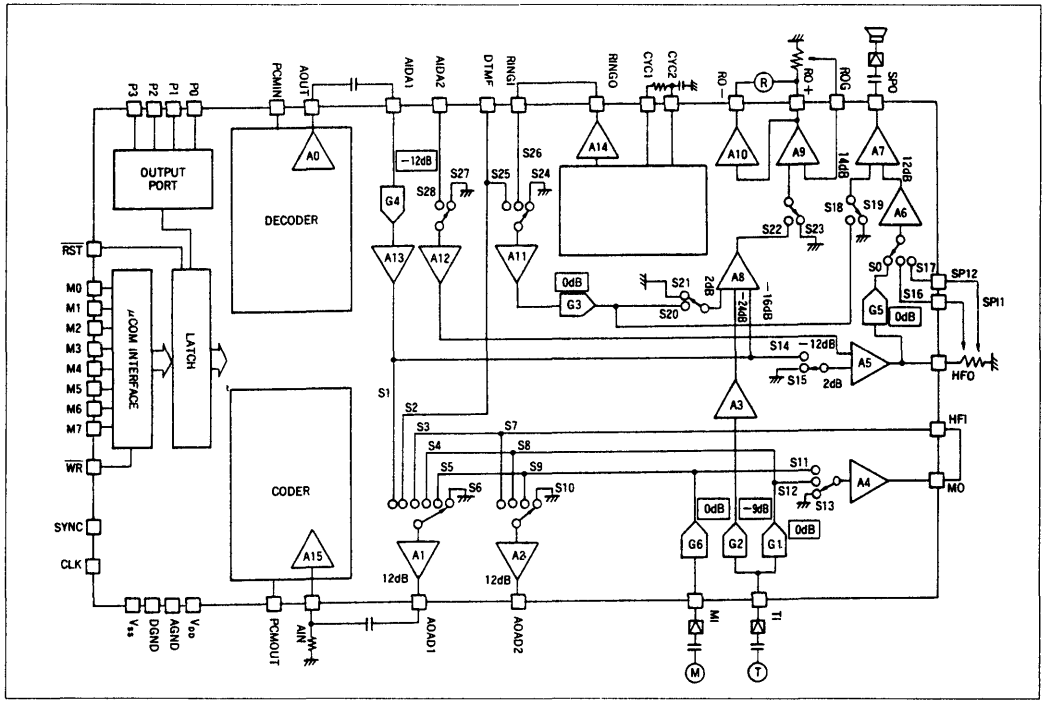
(Top View)

3

Pin Descriptions

Pin No.	Symbol	Power & clock	Analog I/O		Digital		Function
			Input	Output	Input	Output	
1	TI		O				Transmitter Input
2	AOAD2			O			Analog Output to A/D 2
3	AOAD1			O			Analog Output to A/D 1
4	AIN		O				Analog Input To A/D Part
5	Vss	O					Negative Power Supply (–5 V±5%)
6	PCMOUT					O	PCM Output : Open Drain
7	DGND	O					Digital Ground
8	CLK	O			O		PCM Shift Clock (64–2048kHz)
9	SYNC	O			O		Frame SYNC (8 kHz) With Pull-Up
10	PCMIN				O		PCM Input
11	P0					O	Output Port 0
12	P1					O	Output Port 1
13	P2					O	Output Port 2
14	P3					O	Output Port 3
15	V_{DD}	O					Positive Power Supply (+5 V±5%)
16	$\overline{RST}$				O		Reset
17	$\overline{WR}$				O		Write
18	M7				O		Data Bus 7
19	M6				O		Data Bus 6
20	M5				O		Data Bus 5
21	M4				O		Data Bus 4
22	M3				O		Data Bus 3
23	M2				O		Data Bus 2
24	M1				O		Data Bus 1
25	M0				O		Data Bus 0
26	CYC2		O	O			Cycle Freq. Adjust 2
27	CYC1			O			Cycle Freq. Adjust 1
28	RINGO			O			Ringing Signal Output
29	RINGI		O				Ringing Signal Input
30	DTMF		O				DTMF Signal Input
31	RO–			O			Receiver Output –
32	RO+			O			Receiver Output +
33	ROG		O				Receiver Gain Control
34	AIDA2		O				Analog Input From D/A 2
35	AIDA1		O				Analog Input From D/A 1
36	AOUT			O			Analog Output From D/A Part
37	SPO			O			Speaker Output
38	AGND	O					Analog Ground
39	SPI2		O				Speaker Input 2
40	SPI1		O				Speaker Input 1
41	HFO			O			Hands Free Output
42	MO			O			Microphone Output
43	HFI		O				Hands Free Input
44	MI		O				Microphone Input

Block Diagram



Descriptions for Function

Block Diagram of special CODEC LSI for digital telephone is shown in Fig. 2. The descriptions for function in each block are as follows.

CODEC Part

CODEC core is corresponding to HD44277P (A-law) and HD44278P (μ-law) for HD81019 and HD81020 respectively.

For a sampling rate of 8 kHz, PCM input/output data rate can be selected from 64 kHz to 2048 kHz in synchronous operation. Internal PLL circuit generates the internal clock from the 8kHz synchronization clock.

Analog Signal Input

Analog input for transmission (TI and MI pins)

Two analog input pins are provided for transmission. One is MI pin input from microphone and the other is TI pin input from Transmitter.

The input signal from Transmitter is transfered to following four lines after Gain Control.

1. AMP A4 : The line to output to external treatment for echo cancellation
2. AMP A1 : The line to output to CODEC part (A to D side) directly
3. AMP A2 : The line to output to external CODEC (A to D side) directly
4. AMP A8 : The line to output side tone to Receiver (the output of analog addition)

And input signal from microphone is transfered to following three lines.

1. AMP A4 : The line to output to external treatment for echo cancellation
2. AMP A1 : The line to output to CODEC part (A to D side) directly
3. AMP A2 : The line to output to external CODEC (A to D side) directly

Echo cancellation input (HFI pin)

The input signal from Microphone or Transmitter is output by AMP A4, and input to HFI pin after external treatment for echo cancellation.

And analog input signal from HFI pin is transfered to following two lines.

1. AMP A1 : The line to output to CODEC part (A to D side) directly
2. AMP A2 : The line to output to external CODEC (A to D side) directly

Analog Inputs for Receiving Signals (AIDA1 and AIDA2 pins)

Two amplifiers are prepared for receiving analog signals.

One (AIDA1) is to input receiving analog signal from CODEC part (D to A side). The other is to input analog signal from external CODEC (D to A side). Analog input signal from CODEC part is transfered to following three lines after Gain Control.

1. AMP A1 : The line for analog loopback
2. AMP A5 : The line for output to Speaker
3. AMP A8 : The line for output to Receiver

DTMF signal input (DTMF pin)

It's a input pin for DTMF signal. DTMF signal is transfered to two lines. One is to output to CODEC part directly, the other is to input to AMP A11. The output of AMP A11 is transfered to following two directions after Gain Control.

1. AMP A7 : DTMF Signal output line to Speaker (the output of analog addition)
2. AMP A8 : The line to output DTMF signal to Receiver (the output of analog addition)

Ringing signal input (RINGI pin)

It's to input Ringing signal.

AMP A11 : Amplifier for Ringing signal Input
The output of AMP A11 is transfered to AMP A7 or A8 after Gain Control.

1. AMP A7 : The line to output Ringing signal to Speaker (the output of analog addition)
2. AMP A8 : The line to output Ringing signal to Receiver (the output of analog addition)

Input pin to output speech signal to Loud Speaker (SPI pin)

External speech signal is input at this pin and output to Loud Speaker.

AMP A6 : Input amplifier to output speech signal to Loud Speaker

Analog Signal Output

Output pin 1 for transmission signal (AOAD1 pin)

It's a output pin to output analog signal to CODEC part (A to D side) directly.

AMP A1 : Amplifier for selection of analog signal

The output from this amplifier is one of following four.

1. AMP A13 : Signal for analog loopback (via Gain Control)
2. Transmitter Input Signal or one via external treatment for echo cancellation (via Gain Control)
3. DTMF signal
4. Microphone Input Signal or one via external treatment for echo cancellation (via Gain Control)

Output pin 2 for transmission signal (AOAD2 pin)

It's a output pin to output analog signal to external CODEC (A to D side) directly.

AMP A2 : Amplifier for selection of analog signals

The output from this amplifier is one of followings.

1. Input signal from Transmitter or one via external treatment for echo cancellation (via Gain Control)
2. Input signal from Microphone or one via external treatment for echo cancellation (via Gain Control)

Output pin for Receiving analog signal to Speaker

On Hands Free mode, it's a output pin to output the signal once to external. The signal becomes input to Loud Speaker.

AMP A5 : the amplifier to select or add analog signals

The signal from this amplifier is one of followings or addition of them.

1. Analog signal from CODEC part (via Gain Control)
2. Analog signal from external CODEC

Output pin to Loud Speaker (SPO pin)

It's a output pin to Loud Speaker.

AMP A7 : the amplifier to select or add analog signals

The output of this amplifier is the selection or the addition of followings.

1. AMP A6 :Speech signal output to Loud Speaker
2. AMP A1 : Ringing or DTMF signal (via Gain Control)

Output pins to Receiver (RO+ and RO– pins)

They are output pins to Receiver.

AMP A8 : the amplifier to select or add analog signals

AMP A9 : the amplifier for Gain Control by external resistors

AMP A10 : The amplifier to invert the output of AMP A9

The outputs of these amplifiers are the selection or the addition of followings.

1. Side Tone of Transmitter input signal (via Gain Control)

2. AMP A11 : Ringing Signal or DTMF Signal (via Gain Control)
3. Receiving speech signal from CODEC part (via Gain Control)

Output pin to Microphone (MO pin)

AMP A4 : Output amplifier for external treatment for echo cancellation

The output from this amplifier is one of followings.

1. The input from Microphone (via Gain Control)
2. The input from Transmitter (via Gain Control)

Ringing Signal Generator

Tone

Ringing Tone is selected one of 1 tone, 2 tone, 3 tone and no output by the signal from microcomputer interface.

M7	M6	M5	M4	M3	M2	M1	M0		
0	1	1	1	*	*	T1	T0	Output	Note
0	1	1	1	*	*	0	0	No Output	output becomes GND level
						0	1	1 Tone	the waveform with freq. F1 is output
						1	0	2 Tone	the waveforms with freq. F1 and F2 are output alternately :Note 1
						1	1	3 Tone	the waveforms with freq. F1, F2 and F3 are output in sequence :Note 1

Note 1: The period of warble is determined by external CR.

Example; 2 Tone: F1 → F2 → F1 → F2 → ···
3 Tone: F1 → F2 → F3 → F1 → F2 → F3 → ···

Frequency

F1 is selected one of sixteen frequencys by 4 bits (R13–R10) optionally.
F2 is selected one of sixteen frequencys by 4 bits (R23–R20) optionally.
F3 is selected one of sixteen frequencys by 4 bits (R33–R30) optionally.

M7	M6	M5	M4	M3	M2	M1	M0	Hex	(μs)	(Hz)
1	1	0	0	0	0	0	0	0	0	0
	(F1)			0	0	0	1	1	250	4000
	OR			0	0	1	0	2	500	2000
1	1	0	1	0	0	1	1	3	750	1333.3
	(F2)			0	1	0	0	4	1000	1000
	OR			0	1	0	1	5	1250	800
1	1	1	0	0	1	1	0	6	1500	666.7
	(F3)			0	1	1	1	7	1750	571.4
				1	0	0	0	8	2000	500
				1	0	0	1	9	2250	444.4
				1	0	1	0	A	2500	400
				1	0	1	1	B	2750	363.6
				1	1	0	0	C	3000	333.3
				1	1	0	1	D	3250	307.7
				1	1	1	0	E	3500	285.7
				1	1	1	1	F	3750	266.7

Waveform

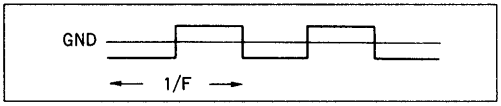
Waveform is selected one of rectangle, steps and envelope wave.

rectangle/steps wave (ENV = "0" on this mode)

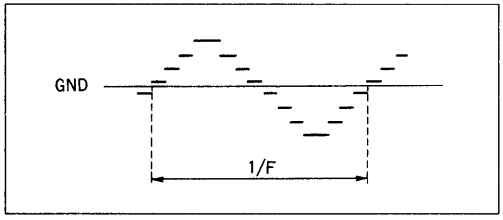
M7	M6	M5	M4	M3	M2	M1	M0
0	1	1	1	Mute	PL/LD	*	*

PL/LD : "0" = rectangle wave, "1" = steps wave

rectangle wave : the pulse with 50% duty



steps wave : 16 steps per period with 8 amplitudes



Envelope

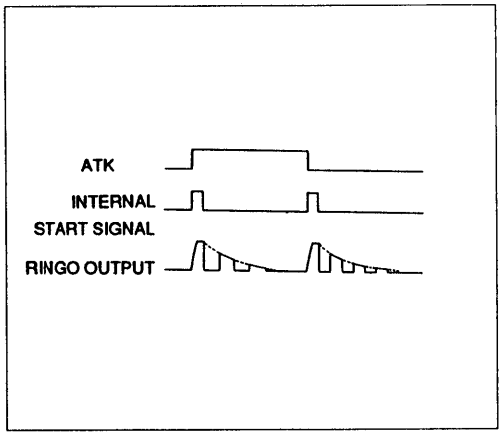
M7	M6	M5	M4	M3	M2	M1	M0
0	1	0	1	*	*	ENV	ATK

ENV : "0" = rectangle or steps wave, "1" = envelope

Note: the setting of ENV = "1" is prior to the one of rectangle/steps. ENV = "0" should be set on rectangle/steps mode.

ATK : When ATK is changed as 0→1 or 1→0, internal start signal for envelope is generated.

Example:

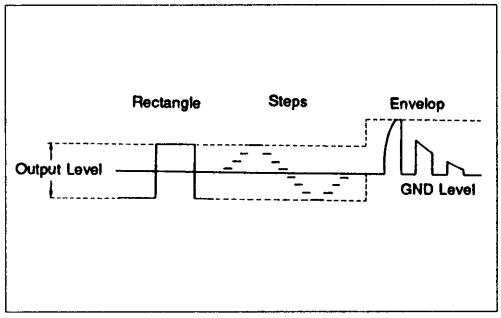


The time constant for envelope is defined by external C,R.

On 2 or 3 tone mode the change of frequencys is done by internal start signal.

Output Level (RINGO Output)

Output level is fixed to –24 dBV (0.063 Vrms) on steps wave.



Output Port

Four output ports (P0 to P3) are provided to control external amplifiers and etc.. Each port is controlled by the signal from 8 bit microcomputer interface.

M7	M6	M5	M4	M3	M2	M1	M0
0	1	1	0	P3	P2	P1	P0

Bit	"1"	"0"
P3	Port3 High	Port3 Low
P2	Port2 High	Port2 Low
P1	Port1 High	Port1 Low
P0	Port0 High	Port0 Low

Microcomputer Interface

Various kinds of control commands on data bus (M0 to M7) are latched by $\overline{WR}$, and following states are set.

1. states of various analog switches
2. Gain Control level for lines
3. output level for output ports
4. Ringing signal

And each switch and Gain Control is initialized by input low level at $\overline{RST}$ pin. Initial value is shown in the later pages on microcomputer interface command.

Others

Power down

There are two methods for power down.

stopping SYNC pulse

By this method only CODEC part puts into power down mode.

And the function of Ringing is stopped.

The strobes can be high, low or floating, but as long as it is static, the powered down mode is in effect.

by the command from microcomputer interface

M7	M6	M5	M4	M3	M2	M1	M0
0	1	0	0	*	*	*	PD

PD = "1" : Power Down
PD = "0" : Normal

By this method all parts except microcomputer interface put into power down mode. The contents in command latches aren't changed.

Mute

By Mute command, following analog outputs are kept GND level.

After release the Mute command, all states come back to previous.

The contents in command latches aren't changed.

M7	M6	M5	M4	M3	M2	M1	M0
0	1	1	1	Mute	*	*	*

Mute : "0" = Normal
"1" = Mute

On Mute mode, switches as S6, S10, S13, S15, S19, S23, S27 are put on, consequently following analog outputs become GND level.

AOAD1, AOAD2, MO, HFO, SPO, RO+, RO–, RINGO

3

Microcomputer Interface Command

Microcomputer Interface (Command List)

MSB							LSB	Note
M7	M6	M5	M4	M3	M2	M1	M0	
0	0	0	0	*	*	*	*	NOP
0	0	0	1	G41	G40	G11	G10	Gain Control:G4,G1
0	0	1	0	G22	G21	G20	*	Gain Control:G2
0	0	1	1	G32	G31	G30	*	Gain Control:G3
0	1	0	0	G52	G51	G50	PD	Gain Control:G5, PWR DWN
0	1	0	1	G61	G60	ENV	ATK	Gain Control:G6, Envelop
0	1	1	0	P3	P2	P1	P0	Port Signal
0	1	1	1	Mute	PL/LD	T1	T0	Ringing Control
1	0	0	0	A12	A11	A10	27/28	Switch Control 1
1	0	0	1	A21	A20	A41	A40	Switch Control 2
1	0	1	0	A111	A110	21/20	19/18	Switch Control 3
1	0	1	1	23/22	15/14	A61	A60	Switch Control 4
1	1	0	0	R13	R12	R11	R10	Ringing Tone 1
1	1	0	1	R23	R22	R21	R20	Ringing Tone 2
1	1	1	0	R33	R32	R31	R30	Ringing Tone 3
1	1	1	1	*	*	*	*	NOP

Gain Control

[ ] Initial

G1

0	0	0	1	*	*	G11	G10

M7	M6	M5	M4	M3	M2	M1	M0	Gain (dB)
0	0	0	1	*	*	0	0	[0]
				*	*	0	1	–3
				*	*	1	0	–6
				*	*	1	1	–9

G4

0	0	0	1	G41	G40	*	*

M7	M6	M5	M4	M3	M2	M1	M0	Gain (dB)
0	0	0	1	0	0	*	*	–6
				0	1	*	*	[–12]
				1	0	*	*	–15
				1	1	*	*	–∞

G2

0	0	1	0	G22	G21	G20	*

M7	M6	M5	M4	M3	M2	M1	M0	Gain (dB)
0	0	1	0	0	0	0	*	0
				0	0	1	*	–3
				0	1	0	*	–6
				0	1	1	*	[–9]
				1	0	0	*	–12
				1	0	1	*	–15
				1	1	0	*	–18
				1	1	1	*	–∞

G3	0	0	1	1	G32	G31	G30	*

M7	M6	M5	M4	M3	M2	M1	M0	Gain (dB)
0	0	1	1	0	0	0	*	0
				0	0	1	*	–6
				0	1	0	*	–12
				0	1	1	*	–18
				1	0	0	*	–24
				1	0	1	*	–30
				1	1	0	*	–36
				1	1	1	*	–42

G5	0	1	0	0	G52	G51	G50	*

M7	M6	M5	M4	M3	M2	M1	M0	Gain (dB)
0	1	0	0	0	0	0	*	0
				0	0	1	*	–6
				0	1	0	*	–12
				0	1	1	*	–18
				1	0	0	*	–24
				1	0	1	*	–30
				1	1	0	*	–36
				1	1	1	*	–∞

G6	0	1	0	1	G61	G60	*	*

M7	M6	M5	M4	M3	M2	M1	M0	Gain (dB)
0	1	0	1	0	0	*	*	0
				0	1	*	*	–3
				1	0	*	*	–6
				1	1	*	*	–9

Analog signal line setting function

Controlling analog switches (S1 to S28) allows the following lines to be set:

- Receive signal line (with handset).
- Transmit signal line (with handset).
- Side tone adjusting line.
- Receive signal line (with hands free).
- Transmit signal line (with hands free).
- Ringing signal output line (to loud speaker).
- Ringing signal output line (to receiver).
- Analog loopback line.
- Second transmission/receiving line.
- Loud speaker output line.

The analog switch control commands are given below.

Switch Control

☐ Initial

Switch Control 1	1	0	0	0	A12	A11	A10	*	
	7	6	5	4	3	2	1	0	SW
	1	0	0	0	0	0	0	*	☐ SW6 ON
					0	0	1	*	SW6 ON
					0	1	0	*	SW6 ON
					0	1	1	*	SW5 ON
					1	0	0	*	SW4 ON
					1	0	1	*	SW3 ON
					1	1	0	*	SW2 ON
					1	1	1	*	SW1 ON
	1	0	0	0	*	*	*	27/28	
	7	6	5	4	3	2	1	0	SW
	1	0	0	0	*	*	*	0	☐ SW27 ON
					*	*	*	1	SW28 ON
Switch Control 2	1	0	0	1	A21	A20	*	*	
	7	6	5	4	3	2	1	0	SW
	1	0	0	1	0	0	*	*	☐ SW10 ON
					0	1	*	*	SW9 ON
					1	0	*	*	SW8 ON
					1	1	*	*	SW7 ON
	1	0	0	1	*	*	A41	A40	
	7	6	5	4	3	2	1	0	SW
	1	0	0	1	*	*	0	0	☐ SW13 ON
					*	*	0	1	SW13 ON
					*	*	1	0	SW12 ON
					*	*	1	1	SW11 ON

Switch Control 3	1	0	1	0	A111	A110	*	*	
	7	6	5	4	3	2	1	0	SW
	1	0	1	0	0	0	*	*	SW24 ON
					0	1	*	*	SW24 ON
					1	0	*	*	SW25 ON
					1	1	*	*	SW26 ON
	1	0	1	0	*	*	21/20	19/18	
	7	6	5	4	3	2	1	0	SW
	1	0	1	0	*	*	0	*	SW21 ON
					*	*	1	*	SW20 ON
	7	6	5	4	3	2	1	0	SW
	1	0	1	0	*	*	*	0	SW19 ON
					*	*	*	1	SW18 ON
Switch Control 4	1	0	1	1	23/22	15/14	A61	A60	
	7	6	5	4	3	2	1	0	SW
	1	0	1	1	0	*	*	*	SW23 ON
					1	*	*	*	SW22 ON
	7	6	5	4	3	2	1	0	SW
	1	0	1	1	*	0	*	*	SW15 ON
					*	1	*	*	SW14 ON
	7	6	5	4	3	2	1	0	SW
	1	0	1	1	*	*	0	0	SW0 ON
					*	*	0	1	SW0 ON
					*	*	1	0	SW16 ON
					*	*	1	1	SW17 ON

Port Signal

M7	M6	M5	M4	M3	M2	M1	M0
0	1	1	0	P3	P2	P1	P0

Bit	"1"	"0"
P3	Port 3 High	Port 3 Low
P2	Port 2 High	Port 2 Low
P1	Port 1 High	Port 1 Low
P0	Port 0 High	Port 0 Low

Ringing Control

M7	M6	M5	M4	M3	M2	M1	M0
0	1	1	1	Mute	PL/LD	T1	T0

MUTE: "1" = MUTE, "0" = NORMAL
PL/LD: "1" = STEPS WAVE, "0" = RECTANGLE WAVE

T1	T0	Tone
0	0	No Output
0	1	1 Tone
1	0	2 Tone
1	1	3 Tone

M7	M6	M5	M4	M3	M2	M1	M0	Hex	(μs)	(Hz)
1	1	0	0	0	0	0	0	0	0	0
	(F1)			0	0	0	1	1	250	4000
	OR			0	0	1	0	2	500	2000
1	1	0	1	0	0	1	1	3	750	1333.3
	(F2)			0	1	0	0	4	1000	1000
	OR			0	1	0	1	5	1250	800
1	1	1	0	0	1	1	0	6	1500	666.7
	(F3)			0	1	1	1	7	1750	571.4
				1	0	0	0	8	2000	500
				1	0	0	1	9	2250	444.4
				1	0	1	0	A	2500	400
				1	0	1	1	B	2750	363.6
				1	1	0	0	C	3000	333.3
				1	1	0	1	D	3250	307.7
				1	1	1	0	E	3500	285.7
				1	1	1	1	F	3750	266.7

Pin/Function Descriptions

Pin No.	Symbol	Descriptions
8	CLK	Any of 64 kHz to 2048 kHz clock can be accepted with the pin. And it is automatically divided down to provide the internal clocks. This TTL compatible input shifts PCM data out of the coder on the positive going edge and PCM data into the decoder on the negative going edge after receiving a positive edge on the SYNC.
9	SYNC	This TTL compatible pulse input (typ.8 kHz) is used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK with this positive going edge occurring after the falling edge of the CLOCK. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output and input.
6	PCMOUT	This is a LS-TTL compatible open drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK signal following a positive edge on the SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
10	PCMIN	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK.
4	AIN	It is the input of analog signal in the range of $-V_{REF}$ to $+V_{REF}$ (–2.5 to 2.5V).
36	AOUT	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100 pF.
15 5 38 7	V_{DD} V_{SS} AGND DGND	These are power supply pins. V_{DD} and Vss are positive and negative supply pins respectively (+5 V,–5 V). Analog and digital ground pins are separated for minimizing crosstalk.
11–14	P0–P3	These pins are output ports for control of externally connected amplifiers. They are 4 ports, P0 to P4. Each ports are controlled by the signal from microcomputer interface.
16	$\overline{RST}$	Command latches in microcomputer interface are initialized by input of Low level. Consequently internal switches, Gain Control and Ringing part are initialized. This pin is TTL level input.
25–18	M0–M7	These are 8 bit parallel input for microcomputer interface, and TTL level input. Upper 4 bits show commands and lower 4 bits show data.
17	$\overline{WR}$	This is Write signal for M0–M7, 8 bit parallel input. The data of M0–M7 are latched at rising edge of WR. It is TTL level input.

Pin/Function Descriptions

Pin No.	Symbol	Descriptions
3	AOAD1	This is analog signal output pin (No.1) for transmit. This output signal is input to CODEC part (A to D side). As output signal 1) Analog Loopback Signal 2) Transmitter Input Signal or one that is output from M0 after Gain Control and input from HFI after echo cancellation externally. 3) DTMF Signal 4) Microphone input signal or one that is output from M0 after Gain Control and input from HFI after echo cancellation externally. one of four is output.
2	AOAD2	This is analog signal output pin (No.2) for transmit. This output signal is normally input to external CODEC (A to D side of external CODEC). As output signal, either above mentioned 2) or 4) is output.
41	HFO	It's output of analog received signal for Hands Free. One of analog signal from CODEC part and from external CODEC, or addition of them is output.
37	SPO	It's output pin to Loud Speaker. One of the signal from CODEC part, external CODEC, ringing signal and DTMF signal is selected, or addition of these is output.
1	TI	It's input pin for Transmitter Signal.
44	MI	It's input pin for Microphone Signal.
43	HFI	Input signal from Transmitter or Microphone is output to MO pin after gain control, and it is input from HFI after external echo cancellation.
35	AIDA1	It's input pin for analog signal from CODEC part.
34	AIDA2	It's input pin for analog signal from external CODEC.
40 39	SPI1 SPI2	These are input pins to control the gain of analog receive signal (HFO output) for Hands Free.
42	MO	This is output pin of Microphone or transmitter input after Gain Control.
32 31	RO+ RO–	Receiver output pin (double end)
33	ROG	Gain Control pin for Receiver output
30	DTMF	DTMF Signal input pin
28	RINGO	Ringing Signal output pin

Pin/Function Descriptions

Pin No.	Symbol	Descriptions
29	RINGI	Input pin for Ringing Signal This pin is used to input from RINGO directly or to input from external Ringer.
27 26	CYC1 CYC2	External C, R is attached at these pins to define warble frequency on 2 tone or 3 tone mode. And on envelope mode external C, R is attached at these pins for envelope's time constant.

Electrical Characteristics

Absolute Maximum Ratings

Note1, Note2

Item	Symbol	Rating	Unit
Positive Power Supply	V_{DD}	–0.3—+7	V
Negative Power Supply	Vss	–7—+0.3	V
Digital Input/Output Voltage	Vd	$-0.3<Vd<V_{DD}+0.3$	V
Analog Input/Output Voltage	Va	$Vss-0.3<Va<V_{DD}+0.3$	V
Power Dissipation	Pd	500	mW
Operation temperature	Topr	0—+70	°C
Storage Temperature	Tstg	–55—+125	°C

Notes 1 : All voltage is based on both AGND (analog ground) and DGND (digital ground).
2 : This rating is also applied on power-on and power-off.

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Static Characteristics (V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, Vcc = 5 ± 0.25 V, Ta = 0to+70°C)

Symbol	Pin No.	Item	Min	Typ	Max	Unit	Condition & Note
I_{DD}	15	V_{DD} Current		18.0	28.0	mA	AIN = 0V
Iss	5	Vss Current	–28.0	–18.0			PCMIN = +0 code
I_{DDST}	15	V_{DD} Current PD		2.0	5.0		R_L(AOUT) = 600Ω
		(Standby) SYNC					
Issst	5	Vss Current PD	–2.0	–0.2			
		(Standby) SYNC	–23.0	–13.0			
I_L	All Input	Input Leak Current	–10.0		10.0	μA	V_M = 0.8 V
	Except 9		–10.0		10.0		V_M = 2.0 V
					10.0		V_{DD} = V_M = 5.25 V
I_{PL}	9	Pull Up Current	–100		0	μA	
I_{DL}	6, 11–14	Digital Output			10.0	μA	V_{DD} = V_M = 5.25 V
		Leak Current					
C_{AIN}	4	Analog Input Cap.			10	pF	@ 1MHz, Vbias = 0 V
C_{DIN}	8–10	Digital Input Cap.			10	pF	
	16–25						
V_{OFFIN}	4	Analog Offset Input	–200		200	mV	
V_{OFFO}	36	Analog Offset Output	–100		100	mV	PCMIN = +0 code
C_{DOUT}	6, 11–14	Digital Output Cap.			15.0	pF	@ 1 MHz, Vbias = 0 V
V_{OL1}	6	PCM Output			0.4	V	R_L = 500Ω
		Low Voltage					+ I_{OL} = 0.8 mA
V_{OH1}	6	PCM Output	Vcc-			V	I_{OH} = –150 μA
		High Voltage	0.3				
V_{OL2}	11–14	Digital Output			0.4	V	+I_{OL} = 0.8 mA
		Low Voltage					
V_{OH2}	11–14	Digital Output	2.4			V	I_{OH} = –200μA
		High Voltage	V_{DD}-1.2			V	I_{OH} = -20μA
V_{IL}	8–10	Digital Input			0.8	V	
	16–25	Low Voltage					
V_{IH}	8–10	Digital Input	2.0			V	
	16–25	High Voltage					

Dynamic Characteristics (V_{DD} = 5 ± 0.25 V, V_{SS} = −5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0 to +70°C)

Symbol	Item	Min	Typ	Max	Unit	Note
Fs	SYNC Frequency	7.99	8.00	8.01	kHz	
Fc	PCM Bit Clock Rate	64		2048	kHz	
twc	Clock Pulse Width	200			ns	
twsh	SYNC Pulse High Width	200			ns	
twsl	SYNC Pulse Low Width	8			µs	
tr	Logic Input Rise Time	5		50	ns	
tf	Logic Input Fall Time	5		50	ns	
tbcs	Previous Clock To SYNC Delay	40			ns	Note 1
tcs	Clock to SYNC Delay			100	ns	Note 1,3
tcd1	Clock to PCM MSB Delay			170	ns	Note 1,2,4
tsd	SYNC to PCM MSB Delay			170	ns	Note 1,2,4
tcd	Clock to PCMOUT Delay			180	ns	Note 1,2,5
tsu	PCMIN Setup Time	65			ns	Note 1
thd	PCMIN Hold Time	120			ns	Note 1
tMSP	M0–M7 Setup Time	50			ns	
tMHD	M0–M7 Hold Time	10			ns	
tPOD	P0–P3 Data Delay			50	ns	
twRL	$\overline{WR}$ Low Width	100			ns	
twRH	$\overline{WR}$ High Width	100			ns	
tRSTL	RST Low Width	100			ns	

Note 1. tr, tf digital input or clock is assumed 5ns for timing measurement.

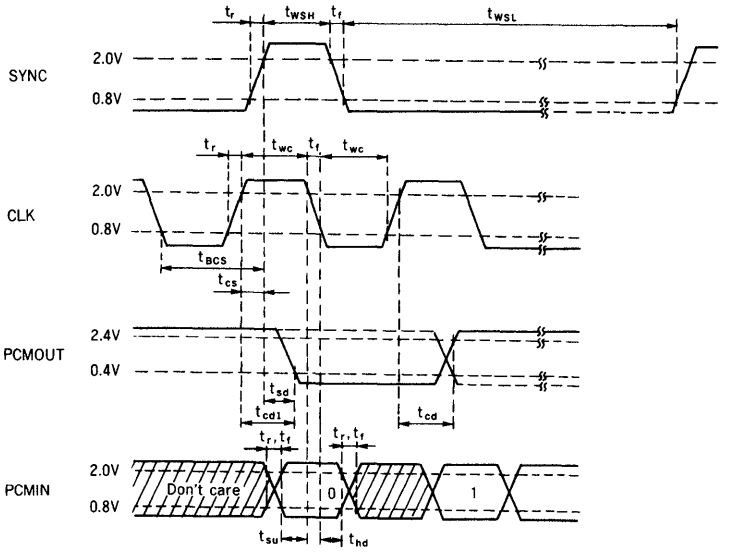
Note 2. PCMOUT Load Condition: 500 Ω + 165 pF + 2 LS – TTL Equivalent
(I_{IL} = 0.8 mA, I_{IH} = −150 µA, V_{OH} = 2.4 V, V_{OL} = 0.4 V)

Note 3. Positive value shows SYNC delay from CLOCK.

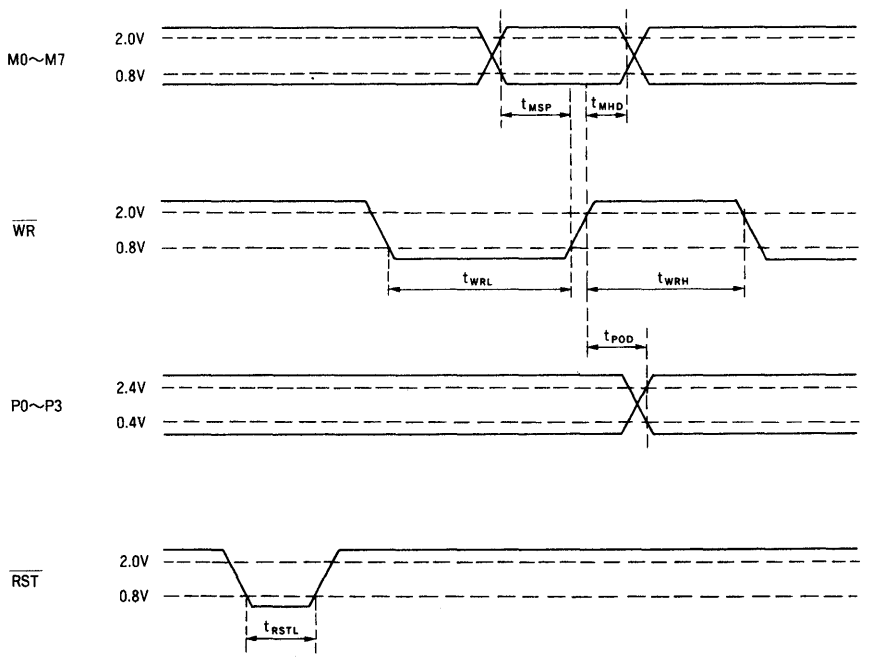
Note 4. tcd1, tsd are specified by CLOCK or SYNC which has slower rise time.

Note 5. tcd specification is valid for the data except MSB.

Timing Chart For CODEC Part



Microcomputer Interface Timing Chart



System Characteristics (HD81019 : A-law) (V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, Vcc = 5 ± 0.25 V, Ta = 0 to +70°C, Aout Load = 600 Ω, PCM Bit Clock Rate = 2048 kHz, AIN Input, Measure At A_{OUT})

Symbol	Items	Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Distortion Ratio (A–A)	820 Hz Tone	–45 dBm0	23			dB	P-wgt
			–40	28				
			–30, –20, –10, 0	34				
GTA	Gain Tracking Error (A–A)	820 Hz Tone Relative to –10 dBm0	–55 dBm0	–1.0		1.0	dB	
			–50	–0.5		0.5		
			–40, –30, –20, –10, 0, 3	–0.3		0.3		
FRX	Frequency Response (Loss) (A–D)	Relative to 820 Hz, 0dBm0 input	0.06 kHz	24			dB	
			0.2	0		2.5		
			0.3–3.0	–0.3		0.3		
			3.4	0		0.8		
			3.78	6.5				
FRR	Frequency Response (Loss) (D-A)	Relative to 820 Hz 0dBm0	0–3 kHz	–0.3		0.3	dB	
			3.4	0		0.8		
			3.78	6.5				
AIL	Analog Input Level (AIN)	820 Hz 0dBm0 input	Ta = 25°C Relative to 1.231Vrms	–0.6		0.6	dB	Power Supply: ±5 V ±5%
AOL	Analog Output Level (AOUT)	820 Hz 0dBm0 output	Ta = 25°C Relative to 1.231 Vrms	–0.6		0.6	dB	
ICNX	Idle Ch. Noise	A–D	AIN = AGND			–70	dBm	
ICNR	Idle Ch. Noise	D–A	PCMIN = +0 code			–75	–0P	
XTKA	Crosstalk (AIN-AOUT)	820 Hz	0dBm0 input			–65	dB	
XTKD	Crosstalk (PCMIN-PCMOUT)	820 Hz	0dBm0 input			–65	dB	
PSRR	PSRR	A-A AIN = AGND 0.3–50 kHz	Vdd Mod. = +5 V+100 mVop		30		dB	
			Vss Mod. = –5 V+100 mVop		30		dB	

3

System Characteristics (HD81020 : μ-law) (V_{DD} = 5 ± 0.25 V, V_{SS} = –5 ± 0.25 V, V_{CC} = 5 ± 0.25 V, Ta = 0 to +70°C, Aout Load = 600 Ω, PCM Bit Clock Rate = 2048 kHz, AIN Input, Measure At A_{OUT})

Symbol	Items	Conditions		Min	Typ	Max	Unit	Note
SDA	Signal to Distortion Ratio (A–A)	1020 Hz Tone	–45 dBm0	23			dB	C-wgt
			–40	28				
			–30, –20, –10, 0	34				
GTA	Gain Tracking Error (A-A)	1020 Hz Tone Relative to –10 dBm0	–55 dBm0	–1.0		1.0	dB	
			–50	–0.5		0.5		
			–40, –30, –20, –10, 0, 3	–0.3		0.3		
FRX	Frequency Response (Loss) (A–D)	Relative to 1020 Hz, 0dBm0 input	0.06 kHz	24			dB	
			0.2	0		2.5		
			0.3–3.0	–0.3		0.3		
			3.4	0		0.8		
			3.78	6.5				
FRR	Frequency Response (Loss) (D-A)	Relative to 1020 Hz 0dBm0	0–3 kHz	–0.3		0.3	dB	
			3.4	0		0.8		
			3.78	6.5				
AIL	Analog Input Level (AIN)	1020 Hz 0dBm0 input	Ta = 25°C Relative to 1.227Vrms	–0.6		0.6	dB	Power Supply: ±5 V ±5%
AOL	Analog Output Level (AOUT)	1020 Hz 0dBm0 output	Ta = 25°C Relative to 1.231 Vrms	–0.6		0.6	dB	
ICNX	Idle Ch. Noise	A–D	AIN = AGND			20	dBrn	
ICNR	Idle Ch. Noise	D–A	PCMIN = +0 code			15	–CO	
XTKA	Crosstalk (AIN-AOUT)	1020 Hz	0dBm0 input			–65	dB	
XTKD	Crosstalk (PCMIN-PCMOUT)	1020 Hz	0dBm0 input			–65	dB	
PSRR	PSRR	A-A AIN = AGND 0.3–50 kHz	Vdd Mod. = +5 V+100 mVop		30		dB	
			Vss Mod. = –5 V+100 mVop		30		dB	

HD81019 (A-law) : Input Frequency 820 Hz
HD81020 (μ-law) : Input Frequency 1020 Hz
(V_{DD} = 5 ± 0.25 V, Vss = –5 ± 0.25 V, Vcc = 5 ± 0.25 V, Ta = 0 to +70°C)

X: Setting Value

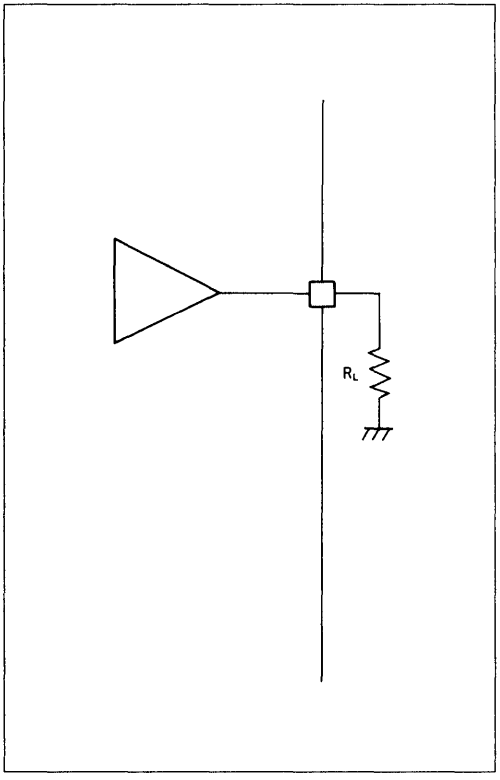
Symbol	Item	Input	Output	Conditions		Min.	Typ.	Max.	Unit	Note
G1	G1 Gain Accuracy	TI –12 dBV	AOAD1	S4 :On		X–1.5		X+1.5	dBV	
G2	G1 Gain Accuracy	TI 0dBV	R0+	S21, S22 :On		X–24 –1.5		X–24 +1.5	dBV	
G3	G1 Gain Accuracy	RINGI –14dBV	SPO	S18, S26 :On		X–3		X+3	dBV	
G4	G1 Gain Accuracy	AIDA1 12dBV	AOAD1	S1 :On	3dB step 6dB step	X–1.5 X–3		X+1.5 X+3	dBV dBV	
G5	G1 Gain Accuracy	AIDA2 0dBV	SPO	S0, S15, S19, S28 :On		X–3		X+3	dBV	
G6	G1 Gain Accuracy	MI –12dBV	AOAD1	S5 :On		X–1.5		X+1.5	dBV	
RF	Ringing FREQ Accuracy		RINGO			–27	–24	–21	dBV	Steps Wave

3

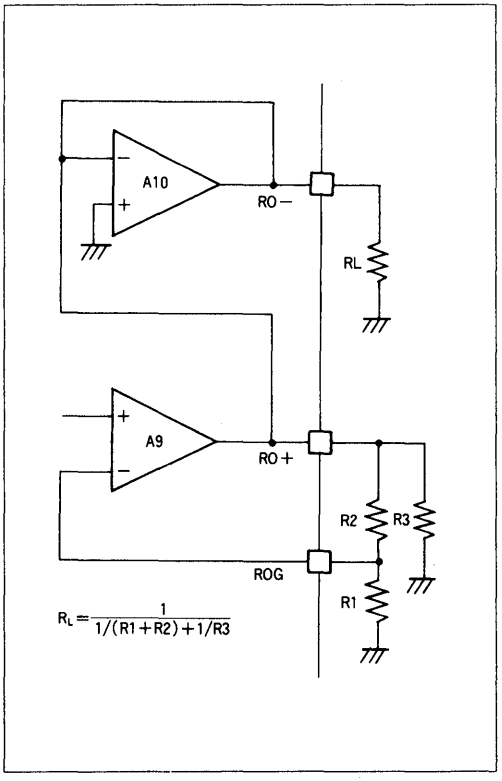
Output Amplifier Drivability

Pin Name	AMP	Condition		Max Output Level	Unit	Note
AOUT	A0		R_L = 600 Ω	4.95	dBV	(1)
AOAD1	A1		R_L = 10 kΩ	6.5	dBV	
AOAD2	A2		R_L = 10 kΩ	6.5	dBV	
MO	A4		R_L = 10 kΩ	–5.5	dBV	
HFO	A5		R_L = 10 kΩ	–5.5	dBV	(1)
SPO	A7		R_L = 10 kΩ	6.5	dBV	
RO+	A9	R1 = 1 kΩ	R_L = 600 Ω	4.95	dBV	(2)
		R2 = 17 kΩ	R_L = 150 Ω	–7.0	dBV	
RO–	A10		R_L = 600 Ω	4.95	dBV	
			R_L = 150 Ω	–7.0	dBV	
RING0	A14		R_L = 10 kΩ	–24	dBV	(1)

Note (1)



Note (2)



How to read a level diagram

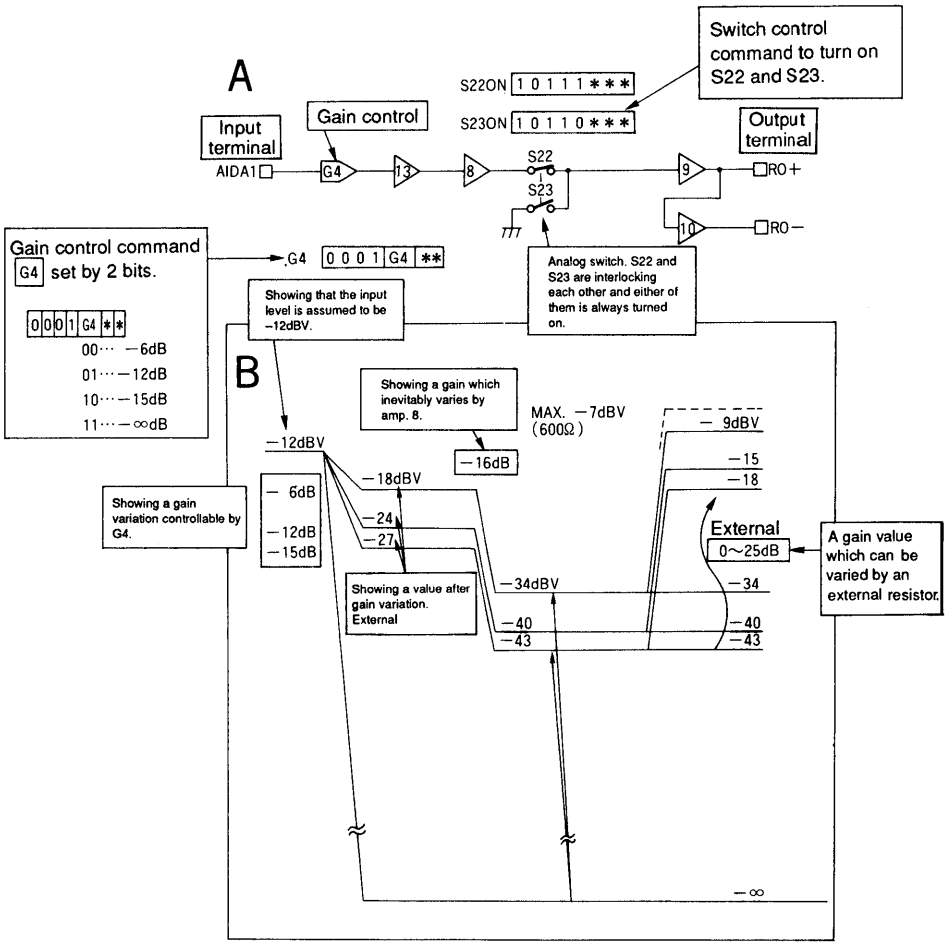
Ten examples of typical signal lines shown in "Microcomputer Interface Timing Chart" are given to show each level diagram.

1. Receive signal line (with handset).
2. Transmit signal line (with handset).
3. Side tone adjusting line.
4. Receive signal line (with hands free).
5. Transmit signal line (with hands free).
6. Ringing signal output line (to loud speaker).
7. Ringing signal output line (to receiver).
8. Analog loopback line.
9. Second transmission/receiving line.
10. Lout speaker output line.

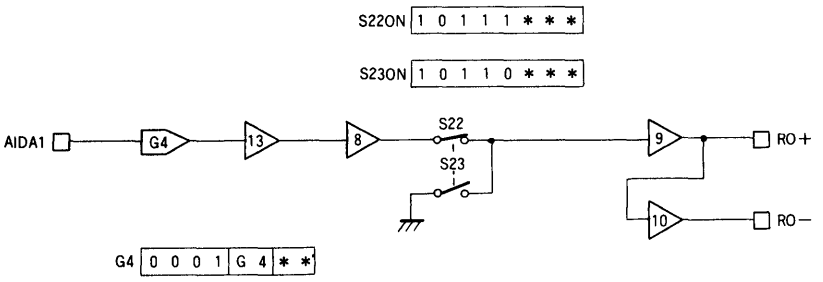
- Object lines are drawn out of the block diagram and shown below as A.
- The level diagram is shown as B in the form corresponding to block diagram A.
- For more information, see the remarks given below.

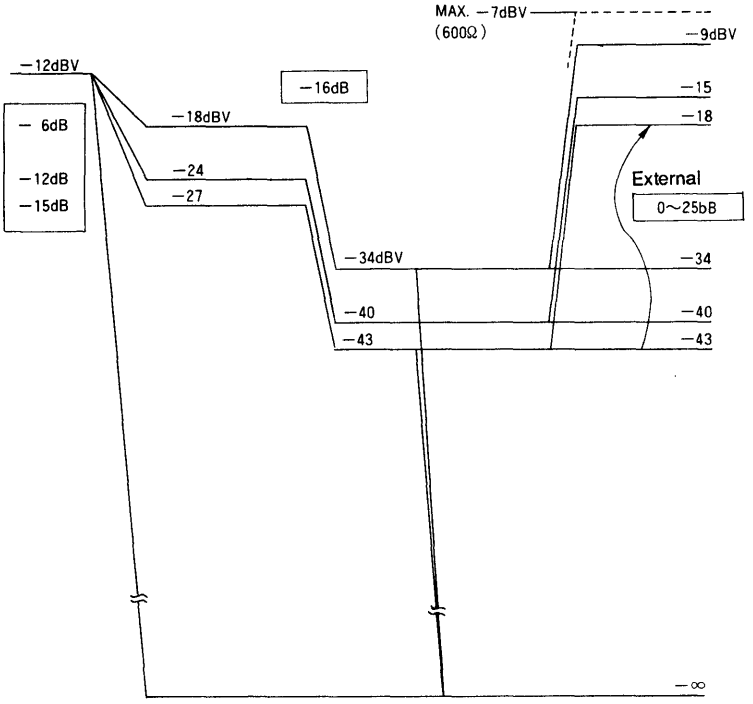
3

1. Receive Signal Line (with handset)

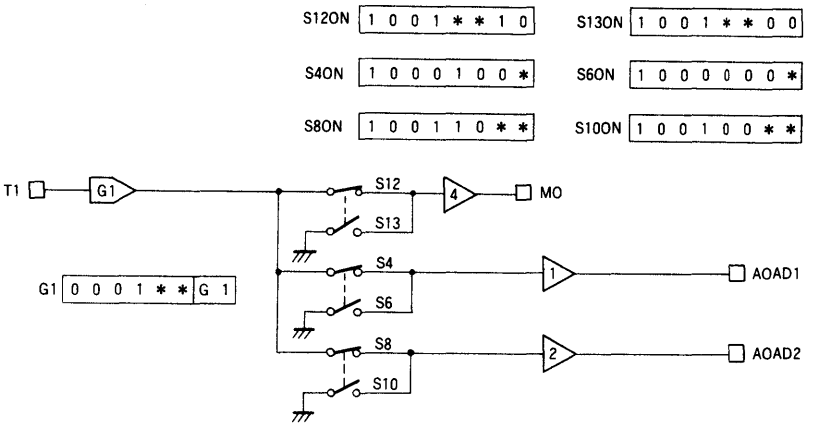


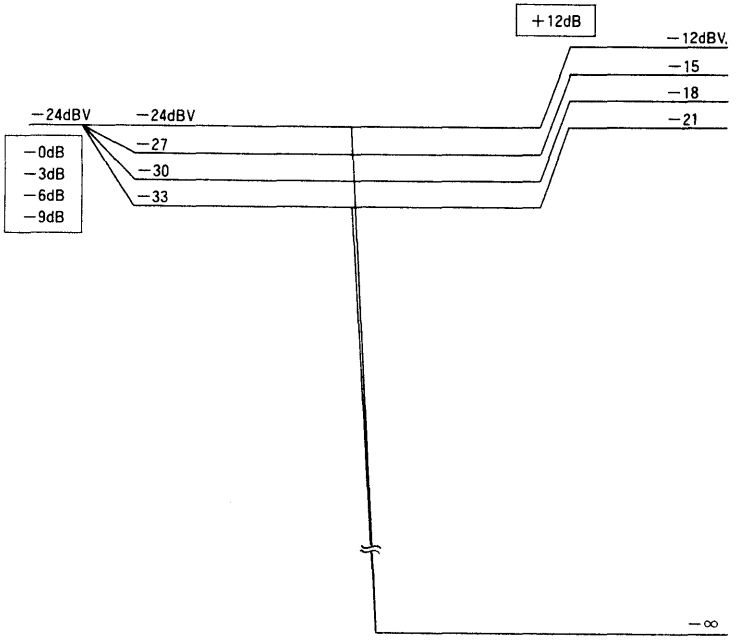
1. Receiving Signal Line (with handset)



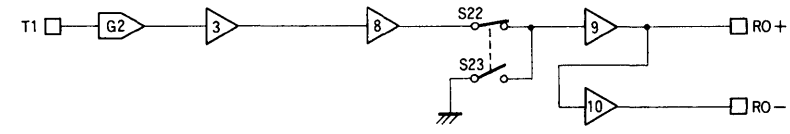


2. Transmit Signal Line (with handset)





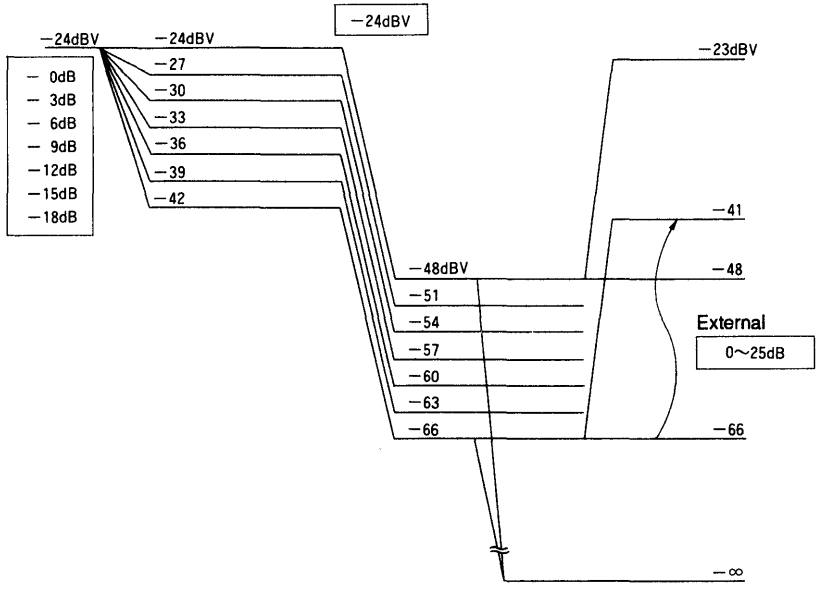
3. Side Tone Adjustment Line



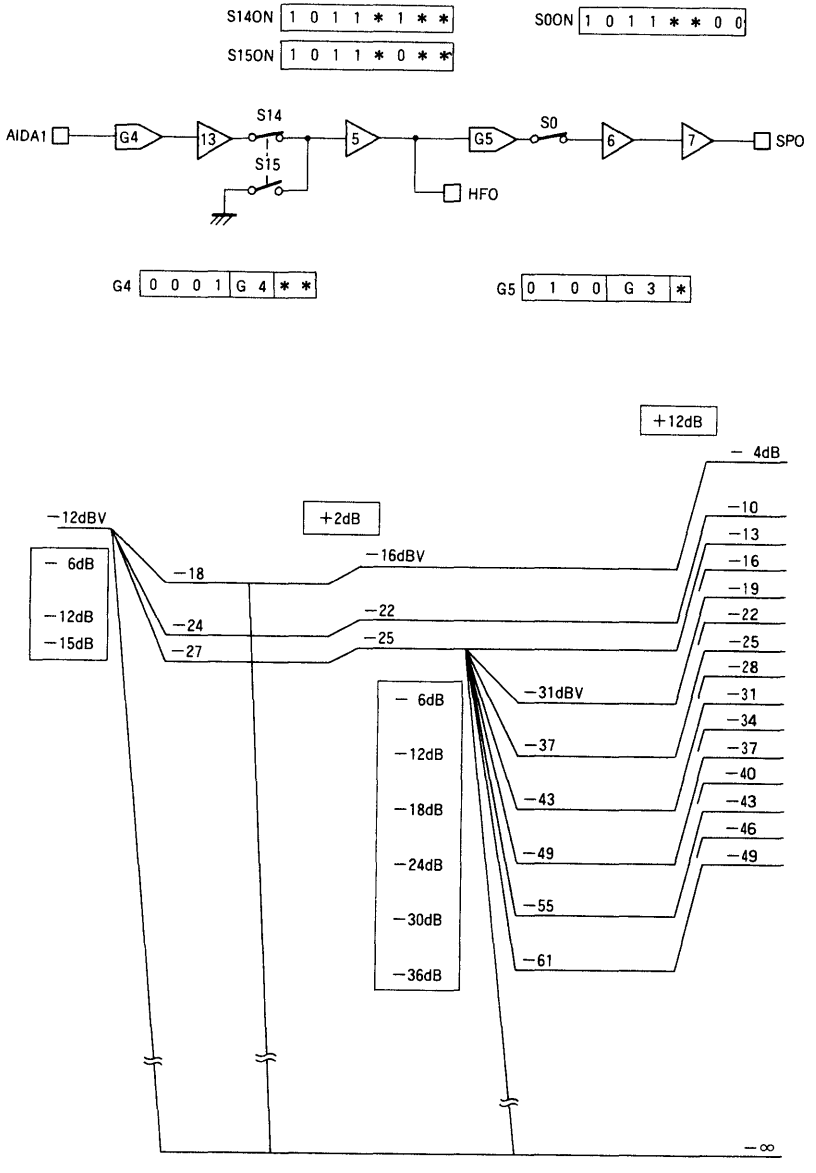
G2	0	0	1	0	G	2	*

S22ON	1	0	1	1	1	*	*	*

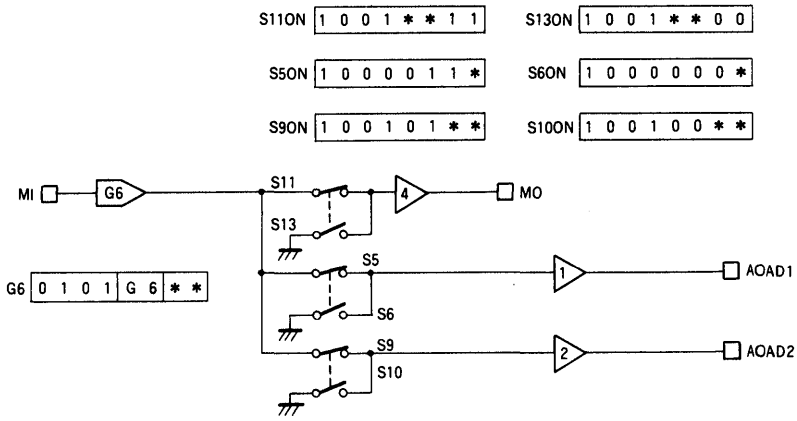
S23ON	1	0	1	1	0	*	*	*

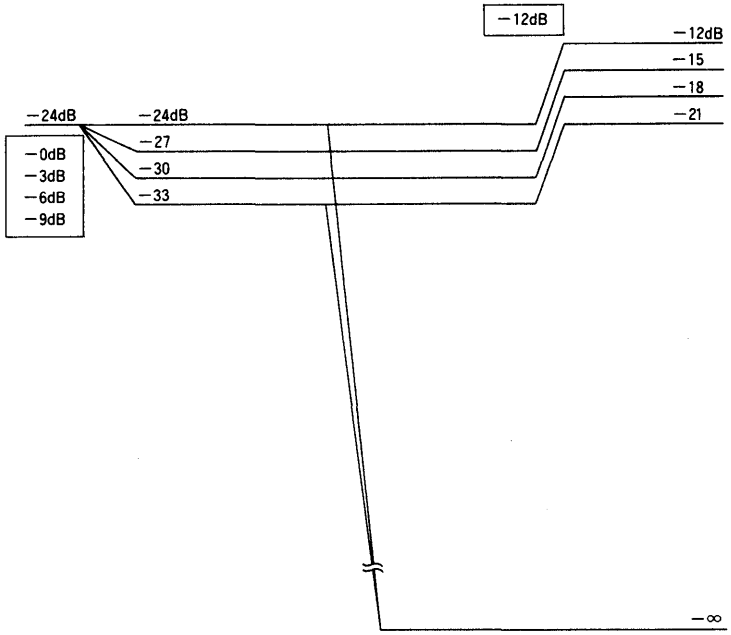


4. Receive Signal Line (with hands free)

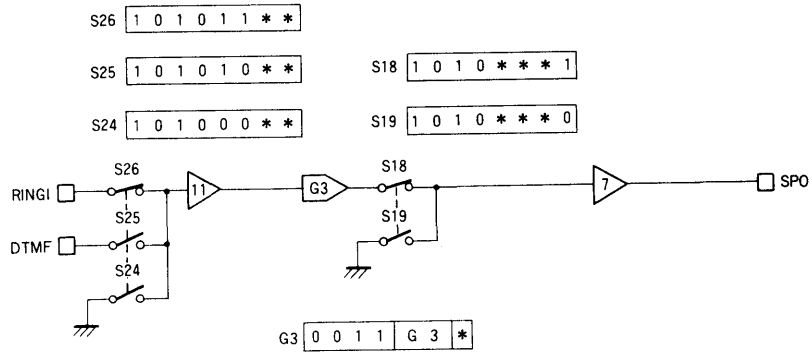


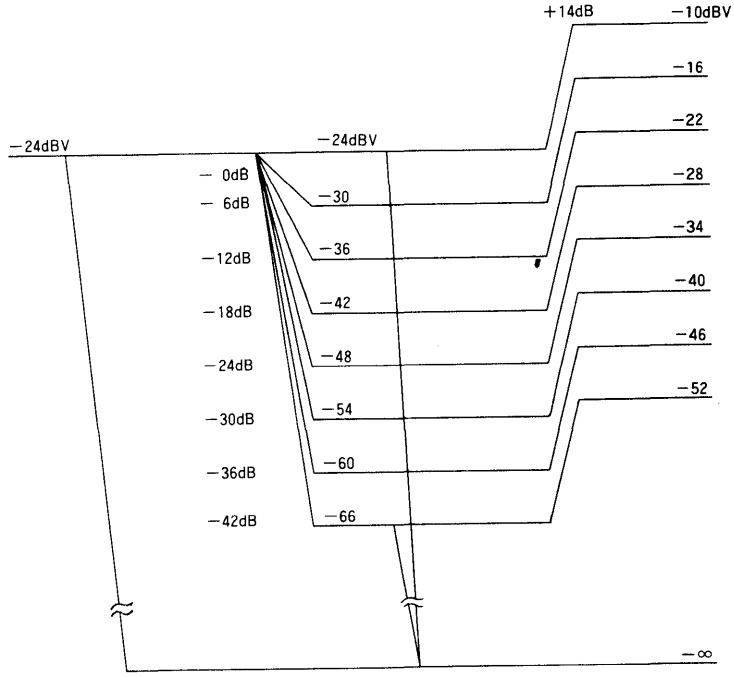
5. Transmit Signal Line (with hands free)



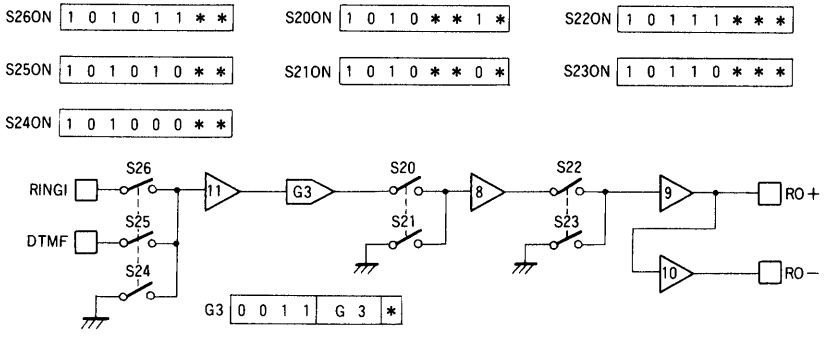


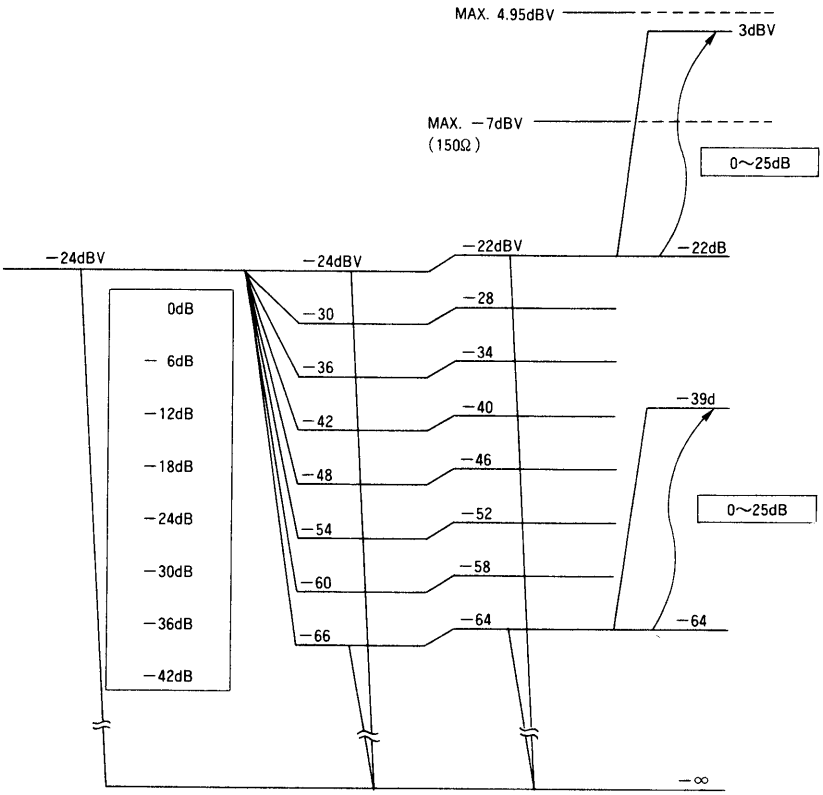
6. Ringing Signal Output Line (to loud speaker)



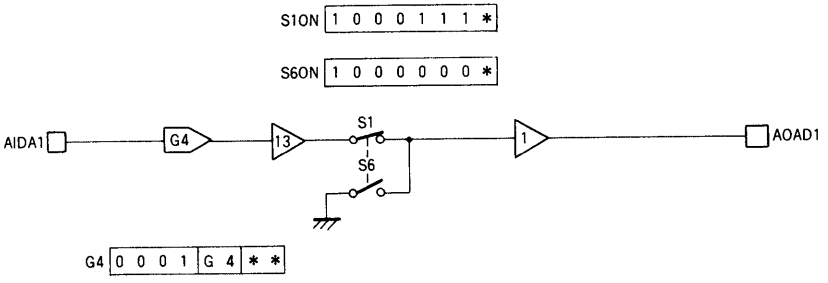


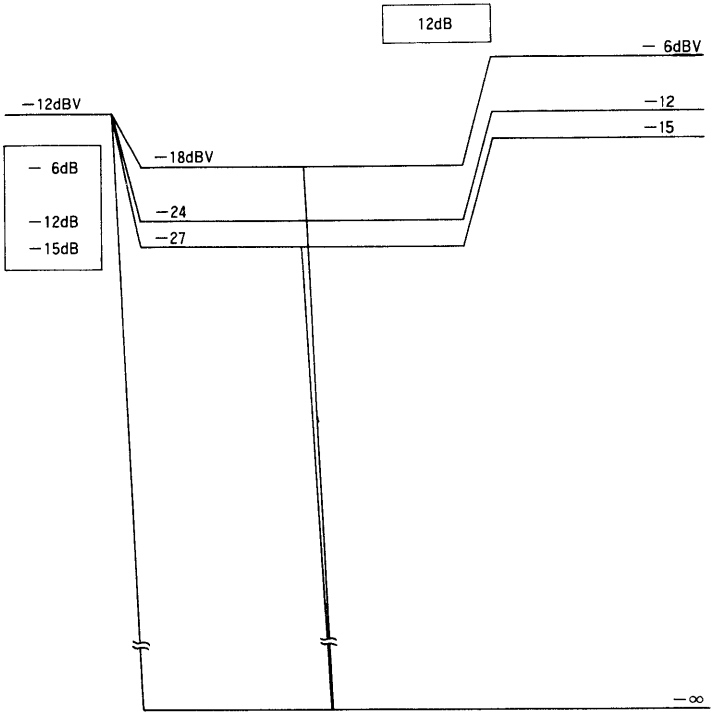
7. Ringing Signal Output Line (to receiver)





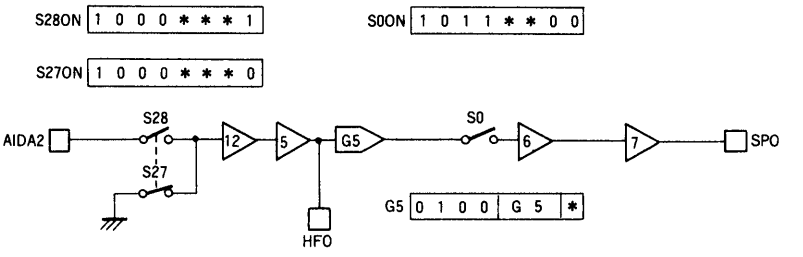
8. Analog Loopback Line

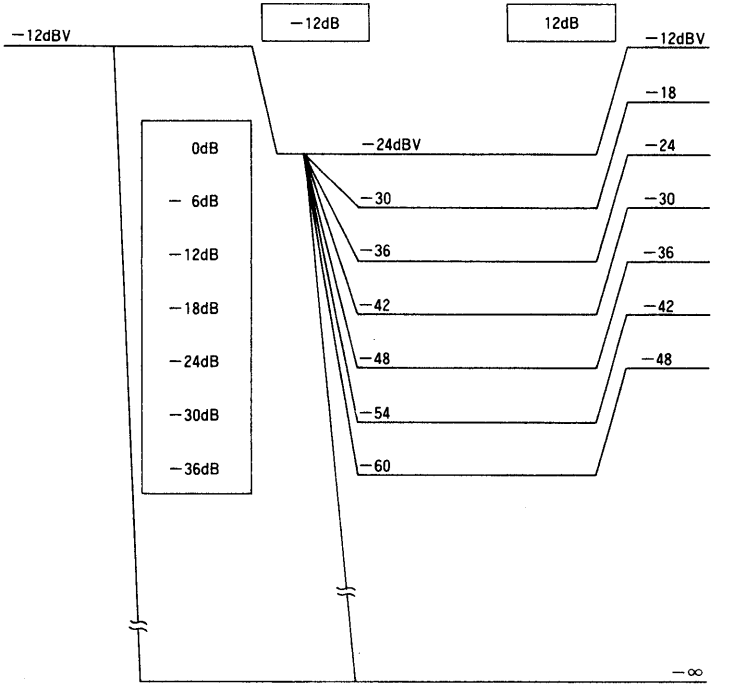




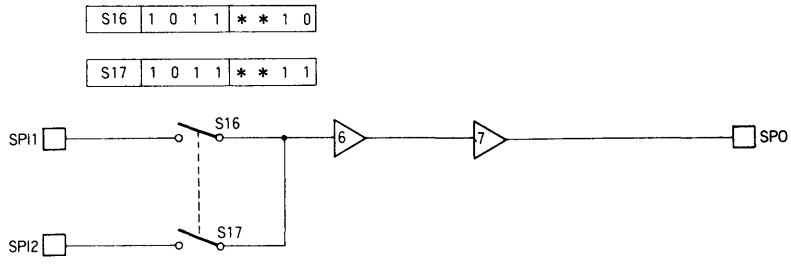
9. Second Transmission/Receiving Line

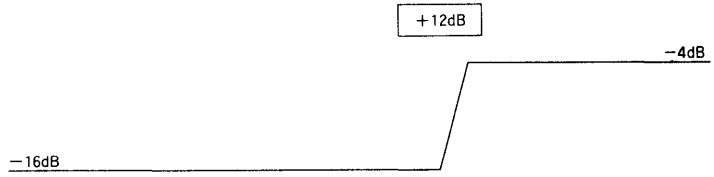
The second receive signal cannot be output from the handset. An outgoing call can be sent from both handset and handsfree. The same is true with what is shown on P. 2 and P. 5. Details are omitted herein.





10. Loud Speaker Output Line





HA16811ANT/HA16811AMP

SLIC IC for PBX Applications

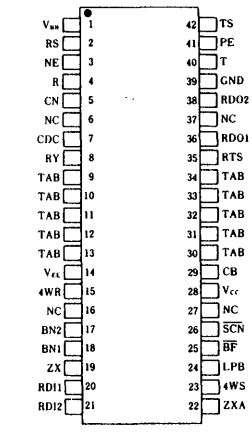
Bipolar linear process monolithic SLIC IC for PBX applications

Features

- Basic Functions: Internal battery feed control (B), loop supervision (S) and 2 W-4 W conversion
- Constant Current Feed: –24 V Supply voltage
- Internal darlington power transistor
- Ring trip detection
- Current shut-off function
- Two internal relay drivers
- Loop back function

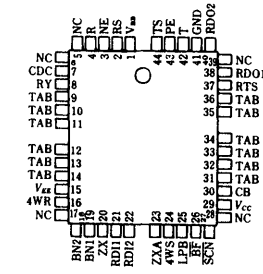
Pin Arrangement

HA16811ANT



(Top View)

HA16811AMP



(Top View)

Function

Basic Function

Current Feed Control

For PBX use, the Hitachi SLIC adapts the constant feed current method for the short distance line use. Therefore, Low power dissipation is realized by keeping the loop current typ. value at 30 mA when loop resistance $R_L = 50\ \Omega$. In addition, integration of power transistors for battery feed save mounting space on line cards.

Noise suppression circuitry insure impedance balance by improving the relative precision of the 39 Ω potential detect emitter resistor (equipped on both V_{BB} and GND sides).

Loop Supervision

The SLIC supervises subscribers' hook status (on/off) and outputs it to the $\overline{SCN}$ pin.

DC loop detection:

Detects DC loop status (open or closed) using a potential detection emitter connected to a current feed circuit and outputs it to the $\overline{SCN}$ pin through comparator

Ring Trip Detection:

See Additional Function

2 W–4 W Conversion

The SLIC provides 2-wire balanced to 4-wire signal ended conversion preventing the 4-wire input signal from returning to the 4-wire output by using external Cx, Zx, Z_{BN} and internal op-amp circuits.

Additional Function

Ring Trip Detection

With an externally connected CR filter, the Hitachi SLIC can detect the off hook of a called subscriber while ring relay sends a ringing signal. When the subscriber goes off hook, a DC current superimposed on the ringing signal flows through the telephone. This superimposed DC current is detected by the SLIC and a ring trip detection signal is sent to the system controller from the SCN pin.

Current Shut-Off Function

For protection PBX systems from the following causes, current feed is stopped by the command issued from the system controller to the $\overline{BF}$ pin.

- Subscriber loop line faults
- Emergency overload

Relay Drivers

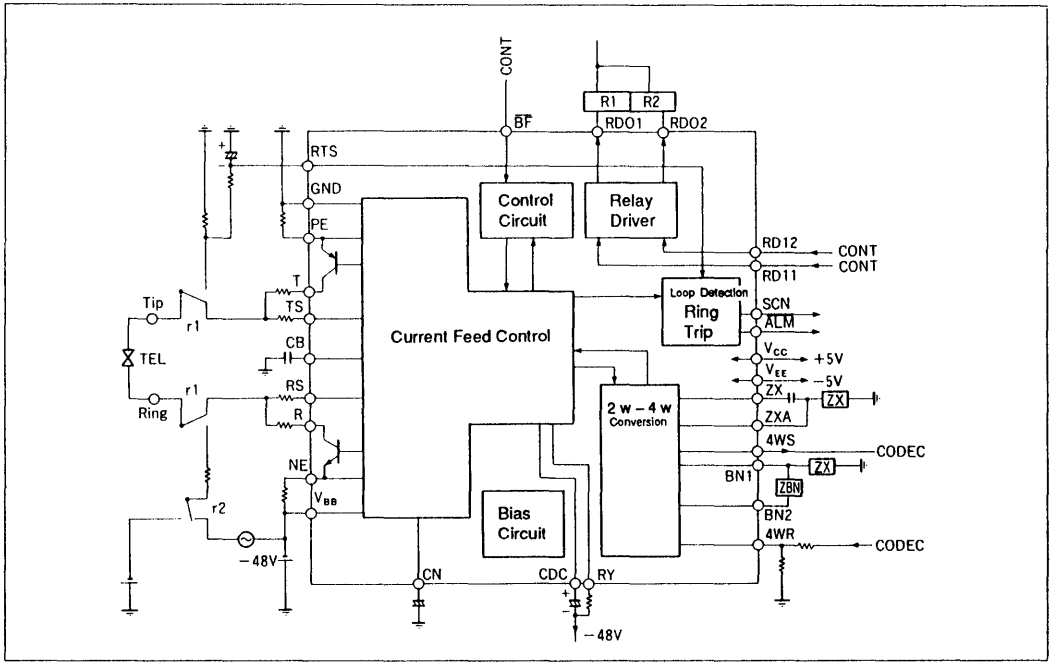
The Hitachi SLIC has two internal relay drivers

which drive the relay coil directly when an enable signal is sent to the RDI1 or RDI2 pin.

Loop Back Function

Though the Hitachi SLIC usually cancels the 4-wire returning signal, loop back command at the LPB pin enable sending a 4-wire input signal as a 4-wire output signal without sending it to the subscriber loop.

Block Diagram



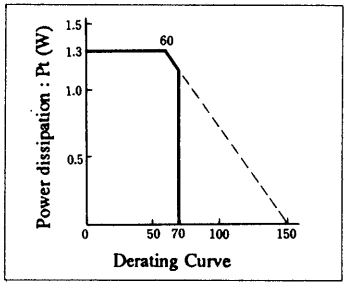
Pin Description

No. NT	No. MP	Pin Name	Functional Description
1	1	V_{BB}	–24 V voltage source input
2	2	Rs	Ring side potential detection input connected to the subscriber line through the detection resistor
3	3	NE	Ring side NPN darlington transistors' emitter potential detection input connected to V_{BB}(–24 V) through the emitter resistor
4	4	R	Ring side current feed output (sink) connected to the subscriber line through the protection resistor
5	5	CN	Connected to ground through the capacitor for power supply noise rejection
6	6	NC	No connection pin. It must not be connected to any other pin or printed circuit
7	7	C_{DC}	Low pass filter capacitor connection pin for DC feedback
8	8	RY	Connected to –24 voltage source through the resistor to make a precise differential feedback loop
9	9	TAB	Heatsink pins, connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.
10	10	TAB	
11	11	TAB	
12	12	TAB	
13	13,14	TAB	
14	15	V_{EE}	–5 V voltage source input
15	16	4WR	4-wire receive input which is connected to CODEC analog output through bleeder resistor for gain adjustment
16	17	NC	No connection pin. It must not be connected to any other pin or printed circuit
17	18	BN2	Analog input of differential amp. For transhybrid rejection, it's connected to the ground through termination impedance Zx, and to BN1 through impedance Z_{BN}
18	19	BN1	Received signal output pin connected to BN2 through balancing impedance Z_{BN}
19	20	ZX	DC cut capacitor and termination impedance Zx run between this terminal and ground
20	21	RDI1	TTL level digital input for relay enable signal from the system controller
21	22	RDI2	TTL level digital input for relay enable signal from the system controller
22	23	ZXA	Analog input of differential amp. For transmission, connected temination impedance Zx and DC cut capacitor
23	24	4WS	4-wire transmission output connected to CODEC
24	25	LPB	TTL level digital input for loop back enable signal from the system controller. The loop back 25mode is enable when input pin voltage is high
25	26	BF	TTL level digital input for current shut off command from the system controller. The current shut is enable when input pin voltage is high
26	27	SCN	TTL level compatible digital output which is common output of loop supervision and ring trip detection signal
27	28	NC	No connection pin. It must not be connected to any other pin or printed circuit.
28	29	Vcc	+5 V voltage source input
29	30	CB	Connected to the ground through the phase compensation capacitor for balance amp.
30	31	TAB	Heatsink pins, connected to the heatsink area fabricated on the print board. They must not be connected to any other pin or printed circuit
31	32	TAB	
32	33	TAB	
33	34	TAB	
34	35,36	TAB	
35	37	RTS	CR filter for ring trip detection connected to this terminal
36	38	RDO1	Analog output of relay driver connected to –24 V voltage source through a relay coil
37	39	NC	No connection pin. It must not be connected to any other pin or printed circuit
38	40	RDO2	Analog output of relay driver connected to –24 V voltage source through a relay coil
39	41	GND	Ground pin
40	42	T	Tip side current feed output (source) connected to the subscriber line through protection resistor
41	43	PE	Tip side PNP darlington transistors' emitter potential detection input connected the ground through emitter resistor.
42	44	TS	Tip side potential detection input connected to the subscriber line through the resistor for detection

Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Ratings	Unit	Notes
Supply Voltage	V_{BB}	–30	V	
	Vcc	7	V	
	V_{EE}	–7	V	
Power Dissipation	P_T	1.3	W	(Note 1)
Operating Temperature	Topr	0 to 70	°C	
Storage Temperature	Tstg	–55 to +125	°C	
Input Voltage	Vin1	–0.3 to Vcc + 0.3	V	Digital input pin (Note 2)
	Vin2	–5.0 to + 0.3	V	RTS pin
Input Current	I_{RS}	±117	mA	Rs pin, t ≤ 2 ms
	I_{TS}	±117	mA	Ts pin, t ≤ 2 ms
Relay Driver Output Source Current	I_{RDO}	–30	mA	RDO1, RDO2 pins

Notes 1: See derating curve
2: Indicates each BF, LPB, RDI1 and RDI2



The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Recommended Operating Conditions

Item		Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage		V_{BB}		–26.4	–24	–21.6	V
		Vcc		4.75	5	5.25	V
		V_{EE}		–5.25	–5	–4.75	V
Loop Resistance		R_L	Line resistance + Terminal resistance	0		600	Ω
Signal Input	2W	Vi2W				3.5	dBm
Level	4W	Vi4W				1.5	dBm
ZX Condition	Load Impedance	R_{ZX1}	Connectable load impedance	10	—	—	kΩ
ZXA Condition	Source Impedance	R_{ZR}	Connectable source impedance	—	—	200	kΩ
BN1 Condition	Source Impedance	R_{BN1}	Connectable source impedance	—	—	50	kΩ
BN2 Condition	Load Impedance	R_{BN2}	Connectable load impedance	10	—	—	kΩ

Electrical Characteristics

Direct Current Characteristics (V_{BB} = –24 V, V_{CC} = 5 V, V_{EE} = –5 V, Ta = 25 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit
Power Supply	On hook	I_{BB}	R_L = ∞	–4.5			mA
		I_{CC}			6.9	11.4	mA
		I_{EE}		–4.4	–2.9		mA
	Off hook	I_{BBL}	R_L = 50 Ω	–9.2			mA
		I_{CCL}				13.4	mA
		I_{EEL}		–4.4			mA
Power Dissipation	On hook	P_{DC}	R_L = ∞			180	mW
	Off hook	P_{DCL}	R_L = 200 Ω			850	mW
Direct Current Feed		I_{LO}	R_L = 50 Ω	26	30	34	mA
		I_{L300}	R_L = 300 Ω	26	30	34	mA
		I_{L600}	R_L = 600 Ω	20			mA
Loop Detection Resistance	Off hook	R_{LTH1}		900			Ω
	On hook	R_{LTH2}				10	kΩ
Relay Driver Output Voltage		RDV_{OH}	I_{OH} = –30 mA	–2.0			V
Ring Trip Comparator Threshold Voltage		$RTSV_{TH}$		–0.97	–0.85	–0.74	V
Input Clamp Diode		V_{FAP}	V_{BB} = –10 V	0.3		3	V
		V_{FAN}	I_F = 117 mA	0.3		3	V
		V_{FBP}		0.3		3	V
		V_{FBN}		0.3		3	V
Ground Short Protection	On	R_{GF1}	V_{BB} = –21.6 V	10			Ω
	Off	R_{GR3}	V_{BB} = –26.4 V			20	kΩ
Battery Short Protection	On	R_{BF1}	V_{BB} = –21.6 V	10			Ω
	Off	R_{BR3}	V_{BB} = –26.4 V			20	kΩ
Digital Input/Output	$\overline{BF}$	BFV_{IH}		2.0			V
		BFV_{IL}				0.8	V
		BFI_{IH}	V_{IH} = 2.0 V	–5	0	5	µA
		BFI_{IL}	V_{IL} = 0.8 V	–10	1	5	µA
	RDI1	$RD1V_{IH}$		2.0			V
		$RD1V_{IL}$				0.8	V
		$RD1I_{IH}$	V_{IH} = 2.0 V	65	100	170	µA
		$RD1I_{IL}$	V_{IL} = 0.8 V	14	40	70	µA
	RDI2	$RD2V_{IH}$		2.0			V
		$RD2V_{IL}$				0.8	V
		$RD2I_{IH}$	V_{IH} = 2.0 V	65	100	170	µA
		$RD2I_{IL}$	V_{IL} = 0.8 V	14	40	70	µA
	LPB	$LPBV_{IH}$				2.0	V
		$LPBV_{IL}$				0.8	V
		$LPBI_{IH}$	V_{IH} = 2.0 V	30	70	160	µA
		$LPBI_{IL}$	V_{IL} = 0.8 V	10	27	60	µA
	SCN	$SCNV_{OL}$	V_{CC} = 5.25 V I_{OL} = 1.6 mA			0.4	V
		$SCNV_{OH}$	V_{CC} = 4.75 I_{OH} = –0.4 mA	2.4			V

Alternating Current Characteristics (V_{BB} = –24 V, V_{CC} = 5 V, V_{EE} = –5 V, Ta = 25 °C)

Item		Symbol	Test Condition	Input Level (Vrms)	Min	Typ	Max	Unit
Transmission Gain	2 w→4 w	G241	f = 1 kHz	1.16	3.55	3.85	4.15	dB
	4 w→2 w	G421	R_L = 200 Ω	0.921	1.7	2.0	2.3	dB
Attenuation Distortion	2 w→4 w	GF24	f = 3.4 kHz	1.16	–0.1		0.1	dB
	4 w→2 w	GF42	1 kHz	0.921	–0.1		0.1	dB
			R_L = 300 Ω					
Idle Channel Noise		NI2	R_L = 200 Ω				–81.1	dBmop
		NI4					–81.1	dBmop
S/N	2 w→4 w	SN24	f = 1 kHz	1.16	53			dB
	4 w→2 w	SN42	R_L = 600 Ω	0.921	53			dB
Impedance Balance		LB2W	f = 3.4 kHz	0.775	40			dB
			R_L = 600 Ω					
Return Loss		LM1	f = 0.3 kHz	1.16	20			dB
			R_L = 200 Ω					
Balance Return Loss		LR	f = 3.4 kHz	0.921	23			dB
			R_L = 600 Ω					
Idle Channel Noise on Alternating Current Induction		NI2AC	R_L = 600 Ω				–72	dBmop
			f = 60 Hz					
			IAC = 6.4 mArms					
Loop Back Transmission Gain	4 w→4 w	GLPB44	f = 1 kHz	0.775	5.7	6.0	6.3	dB
			R_L = 200 Ω					
PSRR	V_{BB}→2w	LB2	f = 3.4 kHz	24.5mVrms		20		dB
	V_{CC}→2 w	LC2	R_L = 600 Ω	24.5mVrms		20		dB
	V_{EE}→2 w	LE2		24.5mVrms		20		dB

Digital Input/Output Logic

$\overline{SCN}$ Output Logic Truth Table

	Item		
$\overline{BF}$	R_L	Ground short	SCN
L	On hook	Ground/battery short	L
	R_L > Rth1	No ground/battery short	H
	Off hook	Ground/battery short	L
	R_L < Rth2	No ground/battery short	L
H	On hook	Ground/battery short	L
	R_L > Rth1	No ground/battery short	H
	Off hook	Ground/battery short	L
	R_L < Rth2	No ground/battery short	H

Loop Back Truth Table

LPB	Loop Back Mode
H	On
L	Off

Digital Input/Output Logic (cont)

Relay Driver Truth Table

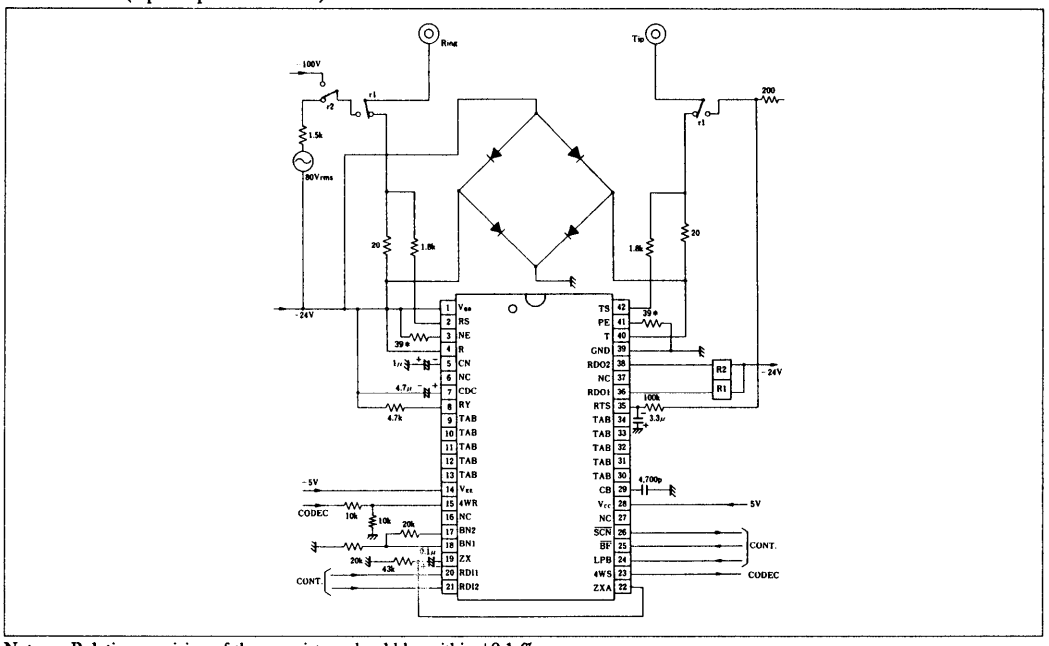
Input		Output	
RDI1	RDI2	RDO1	RDO2
H	—	H(On)	—
L	—	L(Off)	—
—	H	—	H(On)
—	L	—	L(Off)

$\overline{BF}$ Truth Table

$\overline{BF}$	Current Feed
H	Stop feeding
L	Feeding

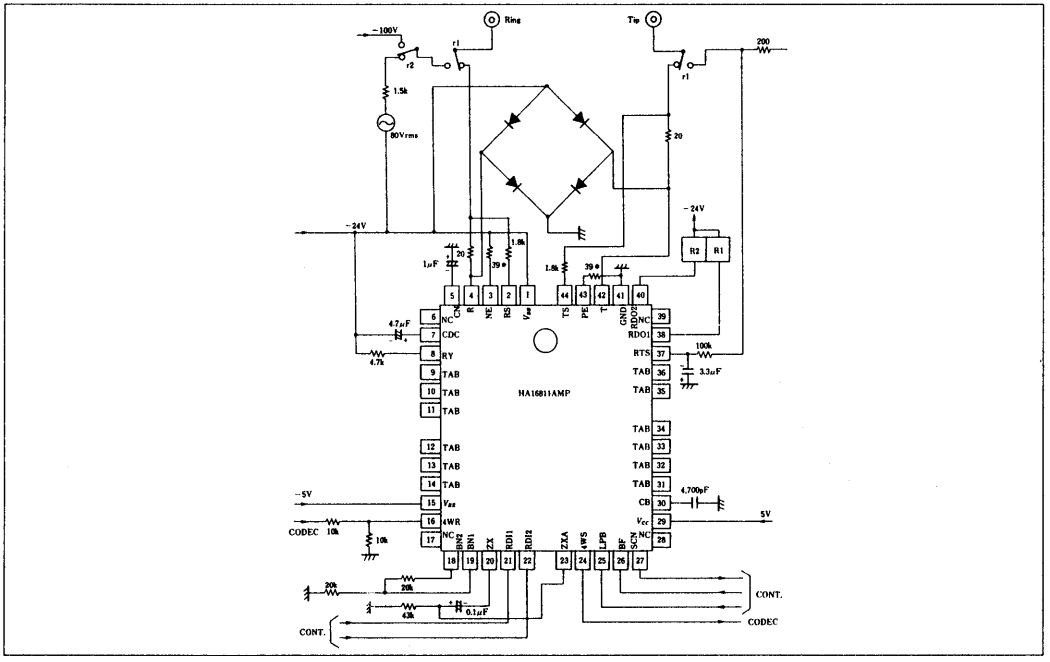
Circuit Example

HA16811ANT (Input Impedance: 600 Ω)



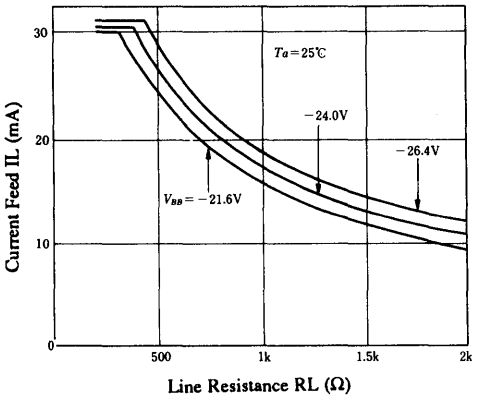
Note: Relative precision of these registers should be within ±0.1 %

HA16811AMP (Input Impedance: 600 Ω)

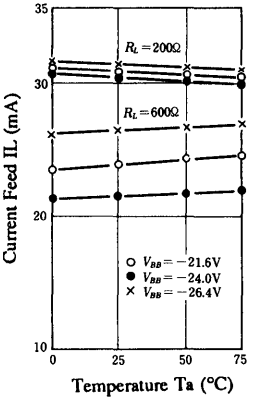


Note: Relative precision of these registers should be within ±0.1 %

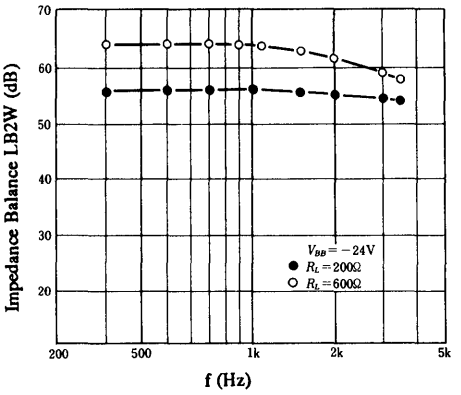
Current Feed vs. Line Resistance Characteristics



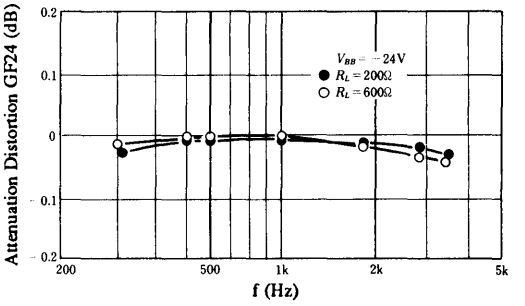
Current Feed vs. Temperature Characteristics



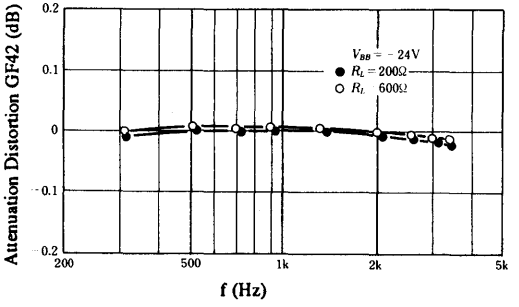
Impedance Balance vs. Frequency Characteristics



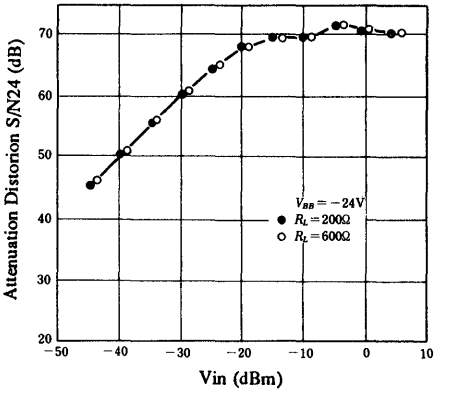
Attenuation Distortion vs. Frequency (2W → 4W) Characteristics



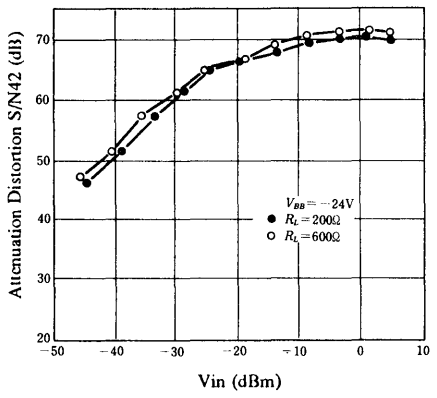
Attenuation Distortion vs. Frequency (4W → 2W) Characteristics



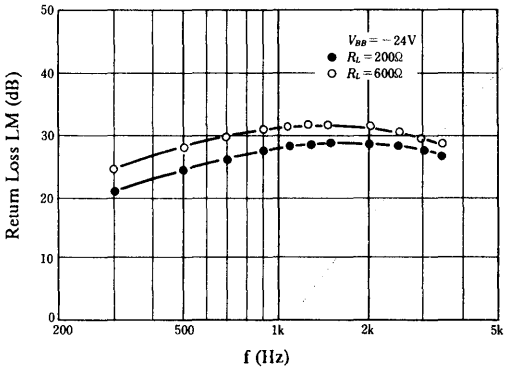
Attenuation Distortion vs. Input (4W → 2W) Characteristics



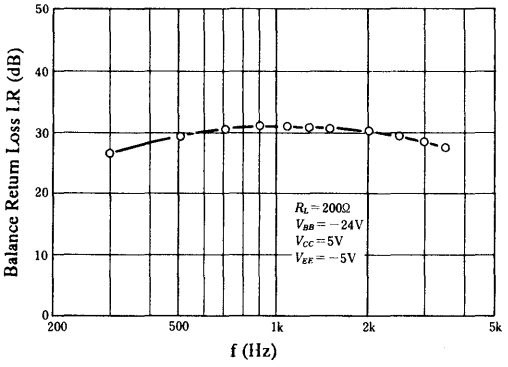
Attenuation Distortion vs. Input (2W → 4W) Characteristics



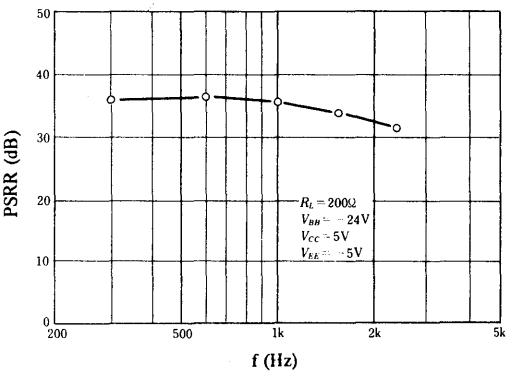
Return Loss vs. Frequency Charcteristics



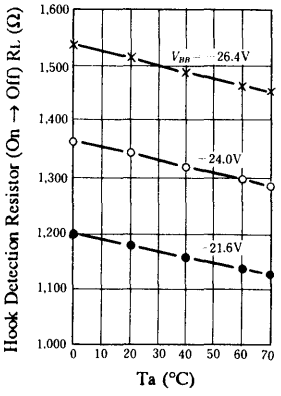
Balance Return Loss vs. Frequency Characteristics



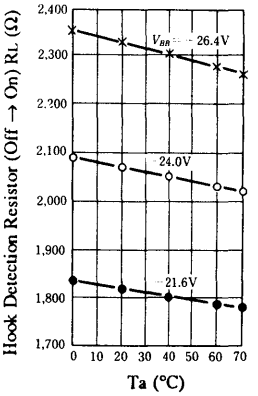
PSRR (VBB) vs Frequency Characteristics



Hook Detection Resistor (On → Off) vs. Temperature Characteristics –1



Hook Detection Resistor (Off → On) vs. Temperature Characteristics –2



HA16816 Series

SLIC IC for Key Telephone Applications

Features

- Basic Functions: Internal battery feed control (B), loop supervision (S) and 2w-4w conversion (H)
- Constant Current Feed: +24V Supply voltage
- Internal darlington power transistor
- Ring trip detection
- Current shut-off function
- Two internal relay drivers
- Loop back function

Function

1. Basic Function

1.1 Current Feed Control

For Key Telephone use, the Hitachi SLIC adapts the constant feed current method for the short distance line use. Therefore, Low power dissipation is realized by keeping the loop current Typ. value at 30mA when loop resistance $R_L = 50\Omega$. In addition, integration of power transistors for battery feed save mounting space on line cards. Noise suppression circuitry insure impedance balance by improving the relative precision of the 39Ω potential detect emitter resistor (equipped on both V_{BB} and GND sides).

1.2 Loop Supervision

The SLIC supervises subscribers' hook status (on/off) and outputs it to the $\overline{SCN}$ pin.

DC Loop Detection:

Detects DC loop status (open or closed) using a potential detection emitter connected to a current feed circuit and outputs it to the $\overline{SCN}$ pin through comparator.

Ring Trip Detection:

See 2-1.

1.3 2w-4w Conversion

The SLIC provides 2-wire balanced to 4-wire signal ended conversion preventing the 4-wire input signal from returning to the 4-wire output by using external Cx, Zx, ZBN and internal opamp circuits.

2. Additional Function

2.1 Ring Trip Detection

With an externally connected CR filter, the Hitachi SLIC can detect the off hook of a called subscriber while ring relay sends a ringing signal. When the subscriber goes off hook, a DC current superimposed on the ringing signal flows through the telephone. This superimposed DC current is detected by the SLIC and a ring trip detection signal is sent to the system controller from the $\overline{SCN}$ pin.

2.2 Current Shut-Off Function

For protection key telephone systems from the following causes, current feed is stopped by the command issued from the system controller to the $\overline{BF}$ pin.

- Subscriber loop line faults
- Emergency overload

2.3 Relay Drivers

The Hitachi SLIC has two internal relay drivers which drive the relay coil directly when an enable signal is sent to the RDI1 or RDI2 pin.

2.4 Loop Back Function

Though the Hitachi SLIC usually cancels the 4-wire returning signal, loop back command at the LPB pin enable sending a 4-wire input signal as a 4-wire output signal without sending it to the subscriber loop.

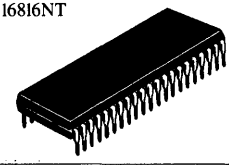
Ordering Information

Type No.	Package
HA16816NT	42 pin 600 mil Plastic Shrink DIP
HA16816MP	44 pin MSP

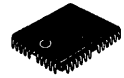
Notes:

1. NC indicates no connection pins. They must not be connected to any other pin or printed circuit.
2. Pins No. 9–13 and 30–34 are heatsink pins, connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.

HA16816NT

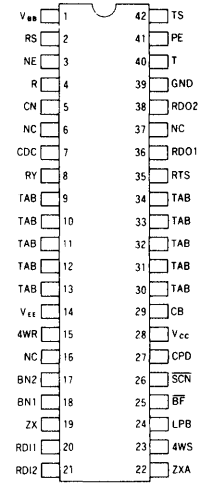


HA16816MP



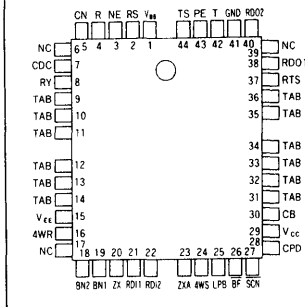
Pin Arrangement

● HA16816NT



(Top View)

● HA16816MP



(Top View)

Digital Input/Output Logic

• $\overline{SCN}$ Output Logic Truth Table

Item			
$\overline{BF}$	R_L	Ground Short	$\overline{SCN}$
L	On hook	Ground/battery short	L
	R_L > Rth1	No ground/battery short	H
	Off hook	Ground/battery short	L
	R_L < Rth2	No ground/battery short	L
H	On hook	Ground/battery short	L
	R_L > Rth1	No ground/battery short	H
	Off hook	Ground/battery short	L
	R_L < Rth2	No ground/battery short	H

• Loop Back Truth Table

LPB	Loop Back Mode
H	On
L	Off

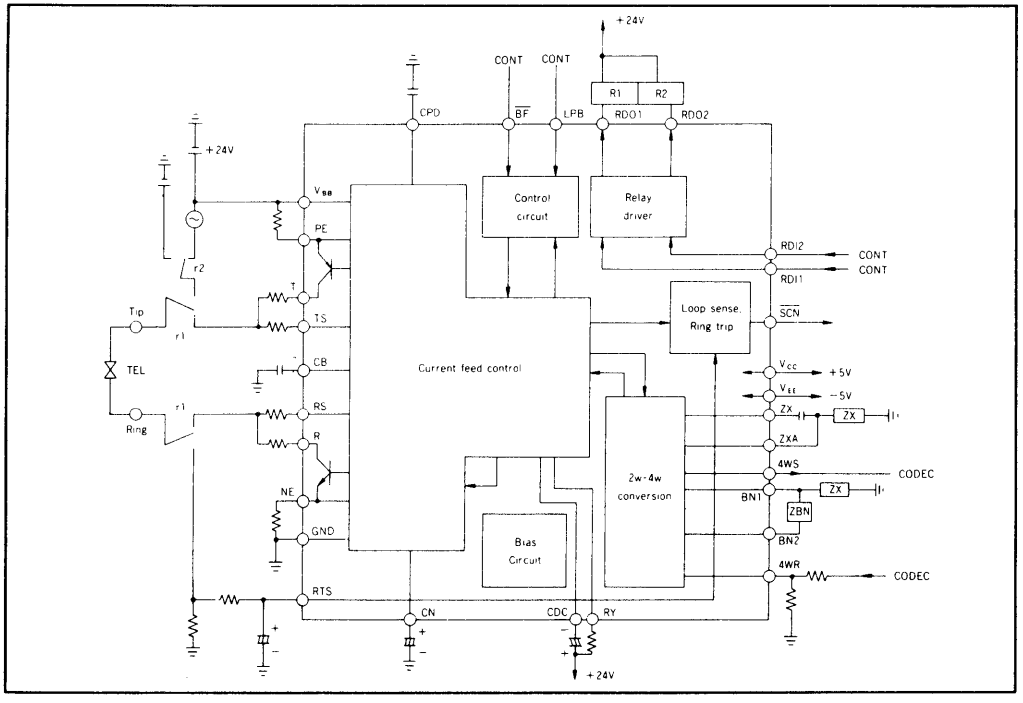
• Relay Driver Truth Table

Input		Output	
RDI1	RDI2	RDO1	RDO2
H	–	L (On)	–
L	–	H (Off)	–
–	H	–	L (On)
–	L	–	H (Off)

• $\overline{BF}$ Truth Table

$\overline{BF}$	Current Feed
H	Stop feeding
L	Feeding

Block Diagram



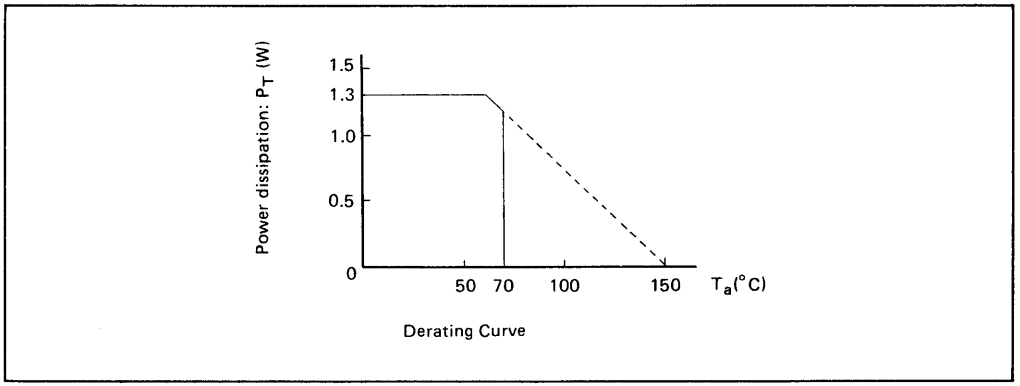
Pin Description

No. NT	MP	Pin name	Functional description
1	1	V_{BB}	+24V voltage source input
2	2	RS	Ring side potential detection input connected to the subscriber line through the detection resistor
3	3	NE	Ring side NPN darlington transistors emitter potential detection input connected to ground through the emitter resistor
4	4	R	Ring side current feed output (sink) connected to the subscriber line through the protection resistor
5	5	CN	Connected to ground through the capacitor for power supply noise rejection
6	6	NC	No connection pin. It must not be connected to any other pin or printed circuit
7	7	CDC	Low pass filter capacitor connection pin for DC feedback
8	8	RY	Connected to +24 voltage source through the resistor to make a precise differential feedback loop
9	9	TAB	Heatsink pins, connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.
10	10	TAB	
11	11	TAB	
12	12	TAB	
13	13	TAB	
	14	TAB	
14	15	V_{EE}	−5V voltage source input
15	16	4WR	4-wire receive input which is connected to CODEC analog output through bleeder resistor for gain adjustment
16	17	NC	No connection pin. It must not be connected to any other pin or printed circuit
17	18	BN2	Received signal output pin connected to BN1 through balancing impedance ZBN
18	19	BN1	Analog input of differential amp. For transhybrid rejection, it's connected to the ground through termination impedance ZX, and to BN2 through impedance ZBN
19	20	ZX	DC cut capacitor and termination impedance ZX run between this terminal and ground
20	21	RD 1	TTL level digital input for relay enable signal from the system controller
21	22	RD 2	TTL level digital input for relay enable signal from the system controller
22	23	ZXA	Analog input of differential amp. For transmission, connected termination impedance ZX and DC cut capacitor
23	24	4WS	4-wire transmission output connected to CODEC
24	25	LPB	TTL level digital input for loop back enable signal from the system controller. The loop back mode is enable when input pin voltage is high
25	26	$\overline{BF}$	TTL level digital input for current shut off command from the system controller. The current shut is enable when input pin voltage is high
26	27	$\overline{SCN}$	TTL level compatible digital output which is common output of loop supervision and ring trip detection signal
27	28	CPD	Connected to ground through ground short/battery short protection delay capacitor
28	29	V_{CC}	+5V voltage source input
29	30	CB	Connected to the ground through the phase compensation capacitor for balance amp.
30	31	TAB	Heatsink pins, connected to the heatsink area fabricated on the print board. They must not be connected to any other pin or printed circuit.
31	32	TAB	
32	33	TAB	
33	34	TAB	
34	35	TAB	
	36	TAB	
35	37	RTS	CR filter for ring trip detection connected to this terminal
36	38	RDO1	Analog output of relay driver
37	39	NC	No connection pin. It must not be connected to any other pin or printed circuit.
38	40	RDO2	Analog output of relay driver
39	41	GND	Ground pin
40	42	T	Tip side current feed output (source) connected to the subscriber line through protection resistor
41	43	PE	Tip side PNP darlington transistors' emitter potential detection input connected to V_{BB} through emitter resistor.
42	44	TS	Tip side potential detection input connected to the subscriber line through the resistor for detection

Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Ratings	Unit	Notes
Supply Voltage	V_{BB}	30	V	
	V_{CC}	7	V	
	V_{EE}	−7	V	
Input Voltage	Vin 1	−0.3 to V_{CC} +0.3	V	Digital input pin (Note 2)
	Vin 2	−0.3 to +5.0	V	RTS pin
Input Current	I_{RS}	±117	mA	Rs pin, t ≤ 2 ms
	I_{TS}	±117	mA	Ts pin, t ≤ 2 ms
Power Dissipation	P_T	1.3	W	(Note 1)
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tstg	−55 to +125	°C	
Relay Drive Output Source Current	I_{RDO}	30	mA	RDO1, RDO2 pins
Junction Temperature	Tjmax	150	°C	

Notes) 1. See derating curve
2. Indicates each BR, LPB, RD 1 and RD 2



Derating Curve

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Recommended Operating Conditions

Item		Symbol	min.	typ.	max.	Unit	Test Condition
Supply Voltage		V_{BB}	21.6	24	26.4	V	
		V_{CC}	4.75	5	5.25	V	
		V_{EE}	−5.25	−5	−4.75	V	
Loop Resistance		R_L	0	—	600	Ω	Line resistance + Terminal resistance
Signal Input Level	2W	V_{i2W}	—	—	3.5	dBm	
	4W	V_{i4W}	—	—	1.5	dBm	
ZX Condition	Load Impedance	R_{ZX1}	10	—	—	kΩ	Connectable load impedance
ZXA Condition	Source Impedance	R_{ZR}	—	—	200	kΩ	Connectable source impedance
BN1 Condition	Source Impedance	R_{BN1}	—	—	50	kΩ	Connectable source impedance
BN2 Condition	Load Impedance	R_{BN2}	10	—	—	kΩ	Connectable load impedance

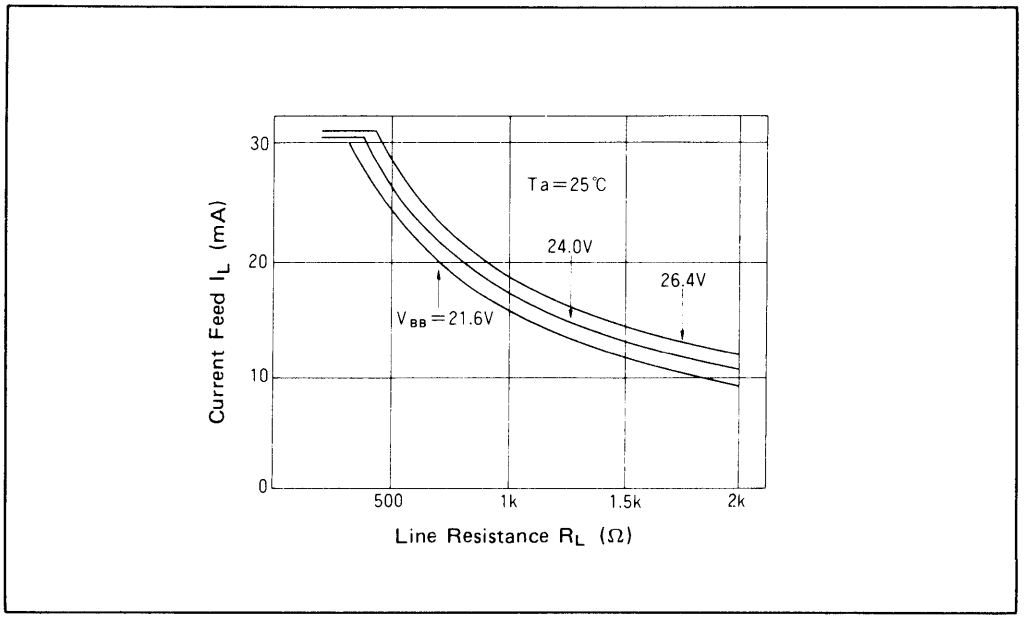
Electrical Characteristics

DC Characteristics (V_{BB} = 24V, V_{CC} = 5V, V_{EE} = –5V, Ta = 25°C)

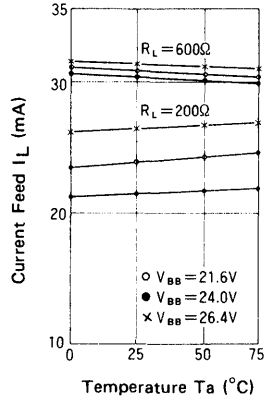
Item		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Power Supply	On hook	I_{BB}	–	–	4.5	mA	R_L=∞
		I_{CC}	–	6.9	11.4	mA	
		I_{EE}	–5.9	–2.9	–	mA	
	Off hook	I_{BBL}	–	–	9.2	mA	R_L=50Ω
		I_{CCL}	–	–	13.4	mA	
		I_{EEL}	–6.2	–	–	mA	
Power Dissipation	On hook	P_{DC}	–	–	180	mW	R_L=∞
	Off hook	P_{DCL}	–	–	850	mW	R_L=200Ω
Direct Current Feed		I_{L0}	26	30	34	mA	R_L=50Ω
		I_{L300}	26	30	34	mA	R_L=300Ω
		I_{L600}	20	–	–	mA	R_L=600Ω
Loop Detection Current	Off hook	I_{LTH1}	10	–	15	mA	
	On hook	I_{LTH2}	5	–	9.5	mA	
Relay Driver Output Voltage		RDV_{OL}	–	–	2.0	V	I_{OL}=30mA
Ring Trip Comparator Threshold Voltage		$RTSV_{TH}$	0.74	0.85	0.97	V	
Input Clamp Diode		V_{FAP}	0.3	–	3	V	V_{BB}=10V
		V_{FAN}	0.3	–	3	V	I_F=177mA
		V_{FBP}	0.3	–	3	V	
		V_{FBN}	0.3	–	3	V	
Ground Short Protection	On	R_{GF1}	10	–	–	Ω	V_{BB}=21.6V
	Off	R_{GR3}	–	–	20	kΩ	V_{BB}=26.4V
Battery Short Protection	On	R_{BF1}	10	–	–	Ω	V_{BB}=21.6V
	Off	R_{BR3}	–	–	20	kΩ	V_{BB}=26.4V
Digital Input/Output	BF	BFV_{IH}	2.0	–	–	V	
		BFV_{IL}	–	–	0.8	V	
		BFI_{IH}	–2	0	2	μA	V_{IH}=2.0V
		BFI_{IL}	–2	1	2	μA	V_{IL}=0.8V
	RD11	$RD1V_{IH}$	2.0	–	–	V	
		$RD1V_{IL}$	–	–	0.8	V	
		$RD1I_{IH}$	65	100	170	μA	V_{IH}=2.0V
		$RD1I_{IL}$	14	40	70	μA	V_{IL}=0.8V
	RD12	$RD2V_{IH}$	2.0	–	–	V	
		$RD2V_{IL}$	–	–	0.8	V	
		$RD2I_{IH}$	65	100	170	μA	V_{IH}=2.0V
		$RD2I_{IL}$	14	40	70	μA	V_{IL}=0.8V
	LPB	$LPBV_{IH}$	2.0	–	–	V	
		$LPBV_{IL}$	–	–	0.8	V	
		$LPBI_{IH}$	–2	–	2	μA	V_{IH}=2.0V
		$LPBI_{IL}$	–2	–	2	μA	V_{IL}=0.8V
	SCN	$SCNV_{OL}$	–	–	0.4	V	V_{CC}=5.25V I_{OL}=1.6mA
		$SCNV_{OH}$	2.4	–	–	V	V_{CC}=4.75V I_{OH}=–0.4mA

AC Characteristics (V_{BB} = 24V, V_{CC} = 5V, V_{EE} = −5V, Ta = 25°C)

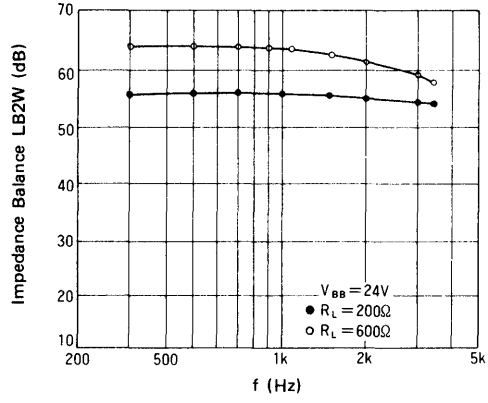
Item		Symbol	Input Level (Vrms)	Min.	Typ.	Max.	Unit	Test Condition
Transmission	2w→4w	G241	1.16	3.55	3.85	4.15	dB	f=1kHz
Gain	4w→2w	G421	0.921	1.7	2.0	2.3	dB	R_L=200Ω
Attenuation	2w→4w	GF24	1.16	−0.1	—	0.1	dB	f=3.4kHz 1kHz
Distortion	4w→2w	GF42	0.921	−0.1	—	0.1	dB	R_L=200Ω
Idle Channel Noise		NI2	—	—	—	−81.1	dBmop	R_L=200Ω
		NI4	—	—	—	−81.1	dBmop	
S/N	2w→4w	SN24	1.16	53	—	—	dB	f=1kHz
	4w→2w	SN42	0.921	53	—	—	dB	R_L=600Ω
Impedance Balance		LB2W	0.775	40	—	—	dB	f=3.4kHz R_L=600Ω
Return Loss		LM1	1.16	20	—	—	dB	f=0.3kHz R_L=200Ω
Balance Return Loss		LR	0.921	25	—	—	dB	f=3.4kHz R_L=600Ω
Idle Channel Noise on Alternating Current Induction		NI2AC	—	—	—	−72	dBmop	R_L=600Ω f=60Hz I_{AC}=6.4 mArms/ one-way line
Loop Back Transmission Gain	4w→4w	GLPB44	0.775	5.7	6.0	6.3	dB	f=1kHz R_L=200Ω
PSRR	V_{BB}→2w	LB2	24.5mVrms	20	—	—	dB	f=3.4kHz
	V_{CC}→2w	LC2	24.5mVrms	20	—	—	dB	R_L=600Ω
	V_{EE}→2w	LE2	24.5mVrms	20	—	—	dB	



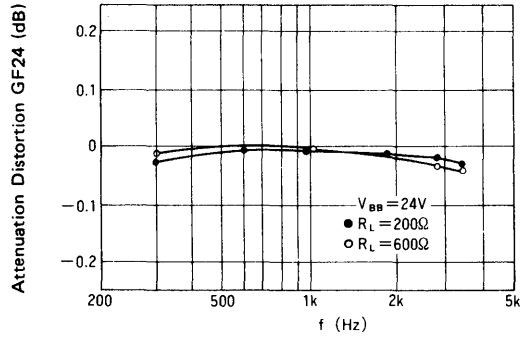
Current Feed vs. Line Resistance Characteristics



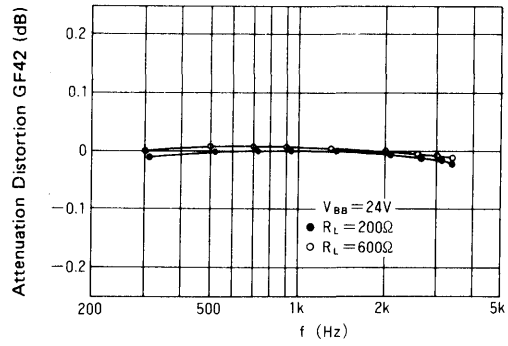
Current Feed vs. Temperature Characteristics



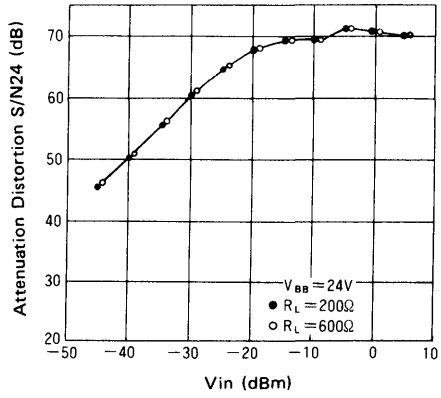
Impedance Balance vs. Frequency Characteristics



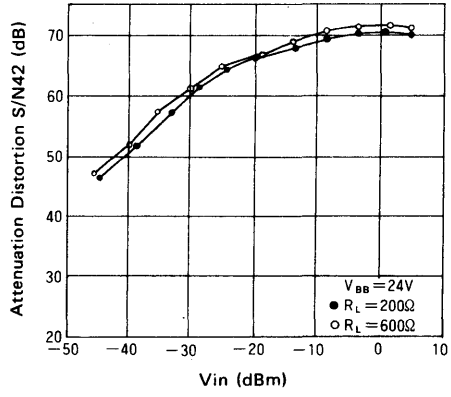
Attenuation Distortion vs. Frequency (2W → 4W) Characteristics



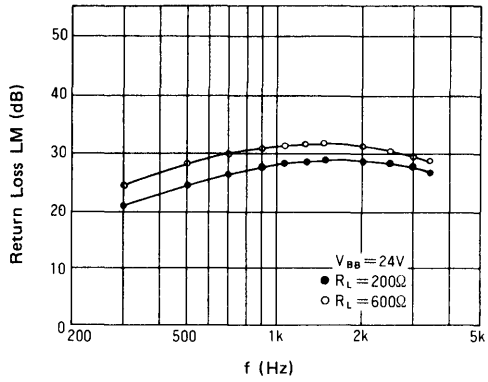
Attenuation Distortion vs. Frequency (4W → 2W) Characteristics



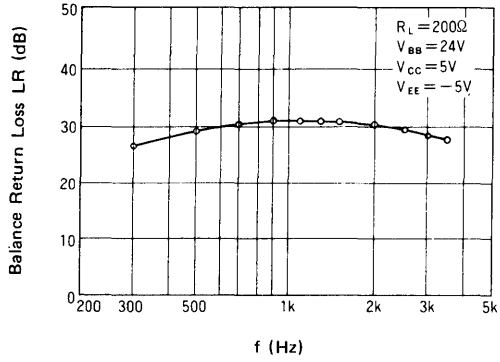
Attenuation Distortion vs. Input (2W → 4W) Characteristics



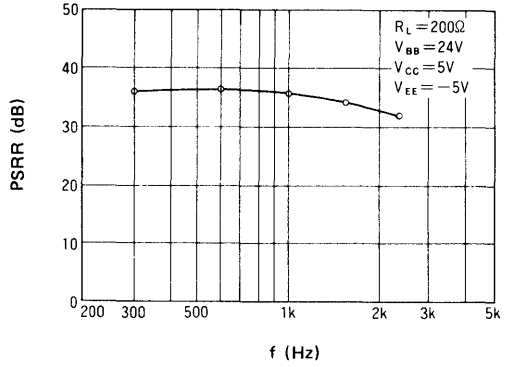
Attenuation Distortion vs. Input (4W → 2W) Characteristics



Return Loss vs. Frequency Characteristics



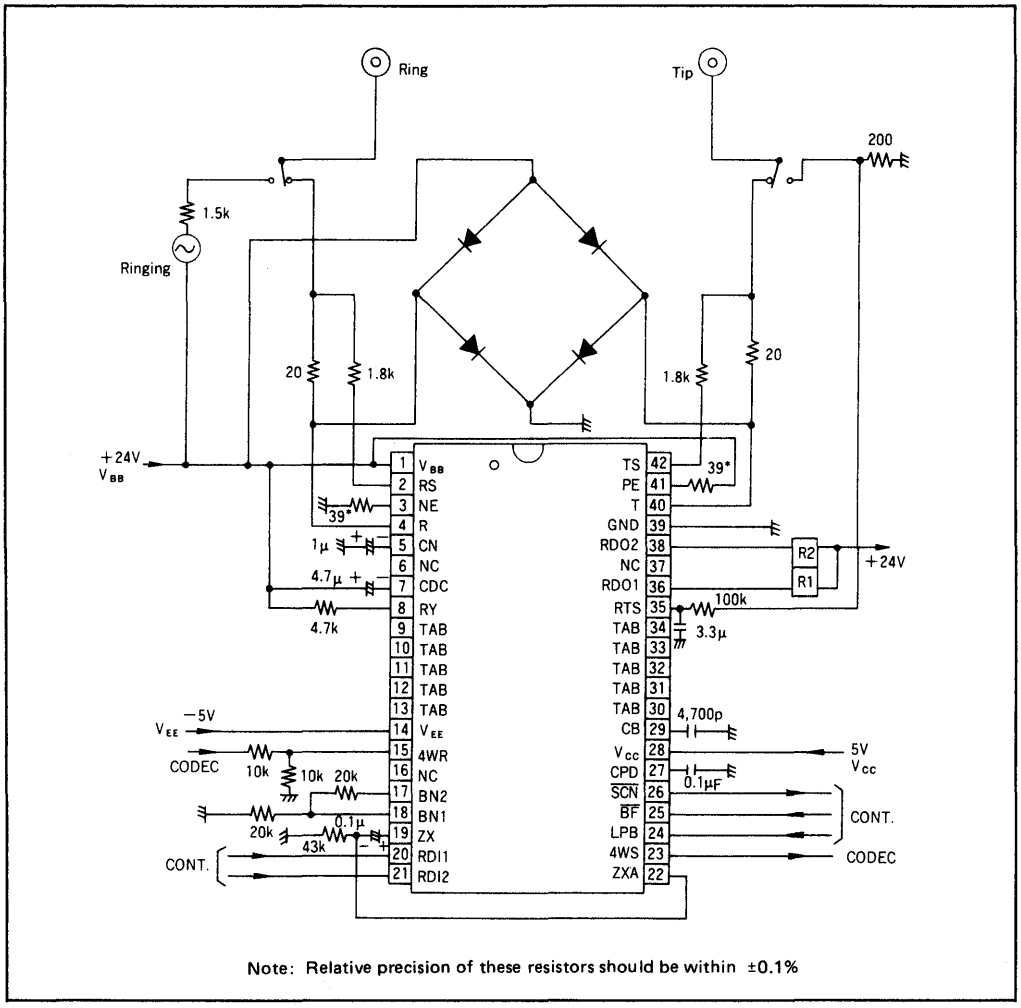
Balance Return Loss vs. Frequency Characteristics



PSRR (V_{BB}) vs. Frequency Characteristics

Circuit Example (HA16816NT)

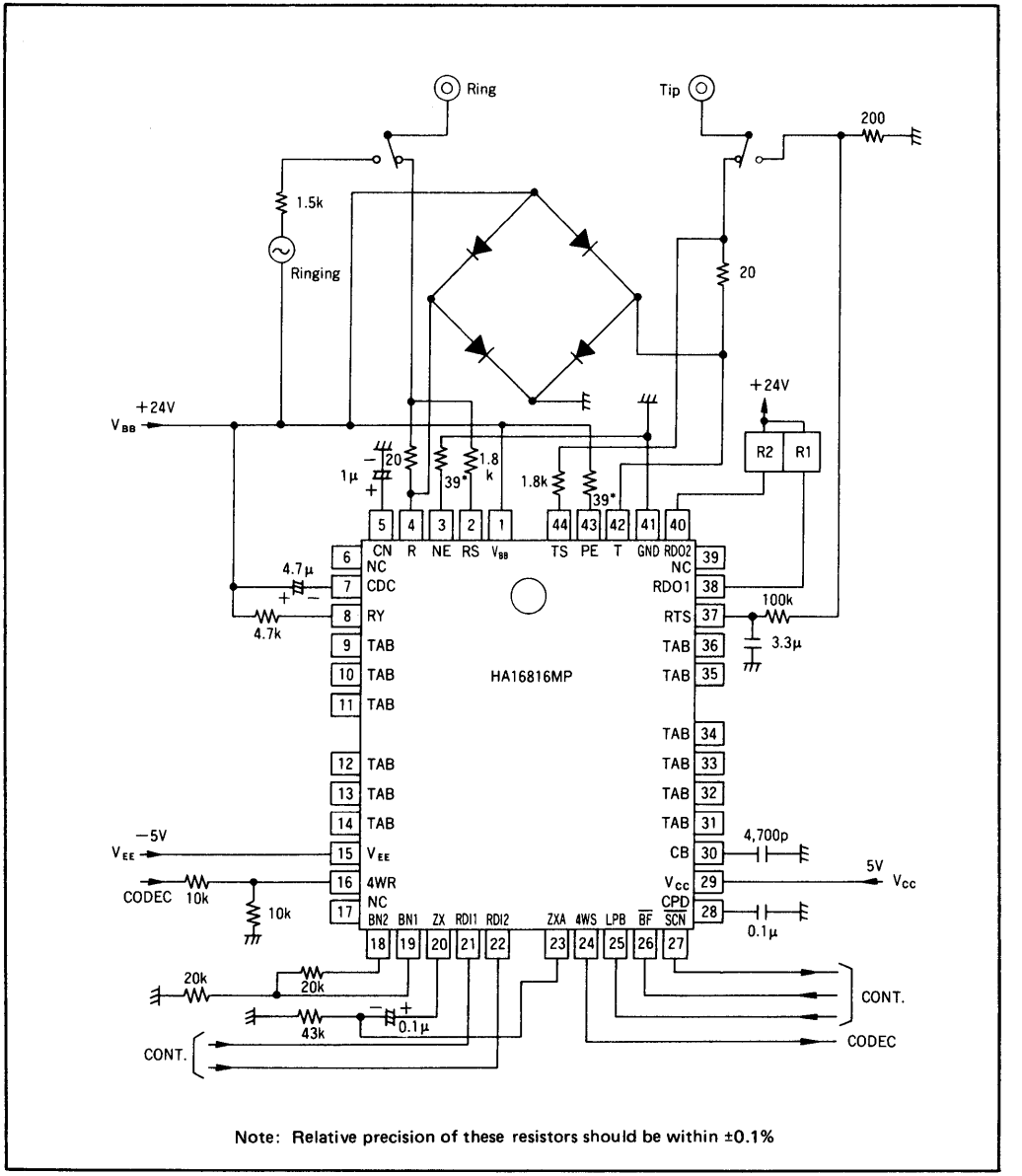
Input Impedance: 600Ω



Note: Relative precision of these resistors should be within ±0.1%

Circuit Example (HA16816MP)

Input Impedance: 600Ω

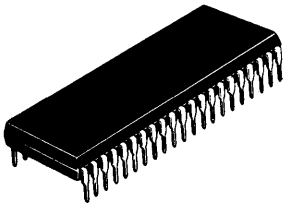


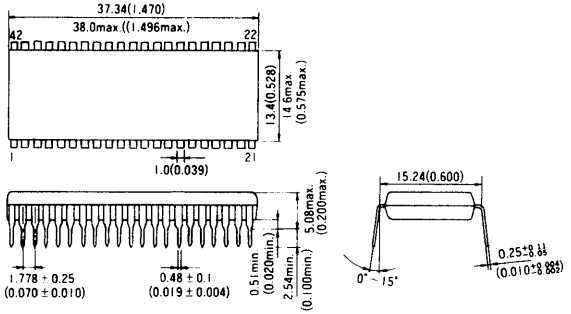
Note: Relative precision of these resistors should be within ±0.1%

Package Dimensions

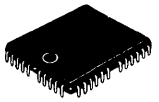
Unit: mm (inch)

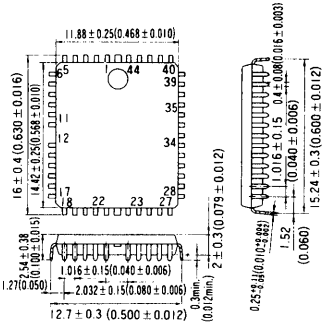
HA16816NT





HA16816MP





3

SLIC IC for PBX Applications

Bipolar linear process monolithic SLIC IC for PBX applications

Features

- Basic Functions: Internal battery feed control (B), loop monitor (S) and 2 W–4 W conversion
- Constant Current Feed: –48 V supply voltage
- Internal Darlington power transistor
- Ring trip detection
- Current shutdown function
- Two internal relay drivers

Functions

Basic Functions

Current Feed Control

For PBX use, the Hitachi SLIC adapts the constant feed current method for short distance line use. Therefore, low power dissipation is realized by keeping the loop current Typical value at 27 mA when loop resistance RL = 50 Ω. In addition, integration of power transistors for battery feed saves mounting space on line cards.

Noise suppression circuitry insures impedance balance by improving the relative precision of the 39 Ω potential detect emitter resistor (equipped on both VBB and GND sides).

Loop Detection

The SLIC detects subscribers' hook status (on/off) and outputs it to the SCN pin.

DC loop detection:

Detects DC loop status (open or closed) using a potential detection emitter connected to a current feed circuit and outputs it to the SCN pin through a comparator.

Ring Trip Detection:

See Additional Functions

2 w–4 w Conversion

The SLIC provides 2-wire balanced to 4-wire single ended conversions preventing the 4-wire input signal from returning to the 4-wire output by using external Cx, Zx, ZBN and internal opamp circuits.

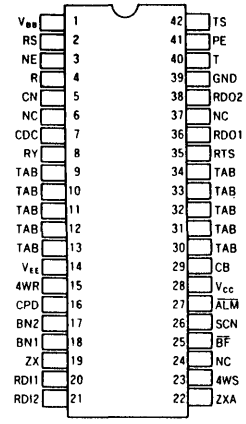
Additional Functions

Ring Trip Detection

With an externally connected CR filter, the Hitachi SLIC can detect the off-hook status of a called subscriber while ring relay is sending a ringing signal. When the subscriber goes off hook, a DC current superimposed on the ringing signal flows through the

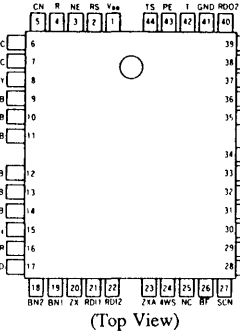
Pin Arrangement

HA16817NT



(Top View)

HA16817MP



(Top View)

Current Shut-Off Function

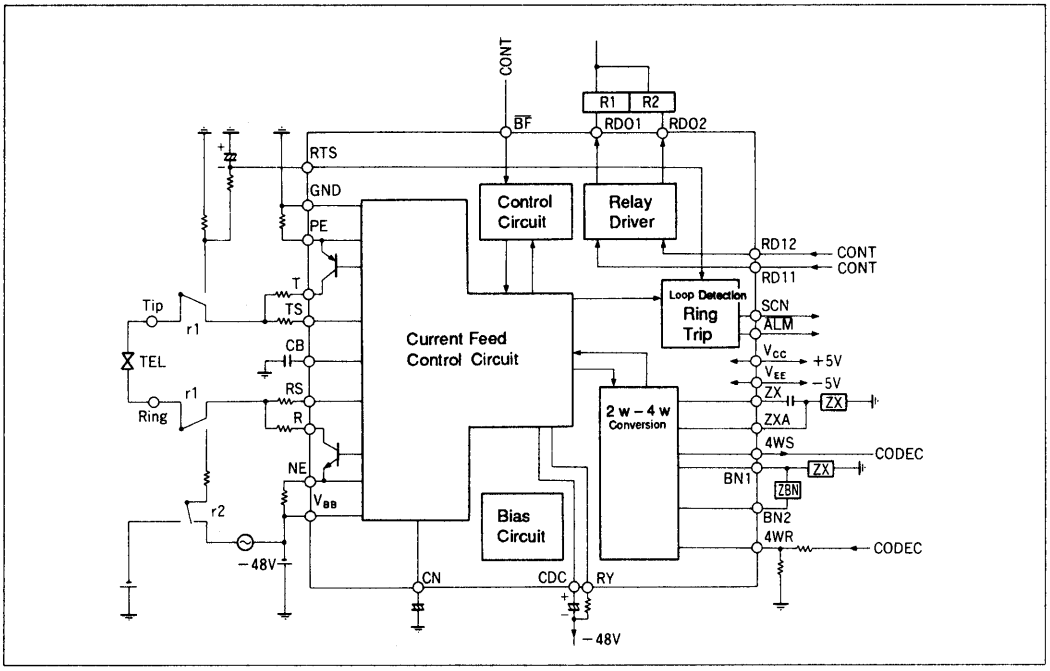
To protect PBX systems from the following problems, current feed is stopped by a command issued from the system controller to the BF pin.

- Subscriber loop line faults
- Emergency overload

Relay Drivers

The Hitachi SLIC has two internal relay drivers which drive the relay coil directly when an enable signal is sent to the RDI1 or RDI2 pin.

Block Diagram



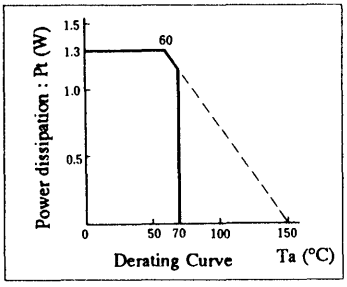
Pin Description

No. NT	No. MP	Name	Functional Description
1	1	V_{BB}	–48 V source input
2	2	RS	Ring-side potential detection input connected to the subscriber line through the detection resistor
3	3	NE	Ring-side NPN Darlington transistors' emitter potential detection input connected to V_{BB} (–48 V) through the emitter resistor
4	4	R	Ring-side current feed output (sink) connected to the subscriber line through the protection resistor
5	5	CN	Connected to ground through the noise filtering capacitor for power supply
6	6	NC	No connection.Must not be connected to any other pin or printed circuit
7	7	CDC	Low-pass filter capacitor connection pin for DC feedback
8	8	RY	Connected to –48 voltage source through the resistor to make a precise differential feedback loop
9-10	9-14	TAB	Heatsink pins, connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.
14	15	V_{EE}	–5 voltage source input
15	16	4WR	4-wire receive input which is connected to CODEC analog output through bleeder resistor for gain adjustment
16	17	CPD	Ground/battery short protection capacitor pin. Ground through capacitor.
17	18	BN2	Received signal output pin connected to BN1 through balancing impedance Z_{BN}
18	19	BN1	Analog input of differential amp. For transhybrid rejection, it's connected to the ground through termination impedance Zx, and to BN2 through impedance Z_{BN}.
19	20	ZX	DC cut capacitor and termination impedance Zx run between this terminal and ground
20	21	RDI1	TTL-level digital input for relay enable signal from the system controller
21	22	RDI2	TTL-level digital input for relay enable signal from the system controller
22	23	ZXA	Analog input of differential amp. For transmission, connected between termination impedance Zx and DC cut capacitor.
23	24	4WS	4-wire transmission output connected to CODEC
24	25	NC	No connection.Must not be connected to any other pin or printed circuit
25	26	$\overline{BF}$	TTL-level digital input for current shut-off command from the system controller. The current shut-off is enabled when input pin voltage is high.
26	27	SCN	TTL-level compatible digital output which is the common output of loop monitor and ring trip detection signals
27	28	$\overline{ALM}$	Ground detection output pin
28	29	Vcc	+5 voltage source input
29	30	CB	Connected to the ground through the phase compensation capacitor for balance amp
30-34	31-36	TAB	Heatsink pins, connected to the heatsink area fabricated on the printed board. They must not be connected to any other pin or printed circuit.
35	37	RTS	CR for ring trip detection is connected to this terminal.
36	38	RDO1	Analog output of relay driver connected to –48 voltage source through a relay coil
37	39	NC	No connection. Must not be connected to any other pin or printed circuit.
38	40	RDO2	Analog output of relay driver connected to –48 voltage source through a relay coil
39	41	GND	Ground pin
40	42	T	Tip-side current feed output (sink) connected to the subscriber line through the protection resistor
41	43	PE	Tip-side PNP Darlington transistors' emitter potential detection input connected to V_{BB} (–48 V) through the emitter resistor
42	44	TS	Ring-side potential detection input connected to the subscriber line through the detection resistor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Notes
Supply Voltage	V_{BB}	–60	V	
	V_{CC}	7	V	
	V_{EE}	–7	V	
Power Dissipation	P_T	1.3	W	(Note 1)
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tstg	–55 to +125	°C	
Junction Temperature	Tjmax	150	°C	
Input Voltage	Vin1	–0.3 to Vcc+0.3	V	Digital input pin (Note 2)
	Vin2	–5.0 to +0.3	V	RTS pin
Input Current	I_{RS}	±117	mA	Rs pin, t ≤ 2 ms
	I_{TS}	±117	mA	Ts pin, t ≤ 2 ms
Relay Driver Output Source Current	I_{RDO}	–30	mA	RDO1, RDO2 pins

Notes 1: See derating curve
2: Indicates each $\overline{BF}$, LPB, RDI1 and RDI2



The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Recommended Operating Conditions

Item		Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage		V_{BB}		–53	–48	–43	V
		Vcc		4.75	5	5.25	V
		V_{EE}		–5.25	–5	–4.75	V
Loop Resistance		R_L	Line resistance + Terminal resistance	50		1200	Ω
Signal Input Level	2W	V_{I2W}				3.5	dBm
	4W	V_{I4W}				1.5	dBm
ZX condition	Load impedance	R_{ZX1}	Connectable load impedance	10			kΩ
ZXA condition	Signal source impedance	R_{ZR}	Connectable signal source impedance			200	kΩ
BN1 condition	Signal source impedance	R_{BN1}	Connectable signal source impedance			50	kΩ
BN2 condition	Load impedance	R_{BN2}	Connectable load impedance	10			kΩ

Electrical Characteristics

DC Characteristics (V_{BB} = –48 V, V_{CC} = 5 V, V_{EE} = –5 V, Ta = 25°C)

Item		Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply	On hook	I_{BB}	R_L = ∞	–4.0	–1.3	—	mA
		I_{CC}		—	6.6	12.0	mA
		I_{EE}		–5.0	–2.5	—	mA
	Off hook	I_{BBL}	R_L = 50 Ω	–9.0	–4.8	—	mA
		I_{CCL}		—	8.1	14.0	mA
		I_{EEL}		–5.0	–2.5	—	mA
Power Dissipation	On hook	P_{DC}	R_L = ∞	—	—	270	mW
	Off hook	P_{DCL}	R_L = 200 Ω	—	—	1300	mW
Direct Current Feed		I_{LO}	R_L = 50 Ω	24	27	31	mA
		I_{L300}	R_L = 600 Ω	24	27	31	mA
		I_{L600}	R_L = 1200 Ω	20	—	—	mA
Loop Detection	Off hook	I_{LTH1}		11	—	16	mA
Current	On hook	I_{LTH2}		6	—	11	mA
Relay Driver Output Voltage		RDV$_{OH}$	I_{OH} = –30 mA	–2.0	—	—	V
Ring Trip Comparator Threshold Voltage		RTSV$_{TH}$		–0.97	–0.85	–0.74	V
Input Clamp Diode		V_{FAP}	V_{BB} = 10 V	0.3	—	3	V
		V_{FAN}	I_F = 117 mA	0.3	—	3	V
		V_{FBP}		0.3	—	3	V
		V_{FBN}		0.3	—	3	V
Ground Short	On	R_{GF1}	V_{BB} = –43 V	250	—	—	Ω
Protection	Off	R_{GR3}	V_{BB} = –48 V	—	—	20	kΩ
Battery Short	On	R_{BF1}	V_{BB} = –43 V	250	—	—	Ω
Protection	Off	R_{BR3}	V_{BB} = –48 V	—	—	20	kΩ
Digital Input/Output	$\overline{BF}$	BFV$_{IH}$	—	2.0	—	—	V
		BFV$_{IL}$	—	—	—	0.8	V
		BFI$_{IH}$	V_{IH} = 2.0 V	–5	0	5	µA
		BFI$_{IL}$	V_{IL} = 0.8 V	–10	1	5	µA
	RDI1	RD1V$_{IH}$	—	2.0	—	—	V
		RD1V$_{IL}$	—	—	—	0.8	V
		RD1I$_{IH}$	V_{IH} = 2.0 V	65	100	170	µA
		RD1I$_{IL}$	V_{IL} = 0.8 V	14	40	70	µA
	RDI2	RD2V$_{IH}$	—	2.0	—	—	V
		RD2V$_{IL}$	—	—	—	0.8	V
		RD2I$_{IH}$	V_{IH} = 2.0 V	65	100	170	µA
		RD2I$_{IL}$	V_{IL} = 0.8 V	14	40	70	µA
	SCN	SCNV$_{OL}$	V_{CC} = 5.25 V I_{OL} = 1.6 mA	—	—	0.4	V
		SCNV$_{OH}$	V_{CC} = 4.75 V I_{OH} = –0.4 mA	2.4	—	—	V
	$\overline{ALM}$	ALMV$_{OL}$	V_{CC} = 5.25 V I_{OL} = 1.6 mA	—	—	0.4	V
		ALMV$_{OH}$	V_{CC} = 4.75 V I_{OH} = –0.4 mA	2.4	—	—	V

AC Characteristics (V_{BB} = –48 V, V_{CC} = 5 V, V_{EE} = –5 V, Ta = 25°C)

Item		Symbol	Test Condition	Input Level (Vrms)	Min	Typ	Max	Unit
Transmission Gain	2 w→4 w	G241	f = 1 kHz	1.16	3.55	3.85	4.15	dB
	4 w→2 w	G421	R_L = 200 Ω	0.921	1.7	2.0	2.3	dB
Attenuation Distortion	2 w→4 w	GF24	f = 3.4 kHz f = 1 kHz	1.16	–0.1	—	0.1	dB
	4 w→2 w	GF42	R_L = 200 Ω	0.921	–0.1	—	0.1	dB
Idle Channel Noise		NI2	R_L = 200 Ω	—	—	—	–81.1	dBmop
		NI4		—	—	—	–81.1	dBmop
S/N	2 w→4 w	SN24	f = 1 kHz	1.16	53	—	—	dB
	4 w→2 w	SN42	R_L = 1.2 Ω	0.921	53	—	—	dB
Impedance Balance		LB2W	f = 3.4 kHz 1 kHz R_L = 1.2 kΩ	0.775	40	—	—	dB
Return Loss		LM1	f = 0.3 kHz R_L = 200 Ω	1.16	20	—	—	dB
Balance Return Loss		LR	f = 3.4 kHz R_L = 1.2 kΩ	0.921	23	—	—	dB
Idle Channel Noise on Alternating Current Induction		NI2AC	R_L = 1.2 kΩ f = 60 Hz IAC = 6.4 mArms	—	—	—	–67	dBmop
PSRR	V_{BB}→2 w	LB2	f = 3.4 kHz	24.5 mVrms	20	—	—	dB
	V_{CC}→2 w	LC2	R_L = 1.2 kΩ	24.5 mVrms	20	—	—	dB
	V_{EE}→2 w	LE2		24.5 mVrms	20	—	—	dB

Digital Input/Output Logic

SCN, ALM Output Logic Truth Table

		Status			
$\overline{BF}$	RL	Ground (Note 1)	Ground Protection (Note 2)	SCN	$\overline{ALM}$
L	On hook	T	T	H	L
			F	H	H
		F	F	L	H
	Off hook	T	T	H	L
			F	H	H
		F	F	H	H
H	On hook	T	T	H	L
			F	L	H
		F	F	L	H
	Off hook	T	T	H	L
			F	L	H
		F	F	L	H

Notes 1 T: Ground/battery short F: No ground/battery short
2 T: Ground protection F: No ground protection

Relay Driver Truth Table

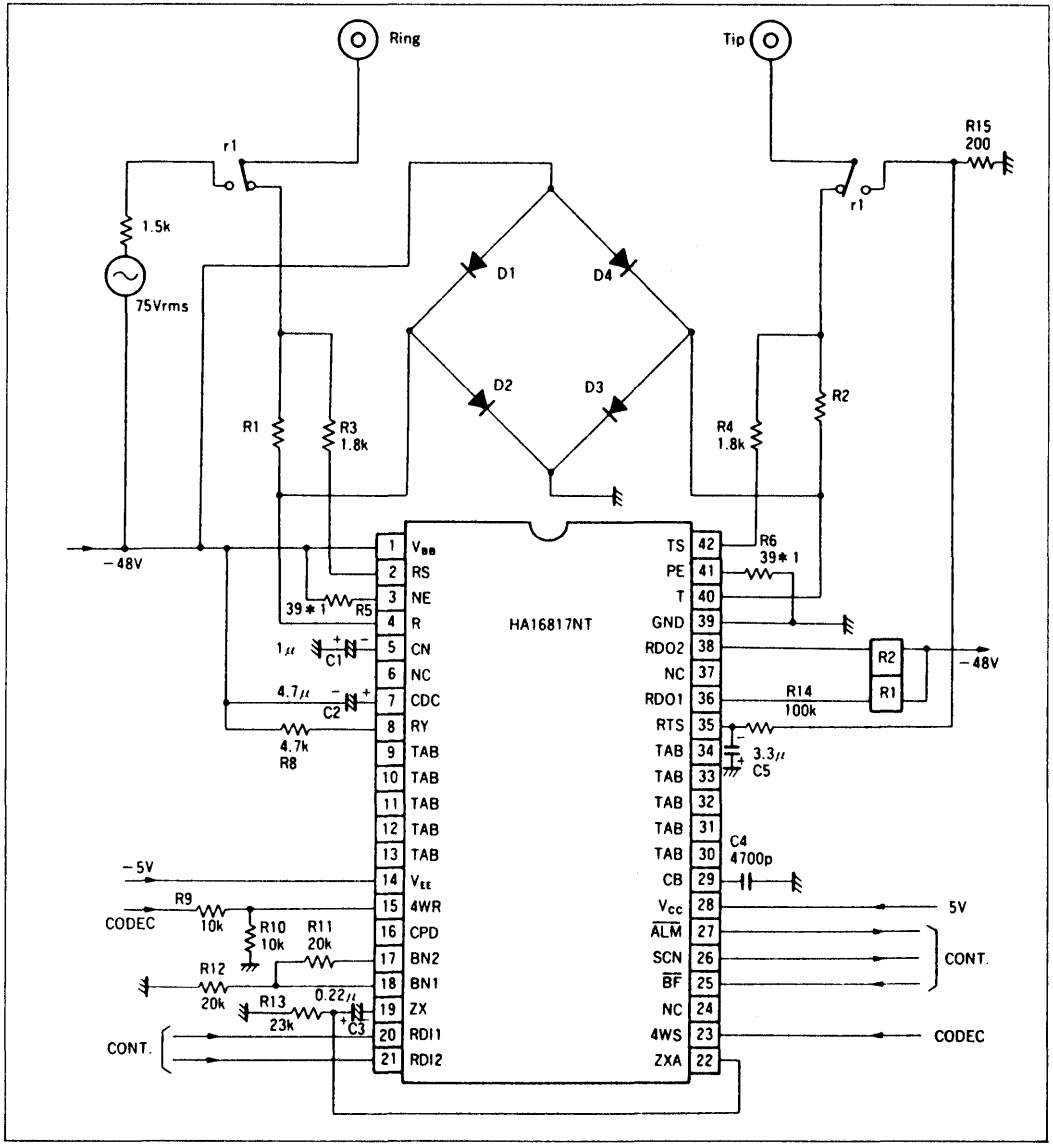
Input		Output	
RDI1	RDI2	RDO1	RDO2
H	—	H(ON)	—
L	—	L(OFF)	—
—	H	—	H(ON)
—	L	—	L(OFF)

BF Truth Table

BF	Battery Feed
H	Battery feed shut down
L	Battery feed

Application Circuit Example

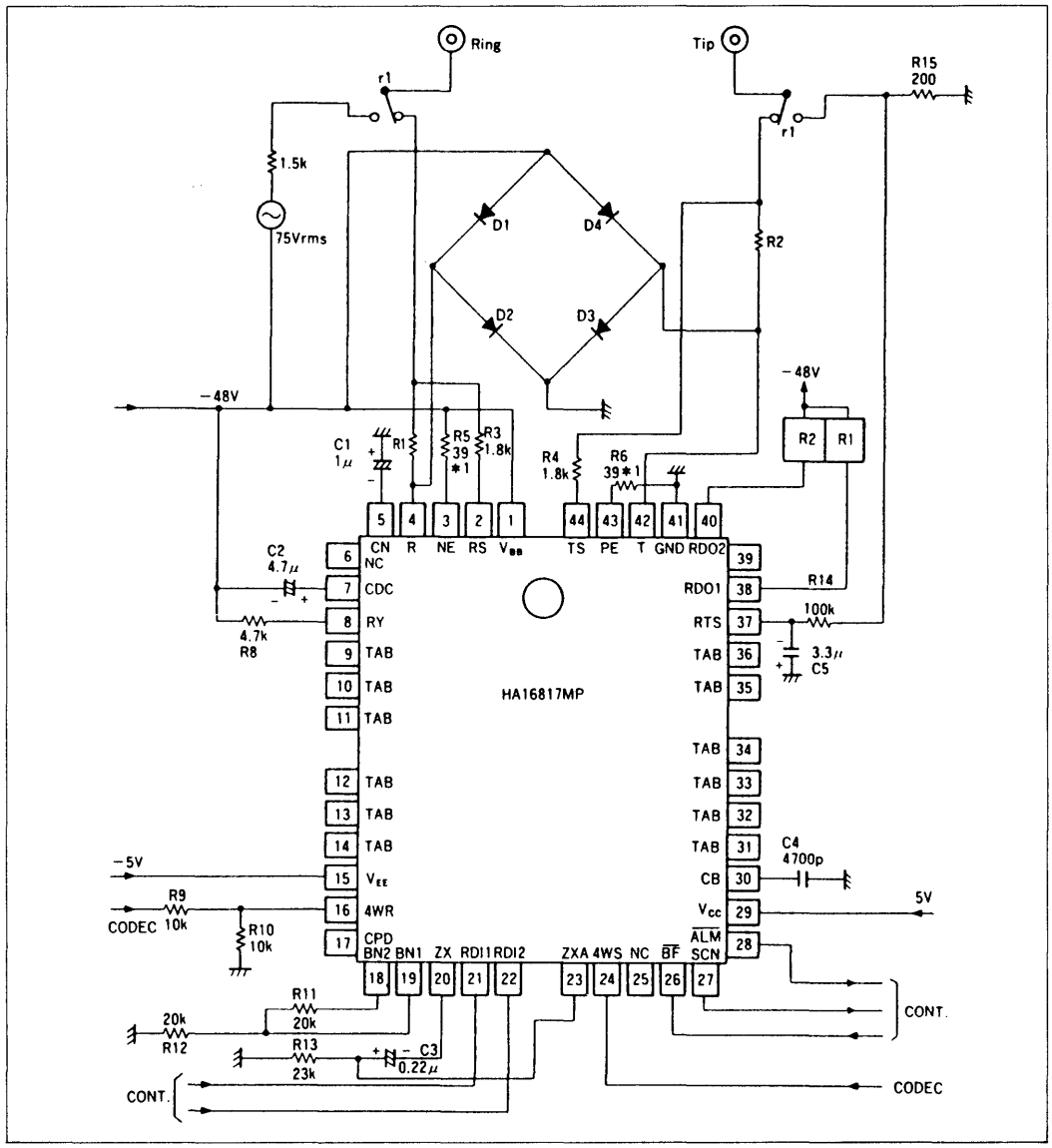
HA16817NT (Input impedance: 600Ω)



Note: Relative precision of these registers should be within ±0.1%

Figure 1

HA16817MP (Input impedance: 600Ω)



Note: Relative precision of these registers should be within ±0.1%

External Connected Components Specification Example

Table 1

Name	Spec	Accuracy	Unit	Power dissipation	Remark	Note
R1	200	5%	Ω	500 mW	For R pin lightning surge protection	1
R2	200	5%	Ω	500 mW	For T pin lightning surge protection	↓
R3	1.8	1%	kΩ	5 mW	For RS pin lightning surge protection	2
R4	1.8	1%	kΩ	5 mW	For TS pin lightning surge protection	↓
R5	39	0.1%	Ω	140 mW		3
R6	39	0.1%	Ω	140 mW		↓
R7	1.5	3%	kΩ	2.9 W	The current during ring-tripping should be considered.	4
R8	4.7	1%	kΩ	0.42 mW		5
R9	10		kΩ	0.08 mW		↓
R10	10		kΩ	0.08 mW		↓
R11	20		kΩ	0.01 mW		↓
R12	20		kΩ	0.01 mW		↓
R13	23		kΩ	0.02 mW		↓
R14	100	5%	kΩ	5.3 mW		
R15	200	3%	Ω	390 mW	The current during ring-tripping should be considered.	4
C1	1	20%	μF	—	(high drive voltage) 60	
C2	4.7	20%	μF	—	15 V	
C3	0.22	10%	μF	—	15 V	6
C4	4700	10%	pF	—	60 V	
C5	3.3	10%	μF	—	60 V	
D1	IFpeak≥1 A	—	A		For R and T pin lightning surge protections	1
D2	↓	—	A			
D3	↓	—	A			
D4	↓	—	A			

Notes

1. R1, R2 are important part in HA16817 Application Circuit because R1, R2 divided the power dissipation between HA16817.
   R1, R2 change the spec. for line feed resistance R_L.

   $Pd = I_L \cdot [V_{BB} - I_L(R1 + R2 + R5 + R6) - I_L R_L]$

   Example
   $50\ \Omega \leq R_L \leq 600\ \Omega \rightarrow R1 = R2 = 300\ \Omega$ (1/2W)
   $600\ \Omega \leq R_L \leq 1200\ \Omega \rightarrow R1 = R2 = 100\ \Omega$ (1/4W)

   1) The resistance should be able to withstand the lightning surge current of 200 V/R1 and 200 V/R2 during lightning surge time ≅ 2 ms.
   2) D1-D4 also should be able to withstand the lightning surge current peak.

2. The resistance should be able to withstand lightning surge current of 117 mA during surge time ≅ 2 ms.

3. When high-speed, large amplitude (more than around 7 Vo-p) impulse noise is input to the tip and ring pins, peak current 150 mA (max), flows through the resistor.

4. Delay time for relay switching must be considered when ring tripping.
   Trip delay depends on the time constant of the external filter. In this case, the estimated time is around 300 ms (max).

   Current for ring trip = (V_{BB} + VRinging) / (R7 + R15)

	R7	R15
Power dissipation when tripping	8 W	1.1 W

5. These resistances are inserted to the pass which is only for audio signals. Therefore, the level of the

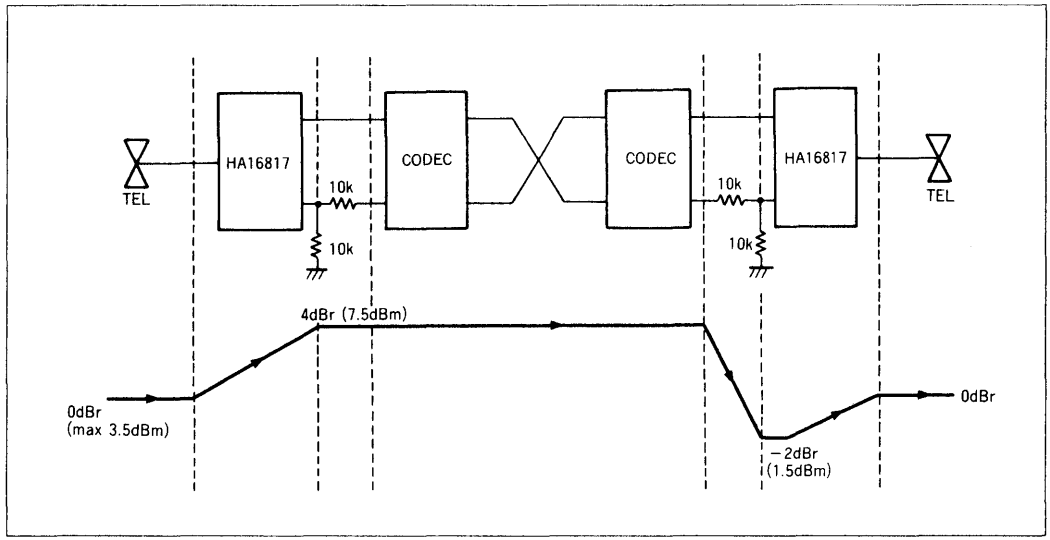


Figure 2

audio signals should be considered in power dissipation calculations. The power dissipation in the above table is calculated according to the assumed level diagram shown below.
The 4 WR to BN 2 gain is 0dB (BN 1 is a buffer amp input pin).

6. These values have a great effect on return loss and balance return loss. Therefore, capacitors whose temperature coefficients are high, such as layer-built ceramic capacitors, are not adequate for this circuit. At the ZX pin, DC0 volts appears when the hook status is "On" and –8 volts appears when the status is "Off". Verify polarity when using tantalum capacitors and the like.

Direct Current Feed

Direct current feed characteristics separate into a characteristic in a fixed current feed area and a characteristic in a fixed resistance feed area. In the fixed current feed area, the current is fed constantly by any supply voltage (V_{BB}) and line resistance. In the fixed resistance area, on the other hand, the current feed depends on the values of power supply and line resistance. The values can be obtained with the following formula.

$$I_L = |V_{BB}|/(R_L+Rf)\ (A)$$

Rf means feed resistance and is 800 Ω ± 10%.
(2x400 Ω)

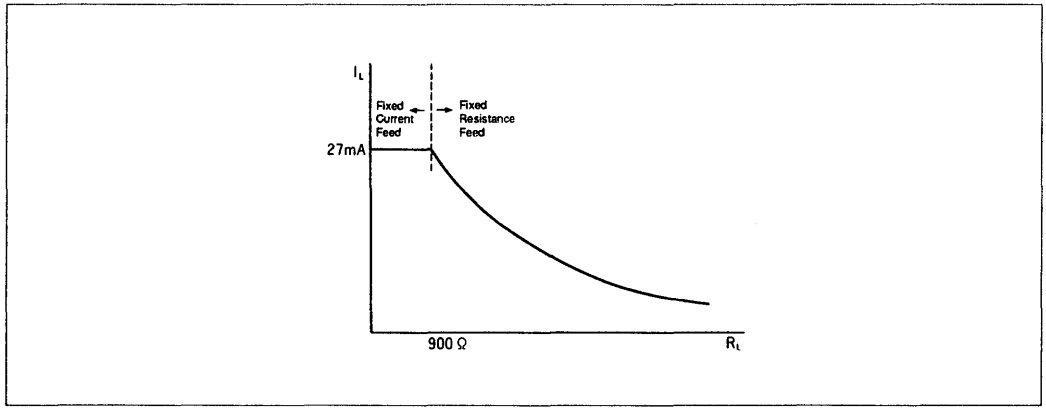


Figure 3

Termination Impedance Setting

By selecting an adequate external impedance, a termination impedance can be set at the required value. When the impedance of the Zx pin to GND is denoted Zx, termination impedance Z_T is obtained with the following formula.

$Z_T = Z_X/K$ HA16817 K = 38.7
HA16817A K = 75.8

Be sure to insert Cx, since it is also a coupling capacitor between Zx and Z_{XA} and cannot be omitted.

When using Cx only for DC out, the capacitance should be selected so that the impedance in the speech band is much lower than the termination impedance. Normally, around 0.1 μF is adequate. At the ZX pin, DC0 volts appears when the hook status is "On" and -8 volts appears when the status is "Off". Verify polarity when using electrolytic capacitors and the like.

Table 2 shows the specifications of termination impedance and external circuit constants for three countries excerpted from the CCITT Recommendation.

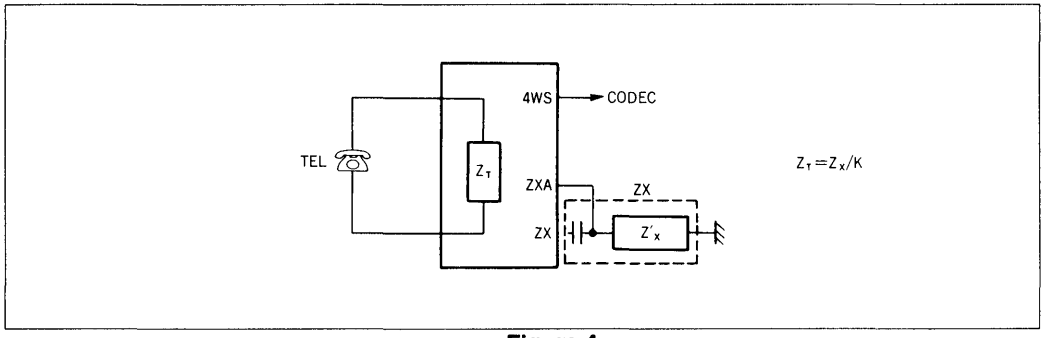


Figure 4

Table 2 Termination Impedance and External Circuit

No.	1	2
ZT	1μF, 600Ω	820Ω, 260Ω, 0.18μF
ZX of HA16817A	ZXA, ZX, 45.5kΩ, 0.013μF	62kΩ, 20kΩ, ZXA, ZX, 2400pF, 0.1μF
ZX of HA16817	ZXA, ZX, 23.2kΩ, 0.026μF	32kΩ, 10kΩ, ZXA, ZX, 4700pF, 0.22μF

$Z_T = 600\Omega + 1/(j\omega \times 1\mu F)$
$Z_X = K \times Z_T = K \times 600\Omega + 1/(j\omega \times 1\mu F/K)$

Balancing Network Setting

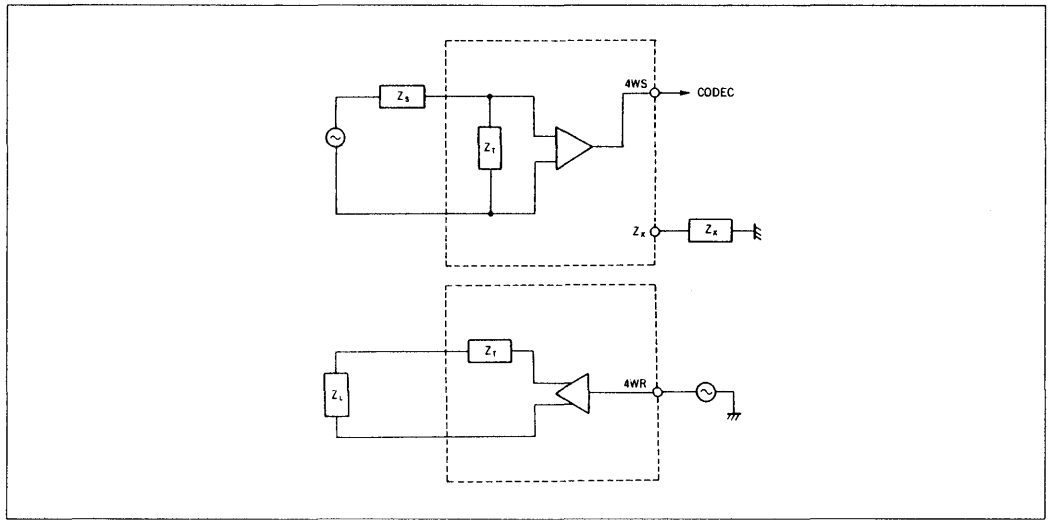
The 4 W to 4 W transfer function is

$G44 = 4\,[Z_{BN} / (Z_{BN} + Z_{XO}) - Z_T / (Z_L + Z_T)]$.

Therefore, when $Z_L = Z_T$, the formula becomes

$G44 = 4\,[Z_{BN} / (Z_{BN} + Z_{XO}) - 1/2]$.

$G44 \fallingdotseq 0$ can be obtained when $Z_{BN} = Z_{XO}$.



Level Diagram

The 2 W-4 W transmission gain formula is

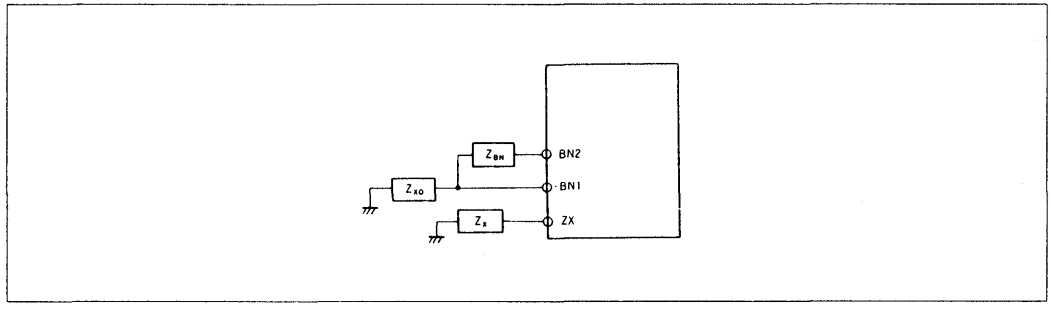
$G24 = 20 \log |2\,Z_T / (Z_S + Z_T)| + 3.85\ (\pm 0.3)$ (dB)

The 4 W-2 W transmission gain formula is

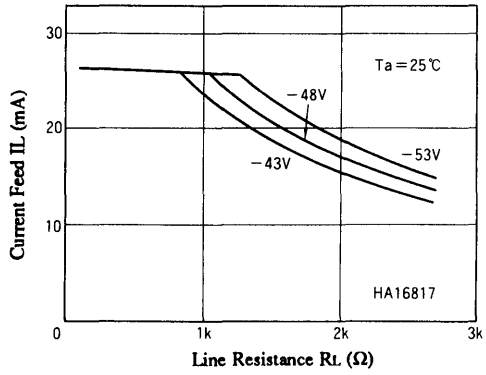
$G42 = 20 \log |2\,Z_T / (Z_S + Z_T)| + 2.0\ (\pm 0.3)$ (dB)

Therefore, when $Z_T = Z_L = Z_S$, the following formulas are obtained.

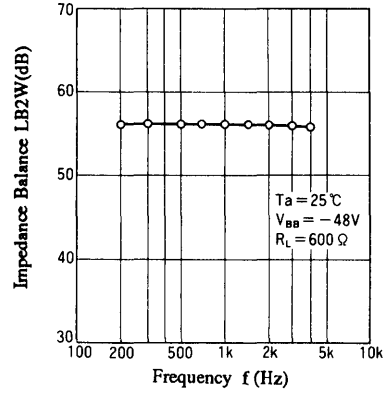
	HA16817	HA16817A	
G24	3.85 ±0.3	6.00 ±0.3	dB
G42	2.00 ±0.3	2.00 ±0.3	dB



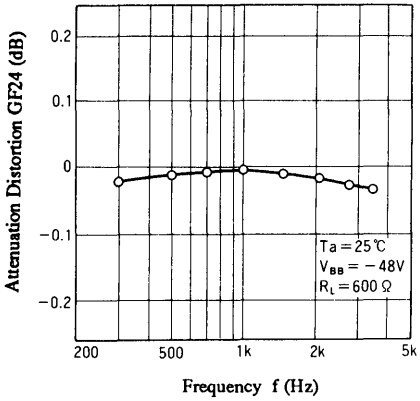
Current Feed vs. Line Resistance characteristics



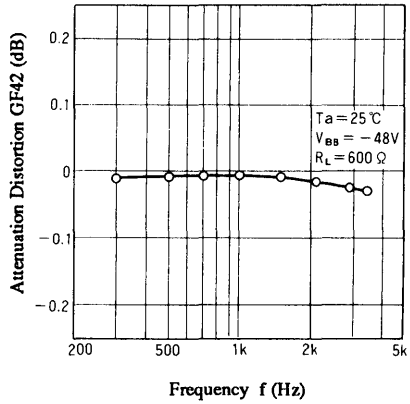
Impedance Balance vs. Frequency Characteristics



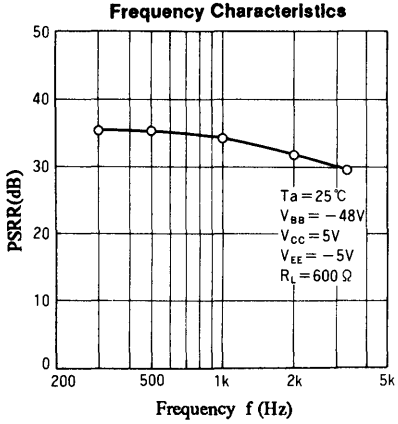
Attenuation Distortion vs. Frequency (2W→ 4W) Characteristics



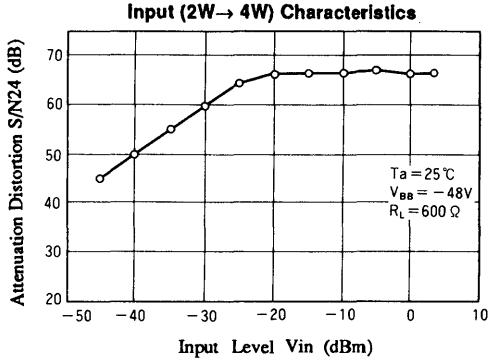
Attenuation Distortion vs. Frequency (4W→ 2W) Characteristics



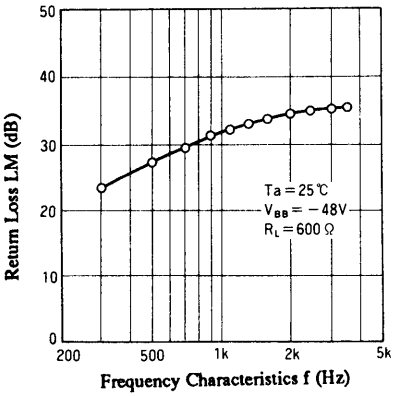
PSRR (VBB) vs. Frequency Characteristics



Attenuation Distortion vs. Input (2W→ 4W) Characteristics



Return Loss vs. Frequency Characteristics



Section Four

Devices for Serial Communication Applications

The absolute maximum ratings referenced in the data sheet sections of this manual are limiting values, to be applied individually and beyond which operation of the described circuits may be impaired. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the circuit's reliability.

The "Electrical Characteristics" of the circuits described in this manual are for reference only.

HD64180S (NPU)

Network Processing Unit (NPU)
CMOS 8-bit Microprocessor for Communications Applications

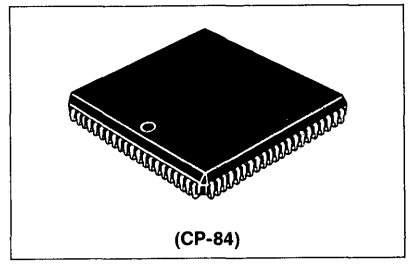
Description

The HD64180S Network Processing Unit (NPU) provides multi-purpose high-speed communication control functions on a single LSI chip. The HD64180S allows efficient, high-performance communication protocol and user application processing at a low cost.

Built-in features of the HD64180S include an 8-bit CPU, a 2-channel serial interface (MSCI, ASCI/CSIO), a DMAC with 2-channel chained block transfer capabilities, and a timer. The MSCI provides asynchronous, byte synchronous, and bit synchronous communication modes, and enables serial communications using protocols such as HDLC. The built-in features of the HD64180S allow it to control communication using various protocols as well as application processing. In distributed environments, communication throughput can be increased by eliminating the need for the main processor to do communication processing.

The built-in features of the HD64180S also make it flexible. Applications range from a communication subsystem processor for inter-computer links or an ISDN protocol processor to a controller in a distributed control system for industrial robots.

In addition, the HD64180S is designed to interface with conventional communication LSIs and to be compatible with existing communication software. It can be used with almost any type of communication system.



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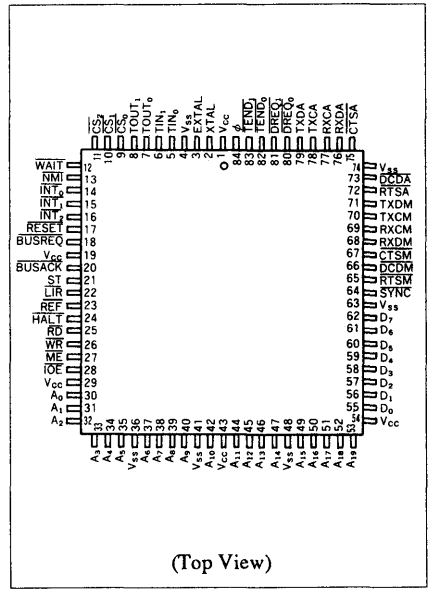
*For details about HD64180S specifications, please refer to "HD64180S NPU Hardware Manual" (Order Number M21T022).

Pin Arrangement



(Top View)

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Characteristics

Item	Specifications
CPU	• Software compatible with HD64180Z • 80 type bus interface • On-chip MMU (1 Mbyte physical address space)
DMAC	• 2 channels • DMA transfer between memory and memory, memory and I/O (memory-mapped I/O), and memory and MSCI • Chained-block transfer between memory and MSCI • Internal interrupt requests av ailable
Multiprotocol serial communications interface (MSCI)	• Full duplex channel • Asynchronous, byte synchronous (mono-, Bi-, or external synchronous), or bit synchronous (HDLC or loop) selectable • Transmit/receive control using modem control signals ($\overline{\text{RTSM}}$, $\overline{\text{CTSM}}$, and $\overline{\text{DCDM}}$) • Internal Advanced Digital PLL (ADPLL) clock extraction receive data and/or receive clock noise suppression • On-chip baud rate generator • Internal interrupt requests available • Maximum transfer rate 7.1 Mbps (with 10 MHz clock)
Asynchronous serial communications interface/clocked serial I/O port (ASCI/CSIO)	• Full duplex channel • Asynchronous or clocked serial mode (selectable) • Transmit/receive control using modem control signals ($\overline{\text{RTSA}}$, $\overline{\text{CTSA}}$, and $\overline{\text{DCDA}}$) • On-chip baud rate generator • Internal interrupt requests available
Timers	• 2 channels • 8-bit reloadable up-counter • Output waveform generator and external event count functions • Internal interrupt requests available
Interrupt controller	• Four external interrupt lines ($\overline{\text{NMI}}$, $\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$, and $\overline{\text{INT}}_2$) • Fifteen internal interrupt sources
Memory access support function	• Internal refresh controller • Internal wait state controller • Internal chip-select controller
Other functions	• On-chip clock oscillator circuit • Low power dissipation modes (sleep and system stop)

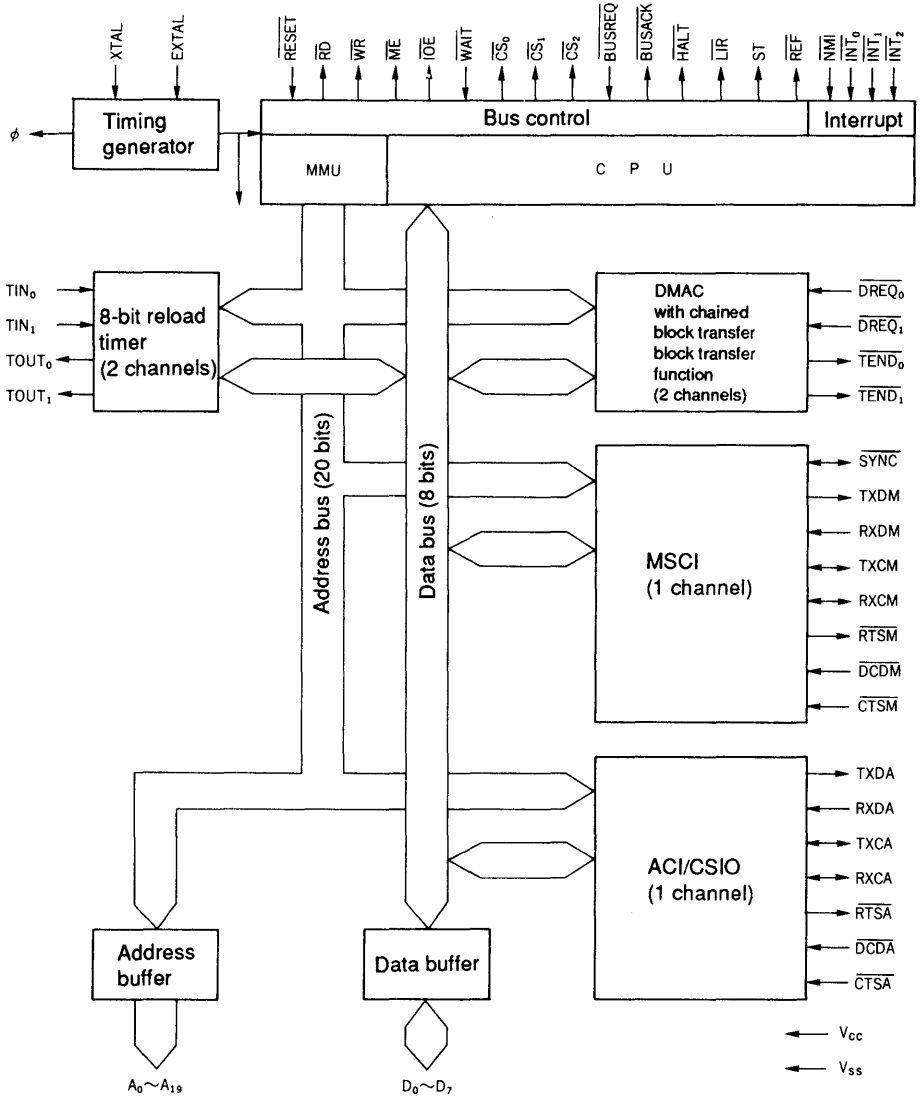
Ordering Information

Product Name	Max Operating Frequency	Package
HD64180SCP6	6 MHz	CP-84 (84-pin PLCC)
HD64180SCP8	8 MHz	
HD64180SCP10	10 MHz	

Signal Functions

Type	Mnemonic	I/O	Function
Power Supply	Vcc	I	Power supply
	Vss	I	Ground
Clock	XTAL	I	Crystal
	EXTAL	I	External clock
	ø	O	System clock
Reset	$\overline{\text{RESET}}$	I	Reset
Address Bus	$A_0 - A_{19}$	O	Address bus
Data Bus	$D_0 - D_7$	I/O	Data bus
Memory I/O	$\overline{\text{RD}}$	O	Read
Interface	$\overline{\text{WR}}$	O	Write
	$\overline{\text{ME}}$	O	Memory enable
	$\overline{\text{IOE}}$	O	I/O enable
	$\overline{\text{WAIT}}$	I	Wait request
	$\overline{\text{CS}_0} - \overline{\text{CS}_2}$	O	Programmable chip-select
System Control	$\overline{\text{BUSREQ}}$	I	Bus request
	$\overline{\text{BUSACK}}$	O	Bus request acknowledge
	$\overline{\text{HALT}}$	O	Halt
	$\overline{\text{LIR}}$	O	Opcode fetch
	ST	O	Status
	$\overline{\text{REF}}$	O	Refresh
Interrupt Control	$\overline{\text{NMI}}$	I	Non-maskable interrupt
	$\overline{\text{INT}_0} - \overline{\text{INT}_2}$	I	Interrupt request
DMAC	$\overline{\text{DREQ}_0}$, $\overline{\text{DREQ}_1}$	I	DMA request (channel 0, 1)
	$\overline{\text{TEND}_0}$, $\overline{\text{TEND}_1}$	O	DMA end (channel 0, 1)
MSCI	TXDM	O	Transmit data
	RXDM	I	Receive data
	TXCM	I/O	Transmit clock
	RXCM	I/O	Receive clock
	$\overline{\text{RTSM}}$	O	Modem control
	$\overline{\text{DCDM}}$	I	
	$\overline{\text{CTSM}}$	I	
	$\overline{\text{SYNC}}$	I/O	Synchronization
ASCI/CSIO	TXDA	O	Transmit data
	RXDA	I	Receive data
	TXCA	I/O	Transmit clock
	RXCA	I/O	Receive clock
	$\overline{\text{RTSA}}$	O	Modem control
	$\overline{\text{DCDA}}$	I	
	$\overline{\text{CTSA}}$	I	
Timer	TIN_0, TIN_1	I	Event input (channel 0, 1)
	TOUT_0, TOUT_1	O	Timer output (channel 0, 1)

Block Diagram



HD64570 (SCA)

Serial Communications Adapter

Description

The HD64570 Serial Communications Adapter (hereinafter referred to as SCA) is a high-speed, high-performance data communication controller providing efficient, high-performance communication protocol processing at low cost.

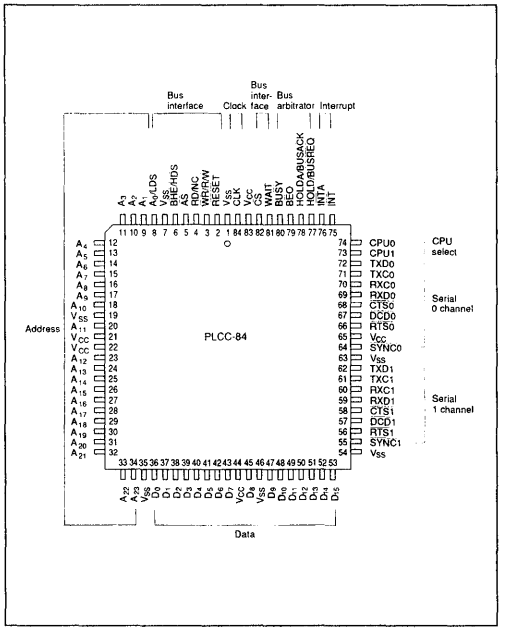
The SCA incorporates powerful key functions such as a two-channel multiprotocol serial communications interface (MSCI), a four-channel direct memory access controller (DMA controller) with chained-block transfer function, and a four-channel timer. The built-in MSCI, supporting various communication protocol modes such as asynchronous, byte synchronous, and bit synchronous modes, allows serial communications using protocols such as HDLC. In addition, the SCA supports four types of 8/16-bit bus interfaces, allowing a direct interface with the host MPU. This bus interface capability combined with 32-byte deep receive and transmit FIFOs in the MSCI can provide high throughput for many communication systems. Accordingly, the SCA can be widely adopted to a computer communication controller that requires multi-channel serial communications, PBXs, and office automation equipment such as personal computers and facsimiles.

*For details about HD64570 specifications, please refer to "HD64570 SCA User's Manual" (Order Number M50T007).

SCA Features

- Multiprotocol Serial Communications Interface (MSCI)
  - —Two full duplex channels
  - —Asynchronous, byte synchronous (mono-sync, bi-sync, or external synchronous), or bit synchronous (HDLC or loop) modes
  - —32-byte deep for both receive and transmit buffers
  - —Transmission and reception control using modem control signals ($\overline{RTS}$, $\overline{CTS}$, and $\overline{DCD}$)
  - —Advanced digital PLL (ADPLL) function
    - —Clock extraction
    - —Noise suppression for receive data and receive clock
  - —Baud rate generator
  - —Interrupt request
  - —Maximum transfer rate: 7.1 Mbps (f = 10 MHz)
- Direct Memory Access Controller (DMA Controller)
  - —Four channels
  - —DMA transfer between memory and built-in MSCI
  - —Chained block transfer in bit synchronous mode
  - —Programmable channel priority
  - —Programmable bus release and channel switch conditions
- Timer
  - —Four channels
  - —16-bit reloadable upcounter timer
  - —Interrupt request
- Wait State Controller
  - —Wait state control using an external pin or software
- Interrupt Controller
  - —Interrupt request to the MPU
  - —20 interrupt sources
  - —Programmable acknowledge cycle
- Bus Arbitrator
  - —Bus arbitrator between the built-in DMA controller and external bus masters
  - —Multiple serial channels realized by daisy chain structure
- Bus Interface
  - —HD641016, HD64180, and other two other types of 16-bit bus interfaces available by mode switching through external pins
  - —8-bit or 16-bit programmable bus width
  - —Byte swap function
  - —16 Mbytes of address space
- Maximum operation frequency
  - —10 MHz
- Package
  - —CP-84 (84-pin PLCC)

SCA Pin Arrangement



The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Table 2-1 CP-84 Pin Configuration

Pin No.	Pin Name CPU Mode 0	CPU Mode 1	CPU Mode 2	CPU Mode 3	Pin No.	Pin Name CPU Mode 0	CPU Mode 1	CPU Mode 2	CPU Mode 3
1	V_{SS}				43	D_7			
2	$\overline{RESET}$				44	V_{CC}			
3	$\overline{WR}$	$\overline{WR}$	R/$\overline{W}$	R/$\overline{W}$	45	D_8			
4	$\overline{RD}$	$\overline{RD}$	N.C.	N.C.	46	V_{SS}			
5	$\overline{AS}$				47	D_9			
6	$\overline{BHE}$	N.C.	$\overline{HDS}$	$\overline{HDS}$	48	D_{10}			
7	V_{SS}				49	D_{11}			
8	A_0	A_0	$\overline{LDS}$	$\overline{LDS}$	50	D_{12}			
9	A_1				51	D_{13}			
10	A_2				52	D_{14}			
11	A_3				53	D_{15}			
12	A_4				54	V_{SS}			
13	A_5				55	$\overline{SYNC1}$			
14	A_6				56	$\overline{RTS1}$			
15	A_7				57	$\overline{DCD1}$			
16	A_8				58	$\overline{CTS1}$			
17	A_9				59	RxD1			
18	A_{10}				60	RxC1			
19	V_{SS}				61	TxC1			
20	A_{11}				62	TxD1			
21	V_{CC}				63	V_{SS}			
22	V_{CC}				64	$\overline{SYNC0}$			
23	A_{12}				65	V_{CC}			
24	A_{13}				66	$\overline{RTS0}$			
25	A_{14}				67	$\overline{DCD0}$			
26	A_{15}				68	$\overline{CTS0}$			
27	A_{16}				69	RxD0			
28	A_{17}				70	RxC0			
29	A_{18}				71	TxC0			
30	A_{19}				72	TxD0			
31	A_{20}				73	CPU1			
32	A_{21}				74	CPU0			
33	A_{22}				75	$\overline{INT}$			
34	A_{23}				76	$\overline{INTA}$			
35	V_{SS}				77	HOLD	$\overline{BUSREQ}$	$\overline{BUSREQ}$	$\overline{BUSREQ}$
36	D_0				78	HOLDA			
37	D_1				79	$\overline{BEO}$			
38	D_2				80	$\overline{BUSY}$			
39	D_3				81	WAIT			
40	D_4				82	$\overline{CS}$			
41	D_5				83	V_{CC}			
42	D_6				84	CLK			

Note: Refer to section 2.2, Pin Functions, for details on CPU modes.

2.2 Pin Functions

The SCA pin functions are summarized in table 2-2.

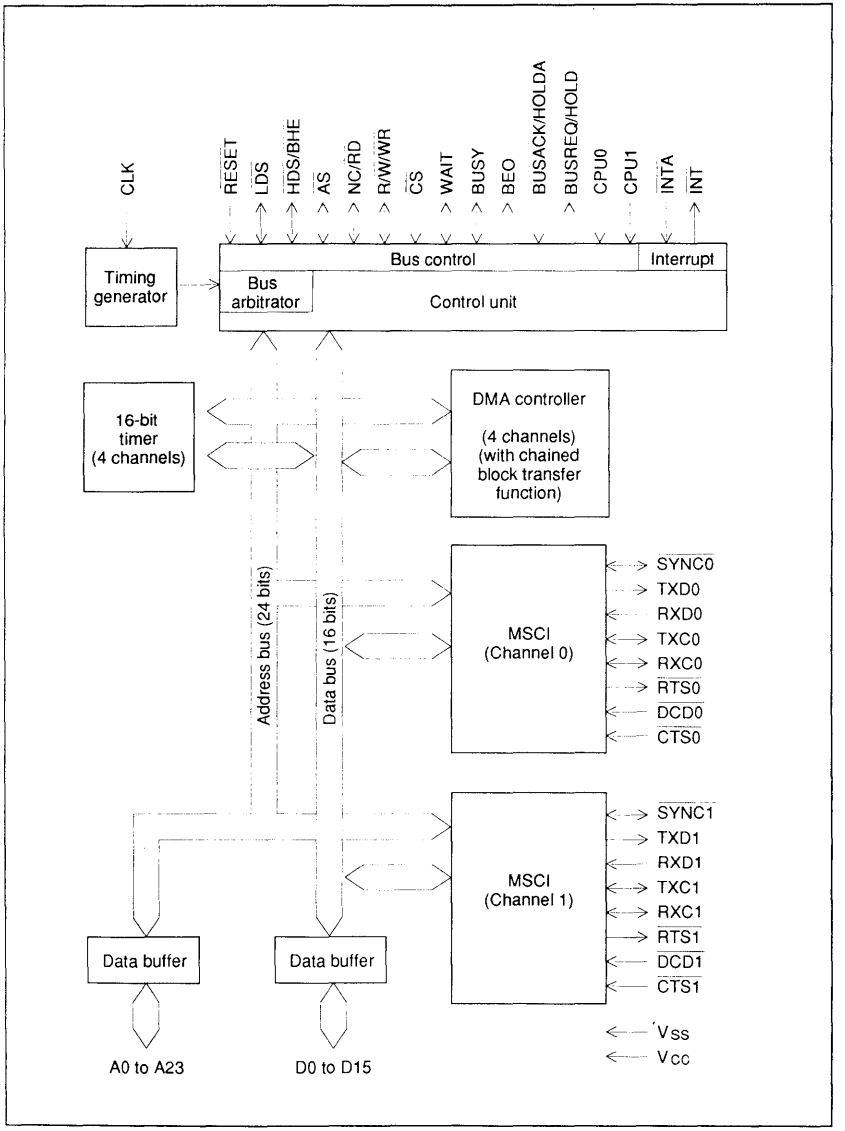
Table 2-2 SCA Pin Functions

Type	Symbol	I/O	Function
Power supply	V_{CC}	I	Power supply
	V_{SS}	I	Ground
Clock	CLK	I	System clock
Reset	$\overline{RESET}$	I	Reset
Address bus	A_0 to A_7	I/O	Address bus
	A_8 to A_{23}	O	Address bus
Address bus	D_0 to D_{15}	I/O	Data bus
Bus interface	$\overline{RD}$	I/O	Read
	$\overline{WR}$	I/O	Write
	R/$\overline{W}$	I/O	Read/write
	$\overline{HDS}$	I/O	Higher data strobe
	$\overline{LDS}$	I/O	Lower data strobe
	$\overline{BHE}$	I/O	Higher byte access strobe
	WAIT	I/O	Wait request
	$\overline{CS}$	I	Chip select
	$\overline{AS}$	I/O	Address strobe
System control	$\overline{BUSREQ}$	O	Bus request
	$\overline{BUSACK}$	I	Bus request acknowledge
	HOLD	O	Hold request
	HOLDA	I	Hold request acknowledge
	$\overline{BEO}$	O	Bus enable
	$\overline{BUSY}$	I/O	Bus busy
	CPU0, CPU1	I	Bus interface mode selection (Refer to table 2-3.)
Interrupt	$\overline{INT}$	O	Interrupt request
	$\overline{INTA}$	I	Interrupt request acknowledge
MSCI	TXD0, TXD1	O	Transmit data
	RXD0, RXD1	I	Receive data
	TXC0, TXC1	I/O	Transmit clock
	RXC0, RXC1	I/O	Receive clock
	$\overline{RTS0}$, $\overline{RTS1}$	O	Modem control ($\overline{RTS}$)
	$\overline{DCD0}$, $\overline{DCD1}$	I	Modem control ($\overline{DCD}$)
	$\overline{CTS0}$, $\overline{CTS1}$	I	Modem control ($\overline{CTS}$)
	$\overline{SYNC0}$, $\overline{SYNC1}$	I/O	Synchronization

Table 2-3 CPU Mode (Bus Interface Mode) Selection by CPU0 and CPU1

CPU0	CPU1	CPU Mode
0	0	Mode 0 (80 series 16-bit CPU)
0	1	Mode 1 (HD64180)
1	0	Mode 2 (HD641016)
1	1	Mode 3 (68 series 16-bit CPU)

SCA Block Diagram



Section Five

Devices for Fiber Optic Transmission GaAs Optical Transmission Components

The absolute maximum ratings referenced in the data sheet sections of this manual are limiting values, to be applied individually and beyond which operation of the described circuits may be impaired. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the circuit's reliability.

The "Electrical Characteristics" of the circuits described in this manual are for reference only.

HA29001

Preliminary

GaAs IC/Laser Diode Driver for Optical Communication

This HA29001 is a Laser Diode Driver for Fiber Optic System.

Features

- Driving Current; 50mA
- Output Signal Rise/Fall time; 100ps
- Single power supply of -5.2V
- 14 pin package

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply Voltage	V_{ss}	-7.5 to +0.5	V	
Input Voltage	V_{in}	V_{SS} to 0	V	
Supply Current	I_{ss}	~ 150	mA	
Storage Temperature	T_{stg}	-55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

5

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage	V_{ss}	-5.46	-5.2	-4.94	V	
Operating Temperature	T_a	0		+65	°C	
Input Reference Voltage	V_{ref}		-1.3		V	
Input Voltage	V_{in}	0.4		1.1	V_{p-p}	Capacitor Coupled

DC Characteristics (V_{ss}: -5.2V +/-5%)

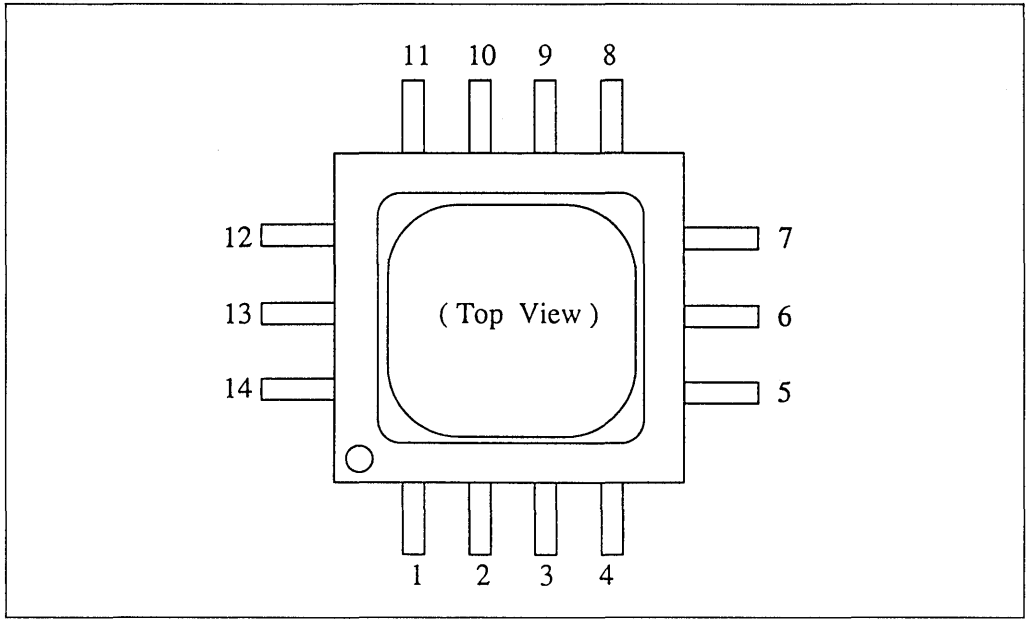
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Signal Current	I_s	See Test Circuit		50	80	mA
Bias Current	I_b	See Test Circuit		50	80	mA
Supply Current	I_{ss}			40		mA

AC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Signal Current Rise Time	tr*	Ib = 50 mA		100	150	ps
Signal Current Fall Time	tf*	Ib = 50 mA		100	150	ps

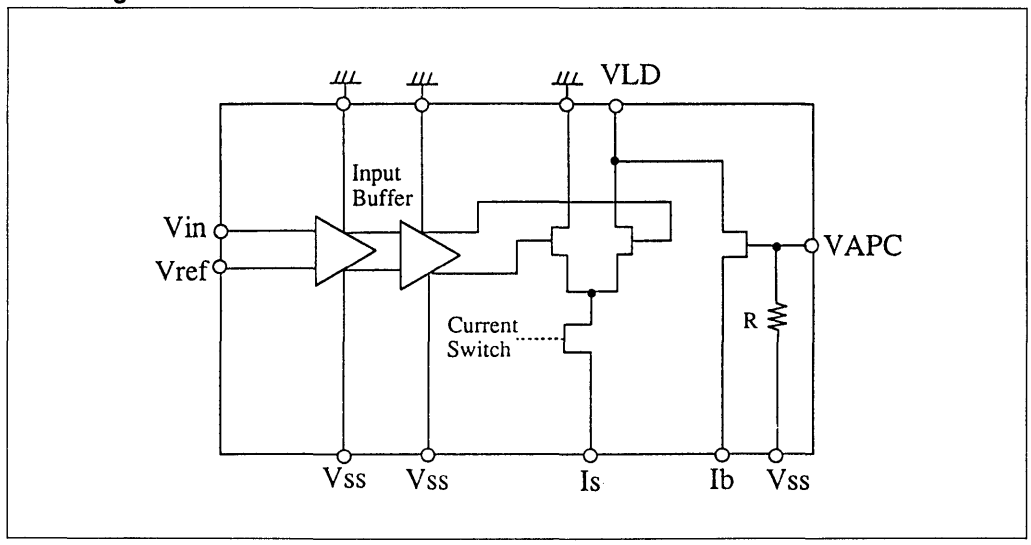
*10% to 90%

Package



Pin #	Symbol	Function
1	N/C	No Connection
2	N/C	No Connection
3	VLD	LD Connection
4	VLD	LD Connection
5	VAPC	APC
6	Ib	Bias Current Out
7	Is	Signal Current Out
8	GND	GND
9	GND	GND
10	GND	GND
11	V_{ref}	ECL Reference Voltage
12	N/C	No Connection
13	V_{in}	Signal Input
14	V_{ss}	Voltage Source

Block Diagram



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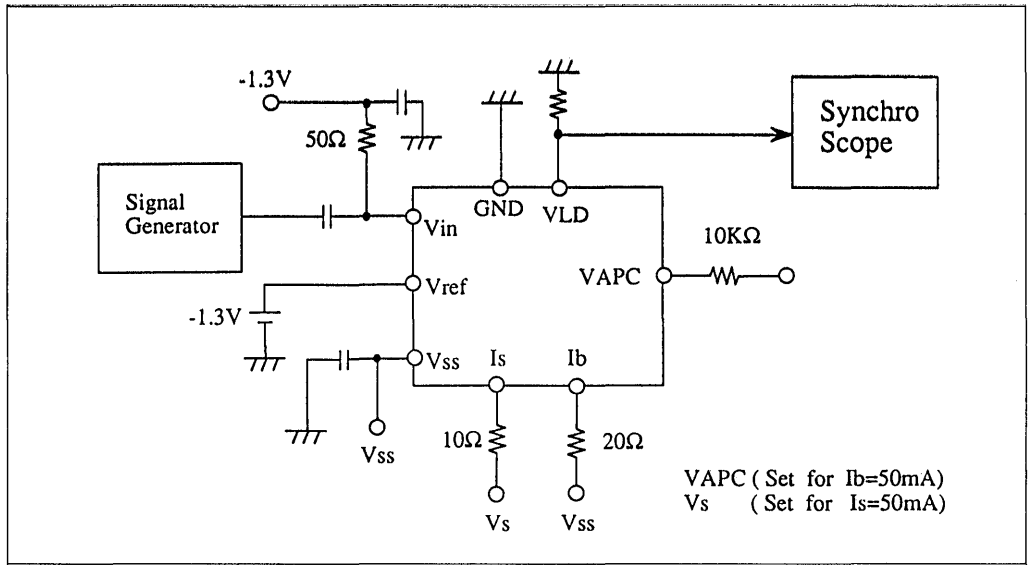
AC Measurement Circuit



PHS6902

Preliminary

4 to 1 Multiplexer GaAs IC for Optical Transmission

The PHS6902 is a 4 to 1 Multiplexer GaAs IC for Optical Transmission systems.

Features

- 4 to 1 Multiplexer with on-chip clock synchronization circuitry
- Clock speed 2.4 GHz
- ECL compatible I/O's
- Single Power Supply of –5.2 V
- 32 pin package containing internal decoupling capacitors.

5

Absolute Maximum Ratings

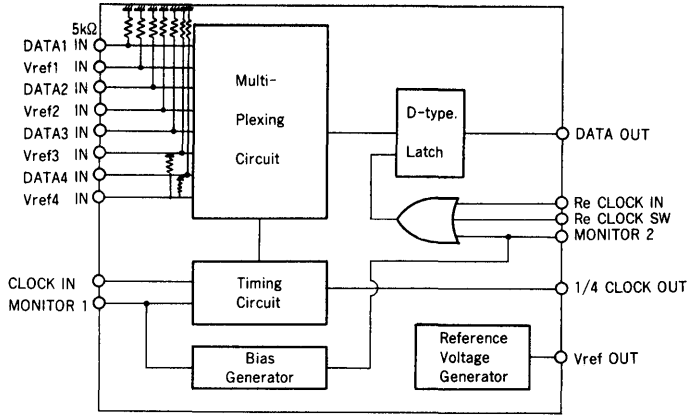
Item	Symbol	Ratings	Unit	Remarks
Supply Voltage	Vss (+)	+0.5	V	
	Vss (–)	–7.0		
Input Voltage	V_{IH}	0	V	
	V_{IL}	Vss		
Supply Current	Iss	500	mA	
Output Current	Io	50	mA	
Power Dissipation	P_D	2.5	W	
Operating Temparature	Ta	–10 to +80	°C	
Storage Temparature	Tstg	–65 to +150	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

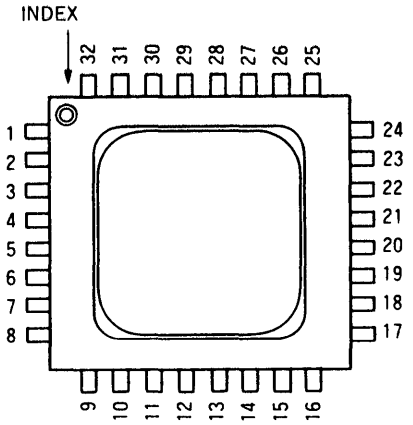
Recommended Operational Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Supply Voltage	Vss	–5.46	–5.20	–4.94	V	
Input Voltage	V_{IH}	–1.1		–0.8	V	
	V_{IL}	–1.8		–1.6		
Output termination Voltage	V_{TT}		–2.0		V	
Input reference Voltage	Vref	–1.386	–1.320	–1.254	V	
Input clock	CKp-p	0.6	0.8	1.2	Vp-p	
Input re-clock	RCKp-p	0.6	0.8	1.2	Vp-p	

Block Diagram



Pin Description



(Top View)

Pin No	Pin Name	Function
1	Monitor 2	Gate Bias Control Pin, Normaly Open
2	GND	GND
3	DATA OUT	Data Out of Moltiplexer
4	GND	GND
5	1/4 Clock out	1/4 Clock Out of Input Clock
6	GND	GND
7	Monitor 1	Gate Bias Control Pin, Normaly Open
8	GND	GND
9	GND	GND
10	Clock In	Clock Input
11	GND	GND
12	GND	GND
13	Vss	–5.2 V Voltage Source Input
14	GND	GND
15	Vref out	Output Pin of ECL Reference Level Voltage
16	GND	GND
17	Data 1 IN	Data 1 INPUT
18	Vref 1 IN	–1.32 V Voltage Source Input
19	Data 2 IN	Data 2 INPUT
20	Vref 2 IN	–1.32 V Voltage Source Input
21	Data 3 IN	Data 3 INPUT
22	Vref 3 IN	–1.32 V Voltage Source Input
23	Data 4 IN	Data 4 INPUT
24	Vref 4 IN	–1.32 V Voltage Source Input

25	GND	GND
26	GND	GND
27	GND	GND
28	GND	GND
29	GND	GND
30	Re Clock IN	Clock input for clock sycronization to DATA OUT
31	Re Clock SW	ON/OFF switch for clock sycronization to DATA OUT
32	GND	GND

Electrical Characteristics

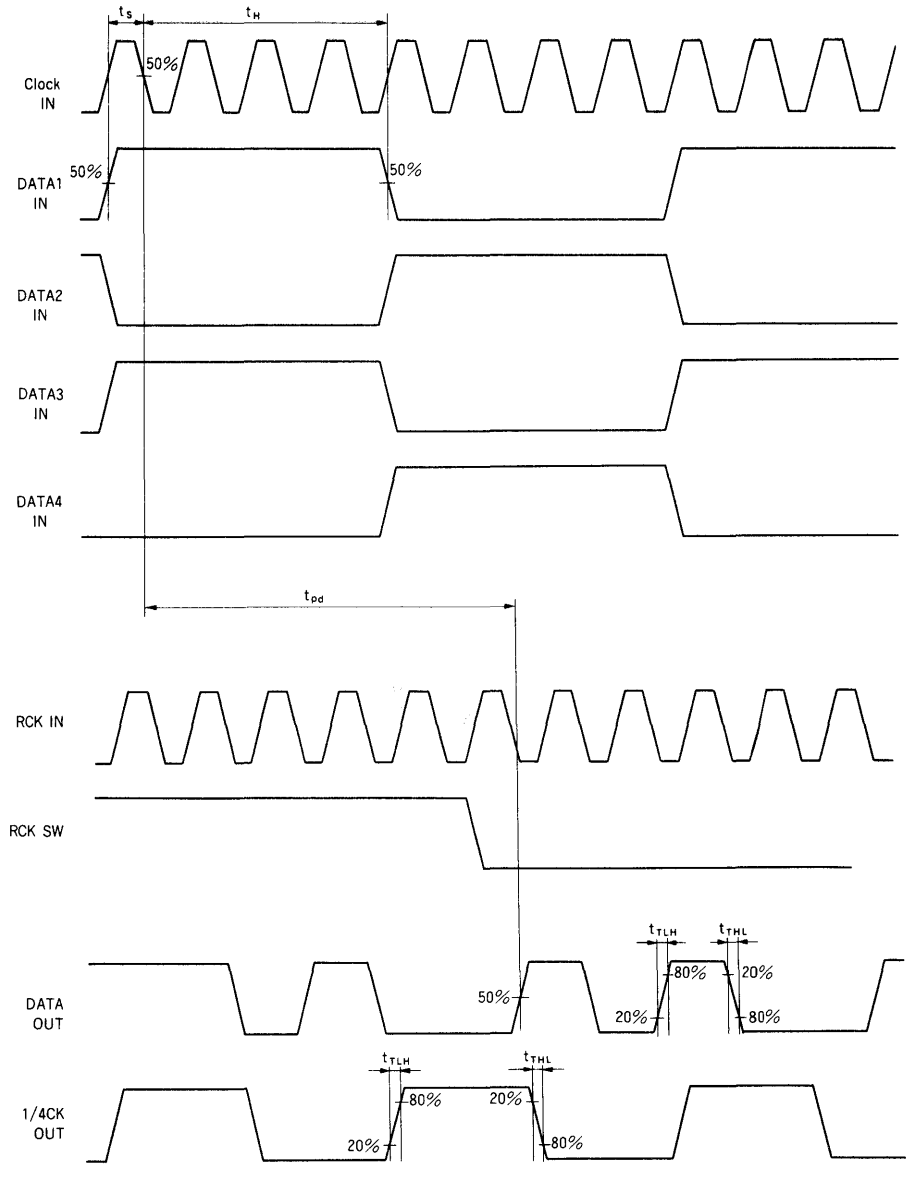
DC Characteristics

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ max, $R_T = 50\ \Omega$	–1.1		–0.8	V
	V_{OL}	$V_{IN} = V_{IL}$ min, $V_{TT} = -2$ V	–1.8		–1.6	
Input Voltage	V_{IH}		–1.1			V
	V_{IL}				–1.5	
Input Current	I_{IH}	$V_{IN} = V_{IH}$ max		160		μA
	I_{IL}	$V_{IN} = V_{IL}$ min		360		
Output Current	I_{OH}	$R_T = 50\Omega$			24	mA
	I_{OL}	$V_{TT} = -2$ V			8	
Supply Current	Iss			300		mA

AC Characteristics

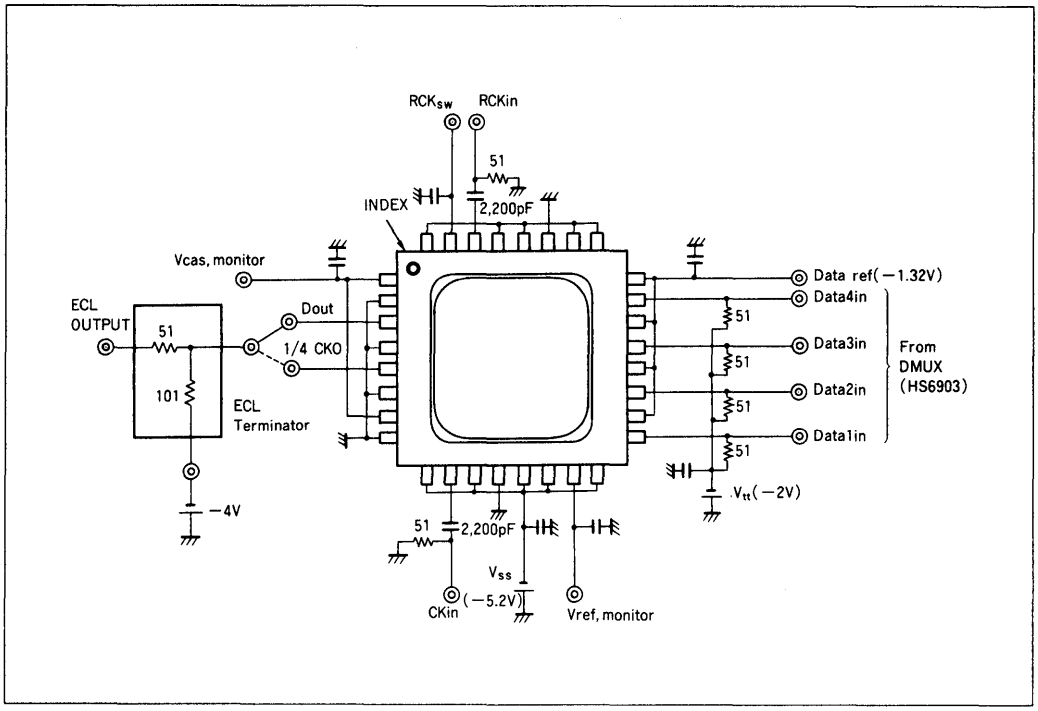
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation delay between clock input and output data	tpd	50% to 50%		1.0		ns
Input data setup time	ts	50% to 50%	0.1			ns
Input data hold time	t_H	50% to 50%	0.1			ns
Clock input rate	fc max		2.4	3.0		GHz
	fe min				0.5	
Output transition time	t_{TLH}	20% to 80%, C_L= 2pF		0.15		ns
	t_{THL}	$R_T = 50\ \Omega$		0.15		

Time chart


t_s
t_H
Clock IN
50%
DATA1 IN
50%
50%
DATA2 IN
DATA3 IN
DATA4 IN
t_{pd}
RCK IN
RCK SW
t_{TLH}
t_{THL}
80%
20%
50%
20%
80%
DATA OUT
t_{TLH}
t_{THL}
80%
20%
20%
80%
1/4CK OUT

5

Test Circuit



Mechanical Drawings

Item	Content
Outward Form	12 x 12 x 3.35 t (mm) quad leaded chip carrier
Pin Count	32
Pin Pitch	1.27 (mm)
Characteristic Impedance of Signal Line	50 ± 5 (Ω)
Noise Decoupling Chip Capacitors	located in package
Thermal Resistance	20 (°C/W) with Fin at natural convection

PHS6903

Preliminary

1 to 4 Demultiplexer GaAs IC for Optical Transmission

The PHS6903 is a 1 to 4 Demultiplexer GaAs IC for Optical Transmission systems.

Features

- 1 to 4 Demultiplexer with on-chip clock synchronization circuitry
- Clock input 2.4 GHz
- ECL compatible I/O's
- Single Power Supply of –5.2 V
- 32 pin package containing internal decoupling capacitors

Absolute Maximum Ratings

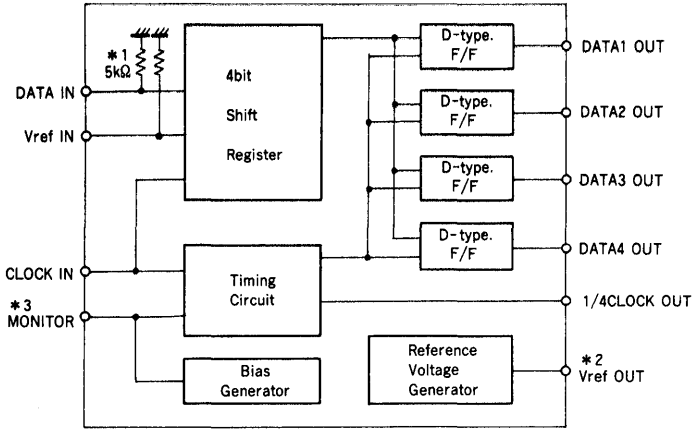
Item	Symbol	Ratings	Unit	Remarks
Supply Voltage	Vss (+)	+0.5	V	
	Vss (–)	–7.0		
Input Voltage	V_{IH}	0	V	
	V_{IL}	Vss		
Supply Current	Iss	500	mA	
Output Current	Io	50	mA	
Power Dissipation	P_D	2.5	W	
Operating Tenparature	Ta	–10 to +80	°C	
Storage Temparature	Tstg	–65 to +150	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

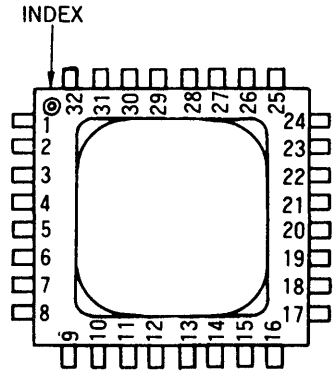
Recommended Operational Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Supply Voltage	Vss	–5.46	–5.20	–4.94	V	
Input Voltage	V_{IH}	–1.1		–0.8	V	
	V_{IL}	–1.8		–1.6		
Output termination voltage	V_{TT}		–2.0		V	
Input reference voltage	Vref	–1.386	–1.320	–1.254	V	
Input clock	CKp-p	0.6	0.8	1.2	Vp-p	

Block Diagram



Pin Description



Pin No	Pin Name	Function
1	DATA 4 OUT	DATA 4 OUTPUT
2	GND	GND
3	DATA 3 OUT	DATA 3 OUTPUT
4	GND	GND
5	DATA 2 OUT	DATA 2 OUTPUT
6	GND	GND
7	DATA 1 OUT	DATA 1 OUTPUT
8	GND	GND
9		
10		
11	1/4 clock out	1/4 clock out of input clock
12	GND	GND
13	Vss	–5.2 V voltage source input
14	GND	GND
15		
16		
17	Monitor	Gate bias control Pin, Normaly Open
18	GND	GND
19	Clock in	Clock input
20	GND	GND
21	Vref Out	Output Pin of ECL reference level voltage
22	Vref In	–1.32 V voltage source input
23	GND	GND
24	Data In	Data Input

25	GND	GND
26		
27		
28		
29		
30		
31		
32		
33		
34		

Electrical Characteristics

DC Characteristics

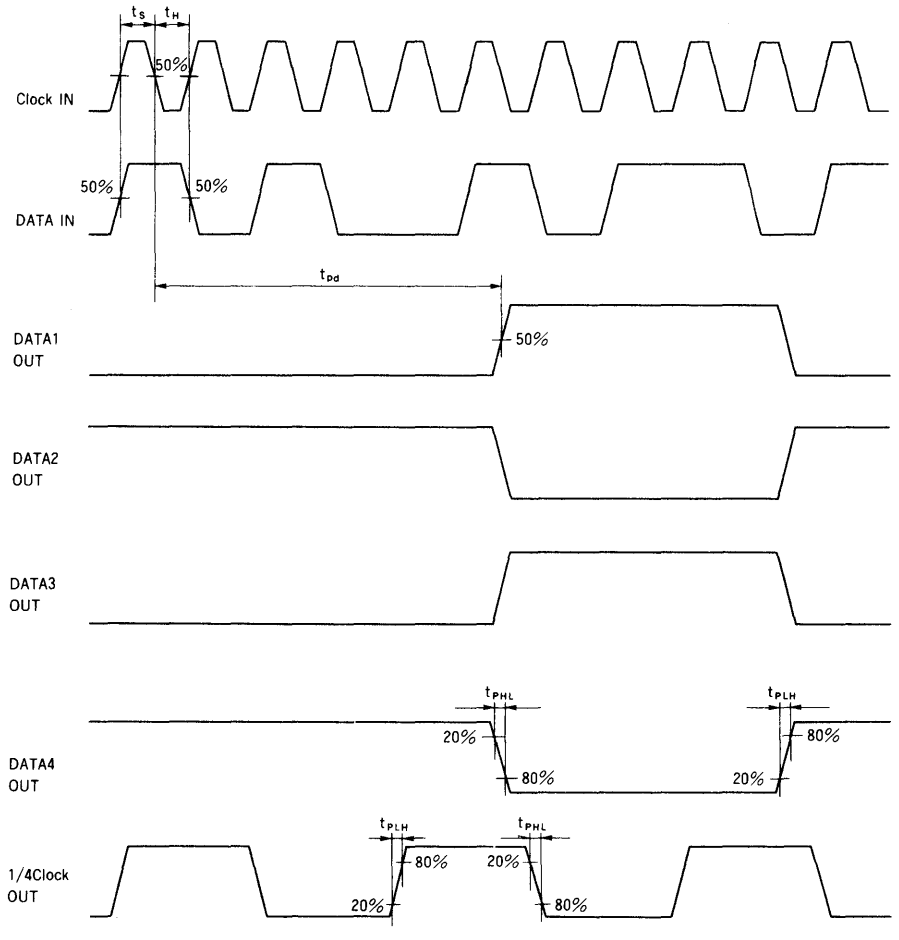
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ max, $R_T = 50\ \Omega$	–1.1		–0.8	V
	V_{OL}	$V_{IN} = V_{IL}$ min, $V_{TT} = -2$ V	–1.8		–1.6	
Input Voltage	V_{IH}		–1.1			V
	V_{IL}				–1.5	
Input Current	I_{IM}	$V_{IN} = V_{IH}$ max		160		μA
	I_{IL}	$V_{IN} = V_{IL}$ min		360		
Output Current	I_{OH}	$R_T = 50\Omega$			24	mA
	I_{OL}	$V_{TT} = -2$ V			8	
Supply Current	Iss			300		mA

AC Characteristics

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation delay time between data input and output	tpd	50% to 50%		*		ns
Input data setup time	ts		0.1			ns
Input data hold time	t_H		0.1			ns
Clock inter rate	fc max		2.4	3.6		GHz
	fc min				0.5	
Output Signal transition time	t_{TLH}	20% to 80%		0.25		ns
	t_{THL}	$R_T = 50\ \Omega$		0.25		

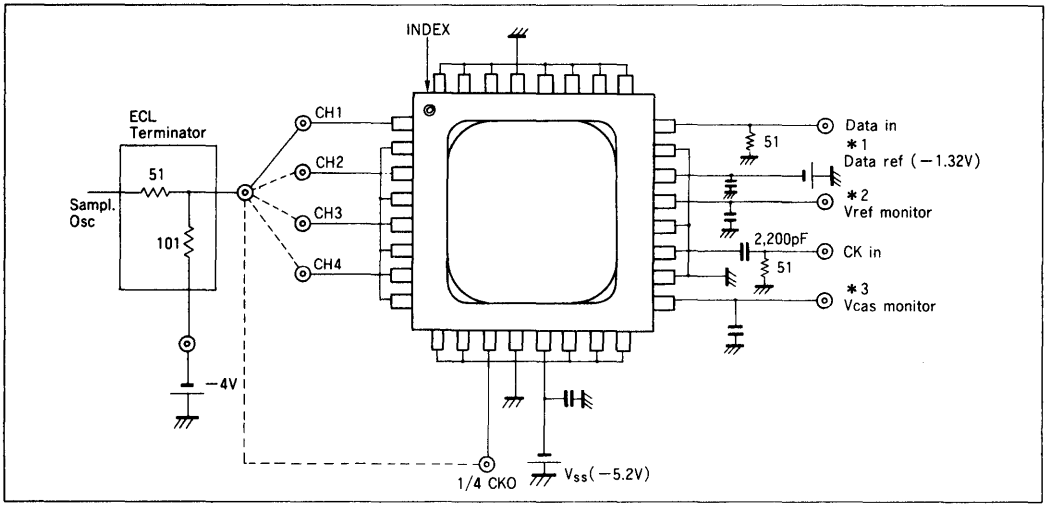
* tpd = (4T + 1.0) ns, T: Input Clock Sycle

Time Chart


t_S
t_H
50%
Clock IN
50%
50%
DATA IN
t_{pd}
DATA1
OUT
50%
DATA2
OUT
DATA3
OUT
t_{PHL}
t_{PLH}
20%
80%
80%
20%
DATA4
OUT
t_{PLH}
t_{PHL}
80%
20%
20%
80%
1/4Clock
OUT

5

Test Circuit



Mechanical Drawings

Item	Content
Outward Form	12 x 12 x 3.35 t(mm) quad leaded chip carrier
Pin Count	32
Pin Pitch	1.27 (mm)
Characteristic Impedance of Signal Line	50 ± 5 (Ω)
Noise Decoupling Chip Capacitors	located in package
Thermal Registance	20 (°C/W) with Fin at natural convection

HA29201

Preliminary

GaAs IC/Decision Circuit for Optical Communication

This HA29201 is a high speed and high sensitivity decision circuit IC for fiber optic system synchronized with external clock, it regenerates clear digital wave form. It operates from a single power supply voltage of –5.2V.

Features

- Input discrimination sensitivity of 50mV at 2.4GHz clock input.
- ECL compatible output
- Single power supply of –5.2V
- 20 pin package containing internal decoupling capacitors and input termination resistors of 50Ω

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply Voltage	V_{ss}	–7.5 to +0.5	V	
Input Voltage	V_{in}	V_{SS} to 0	V	
Supply Current	I_{ss}	200	mA	
Power Dissipation	P_t	1.5	W	
Storage Temperature	T_{stg}	–55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage	V_{ss}	–5.46	–5.2	–4.94	V	
Operating Temperature	T_a	0		+65	°C	
Clock Input Voltage	V_{in}	800			mV_{p-p}	

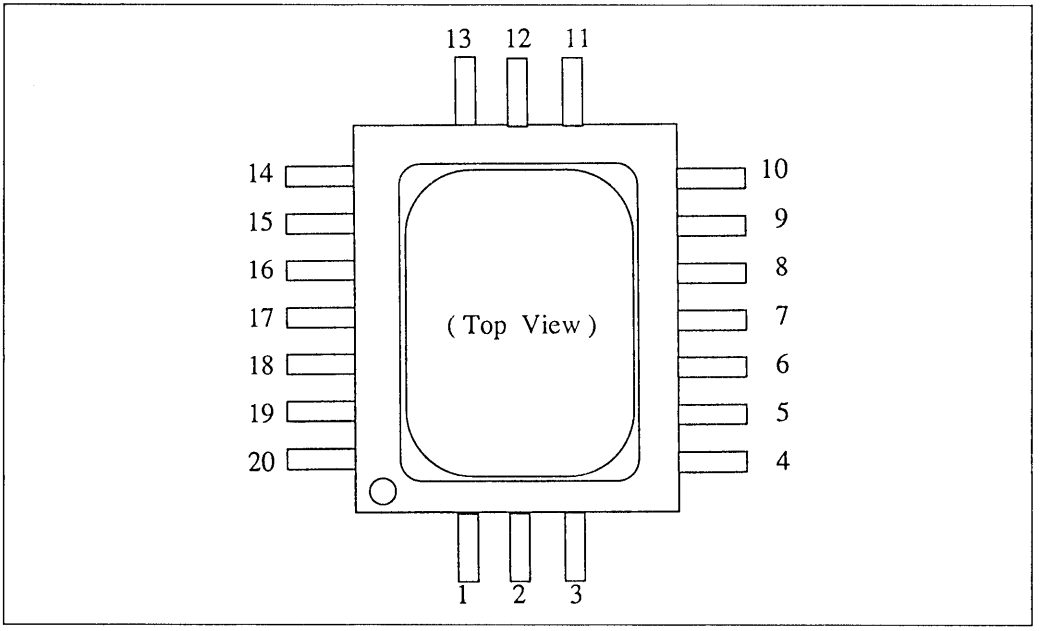
DC Characteristics (V_{ss}: –5.2V +/–5%)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Voltage	V_{OH}	V_{IH} = +0.2V, V_{IL} = –0.4V	–1.1		–0.8	V
	V_{OL}	V_r = –0.1+/–0.1V, V_{TT} = –2.0V, R_t = 50Ω	–1.9		–1.5	V
Supply Current	I_{ss}			150		mA

AC Characteristics

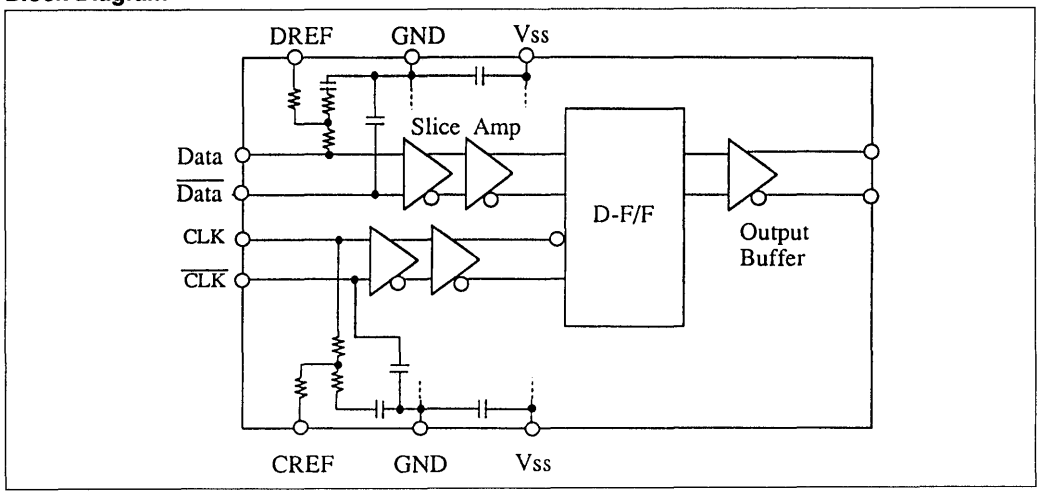
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Decision Sensitivity	V_{in} min	fc = 2.4GHz		50		mV_{p-p}
Output Transition Time	tr	R_t = 50Ω V_T = 2.0V, 20% to 80%		150		ps
	tf			150		ps

Package

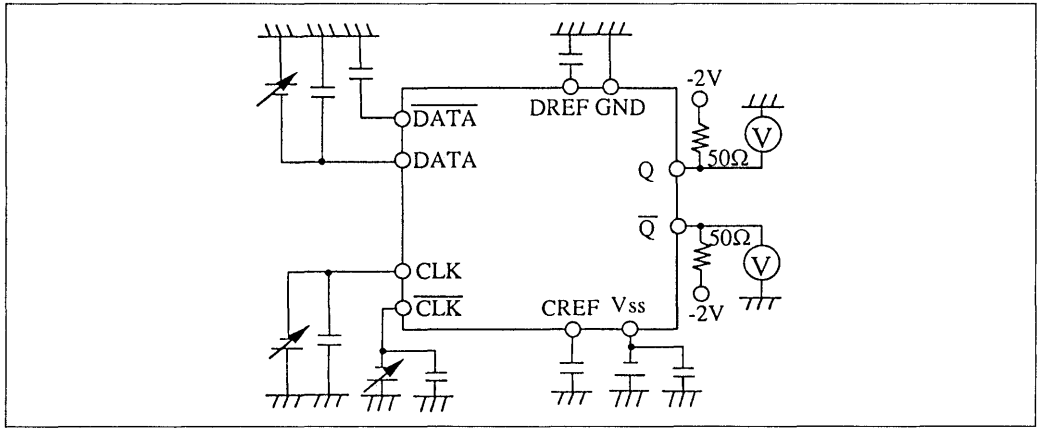


Pin #	Symbol	Function
1	Data	Data Input (-)
2	V_{SS}	-5.2V Source Input
3	N/C	No Connection
4	N/C	No Connection
5	GND	
6	Q	+Signal Output
7	GND	
8	Q	-Signal Output
9	GND	
10	N/C	No Connection
11	N/C	No Connection
12	V_{SS}	-5.2V Source Input
13	CLK	Clock (-)
14	CREF	Clock Input Level Adjustment
15	GND	
16	CLK	Clock (+)
17	GND	
18	Data	Data Input (+)
19	GND	
20	DREF	Data Input Level Adjust

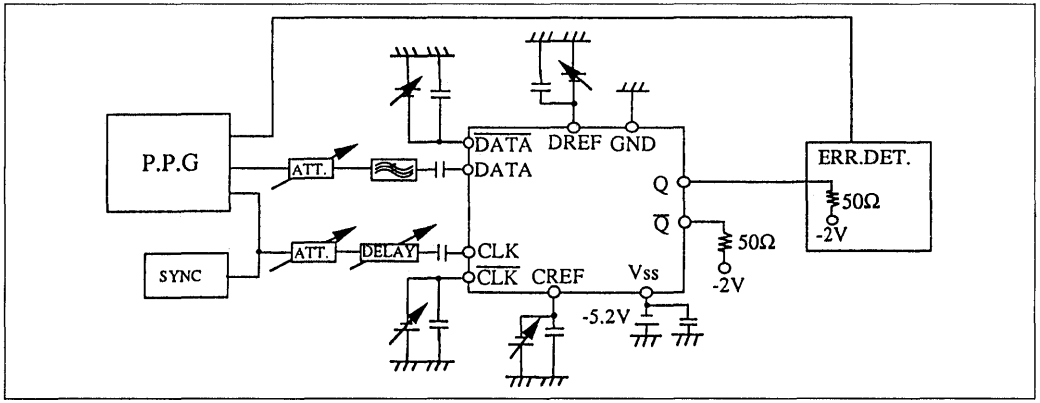
Block Diagram



DC Measurement Circuit



Sensitivity and Phase Measurement Circuit



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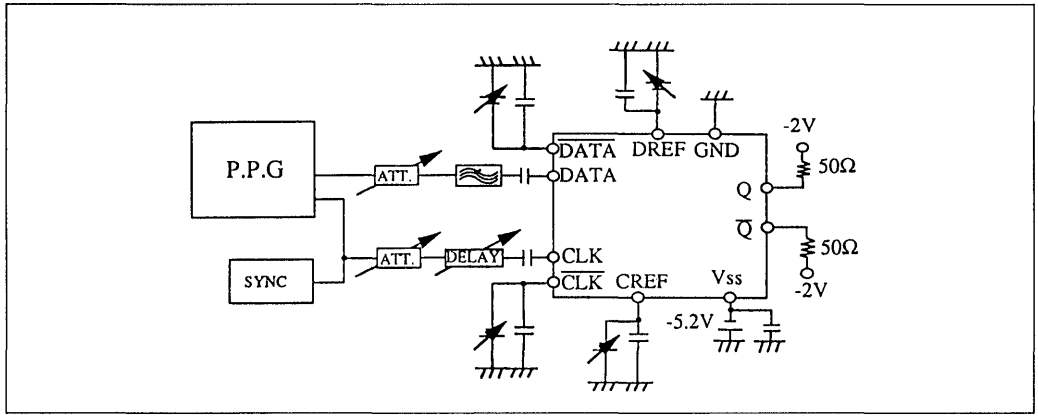
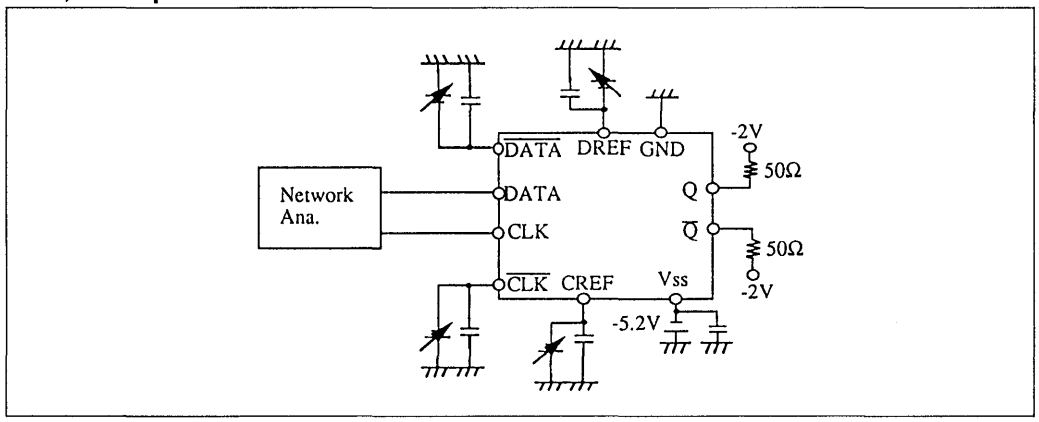
t_r/t_f Measurement Circuit



DATA, CLK input VSWR Measurement Circuit



HA29202

Preliminary

GaAs IC/Preamplifier for Optical Communication

This HA29202 is a high speed transimpedance GaAs preamplifier for fiber optic systems. The pre-amp transforms small current signal received by a photodiode into a voltage signal. It operates from a power supply voltage of –5.2V and +5V.

Features

- Transimpedance; 1kΩ
- Bandwidth of 2.4GHz
- Equivalent input noise current; 10pA/√Hz
- Power supply of –5.2V/+5.0V

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply Voltage	$V_{ss}(-)$	–7.5 to +0.5	V	
Supply Voltage	$V_{DD}(+)$	+0.5 to +7.5V	V	
Input Current	C_{in}	0.5	mA	
Supply Current	I_{ss}	40	mA	
Storage Temperature	T_{stg}	–55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

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Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage	$V_{ss}(-)$	–5.46	–5.2	–4.94	V	
Supply Voltage	$V_{DD}(+)$	4.75	5.0	5.25	V	
Operating Temperature	T_a	0		+65	°C	

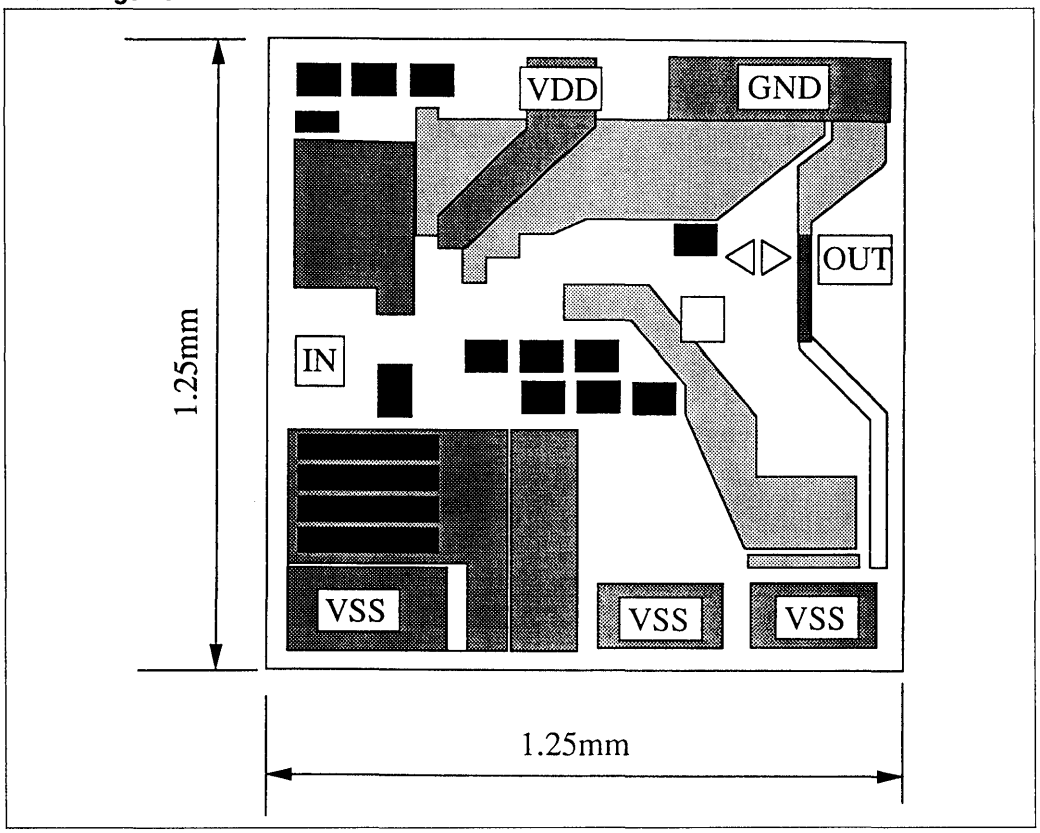
DC Characteristics (V_{ss}: –5.2V +/–5%)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Voltage	V_{out}	V_{in} open		–1.5		V
Input Current	IL_{max}			200		μA
Power Dissipation	P_d			150		mW

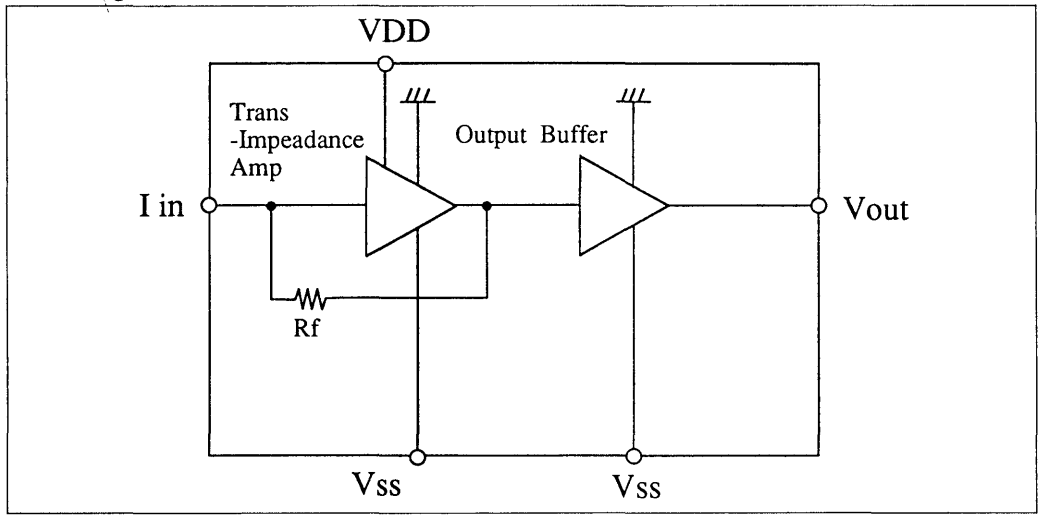
AC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Transimpedance	ZT			1000		Ω
Bandwidth	fB			2.4		GHz
Equivalent Input Noise Current	I_n			10		pA/Hz

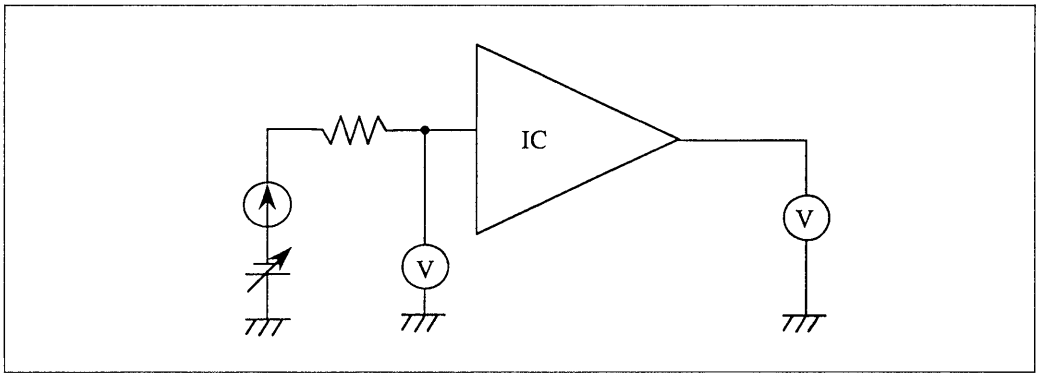
Pad Arrangement



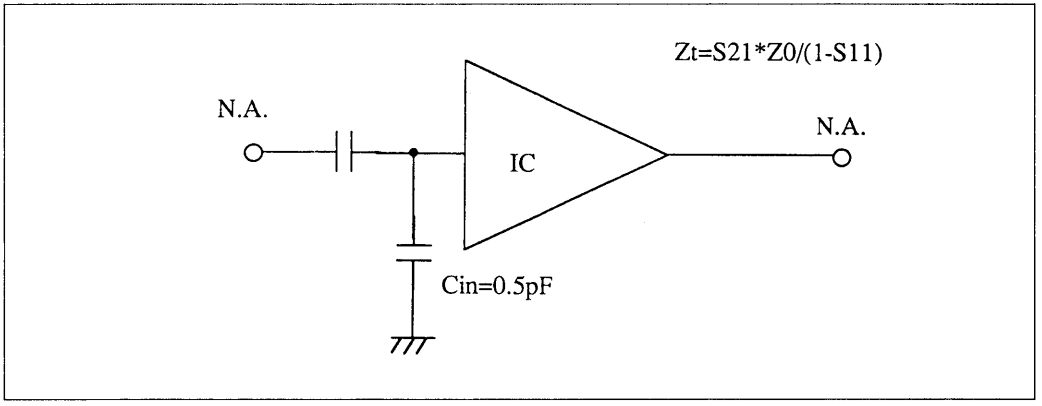
Block Diagram



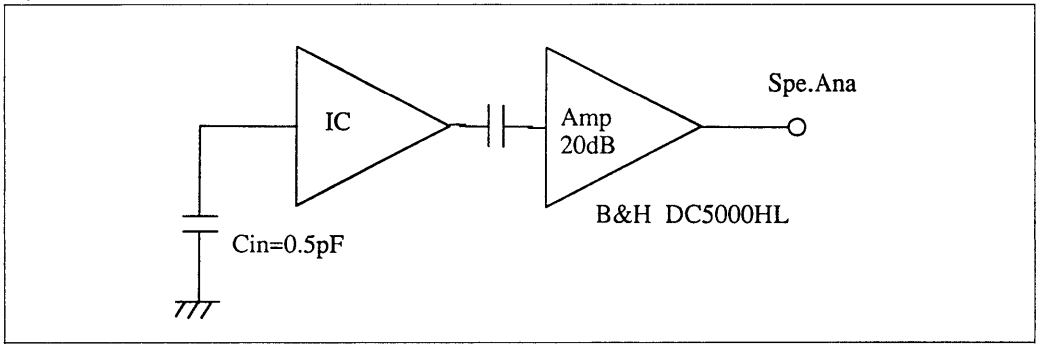
DC Measurement Circuit



AC Measurement Circuit



Input Noise Current Measurement Circuit



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HA29203

Preliminary

GaAs IC/AGC Amplifier for Optical Communication

This HA29203 is a gain controllable amplifier for fiber optic system. It achieves a maximum gain (17 dB) and gain dynamic range (30 dB) over a very wide bandwidth (50M–2.5GHz).

Features

- Bandwidth of 2.5GHz
- Maximum gain; 17dB
- 50Ω line driving capability
- Single power supply of –5.2V

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply Voltage	V_{ss}	–7.5 to +0.5	V	
Input Voltage	V_{inH}	0	V	
Input Voltage	V_{inL}	V_{ss}	V	
Supply Current	I_{ss}	200	mA	
Storage Temperature	T_{stg}	–55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage	V_{ss}	–5.46	–5.2	–4.94	V	
Operating Temperature	T_a	0		+65	°C	

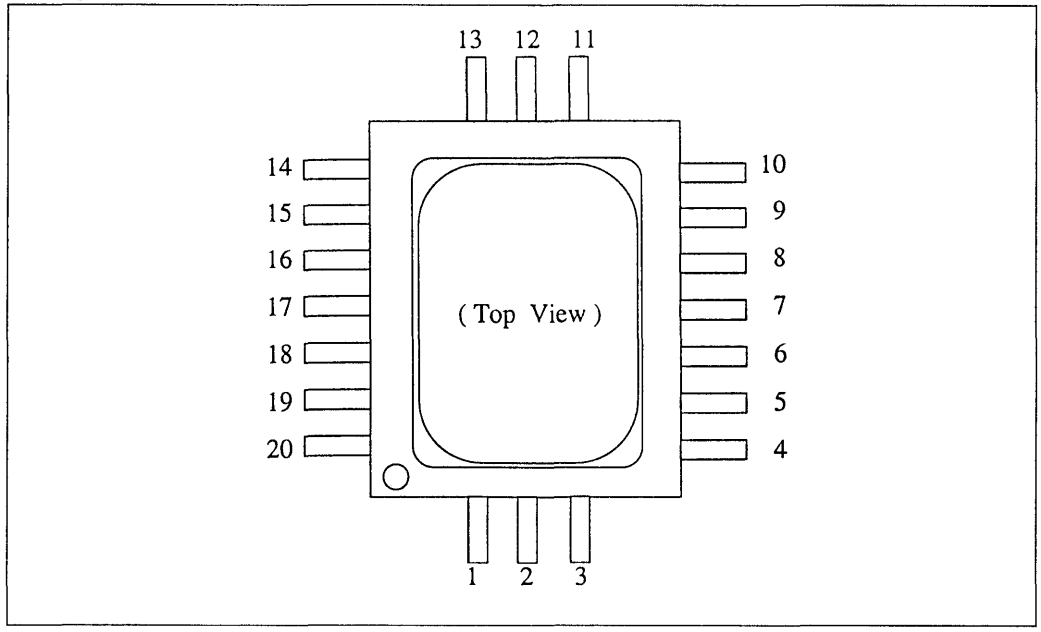
DC Characteristics (V_{ss}: –5.2V +/–5%)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Voltage	V_{out}			–1.3		V
AGC Voltage	V_{agc}(max)	Max. Gain		–2.5		V
AGC Voltage	V_{agc}(min)	Min. Gain		–3.0		V
Power Dissipation	P_d			750		mW

AC Characteristics

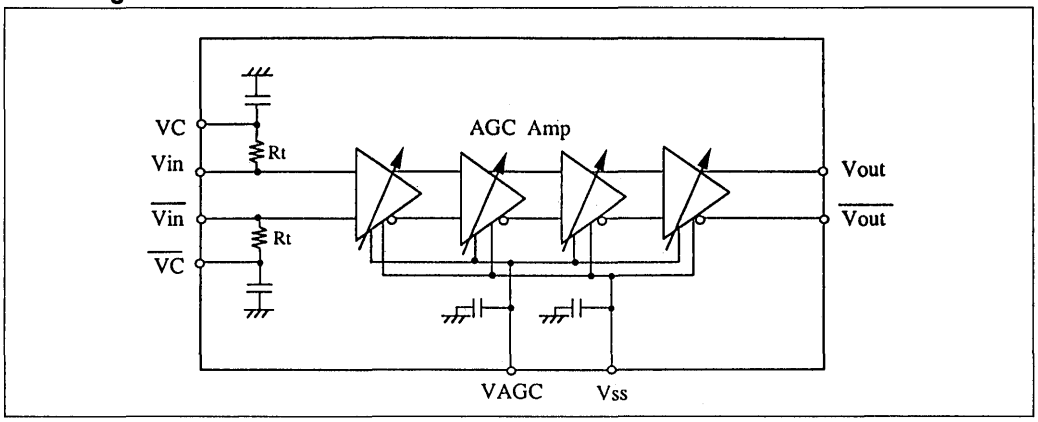
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Bandwidth	fB	3dB Down		2.5		GHz
Gain	G_{max}			17		dB
Dynamic Range	D_{ran}			30		dB
Input Impedance	Z_{in}			50		Ω
Output Impedance	Z_{out}			50		Ω

Package

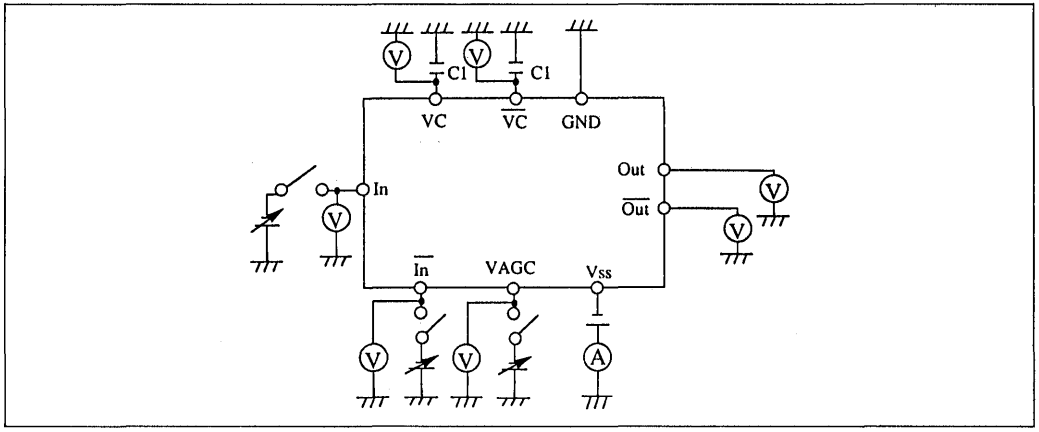


Pin #	Symbol	Function
1	N/C	No Connection
2	V_{ss}	-5.2V Source Input
3	VAGC	Gain Control
4	N/C	No Connection
5	GND	
6	$\overline{Out}$	-Signal Output
7	GND	
8	Out	+Signal Output
9	GND	
10	N/C	No Connection
11	(VAGC)	Gain Control
12	V_{ss}	-5.2V Source Input
13	N/C	No Connection
14	VC	+Input Level Adjust
15	GND	
16	In	+Signal Input
17	GND	
18	$\overline{In}$	-Signal Input
19	GND	
20	$\overline{VC}$	-Input Level Adjust

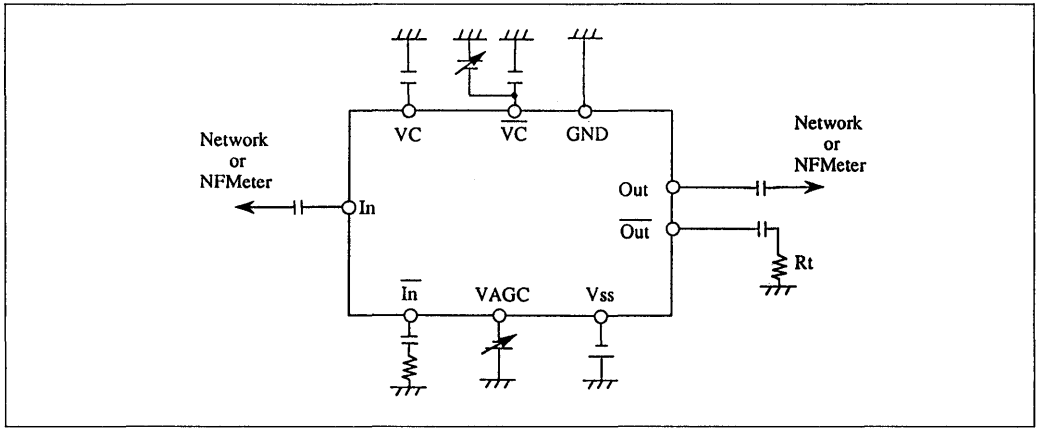
Block Diagram



DC Measurement Circuit



AC Measurement Circuit



HA29204

Preliminary

GaAs IC/Main Amplifier for Optical Communication

This HA29204 is a fixed gain amplifier for fiber optic system. It achieves a high gain (18 dB) over a very wide bandwidth of 2.5GHz.

Features

- Bandwidth of 2.5GHz
- Typical gain; 18dB
- 50Ω line driving capability
- Single power supply of -5.2V
- 20pin package containing internal decoupling capacitors and input termination resistors of 50Ω.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply Voltage	V_{ss}	-7.5 to +0.5	V	
Input Voltage	V_{in}	V_{ss} to -2.0	V	
Supply Current	I_{ss}	~200	mA	
Storage Temperature	T_{stg}	-55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

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Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage	V_{ss}	-5.46	-5.2	-4.94	V	
Operating Temperature	T_a	0		+65	°C	

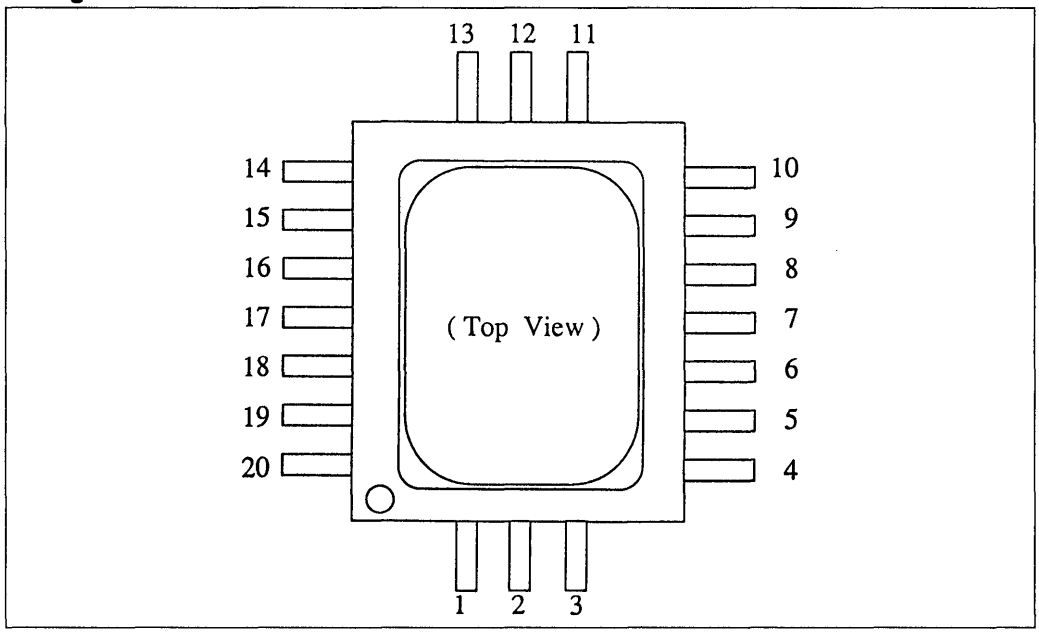
DC Characteristics (V_{ss}: -5.2V +/-5%)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Voltage (+)	V_{in+}	Terminal Open		-3.9		V
Input Voltage (-)	V_{in-}	Terminal Open		-3.9		V
Offset Voltage	V_{off}			50		mV
Vco Voltage	V_{co}	VC Terminal Open		-3.9		V
Output Voltage	V_{out}			-2.4		V
Power Consumption	P			750		mW

AC Characteristics

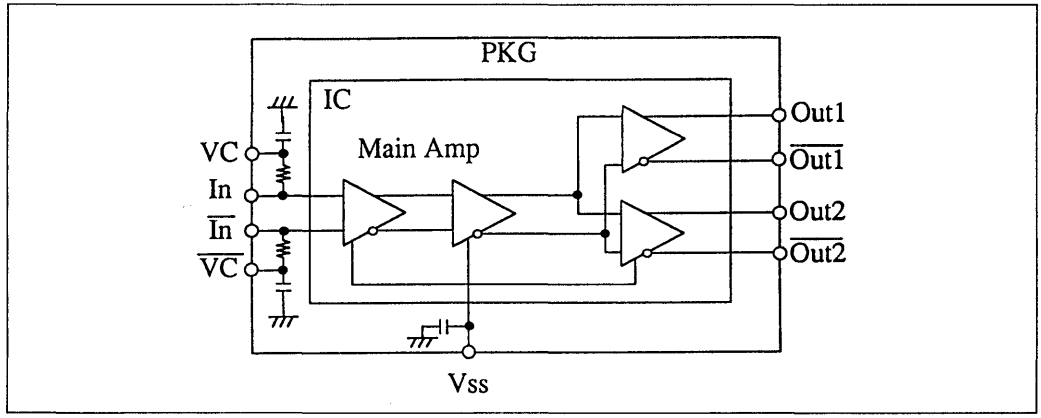
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Bandwidth	fB	3dB Down		2.5		GHz
Gain	G	100MHz		18		dB
Gain Deviation	△GF	50MHz to 1.5GHz		-1.0/+1.0		dB
Output Voltage Swing	V_{out}			0.5		V_{p-p}
Noise Figure	NF			20		dB
Input Impedance	Z_{in}			50		Ω
Input VSWR	V_{si}	50MHz to 2.5GHz		1.6		
Output Impedance	Z_{out}			50		Ω
Output VSWR	V_{so}	50MHz to 2.5GHz		1.6		

Package

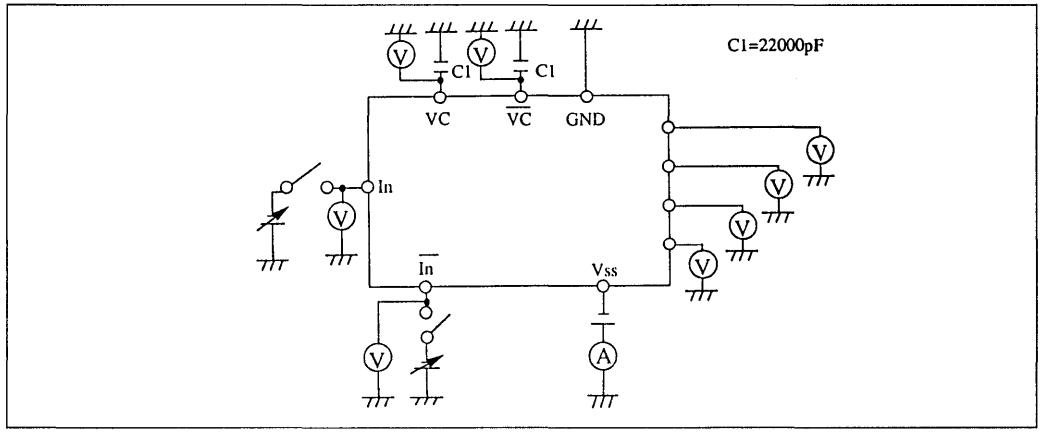


Pin #	Symbol	Function
1	N/C	No Connection
2	V_{ss}	-5.2V Source Input
3	N/C	No Connection
4	Out2	+Signal Output
5	GND	
6	Out2	-Signal Output
7	GND	
8	Out1	+Signal Output
9	GND	
10	Out1	-Signal Output
11	N/C	No Connection
12	V_{ss}	-5.2V Source Input
13	N/C	No Connection
14	VC	+Input Level Adjust
15	GND	
16	In	+Signal Input
17	GND	
18	$\overline{In}$	-Signal Input
19	GND	
20	$\overline{VC}$	-Input Level Adjust

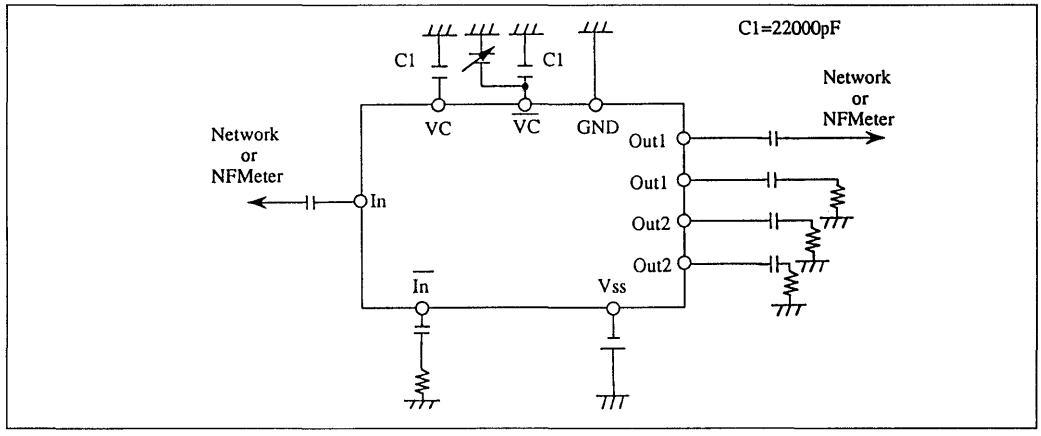
Block Diagram



DC Measurement Circuit



AC Measurement Circuit



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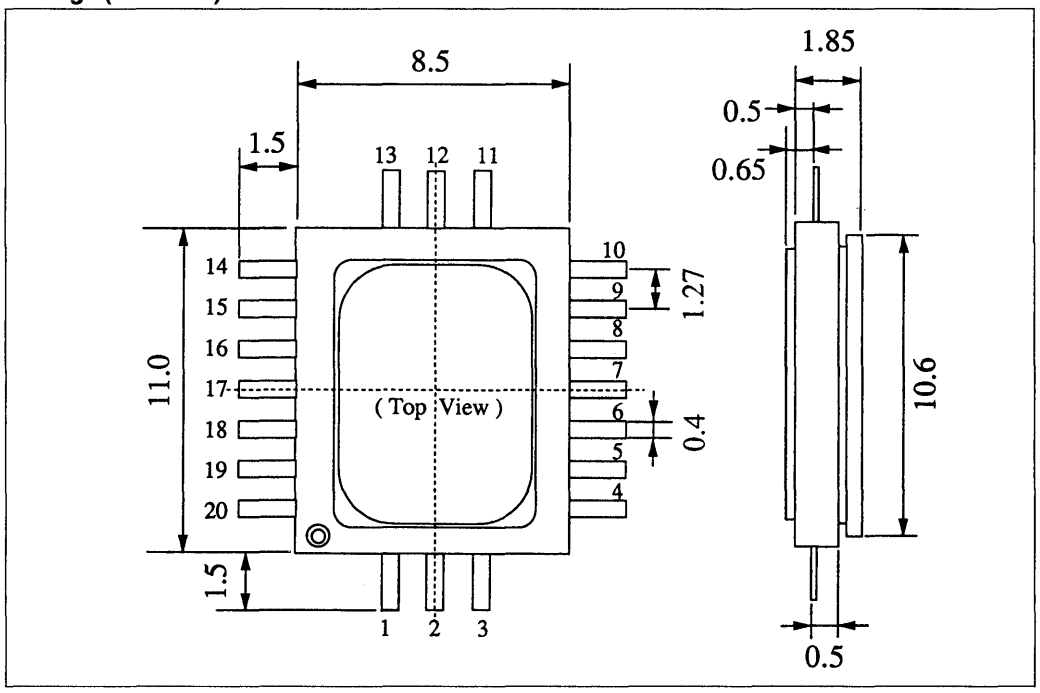
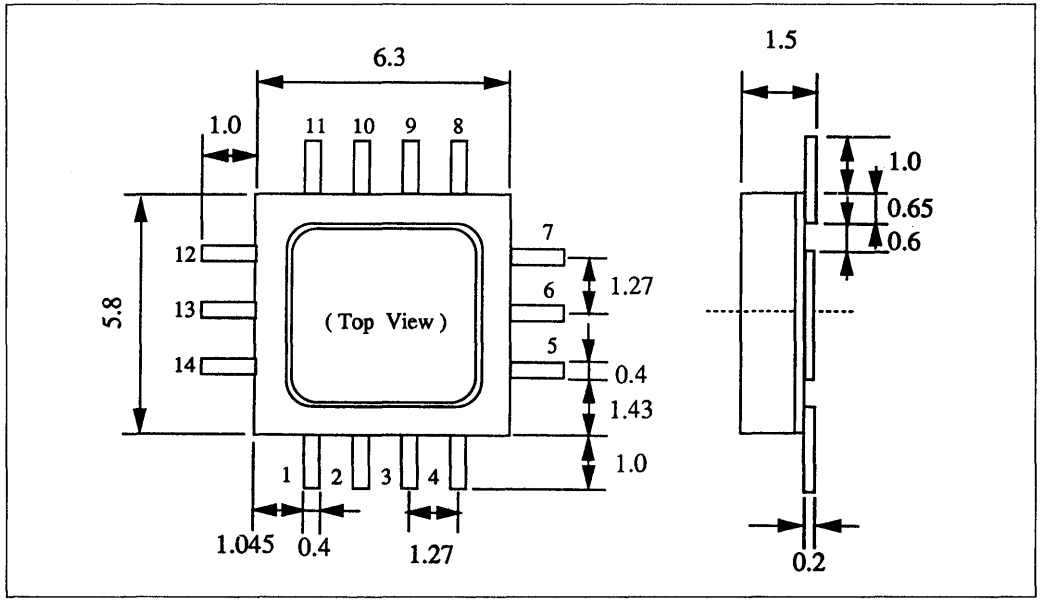
Package (Unit: mm)



Package (Unit: mm)



Section Six

Laser Diodes, LEDs, PINs and APDs for Fiber Optic Communications and Office Automation Equipment

The absolute maximum ratings referenced in the data sheet sections of this manual are limiting values, to be applied individually and beyond which operation of the described circuits may be impaired. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the circuit's reliability.

The "Electrical Characteristics" of the circuits described in this manual are for reference only.

Family Introduction

Laser Diodes (LD)

Chips	Packages											
	A	AC	E	G	MG	HG	FG	TR	DM	BF	DL	MF
HL6711				HL6711G								
HL7801			HL7801E									
HL7802			HL7802E	HL7802G								
HL7806				HL7806G	HL7806MG							
HL7831				HL7831G		HL7831HG						
HL7832				HL7832G		HL7832HG						
HL7836				HL7836G	HL7836MG							
HL7838				HL7838G								
HL8311	HLP1400		HL8311E	HL8311G								
HL8312/ HL8315			HL8312E HL8315E	HL8312G								
HL8314			HL8314E	HL8314G								
HL8318			HL8318E	HL8318G								
HL1221	HL1221A	HL1221AC										
HL1321	HLP5400	HL1321AC					HL1321FG			HL1321BF	HL1321DL	
HL1322	HL1322A	HL1322AC										
HL1323								HL1323TR	HL1323DM			
HL1341	HL1341A	HL1341AC					HL1341FG			HL1341BF	HL1341DL	
HL1361	HL1361A	HL1361AC										
HL1521	HL1521A	HL1521AC					HL1521FG					
HL1541	HL1541A	HL1541AC					HL1541FG		HL1541DM	HL1541BF	HL1541DL	
HL1561	HL1561A	HL1561AC								HL1561BF		
HL6712				HL6712G								
HL7851				HL7851G								
HL1324												HL1324MF

Infra-red Emitting Diodes (IRED)

	Packages								
Chips	R	RG	SG	VG	MA	ML	SL	CL	TR
HLP30	HLP20R –HLP40R	HLP20RG –HLP40RG							
HE7601			HE7601SG						
HE8403	HE8403R		HE8403SG			HE8403ML			HE8403TR
HE8404			HE8404SG						
HE8805				HE8805VG					
HE8806				HE8806VG					
HE8807			HE8807SG				HE8807SL	HE8807CL	
HE8811			HE8811						
HE8812			HE8812SG						
HE1301	HE1301R		HE1301SG			HE1301ML			HE1301TR

Photo Diode (PD)

	Packages				
Chips	QG	TG	LG	CX	TR
HR8101	HR8101				
HR8102		HR8102			
HR8202		HR8202TG			
HR1103		HR1103TG		HR1103CX	HR1103TR
HR1104		HR1104TG		HR1104CX	
HR1105		HR1105TG			
HR1106					
HR1201		HR1201TG		HR1201CX	

6

Laser Diodes

HL6711G

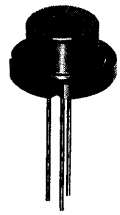
Laser Diode

Features

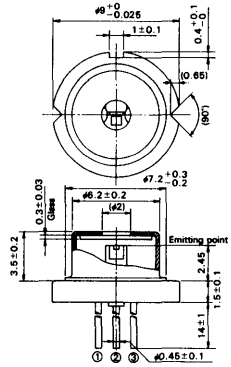
- Visible light output: λ_p = 670 nm typ.
- Threshold currents: I_{th} = 80 mA typ.
- Built-in photodiode for monitoring laser output

Applications

- Bar code readers
- Measurement or control equipment
- Various other types of optical equipment



Package Dimensions



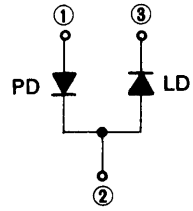
Notes: Optical path: 2.55 mm
Refraction index of window glass: 1.46 – 1.53

1. Photodiode anode
2. Common (Case)
3. Laser diode cathode

(Unit: mm)

G-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +85	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		80	95	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.4	0.7	0.8	mW/mA	$\frac{3(mW)}{I(5\ mW) - I(2\ mW)}$
Lasing wavelength	λ_p	660	670	680	nm	P_O = 5 mW
Beam divergence parallel to the junction	$\theta_{//}$	6	8	10	deg.	P_O = 5 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	40	deg.	P_O = 5 mW
Monitor current	I_S	30	100	150	μA	$V_{R(PD)}$ = 5 V, P_O = 5mW

HL6712G

Preliminary

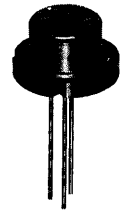
Laser Diode

Description

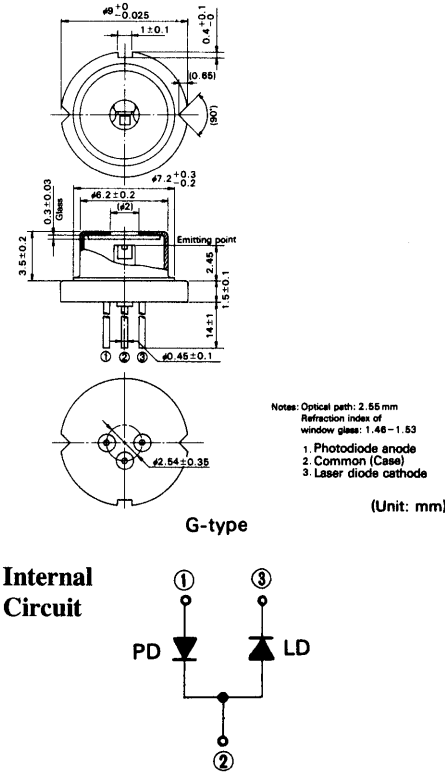
HL6712G is a 0.67μm AlGaInP laser diode with double heterojunction structure. It is suitable as light source in laser pointer, laser bar code reader, measurement equipment and various other types of optical equipment. To get the single longitudinal mode and visible wavelength, the extensive studies on crystal and the optimization of the laser diode die structure have been pursued.

Features

- Visible light output; 0.67μm typ.
- High power output; 5mW CW
- Single longitudinal mode
- Built-in photodiode for monitoring laser output



Package Dimensions



G-type

Internal Circuit

Absolute Maximum Ratings (T_c=25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photo diode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +85	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_c=25°C)

Items	Symbols	min.	typ.	max.	Unit	Test condition
Threshold current	I_{th}		45	65	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.2	0.5	0.8	mW/mA	$\frac{3(mW)}{I(4mW)-I(1mW)}$
Lasing wavelength	λ_p		670	680	nm	P_O = 5mW
Beam divergence parallel to the junction	$\theta_{//}$	6	9	14	deg.	P_O = 5mW
Beam divergence perpendicular to the junction	$\theta\perp$	25	35	45	deg.	P_O = 5mW
Monitor Current	I_S		0.9			P_O = 5mW, V_r(PD) = 5mW
Astigmatism	A_S		10		μm	P_O = 5mW

6

HL7801E

Laser Diode

Description

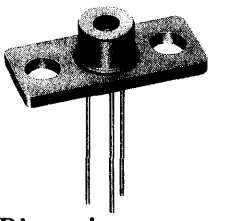
HL7801E is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

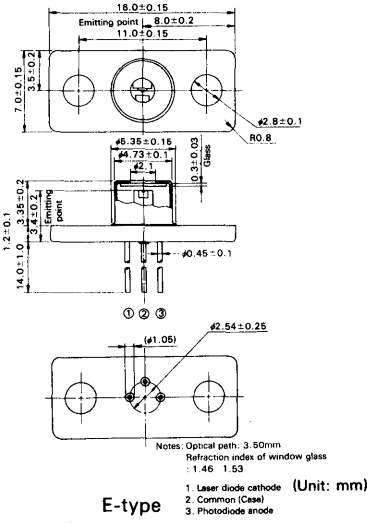
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 760–800 nm
- Built-in photodiode for monitoring laser output
- Low astigmatism: As = 2 μm typ.
- Small beam ellipticity:
  $\theta_{//}$ = 15 deg., $\theta_{\perp}$ = 30 deg. typ.
- Single longitudinal mode

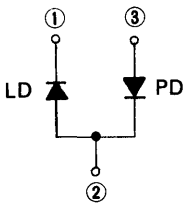


Package Dimensions



E-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

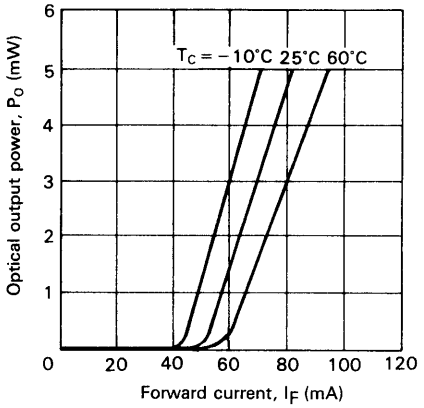
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

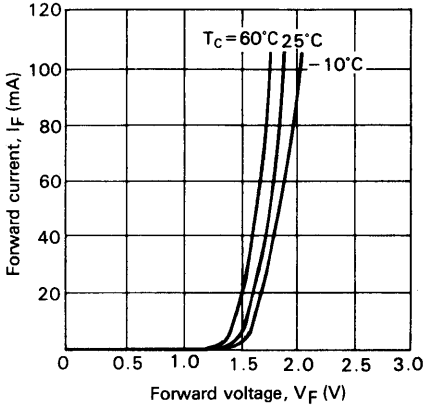
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	90	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.13	0.25		mW/mA	$\frac{3(mW)}{I(4\ mW) - I(1\ mW)}$
Lasing wavelength	λ_p	760	780	800	nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$	10	15	20	deg.	P_O = 3 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	40	deg.	P_O = 3 mW
Monitor current	I_S	0.1	0.3		mA	P_O = 3 mW

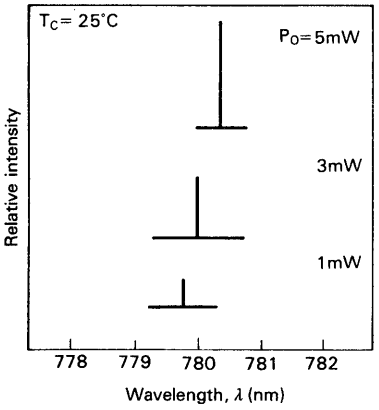
Optical Output Power vs. Forward Current



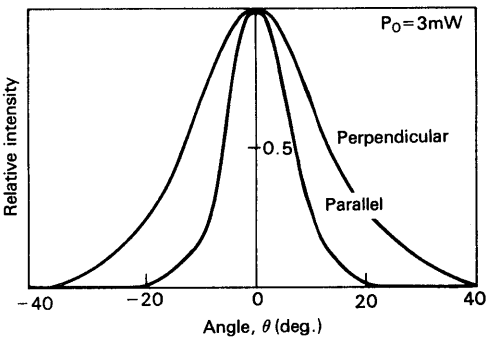
Forward Current vs. Forward Voltage



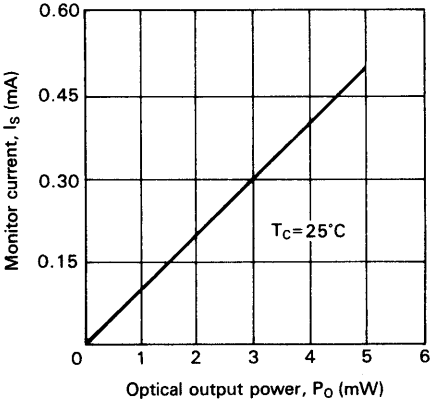
Lasing Spectrum



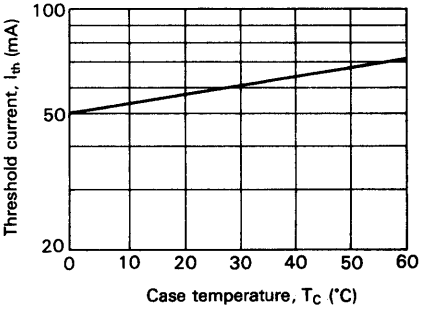
Far Field Pattern



Monitor Current vs. Optical Output Power



Threshold Current vs. Case Temperature



6

HL7802E

Laser Diode

Description

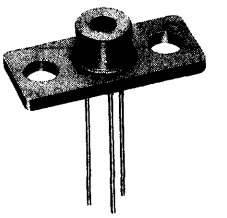
HL7802E is a high-power 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

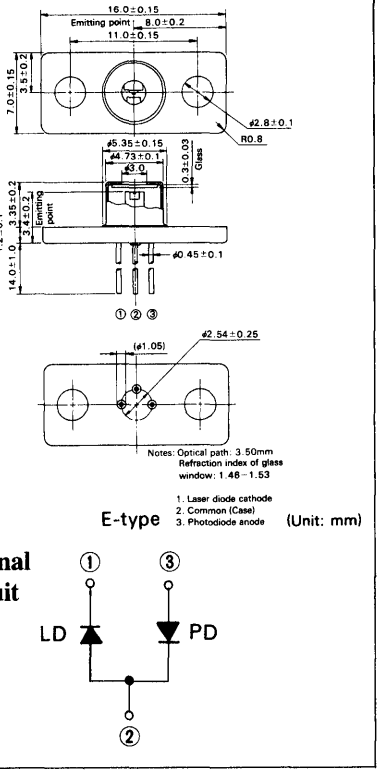
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



Package Dimensions



Internal Circuit

Absolute Maximum Ratings (T_C = 25°C)

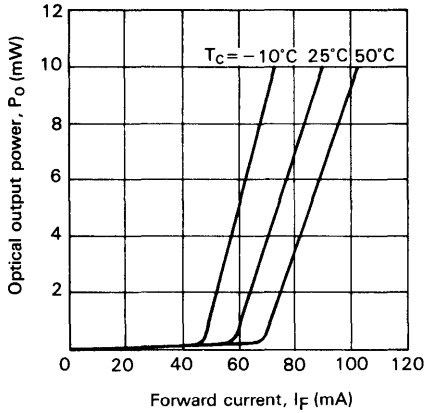
Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

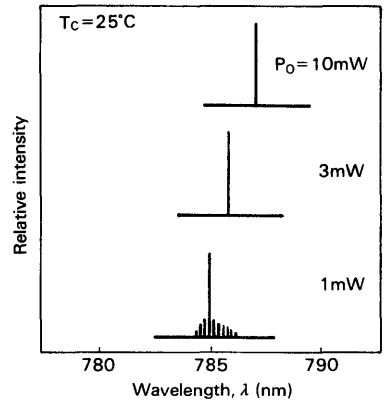
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	90	mA	
Optical output power	P_O	10			mW	Kink free
Slope efficiency	η	0.13	0.25	—	mW/mA	$\frac{6(mW)}{I(8\ mW) - I(2\ mW)}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	7	11	15	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	35	deg.	P_O = 10 mW
Monitor current	I_S	0.35			mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

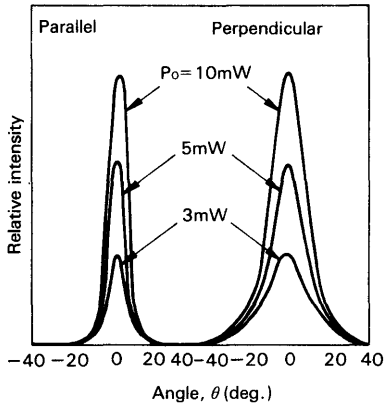
Optical Output Power vs. Forward Current



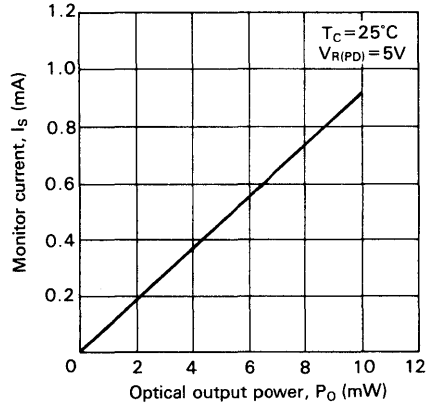
Lasing Spectrum



Far Field Pattern



Monitor Current vs. Optical Output Power



6

HL7802G

Laser Diode

Description

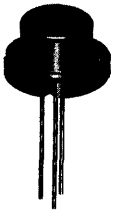
HL7802G is a high-power 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

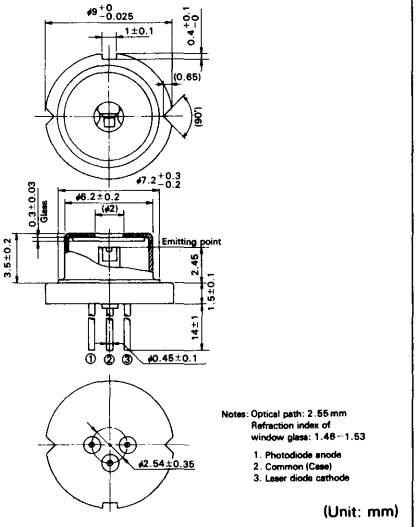
Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



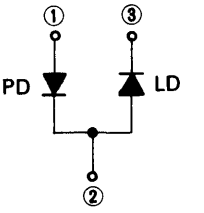
Package Dimensions



(Unit: mm)

G-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

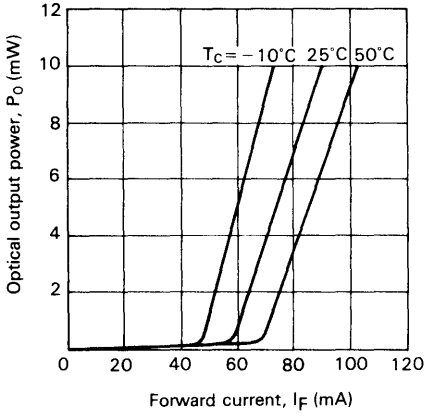
Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

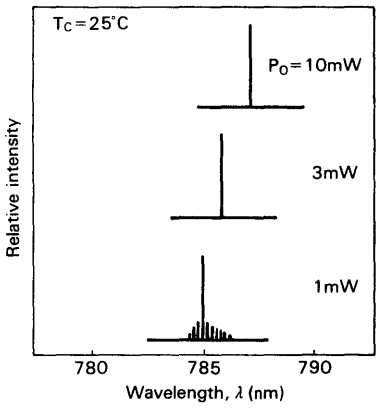
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	90	mA	
Optical output power	P_O	10			mW	Kink free
Slope efficiency	η	0.13	0.25		mW/mA	$\frac{6(mW)}{I\,(8\,mW) - I\,(2\,mW)}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	7	11	15	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	30	35	deg.	P_O = 10 mW
Monitor current	I_S	0.35			mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

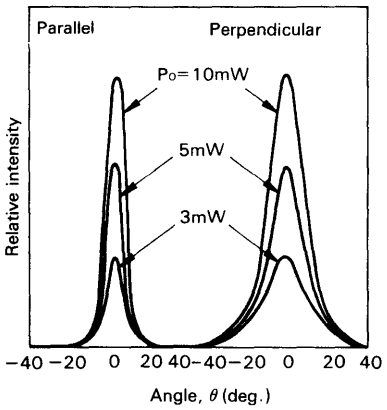
Optical Output Power vs. Forward Current



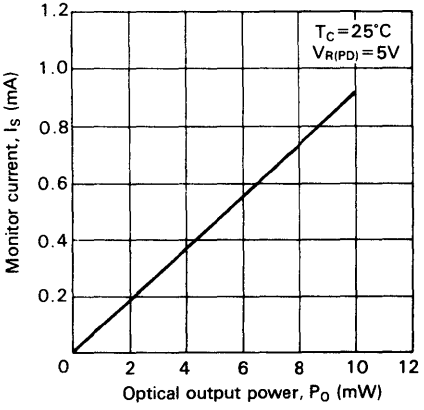
Lasing Spectrum



Far Field Pattern



Monitor Current vs. Optical Output Power



6

HL7806G

Laser Diode

Description

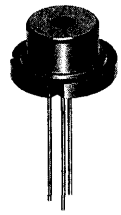
HL7806G is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

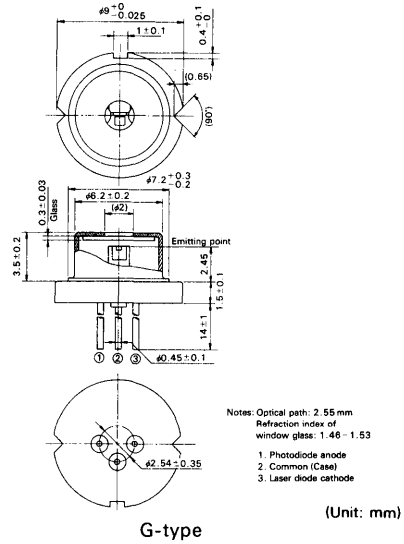
Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 775–795 nm
- Built-in photodiode for monitoring laser output
- Low astigmatism: As = 2 μm typ.
- Small beam ellipticity:
  $\theta_{//}$ = 14 deg., $\theta_{\perp}$ = 27 deg. typ.
- Single longitudinal mode

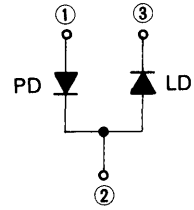


Package Dimensions



G-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

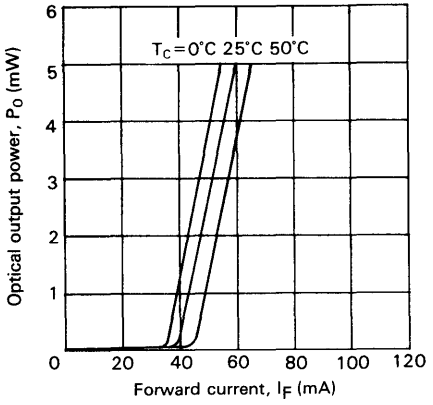
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

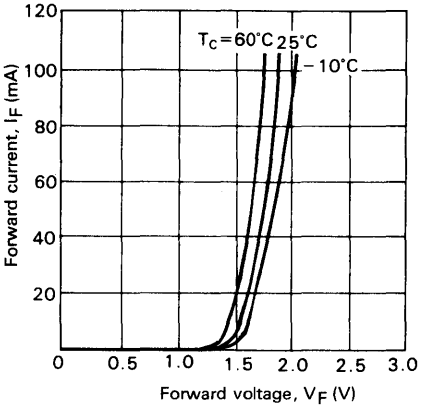
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		40	70	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.15	0.25		mW/mA	$\frac{3(mW)}{I(4\ mW) - I(1\ mW)}$
Lasing wavelength	λ_p	775	785	795	nm	P_O = 5 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	14	20	deg.	P_O = 5 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	27	45	deg.	P_O = 5 mW
Monitor current	I_S	0.35	1.0	1.65	mA	$V_{R(PD)}$ = 5 V, P_O = 5±0.05 mW

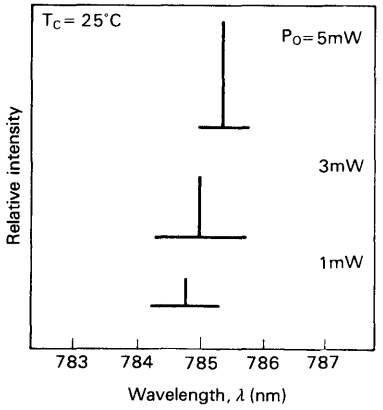
Optical Output Power vs. Forward Current



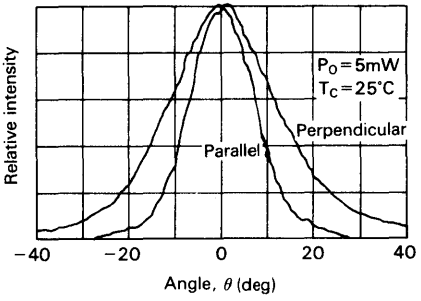
Forward Current vs. Forward Voltage



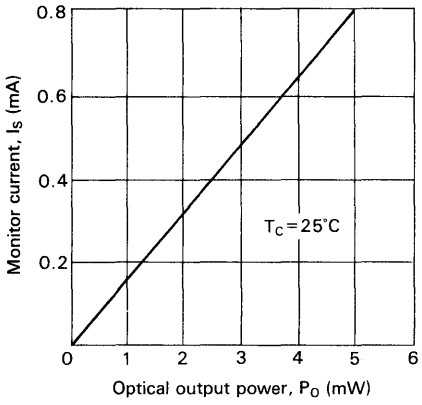
Lasing Spectrum



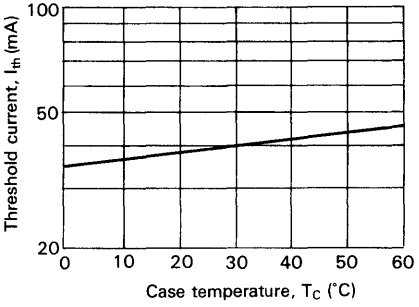
Far Field Pattern



Monitor Current vs. Optical Output Power

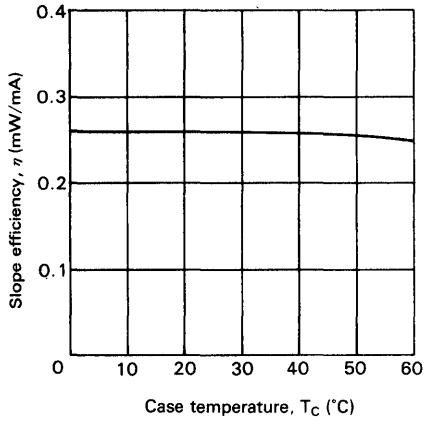


Threshold Current vs. Case Temperature

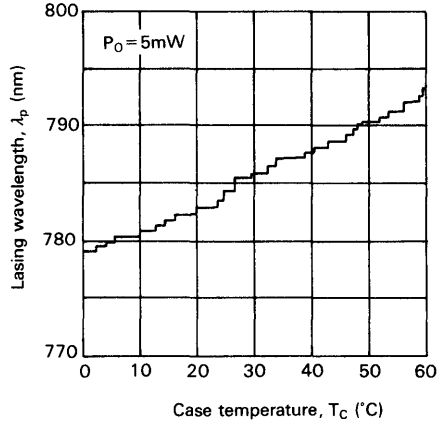


6

Temperature Dependence of Slope Efficiency



Temperature Dependence of Lasing Wavelength



HL7806MG

Laser Diode

Description

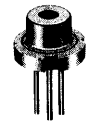
HL7806MG is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

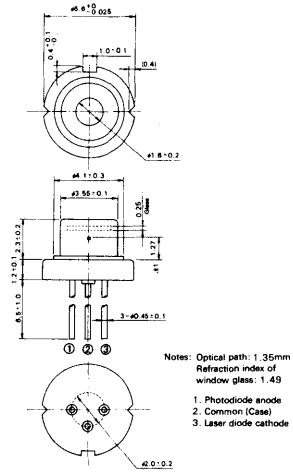
Hermetic sealing of the package achieves high reliability. The package capacity is five times as small as G-type's.

Features

- Visible light output: λ_p = 775–795 nm
- Built-in photodiode for monitoring laser output
- Low astigmatism: As = 2 μm typ.
- Small beam ellipticity:
  $\theta_{//}$ = 14 deg., $\theta_{\perp}$ = 27 deg. typ.
- Single longitudinal mode

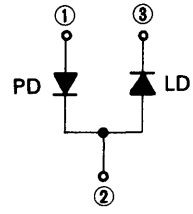


Package Dimensions



MG-type (Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

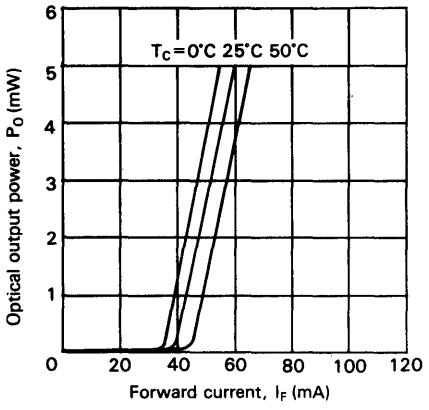
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

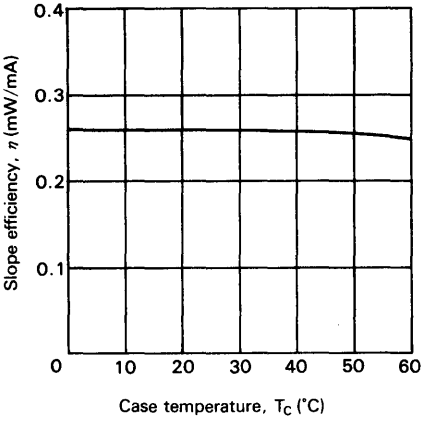
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		40	70	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.15	0.25		mW/mA	$\frac{3(mW)}{I\,(4\,mW) - I\,(1\,mW)}$
Lasing wavelength	λ_p	775	785	795	nm	P_O = 5 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	14	20	deg.	P_O = 5 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	27	45	deg.	P_O = 5 mW
Monitor current	I_S	0.2	0.5	0.8	mA	$V_{R(PD)}$ = 5 V, P_O = 5±0.05 mW

6

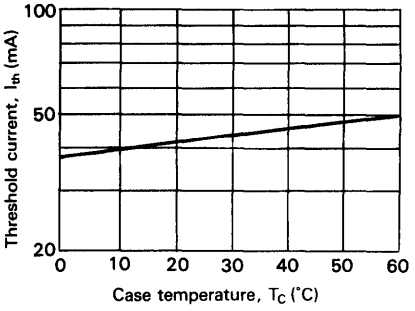
Optical Output Power vs. Forward Current



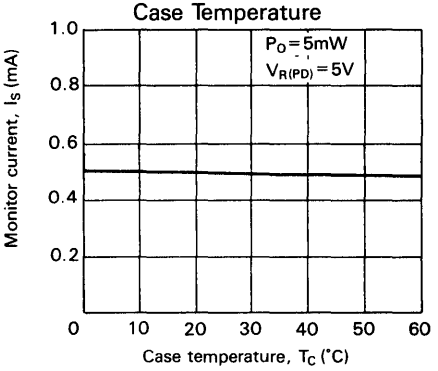
Temperature Dependence of Slope Efficiency



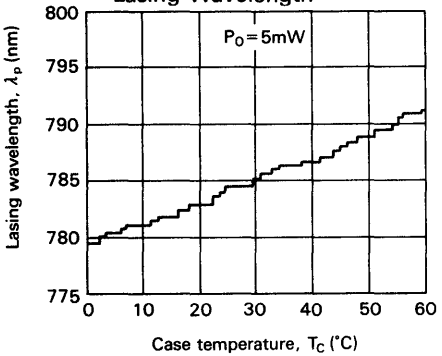
Threshold Current vs. Case Temperature



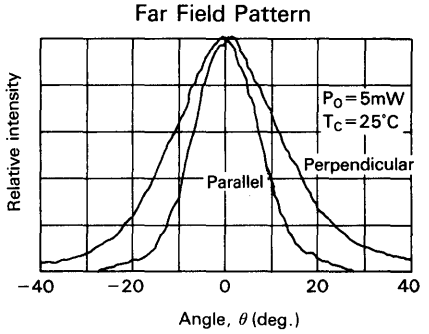
Monitor Current vs. Case Temperature



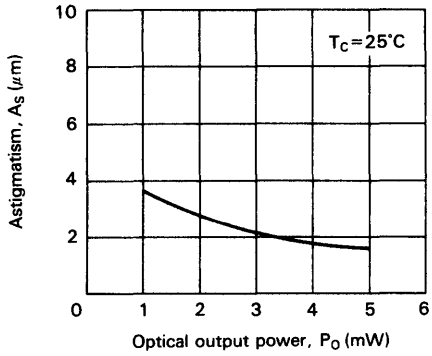
Temperature Dependence of Lasing Wavelength



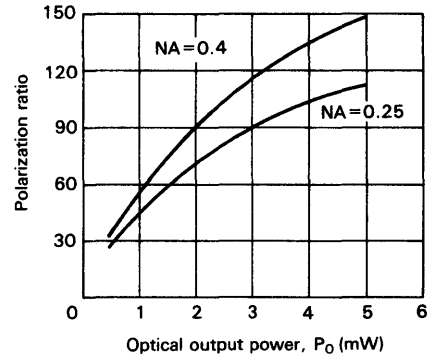
Far Field Pattern



Optical Output Power Dependence of Astigmatism



Optical Output Power Dependence of Polarization Ratio



6

HL7831G

Laser Diode

Description

HL7831G is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

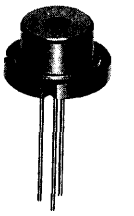
It is suitable as a light source in compact disc and optical video disc players and various other types of optical equipment.

MOCVD technology is employed to precisely analyze and optimize device conditions in order to realize a low noise level.

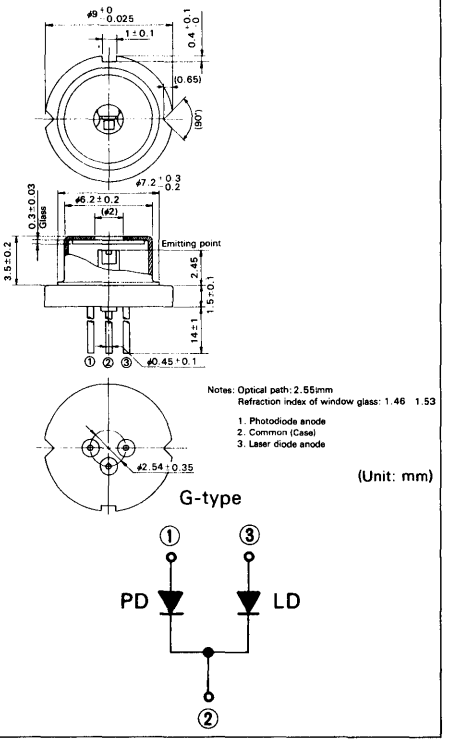
Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Multiple longitudinal mode
- Low noise: S/N = 60 dB min.



Package Dimensions



Absolute Maximum Ratings (T_C = 25°C)

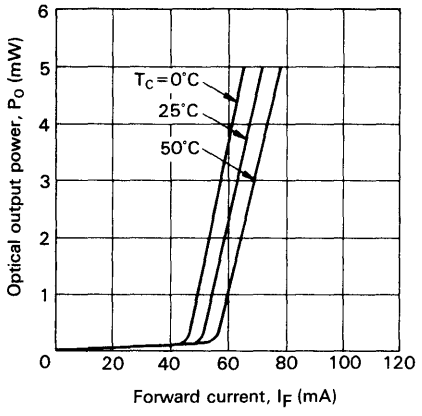
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

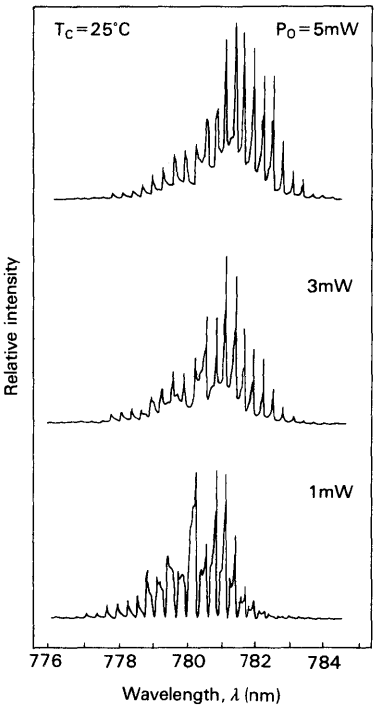
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	80	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.1	0.25	0.6	mW/mA	$\frac{3(mW)}{I(4\ mW) - I(1\ mW)}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$	9	13	16	deg.	P_O = 3 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	35	48	deg.	P_O = 3 mW
Monitor current	I_S	0.3	1.0	1.6	mA	$V_{R(PD)}$ = 5 V, P_O = 3±0.03 mW
Noise	S/N	60			dB	P_O = 3 mW, f = 750 kHz, Δf = 30 kHz

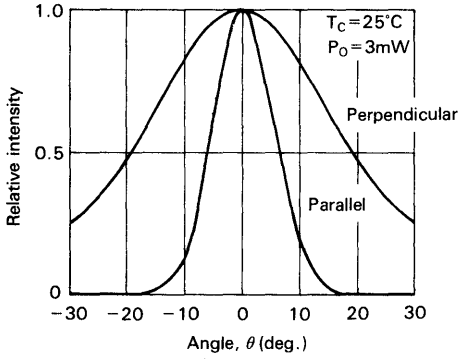
Optical Output Power vs. Forward Current



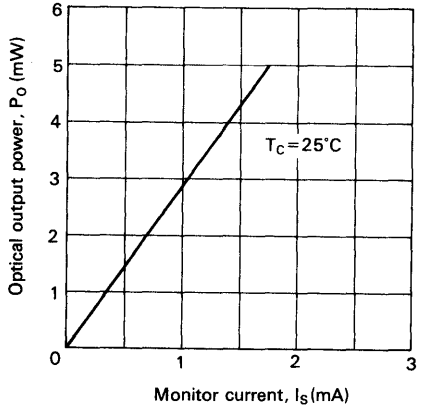
Lasing Spectrum



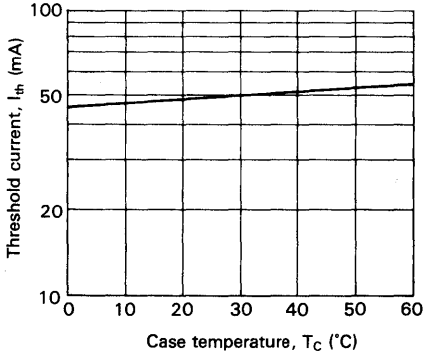
Far Field Pattern



Optical Output Power vs. Monitor Current

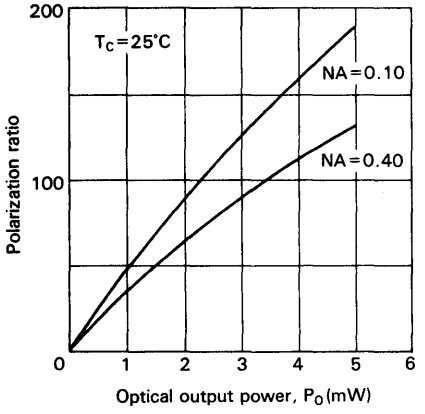


Threshold Current vs. Case Temperature

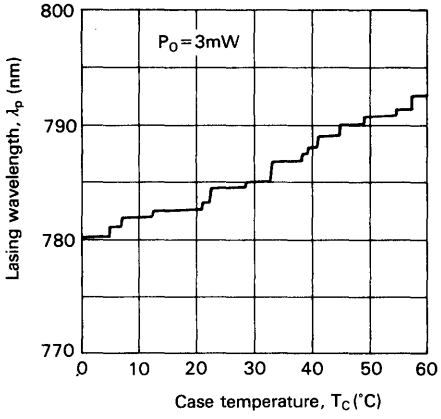


6

Optical Output Power Dependence of Polarization Ratio



Temperature Dependence of Lasing Wavelength



HL7831HG

Laser Diode

Description

HL7831HG is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

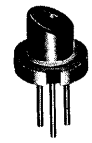
It is suitable as a light source in compact disc and optical video disc players and various other types of optical equipment.

MOCVD technology is employed to precisely analyze and optimize device conditions in order to realize a low noise level.

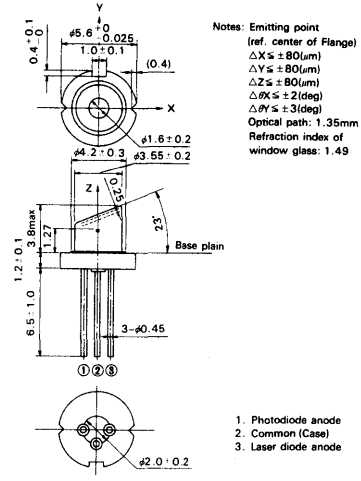
Hermetic sealing of the package achieves high reliability. The package capacity is five times as small as G-type's. Astigmatism is minimized with a slanted glass window of cap.

Features

- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Multiple longitudinal mode
- Low noise: S/N = 60 dB min.
- Low astigmatism: | As | ≦ 10 μm

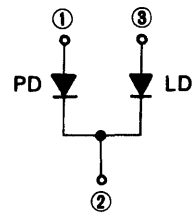


Package Dimensions



HG-type (Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

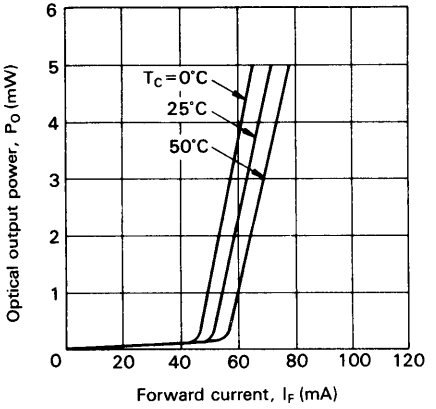
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

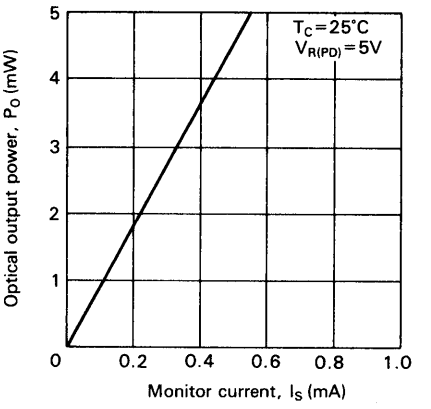
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	80	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.1	0.25	0.6	mW/mA	$\frac{3(mW)}{I(4\ mW) - I(1\ mW)}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$	9	11	16	deg.	P_O = 3 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	35	48	deg.	P_O = 3 mW
Monitor current	I_S	0.15		0.6	mA	$V_{R(PD)}$ = 5 V, P_O = 5±0.05 mW
Noise	S/N	60			dB	P_O = 3 mW, f = 750 kHz, Δf = 30 kHz

6

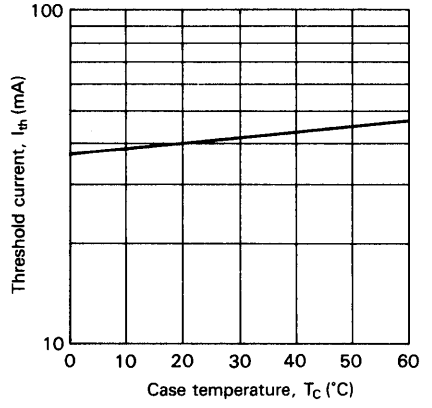
Optical Output Power vs. Forward Current



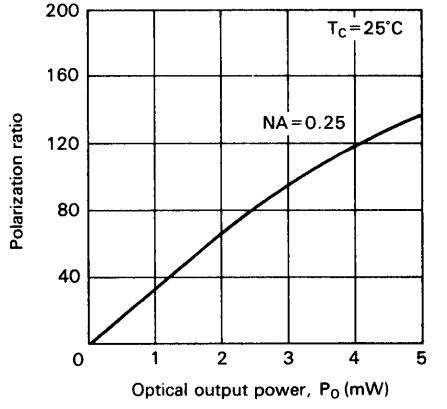
Optical Output Power vs. Monitor Current



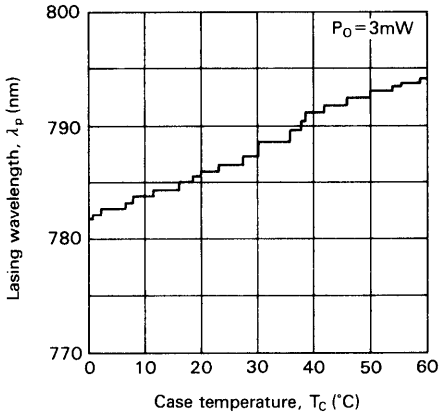
Threshold Current vs. Case Temperature



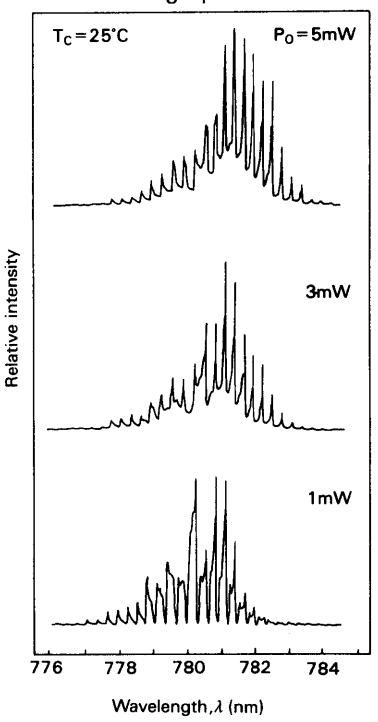
Optical Output Power Dependence of Polarization Ratio



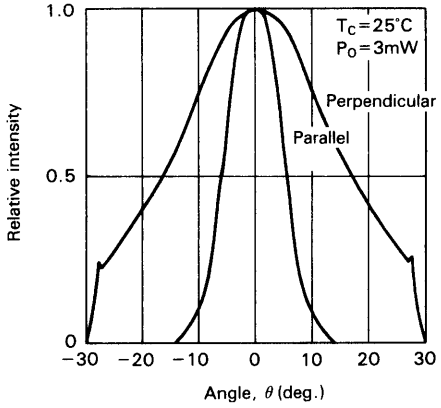
Temperature Dependence of Lasing Wavelength



Lasing Spectrum



Far Field Pattern



6

HL7832G

Laser Diode

Description

HL7832G is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

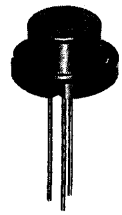
It is suitable as a light source in optical video disc players and various other types of optical equipment.

MOCVD technology is employed to precisely analyze and optimize device conditions in order to realize a low noise level.

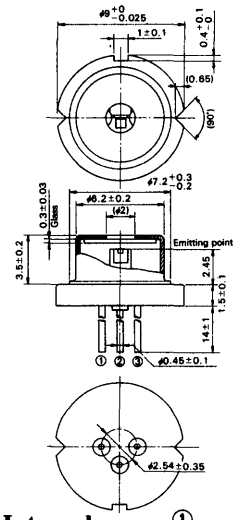
Hermetic sealing of the package achieves high reliability.

Features

- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Multiple longitudinal mode
- Low noise: S/N = 80 dB min.

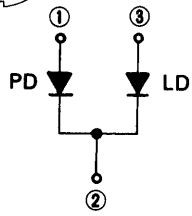


Package Dimensions



(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

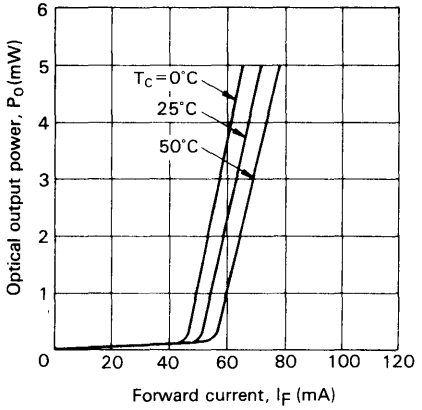
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

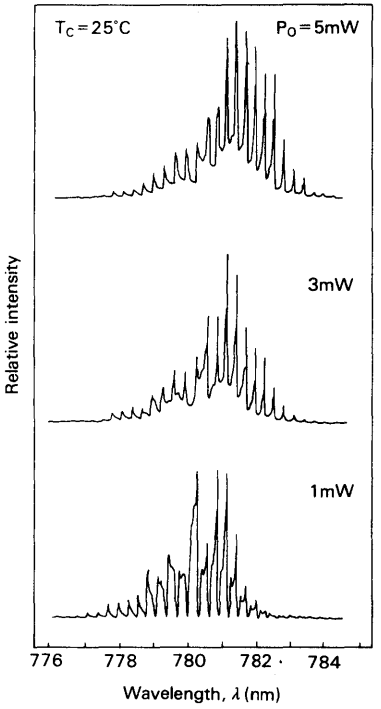
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	80	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.1	0.25	0.6	mW/mA	$\frac{3(mW)}{I(4\ mW) - I(1\ mW)}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	13	14	deg.	P_O = 3 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	25	35	48	deg.	P_O = 3 mW
Monitor current	I_S	0.3	1.0	1.6	mA	$V_{R(PD)}$ = 5 V, P_O = 3±0.03 mW
Noise	S/N	80			dB	P_O = 3 mW, f = 8 MHz, Δf = 100 kHz

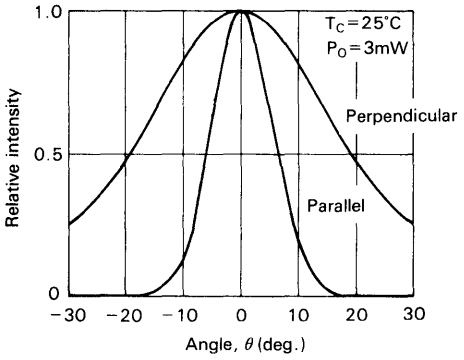
Optical Output Power vs. Forward Current



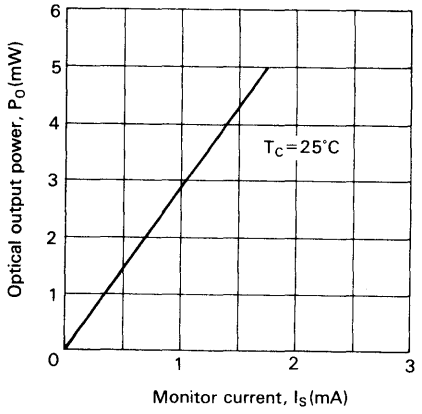
Lasing Spectrum



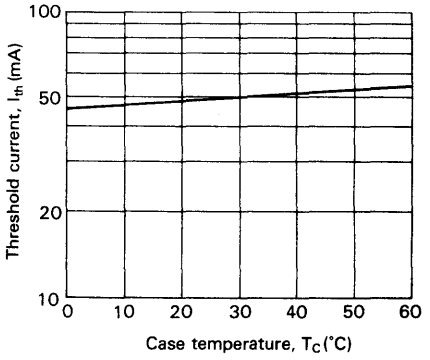
Far Field Pattern



Optical Output Power vs. Monitor Current

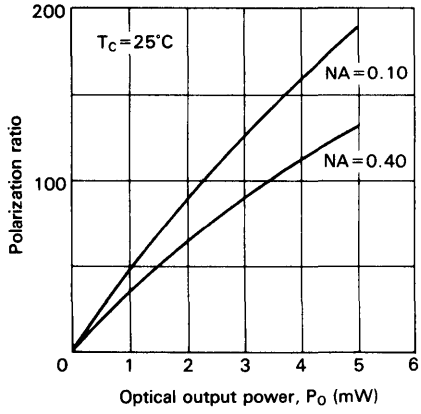


Threshold Current vs. Case Temperature

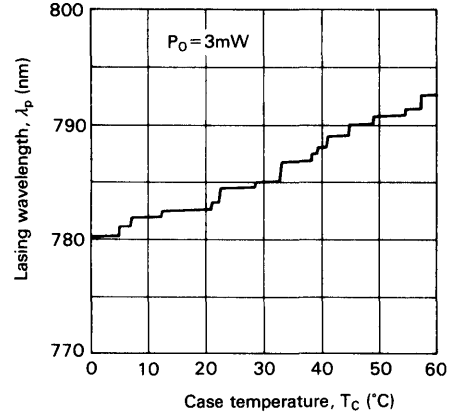


6

Optical Output Power Dependence of Polarization Ratio



Temperature Dependence of Lasing Wavelength



HL7832HG

Laser Diode

Description

HL7832HG is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

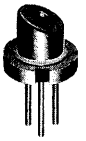
It is suitable as a light source in optical video disc players and various other types of optical equipment.

MOCVD technology is employed to precisely analyze and optimize device conditions in order to realize a low noise level.

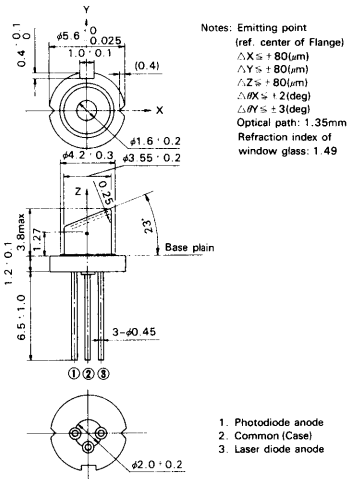
Hermetic sealing of the package achieves high reliability. The package capacity is five times as small as G-type's. Astigmatism is minimized with slanted glass window of cap.

Features

- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Multiple longitudinal mode
- Low noise: S/N = 80 dB min.
- Low astigmatism: | As | $\leqq$ 10 μm

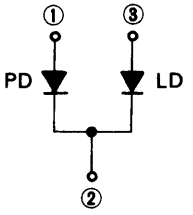


Package Dimensions



HG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

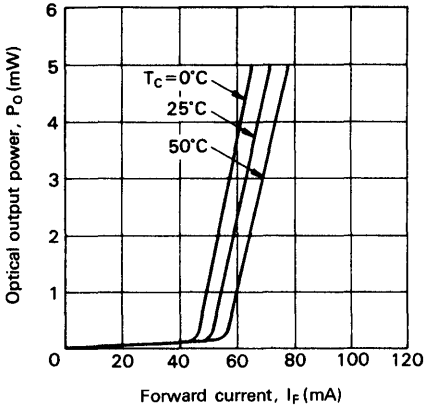
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

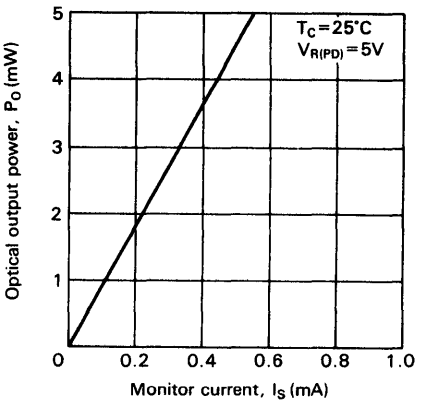
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		50	80	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.1	0.25	0.6	mW/mA	$\frac{3(mW)}{I(4\ mW) - I(1\ mW)}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 5 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 5 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	25	35	48	deg.	P_O = 5 mW
Monitor current	I_S	0.25		1.0	mA	$V_{R(PD)}$ = 5 V, P_O = 5±0.05 mW
Noise	S/N	80			dB	P_O = 5 mW, f = 8 MHz, Δf = 30 kHz

6

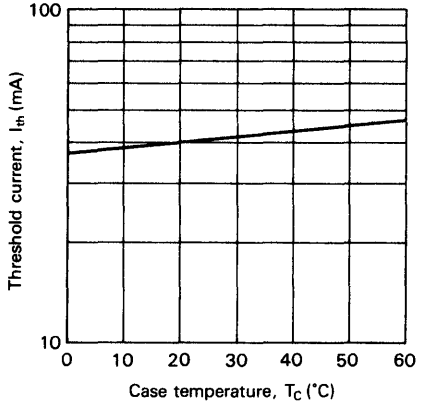
Optical Output Power vs. Forward Current



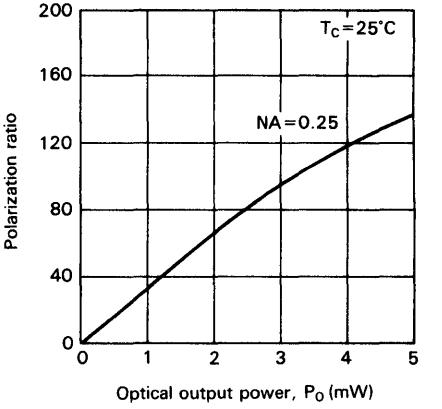
Optical Output Power vs. Monitor Current



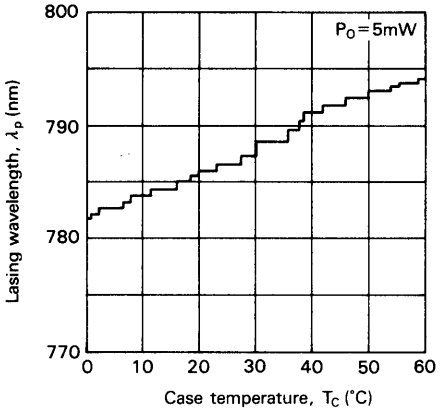
Threshold Current vs. Case Temperature



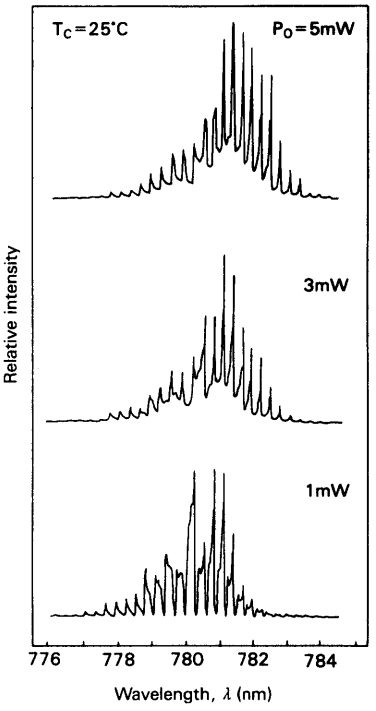
Optical Output Power Dependence of Polarization Ratio



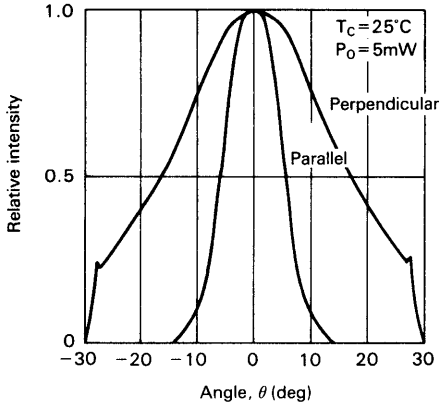
Temperature Dependence of Lasing Wavelength



Lasing Spectrum



Far Field Pattern



6

HL7836G

Laser Diode

Description

HL7836G is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

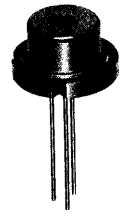
It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

Single positive power supply is available for LD and PD.

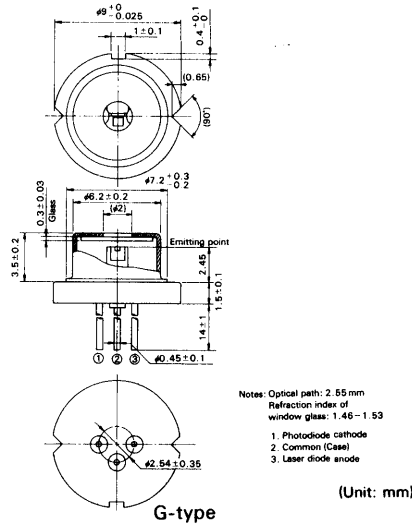
Hermetic sealing of the package achieves high reliability.

Features

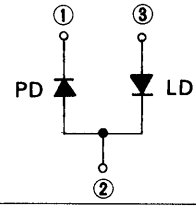
- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Low astigmatism: As = 3 μm typ.
- Single longitudinal mode



Package Dimensions



Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

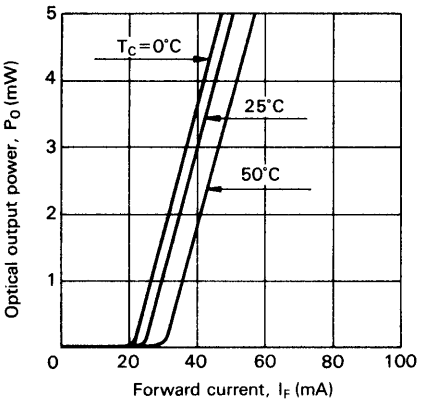
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

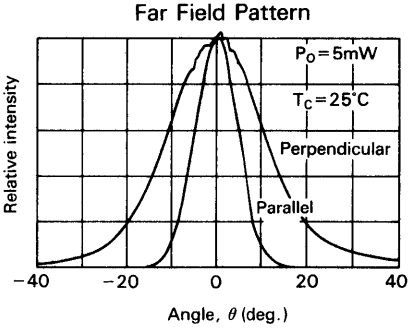
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}	20		60	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.1	0.25	0.45	mW/mA	$\frac{3(\text{mW})}{I(4\text{ mW}) - I(1\text{ mW})}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 5 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	16	deg.	P_O = 5 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	27	35	deg.	P_O = 3 mW
Monitor current	I_S	0.25	1.0	1.65	mA	$V_{R(PD)}$ = 5 V, P_O = 5±0.05 mW

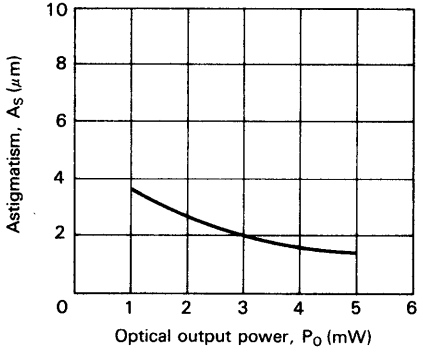
Optical Output Power vs. Forward Current



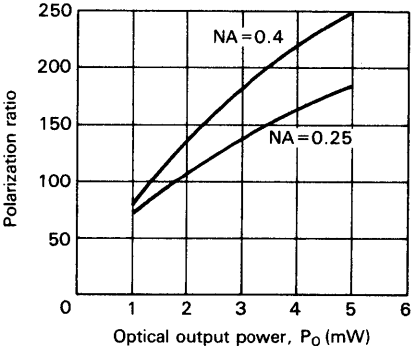
Far Field Pattern



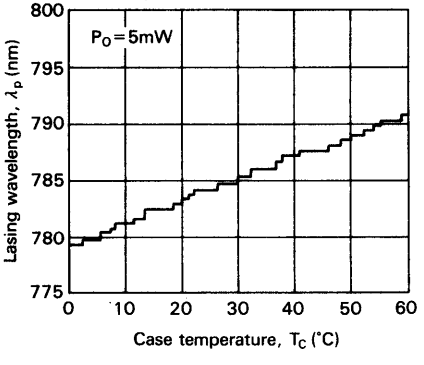
Optical Output Power Dependence of Astigmatism



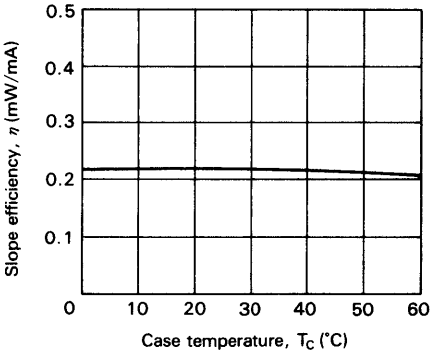
Optical Output Power Dependence of Polarization Ratio



Temperature Dependence of Lasing Wavelength



Temperature Dependence of Slope Efficiency



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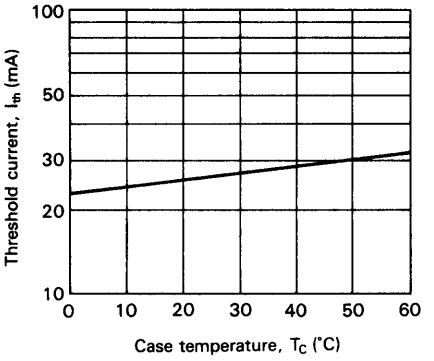
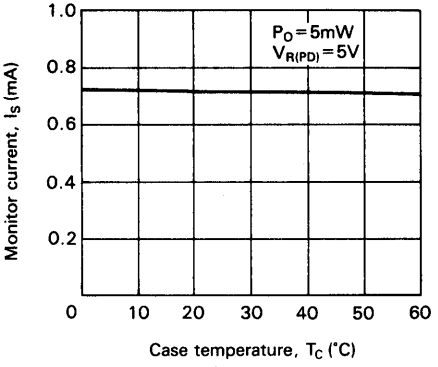
Threshold Current vs.
Case Temperature



Monitor Current vs.
Case Temperature



HL7836MG

Laser Diode

Description

HL7836MG is a 0.78 μm GaAlAs laser diode with double heterojunction structure.

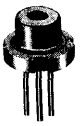
It is suitable as a light source in laser beam printers, laser levelers and various other types of optical equipment.

Single positive power supply is available for LD and PD.

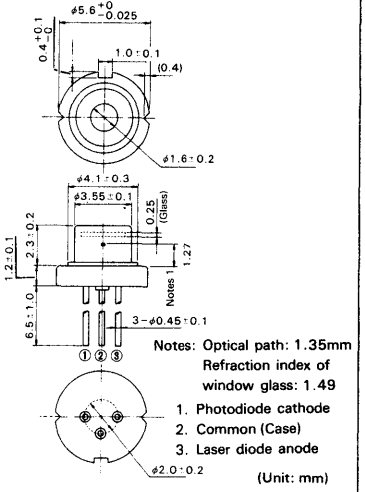
Hermetic sealing of the package achieves high reliability. The package capacity is five times as small as G-type's.

Features

- Visible light output: λ_p = 770–795 nm
- Built-in photodiode for monitoring laser output
- Low astigmatism: As = 3 μm typ.
- Single longitudinal mode



Package Dimensions



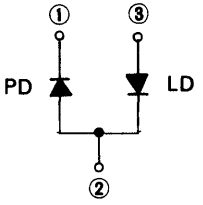
Notes: Optical path: 1.35mm
Refraction index of window glass: 1.49

1. Photodiode cathode
2. Common (Case)
3. Laser diode anode

(Unit: mm)

MG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

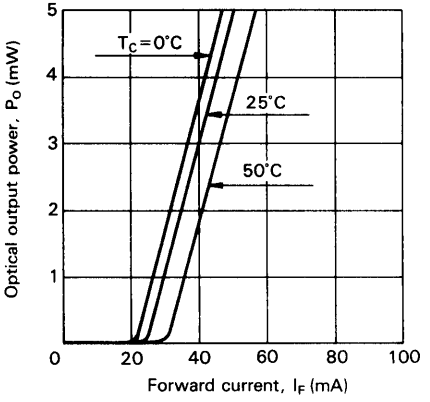
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

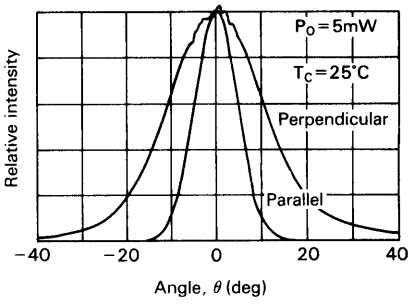
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}	20		60	mA	
Optical output power	P_O	5			mW	Kink free
Slope efficiency	η	0.1	0.25	0.45	mW/mA	$\frac{3(\text{mW})}{I\,(4\text{ mW}) - I\,(1\text{ mW})}$
Lasing wavelength	λ_p	770	785	795	nm	P_O = 5 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	16	deg.	P_O = 5 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	27	35	deg.	P_O = 5 mW
Monitor current	I_S	0.25	0.6	1.0	mA	$V_{R(PD)}$ = 5 V, P_O = 5±0.05 mW

6

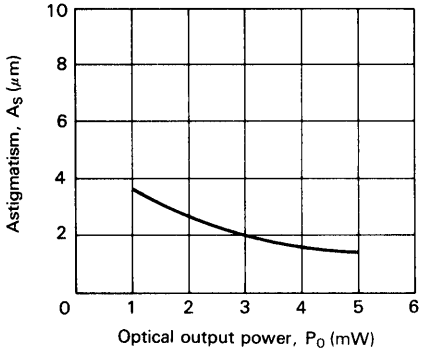
Optical Output Power vs. Forward Current



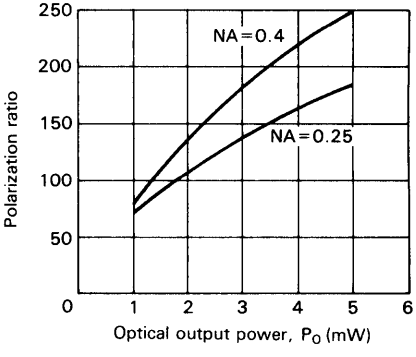
Far Field Pattern



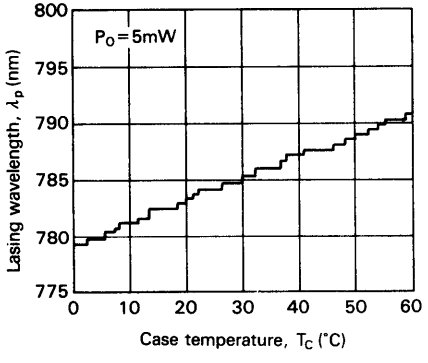
Optical Output Power Dependence of Astigmatism



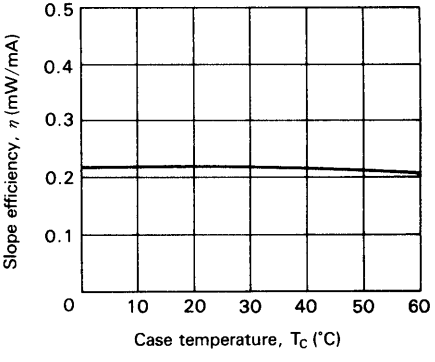
Optical Output Power Dependence of Polarization Ratio



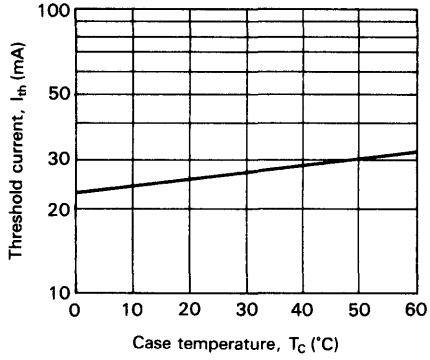
Temperature Dependence of Lasing Wavelength



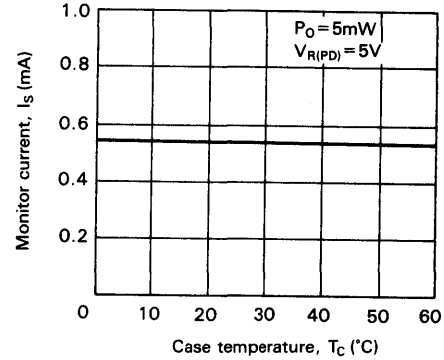
Temperature Dependence of Slope Efficiency



Threshold Current vs.
Case Temperature



Monitor Current vs.
Case Temperature



6

HL7838G

Laser Diode

Description

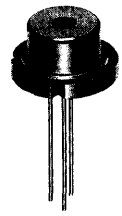
HL7838G is a high-power 0.78 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in laser beam printers, laser levelers, optical disc memories and various other types of optical equipment.

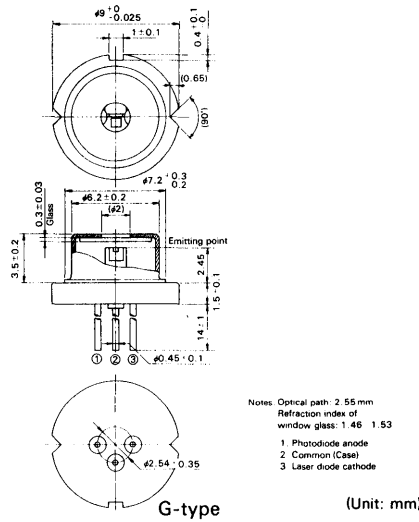
Hermetic sealing of the package achieves high reliability.

Features

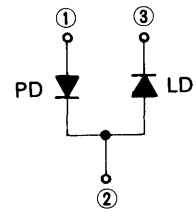
- Visible light output: λ_p = 770–795 nm
- 20 mW (CW), 30 mW (pulse) operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



Package Dimensions



Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	20	mW
Pulse optical output power	$P_{O(pulse)}$	30*	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

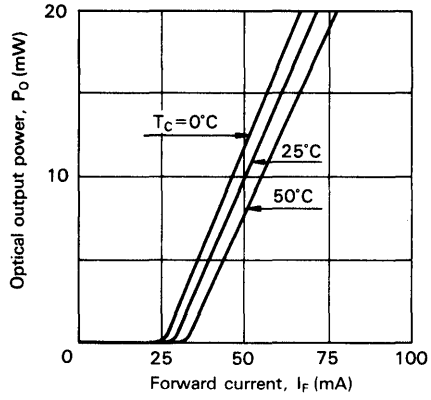
*PW ≦ 1 μs, duty 50%

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

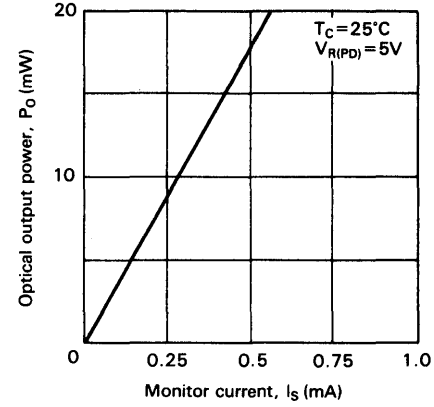
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}	20		70	mA	
Optical output power	P_O	20			mW	Kink free
Slope efficiency	η	0.3	0.45		mW/mA	$\frac{12(mW)}{I(16\ mW) - I(4\ mW)}$
Lasing wavelength	λ_p	770	780	795	nm	P_O = 20 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	10	14	deg.	P_O = 20 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	20	26	35	deg.	P_O = 20 mW
Monitor current	I_S	30			μA	$V_{R(PD)}$ = 5 V, P_O = 2 mW

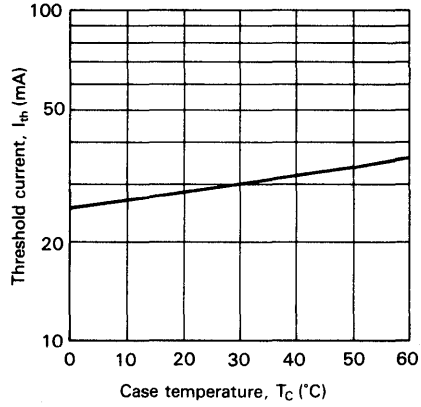
Optical Output Power vs. Forward Current



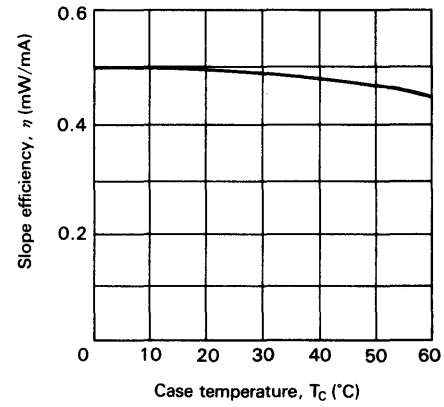
Optical Output Power vs. Monitor Current



Threshold Current vs. Case Temperature



Temperature Dependence of Slope Efficiency



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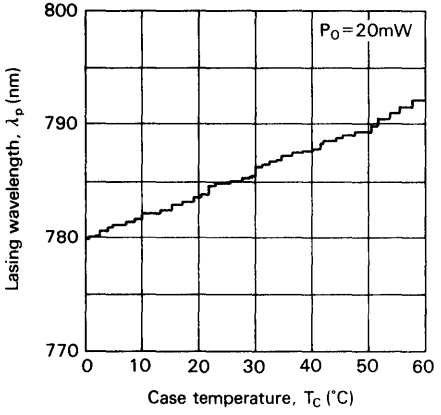
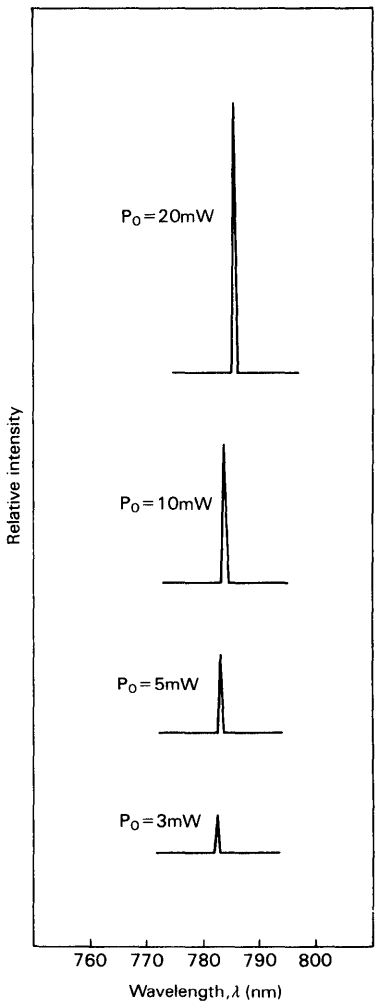
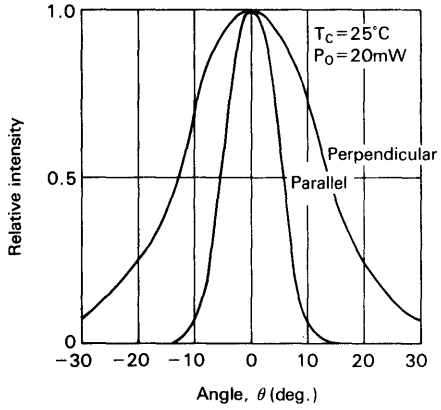
Temperature Dependence of Lasing Wavelength



Lasing Spectrum



Far Field Pattern



HL7851G

Preliminary

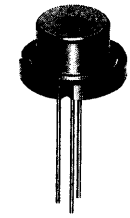
High-Power Visible Laser Diode

Description

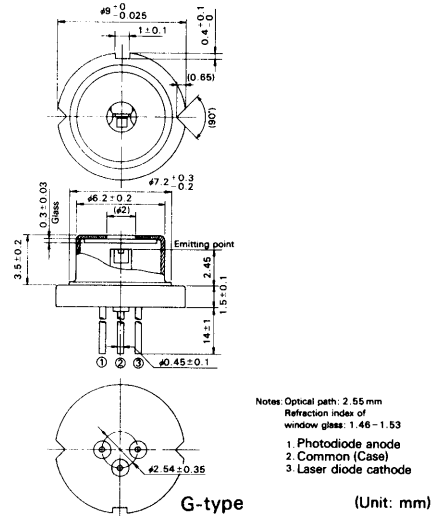
HL7851G is a high-power 0.78μm GaA1As laser diode with multi quantum well structure. It is suitable as a light source in optical disc memories and various other types of optical equipment. Hermetic sealing of the package achieves high reliability.

Features

- Visible light output; $\lambda p = 785$nm typ.
- Small aspect ratio; 9:25
- High-power output; 50mW CW operation
- Built-in photodiode for monitoring power output



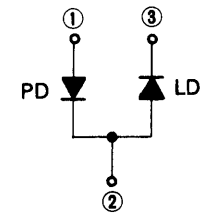
Package Dimensions



Notes: Optical path: 2.55 mm
Refraction index of window glass: 1.46 – 1.53

1. Photodiode anode
2. Common (Case)
3. Laser diode cathode

Internal Circuit



Absolute Maximum Ratings ($T_c = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Optical output power (pulse)	P_O (pulse)	60*	mW
Laserdiode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 ~ +60	°C
Storage temperature	T_{stg}	−40 ~ +85	°C

*Pulse condition pw ≤ 1μs duty ≤ 50%

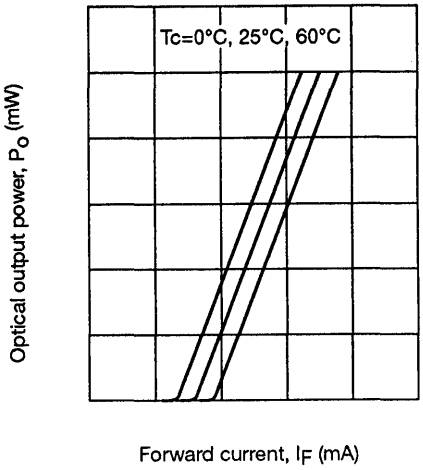
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_c = 25°C$)

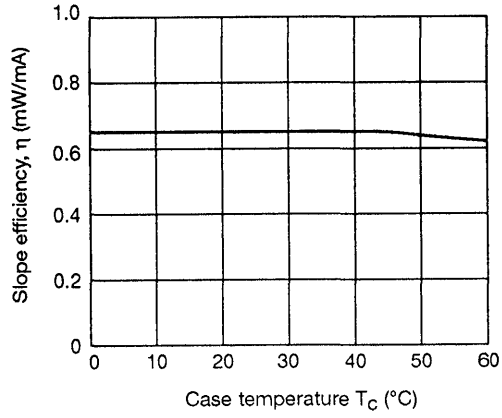
Items	Symbols	min.	typ.	max.	Unit	Test condition
Optical output power	P_O	50	—	—	mW	Kink free
Threshold current	I_{th}	—	80	—	mA	
Operating voltage	V_{op}	—	—	2.7	V	$P_o = 50$mW
Operating current	I_{op}	—	180	—	mA	$P_o = 50$mW
Slope efficiency	η	—	0.6	—	mW/mA	$\frac{40(\text{mW})}{I_{(45\text{mW})} - I_{(5\text{mW})}}$
Lasing wavelength	λ_p	775	785	795	nm	$P_O = 50$mW
Beam divergence parallel to the junction	$\theta_{//}$	6	9	12	deg.	$P_O = 50$mW
Beam divergence perpendicular to the junction	$\theta\perp$	20	25	32	deg.	$P_O = 50$mW
Monitor Current	I_S	0.03	—	—	mA	$P_O = 5$mW, $V_R = 5$V
Astigmatism	A_S	—	—	12	μm	$P_O = 5$mW, NA = 0.4

6

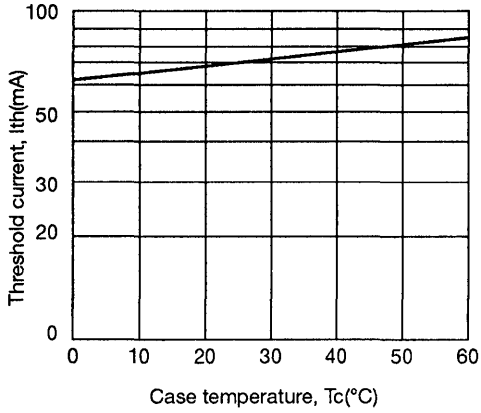
OPTICAL OUPUT POWER vs FORWARD CURRENT



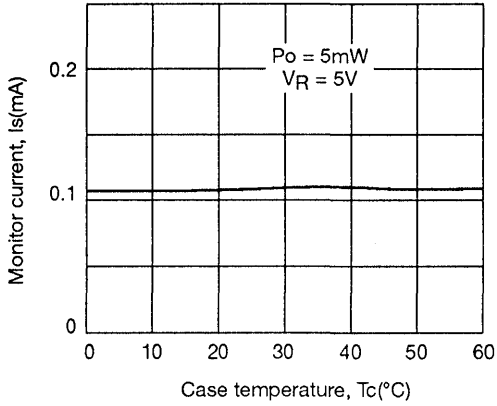
TEMPERATURE DEPENDENCE OF SLOPE EFFICIENCY



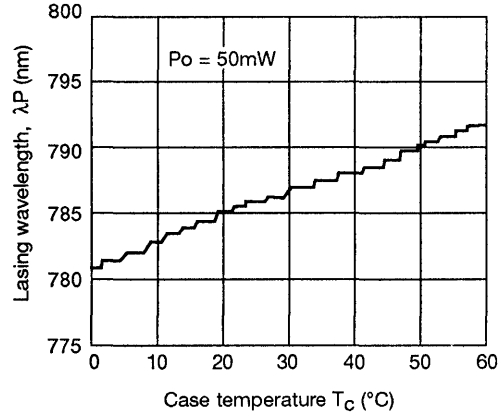
THRESHOLD CURRENT vs CASE TEMPERATURE



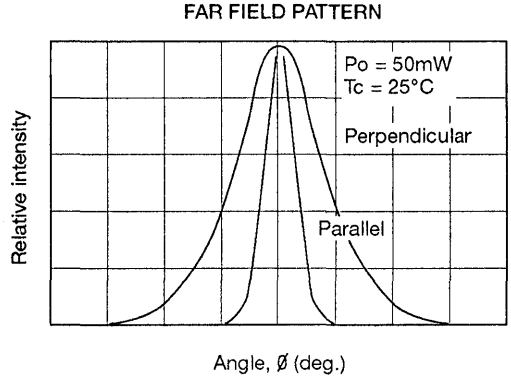
MONITOR CURRENT vs CASE TEMPERATURE



TEMPERATURE DEPENDENCE OF LASING WAVELENGTH



FAR FIELD PATTERN



HLP1400

Laser Diode

Description

HLP1400 is a 0.8 μm GaAlAs laser diode with double heterojunction structure.

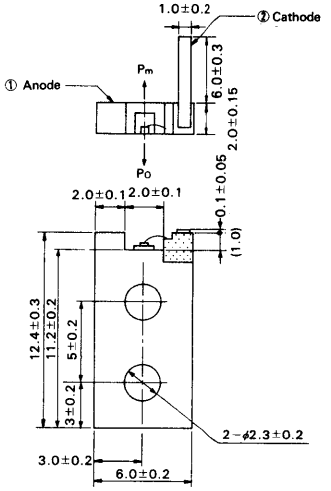
It is suitable as a light source in fiberoptic communications, optical disc memories or various other types of optical equipment.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Infrared light output: λ_p = 800–850 nm
- 15 mW CW operation at room temperature
- Single longitudinal mode

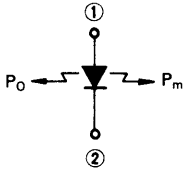
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	15	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

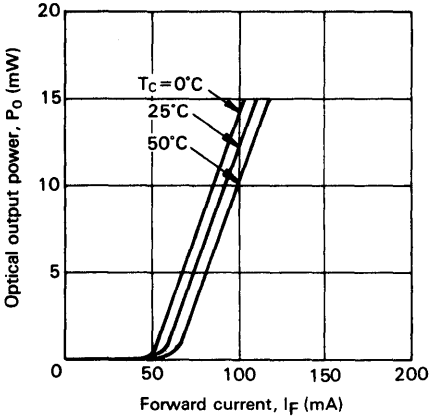
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

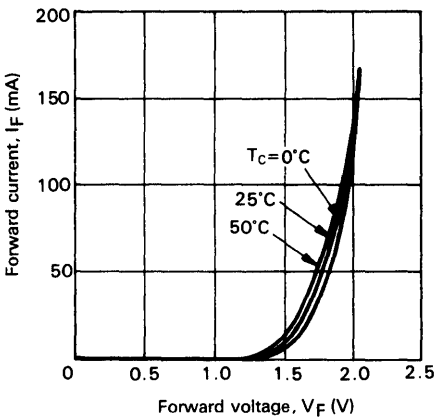
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	15			mW	Kink free
		4	5		mW	$I_F = I_{th} + 25$ mA
Monitor power	P_m	2			mW	$I_F = I_{th} + 25$ mA
Lasing wavelength	λ_p	800	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$		10		deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$		25		deg.	P_O = 10 mW

6

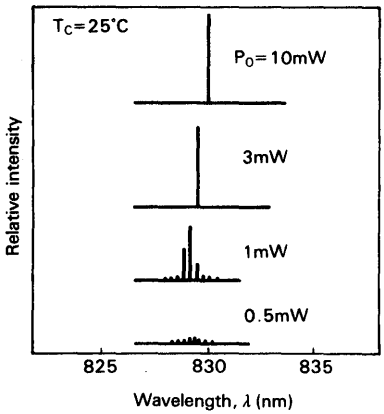
Optical Output Power vs. Forward Current



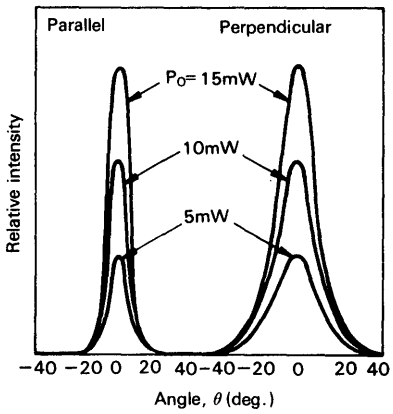
Forward Current vs. Forward Voltage



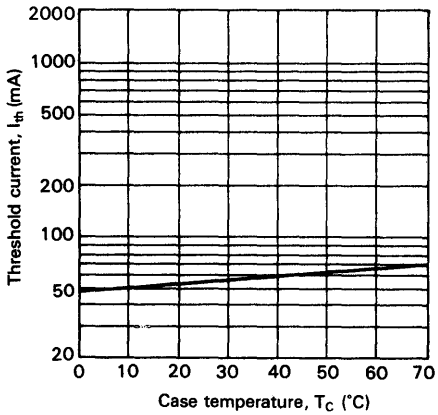
Lasing Spectrum



Far Field Pattern



Threshold Current vs. Case Temperature



HL8311E

Laser Diode

Description

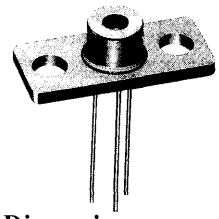
HL8311E is a 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in optical disc memories and various other types of optical equipment.

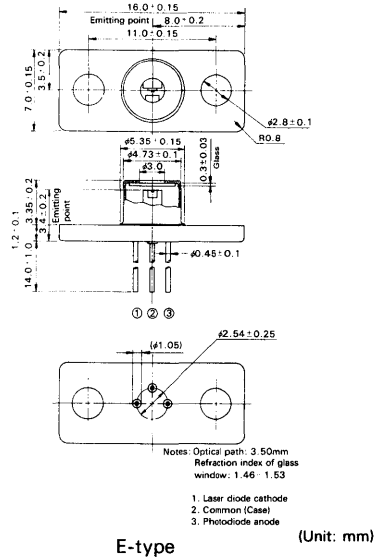
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 800–850 nm
- 15 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode

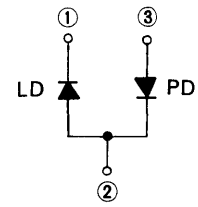


Package Dimensions



E-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	15	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

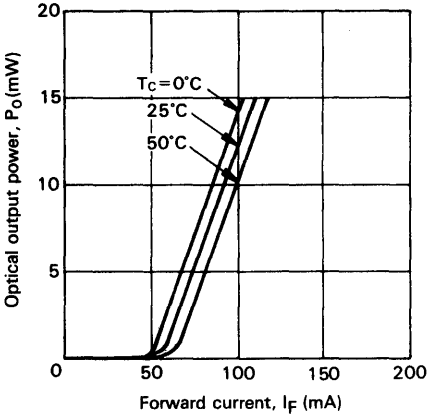
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

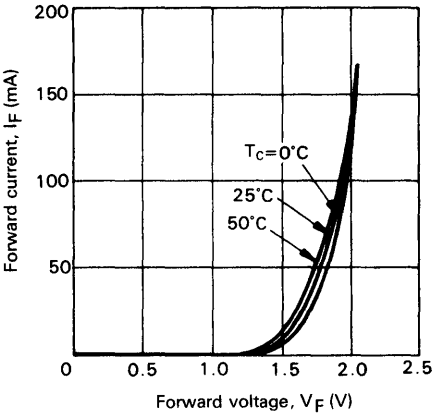
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	15			mW	Kink free
Slope efficiency	η	0.16	0.28		mW/mA	$\frac{8(mW)}{I(12\ mW) - I(4\ mW)}$
Lasing wavelength	λ_p	800	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	35	deg.	P_O = 10 mW
Monitor current	I_S	0.2		3.0	mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

6

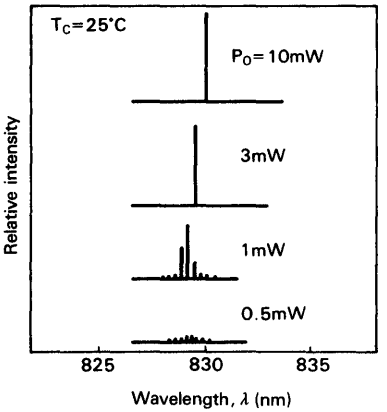
Optical Output Power vs. Forward Current



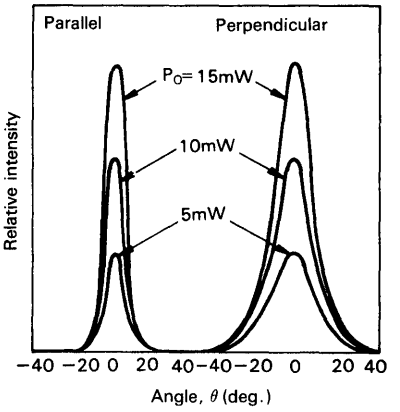
Forward Current vs. Forward Voltage



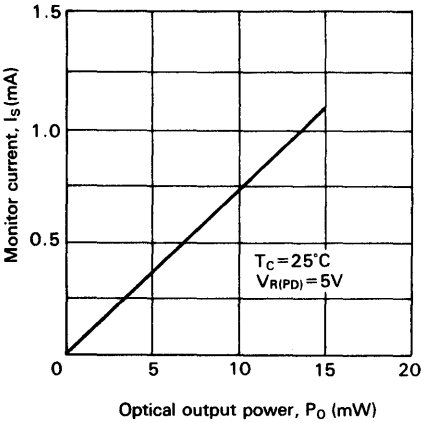
Lasing Spectrum



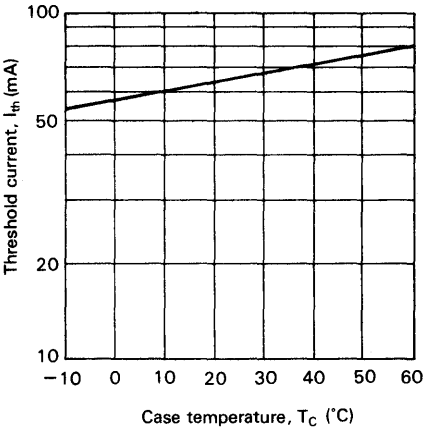
Far Field Pattern



Monitor Current vs. Optical Output Power



Threshold Current vs. Case Temperature



HL8311G

Laser Diode

Description

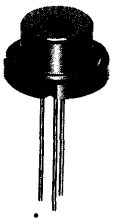
HL8311G is a 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in optical disc memories and various other types of optical equipment.

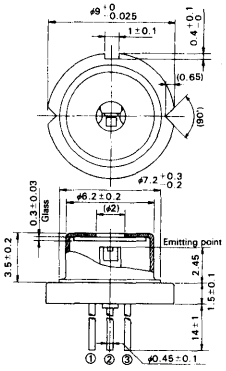
Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 800–850 nm
- 15 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



Package Dimensions

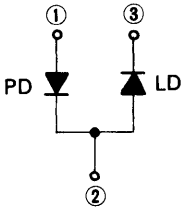


Notes: Optical path: 2.55 mm
Refraction index of window glass: 1.48 – 1.53

1. Photodiode anode
2. Common (Case)
3. Laser diode cathode

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

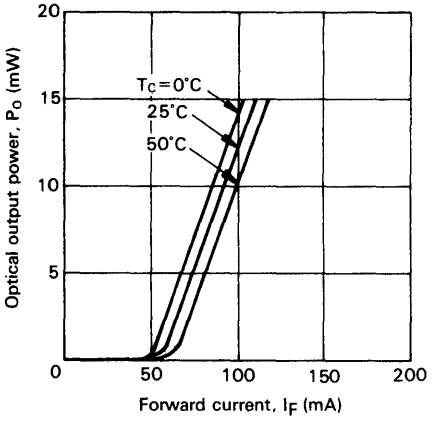
Items	Symbols	Values	Units
Optical output power	P_O	15	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

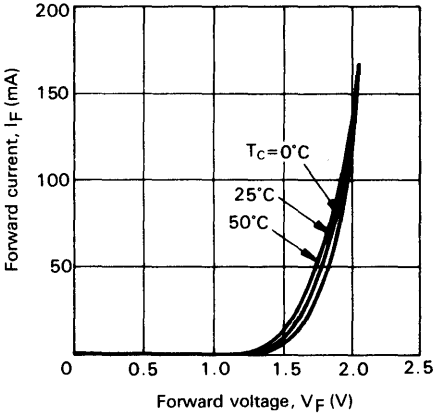
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	15			mW	Kink free
Slope efficiency	η	0.16	0.28		mW/mA	$\frac{8(mW)}{I(12\ mW) - I(4\ mW)}$
Lasing wavelength	λ_p	800	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	35	deg.	P_O = 10 mW
Monitor current	I_S	0.2		3.0	mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

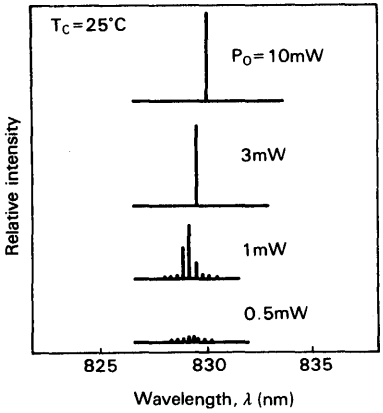
Optical Output Power vs. Forward Current



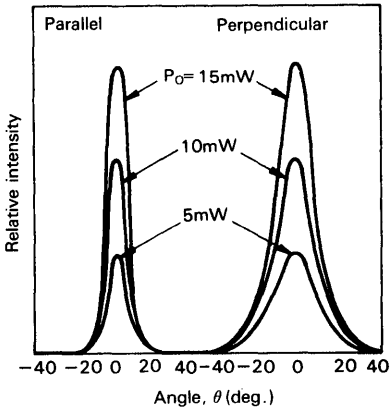
Forward Current vs. Forward Voltage



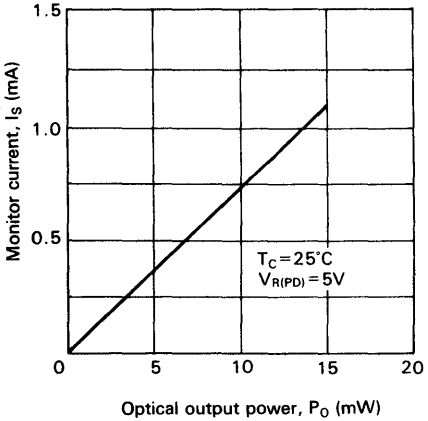
Lasing Spectrum



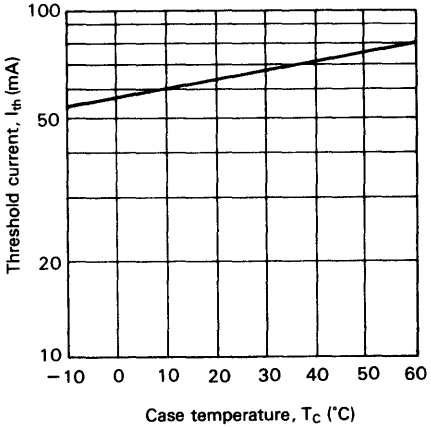
Far Field Pattern



Monitor Current vs. Optical Output Power



Threshold Current vs. Case Temperature



HL8312E

Laser Diode

Description

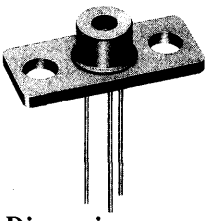
HL8312E is a high-power 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in optical disc memories and various other types of optical equipment.

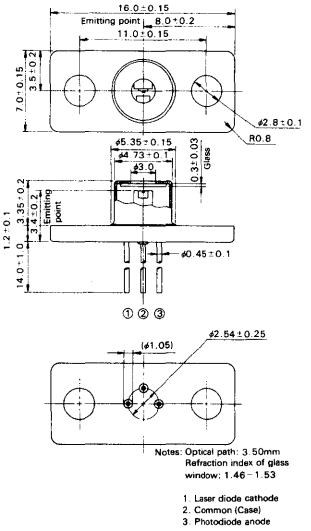
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 810–850 nm
- 20 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode

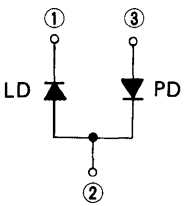


Package Dimensions



E-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

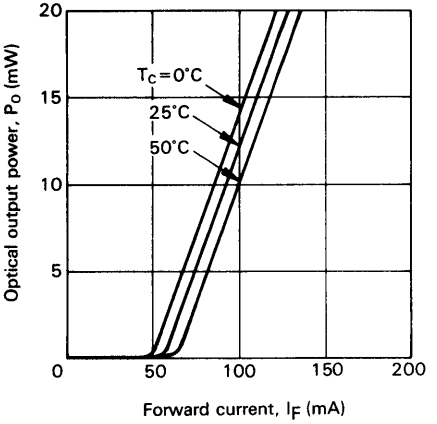
Items	Symbols	Values	Units
Optical output power	P_O	20	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

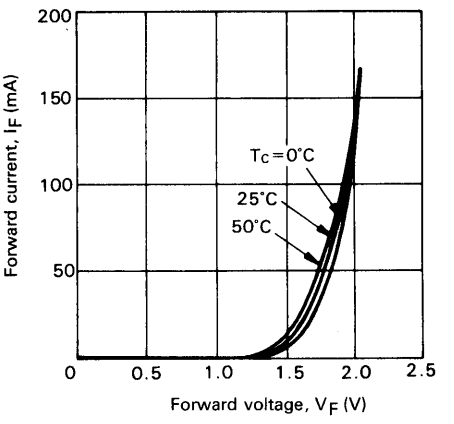
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	20			mW	Kink free
Slope efficiency	η	0.16	0.28		mW/mA	$\frac{12(mW)}{I\,(16\,mW) - I\,(4\,mW)}$
Lasing wavelength	λ_p	810	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	35	deg.	P_O = 10 mW
Monitor current	I_S	0.2		3.0	mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

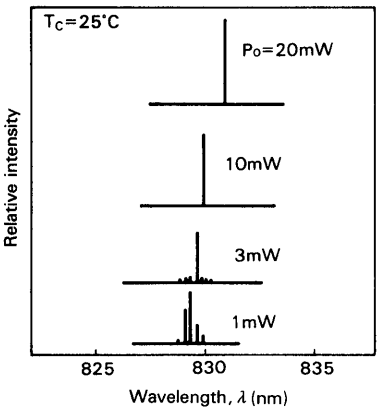
Optical Output Power vs. Forward Current



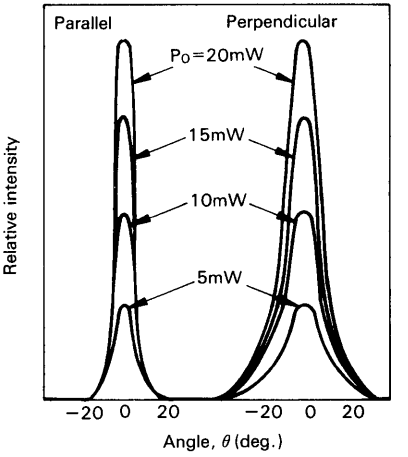
Forward Current vs. Forward Voltage



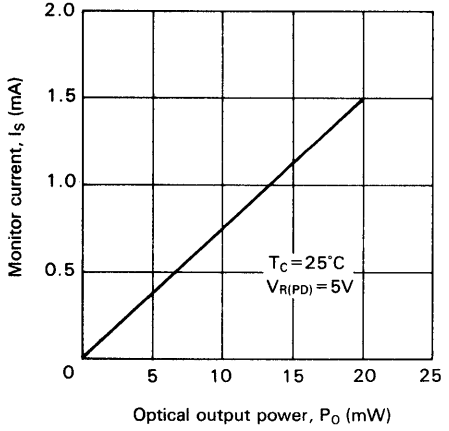
Lasing Spectrum



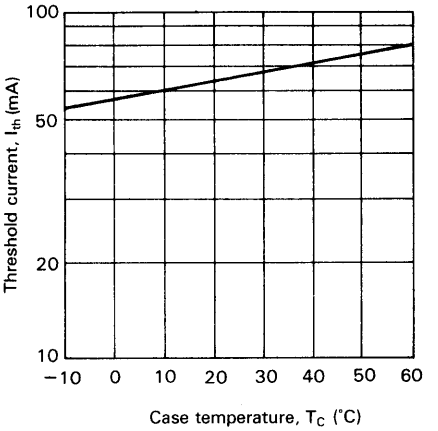
Far Field Pattern



Monitor Current vs. Optical Output Power



Threshold Current vs. Case Temperature



HL8312G

Laser Diode

Description

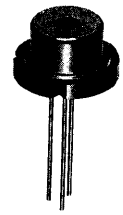
HL8312G is a high-power 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in optical disc memories and various other types of optical equipment.

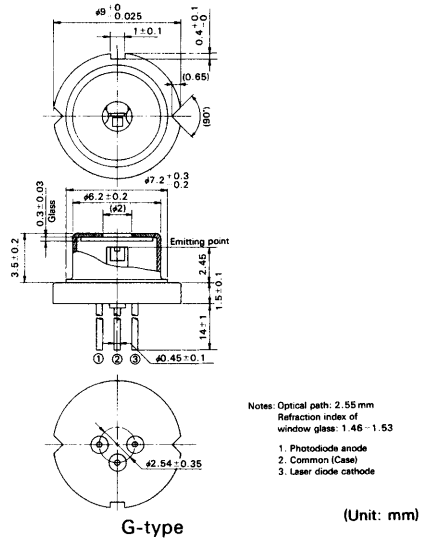
Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 810–850 nm
- 20 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



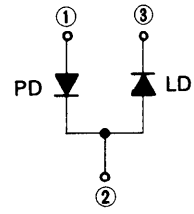
Package Dimensions



G-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

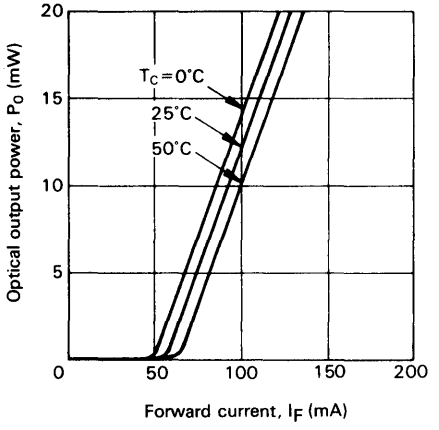
Items	Symbols	Values	Units
Optical output power	P_O	20	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

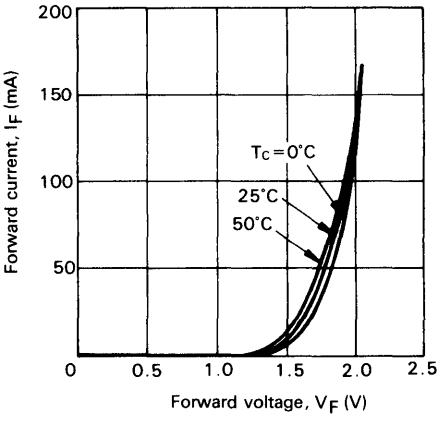
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	20			mW	Kink free
Slope efficiency	η	0.16	0.28		mW/mA	$\frac{12(mW)}{I(16\ mW) - I(4\ mW)}$
Lasing wavelength	λ_p	810	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	35	deg.	P_O = 10 mW
Monitor current	I_S	0.2		3.0	mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

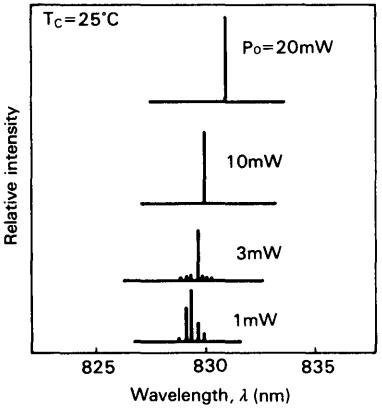
Optical Output Power vs. Forward Current



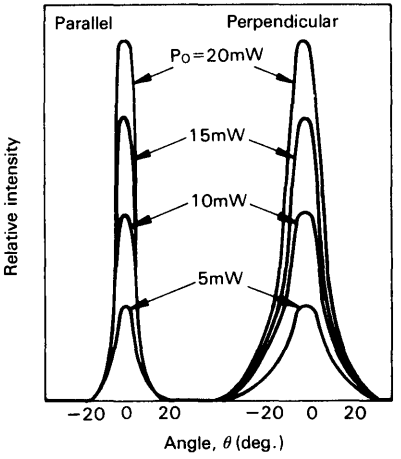
Forward Current vs. Forward Voltage



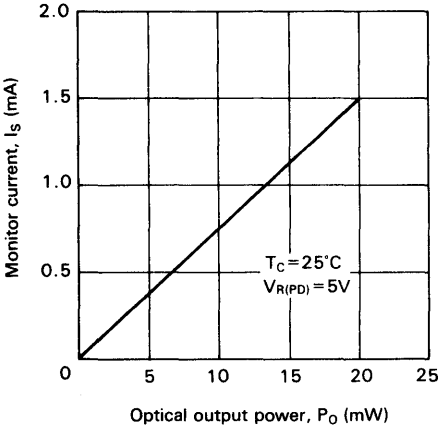
Lasing Spectrum



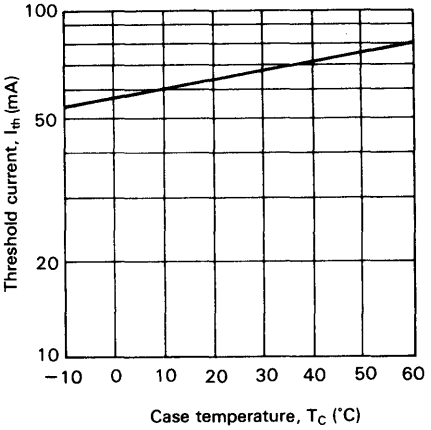
Far Field Pattern



Monitor Current vs. Optical Output Power



Threshold Current vs. Case Temperature



HL8314E

Laser Diode

Description

HL8314E is a high-power 0.8 μm GaAlAs laser diode with double heterojunction structure.

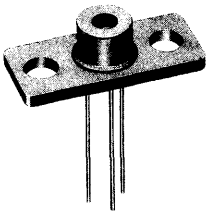
It is suitable as a light source in optical disc memories and various other types of optical equipment.

High power output is obtained through non-symmetrical coating technology for chip mirror facets.

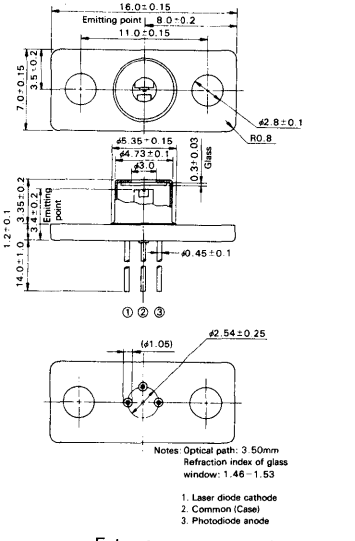
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 810–850 nm
- 30 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode

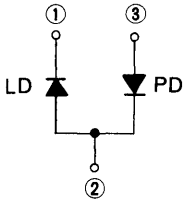


Package Dimensions



E-type (Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

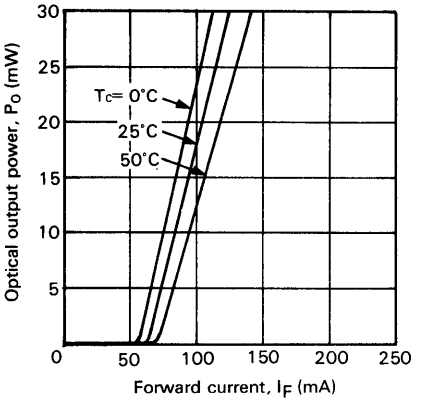
Items	Symbols	Values	Units
Optical output power	P_O	30	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

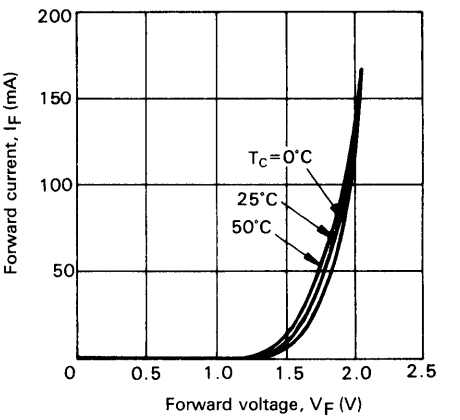
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	30			mW	Kink free
Slope efficiency	η	0.3	0.5		mW/mA	$\frac{18(mW)}{I(24\,mW) - I(6\,mW)}$
Lasing wavelength	λ_p	810	830	850	nm	P_O = 30 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 30 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	32	deg.	P_O = 30 mW
Monitor current	I_S	20			μA	$V_{R(PD)}$ = 5 V, P_O = 3mW

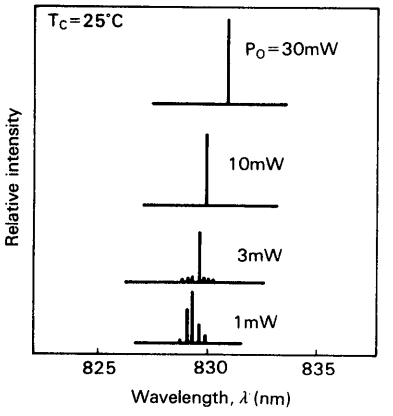
Optical Output Power vs. Forward Current



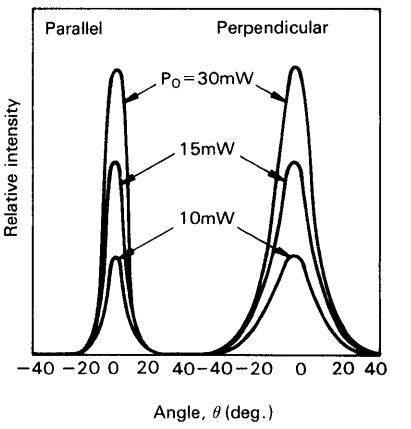
Forward Current vs. Forward Voltage



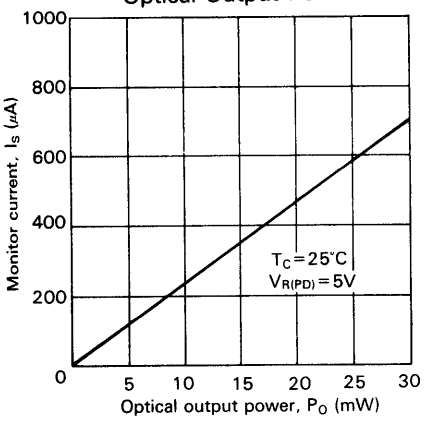
Lasing Spectrum



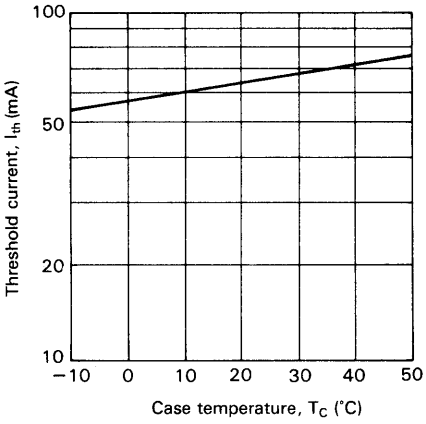
Far Field Pattern



Monitor Current vs. Optical Output Power



Threshold Current vs. Case Temperature



HL8314G

Laser Diode

Description

HL8314G is a high-power 0.8 μm GaAlAs laser diode with double heterojunction structure.

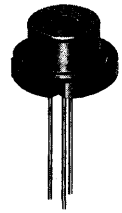
It is suitable as a light source in optical disc memories and various other types of optical equipment.

High power output is obtained through non-symmetrical coating technology for chip mirror facets.

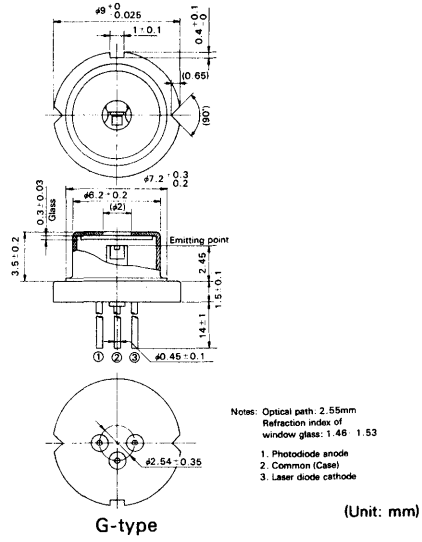
Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 810–850 nm
- 30 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



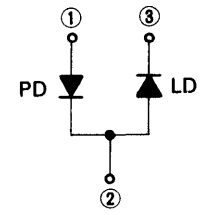
Package Dimensions



G-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	30	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	30			mW	Kink free
Slope efficiency	η	0.3	0.5		mW/mA	$\frac{18(mW)}{I(24\ mW) - I(6\ mW)}$
Lasing wavelength	λ_p	810	830	850	nm	P_O = 30 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 30 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	32	deg.	P_O = 30 mW
Monitor current	I_S	20			μA	$V_{R(PD)}$ = 5 V, P_O = 3 mW

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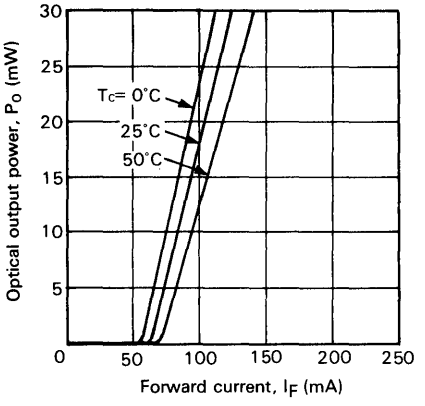
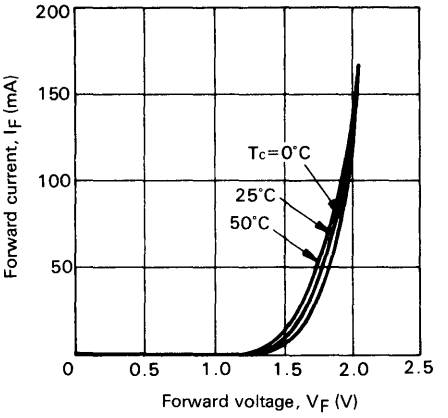
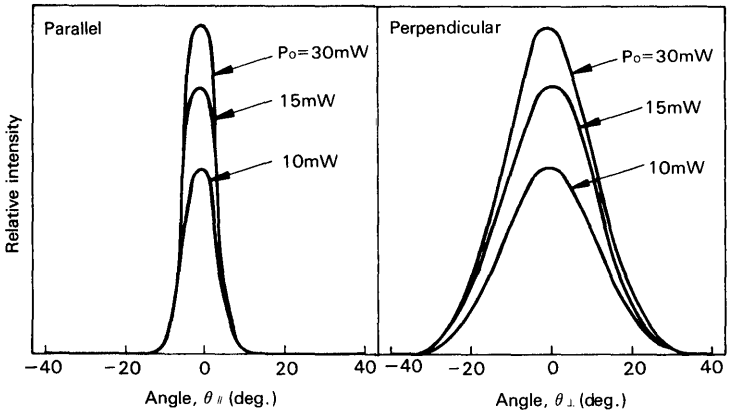
Optical Output Power vs. Forward Current



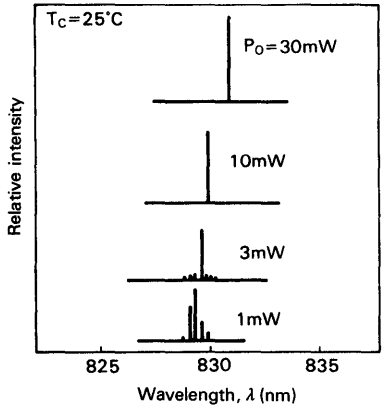
Forward Current vs. Forward Voltage



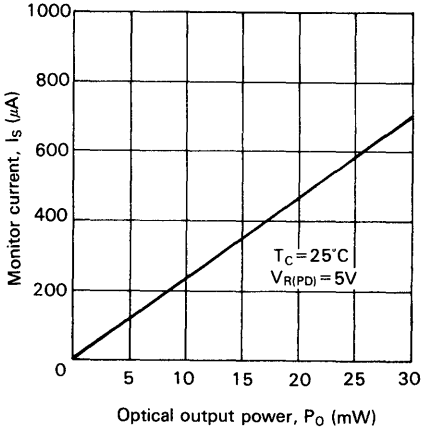
Far Field Pattern



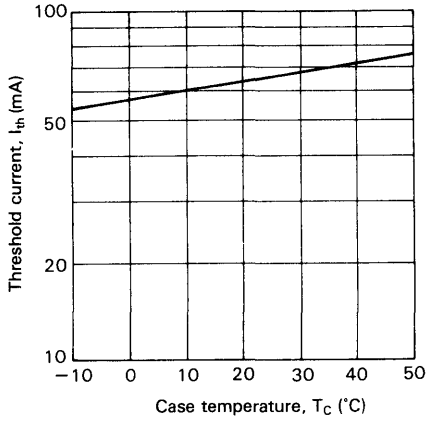
Lasing Spectrum



Monitor Current vs. Optical Output Power



Threshold Current vs.
Case Temperature



6

HL8315E

Laser Diode

Description

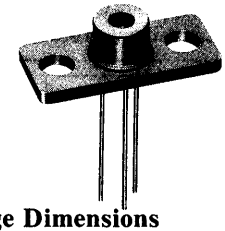
HL8315E is a high-power 0.8 μm GaAlAs laser diode with double heterojunction structure.

It is suitable as a light source in optical disc memories and various other types of optical equipment.

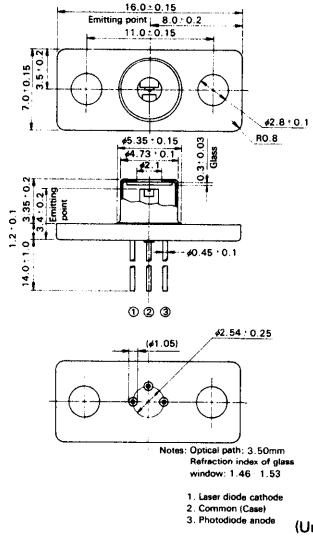
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 800–850 nm
- 20 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Fast pulse response of photodiode: t_r, t_f = 50 ns typ.
- Single longitudinal mode



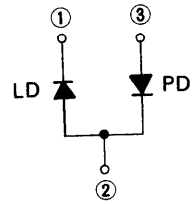
Package Dimensions



(Unit: mm)

E-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

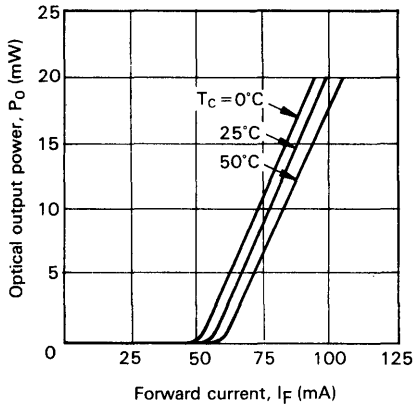
Items	Symbols	Values	Units
Optical output power	P_O	20	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +50	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

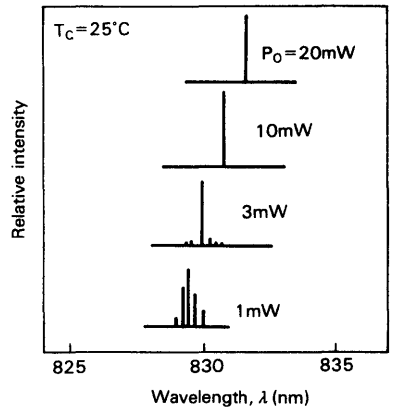
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		60	90	mA	
Optical output power	P_O	20			mW	Kink free
Slope efficiency	η	0.16	0.3		mW/mA	$\frac{12(mW)}{I\,(16\,mW) - I\,(4\,mW)}$
Lasing wavelength	λ_p	800	830	850	nm	P_O = 10 mW
Beam divergence parallel to the junction	$\theta_{//}$	7	11	15	deg.	P_O = 10 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	19	25	35	deg.	P_O = 10 mW
Monitor current	I_S	1.0		3.5	mA	$V_{R(PD)}$ = 5 V, P_O = 10 mW

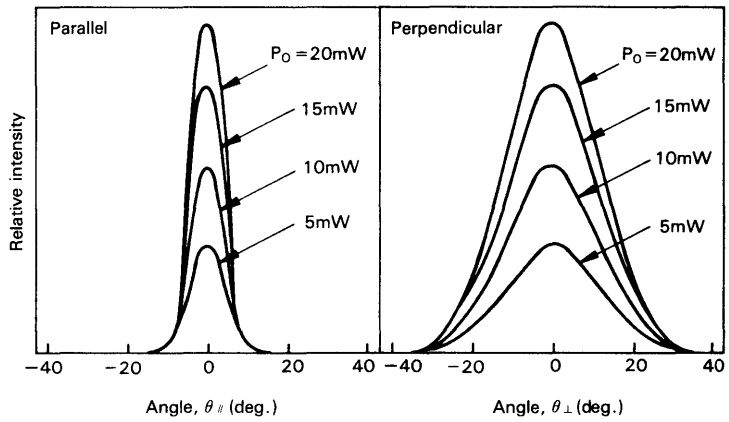
Optical Output Power vs. Forward Current



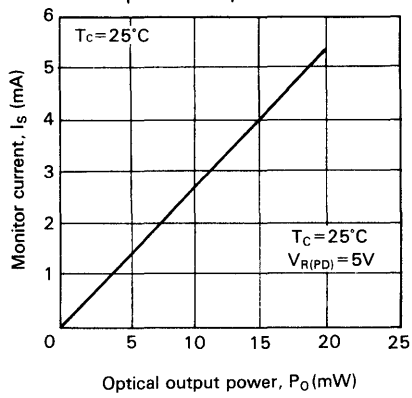
Lasing Spectrum



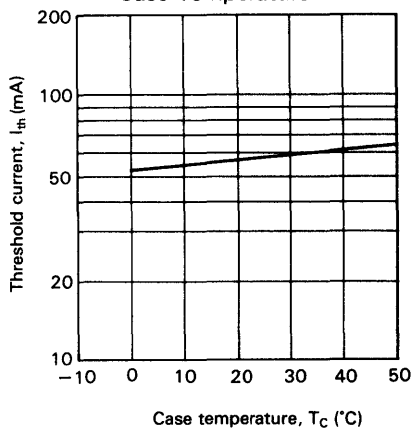
Far Field Pattern



Monitor Current vs. Optical Output Power



Threshold Current vs. Case Temperature



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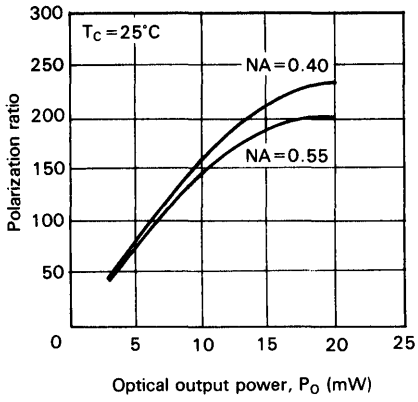
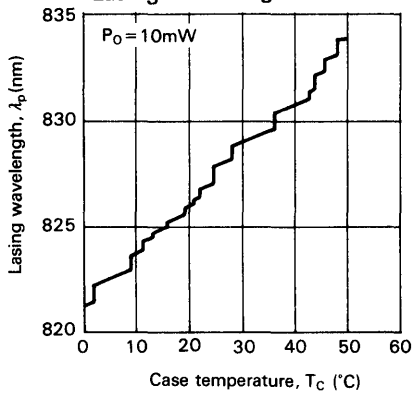
Optical Output Power Dependence of Polarization Ratio



Temperature Dependence of Lasing Wavelength



HL8318E

Laser Diode

Description

HL8318E is a high-power 0.8 μm GaAlAs laser diode with double heterojunction structure.

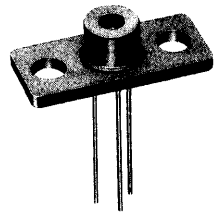
It is suitable as a light source in optical disc memories and various other types of optical equipment.

Single positive power supply is available for LD and PD.

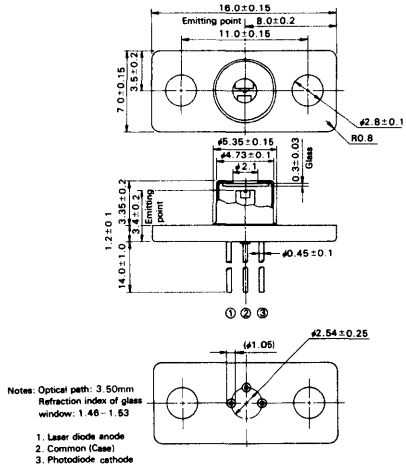
A screw-on type package facilitates the adjustment of optical components. Hermetic sealing of the package achieves high reliability.

Features

- Infrared light output: λ_p = 810–850 nm
- 40 mW (CW), 50 mW (pulse) operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



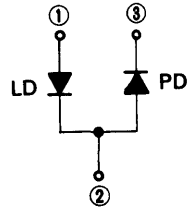
Package Dimensions



(Unit: mm)

E-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	40	mW
Pulse optical output power	$P_{O(pulse)}$	50*	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

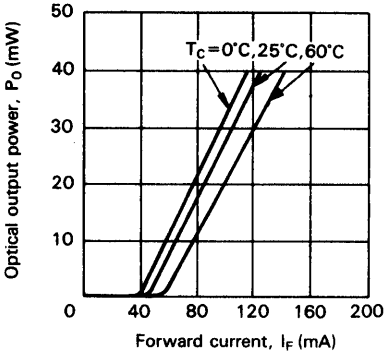
*PW ≦ 1 μs, duty 50%

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

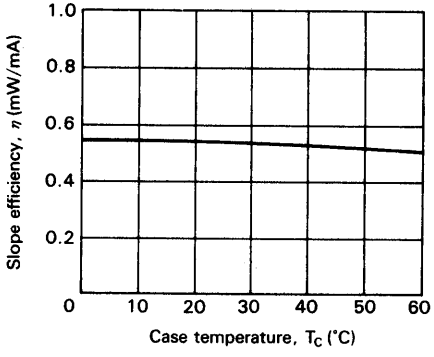
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		40	70	mA	
Optical output power	P_O	40			mW	Kink free
Slope efficiency	η	0.4	0.5	0.9	mW/mA	$\frac{24(mW)}{I(32\ mW) - I(8\ mW)}$
Lasing wavelength	λ_p	810	830	850	nm	P_O = 40 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 40 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	32	deg.	P_O = 40 mW
Monitor current	I_S	40	100	240	μA	$V_{R(PD)}$ = 5 V, P_O = 4mW

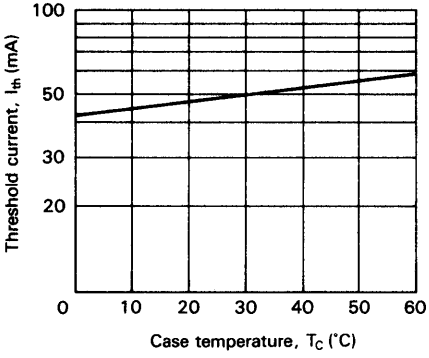
Optical Output Power vs. Forward Current



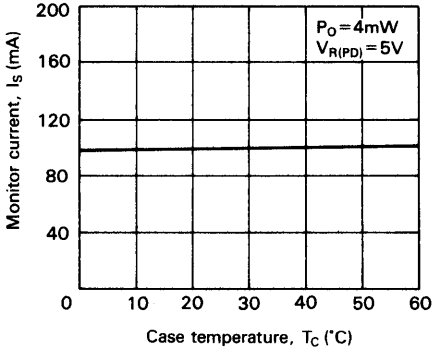
Temperature Dependence of Slope Efficiency



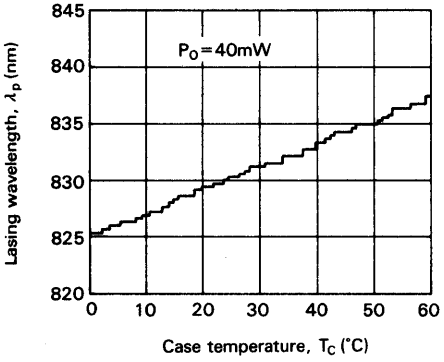
Threshold Current vs. Case Temperature



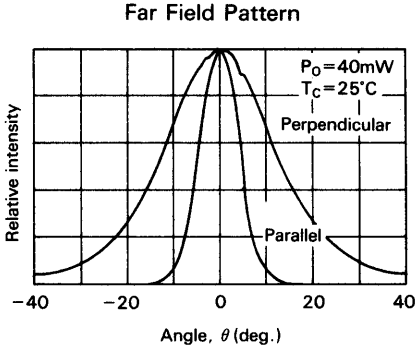
Monitor Current vs. Case Temperature



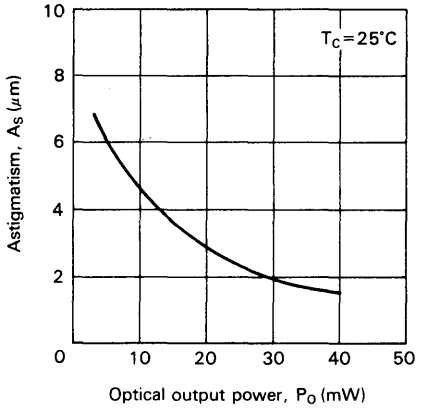
Temperature Dependence of Lasing Wavelength



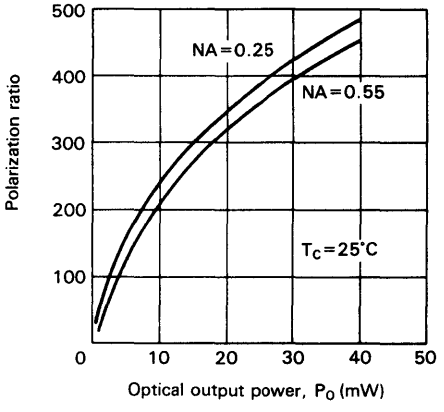
Far Field Pattern



Optical Output Power Dependence of Astigmatism



Optical Output Power Dependence of Polarization Ratio



HL8318G

Laser Diode

Description

HL8318G is a high-power 0.8 μm GaAlAs laser diode with double heterojunction structure.

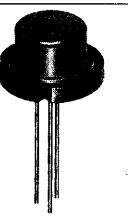
It is suitable as a light source in optical disc memories and various other types of optical equipment.

Single positive power supply is available for LD and PD.

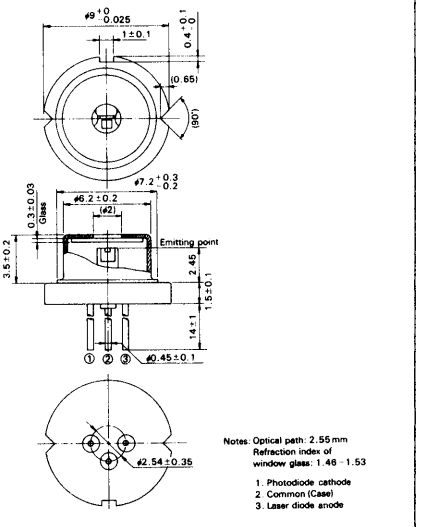
Hermetic sealing of the package achieves high reliability.

Features

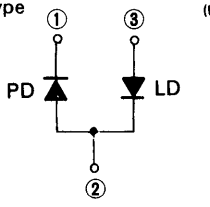
- Infrared light output: λ_p = 810–850 nm
- 40 mW (CW), 50 mW (pulse) operation at room temperature
- Built-in photodiode for monitoring laser output
- Single longitudinal mode



Package Dimensions



Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	40	mW
Pulse optical output power	$P_{O(pulse)}$	50*	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	30	V
Operating temperature	T_{opr}	−10 to +60	°C
Storage temperature	T_{stg}	−40 to +85	°C

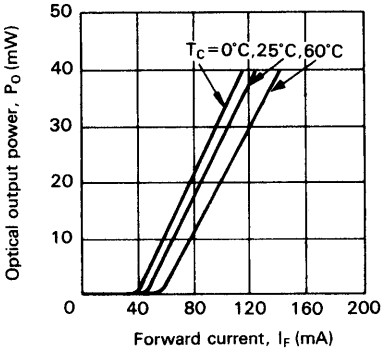
*PW ≦ 1 μs, duty 50%

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

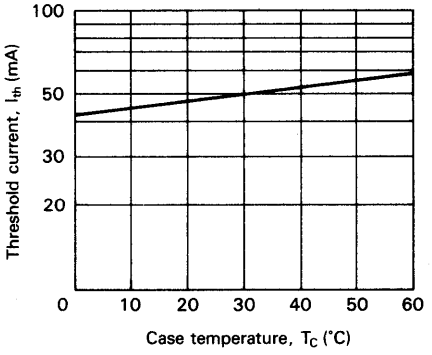
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		40	70	mA	
Optical output power	P_O	40			mW	Kink free
Slope efficiency	η	0.4	0.5	0.9	mW/mA	$\frac{24(mW)}{I\,(32\,mW) - I\,(8\,mW)}$
Lasing wavelength	λ_p	810	830	850	nm	P_O = 40 mW
Beam divergence parallel to the junction	$\theta_{//}$	8	11	14	deg.	P_O = 40 mW
Beam divergence perpendicular to the junction	$\theta_{\perp}$	18	25	32	deg.	P_O = 40 mW
Monitor current	I_S	40	100	240	μA	$V_{R(PD)}$ = 5 V, P_O = 4mW

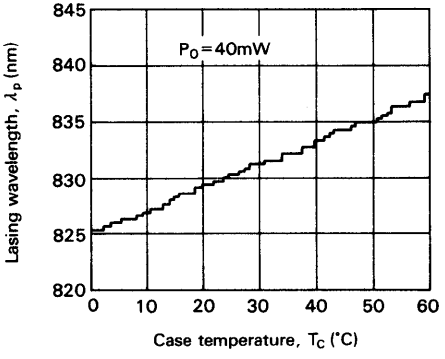
Optical Output Power vs. Forward Current



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



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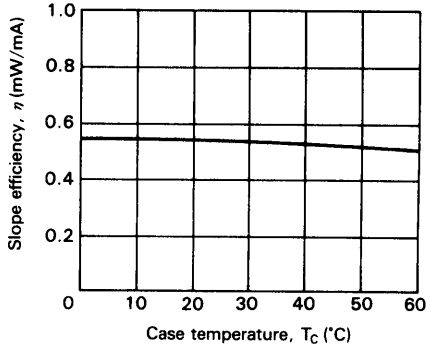
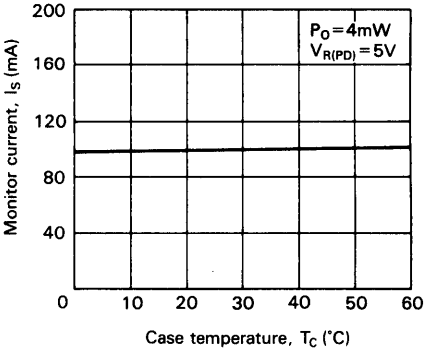
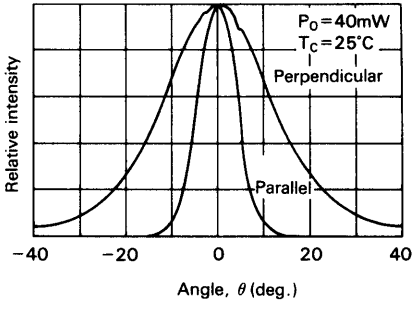
Temperature Dependence of Slope Efficiency



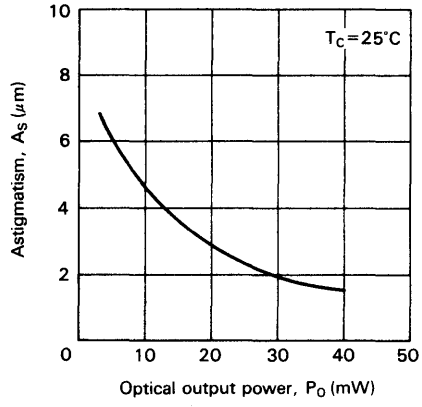
Monitor Current vs. Case Temperature



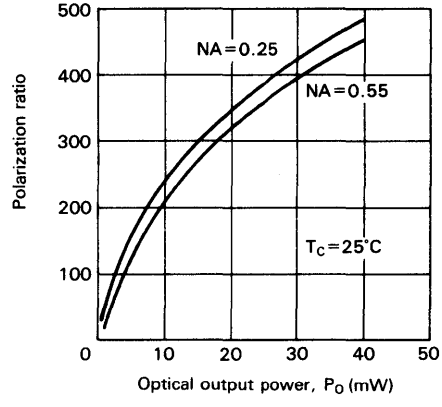
Far Field Pattern



Optical Output Power Dependence of Astigmatism



Optical Output Power Dependence of Polarization Ratio



6

HL1221A

Laser Diode

Description

HL1221A is a 1.2 μm InGaAsP laser diode with double heterojunction structure.

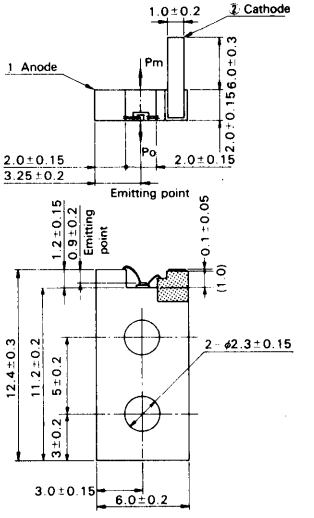
It is suitable as a light source in fiberoptic communications and various other types of optical equipment.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1170–1230 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns

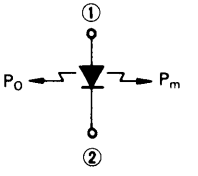
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

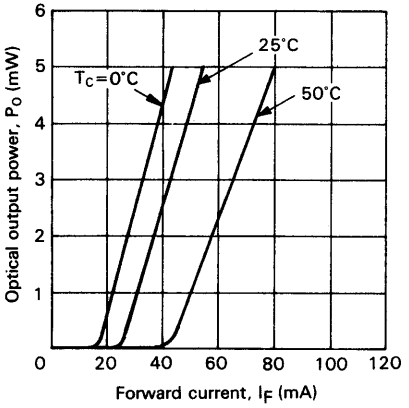
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	0 to +60	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

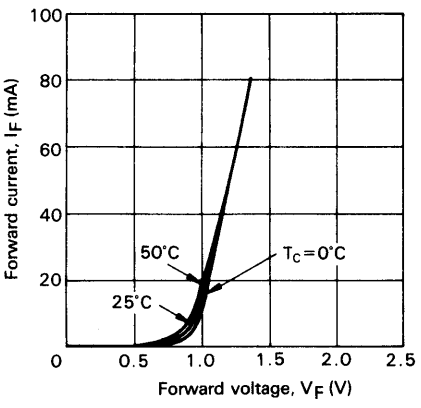
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F - I_{th} + 20$ mA
Monitor power	P_m	1			mW	$I_F - I_{th} + 20$ mA
Lasing wavelength	λ_p	1170	1200	1230	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

Optical Output Power vs. Forward Current

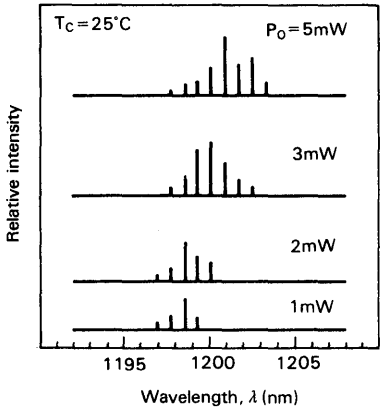


Forward Current vs. Forward Voltage

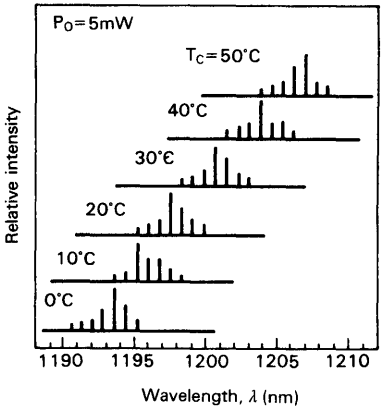


6

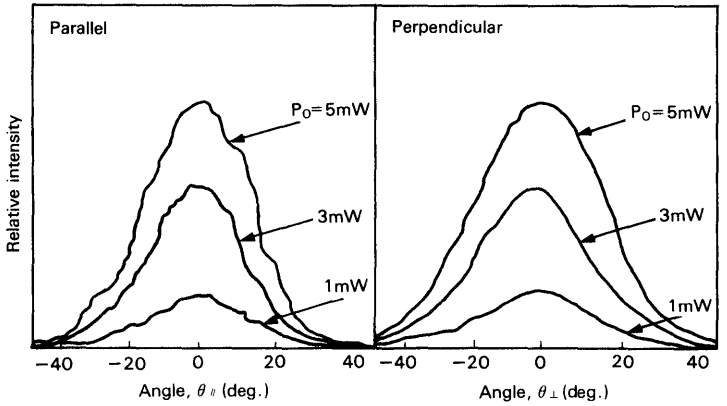
Lasing Spectrum



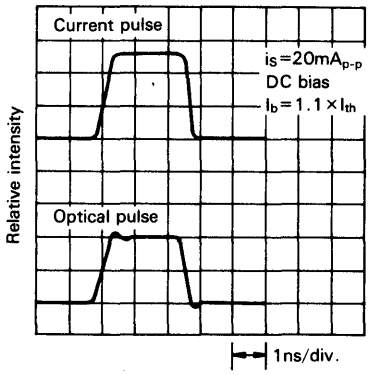
Temperature Dependence of Lasing Spectrum



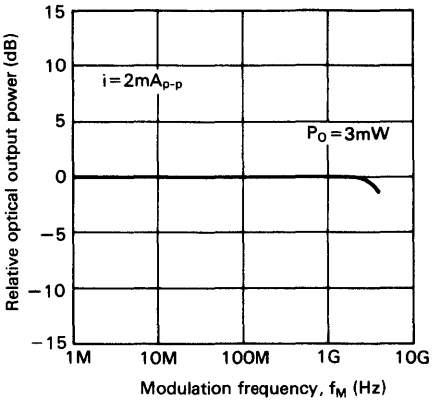
Far Field Pattern



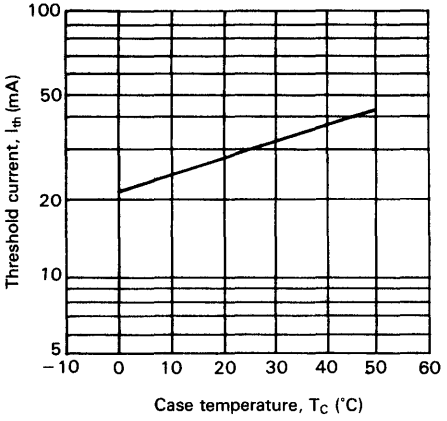
Pulse Response



Frequency Response



Threshold Current vs. Case Temperature



6

HL1221AC

Laser Diode

Description

HL1221AC is a 1.2 μm InGaAsP laser diode with double heterojunction structure.

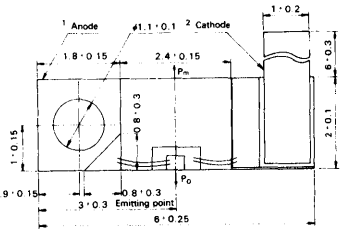
It is suitable as a light source in fiberoptic communications and various other types of optical equipment.

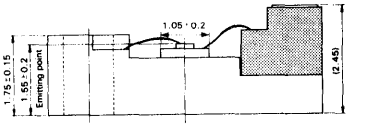
The package is compact to facilitate module assembly.

Features

- Long wavelength light output:
  λ_p = 1170–1230 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns

Package Dimensions

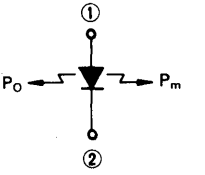




(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

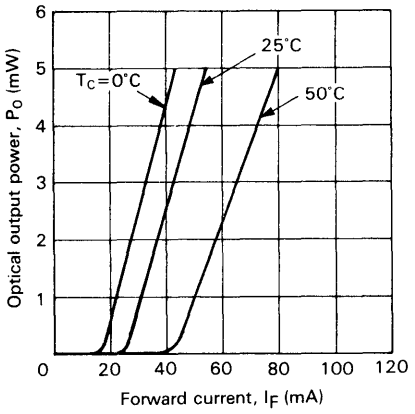
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	0 to +60	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

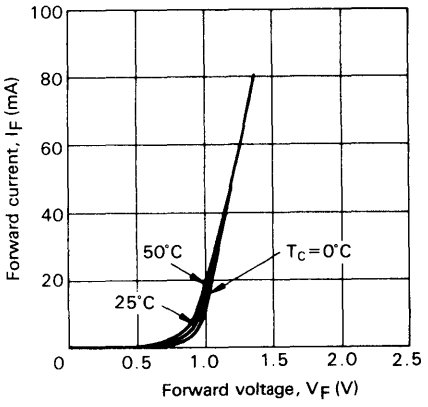
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F - I_{th}$ + 20 mA
Monitor power	P_m	1			mW	$I_F - I_{th}$ + 20 mA
Lasing wavelength	λ_p	1170	1200	1230	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

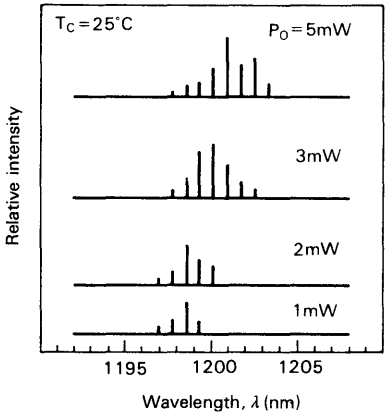
Optical Output Power vs. Forward Current



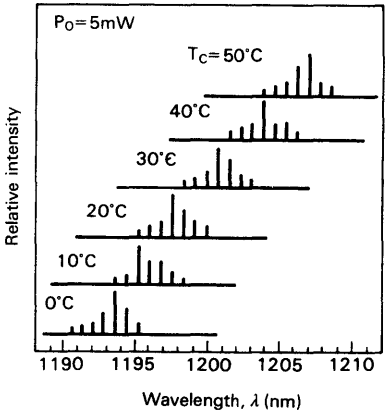
Forward Current vs. Forward Voltage



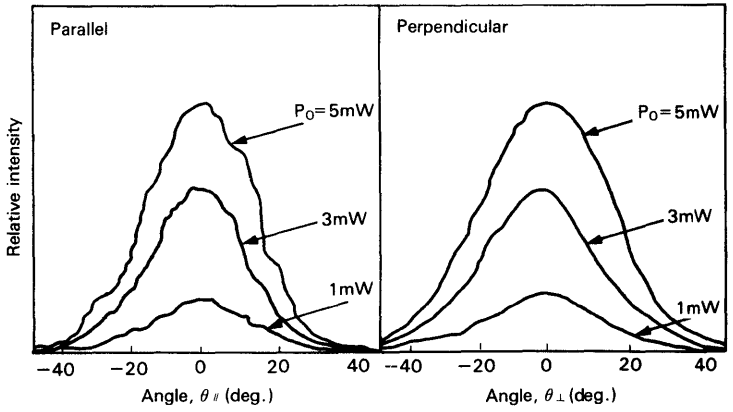
Lasing Spectrum



Temperature Dependence of Lasing Spectrum

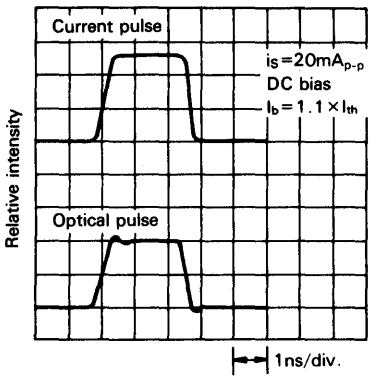


Far Field Pattern

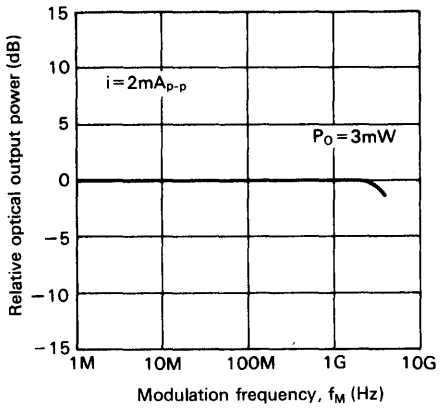


6

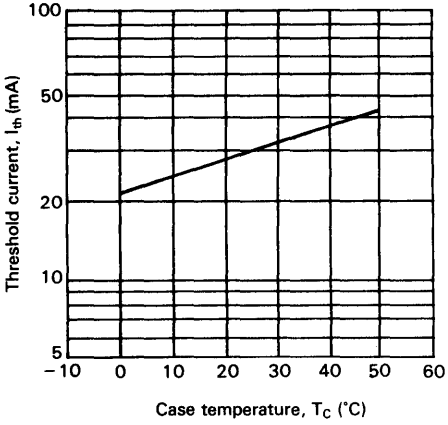
Pulse Response



Frequency Response



Threshold Current vs. Case Temperature



HLP5400

Laser Diode

Description

HLP5400 is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

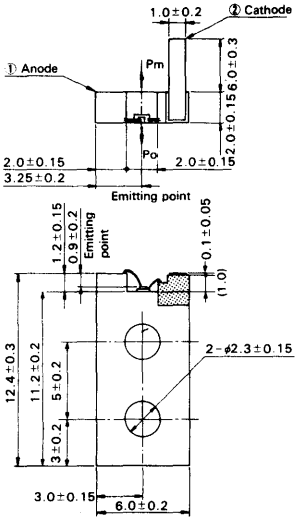
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1270–1330 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns

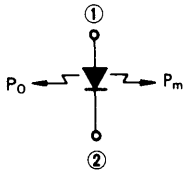
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	0 to +60	°C

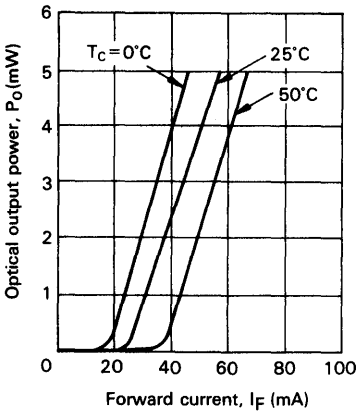
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

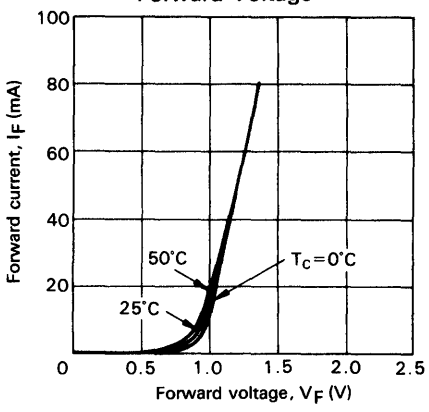
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	80	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1270	1300	1330	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

6

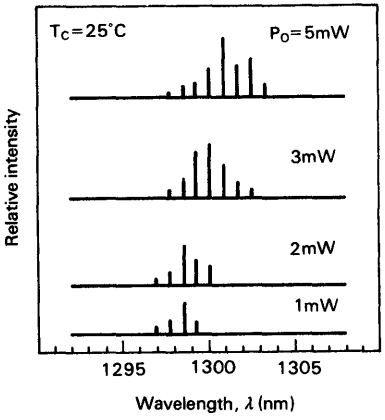
Optical Output Power vs. Forward Current



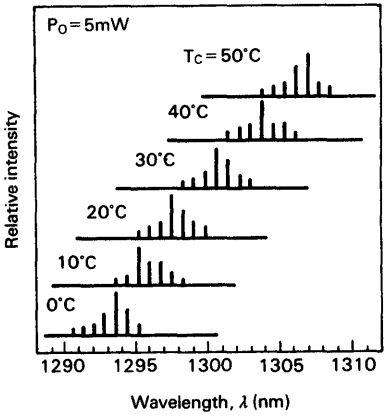
Forward Current vs. Forward Voltage



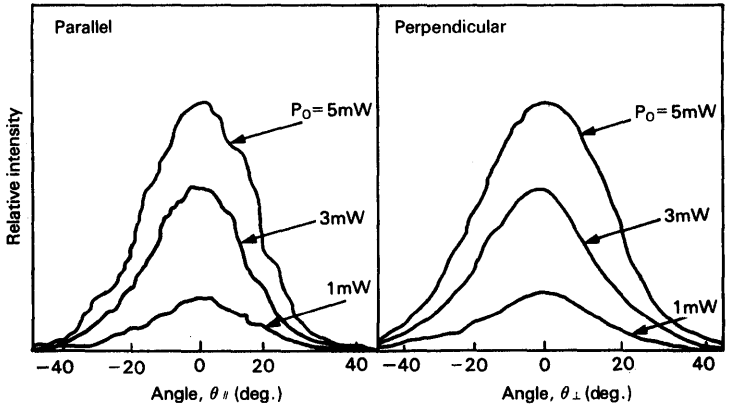
Lasing Spectrum



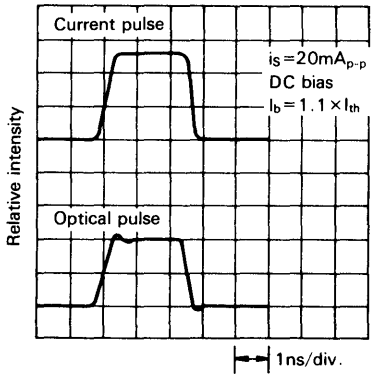
Temperature Dependence of Lasing Spectrum



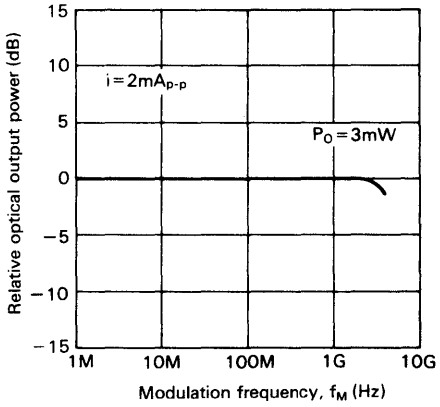
Far Field Pattern



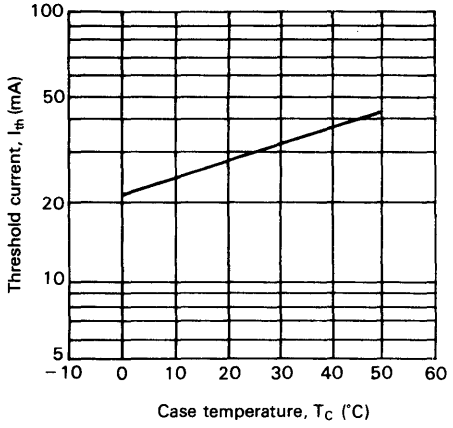
Pulse Response



Frequency Response



Threshold Current vs. Case Temperature



6

HL1321AC

Laser Diode

Description

HL1321AC is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

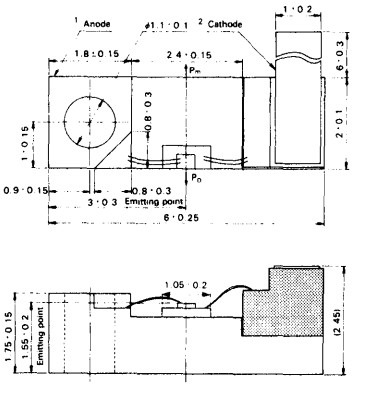
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is compact to facilitate module assembly.

Features

- Long wavelength light output: $\lambda_p = 1270-1330$ nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

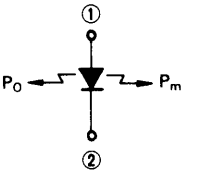
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

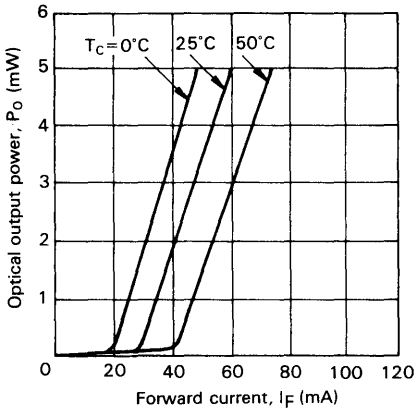
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

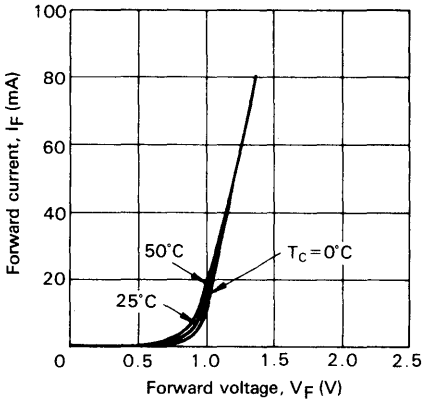
Optical and Electrical Characteristics ($T_C = 25°C$)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1270	1300	1330	nm	$P_O = 3$ mW
Spectral width	$\Delta\lambda$		2		nm	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

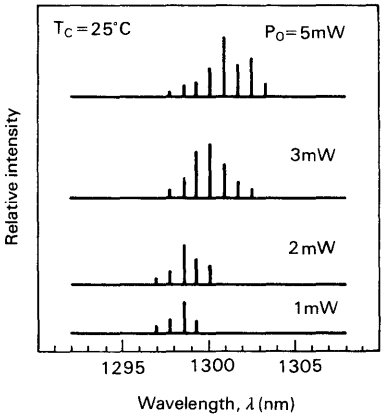
Optical Output Power vs. Forward Current



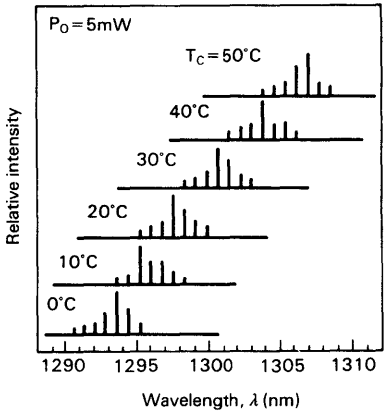
Forward Current vs. Forward Voltage



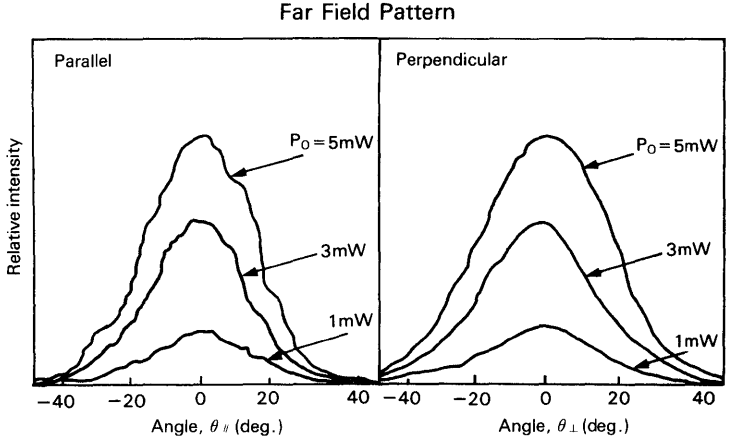
Lasing Spectrum



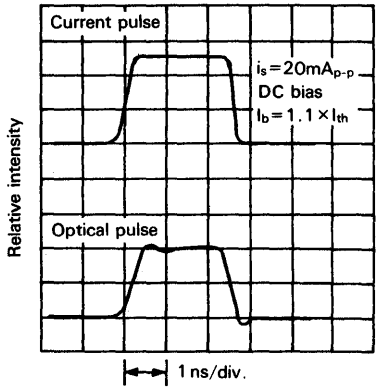
Temperature Dependence of Lasing Spectrum



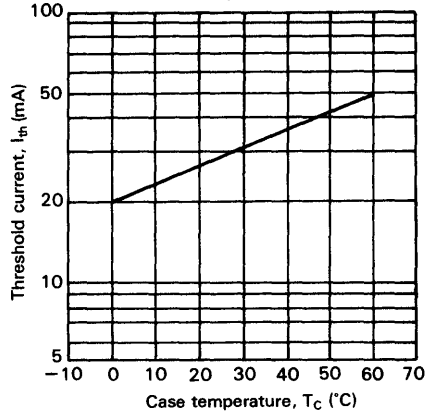
Far Field Pattern



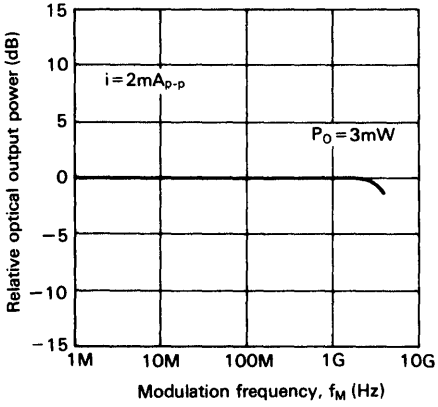
Pulse Response



Threshold Current vs. Case Temperature



Frequency Response



HL1321FG

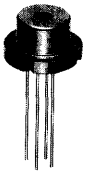
Laser Diode

Description

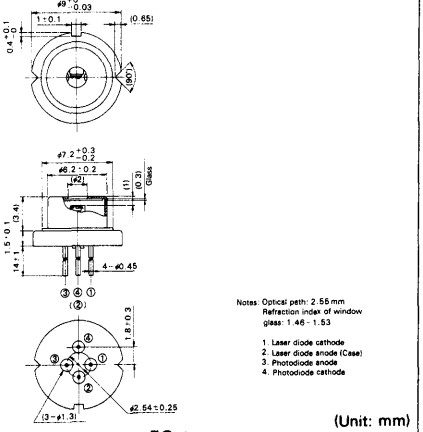
HL1321FG is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The laser beam is output through the glass window in the package cap. Monitoring current is output from a built-in photodiode.



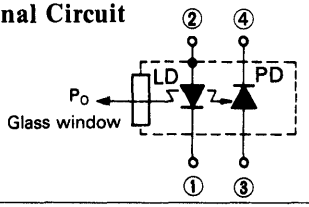
Package Dimensions



FG-type

(Unit: mm)

Internal Circuit



Features

- Long wavelength light output: $\lambda_p = 1290-1330$ nm
- 5 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

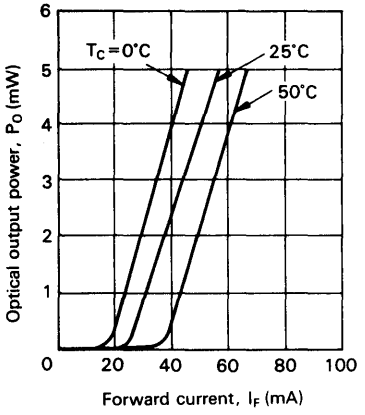
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_C = 25°C$)

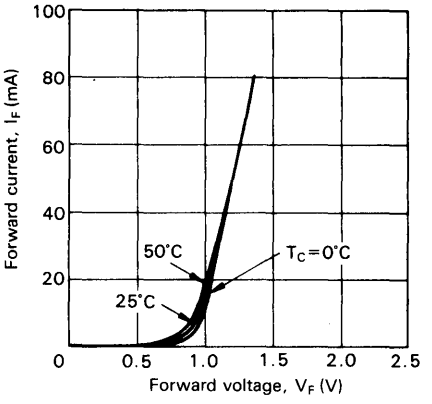
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	$P_O = 3$ mW
Spectral width	$\Delta\lambda$		2		nm	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)} = 5$ V
Monitor current	I_S	100			μA	$V_{R(PD)} = 5$ V, $P_O = 3$ mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)} = 5$ V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r			0.5	ns	$P_O = 3$ mW, $I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f			0.5	ns	$P_O = 3$ mW, $I_{bias} = I_{th}$, 90 to 10%

6

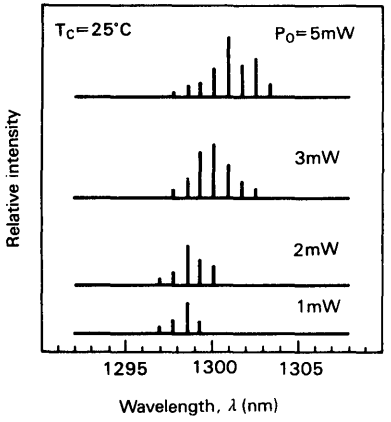
Optical Output Power vs. Forward Current



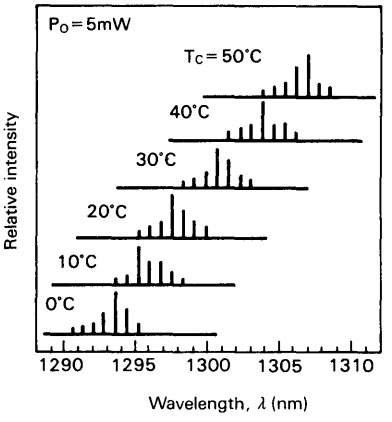
Forward Current vs. Forward Voltage



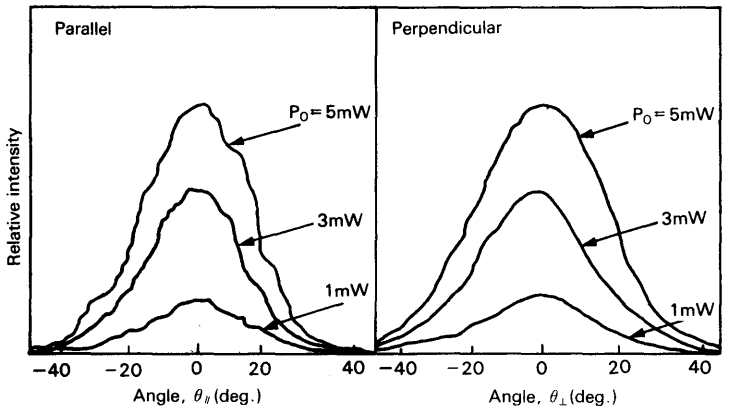
Lasing Spectrum



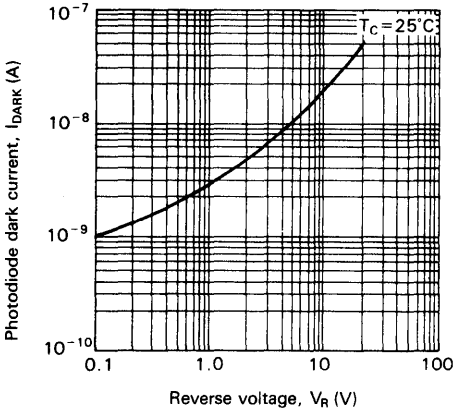
Temperature Dependence of Lasing Spectrum



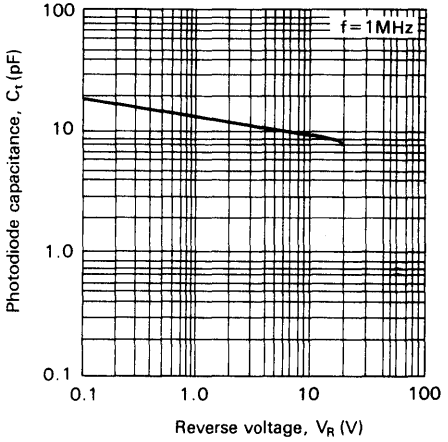
Far Field Pattern



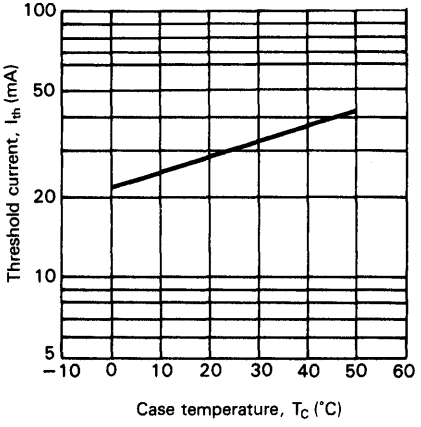
Photodiode Dark Current vs. Reverse Voltage



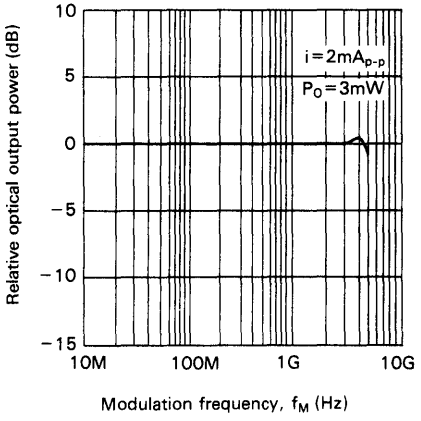
Photodiode Capacitance vs. Reverse Voltage



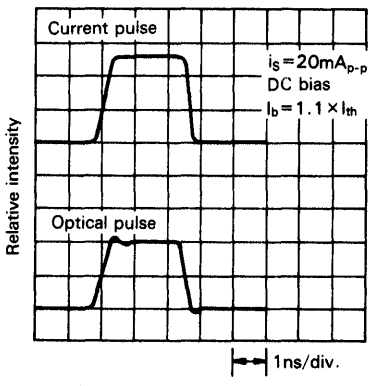
Threshold Current vs. Case Temperature



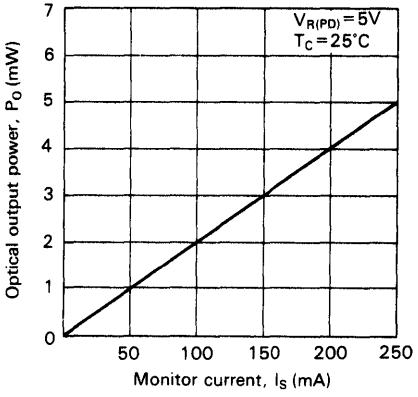
Frequency Response of Laser Diode



Pulse Response of Laser Diode



Optical Cutput Power vs. Monitor Current



6

HL1321BF

Laser Diode

Description

HL1321BF is a laser-diode module in a 14-pin butterfly-type package with a built-in thermoelectronic controller and connected single mode fiber.

It is suitable as a light source in high-speed modulated, high-bit-rate, long-distance fiberoptic communications equipment.

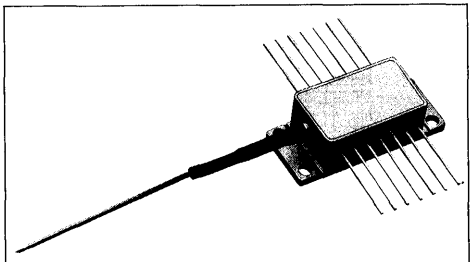
The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

−Fiber specifications−

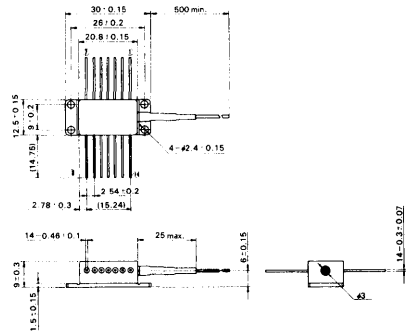
Mode field diameter	: 10.0 ±1.0 μm
λ_c	: 1.10−1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

Features

- Long wavelength light output: λ_p = 1290−1330 nm
- 1.2 mW CW and pulse operation at room temperature
- High-speed modulation (1.8 Gb/s)
- Stabilized operation with built-in thermoelectronic controller



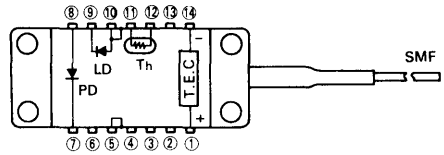
Package Dimensions



(Unit: mm)

BF-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode	⑧ PD anode
② N. C.	⑨ LD cathode
③ N. C.	⑩ LD anode (case)
④ N. C.	⑪ Thermistor
⑤ Case	⑫ Thermistor
⑥ N. C.	⑬ N. C.
⑦ PD cathode	⑭ T. E. C. cathode

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

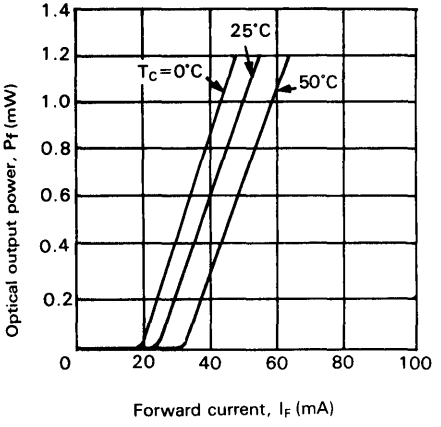
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

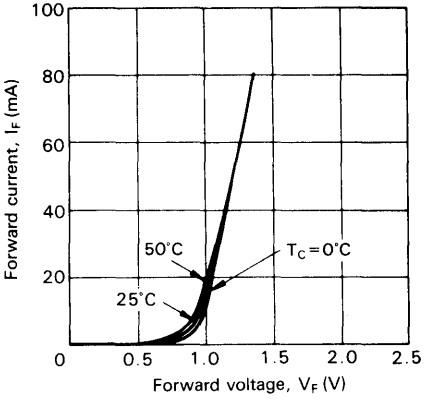
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.6			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_f = 1.0 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 1.0 mW
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	300			μA	$V_{R(PD)}$ = 5 V, P_f = 1.0 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	P_f = 1.0 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

6

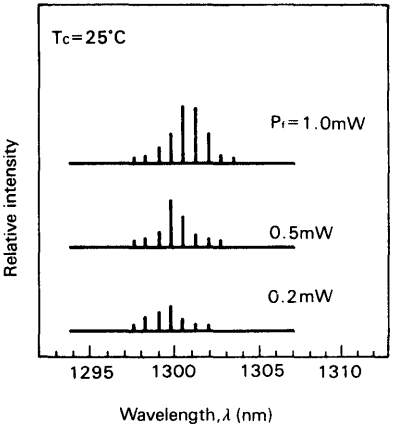
Optical Output Power vs. Forward Current



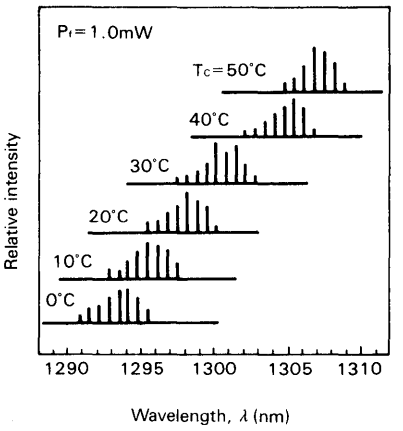
Forward Current vs. Forward Voltage



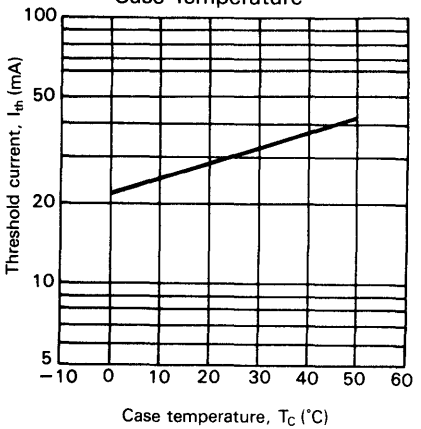
Lasing Spectrum



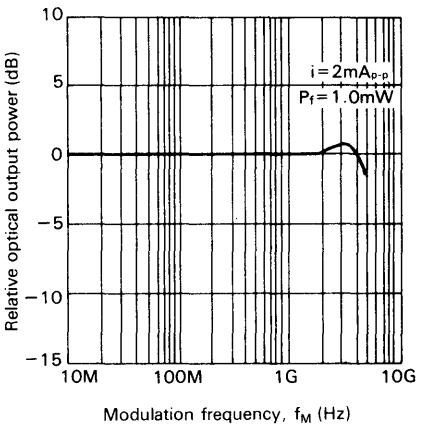
Temperature Dependence of Lasing Spectrum



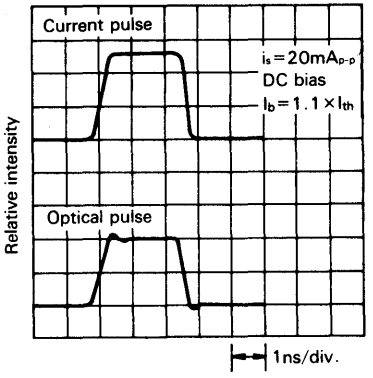
Threshold Current vs. Case Temperature



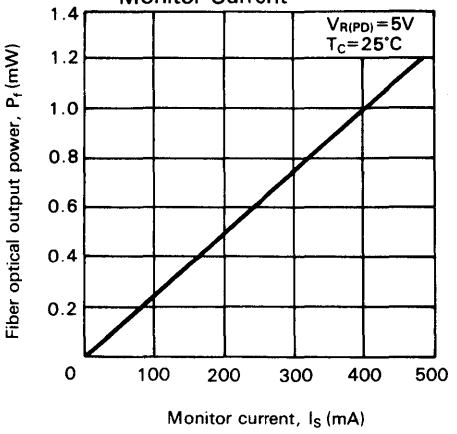
Frequency Response of Laser Diode



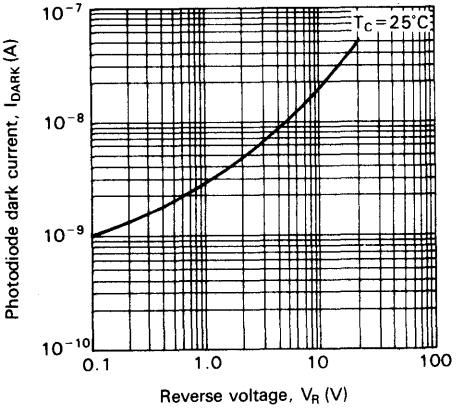
Pulse Response of Laser Diode



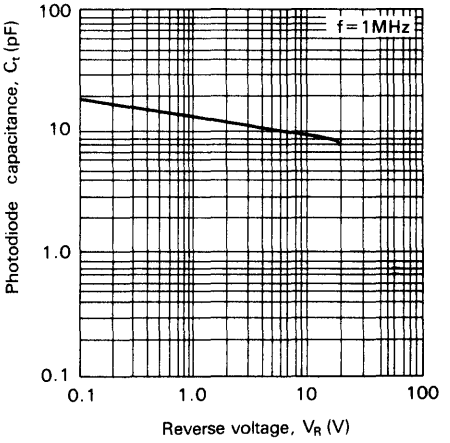
Optical Output Power vs. Monitor Current



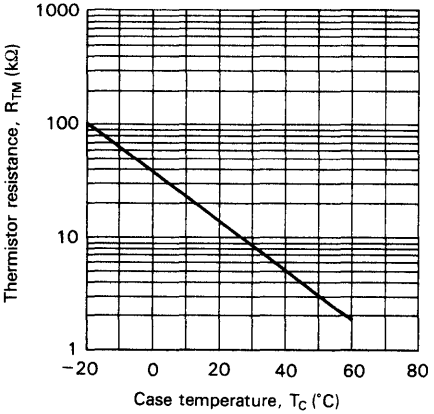
Photodiode Dark Current vs. Reverse Voltage



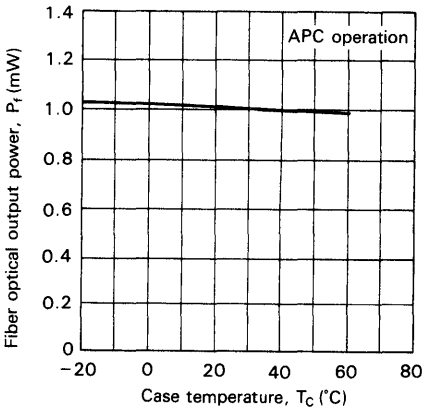
Photodiode Capacitance vs. Reverse Voltage



Thermistor Resistance vs. Case Temperature



Tracking Characteristics



6

HL1321DL

Laser Diode

Description

HL1321DL is a laser-diode module in a 14-pin dual-in-line type package with a built-in thermoelectronic controller and connected single-mode fiber.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

−Fiber specifications−

Mode field diameter	: 10.0 ±1.0 μm
λ_c	: 1.10−1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

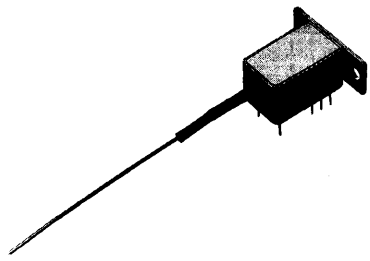
Features

- Long wavelength light output: λ_p = 1290−1330 nm
- 1.2 mW CW and pulse operation at room temperature
- High-speed modulation (800 Mb/s)
- Stabilized operation with built-in thermoelectronic controller

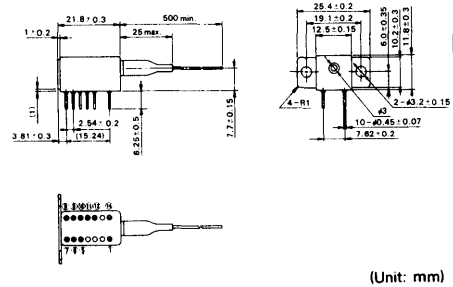
Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



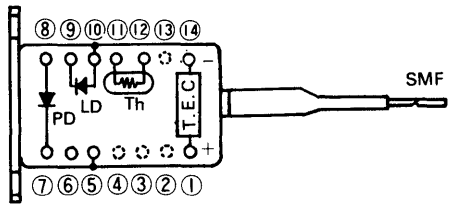
Package Dimensions



(Unit: mm)

DL-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

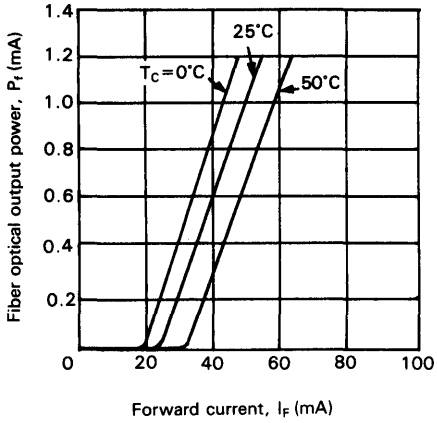
①	T. E. C. anode	⑧	PD anode
②	—	⑨	LD cathode
③	—	⑩	LD anode (case)
④	—	⑪	Thermistor
⑤	Case	⑫	Thermistor
⑥	N. C.	⑬	—
⑦	PD cathode	⑭	T. E. C. cathode

Optical and Electrical Characteristics (T_C = 25°C)

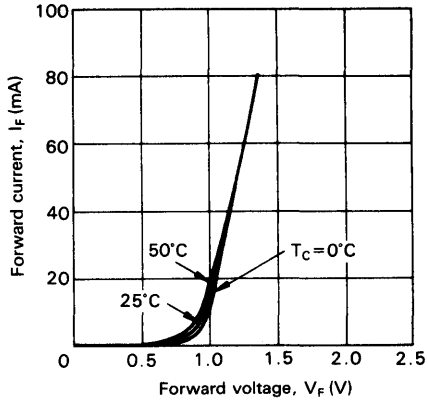
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.6			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_f = 1.0 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 1.0 mW
Rise time	t_r			0.5	ns	P_f = 1.0 mW, $I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f			0.5	ns	P_f = 1.0 mW, $I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	300			μA	$V_{R(PD)}$ = 5 V, P_f = 1.0 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	P_f = 1.0 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

6

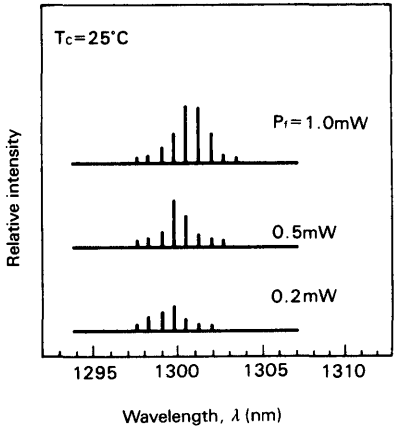
Optical Output Power vs. Forward Current



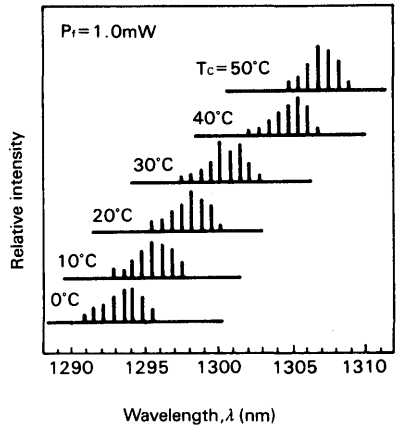
Forward Current vs. Forward Voltage



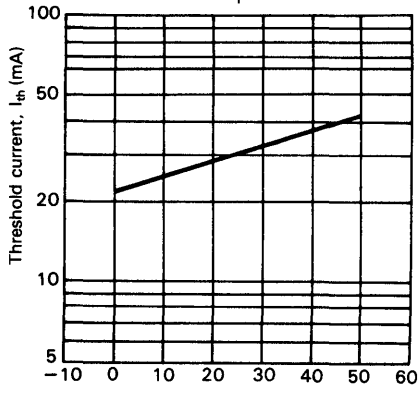
Lasing Spectrum



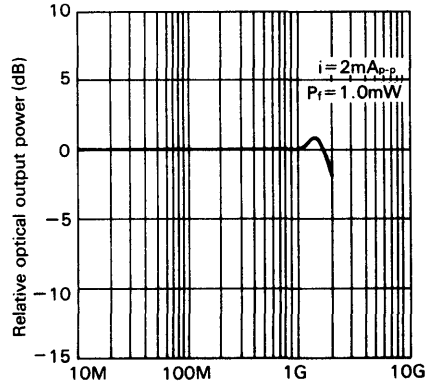
Temperature Dependence of Lasing Spectrum



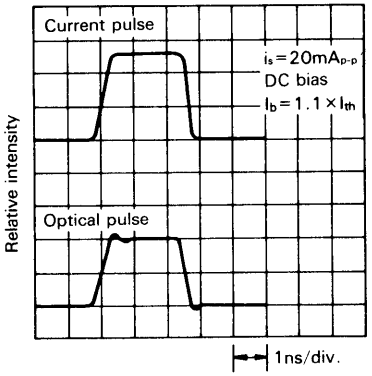
Threshold Current vs. Case Temperature



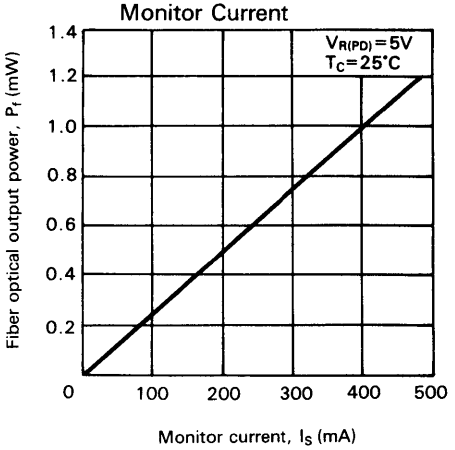
Frequency Response of Laser Diode



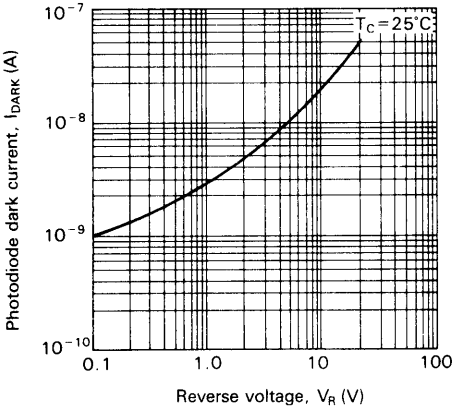
Pulse Response of Laser Diode



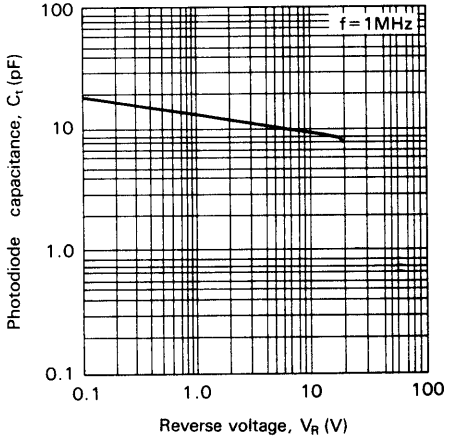
Optical Output Power vs. Monitor Current



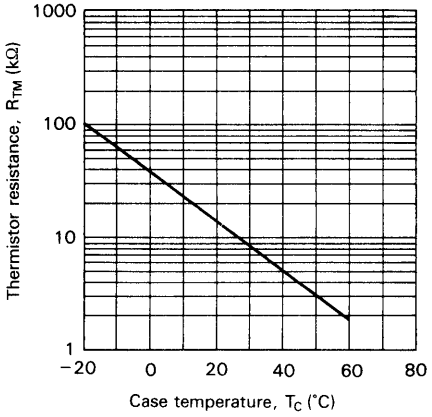
Photodiode Dark Current vs. Reverse Voltage



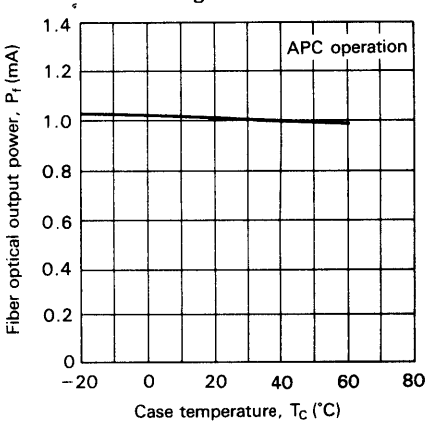
Photodiode Capacitance vs. Reverse Voltage



Thermistor Resistance vs. Case Temperature



Tracking Characteristics



6

HL1322A

Laser Diode

Description

HL1322A is a high-power 1.3 μm InGaAsP laser diode with double heterojunction structure.

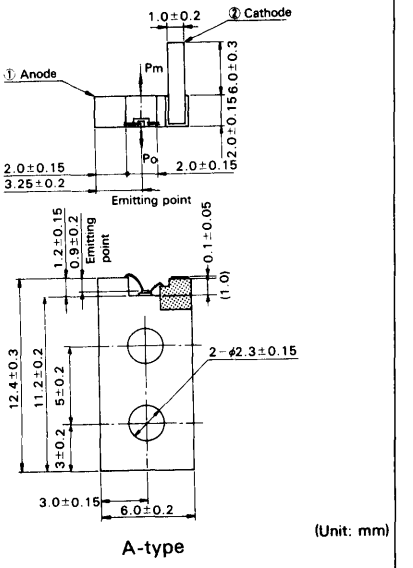
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment. The HL1322A emits higher optical power than HLP5400 and HL1321AC.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1290–1330 nm
- 10 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns

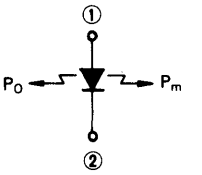
Package Dimensions



A-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

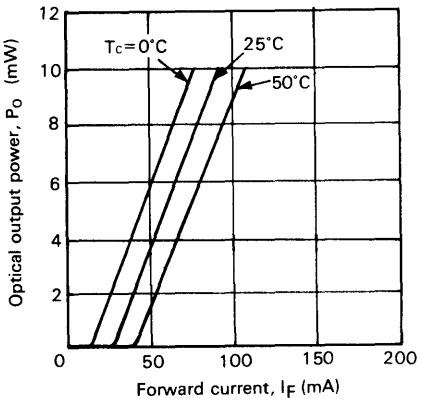
Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

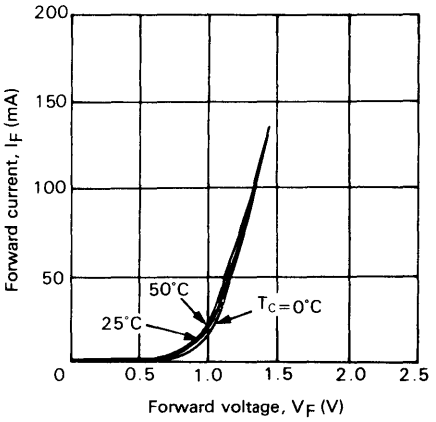
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	10			mW	Kink free
		4			mW	$I_F - I_{th}$ + 40 mA
Monitor power	P_m	2			mW	$I_F - I_{th}$ + 40 mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 6 mW
Spectral width	$\Delta\lambda$			5	nm	P_O = 6 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 6 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 6 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

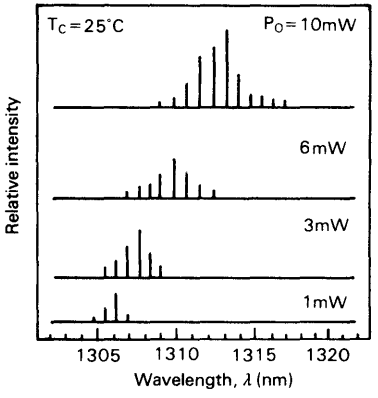
Optical Output Power vs. Forward Current



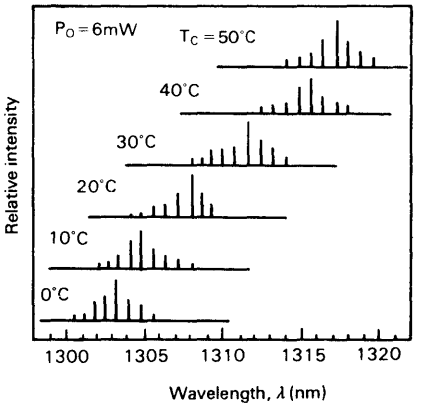
Forward Current vs. Forward Voltage



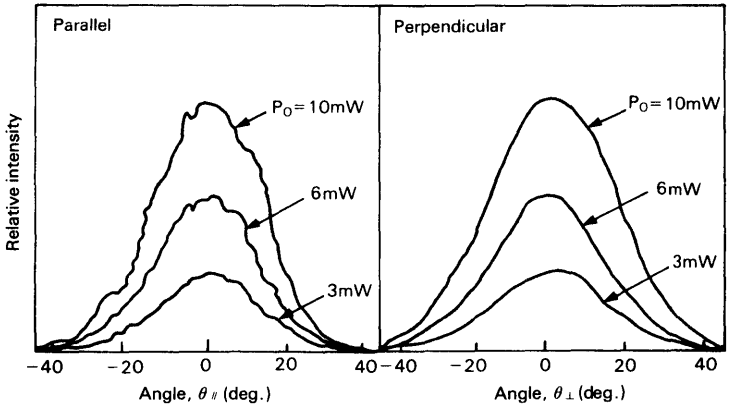
Lasing Spectrum



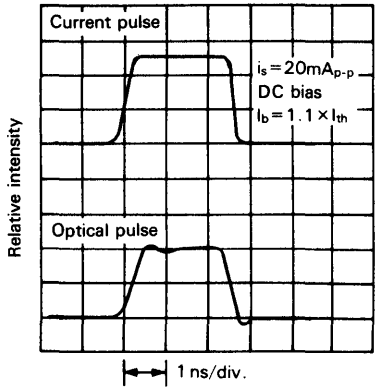
Temperature Dependence of Lasing Spectrum



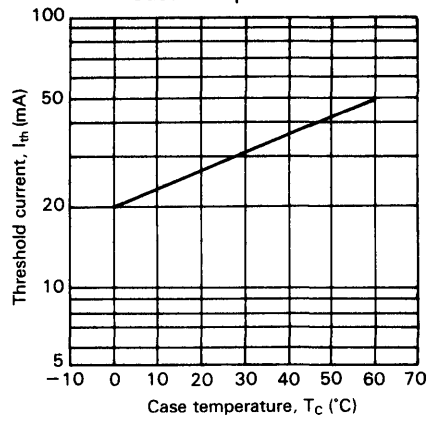
Far Field Pattern



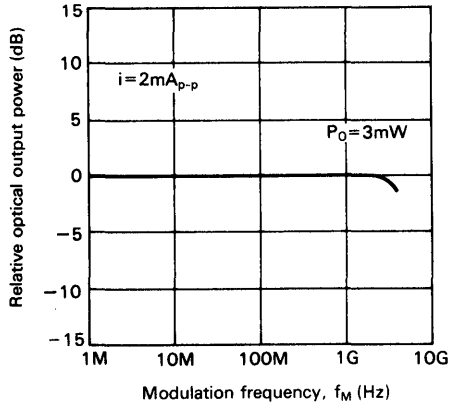
Pulse Response



Threshold Current vs. Case Temperature



Frequency Response of Laser Diode



HL1322AC

Laser Diode

Description

HL1322AC is a high-power 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

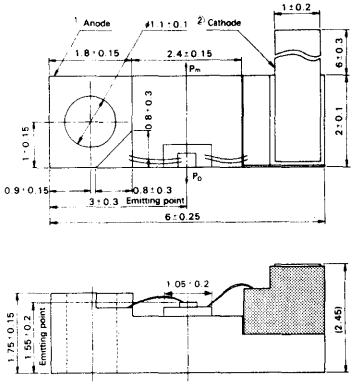
The HL1322AC emits higher optical power than HLP5400 and HL1321AC.

The package is compact to facilitate module assembly.

Features

- Long wavelength light output: λ_p = 1290–1330 nm
- 10 mW CW operation at room temperature
- Fast pulse response: t_r, t_f ≦ 0.5 ns

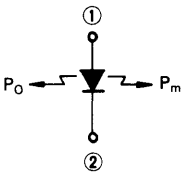
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

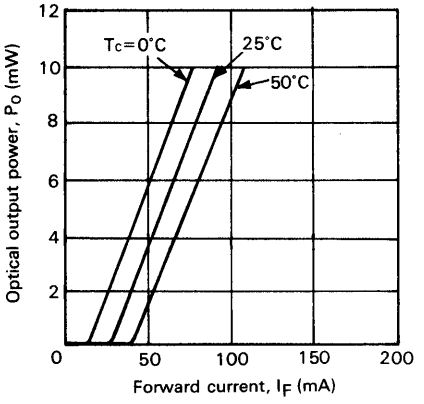
Items	Symbols	Values	Units
Optical output power	P_O	10	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

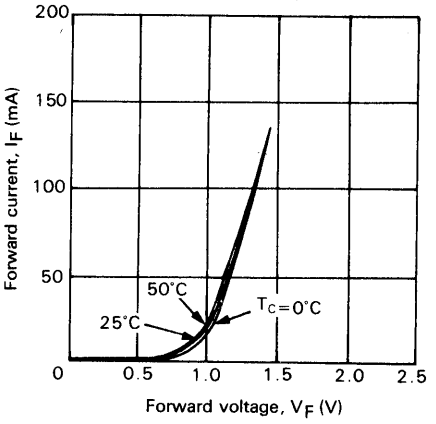
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	10			mW	Kink free
		4			mW	$I_F = I_{th} + 40$ mA
Monitor power	P_m	2			mW	$I_F = I_{th} + 40$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 6 mW
Spectral width	$\Delta\lambda$			5	nm	P_O = 6 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 6 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 6 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

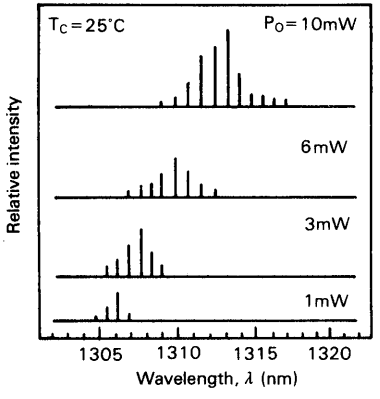
Optical Output Power vs. Forward Current



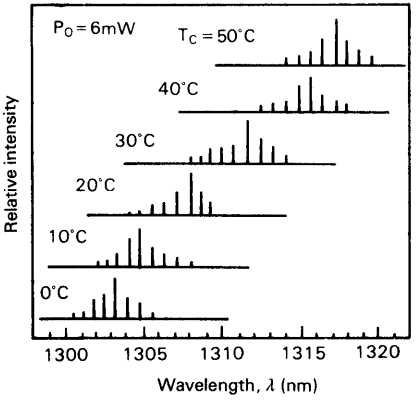
Forward Current vs. Forward Voltage



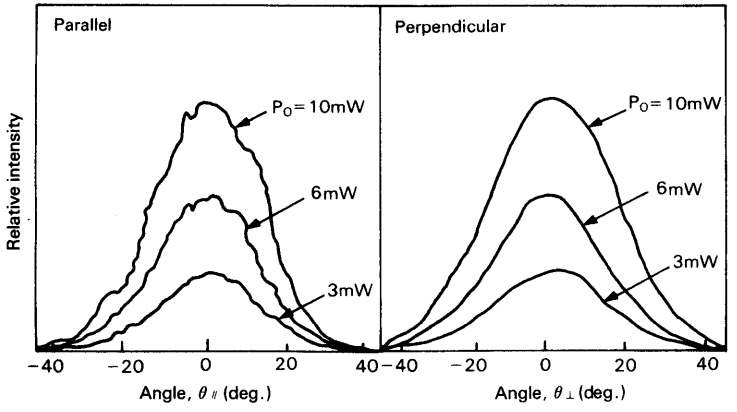
Lasing Spectrum



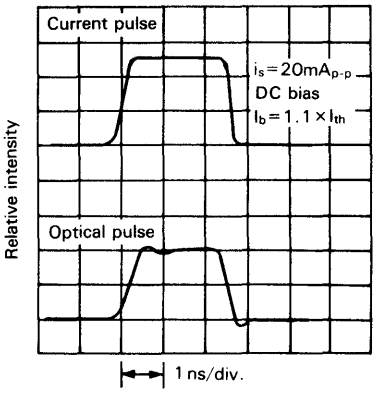
Temperature Dependence of Lasing Spectrum



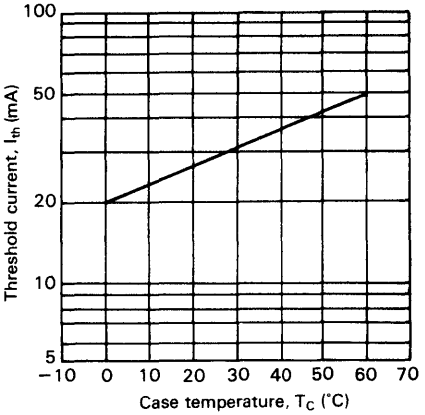
Far Field Pattern



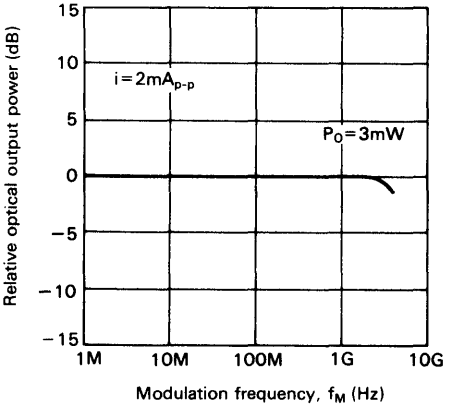
Pulse Response



Threshold Current vs. Case Temperature



Frequency Response of Laser Diode



6

HL1323DM

Laser Diode

Description

HL1323DM is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in short- to intermediate-distance fiberoptic communications systems, e.g. LAN, CATV and LJN.

The laser beam comes out from the connected single-mode fiber; monitoring current by a built-in photodiode.

—Fiber specifications—

Mode field diameter	: 10.0 ± 1.0 μm
Cutoff wavelength	: 1.10–1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

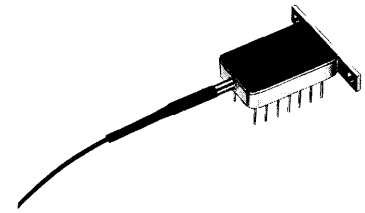
Features

- Long wavelength light output: λ_p = 1260–1340 nm
- 0.3 mW CW and pulse operation at room temperature
- Fast pulse response: t_r, $t_f \leq 0.5$ ns
- Built-in photodiode for monitoring laser output
- Package with thinner-height

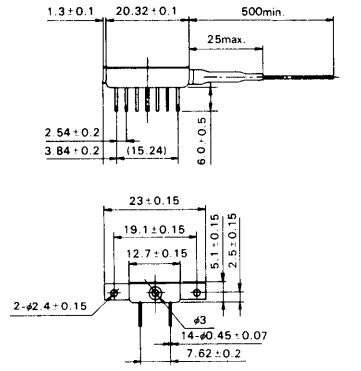
Absolute Maximum Ratings (T_c=25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	0.3	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−20 to +70	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

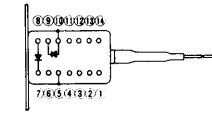


Package Dimensions



DM-type (Unit: mm)

Pin Connection (Bottom view)

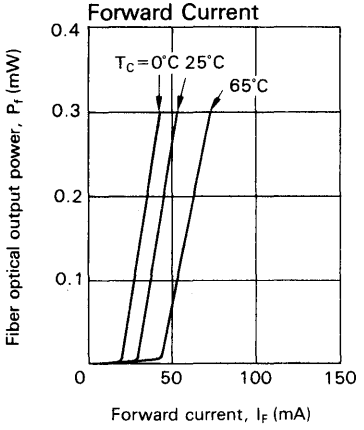


1	N.C.	8	PD Anode
2	N.C.	9	LD Cathode
3	N.C.	10	LD Anode (Case)
4	N.C.	11	N.C.
5	Case	12	N.C.
6	N.C.	13	N.C.
7	PD Cathode	14	N.C.

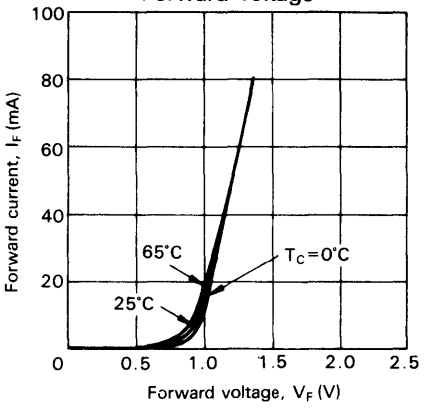
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	0.3			mW	Kink free
		0.14			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1260	1300	1340	nm	P_f = 0.15 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 0.3 mW
Rise time	t_r			0.5	ns	P_f = 0.15 mW, $I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f			0.5	ns	P_f = 0.15 mW, $I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	100			μA	$V_{R(PD)}$ = 5 V, P_f = 0.15 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz

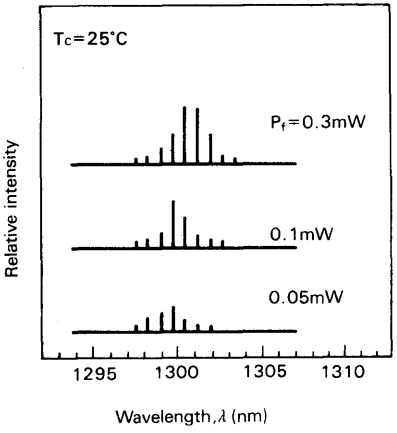
Optical Output Power vs. Forward Current



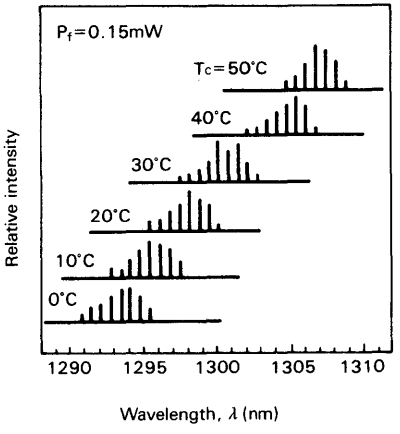
Forward Current vs. Forward Voltage



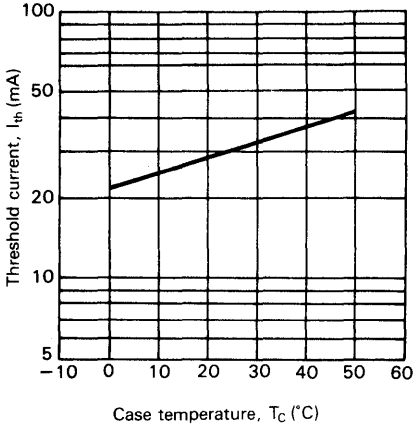
Lasing Spectrum



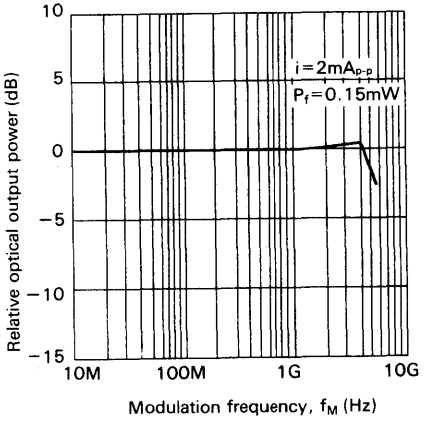
Temperature Dependence of Lasing Spectrum



Threshold Current vs. Case Temperature

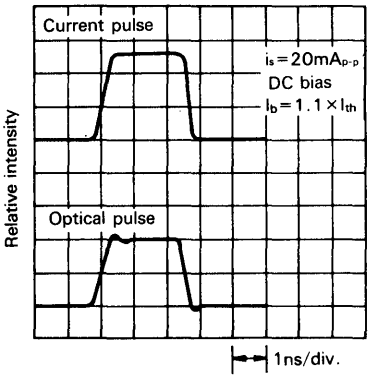


Frequency Response of Laser Diode

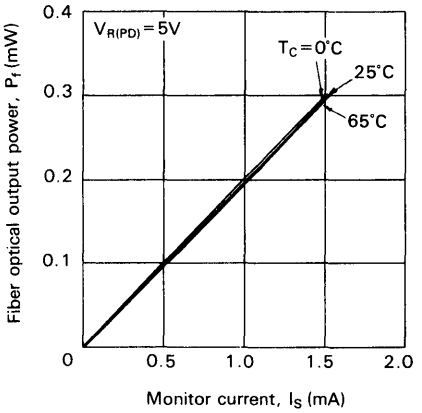


6

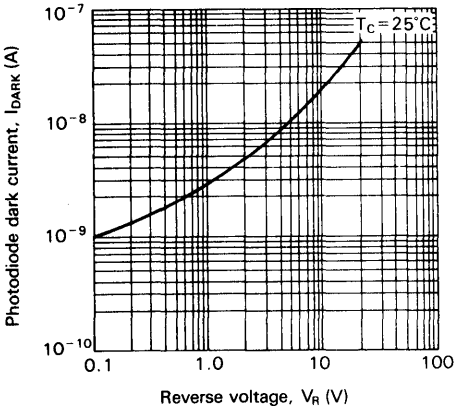
Pulse Response of Laser Diode



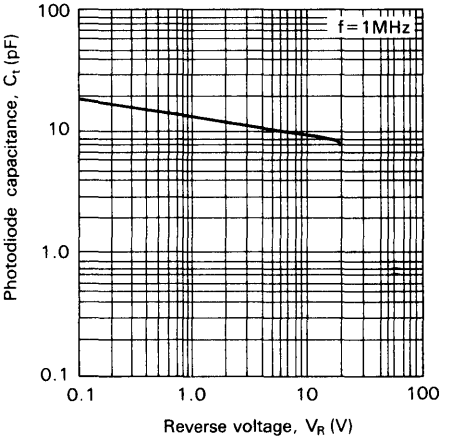
Optical Output Power vs. Monitor Current



Photodiode Dark Current vs. Reverse Voltage



Photodiode Capacitance vs. Reverse Voltage



HL1323TR

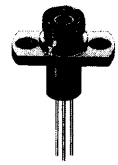
Laser Diode

Description

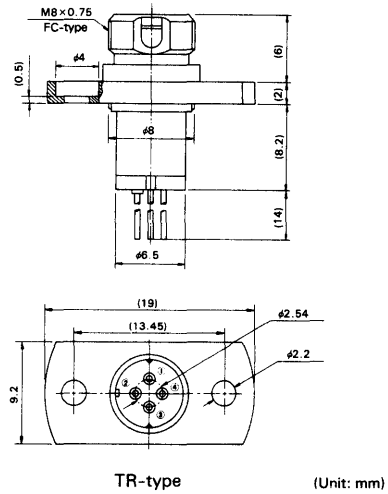
HL1323TR is a 1.3 μm InGaAsP laser diode with double heterojunction structure.

It is suitable as a light source in short- to intermediate-distance fiberoptic communications systems, e.g. LAN, CATV and LJN.

The package with receptacle is suited for easy connecting with FC-PC type connector.

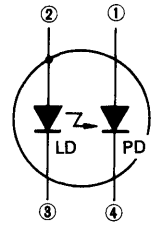


Package Dimensions



TR-type (Unit: mm)

Internal Circuit



① PD anode
② LD anode
③ LD cathode
④ PD cathode

Features

- Long wavelength light output:
  λ_p = 1290–1330 nm
- $P_f \geqq 1.0$ mW (connecting with multi-mode fiber)
  $P_f \geqq 0.3$ mW (connecting with single-mode fiber)
- High-speed modulation (BR $\leqq$ 1 Gb/s)
- Built-in photodiode for monitoring laser output
- Wide operating temperature range: T_{opr} = 0– +60°C

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	0.3*	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

* At SI10/125 FC-PC connector end

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

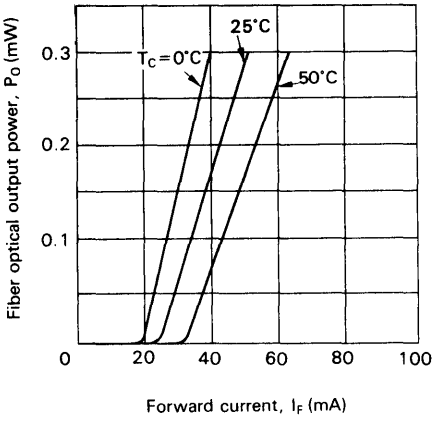
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	0.3*			mW	Kink free
		0.1*	0.2*		mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_f = 0.1 mW
Spectral width	$\Delta\lambda$		2		nm	P_f = 0.1 mW
Rise time	t_r			0.5	ns	P_f = 0.1 mW, $I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f			0.5	ns	P_f = 0.1 mW, $I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	50			μA	$V_{R(PD)}$ = 5 V, P_f = 0.1 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz

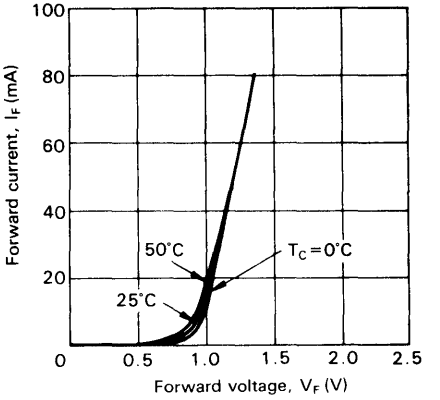
* At SI10/125 FC-PC connector end

6

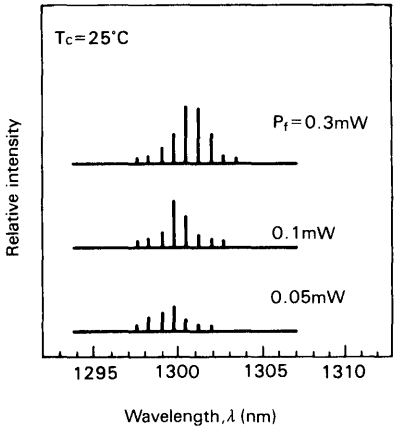
Optical Output Power vs. Forward Current



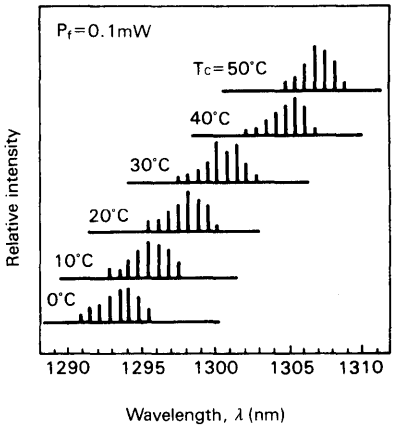
Forward Current vs. Forward Voltage



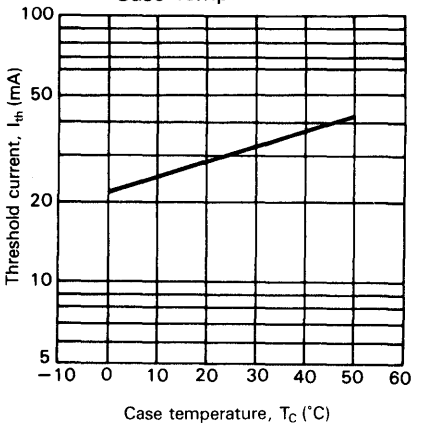
Lasing Spectrum



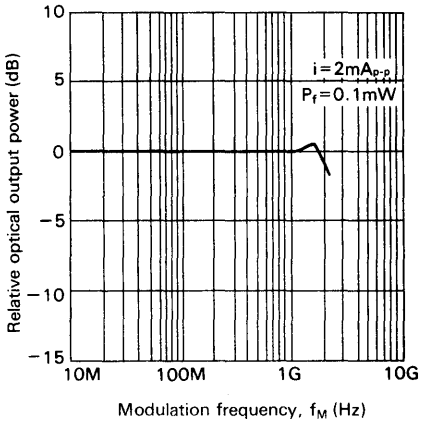
Temperature Dependence of Lasing Spectrum



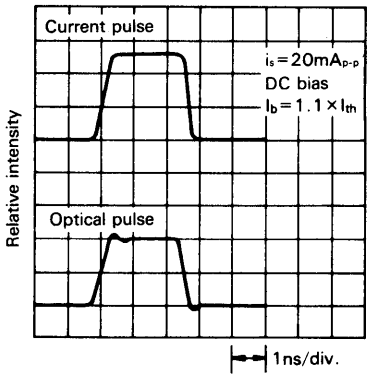
Threshold Current vs. Case Temperature



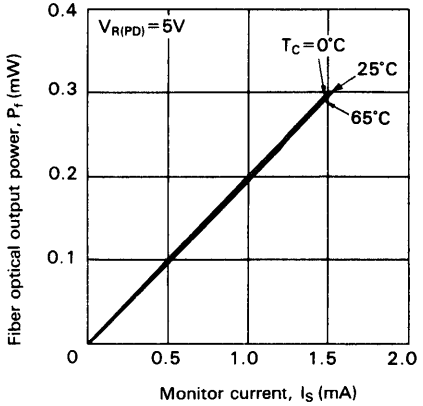
Frequency Response of Laser Diode



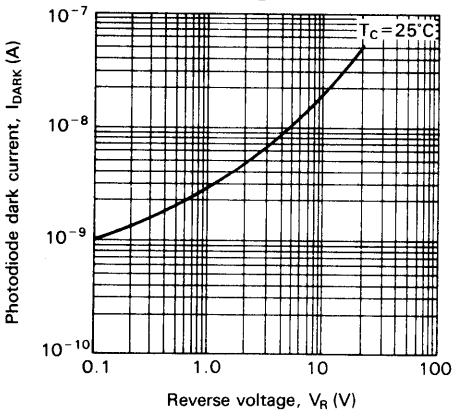
Pulse Response of Laser Diode



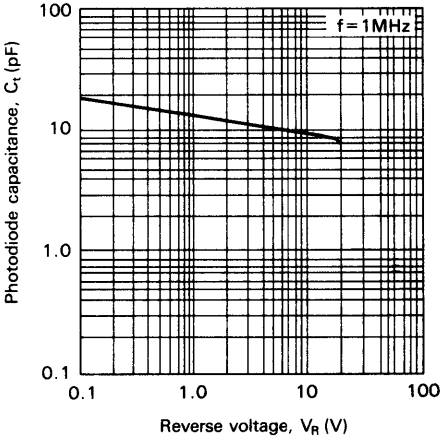
Optical Output Power vs. Monitor Current



Photodiode Dark Current vs. Reverse Voltage



Photodiode Capacitance vs. Reverse Voltage



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HL1324MF

Preliminary

1.3μm Wide Operating Temperature Range LD

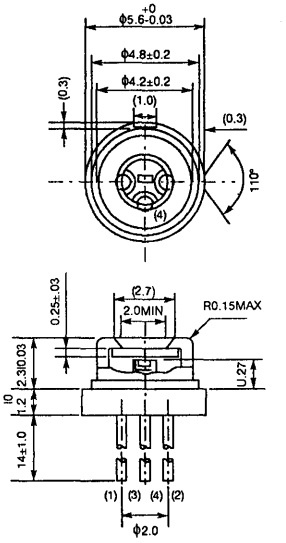
Applications

- Fiber Optic Communications (LAN, CATV, LJN)

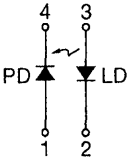
Features

- Wide operating temperature range and High power (Kink Free 5mW at T_c=85°C)
- High Speed Modulation
  B R ≤ 1.G b/s
- Built-in Photodiode for Monitoring
- High Reliability

Package Dimensions



Internal Circuit



Absolute Maximum Ratings (T_c=25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5.0	mW
LD Reverse voltage	$V_{R(LD)}$	2.0	V
PD Reverse voltage	$V_{R(PD)}$	15	V
PD Forward Current	$I_{F(PD)}$	1.0	mA
Operating temperature	T_{opr}	−20 ~ +85	°C
Storage temperature	T_{stg}	−40 ~ +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_c=25°C)

Items	Symbols	Test Conditions	min.	typ.	max.	Units
Threshold Current	I_{th}	—	—	15	35	mA
Optical Output Power	P_O	Kink Free	5	—	—	mW
	P_O	$I_F = I_{th}$ + 20mA	4	—	—	mW
Lasing Wavelength	λ_p	P_o = 5mW	1280	1310	1340	nm
Spectral Width	$\triangle\lambda$	P_o = 5mW	—	5	—	nm
PD Dark Current	I_{DARK}	$V_{R(PD)}$ = 5V	—	—	350	nA
Monitor Current	I_s	$V_{R(PD)}$ = 5V, P_o = 5mW	100	—	—	μA
PD Capacitance	C_t	$V_{R(PD)}$ = 5V, f = 1MHz	—	15	20	pF
Rise Time	tr	$I_{bias} = I_{th}$, 10 ~ 90%	—	—	0.5	ns
Fall Time	tf	$I_{bias} = I_{th}$, 90 ~ 10%	—	—	0.5	ns
Beam Divergence	θ	P_o = 5mW, FWHM	—	20	—	deg
Beam Divergence	θ	P_o = 5mW, FWHM	—	30	—	deg
Forward Voltage	VF	P_o = 5mW	—	—	1.6	V
Photosensitivity saturation voltage	VRs	—	—	—	2.0	V

HL1341A

Laser Diode

Description

HL1341A is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with buried hetero-structure.

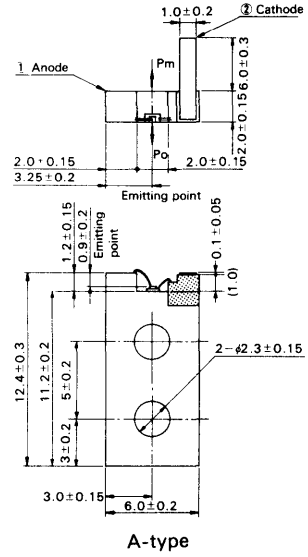
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1290–1330 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- Fast pulse response: t_r, t_f ≦ 0.5 ns

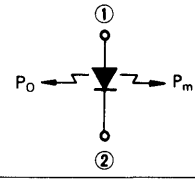
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	35		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

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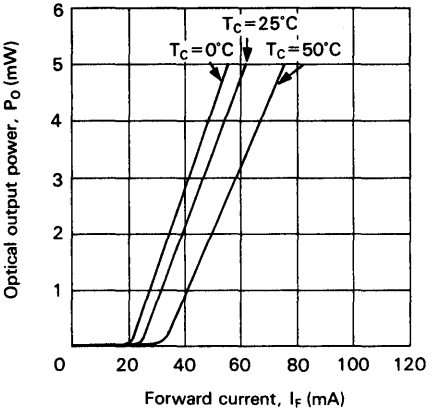
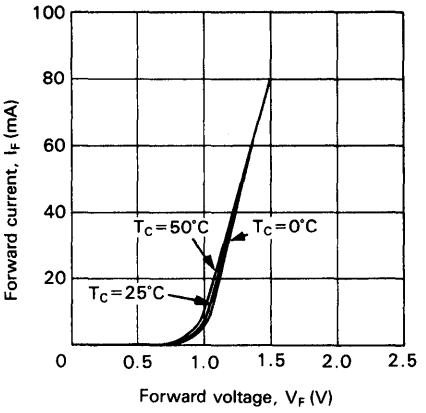
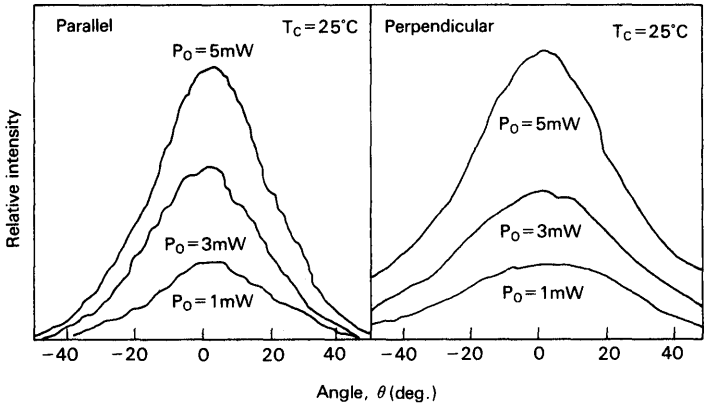
Optical Output Power vs. Forward Current



Forward Current vs. Forward Voltage



Far Field Pattern



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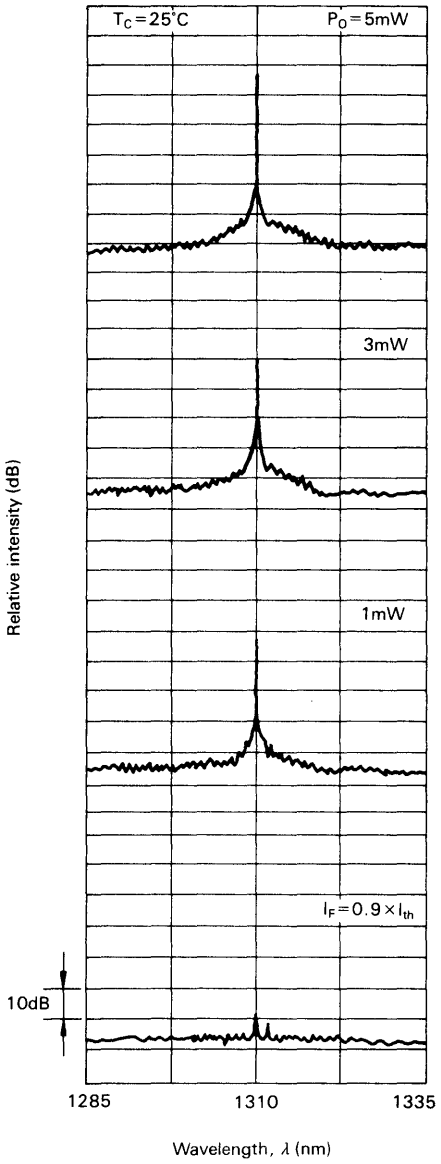
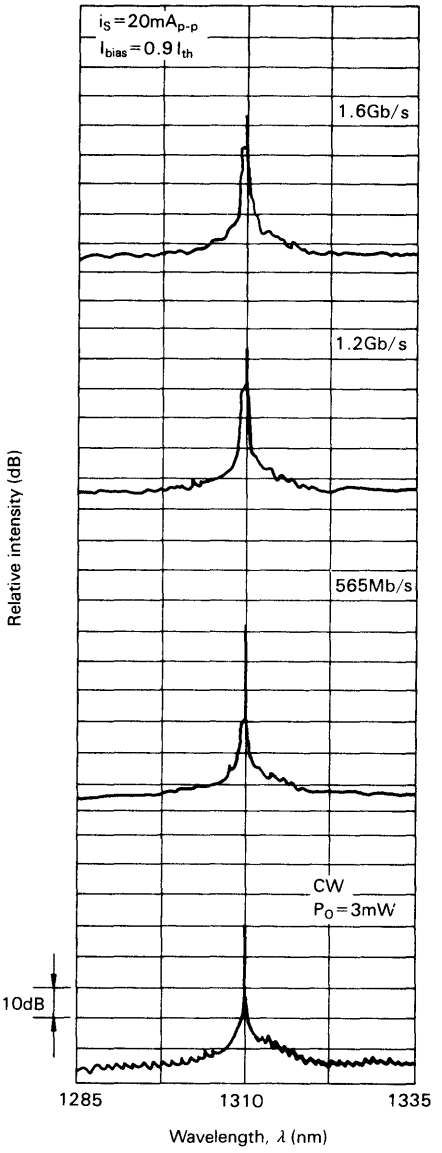
Output Power Dependence of Lasing Spectrum



Frequency Dependence of Lasing Spectrum



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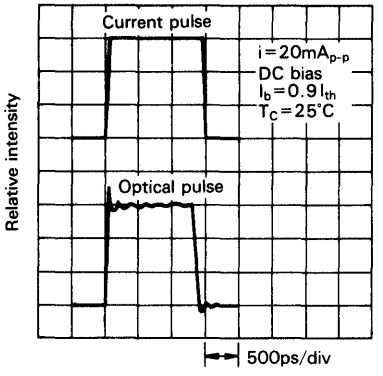
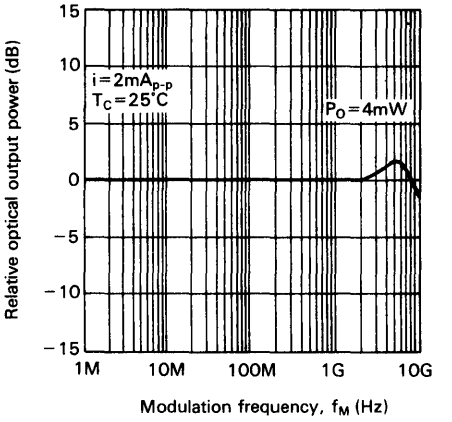
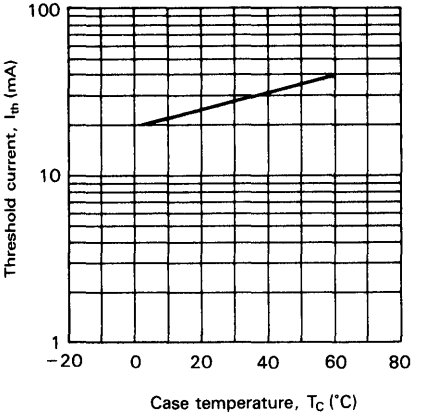
Pulse Response of Laser Diode



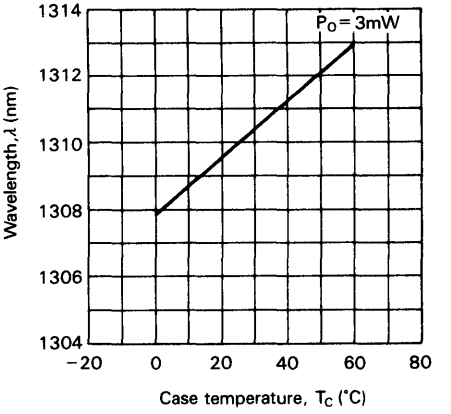
Frequency Response of Laser Diode



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



HL1341AC

Laser Diode

Description

HL1341AC is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with buried hetero-structure.

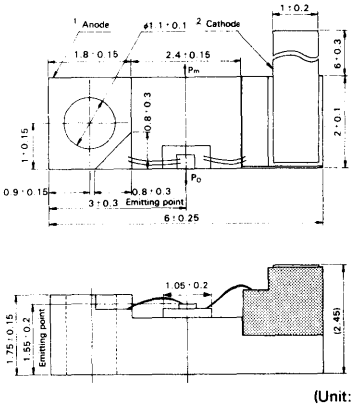
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is compact to facilitate module assembly.

Features

- Long wavelength light output: $\lambda_p = 1290-1330$ nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: $S_r = 35$ dB typ.
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

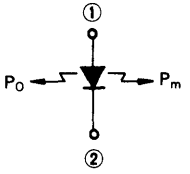
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25$°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_C = 25$°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	$P_O = 3$ mW
Side-mode suppression ratio	S_r	30	35		dB	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

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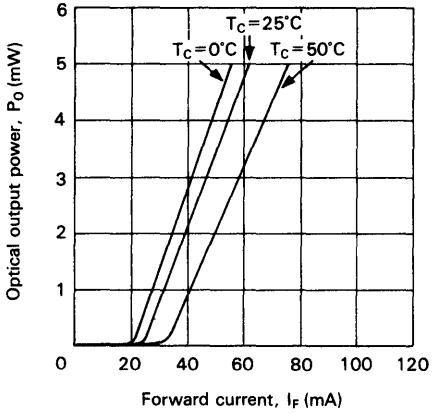
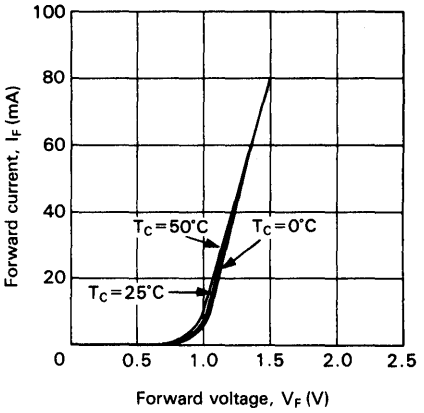
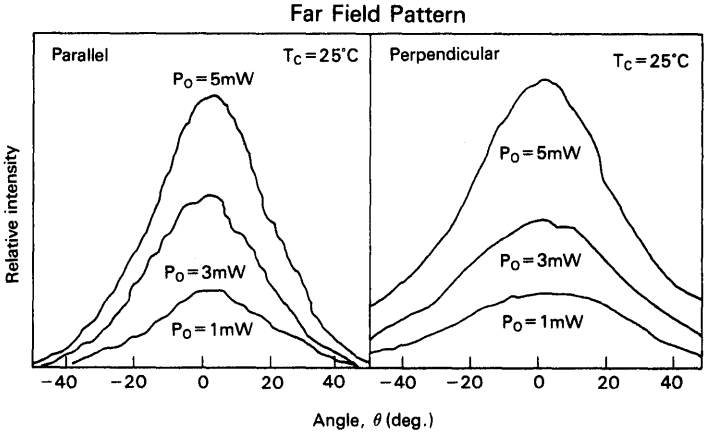
Optical Output Power vs. Forward Current



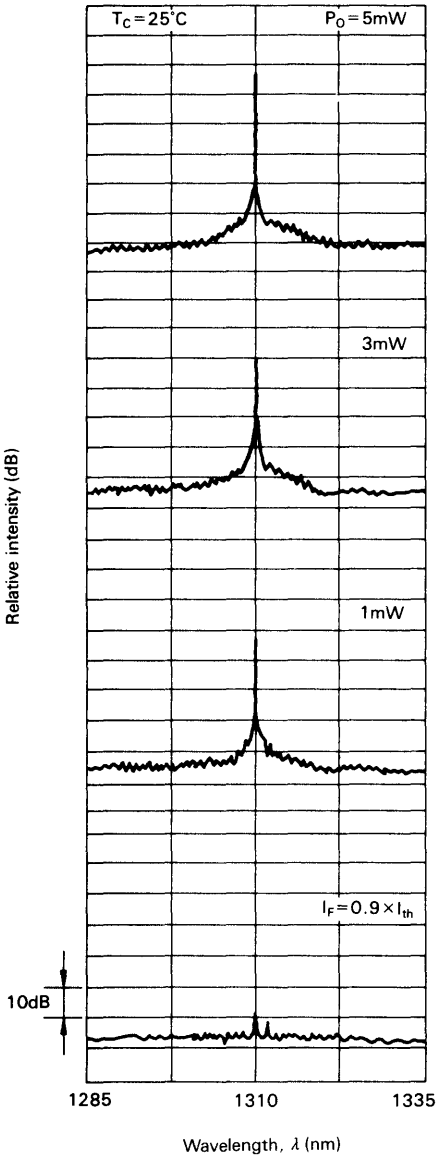
Forward Current vs. Forward Voltage



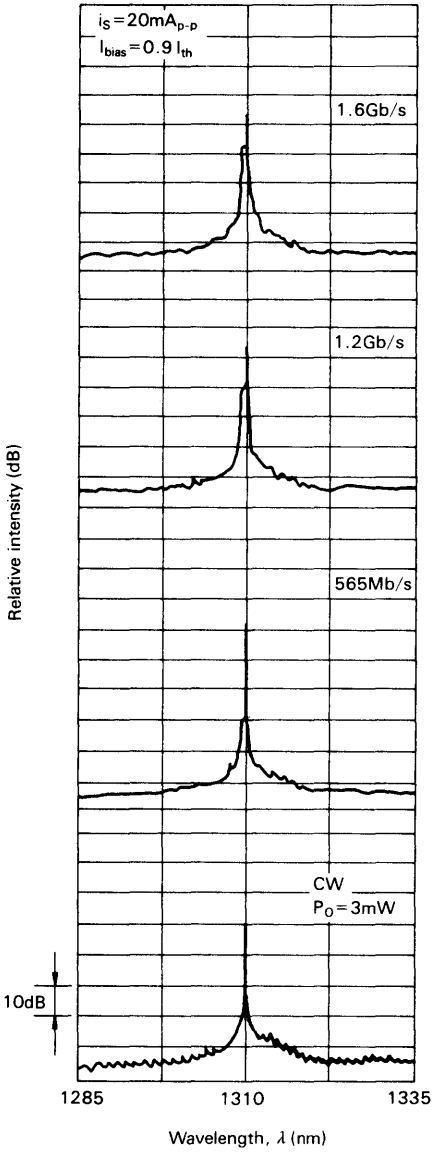
Far Field Pattern



Output Power Dependence of Lasing Spectrum



Frequency Dependence of Lasing Spectrum



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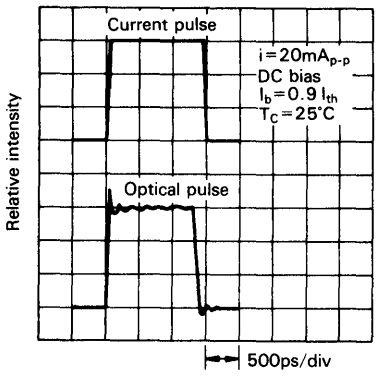
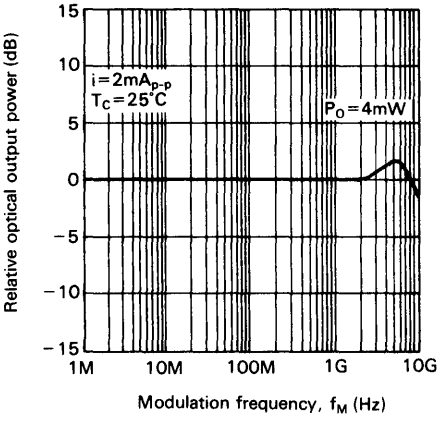
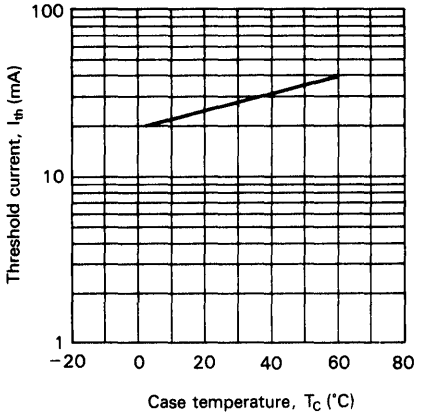
Pulse Response of Laser Diode



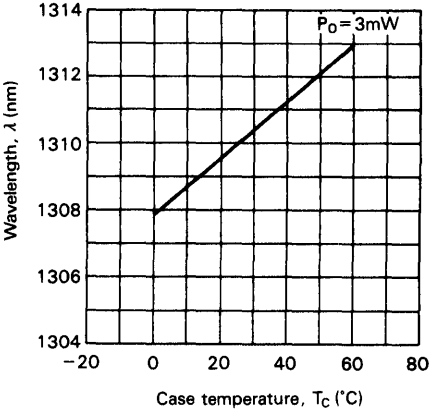
Frequency Response of Laser Diode



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



HL1341FG

Laser Diode

Description

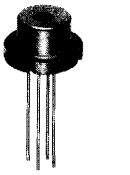
HL1341FG is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with buried heterostructure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

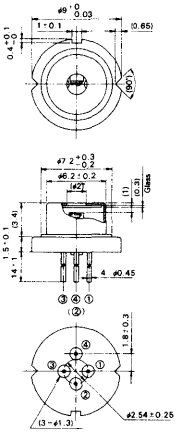
The laser beam is output through the glass window in the package cap. Monitoring current is output from a built-in photodiode.

Features

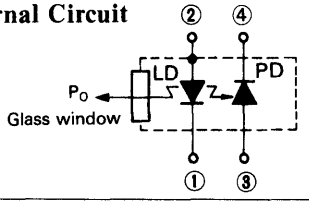
- Long wavelength light output: λ_p = 1290–1330 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- Built-in photodiode for monitoring laser output
- Fast pulse response: t_r, $t_f \leq 0.5$ ns



Package Dimensions



Internal Circuit



Absolute Maximum Ratings (T_C=25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	35		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	50			μA	$V_{R(PD)}$ = 5 V, P_O = 3 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	

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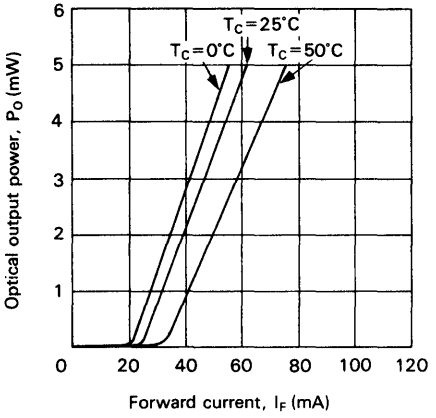
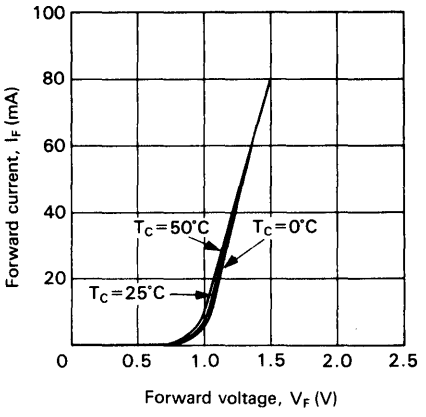
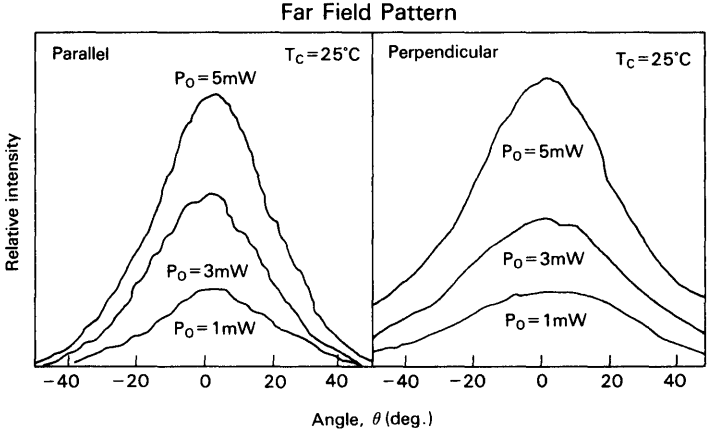
Optical Output Power vs. Forward Current



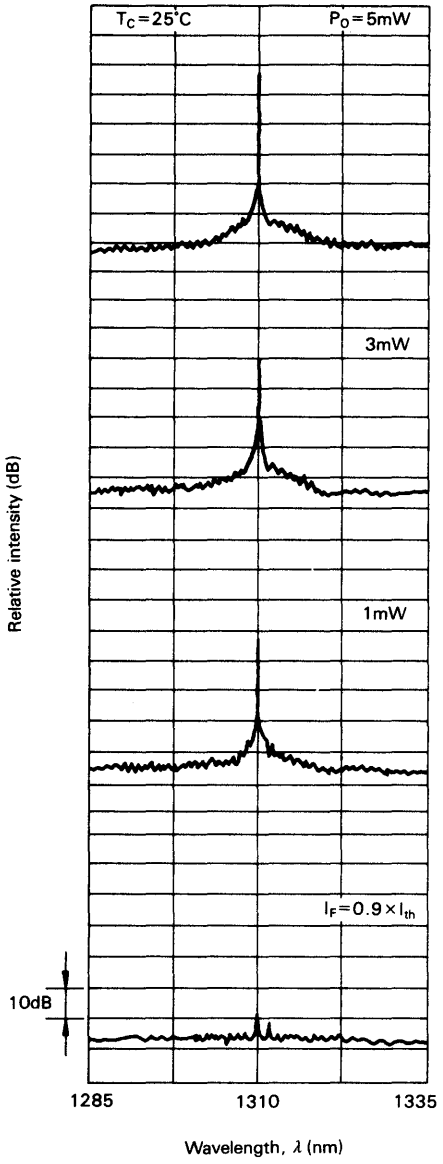
Forward Current vs. Forward Voltage



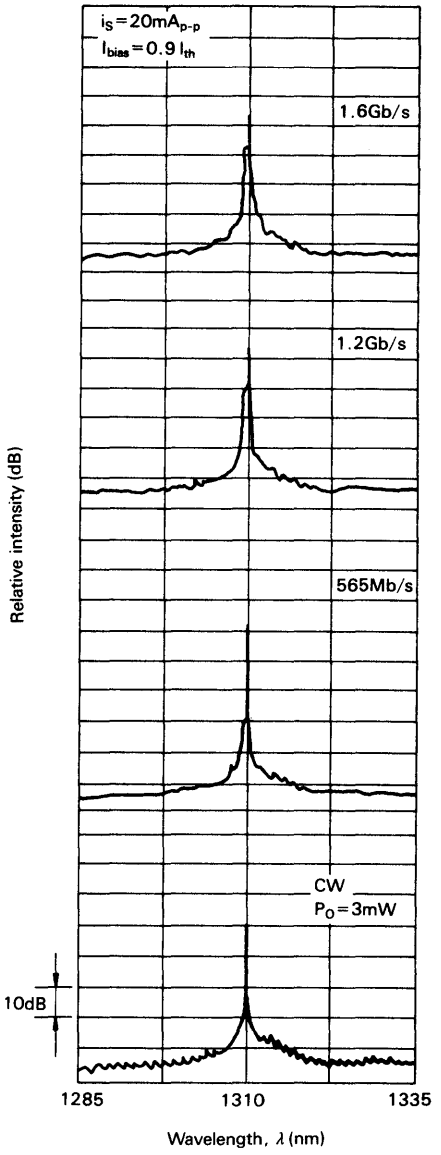
Far Field Pattern



Output Power Dependence of Lasing Spectrum



Frequency Dependence of Lasing Spectrum



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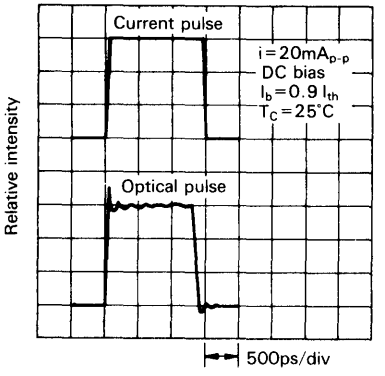
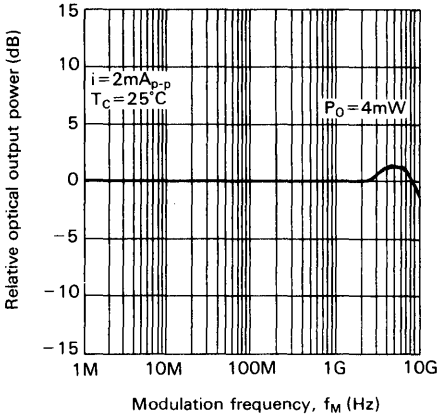
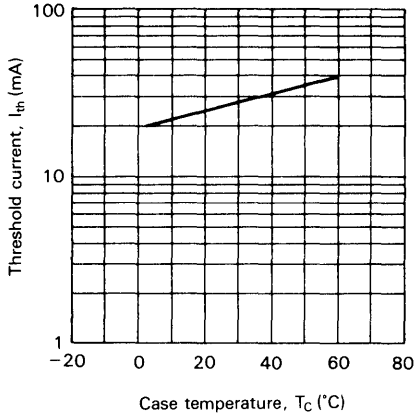
Pulse Response of Laser Diode



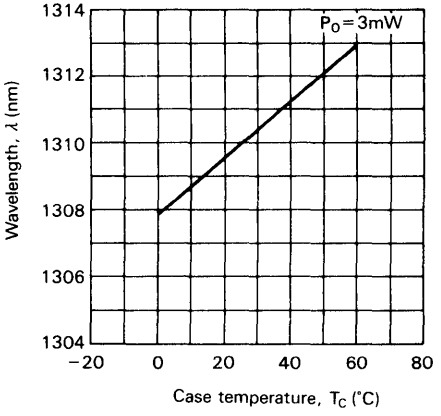
Frequency Response of Laser Diode



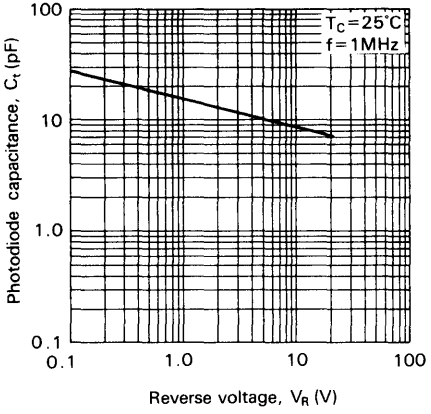
Threshold Current vs. Case Temperature



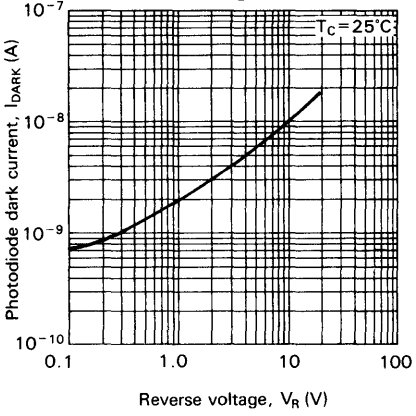
Temperature Dependence of Lasing Wavelength



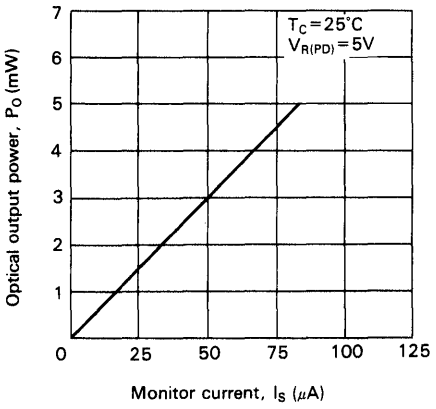
Photodiode Capacitance vs. Reverse Voltage



Photodiode Dark Current vs. Reverse Voltage



Optical Output Power vs.
Monitor Current



6

HL1341BF

Laser Diode

Description

HL1341BF is a DFB laser diode module in a 14-pin butterfly-type package with a built-in thermoelectronic controller and connected single-mode fiber.

It is suitable as a light source in high-speed modulated, high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

Mode field diameter	: 10.0 ± 1.0 μm
Cutoff wavelength	: 1.10—1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

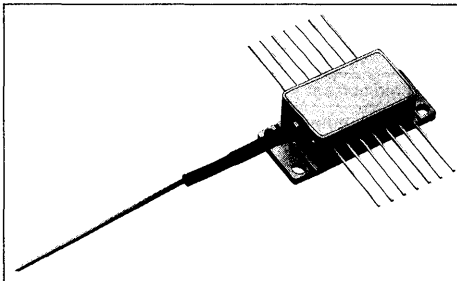
Features

- Long wavelength light output: λ_p = 1290—1330 nm
- 1.0 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- High-speed modulation (1.8 Gb/s)
- Stabilized operation with built-in thermoelectronic controller

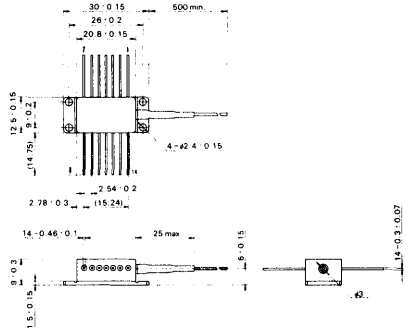
Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.0	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



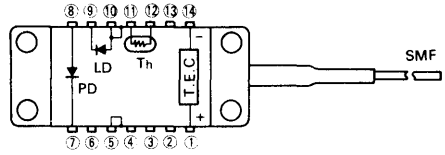
Package Dimensions



(Unit: mm)

BF-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode	⑧ PD anode
② N. C.	⑨ LD cathode
③ N. C.	⑩ LD anode (case)
④ N. C.	⑪ Thermistor
⑤ Case	⑫ Thermistor
⑥ N. C.	⑬ N. C.
⑦ PD cathode	⑭ T. E. C. cathode

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.0			mW	Kink free
		0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	$P_f = 0.5$ mW
Side-mode suppression ratio	S_r	30	35		dB	$P_f = 0.5$ mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)} = 5$ V
Monitor current	I_S	0.3			mA	$V_{R(PD)} = 5$ V, $P_f = 0.5$ mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)} = 5$ V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	$T_C = 60$°C, $P_f = 0.5$ mW
Cooler current	I_C			1.4	A	$\Delta T = 40$°C
Cooler voltage	V_C			1.8	V	$\Delta T = 40$°C
Thermistor resistance	R_{TM}		10		kΩ	

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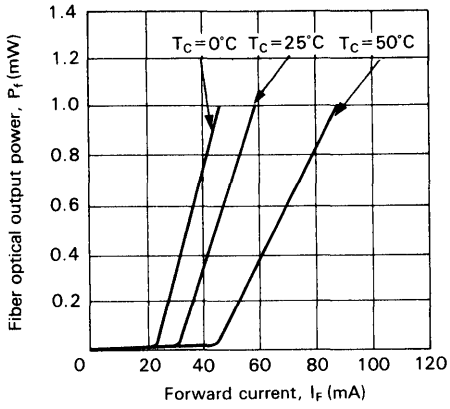
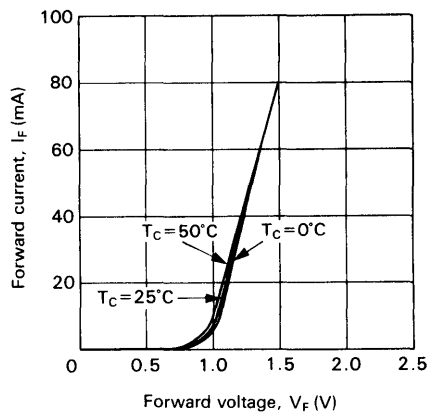
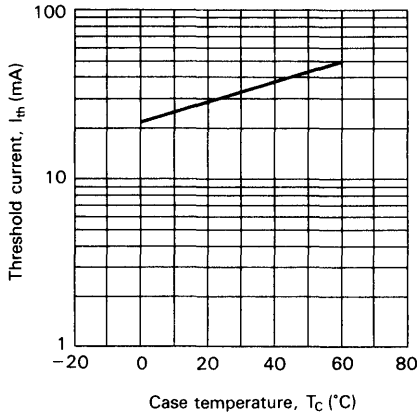
Optical Output Power vs. Forward Current



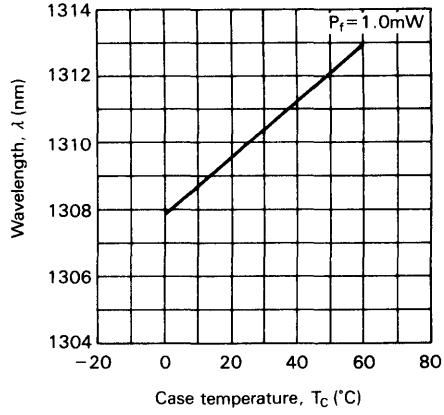
Forward Current vs. Forward Voltage



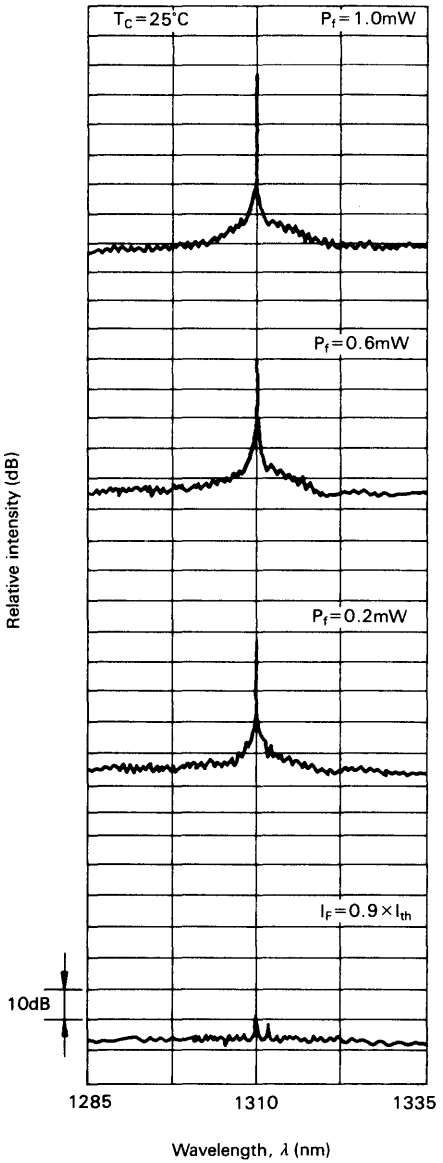
Threshold Current vs. Case Temperature



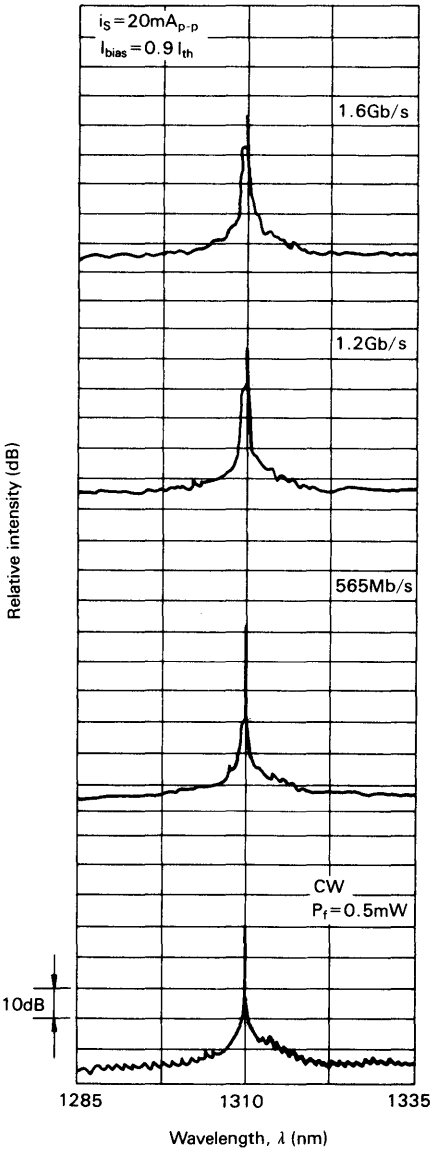
Temperature Dependence of Lasing Wavelength



Output Power Dependence of Lasing Spectrum



Frequency Dependence of Lasing Spectrum



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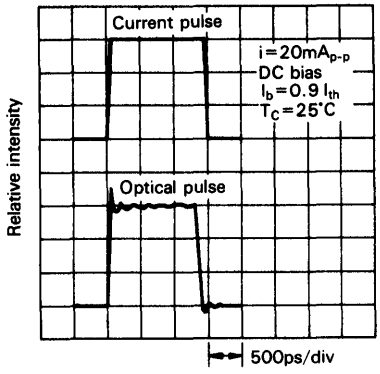
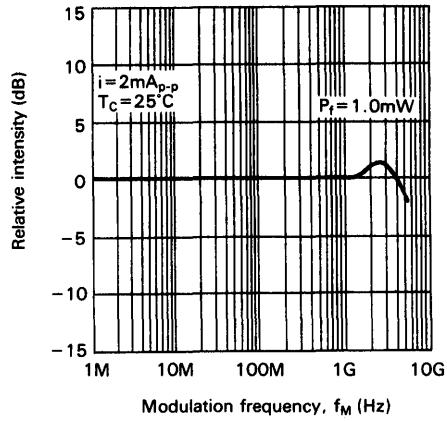
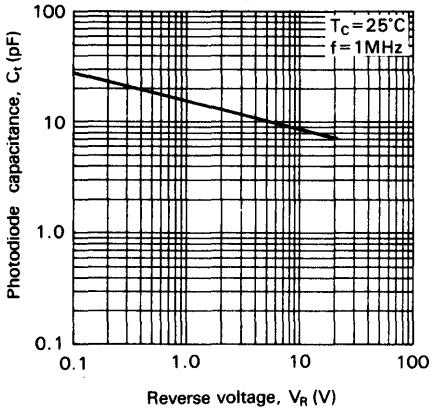
Pulse Response of Laser Diode



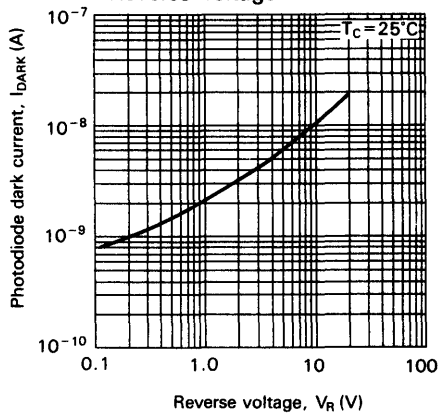
Frequency Response of Laser Diode



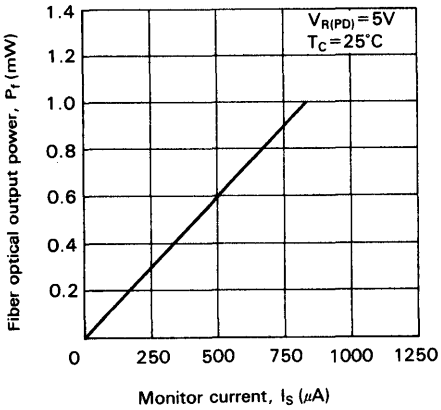
Photodiode Capacitance vs. Reverse Voltage



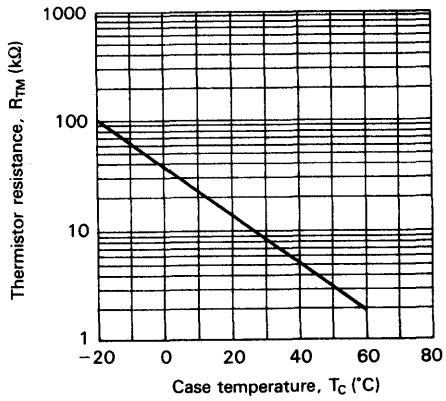
Photodiode Dark Current vs. Reverse Voltage



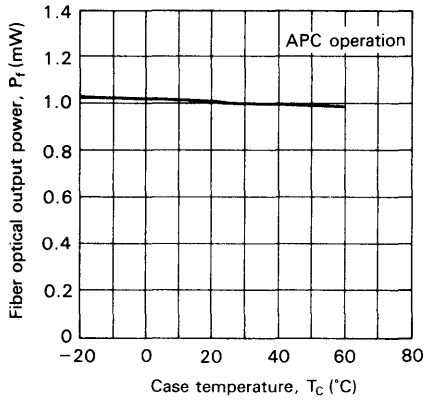
Optical Output Power vs. Monitor Current



Thermistor Resistance vs. Case Temperature



Tracking Characteristics



HL1341DL

Laser Diode

Description

HL1341DL is a DFB laser diode module in a 14-pin dual-in-line type package with a built-in thermoelectronic controller and connected single-mode fiber.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

Mode field diameter	: 10.0 ± 1.0 μm
Cutoff wavelength	: 1.10—1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

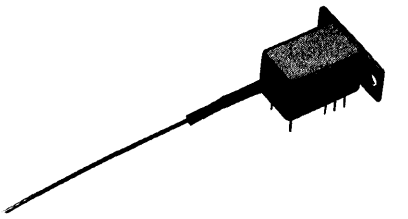
Features

- Long wavelength light output: λ_p = 1290—1330 nm
- 1.0 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- High-speed modulation (800 Mb/s)
- Stabilized operation with built-in thermoelectronic controller

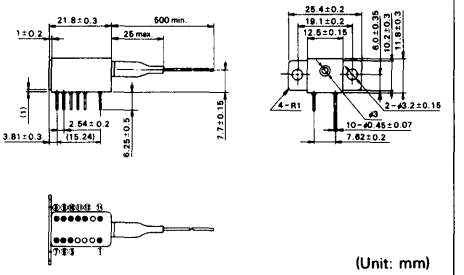
Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.0	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



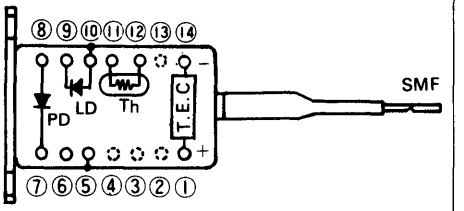
Package Dimensions



(Unit: mm)

DL-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② —
③ —
④ —
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ —
⑭ T. E. C. cathode

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.0			mW	Kink free
		0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r	30	35		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.3			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	T_C = 60°C, P_f = 0.5 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

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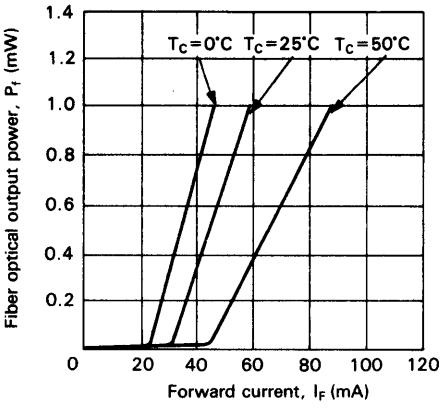
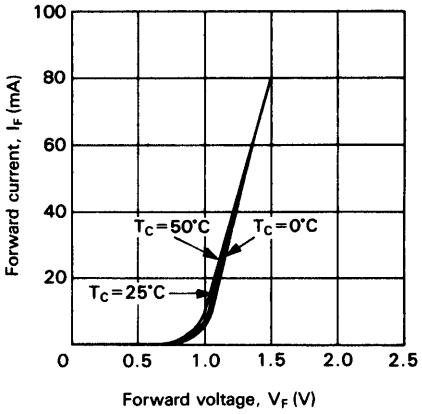
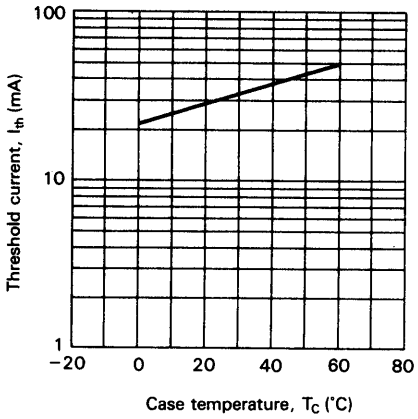
Optical Output Power vs. Forward Current



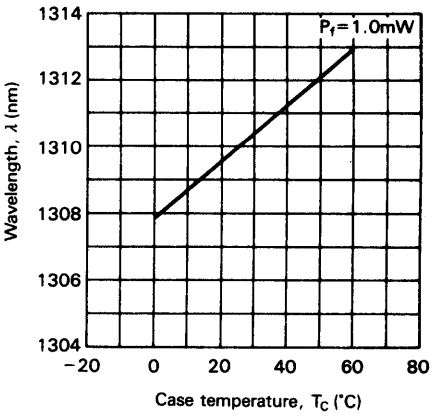
Forward Current vs. Forward Voltage



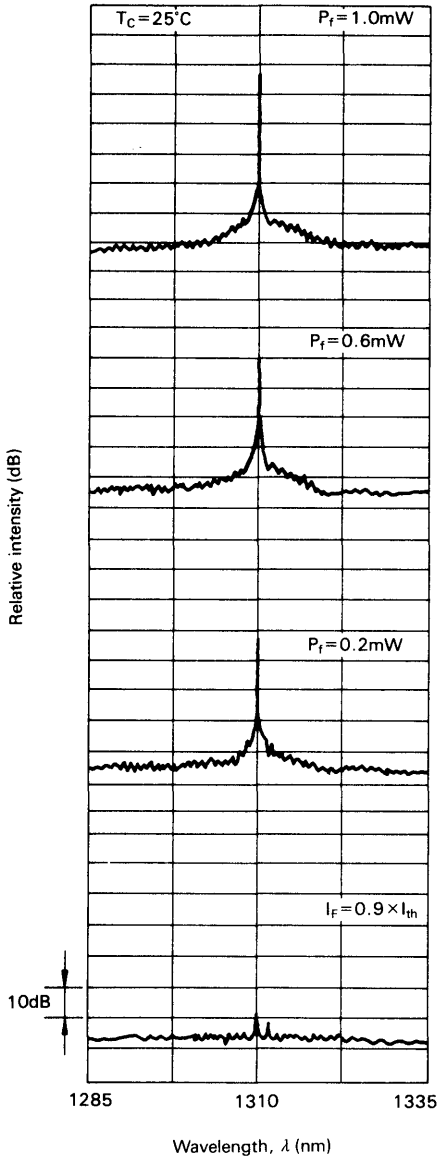
Threshold Current vs. Case Temperature



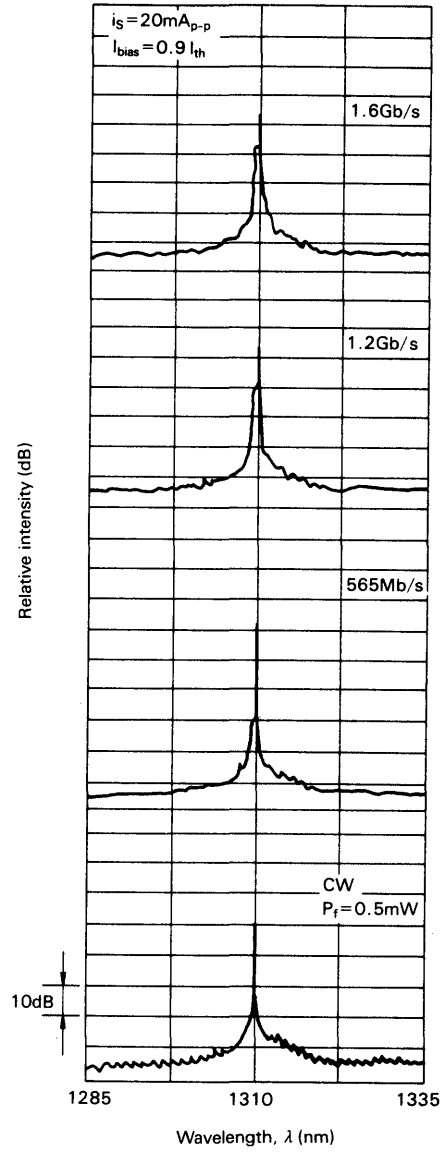
Temperature Dependence of Lasing Wavelength



Output Power Dependence of Lasing Spectrum

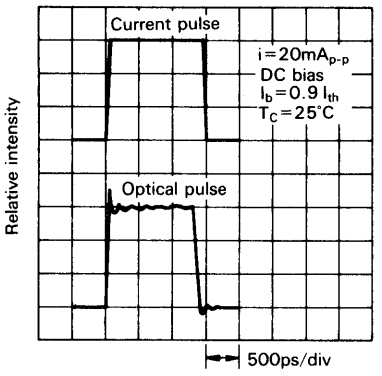


Frequency Dependence of Lasing Spectrum

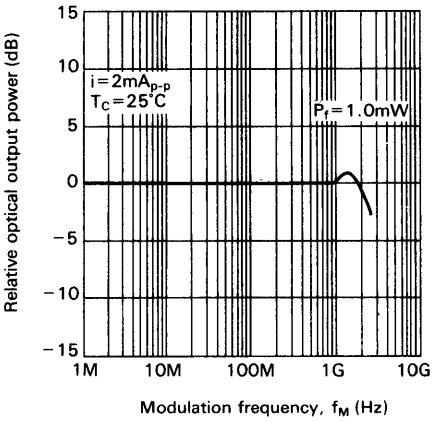


6

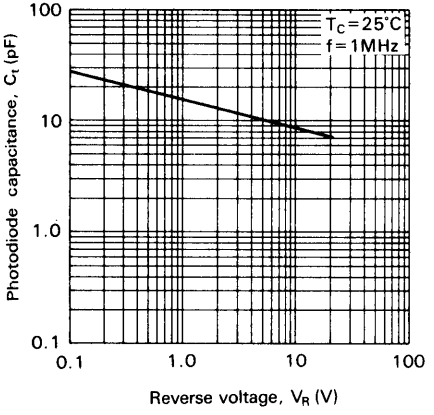
Pulse Response of Laser Diode



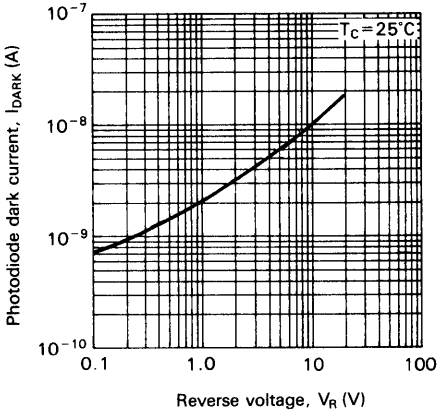
Frequency Response of Laser Diode



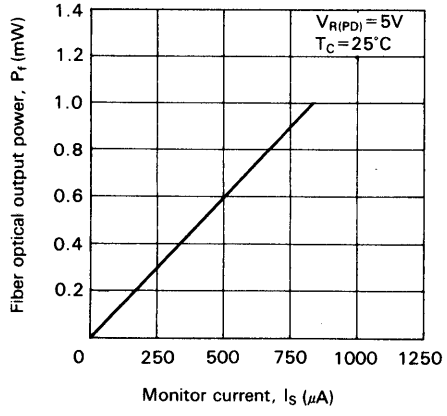
Photodiode Capacitance vs. Reverse Voltage



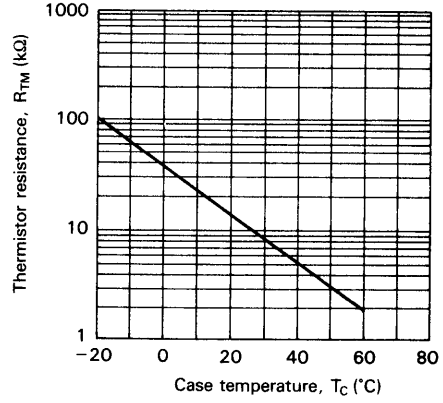
Photodiode Dark Current vs. Reverse Voltage



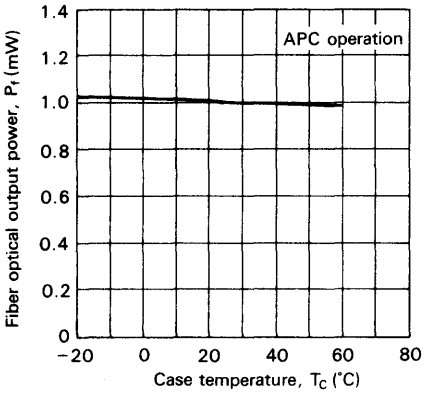
Optical Output Power vs. Monitor Current



Thermistor Resistance vs. Case Temperature



Tracking Characteristics



6

HL1361A

Under Development

Laser Diode

Description

HL1361A is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with $\lambda/4$ phase shifted.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

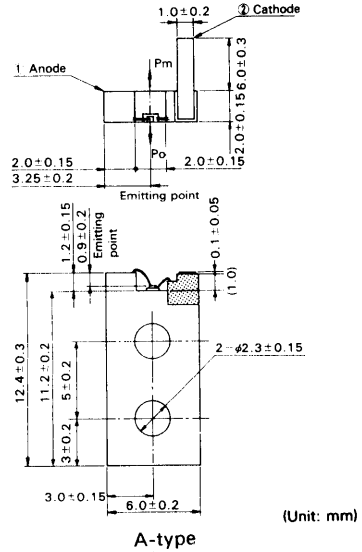
Direct photo-exposure technology is employed to have fine phase-shifted grating.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1290–1330 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: S_r = 38 dB typ.
- Fast pulse response: t_r = 0.15 ns, t_f = 0.2 ns typ.
- High-speed modulation (2.4 Gb/s)

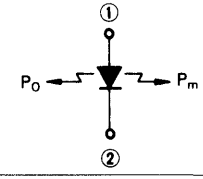
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	1.0			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	38		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r		0.15		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.2		ns	$I_{bias} = I_{th}$, 90 to 10%

HL1361AC

Under Development

Laser Diode

Description

HL1361AC is a 1.3 μm InGaAsP distributed-feedback (DFB) laser diode with $\lambda/4$ phase shifted.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

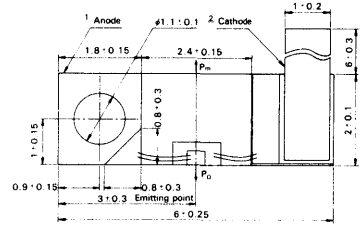
Direct photo-exposure technology is employed to have fine phase-shifted grating.

The package is compact to facilitate module assembly.

Features

- Long wavelength light output: λ_p = 1290–1330 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: S_r = 38 dB typ.
- Fast pulse response: t_r = 0.15 ns, t_f = 0.2 ns typ.
- High-speed modulation (2.4 Gb/s)

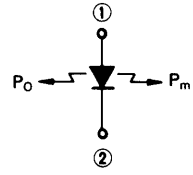
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.5			mW	$I_F = I_{th}$ + 20 mA
Monitor power	P_m	1.0			mW	$I_F = I_{th}$ + 20 mA
Lasing wavelength	λ_p	1290	1310	1330	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	38		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r		0.15		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.2		ns	$I_{bias} = I_{th}$, 90 to 10%

6

HL1521A

Laser Diode

Description

HL1521A is a 1.55 μm InGaAsP laser diode with double heterojunction structure.

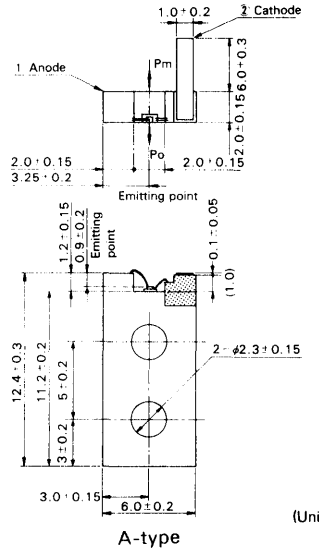
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1530–1570 nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

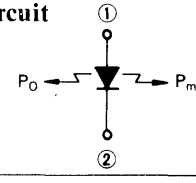
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

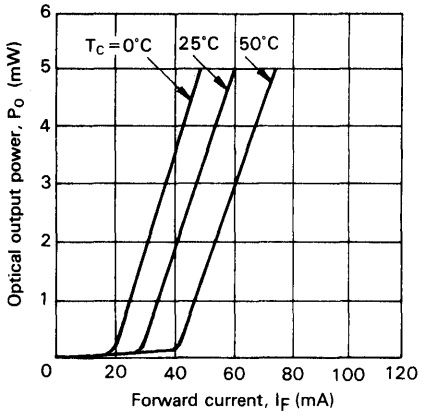
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

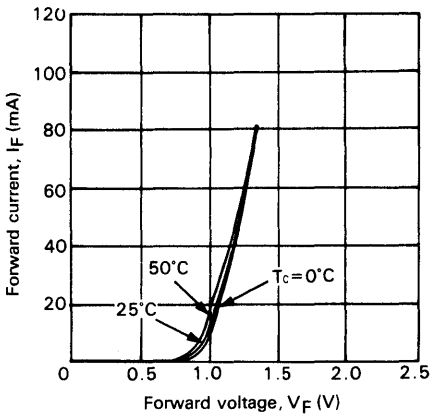
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.0			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.45			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

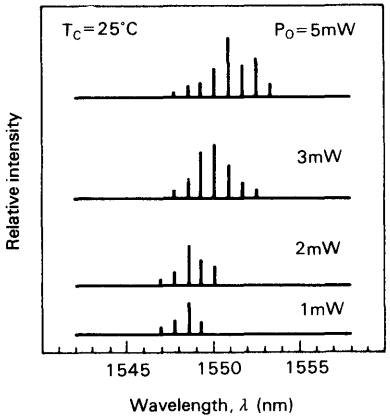
Optical Output Power vs. Forward Current



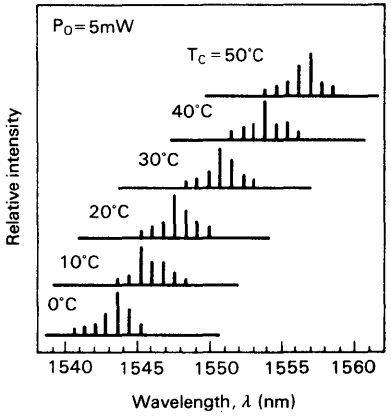
Forward Current vs. Forward Voltage



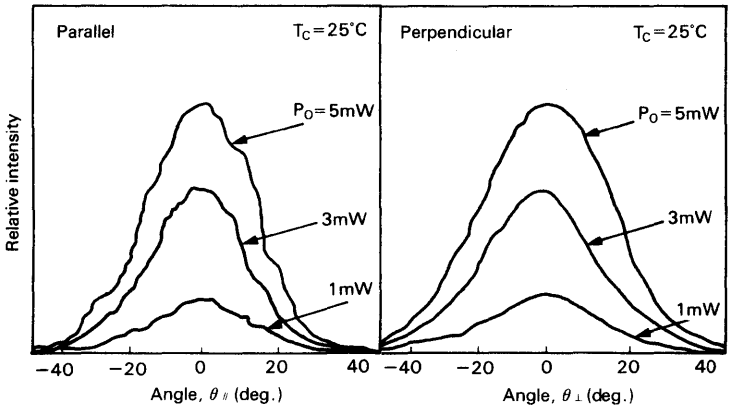
Lasing Spectrum



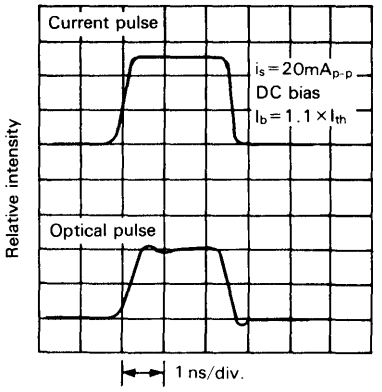
Temperature Dependence of Lasing Spectrum



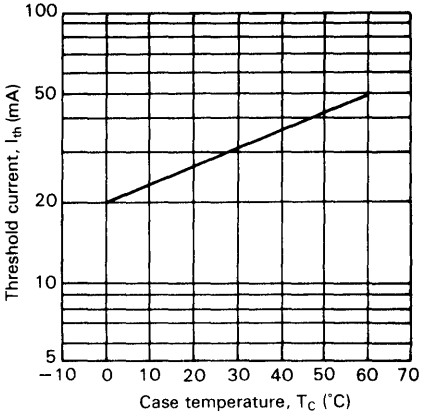
Far Field Pattern



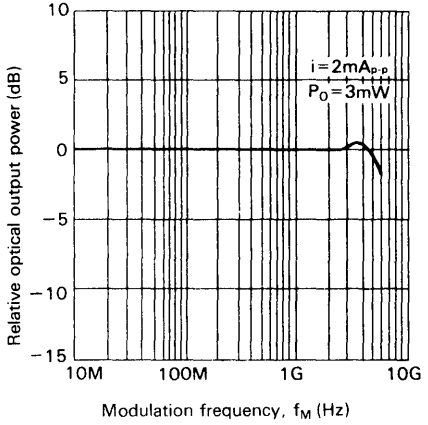
Pulse Response



Threshold Current vs. Case Temperature



Frequency Response of Laser Diode



HL1521AC

Laser Diode

Description

HL1521AC is a 1.55 μm InGaAsP laser diode with double heterojunction structure.

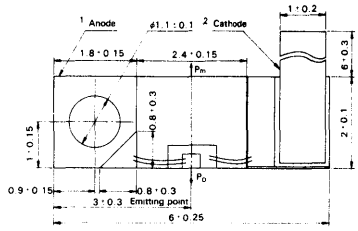
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is compact to facilitate module assembly.

Features

- Long wavelength light output: $\lambda_p = 1530-1570$ nm
- 5 mW CW operation at room temperature
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

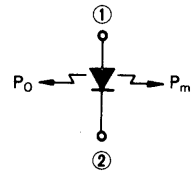
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

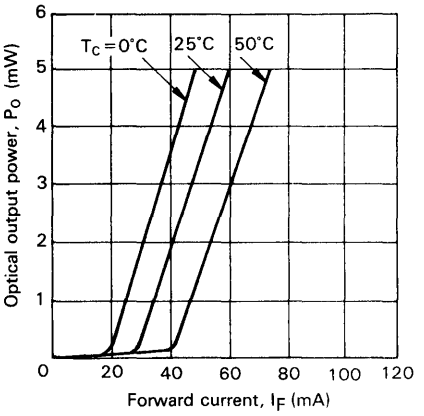
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_C = 25°C$)

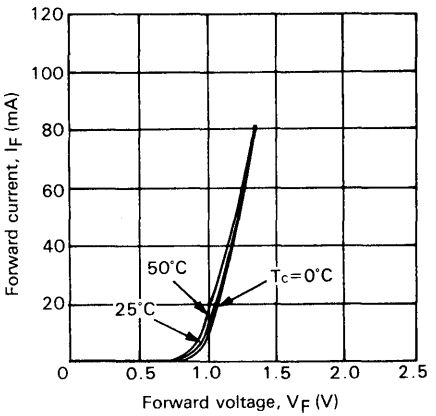
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		2.0			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.45			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	$P_O = 3$ mW
Spectral width	$\Delta\lambda$		2		nm	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

6

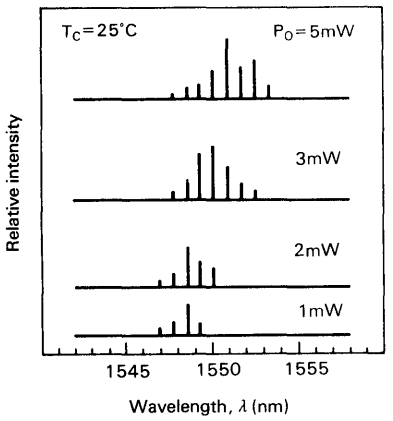
Optical Output Power vs. Forward Current



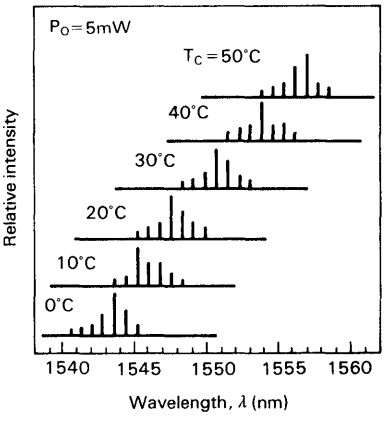
Forward Current vs. Forward Voltage



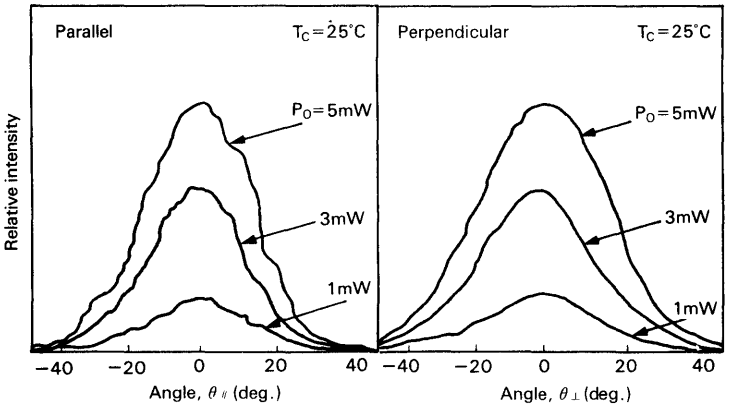
Lasing Spectrum



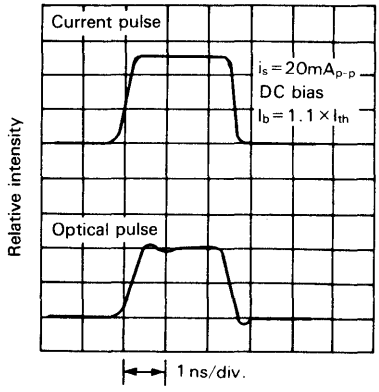
Temperature Dependence of Lasing Spectrum



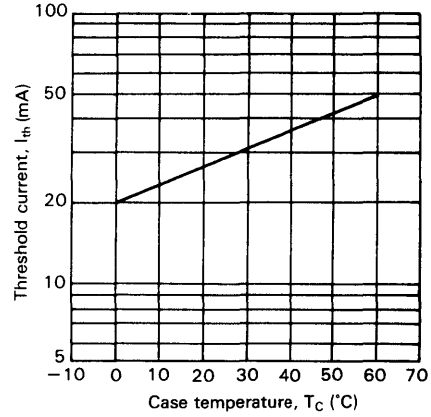
Far Field Pattern



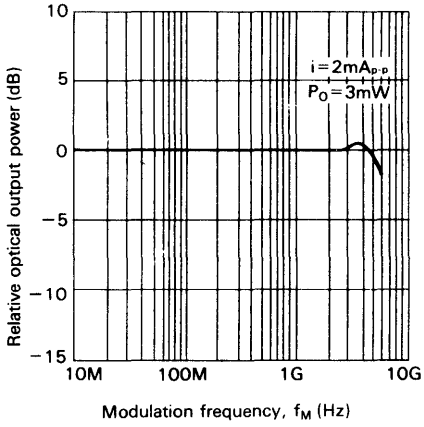
Pulse Response



Threshold Current vs. Case Temperature



Frequency Response of Laser Diode



6

HL1521FG

Laser Diode

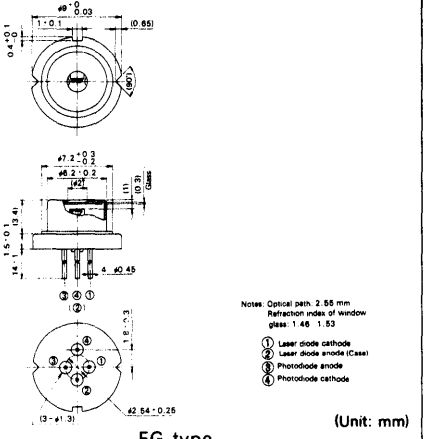
Description

HL1521FG is a 1.55 μm InGaAsP laser diode with buried heterostructure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The laser beam is output through the glass window in the package cap. Monitoring current is output from a built-in photodiode.

Package Dimensions



FG-type

Features

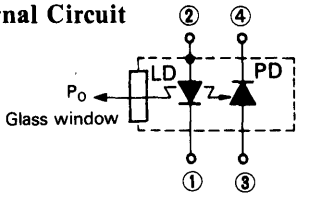
- Long wavelength light output: λ_p = 1530–1570 nm
- 5 mW CW operation at room temperature
- Built-in photodiode for monitoring laser output
- Fast pulse response: t_r, t_f ≦ 0.5 ns

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

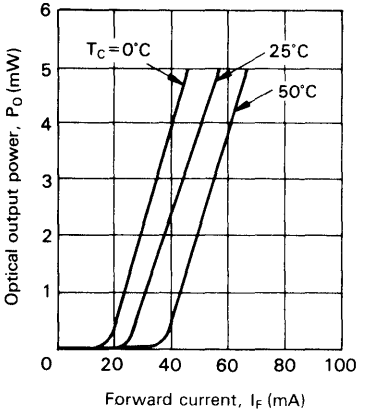
Internal Circuit



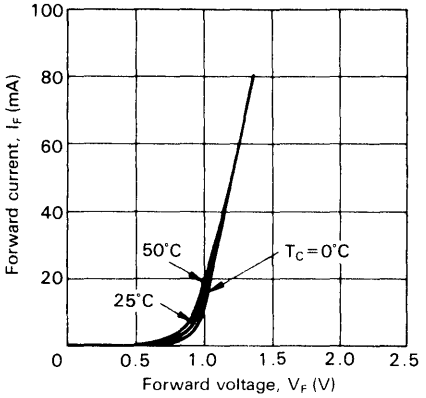
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5			mW	$I_F = I_{th}$ + 20 mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_O = 3 mW
Spectral width	$\Delta\lambda$		2		nm	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	50			μA	$V_{R(PD)}$ = 5 V, P_O = 3 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r			0.5	ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f			0.5	ns	$I_{bias} = I_{th}$, 90 to 10%

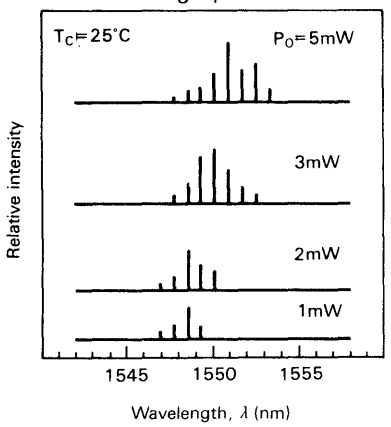
Optical Output Power vs. Forward Current



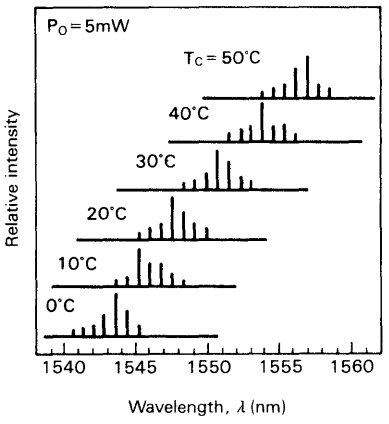
Forward Current vs. Forward Voltage



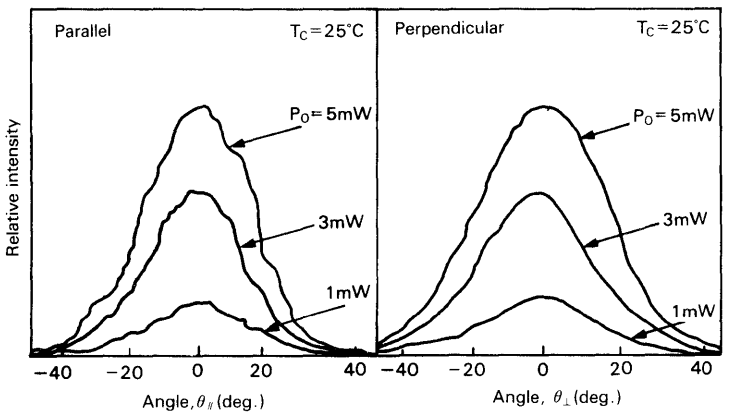
Lasing Spectrum



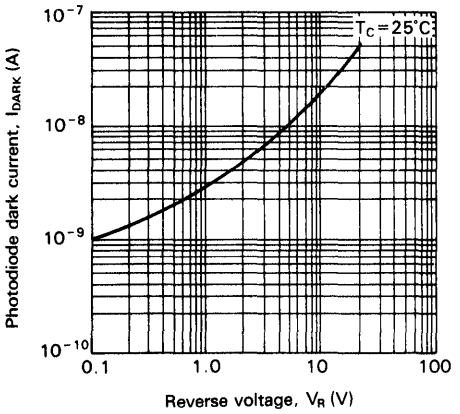
Temperature Dependence of Lasing Spectrum



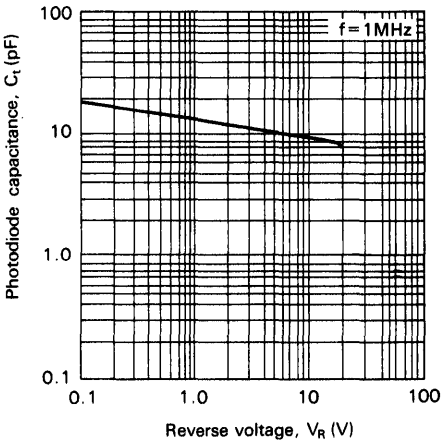
Far Field Pattern



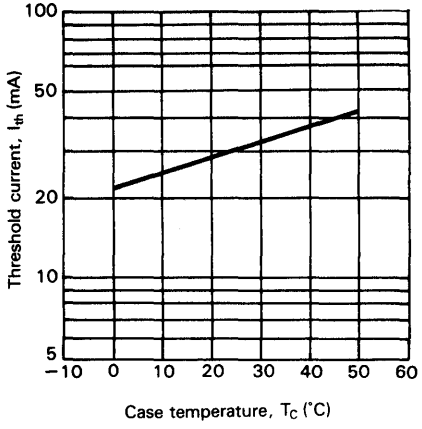
Photodiode Dark Current vs. Reverse Voltage



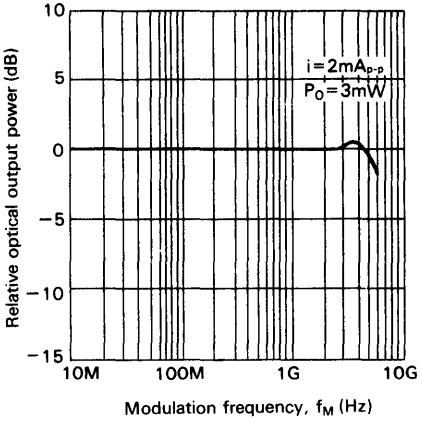
Photodiode Capacitance vs. Reverse Voltage



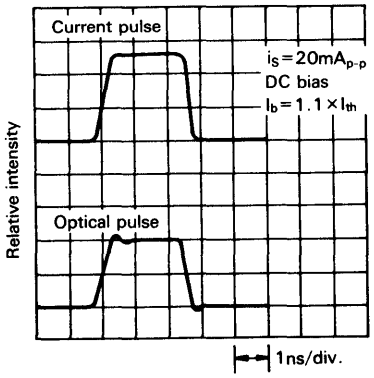
Threshold Current vs. Case Temperature



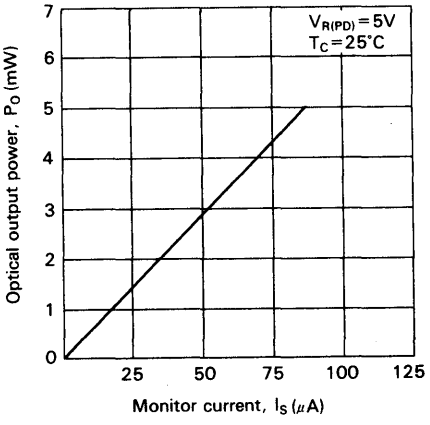
Frequency Response of Laser Diode



Pulse Response of Laser Diode



Optical Output Power vs. Monitor Current



HL1541A

Laser Diode

Description

HL1541A is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with buried heterostructure.

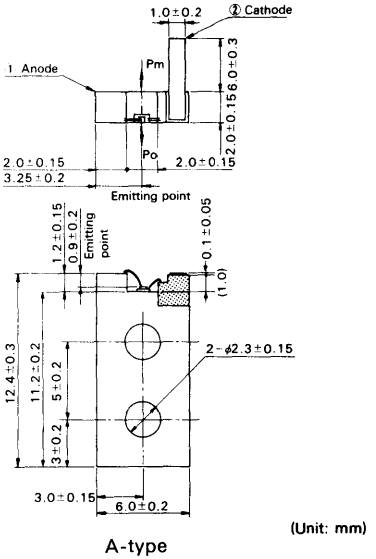
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

- Long wavelength light output: λ_p = 1530–1570 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- Fast pulse response: t_r, t_f ≦ 0.5 ns

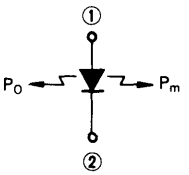
Package Dimensions



(Unit: mm)

A-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	35		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

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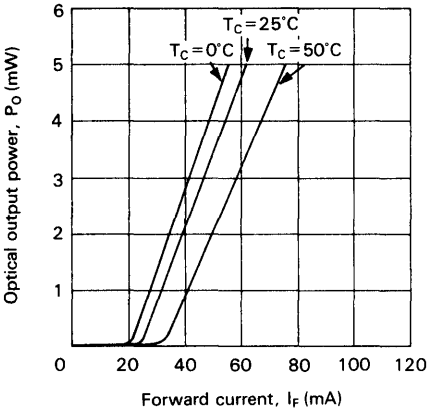
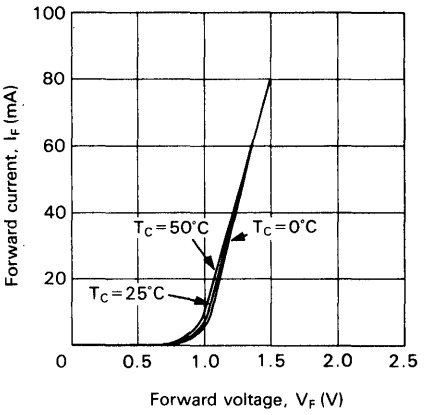
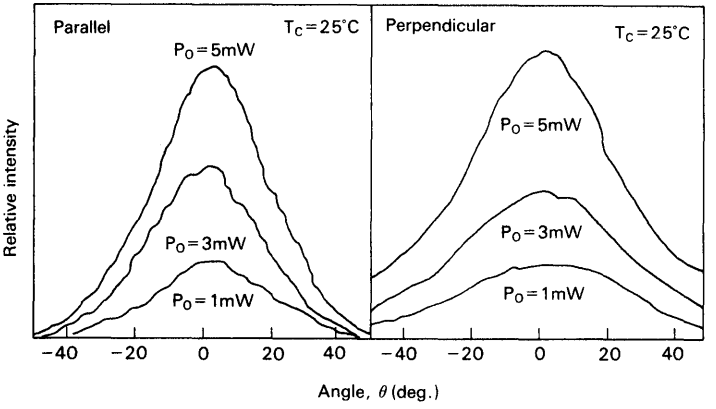
Optical Output Power vs. Forward Current



Forward Current vs. Forward Voltage



Far Field Pattern



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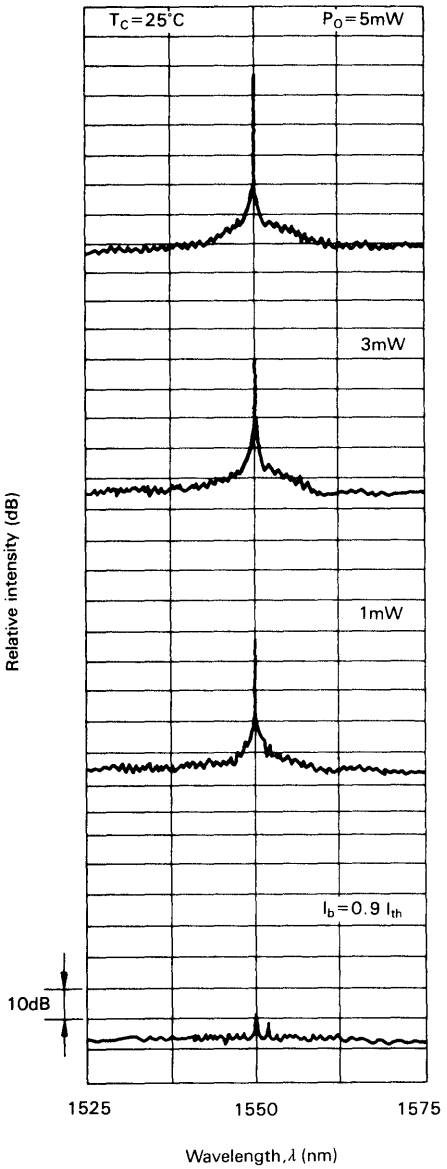
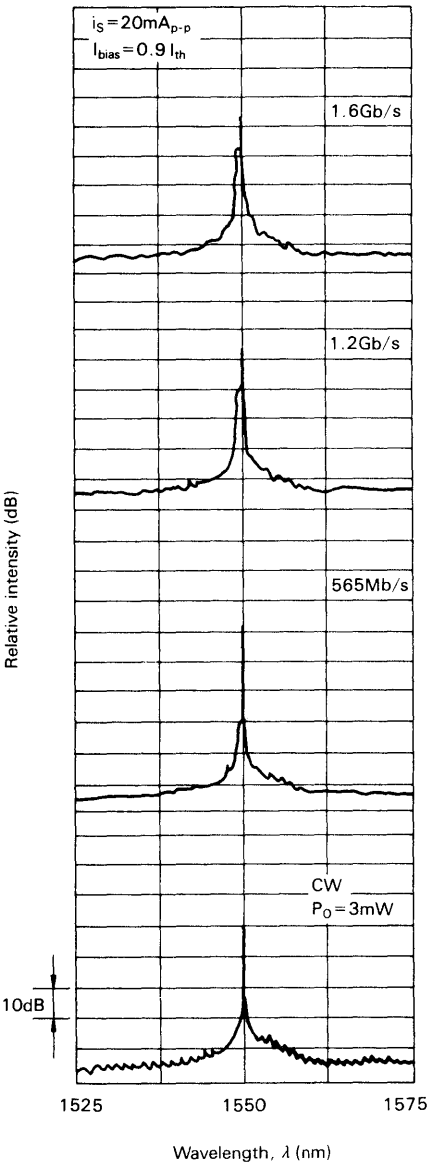
Output Power Dependence of Lasing Spectrum



Frequency Dependence of Lasing Spectrum



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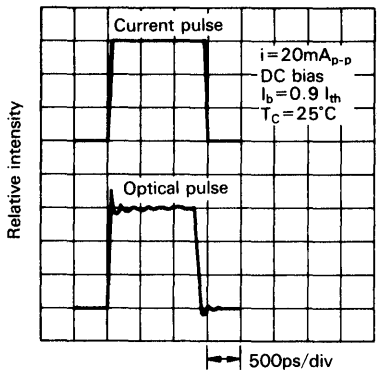
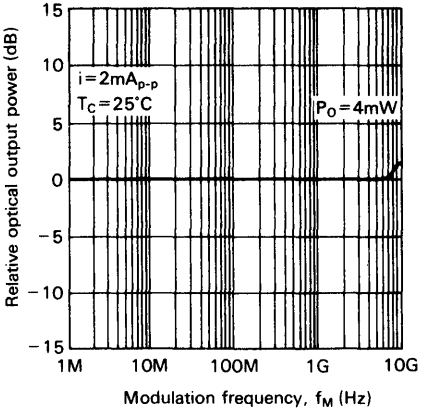
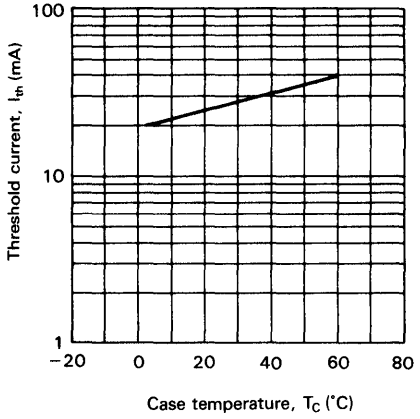
Pulse Response of Laser Diode



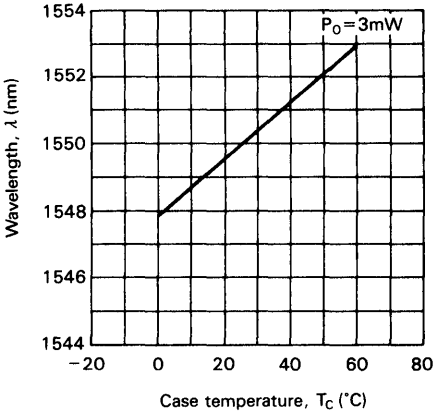
Frequency Response of Laser Diode



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



HL1541AC

Laser Diode

Description

HL1541AC is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with buried hetero-structure.

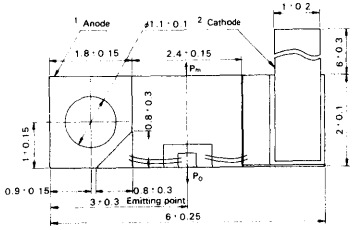
It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

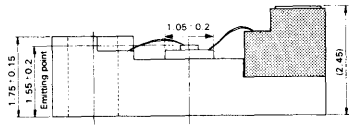
The package is compact to facilitate module assembly.

Features

- Long wavelength light output: $\lambda_p = 1530-1570$ nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: $S_r = 35$ dB typ.
- Fast pulse response: t_r, $t_f \leqq 0.5$ ns

Package Dimensions

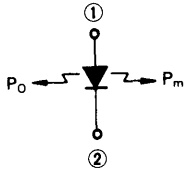




(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

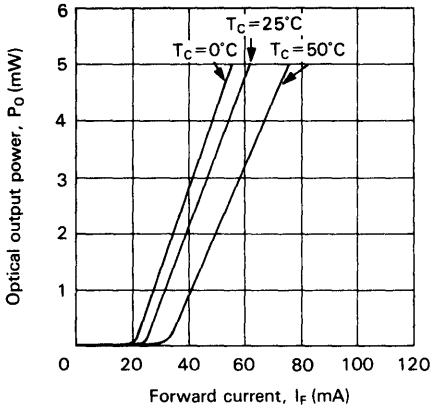
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_C = 25°C$)

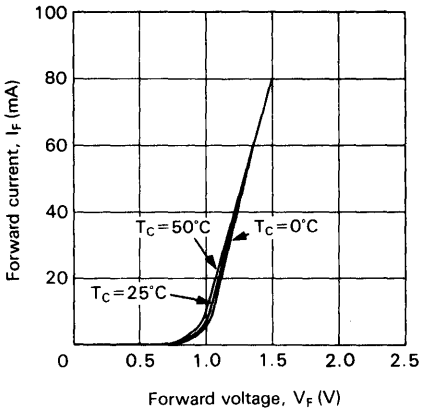
Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.5			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	$P_O = 3$ mW
Side-mode suppression ratio	S_r	30	35		dB	$P_O = 3$ mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	$P_O = 3$ mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	$P_O = 3$ mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	

6

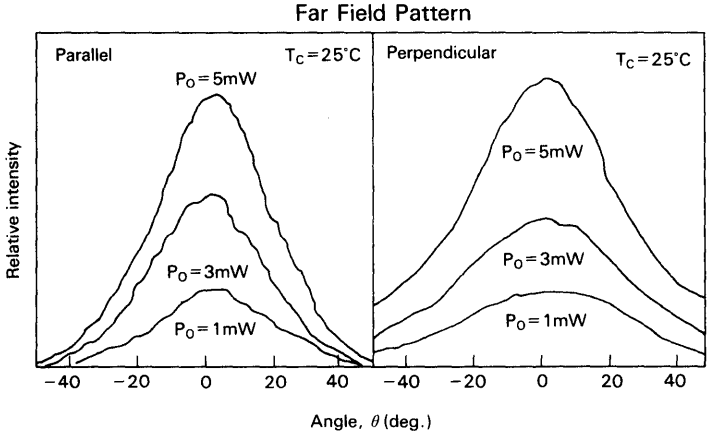
Optical Output Power vs. Forward Current



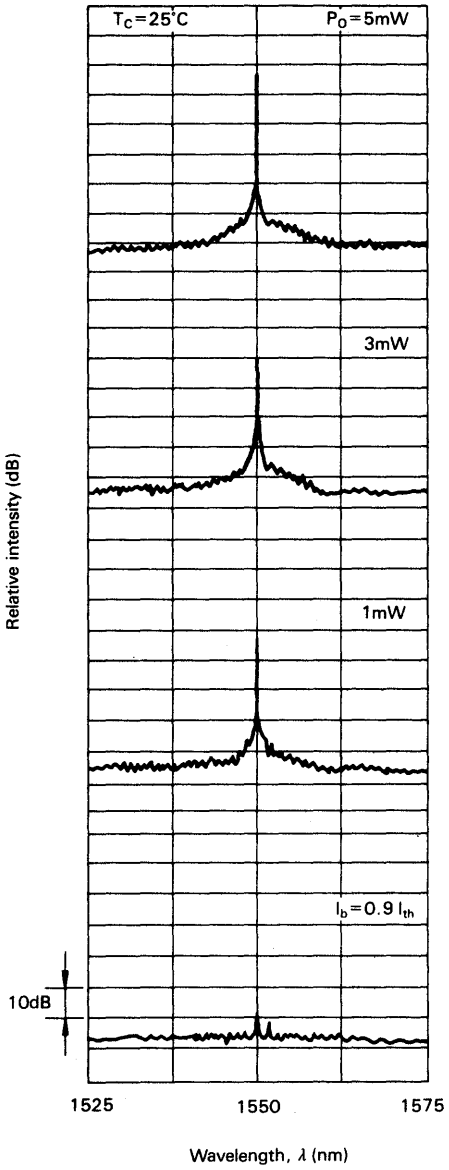
Forward Current vs. Forward Voltage



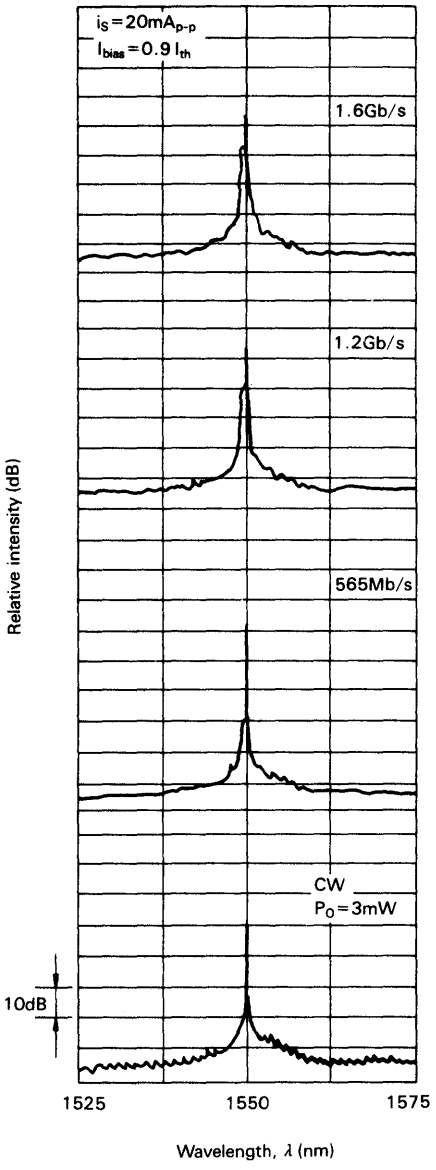
Far Field Pattern



Output Power Dependence of Lasing Spectrum



Frequency Dependence of Lasing Spectrum



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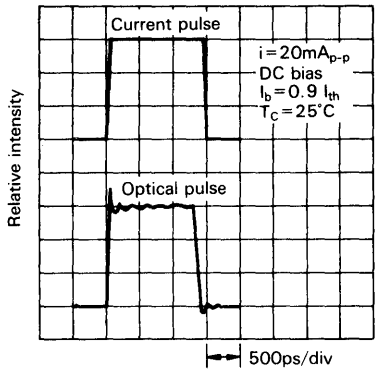
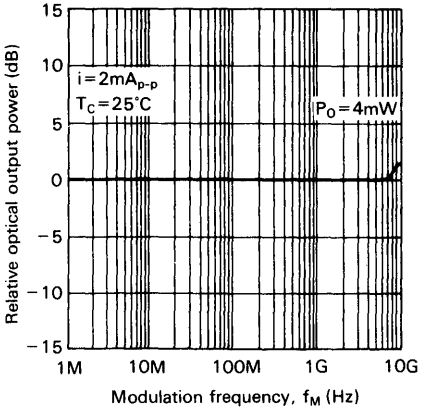
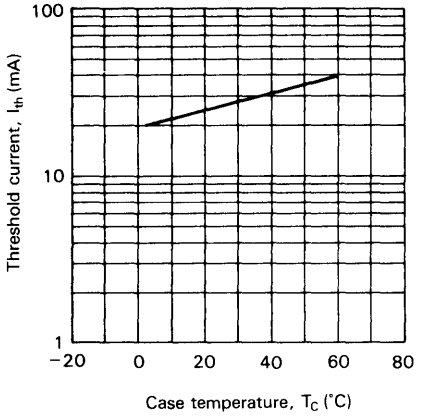
Pulse Response of Laser Diode



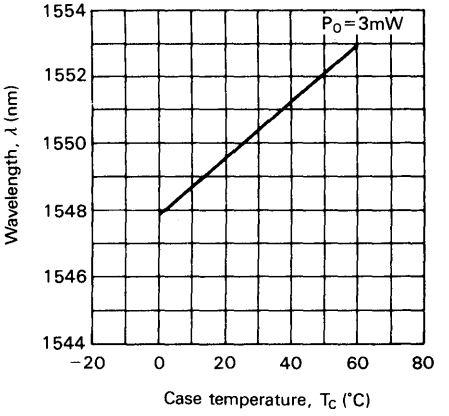
Frequency Response of Laser Diode



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



HL1541FG

Laser Diode

Description

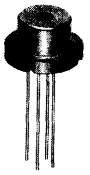
HL1541FG is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with buried hetero-structure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

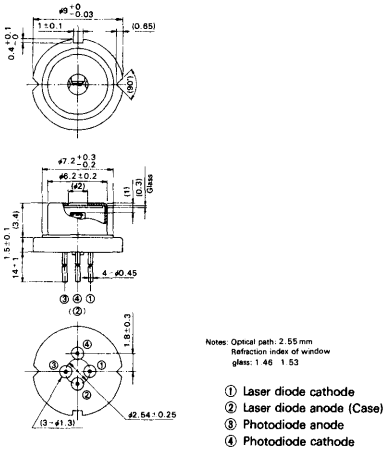
The laser beam is output through the glass window in the package. Monitoring current is output from a built-in photodiode.

Features

- Long wavelength light output:
  λ_p = 1530–1570 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode:
  S_r = 35 dB typ.
- Built-in photodiode for monitoring laser output
- Fast pulse response: t_r, t_f ≦ 0.5 ns



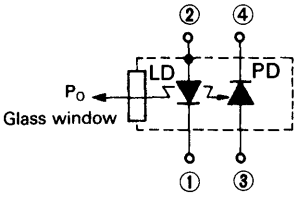
Package Dimensions



FG-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

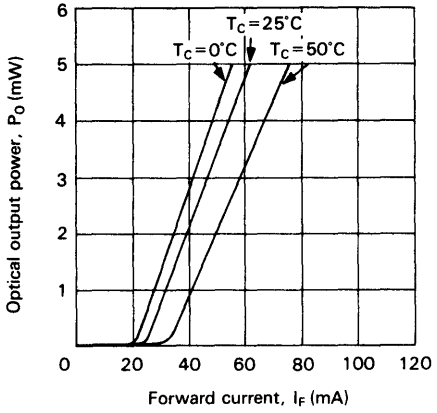
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

6

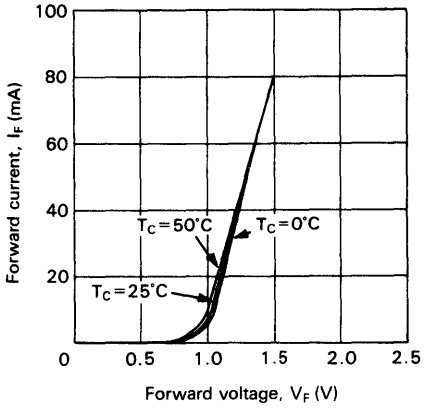
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5	3.0		mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	35		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r			0.5	ns	
Fall time	t_f			0.5	ns	
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	50			μA	$V_{R(PD)}$ = 5 V, P_O = 3 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	

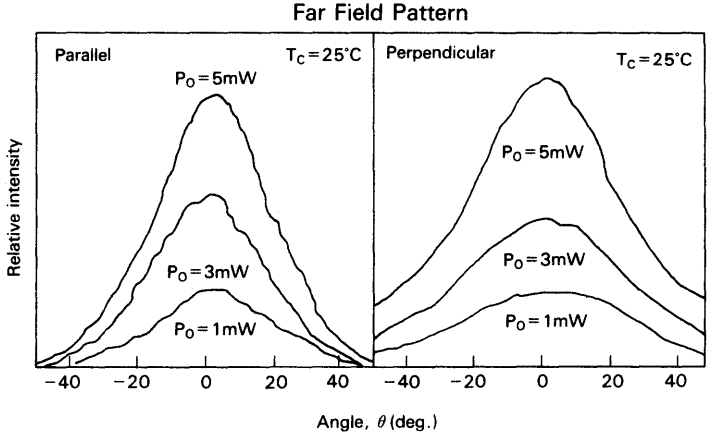
Optical Output Power vs. Forward Current



Forward Current vs. Forward Voltage

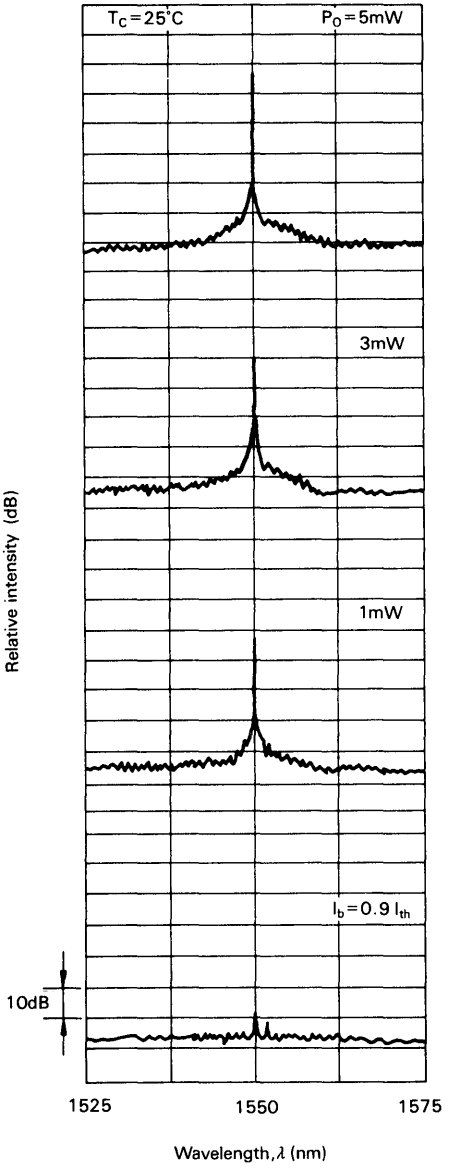


Far Field Pattern

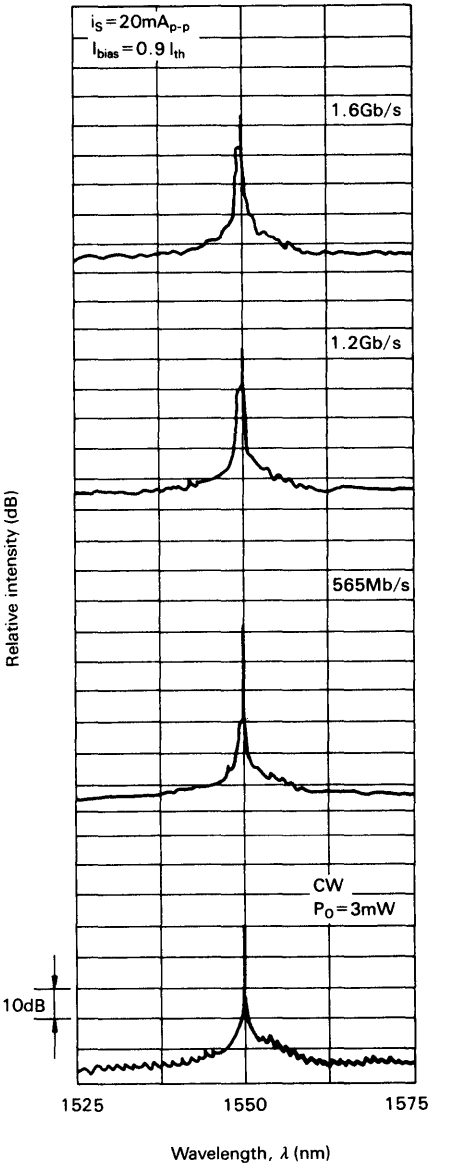


6

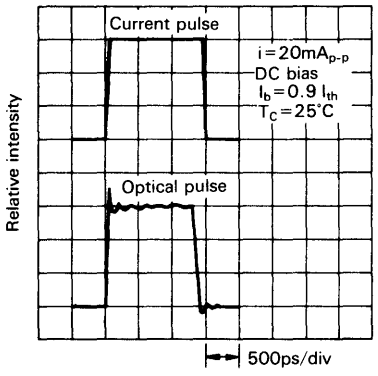
Output Power Dependence of Lasing Spectrum



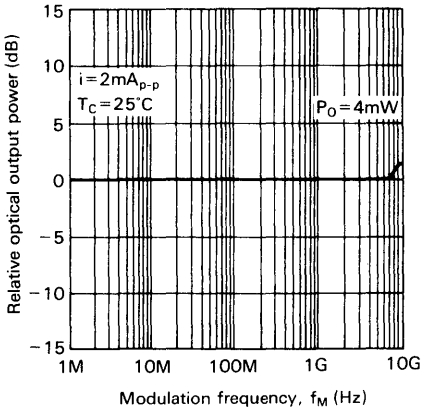
Frequency Dependence of Lasing Spectrum



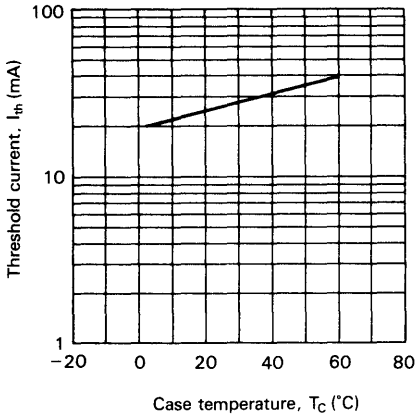
Pulse Response of Laser Diode



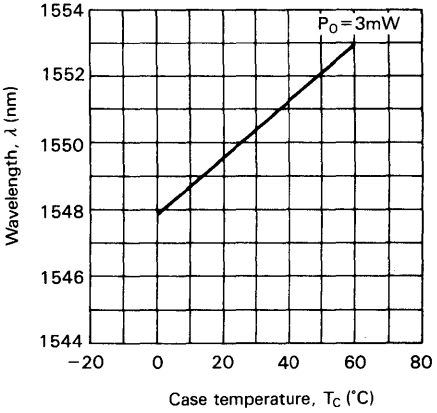
Frequency Response of Laser Diode



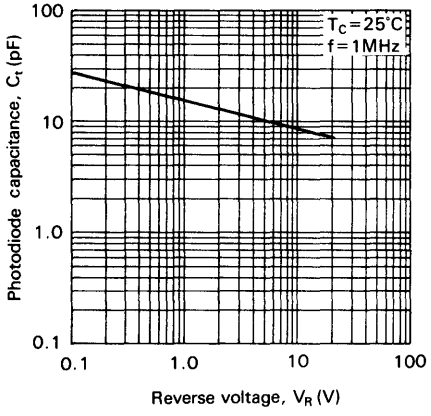
Threshold Current vs. Case Temperature



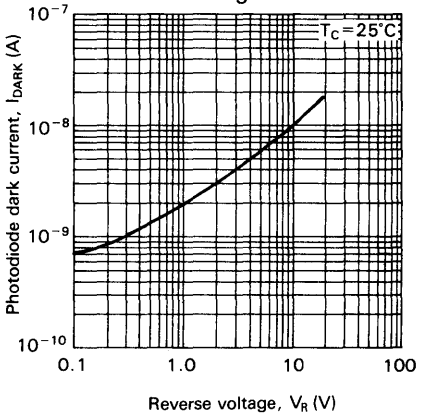
Temperature Dependence of Lasing Wavelength



Photodiode Capacitance vs. Reverse Voltage

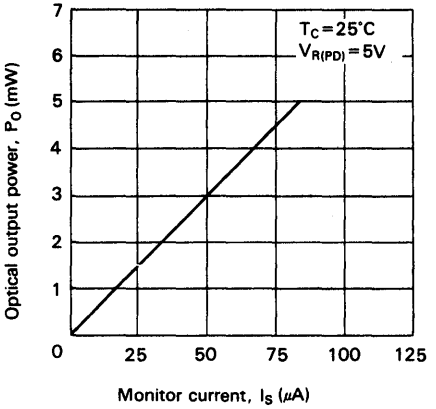


Photodiode Dark Current vs. Reverse Voltage



6

Optical Output Power vs.
Monitor Current



HL1541BF

Laser Diode

Description

HL1541BF is a DFB laser diode module in a 14-pin butterfly-type package with a built-in thermoelectronic controller and connected single mode fiber.

It is suitable as a light source in high-speed modulated, high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

Mode field diameter	: 10.0 ± 1.0 μm
Cutoff wavelength	: 1.10—1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

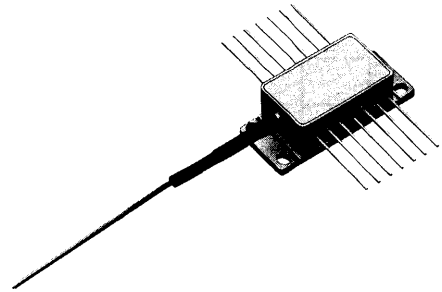
Features

- Long wavelength light output: λ_p = 1530—1570 nm
- 1.0 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- High-speed modulation (1.8 Gb/s)
- Stabilized operation with built-in thermoelectronic controller

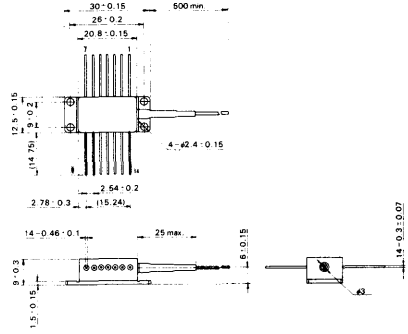
Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.0	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



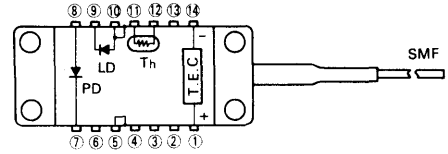
Package Dimensions



(Unit: mm)

BF-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

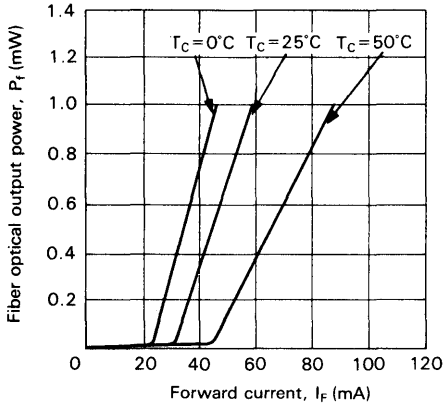
① T. E. C. anode	⑧ PD anode
② N. C.	⑨ LD cathode
③ N. C.	⑩ LD anode (case)
④ N. C.	⑪ Thermistor
⑤ Case	⑫ Thermistor
⑥ N. C.	⑬ N. C.
⑦ PD cathode	⑭ T. E. C. cathode

6

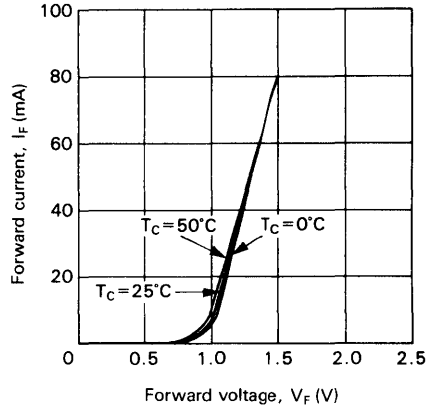
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.0			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r	30	35		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.3			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	T_C = 60°C, P_f = 0.5 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

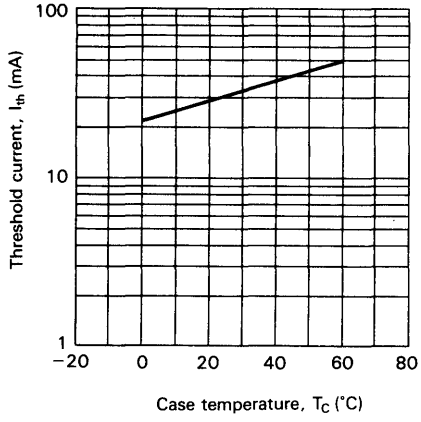
Optical Output Power vs. Forward Current



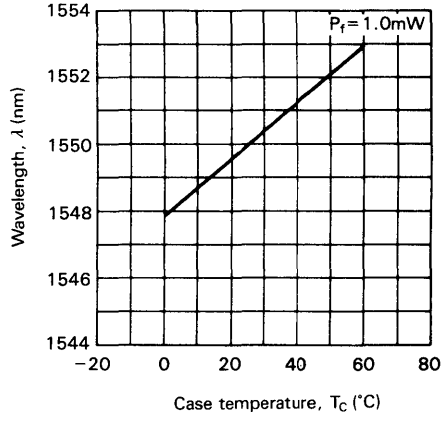
Forward Current vs. Forward Voltage



Threshold Current vs. Case Temperature

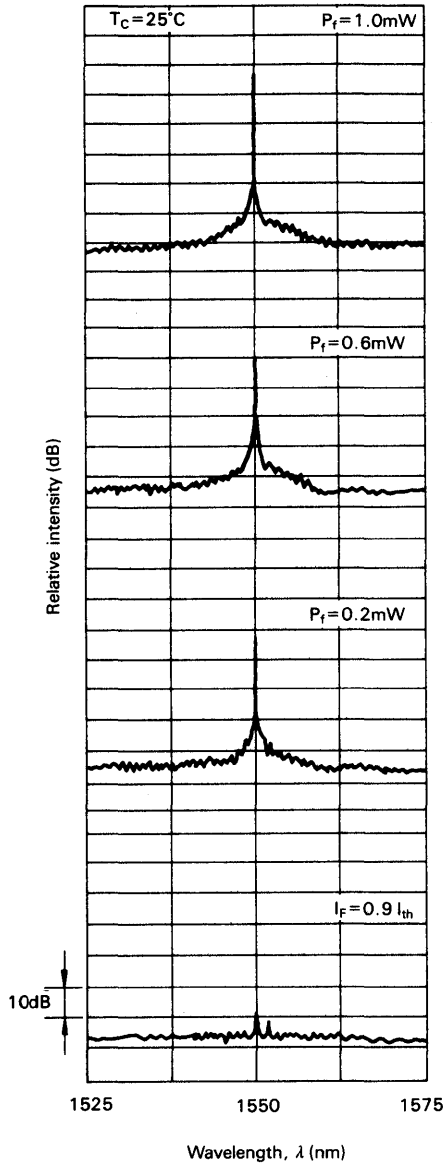


Temperature Dependence of Lasing Wavelength

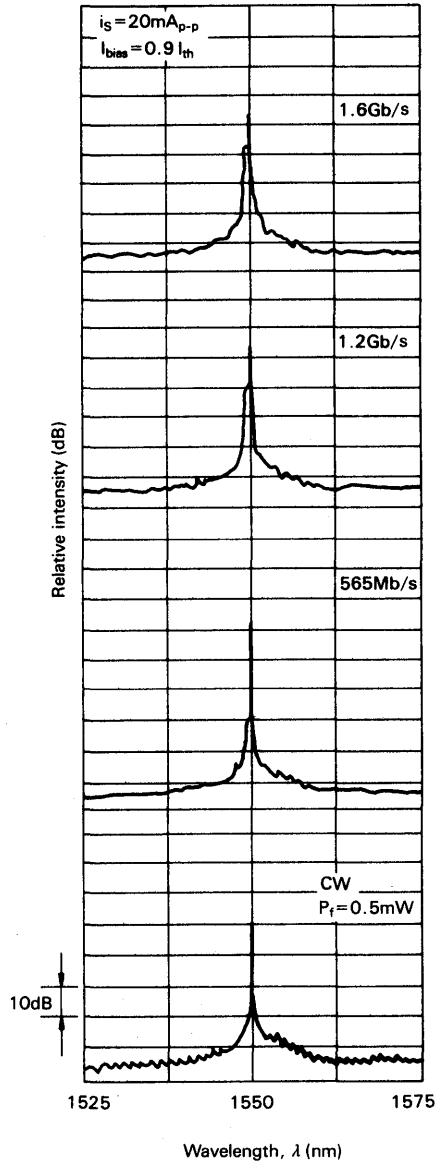


6

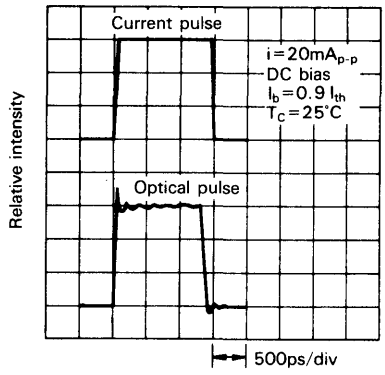
Output Power Dependence of Lasing Spectrum



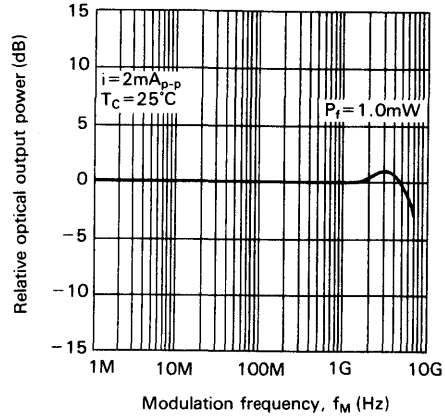
Frequency Dependence of Lasing Spectrum



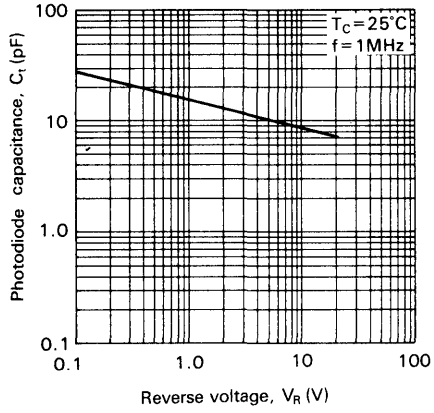
Pulse Response of Laser Diode



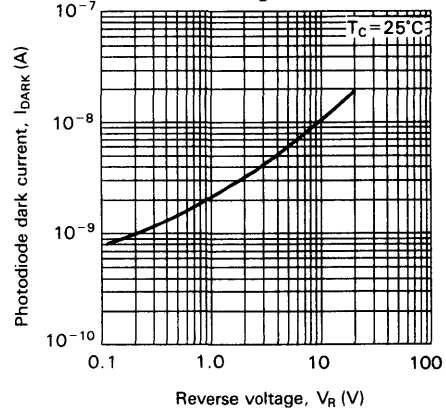
Frequency Response of Laser Diode



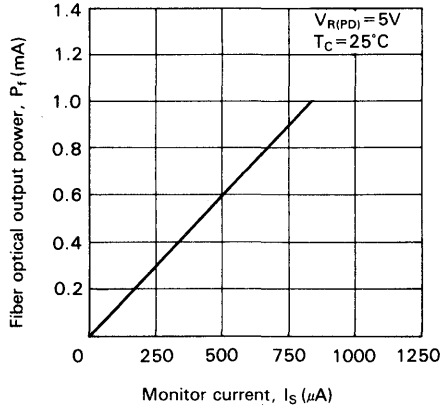
Photodiode Capacitance vs. Reverse Voltage



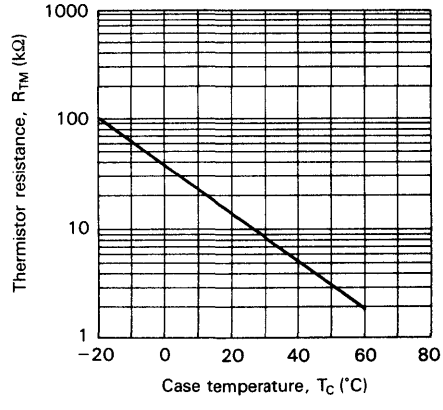
Photodiode Dark Current vs. Reverse Voltage



Optical Output Power vs. Monitor Current

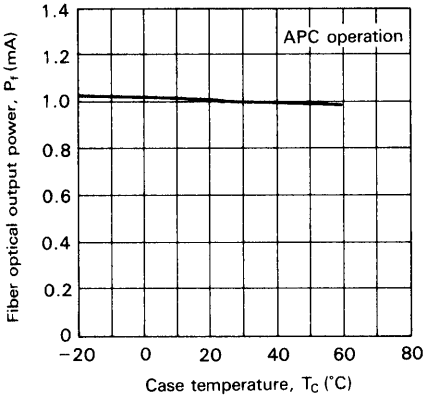


Thermistor Resistance vs. Case Temperature



6

Tracking Characteristics



HL1541DL

Laser Diode

Description

HL1541DL is a DFB laser diode module in a 14-pin dual-in-line type package with a built-in thermoelectronic controller and connected single mode fiber.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

−Fiber specifications−

Mode field diameter	:	10.0 ± 1.0 μm
Cutoff wavelength	:	1.10−1.20 μm
Core diameter	:	10 μm
Outer diameter	:	125 μm
Jacket diameter	:	900 μm
Fiber length	:	More than 500 mm

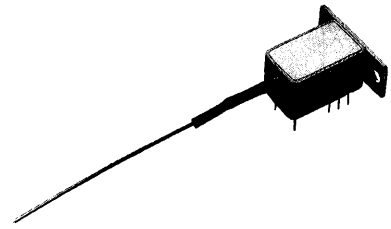
Features

- Long wavelength light output: λ_p = 1530−1570 nm
- 1.0 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- High-speed modulation (800 Mb/s)
- Stabilized operation with built-in thermoelectronic controller

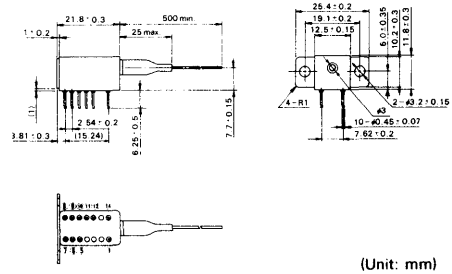
Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.0	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



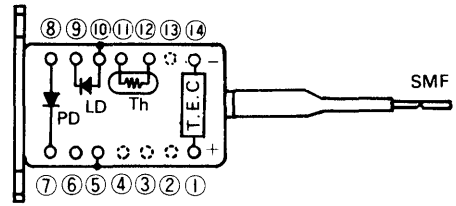
Package Dimensions



(Unit: mm)

DL-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

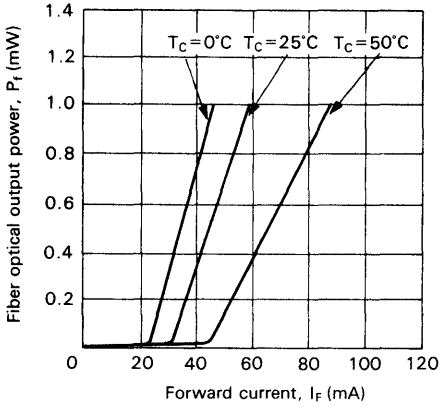
① T. E. C. anode
② —
③ —
④ —
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ —
⑭ T. E. C. cathode

6

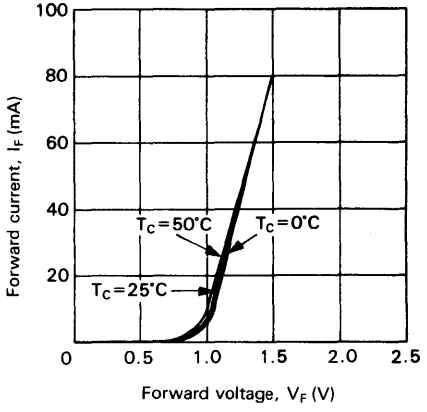
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiberoptical output power	P_f	1.0			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r	30	35		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.3			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	T_C = 60°C, P_f = 0.5 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

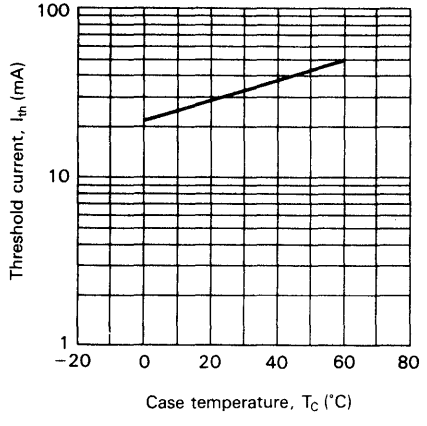
Optical Output Power vs. Forward Current



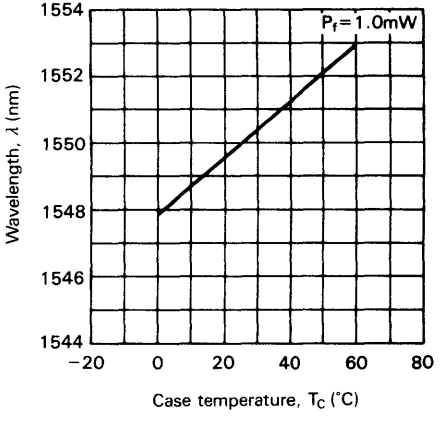
Forward Current vs. Forward Voltage



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



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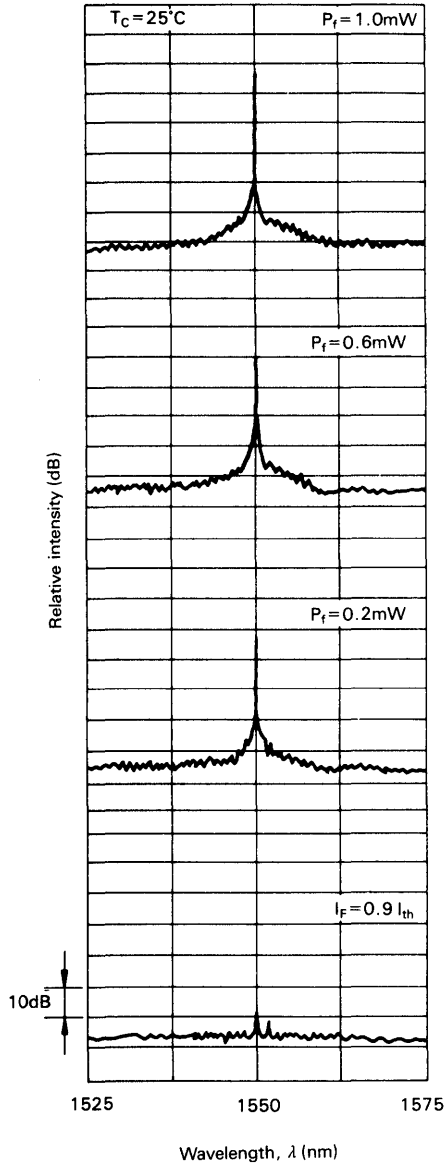
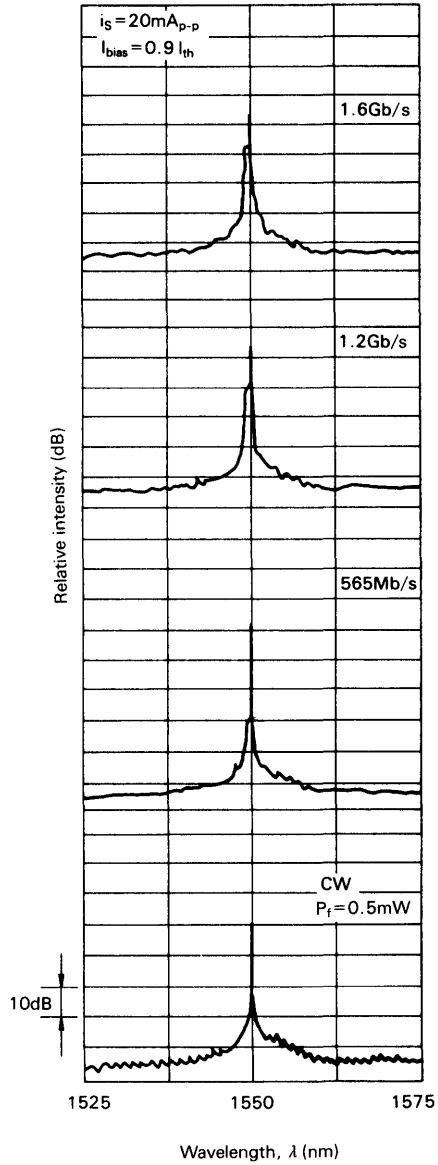
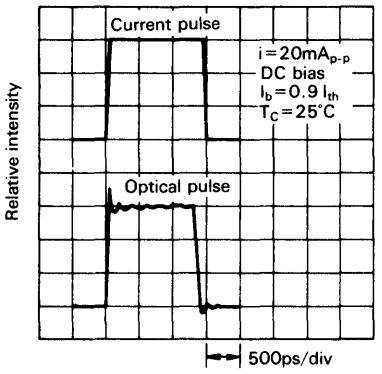
Output Power Dependence of Lasing Spectrum



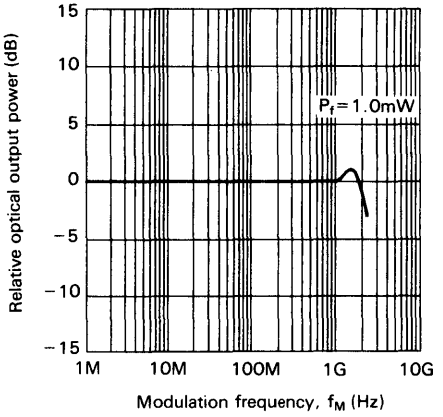
Frequency Dependence of Lasing Spectrum



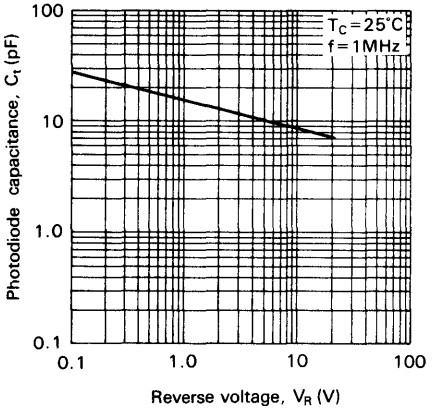
Pulse Response of Laser Diode



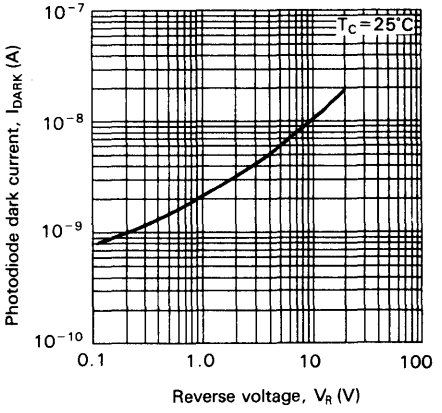
Frequency Response of Laser Diode



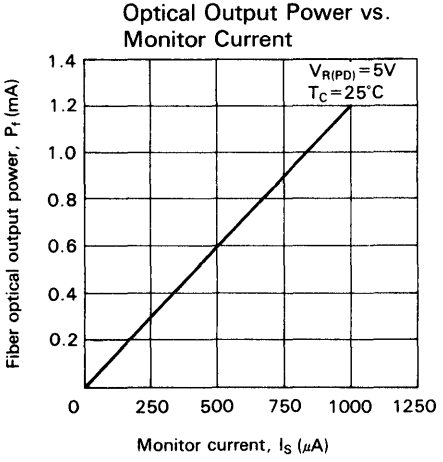
Photodiode Capacitance vs. Reverse Voltage



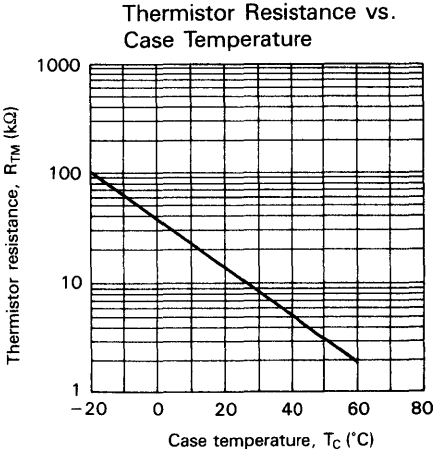
Photodiode Dark Current vs. Reverse Voltage



Optical Output Power vs. Monitor Current

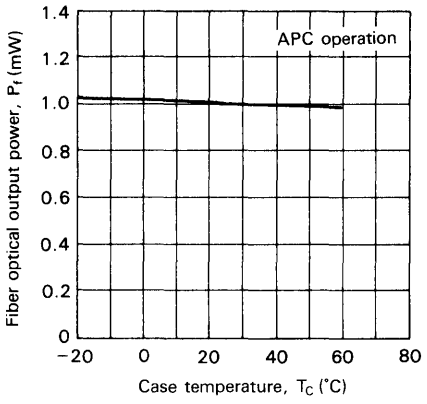


Thermistor Resistance vs. Case Temperature



6

Tracking Characteristics



HL1541DM

Laser Diode

Description

HL1541DM is a 1.55 μm InGaAsP distributed feedback (DFB) laser diode with buried heterostructure.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications equipment.

The laser beam comes out from the connected single-mode fiber; monitoring current by a built-in photodiode.

– Fiber specifications –

Mode field diameter	: 10.0 ± 1.0 μm
Cutoff wavelength	: 1.10–1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

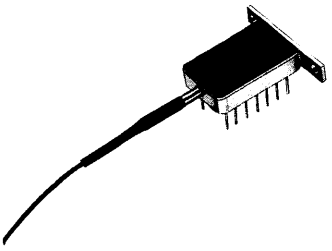
Features

- Long wavelength light output: λ_p = 1530–1570 nm
- 1.2 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode: S_r = 35 dB typ.
- Fast pulse response: t_r = 0.2 ns, t_f = 0.3 ns typ.
- Built-in photodiode for monitoring laser output
- Package with thinner height

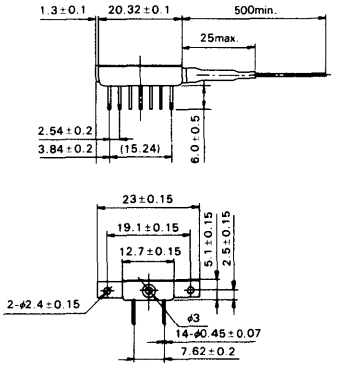
Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.2	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Operating temperature	T_{opr}	0 to +50	°C
Storage temperature	T_{stg}	−40 to +60	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

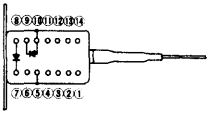


Package Dimensions



DM-type (Unit : mm)

Pin Connection (Bottom view)



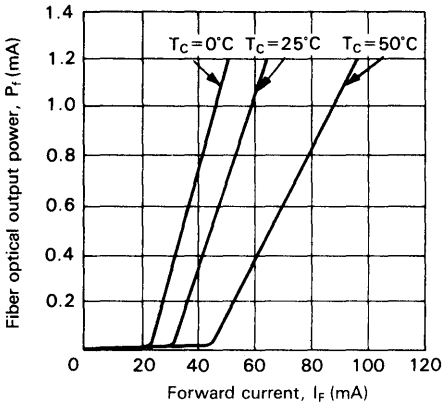
① N.C.
② N.C.
③ N.C.
④ N.C.
⑤ Case
⑥ N.C.
⑦ PD Cathode
⑧ PD Anode
⑨ LD Cathode
⑩ LD Anode (Case)
⑪ N.C.
⑫ N.C.
⑬ N.C.
⑭ N.C.

6

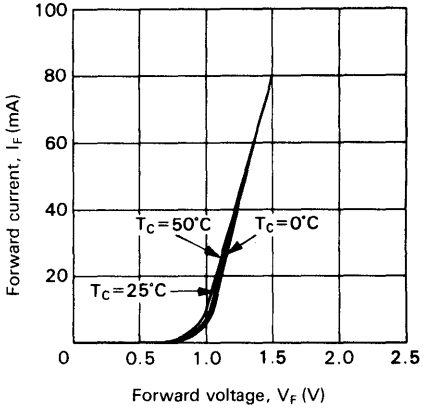
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiber optical output power	P_f	1.2			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r	30	35		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.2		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.3		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			350	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.15			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	

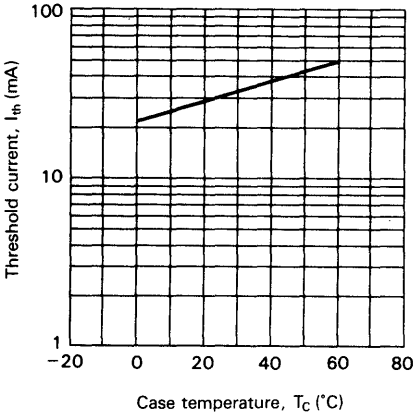
Optical Output Power vs. Forward Current



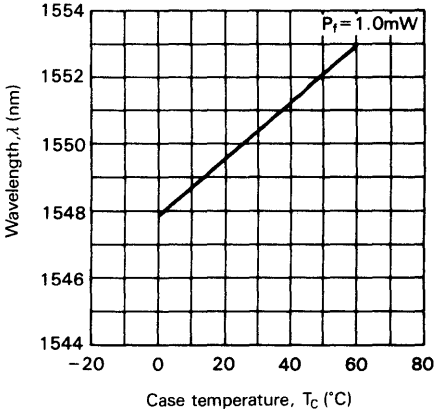
Forward Current vs. Forward Voltage



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



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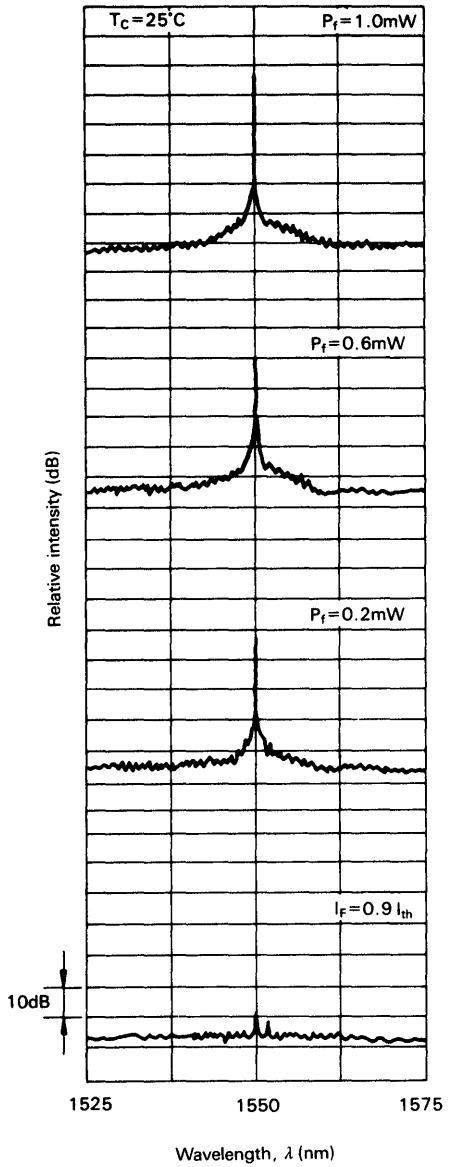
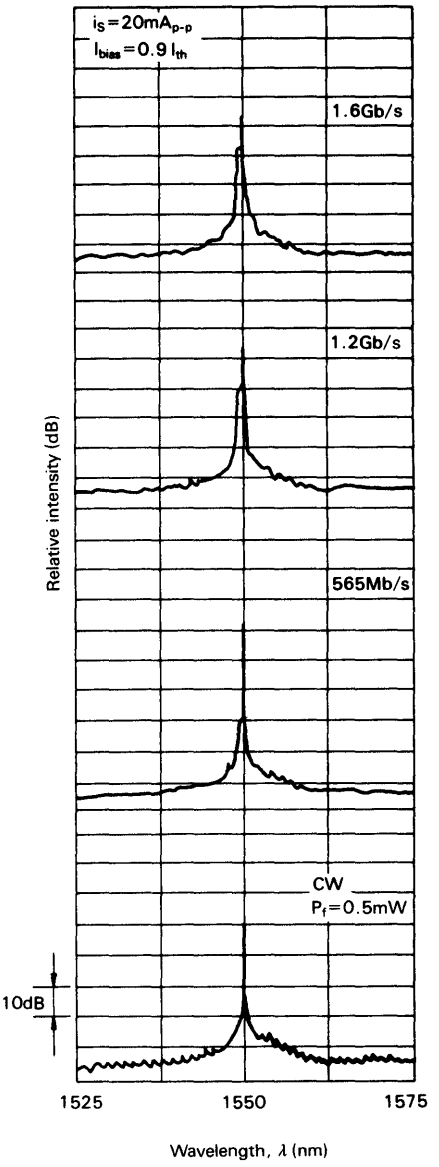
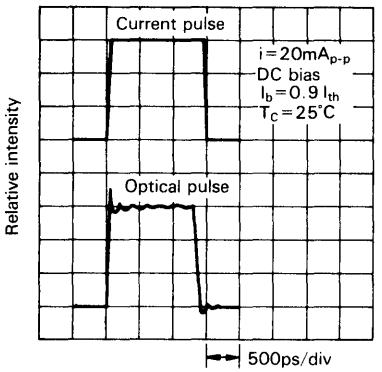
Output Power Dependence of Lasing Spectrum



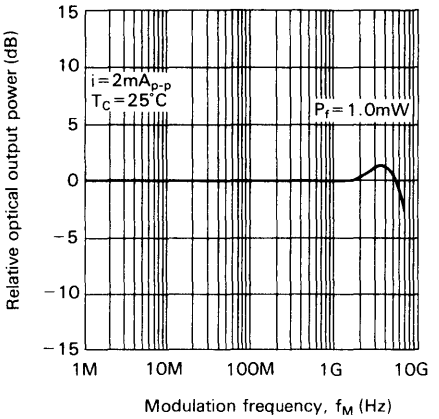
Frequency Dependence of Lasing Spectrum



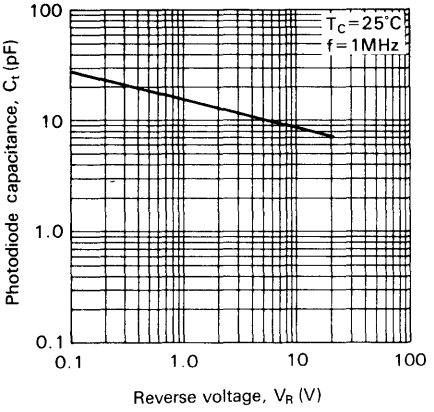
Pulse Response of Laser Diode



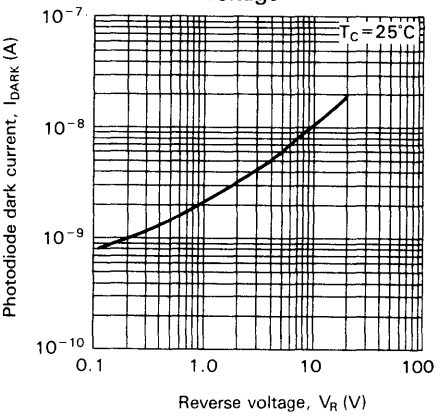
Frequency Response of Laser Diode



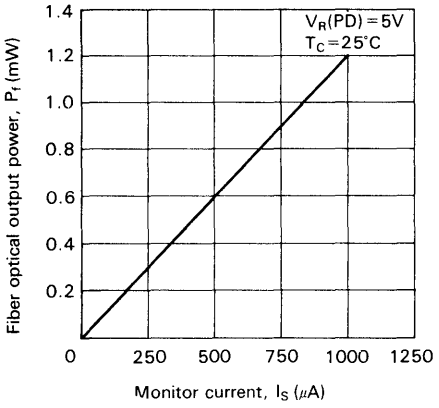
Photodiode Capacitance vs. Reverse Voltage



Photodiode Dark Current vs. Reverse Voltage



Optical Output Power vs. Monitor Current



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HL1561A

Laser Diode

Description

HL1561A is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with $\lambda/4$ phase shifted.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

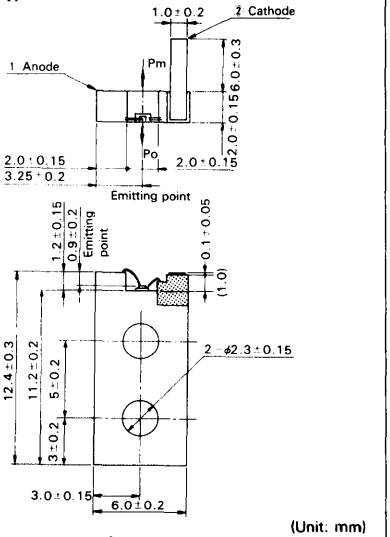
Direct photo-exposure technology is employed to have fine phase-shifted grating.

The package is convenient for system testing because the laser chip is mounted on its stem. This device should be hermetically sealed before mounting on a system.

Features

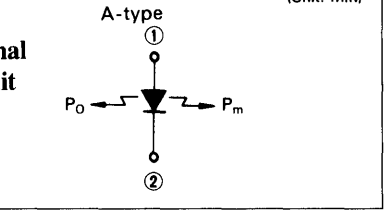
- Long wavelength light output:
  λ_p = 1530–1570 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode:
  S_r = 38 dB typ.
- Fast pulse response: t_r = 0.15 ns, t_f = 0.2 ns typ.
- High-speed modulation (2.4 Gb/s)

Package Dimensions



(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

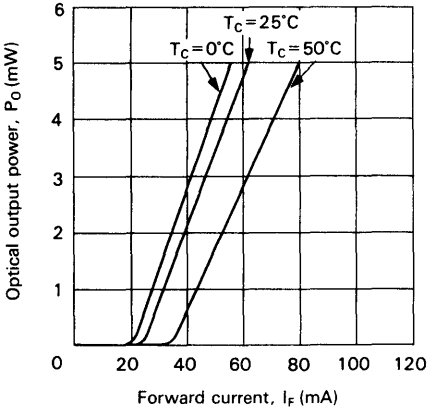
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

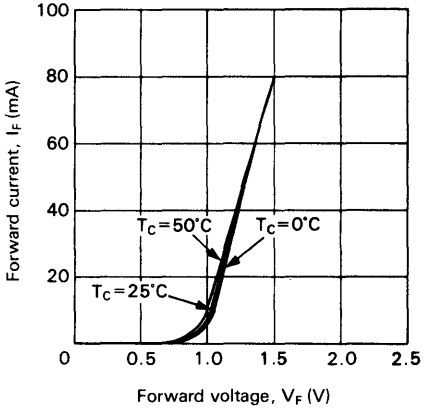
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.6			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	38		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_\perp$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r		0.15		ns	10 to 90%
Fall time	t_f		0.2		ns	90 to 10%

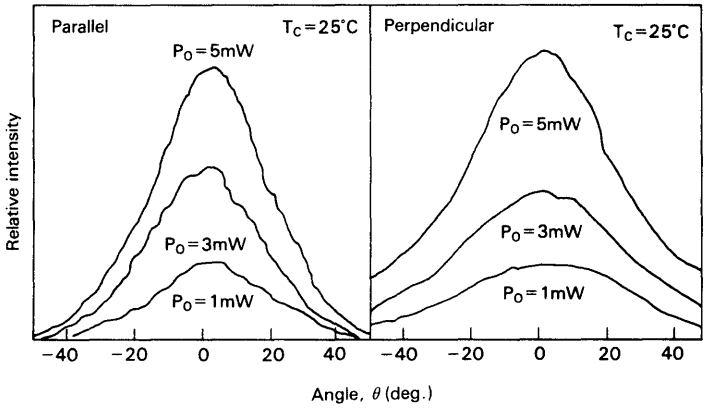
Optical Output Power vs. Forward Current



Forward Current vs. Forward Voltage



Far Field Pattern



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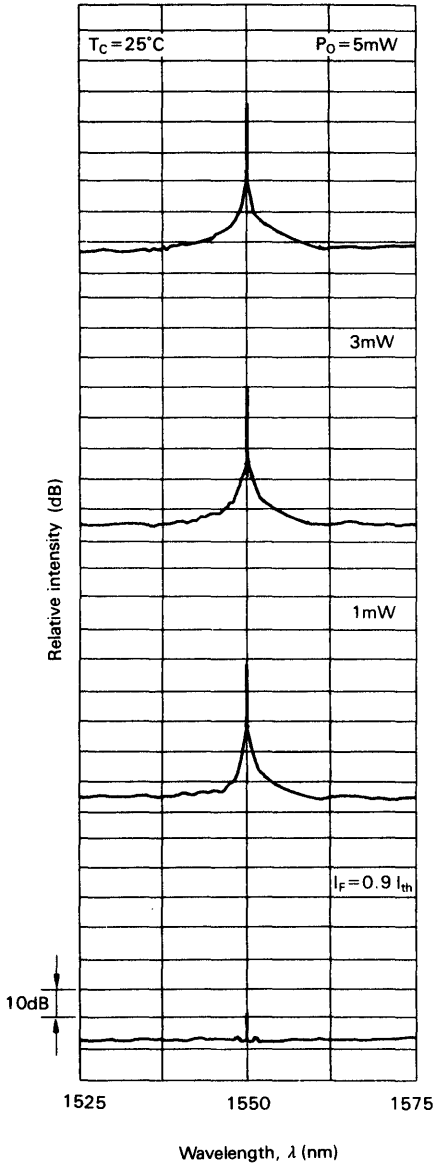
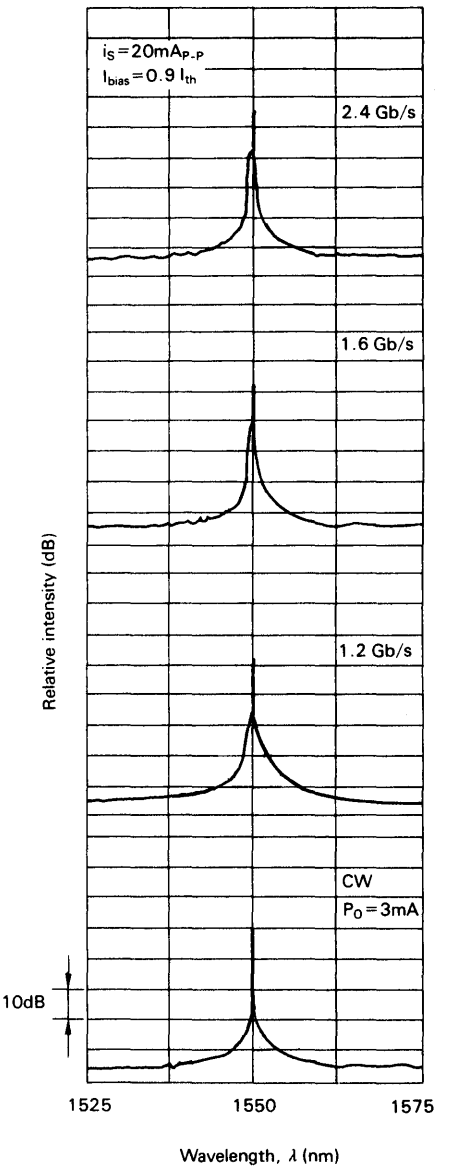
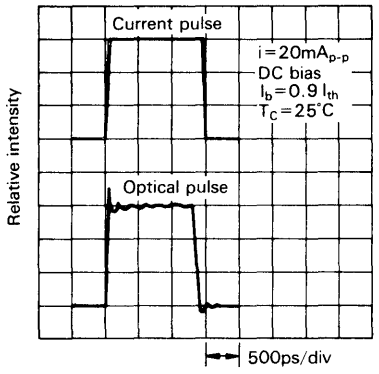
Output Power Dependence of Lasing Spectrum



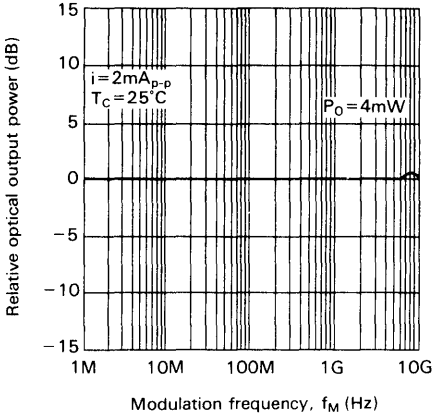
Frequency Dependence of Lasing Spectrum



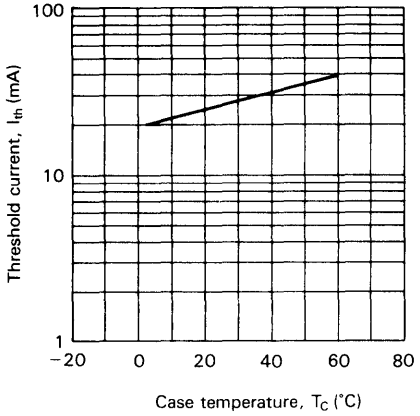
Pulse Response of Laser Diode



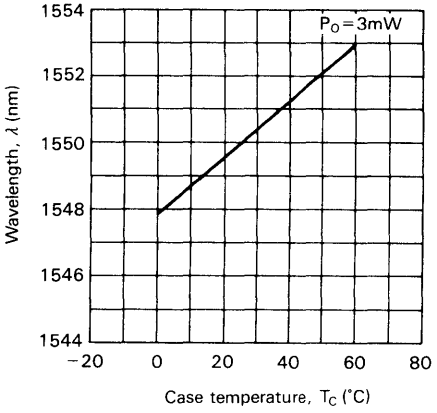
Frequency Response of Laser Diode



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



6

HL1561AC

Laser Diode

Description

HL1561AC is a 1.55 μm InGaAsP distributed-feedback (DFB) laser diode with $\lambda/4$ phase shifted.

It is suitable as a light source in high-bit-rate, long-distance fiberoptic communications and various other types of optical equipment.

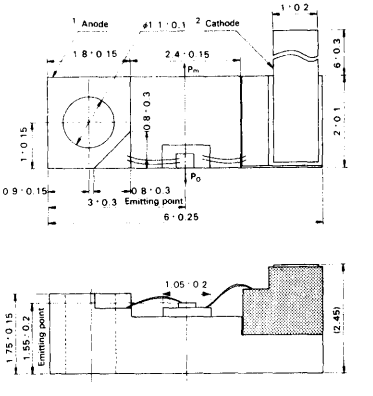
Direct photo-exposure technology is employed to have fine phase-shifted grating.

The package is compact to facilitate module assembly.

Features

- Long wavelength light output: λ_p = 1530–1570 nm
- 5 mW CW operation at room temperature
- Dynamic single longitudinal mode: S_r = 38 dB typ.
- Fast pulse response: t_r = 0.15 ns, t_f = 0.2 ns typ.
- High-speed modulation (2.4 Gb/s)

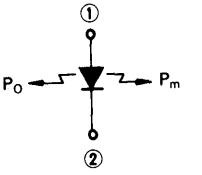
Package Dimensions



(Unit: mm)

AC-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

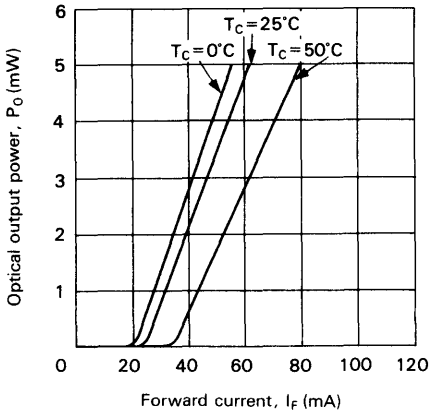
Items	Symbols	Values	Units
Optical output power	P_O	5	mW
Reverse voltage	V_R	2	V
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	0 to +80	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

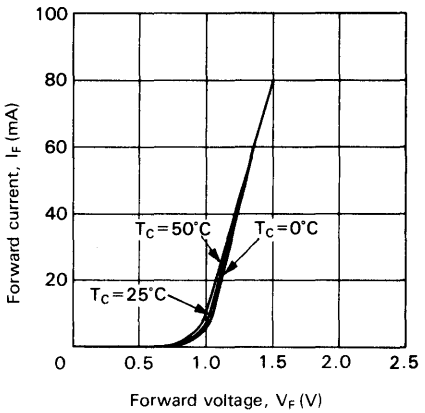
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		25	50	mA	
Optical output power	P_O	5			mW	Kink free
		1.5			mW	$I_F = I_{th} + 20$ mA
Monitor power	P_m	0.6			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1570	1570	nm	P_O = 3 mW
Side-mode suppression ratio	S_r	30	38		dB	P_O = 3 mW
Beam divergence parallel to the junction	$\theta_{//}$		30		deg.	P_O = 3 mW, FWHM
Beam divergence perpendicular to the junction	$\theta_{\perp}$		40		deg.	P_O = 3 mW, FWHM
Rise time	t_r		0.15		ns	10 to 90%
Fall time	t_f		0.2		ns	90 to 10%

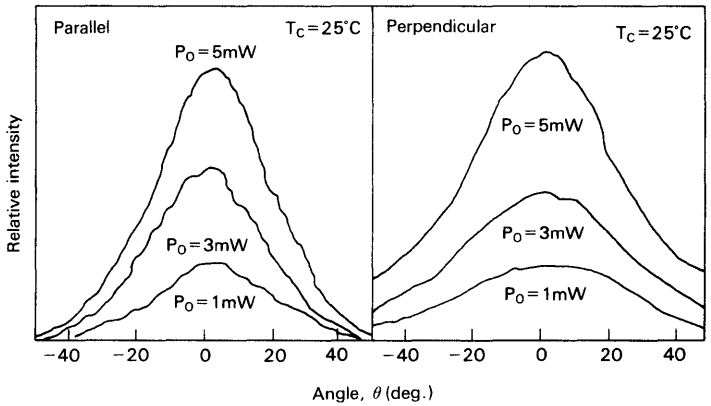
Optical Output Power vs. Forward Current



Forward Current vs. Forward Voltage



Far Field Pattern



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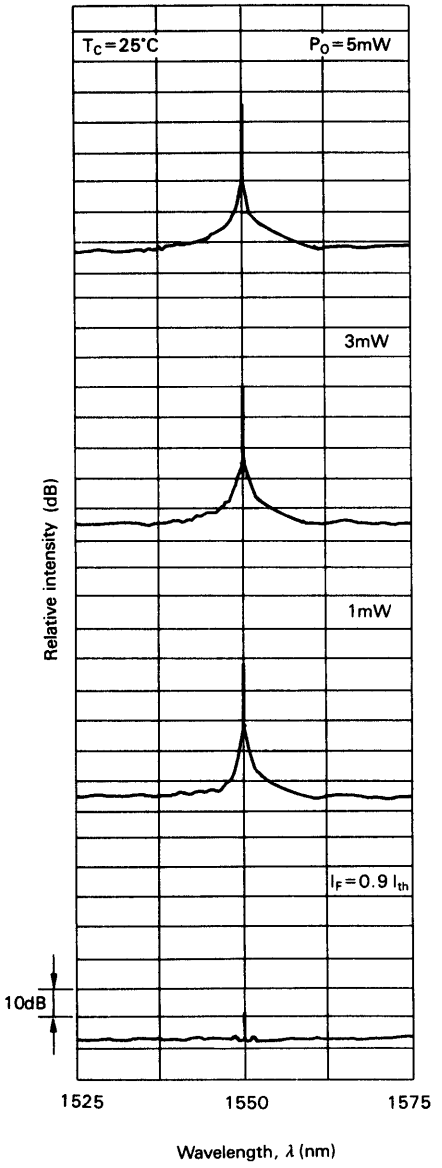
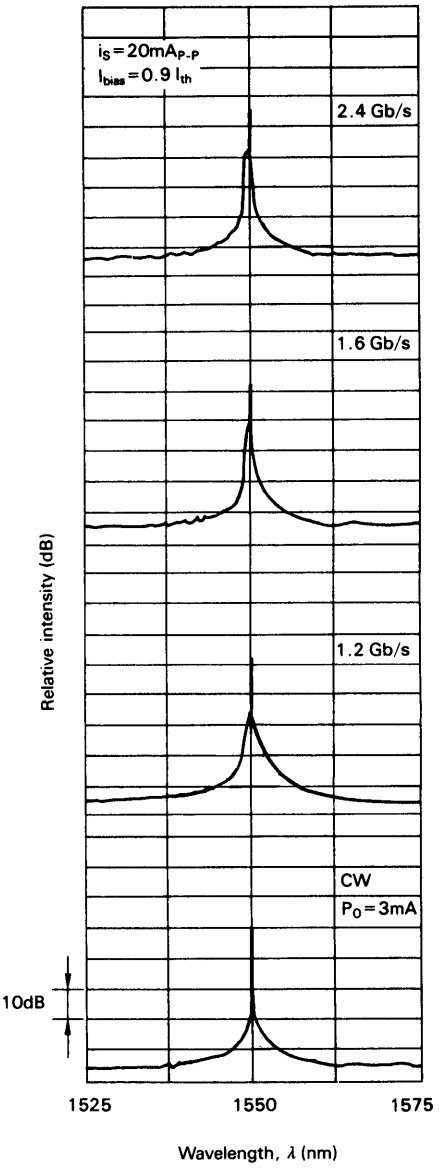
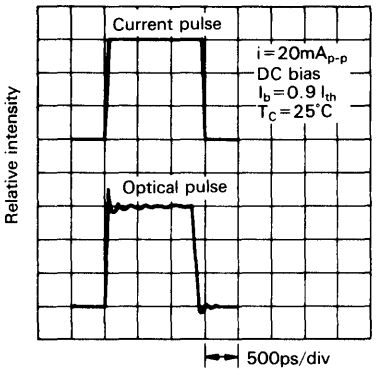
Output Power Dependence of Lasing Spectrum



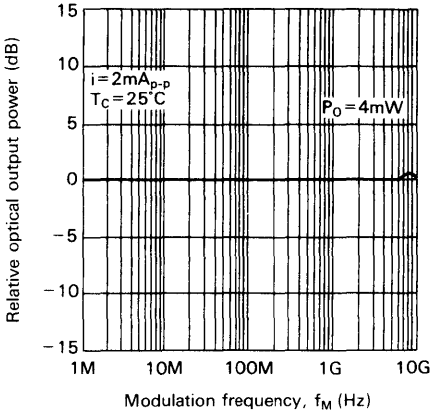
Frequency Dependence of Lasing Spectrum



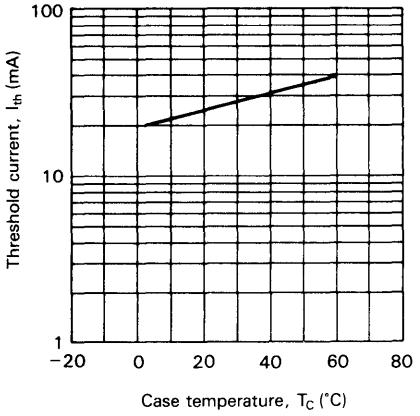
Pulse Response of Laser Diode



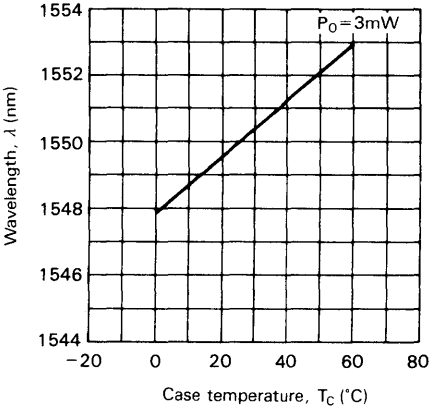
Frequency Response of Laser Diode



Threshold Current vs. Case Temperature



Temperature Dependence of Lasing Wavelength



6

HL1561BF

Laser Diode

Description

HL1561BF is a λ/4 phase shifted DFB laser diode module in a 14-pin butterfly-type package with a built-in thermoelectronic controller and connected single mode fiber.

It is suitable as a light source in high-speed modulated, high-bit-rate, long-distance fiberoptic communications equipment.

The built-in thermoelectronic controller functions to keep the laser chip operation at a constant temperature.

—Fiber specifications—

Mode field diameter	: 10.0 ± 1.0 μm
Cutoff wavelength	: 1.10—1.20 μm
Core diameter	: 10 μm
Outer diameter	: 125 μm
Jacket diameter	: 900 μm
Fiber length	: More than 500 mm

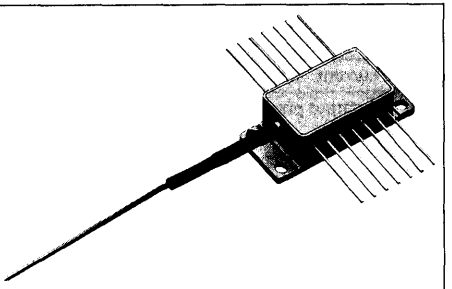
Features

- Long wavelength light output: λ_p = 1530—1570 nm
- 1.0 mW CW and pulse operation at room temperature
- Dynamic single longitudinal mode: S_r = 38 dB typ.
- High-speed modulation (2.4 Gb/s)
- Stabilized operation with built-in thermoelectronic controller

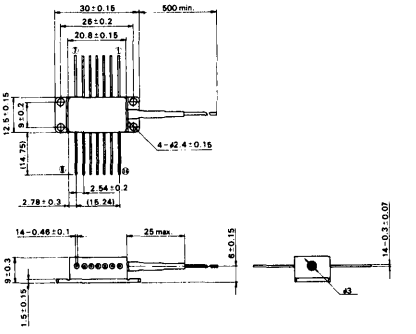
Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Fiber optical output power	P_f	1.0	mW
Laser diode reverse voltage	$V_{R(LD)}$	2	V
Photodiode reverse voltage	$V_{R(PD)}$	15	V
Photodiode forward current	$I_{F(PD)}$	1	mA
Cooler current	I_C	1.4	A
Operating temperature	T_{opr}	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



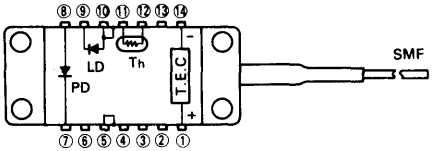
Package Dimensions



(Unit: mm)

BF-type

Pin Connection (Bottom view)



LD; Laser diode
PD; Photodiode
Th; Thermistor
T. E. C. ; T. E. cooler
SMF; Single-mode fiber

① T. E. C. anode
② N. C.
③ N. C.
④ N. C.
⑤ Case
⑥ N. C.
⑦ PD cathode
⑧ PD anode
⑨ LD cathode
⑩ LD anode (case)
⑪ Thermistor
⑫ Thermistor
⑬ N. C.
⑭ T. E. C. cathode

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Threshold current	I_{th}		30	50	mA	
Fiberoptical output power	P_f	1.0			mW	Kink free
		0.3			mW	$I_F = I_{th} + 20$ mA
Lasing wavelength	λ_p	1530	1550	1570	nm	P_f = 0.5 mW
Side-mode suppression ratio	S_r	30	38		dB	P_f = 0.5 mW, CW
Rise time	t_r		0.15		ns	$I_{bias} = I_{th}$, 10 to 90%
Fall time	t_f		0.2		ns	$I_{bias} = I_{th}$, 90 to 10%
Photodiode dark current	I_{DARK}			150	nA	$V_{R(PD)}$ = 5 V
Monitor current	I_S	0.3			mA	$V_{R(PD)}$ = 5 V, P_f = 0.5 mW
Photodiode capacitance	C_t		10	20	pF	$V_{R(PD)}$ = 5 V, f = 1 MHz
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Cooling capacity	ΔT	40			°C	T_C = 60°C, P_f = 0.5 mW
Cooler current	I_C			1.4	A	ΔT = 40°C
Cooler voltage	V_C			1.8	V	ΔT = 40°C
Thermistor resistance	R_{TM}		10		kΩ	

6

Infrared Emitting Diodes

HLP20R, HLP30R, HLP40R

Infrared Emitting Diodes (IRED)

Description

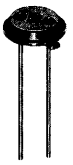
HLP20R, HLP30R and HLP40R are GaAlAs infrared emitting diodes with single heterojunction structure.

They offer a wide range of wavelength and output power, and are suitable for various types of optical equipment.

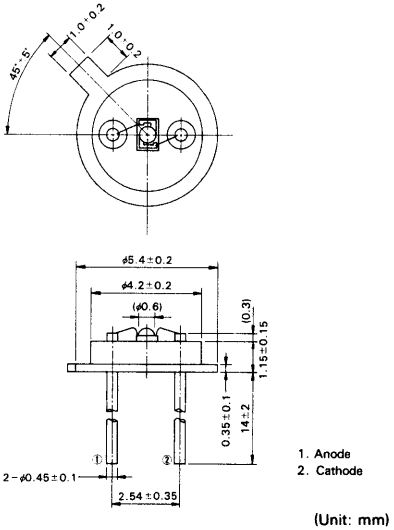
The package should be hermetically sealed before mounting on a system.

Features

- High efficiency
- Selection from a wide range of wavelength and output power
- Narrow spectral width



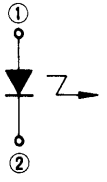
Package Dimensions



(Unit: mm)

R-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25°C$)

Items	Symbols	Values	Units
Forward current	I_F	250	mA
		230*	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	600	mW
Operating temperature	T_{opr}	−20 to +40**	°C
Storage temperature	T_{stg}	−40 to +60**	°C

* Value for devices with λ_p from 735 nm to 785 nm.
** Value for conditions without condensation.

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

6

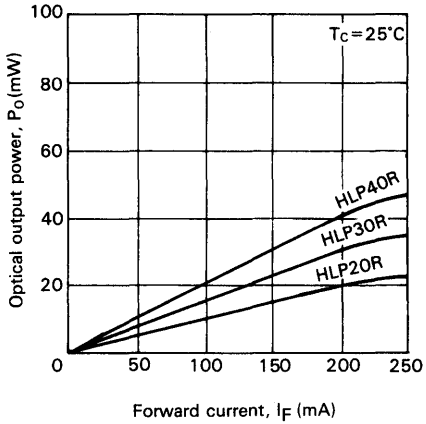
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O		**		mW	I_F = 200 mA
Peak wavelength	λ_p		**		nm	I_F = 200 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 200 mA
Beam divergence	θ_H		180		deg.	I_F = 200 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 200 mA
			2.0*	2.6*	V	I_F = 200 mA
Reverse current	I_R			30	μA	V_R = 3 V
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA
Fall time	t_f		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA

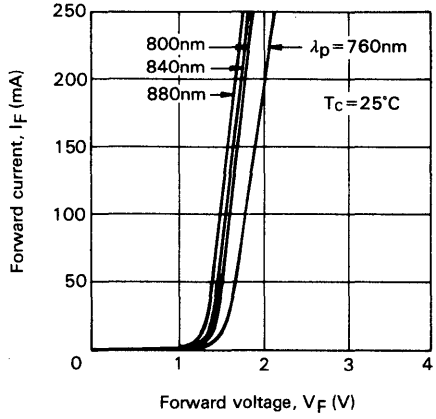
* Value for devices with λ_p from 735 nm to 785 nm.
** HLP20R-HLP40R are grouped with λ_p and P_O as follows.

	λ_p (nm)			P_O (mW)		
Grades	min.	typ.	max.	15 (min.)	25 (min.)	35 (min.)
A	735	760	785	HLP20R	HLP30R	
B	775	800	825		HLP30R	HLP40R
C	815	840	865		HLP30R	HLP40R
D	855	880	905		HLP30R	HLP40R

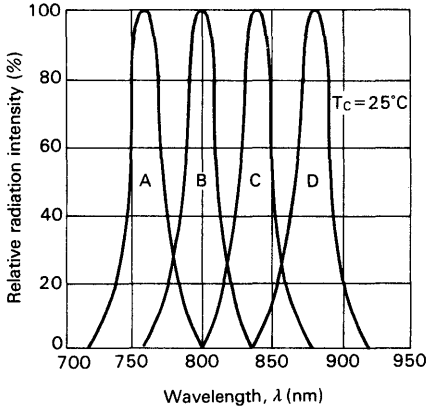
Optical Output Power vs. Forward Current



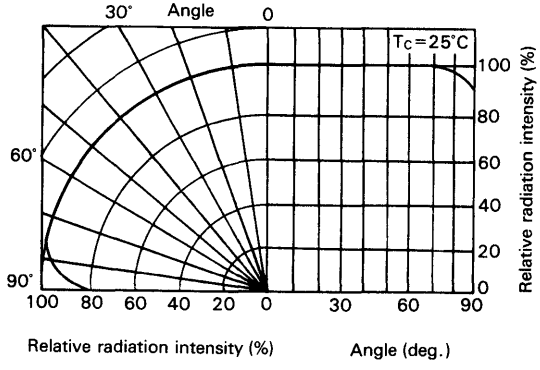
Forward Current vs. Forward Voltage



Emission Spectra of Standard Products



Radiation Pattern



6

HLP20RG, HLP30RG, HLP40RG

Infrared Emitting Diodes (IRED)

Description

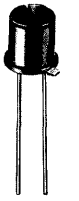
HLP20RG, HLP30RG and HLP40RG are GaAlAs infrared emitting diodes with single heterojunction structure.

They offer a wide range of wavelength and output power, and are suitable for various types of optical equipment.

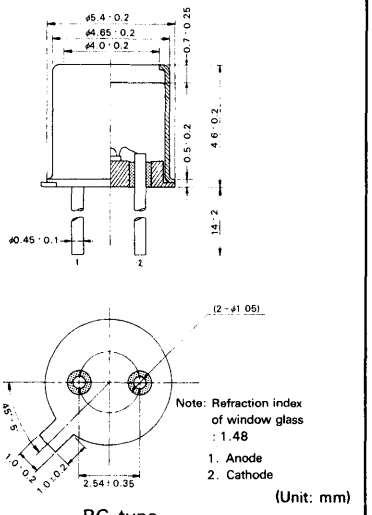
Hermetic sealing of the package achieves high reliability.

Features

- High efficiency
- Selection from a wide range of wavelength and output power
- Narrow spectral width

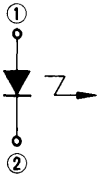


Package Dimensions



RG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	250	mA
		230*	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	600	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +80	°C

* Value for devices with λ_p from 735 nm to 785 nm.

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

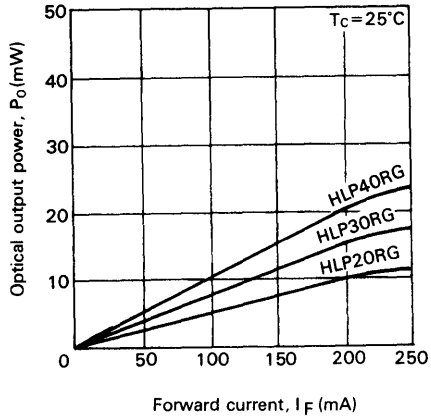
Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O		**		mW	I_F = 200 mA
Peak wavelength	λ_p		**		nm	I_F = 200 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 200 mA
Beam divergence	θ_H		120		deg.	I_F = 200 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 200 mA
			2.0*	2.6*	V	I_F = 200 mA
Reverse current	I_R			30	μA	V_R = 3 V
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA
Fall time	t_f		12		ns	I_F = 50 mA
			20*		ns	I_F = 50 mA

* Value for devices with λ_p from 735 nm to 785 nm.
** HLP20RG-HLP40RG are grouped with λ_p and P_O as follows.

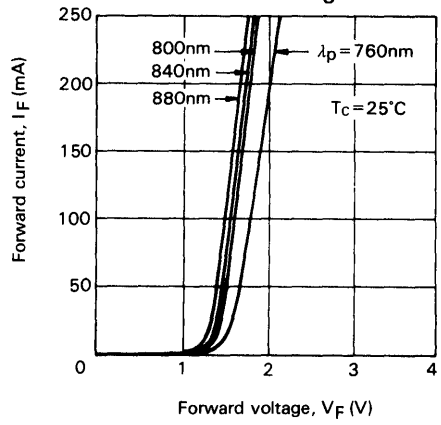
	λ_p (nm)			P_O (mW)		
Grades	**min.**	**typ.**	**max.**	**7 (min.)**	**12 (min.)**	**17 (min.)**
A	735	760	785	HLP20RG	HLP30RG	
B	775	800	825		HLP30RG	HLP40RG
C	815	840	865		HLP30RG	HLP40RG
D	855	880	905		HLP30RG	HLP40RG

6

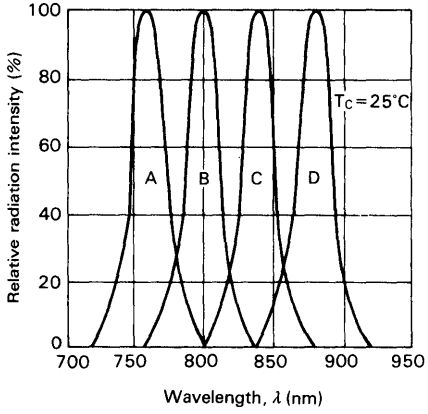
Optical Output Power vs. Forward Current



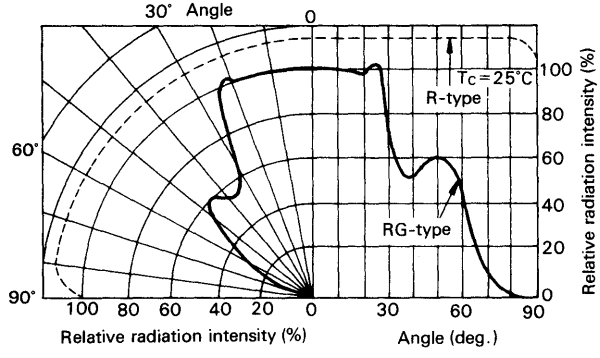
Forward Current vs. Forward Voltage



Emission Spectra of Standard Products



Radiation Pattern



HE7601SG

Infrared Emitting Diodes (IRED)

Description

HE7601SG is a 0.77 μm GaAlAs infrared emitting diode with double heterojunction structure. High brightness output, high power output and high speed response can be obtained.

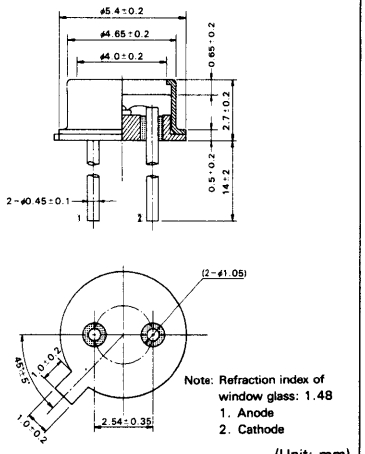
It is suitable as a light source in optical controlling equipment and sensors.

Hermetic sealing of the package achieves high reliability.

Features

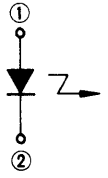
- High power output: $P_O \geqq 30$ mW
- Fast pulse response: $t_r = 5$ns, $t_f = 7$ns typ.

Package Dimensions



SG-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25$°C)

Items	Symbols	Values	Units
Forward current	I_F	250	mA
Reverse voltage	V_R	3	V
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_C = 25$°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	30			mW	I_F = 200 mA
Peak wavelength	λ_p	740	770	800	nm	I_F = 200 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 200 mA
Forward voltage	V_F			2.5	V	I_F = 200 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

HE8403R

Infrared Emitting Diodes (IRED)

Description

HE8403R is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

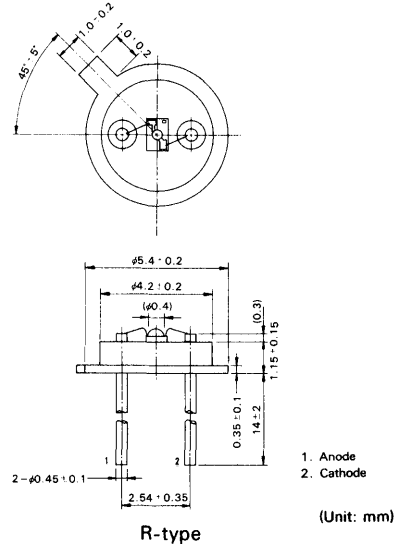
Optical fiber can be close to the chip, achieving high coupling efficiency; suitable as a light source in fiberoptic communications equipment.

The package should be hermetically sealed before mounting on a system.

Features

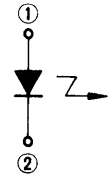
- High efficiency and high brightness output
- High frequency response
- Excellent light-current linearity

Package Dimensions



R-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +40*	°C
Storage temperature	T_{stg}	−40 to +60*	°C

* Value for conditions without condensation.

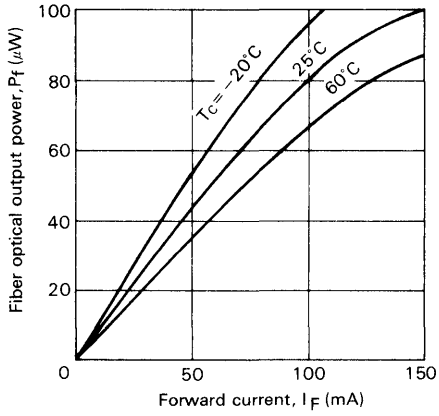
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

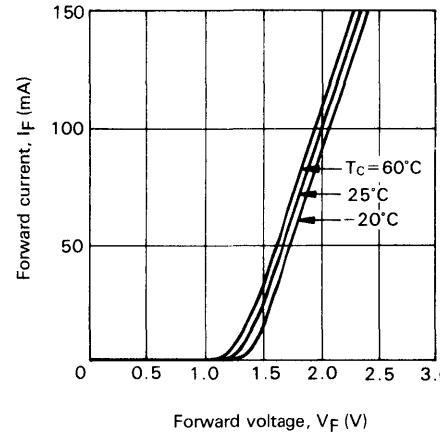
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	50	80		μW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end.

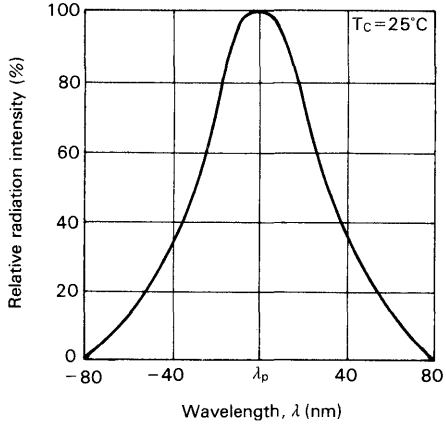
Optical Output Power vs. Forward Current



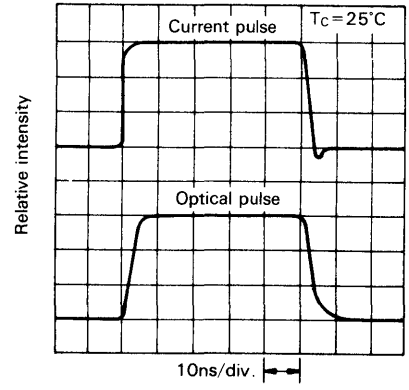
Forward Current vs. Forward Voltage



Spectral Distribution



Pulse Response



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HE8403SG

Infrared Emitting Diodes (IRED)

Description

HE8403SG is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

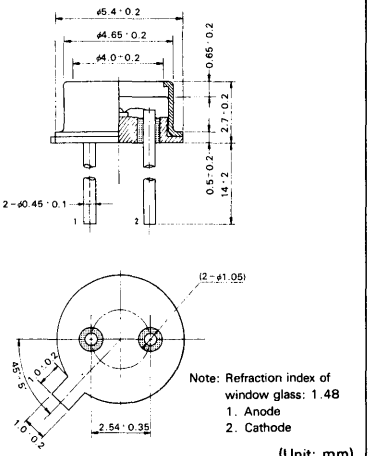
High coupling efficiency can be realized using a rod lens; suitable as a light source in fiberoptic communications equipment.

Hermetic sealing of the package achieves high reliability.

Features

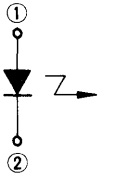
- High efficiency and high brightness output
- High frequency response
- Excellent light-current linearity

Package Dimensions



SG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

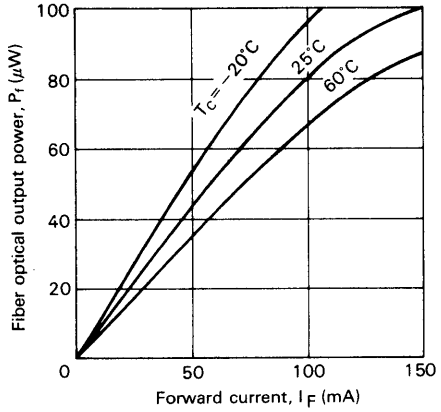
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

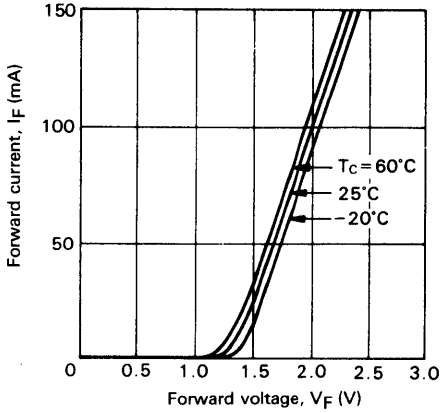
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	40	80		μW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end through rod lens.

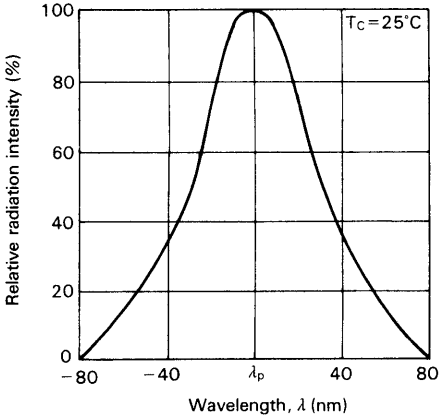
Optical Output Power vs. Forward Current



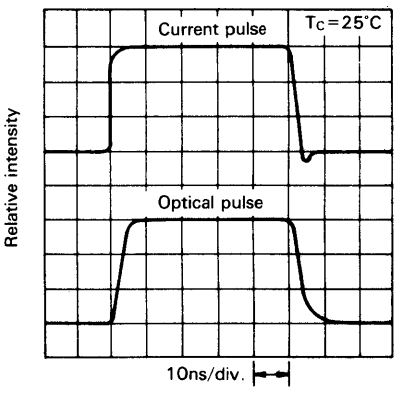
Forward Current vs. Forward Voltage



Spectral Distribution



Pulse Response



6

HE8403ML

Infrared Emitting Diodes (IRED)

Description

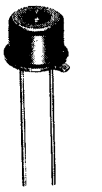
HE8403ML is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

Optical output from the chip is directed to the optical fiber efficiently through the microlens in the cap; suitable as a light source in fiberoptic communications equipment.

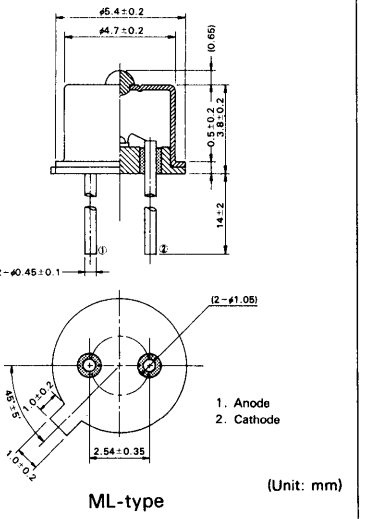
Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high brightness output
- High frequency response
- Excellent light-current linearity



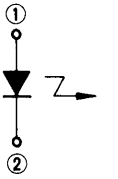
Package Dimensions



(Unit: mm)

ML-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

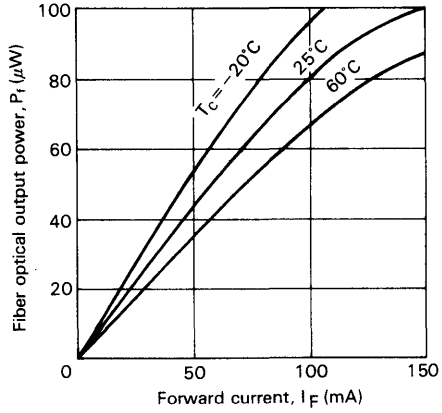
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

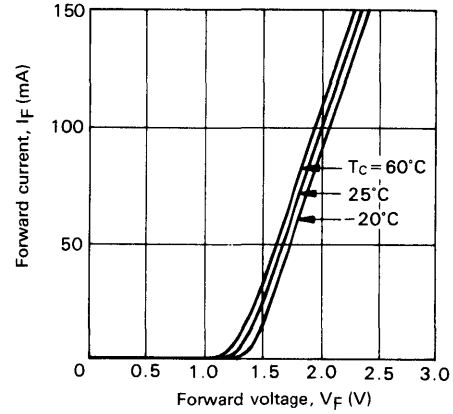
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	50	80		μW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end.

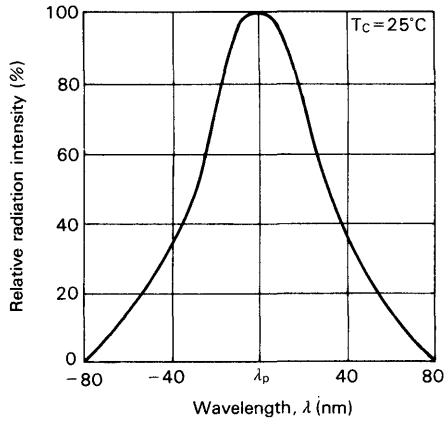
Optical Output Power vs. Forward Current



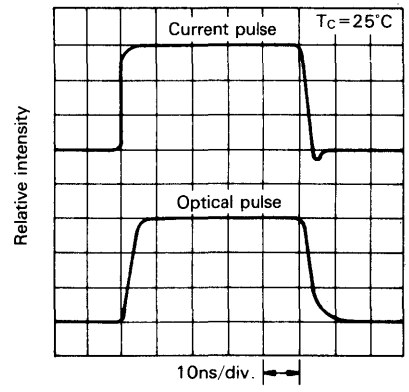
Forward Current vs. Forward Voltage



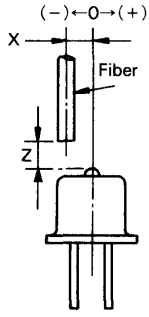
Spectral Distribution

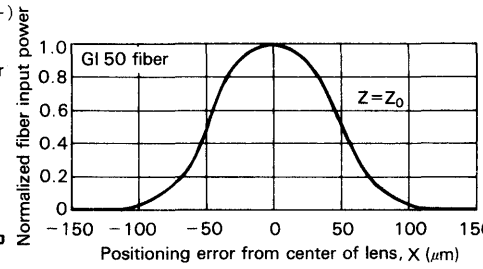


Pulse Response



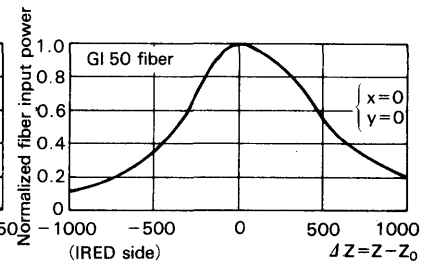
Coupling Characteristics





Fiber input deviation due to lateral fiber positioning error

Z_0: Focal point of lens



Fiber input deviation due to horizontal fiber positioning error

HE8403TR

Infrared Emitting Diodes (IRED)

Description

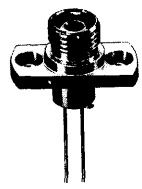
HE8403TR is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure, which provides high speed response.

The package with a receptacle is easily connected with FC-type connector; suitable as a light source in fiberoptic communications equipment.

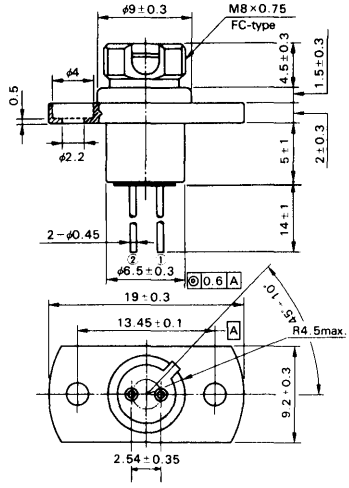
Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high brightness output
- High frequency response
- Wide operating-temperature range: T_{opr} = −20 to +85°C



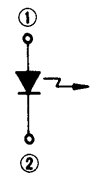
Package Dimensions



1. Anode
2. Cathode

TR-type (Unit : mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +85	°C
Storage temperature	T_{stg}	−40 to +100	°C

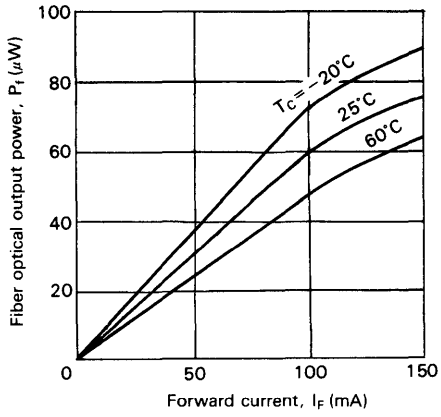
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

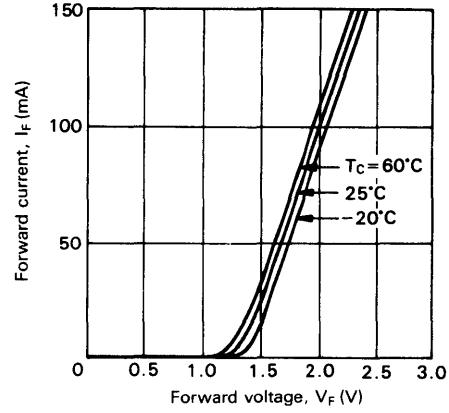
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	40	60		μW	I_F = 100 mA
Peak wavelength	λ_p	800	840	900	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 100 mA
Forward voltage	V_F			2.5	V	I_F = 100 mA
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

* At GI 50/125 fiber end.

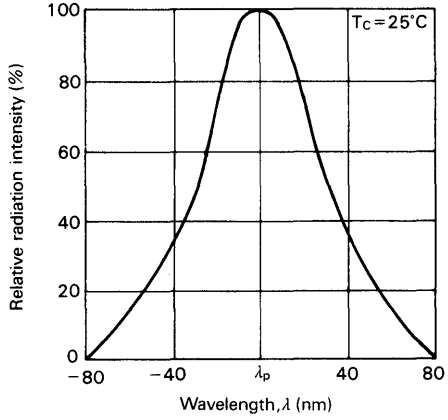
Optical Output Power vs. Forward Current



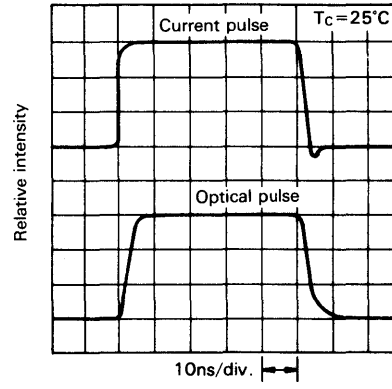
Forward Current vs. Forward Voltage



Spectral Distribution



Pulse Response



6

HE8404SG

Infrared Emitting Diodes (IRED)

Description

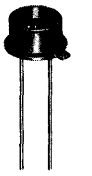
HE8404SG is a 0.82 μm GaAlAs infrared emitting diode with double heterojunction structure. High brightness output, high power output and high speed response can be obtained.

It is suitable as a light source in optical controlling equipment and sensors.

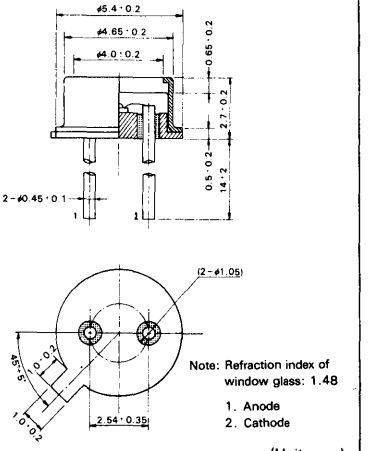
Hermetic sealing of the package achieves high reliability.

Features

- High power output: $P_o \geqq 40$ mW
- Fast pulse response: $t_r = 5$ns, $t_f = 7$ns typ.

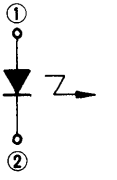


Package Dimensions



SG-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25$°C)

Items	Symbols	Values	Units
Forward current	I_F	250	mA
Reverse voltage	V_R	3	V
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_C = 25$°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	40			mW	$I_F = 200$ mA
Peak wavelength	λ_p	790	820	850	nm	$I_F = 200$ mA
Spectral width	$\Delta\lambda$		50		nm	$I_F = 200$ mA
Forward voltage	V_F			2.5	V	$I_F = 200$ mA
Reverse current	I_R			100	μA	$V_R = 3$ V
Capacitance	C_t		30		pF	$V_R = 0$ V, f = 1 MHz
Rise time	t_r		5		ns	$I_F = 50$ mA
Fall time	t_f		7		ns	$I_F = 50$ mA

HE8805VG

Infrared Emitting Diodes (IRED)

Description

HE8805VG is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

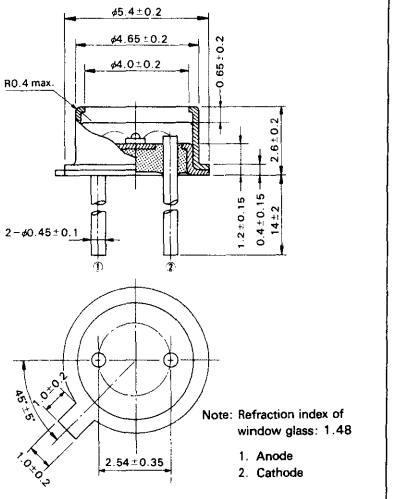
It is suitable as a light source in autofocusing still cameras.

Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high power output
- Narrow spectral width
- Wide radiant directionality

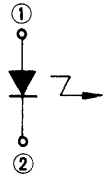
Package Dimensions



VG-type

(Unit: mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

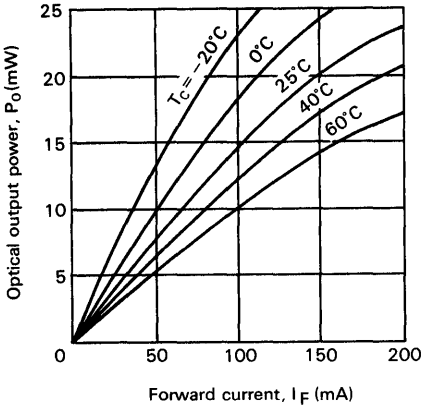
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

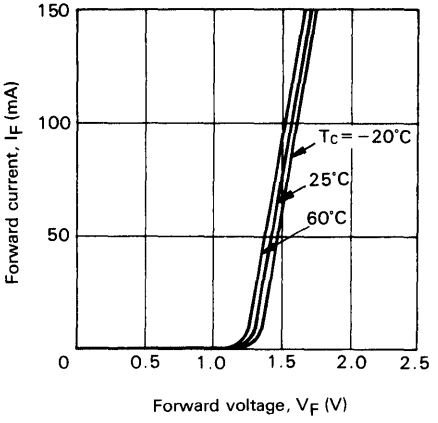
Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	6			mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		20		ns	I_F = 50 mA
Fall time	t_f		20		ns	I_F = 50 mA

6

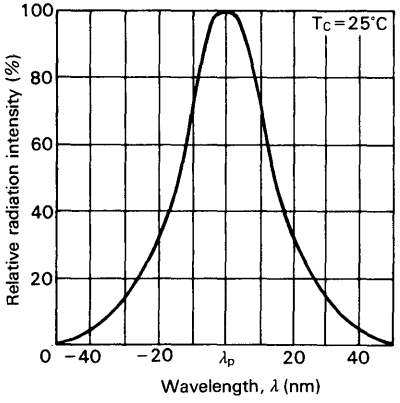
Optical Output Power vs. Forward Current



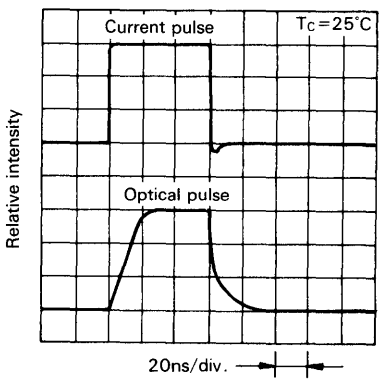
Forward Current vs. Forward Voltage



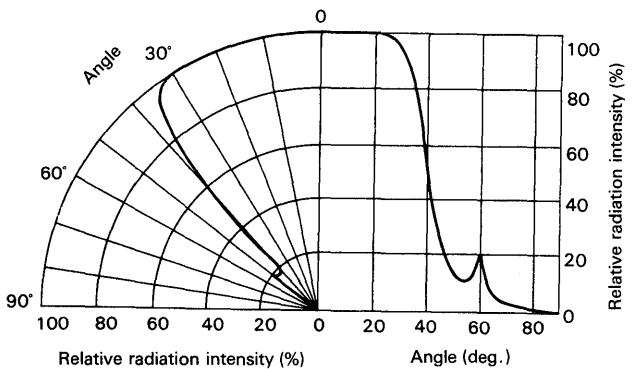
Spectral Distribution



Pulse Response



Radiation Pattern



HE8806VG

Infrared Emitting Diodes (IRED)

Description

HE8806VG is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

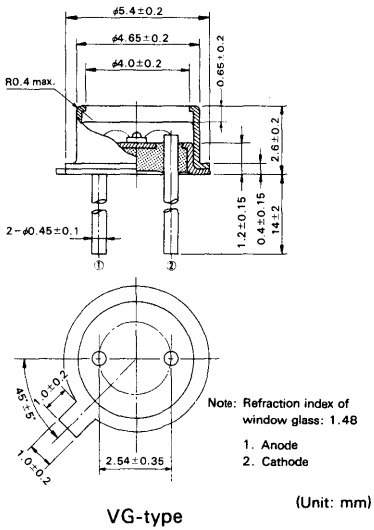
It is suitable as a light source in autofocusing VTR cameras.

Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high power output
- Narrow spectral width
- Wide radiant directionality

Package Dimensions



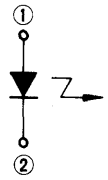
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode

(Unit: mm)

VG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	12			mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		20		ns	I_F = 50 mA
Fall time	t_f		20		ns	I_F = 50 mA

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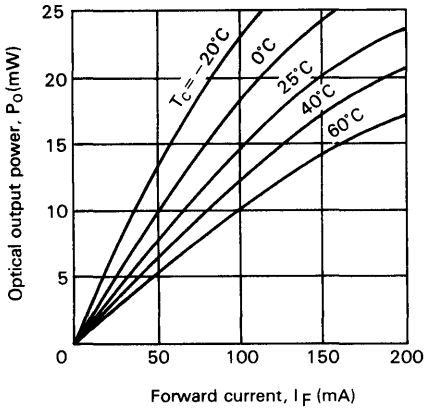
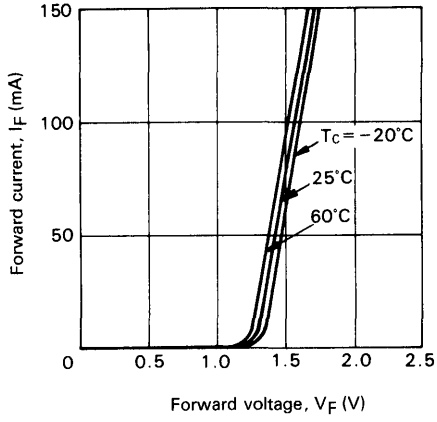
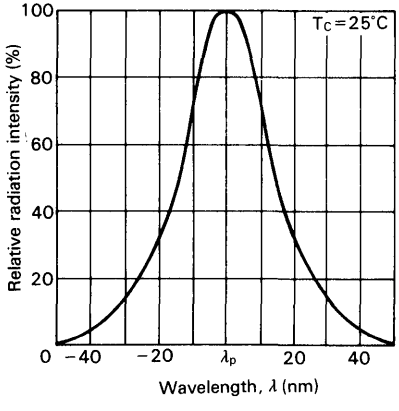
Optical Output Power vs. Forward Current



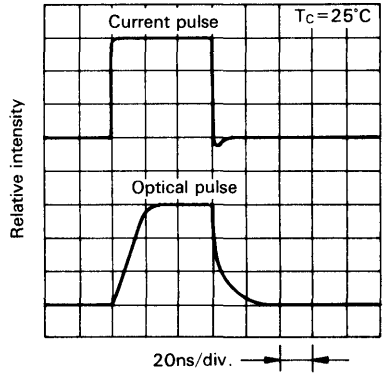
Forward Current vs. Forward Voltage



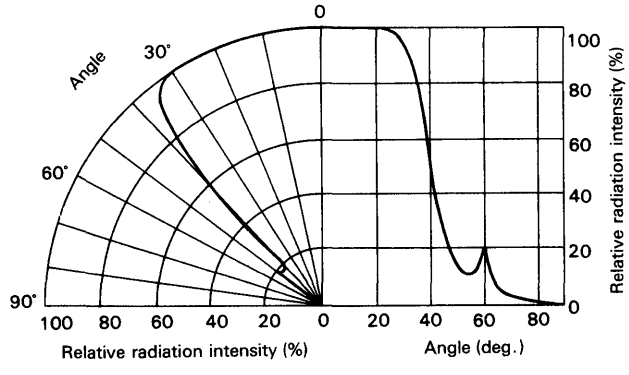
Spectral Distribution



Pulse Response



Radiation Pattern



HE8807SG

Infrared Emitting Diodes (IRED)

Description

HE8807SG is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

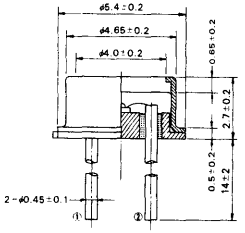
Radiant directionality is wide and radiant intensity is high; suitable as a light source in encoders and sensors.

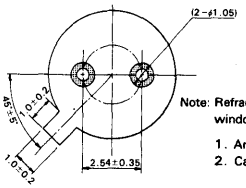
Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high power output
- Narrow spectral width
- Wide radiant directionality
- High reliability

Package Dimensions





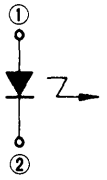
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode

(Unit: mm)

SG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

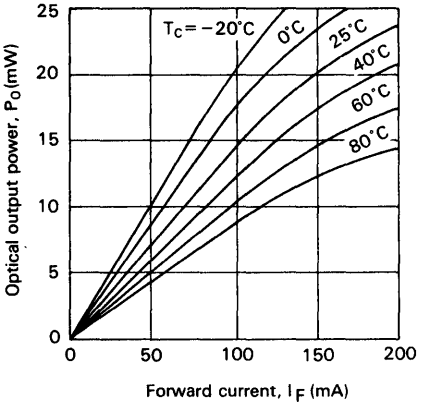
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

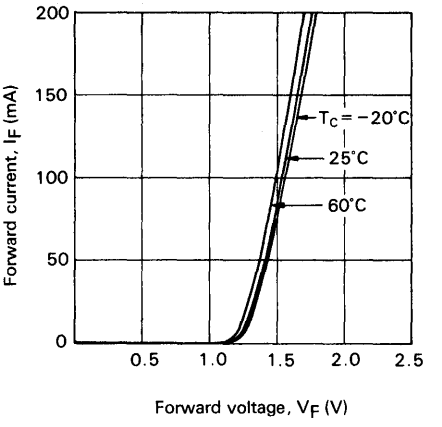
Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	10	20		mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		20		ns	I_F = 50 mA
Fall time	t_f		20		ns	I_F = 50 mA

6

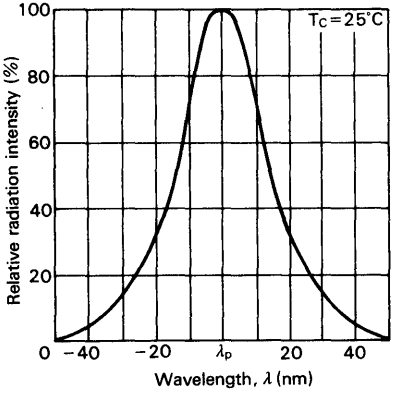
Optical Output Power vs. Forward Current



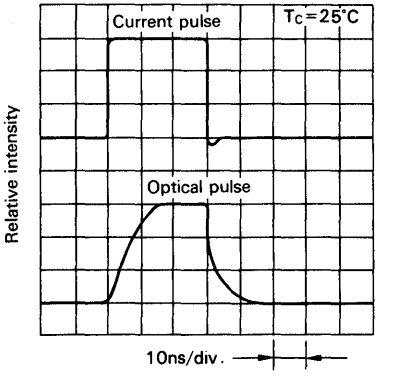
Forward Current vs. Forward Voltage



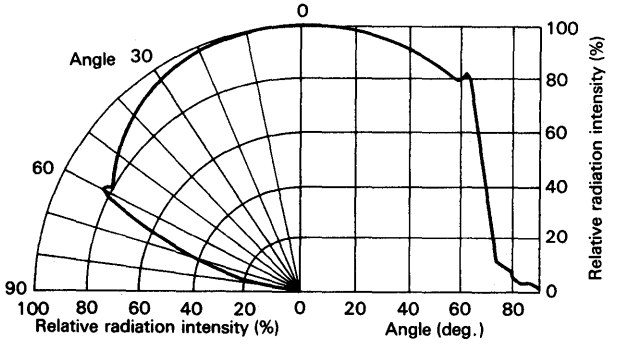
Spectral Distribution



Pulse Response



Radiation Pattern



HE8807SL

Infrared Emitting Diodes (IRED)

Description

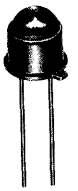
HE8807SL is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

Radiant directionality is narrow and radiant intensity is high; suitable as a light source in encoders and sensors.

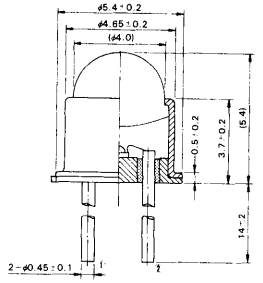
The package is hermetically sealed with the cap and lens, achieving high reliability.

Features

- High efficiency and high power output
- Narrow spectral width
- Narrow radiant directionality



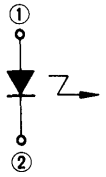
Package Dimensions



(Unit: mm)

SL-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

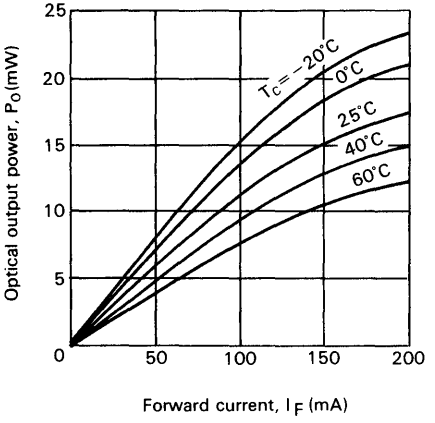
Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

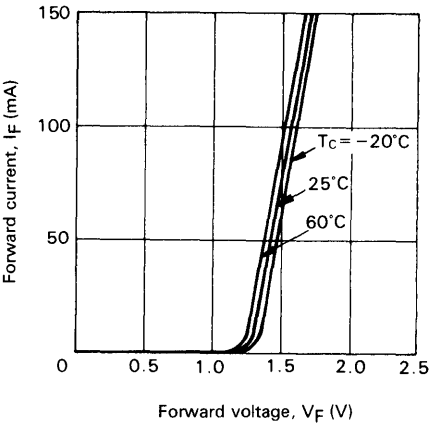
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	5	15		mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		20		ns	I_F = 50 mA
Fall time	t_f		20		ns	I_F = 50 mA

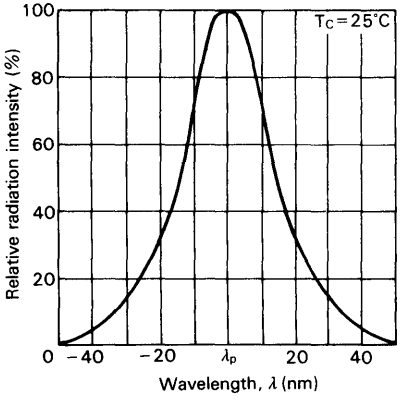
Optical Output Power vs. Forward Current



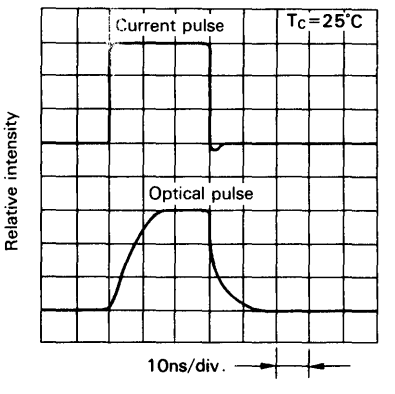
Forward Current vs. Forward Voltage



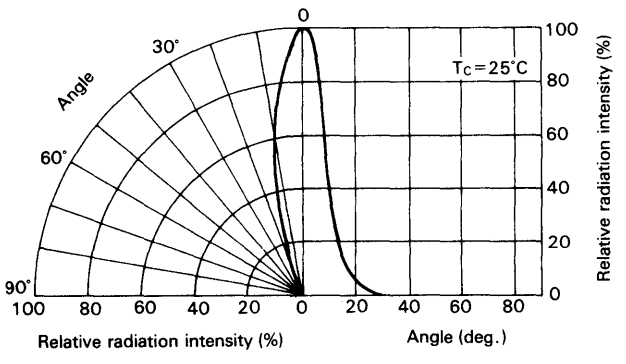
Spectral Distribution



Pulse Response



Radiation Pattern



HE8807CL

Under Development

Infrared Emitting Diodes (IRED)

Description

HE8807CL is a 0.8 μm GaAlAs infrared emitting diode with single heterojunction structure.

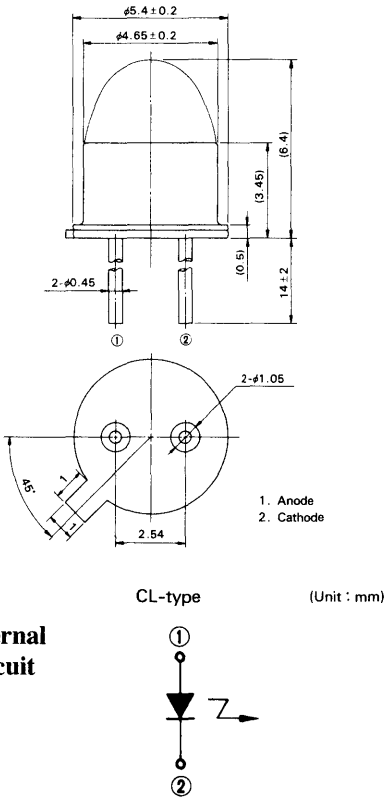
Collimated light beam can be obtained by the package with lens; suitable as a light source in encoders and sensors.

The package is hermetically sealed with the cap and lens, achieving high reliability.

Features

- High efficiency and high power output
- Narrow spectral width
- Collimated light beam

Package Dimensions



CL-type (Unit : mm)

Internal Circuit

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	350	mW
Operating temperature	T_{opr}	−20 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	5	10		mW	I_F = 150 mA
Peak wavelength	λ_p	800	880	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		30	60	nm	I_F = 150 mA
Forward voltage	V_F		1.7	2.3	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		20		ns	I_F = 50 mA
Fall time	t_f		20		ns	I_F = 50 mA

6

HE8811

Infrared Emitting Diodes (IRED)

Description

HE8811 is a 0.8 μm GaAlAs infrared emitting diode with double heterojunction structure. High brightness output, high power output and high speed response can be obtained.

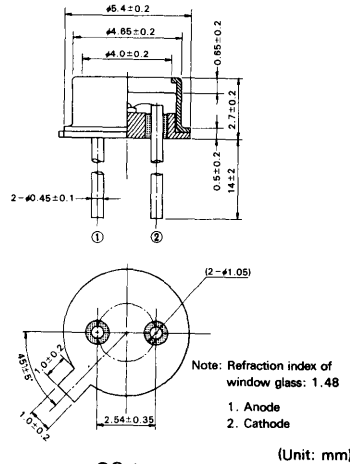
It is suitable as a light source in measuring and beam communications equipment.

Hermetic sealing of the package achieves high reliability.

Features

- High frequency response
- High power output, high efficiency and high brightness output
- Wide radiant directionality

Package Dimensions



(Unit: mm)

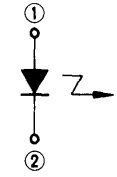
SG-type

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	200	mA
Reverse voltage	V_R	3	V
Tolerable power dissipation	P_d	400	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

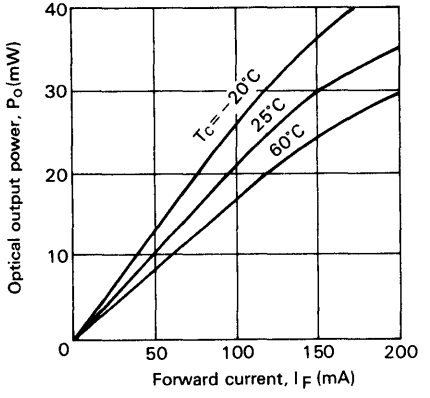
Internal Circuit



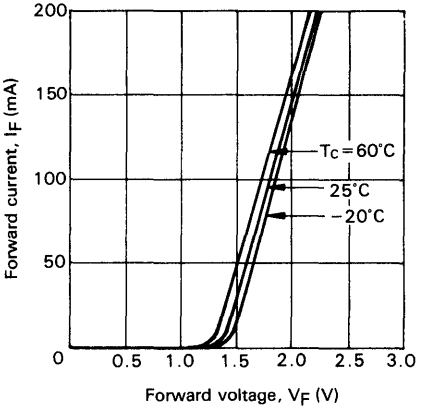
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	20	30		mW	I_F = 150 mA
Peak wavelength	λ_p	780	820	900	nm	I_F = 150 mA
Spectral width	$\Delta\lambda$		50		nm	I_F = 150 mA
Forward voltage	V_F			2.5	V	I_F = 150 mA
Reverse current	I_R			100	μA	V_R = 3 V
Capacitance	C_t		10		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		5		ns	I_F = 50 mA
Fall time	t_f		7		ns	I_F = 50 mA

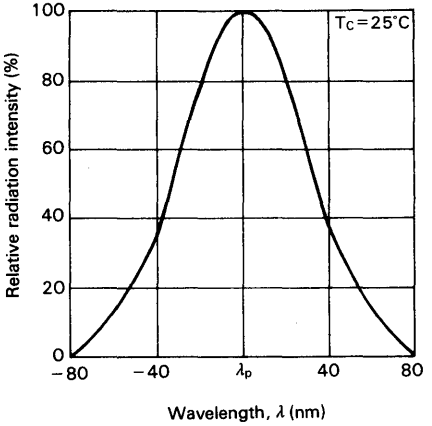
Optical Output Power vs. Forward Current



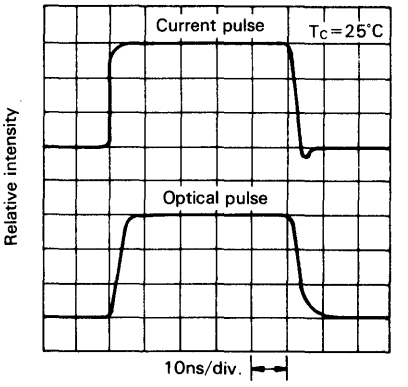
Forward Current vs. Forward Voltage



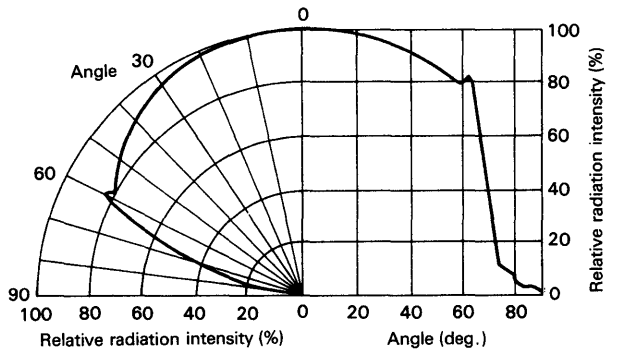
Spectral Distribution



Pulse Response



Radiation Pattern



HE8812SG

Infrared Emitting Diodes (IRED)

Description

HE8812SG is a 0.87 μm GaAlAs infrared emitting diode with double heterojunction structure. High brightness output, high power output and high speed response can be obtained.

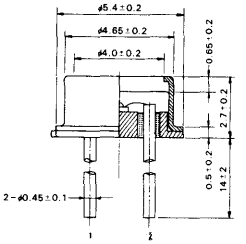
It is suitable as a light source in optical controlling equipment and sensors.

Hermetic sealing of the package achieves high reliability.

Features

- High power output: $P_O \geqq 40$ mW
- Fast pulse response: $t_r = 5$ns, $t_f = 7$ns typ.

Package Dimensions



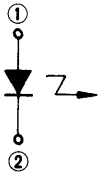
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode

(Unit: mm)

SG-type

Internal Circuit



Absolute Maximum Ratings ($T_C = 25$°C)

Items	Symbols	Values	Units
Forward current	I_F	250	mA
Reverse voltage	V_R	3	V
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics ($T_C = 25$°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Optical output power	P_O	40			mW	$I_F = 200$ mA
Peak wavelength	λ_p	840	870	900	nm	$I_F = 200$ mA
Spectral width	$\Delta\lambda$		50		nm	$I_F = 200$ mA
Forward voltage	V_F			2.5	V	$I_F = 200$ mA
Reverse current	I_R			100	μA	$V_R = 3$ V
Capacitance	C_t		30		pF	$V_R = 0$ V, f = 1 MHz
Rise time	t_r		5		ns	$I_F = 50$ mA
Fall time	t_f		7		ns	$I_F = 50$ mA

HE1301R

Infrared Emitting Diodes (IRED)

Description

HE1301R is a 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

It is suitable as a light source in high-speed digital link (up to 200 Mb/s) of fiberoptic communications equipment.

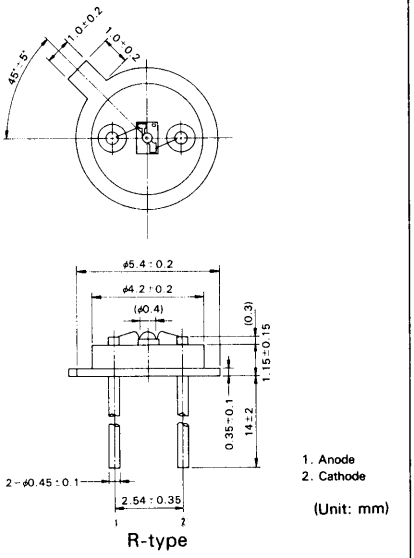
Optical fiber can be close to the chip, achieving high coupling efficiency.

The package should be hermetically sealed before mounting on a system.

Features

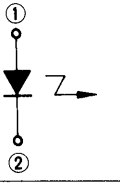
- High power output
- High efficiency and high brightness output
- Fast pulse response

Package Dimensions



R-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +40*	°C
Storage temperature	T_{stg}	−40 to +60*	°C

* Value for conditions without condensation.

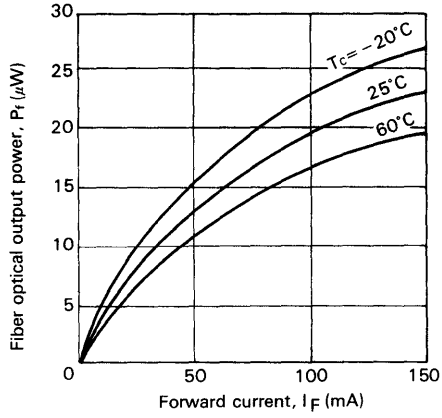
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

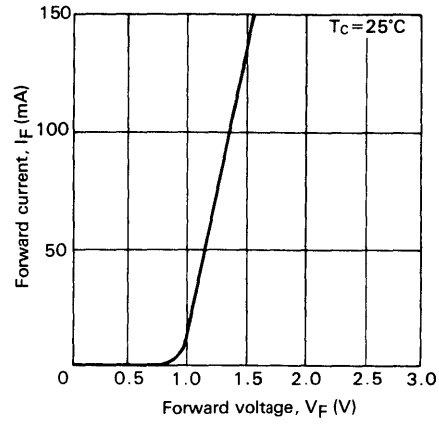
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	15			μW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

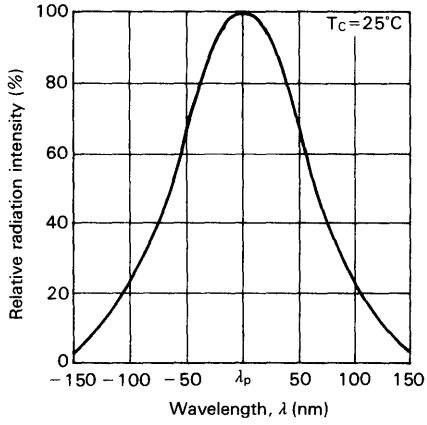
Optical Output Power vs. Forward Current



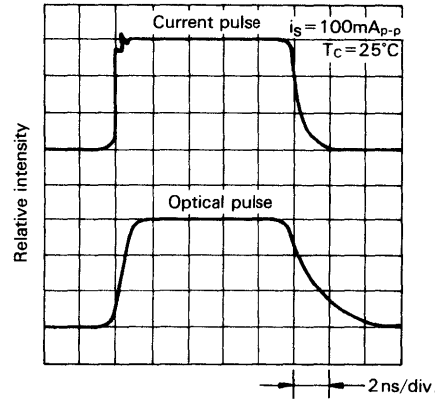
Forward Current vs. Forward Voltage



Spectral Distribution



Pulse Response



6

HE1301SG

Infrared Emitting Diodes (IRED)

Description

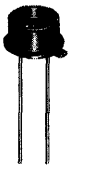
HE1301SG is a 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

High coupling efficiency can be realized using a rod lens; suitable as a light source in fiberoptic communications equipment.

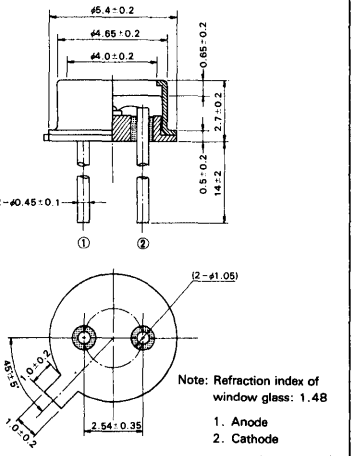
Hermetic sealing of the package achieves high reliability.

Features

- High power output
- High efficiency and high brightness output
- Fast pulse response

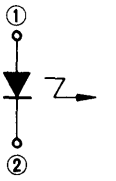


Package Dimensions



SG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

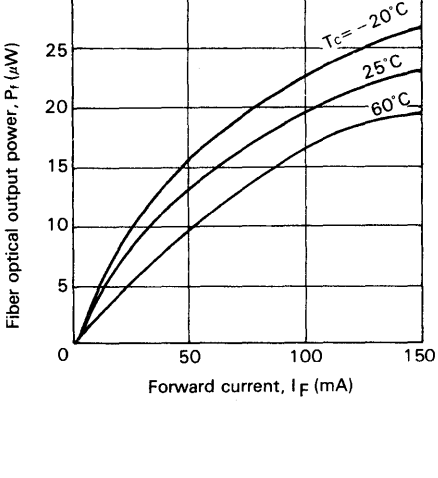
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

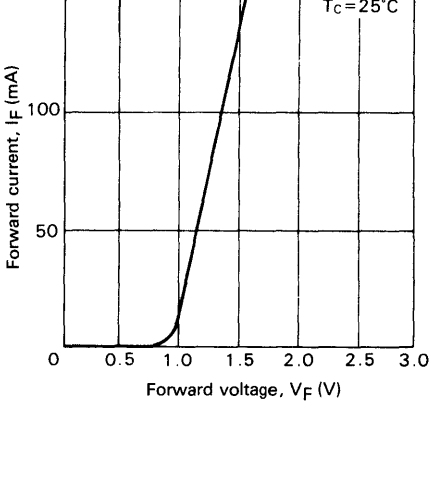
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	15			μW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

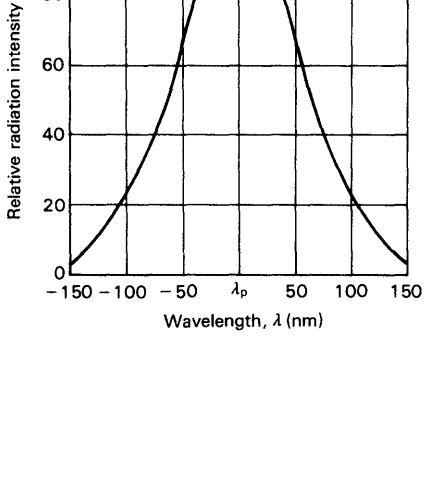
Optical Output Power vs. Forward Current



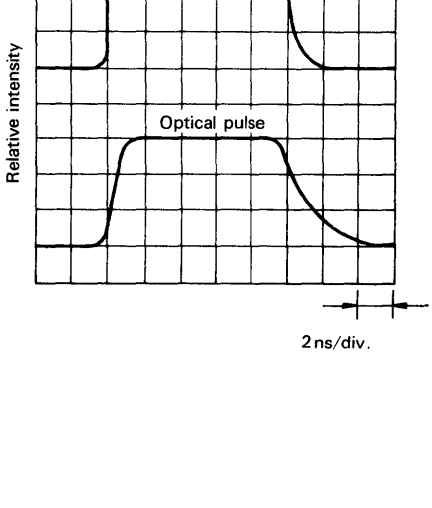
Forward Current vs. Forward Voltage



Spectral Distribution



Pulse Response



6

HE1301ML

Infrared Emitting Diodes (IRED)

Description

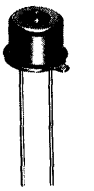
HE1301ML is a 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

Optical output from the chip is directed to the optical fiber efficiently through the microlens in the cap; suitable as a light source in fiberoptic communications equipment.

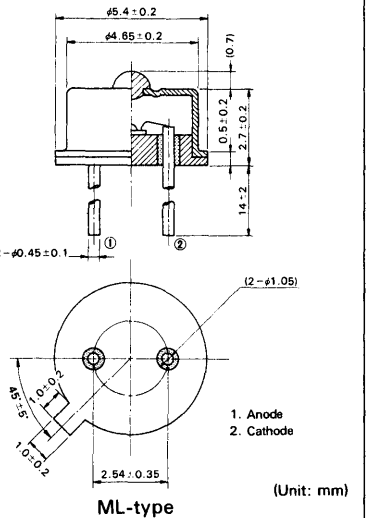
Hermetic sealing of the package achieves high reliability.

Features

- High power output
- High efficiency and high brightness output
- Fast pulse response



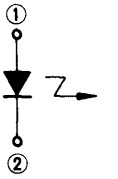
Package Dimensions



(Unit: mm)

ML-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +60	°C
Storage temperature	T_{stg}	−40 to +90	°C

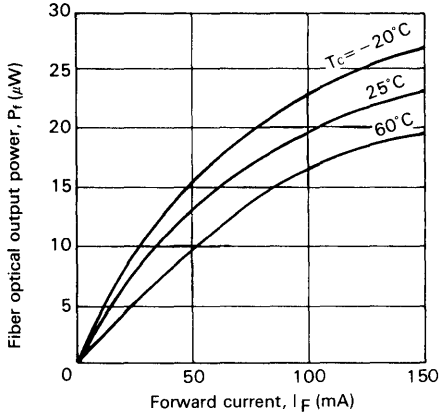
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

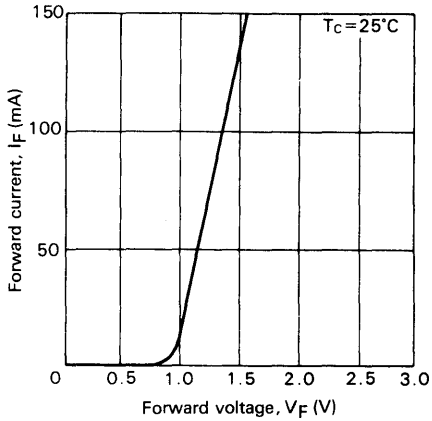
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	15			μW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

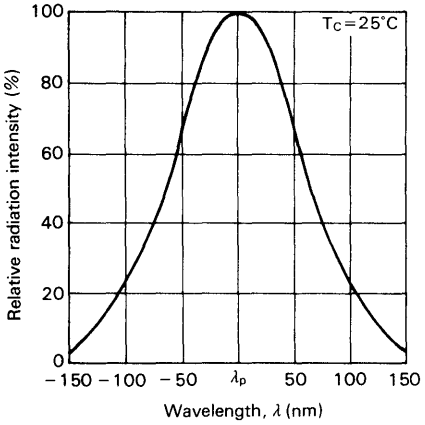
Optical Output Power vs. Forward Current



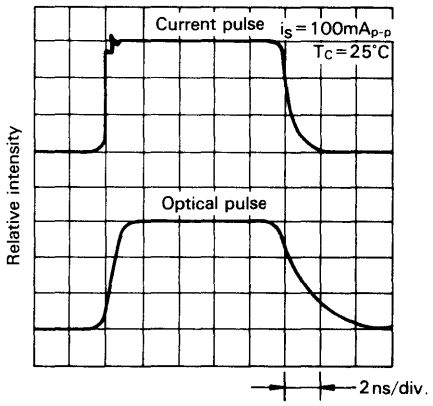
Forward Current vs. Forward Voltage



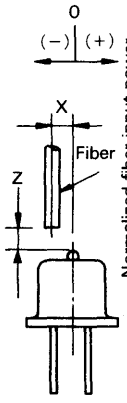
Spectral Distribution

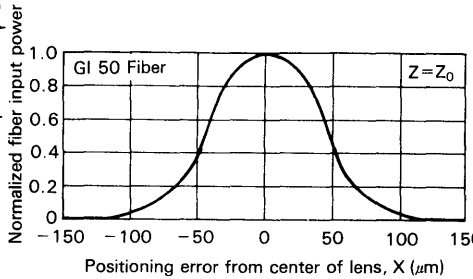


Pulse Response



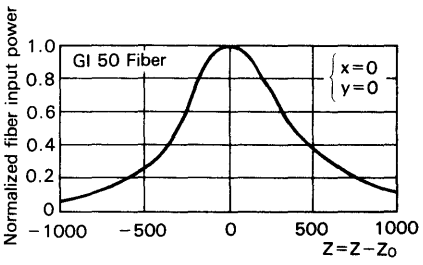
Coupling Characteristics





Fiber input deviation due to lateral fiber positioning error

Z_0: Focal point of lens



Fiber input deviation due to horizontal fiber positioning error

HE1301TR

Infrared Emitting Diodes (IRED)

Description

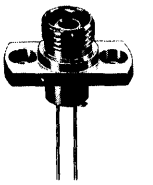
HE1301TR is a 1.3 μm InGaAsP infrared emitting diode with double heterojunction structure, which provides high speed response.

The package with a receptacle is easily connected with FC-type connector; suitable as a light source in fiberoptic communications equipment.

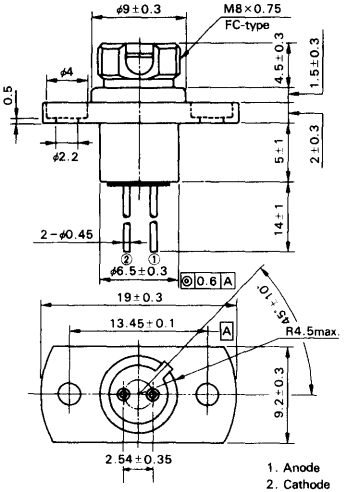
Hermetic sealing of the package achieves high reliability.

Features

- High efficiency and high brightness output
- Fast pulse response
- Wide operating-temperature range: T_{opr} = −20 to +85°C

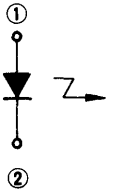


Package Dimensions



TR-type (Unit : mm)

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	150	mA
Reverse voltage	V_R	1.0	V
Tolerable power dissipation	P_d	300	mW
Operating temperature	T_{opr}	−20 to +85	°C
Storage temperature	T_{stg}	−40 to +100	°C

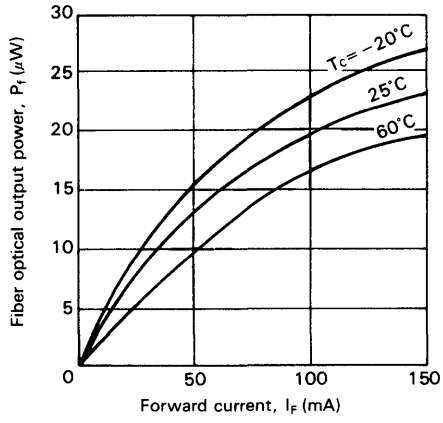
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

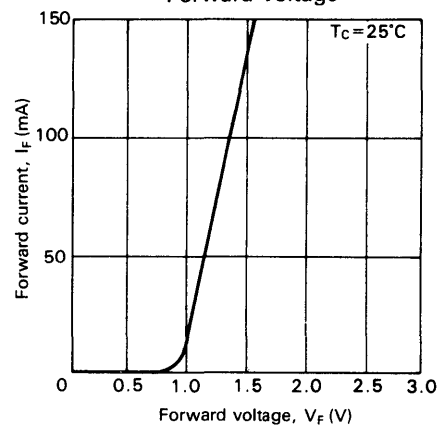
Items	Symbols	min.	typ.	max.	Units	Test conditions
Fiber optical output power	P_f*	15	20		μW	I_F = 100 mA
Peak wavelength	λ_p	1260	1300	1340	nm	I_F = 100 mA
Spectral width	$\Delta\lambda$		140		nm	I_F = 100 mA
Forward voltage	V_F		1.5	2.0	V	I_F = 100 mA
Capacitance	C_t		30		pF	V_R = 0 V, f = 1 MHz
Rise time	t_r		1.5		ns	I_F = 100 mA
Fall time	t_f		4.0		ns	I_F = 100 mA

* At GI 50/125 fiber end.

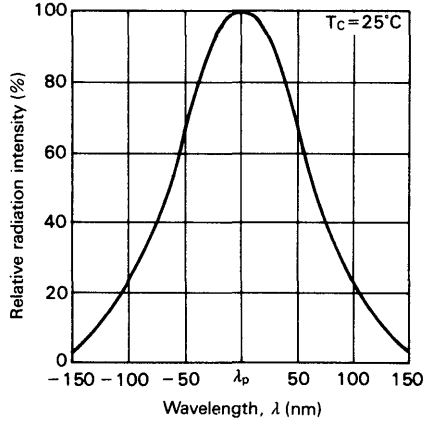
Optical Output Power vs. Forward Current



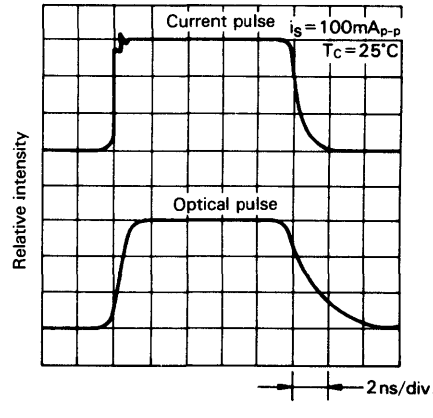
Forward Current vs. Forward Voltage



Spectral Distribution



Pulse Response



6

Photodiodes

HR8101

Photodiode

Description

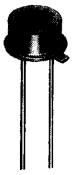
HR8101 is a Si PIN photodiode for detecting 0.6–0.9 μm light.

It is suitable as an optical monitor in measuring and fiberoptic communications and various other types of optical equipment.

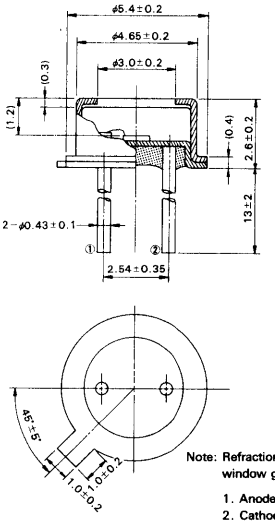
Hermetic sealing of the package achieves high reliability.

Features

- High speed pulse response: t_r, t_f = 30 ns typ.
- Photodetectable area: 0.8 × 0.8 mm□



Package Dimensions



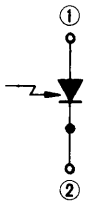
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode (Case)

(Unit: mm)

QG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

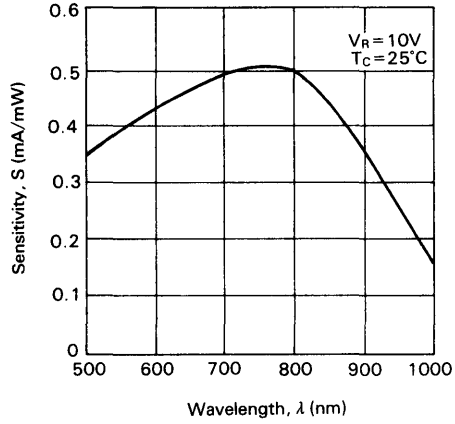
Items	Symbols	Values	Units
Reverse voltage	V_R	100	V
Forward current	I_F	100	mA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

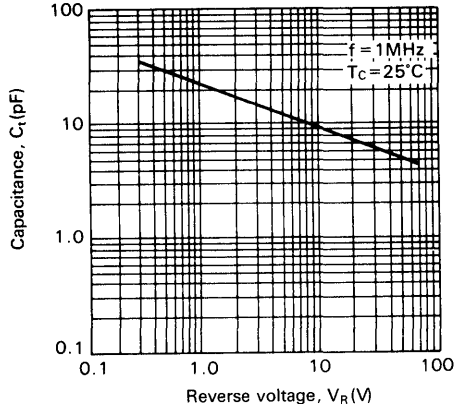
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		2	10	nA	V_R = 10 V
Capacitance	C_t		10	15	pF	V_R = 10 V, f = 1 MHz
Sensitivity	S	0.4			mA/mW	V_R = 10 V, λ_p = 830 nm
Rise time	t_r		30		ns	V_R = 10 V, λ_p = 830 nm R_L = 50 Ω
Fall time	t_f		30		ns	V_R = 10 V, λ_p = 830 nm R_L = 50 Ω

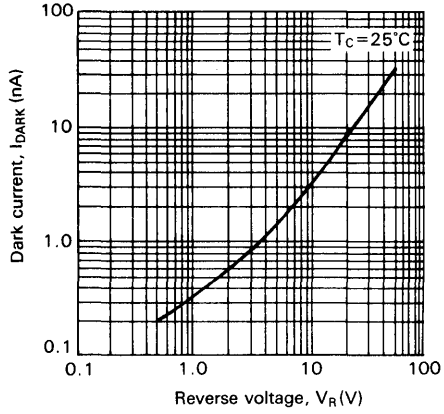
Sensitivity vs. Wavelength



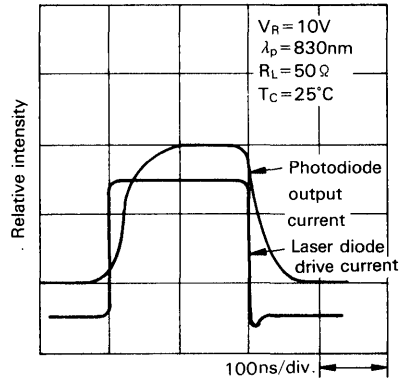
Capacitance vs. Reverse Voltage



Dark Current vs. Reverse Voltage



Pulse Response



HR8102

Photodiode

Description

HR8102 is a Si PIN photodiode for detecting 0.6–0.9 μm light.

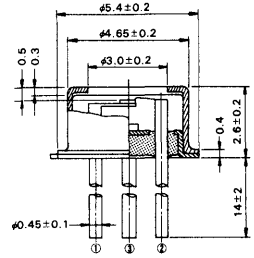
Its high speed pulse response makes it especially suitable as an optical signal detector in high-bit-rate fiberoptic communications equipment.

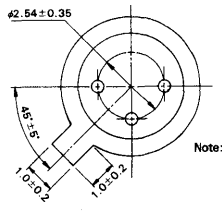
Hermetic sealing of the package achieves high reliability.

Features

- High sensitivity to wide wavelength range
- High speed pulse response: t_r, t_f = 1 ns typ.
- 5 V of low voltage operation
- Photodetectable area: 300 μm dia.

Package Dimensions





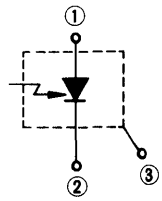
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	100	V
Forward current	I_F	100	mA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

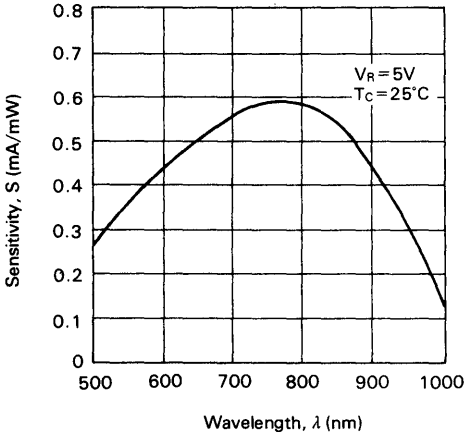
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

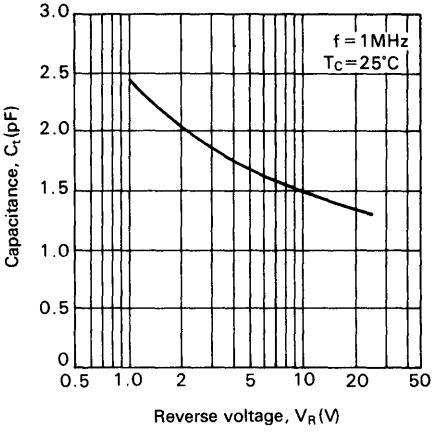
Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		0.5	3	nA	V_R = 10 V
Capacitance	C_t		1.5	3	pF	V_R = 10 V, f = 1 MHz
Sensitivity	S	0.4			mA/mW	V_R = 10 V, λ_p = 830 nm
Rise time	t_r		1.0		ns	V_R = 10 V, λ_p = 830 nm, R_L = 50 Ω
Fall time	t_f		1.0		ns	V_R = 10 V, λ_p = 830 nm, R_L = 50 Ω

6

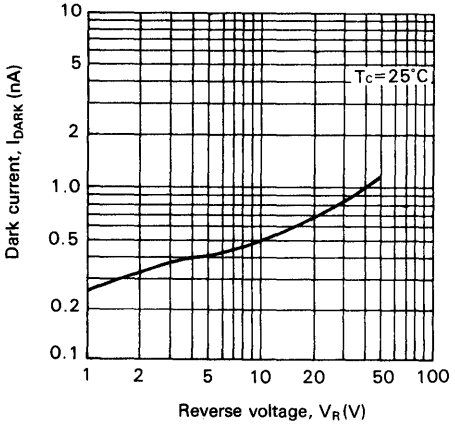
Sensitivity vs. Wavelength



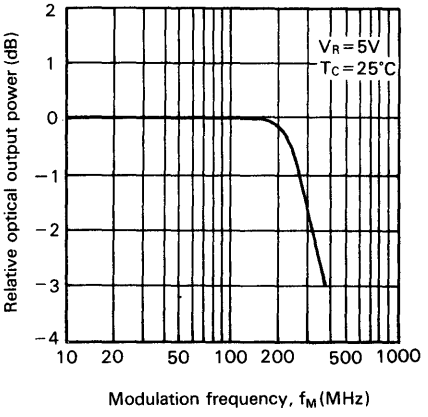
Capacitance vs. Reverse Voltage



Dark Current vs. Reverse Voltage



Frequency Response



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HR8202TG

Photodiode

Description

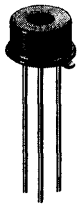
HR8202TG is a Si avalanche photodiode for detecting 0.6 – 0.9 μm light.

Its high frequency characteristics make it especially suitable as an optical signal detector in analog fiberoptic communications equipment.

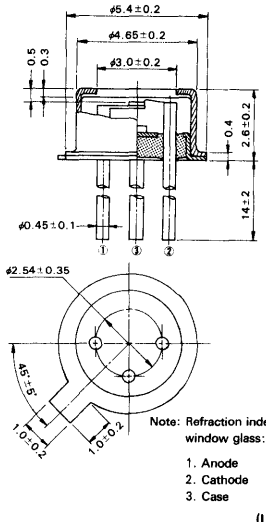
Hermetic sealing of the package achieves high reliability.

Features

- High quantum efficiency: More than 70%
- High speed response : More than 300 MHz
- Low dark current : Less than 3 nA
- Low operation voltage : Less than 200 V
- Photodetectable area : 300 μm dia.



Package Dimensions



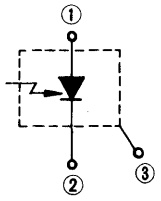
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	100	mA
Reverse current	I_R	200	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

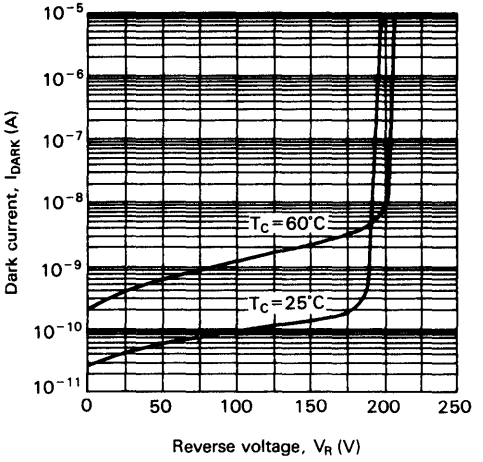
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

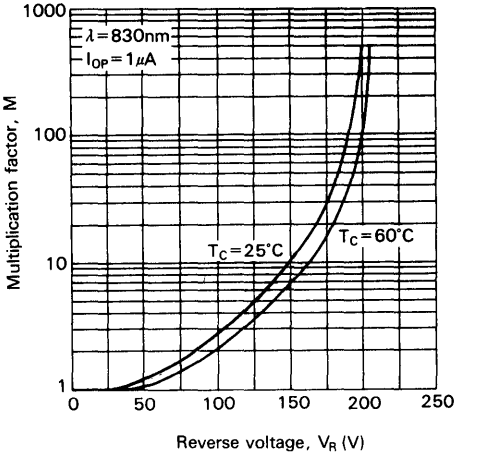
Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		0.5	3	nA	V_R = 0.9 V_B
Capacitance	C_t		1.5		pF	V_R = 100 V, f = 1 MHz
Sensitivity	S	0.46	0.52		mA/mW	λ_p = 830 nm, M = 1
Quantum efficiency	η	70	78		%	λ_p = 830 nm, M = 1
Breakdown voltage	V_B	150	180	220	V	I_{DARK} = 100 μA
Cut-off frequency	f_c		600		MHz	λ_p = 830 nm, R_L = 50Ω, M = 10
Excessive noise factor	F		2			λ_p = 830 nm, M = 10 f = 10 MHz, B = 300 kHz
	x		0.3			
Multiplication factor	M	30				V_R = 0.9 V_B, λ_p = 830 nm

6

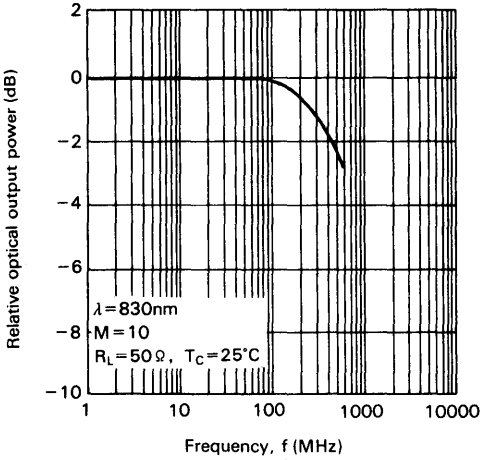
Dark Current vs. Reverse Voltage



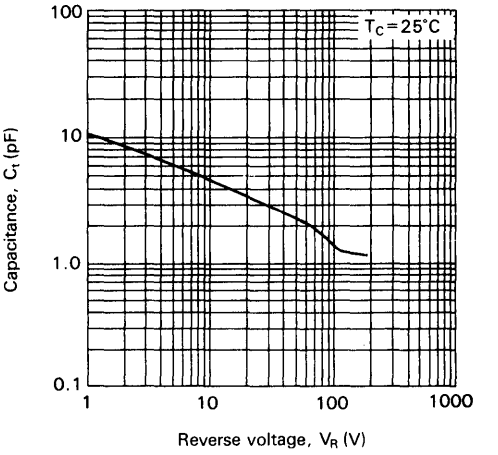
Multiplication Factor vs. Reverse Voltage



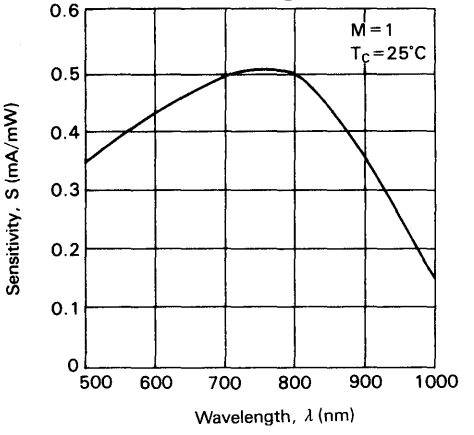
Frequency Response



Capacitance vs. Reverse Voltage



Sensitivity vs. Wavelength



HR1103TG

Photodiode

Description

HR1103TG is an InGaAs PIN photodiode for detecting 1.0–1.65 μm light.

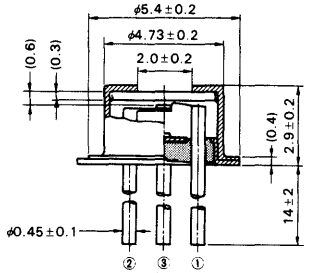
Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

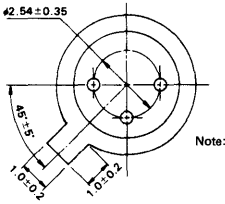
Hermetic sealing of the package achieves high reliability.

Features

- Fast pulse response : t_r, t_f = 0.5 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 1 nA typ.
- Small capacitance : C_t = 1.0 pF typ.
- Photodetectable area : 100 μm dia.

Package Dimensions





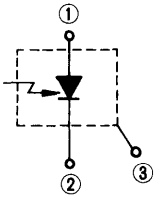
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

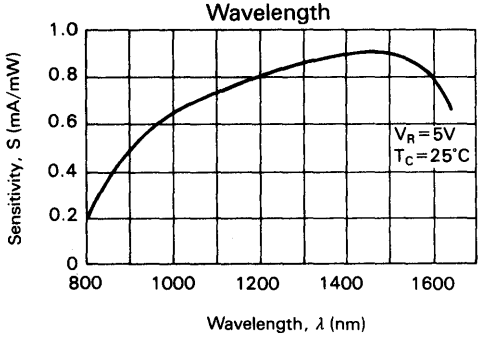
Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

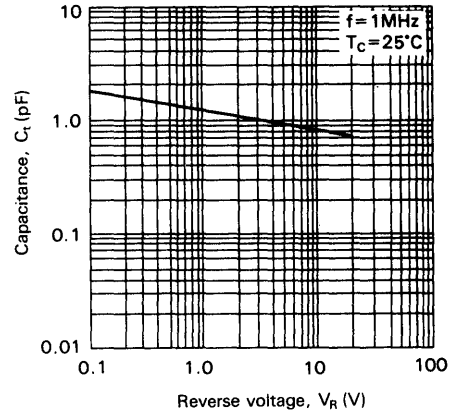
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		1	20	nA	V_R = 5 V
Capacitance	C_t		1.0	1.5	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

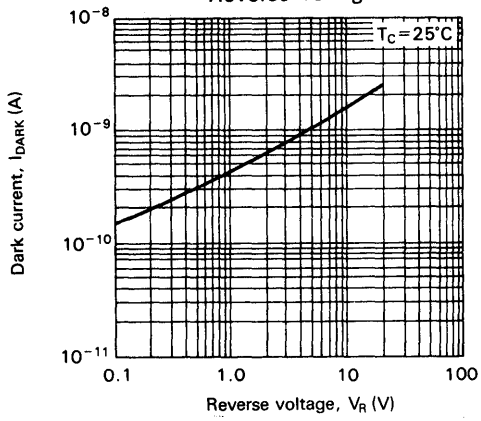
Sensitivity vs. Wavelength



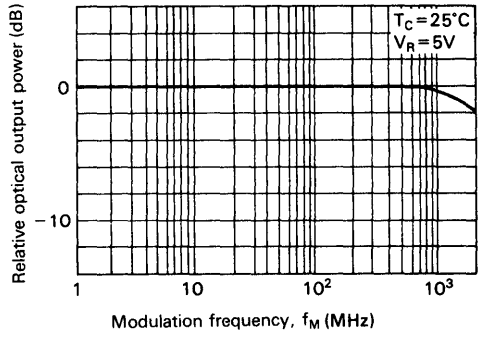
Capacitance vs. Reverse Voltage



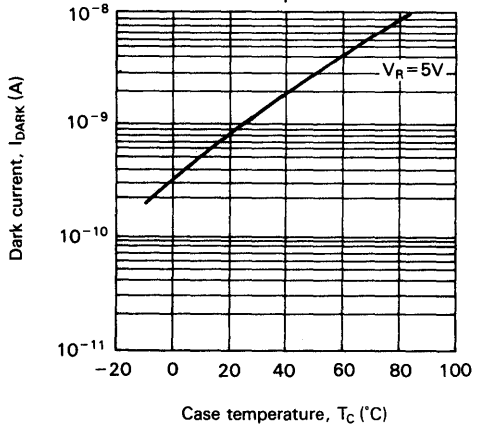
Dark Current vs. Reverse Voltage



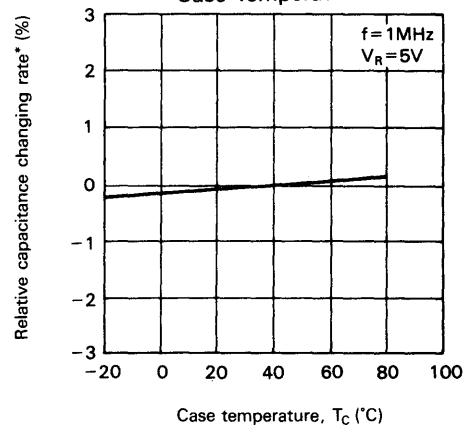
Frequency Response



Dark Current vs. Case Temperature

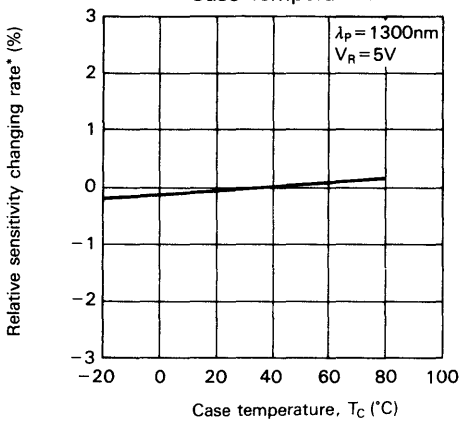


Capacitance vs. Case Temperature



(*Between terminal pins at T_C=25°C)

Sensitivity vs.
Case Temperature



(*At T_C=25°C)

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HR1103CX

Photodiode

Description

HR1103CX is an InGaAs PIN photodiode for detecting 1.0 – 1.65 μm light.

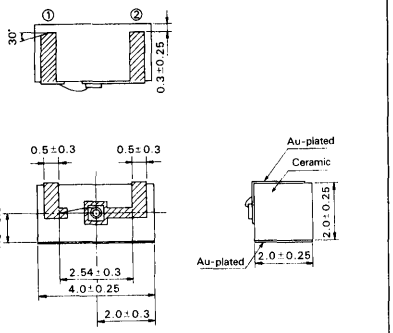
Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

The package is compact for ease in module assembly.

Features

- Fast pulse response : t_r, t_f = 0.5 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 1 nA typ.
- Small capacitance : C_t = 1.2 pF typ.
- Photodetectable area : 100 μm dia.

Package Dimensions

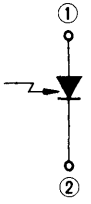


1. Anode
2. Cathode

(Unit: mm)

CX-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

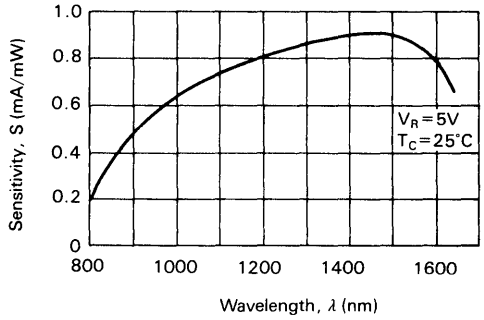
Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

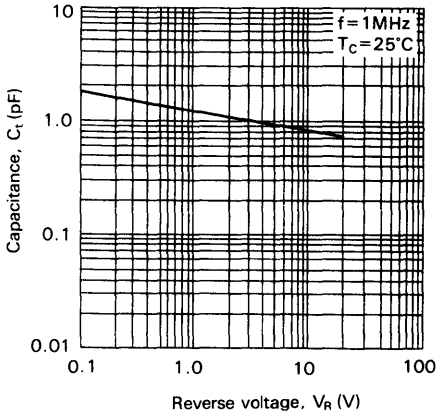
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		1	50	nA	V_R = 5 V
Capacitance	C_t		1.2		pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

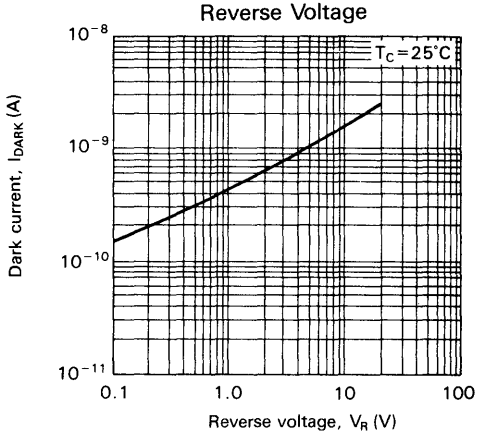
Sensitivity vs. Wavelength



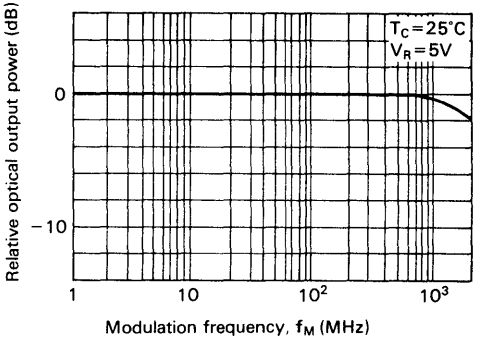
Capacitance vs. Reverse Voltage



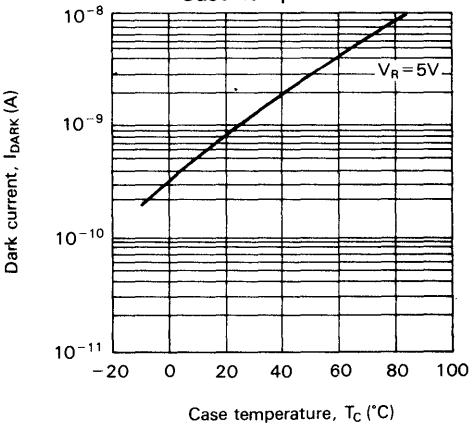
Dark Current vs. Reverse Voltage



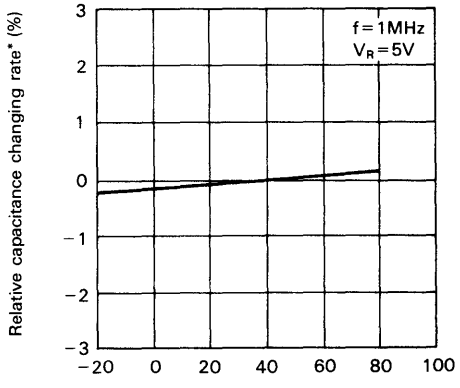
Frequency Response



Dark Current vs. Case Temperature



Capacitance vs. Case Temperature



(* Between terminal pins at T_C=25°C)

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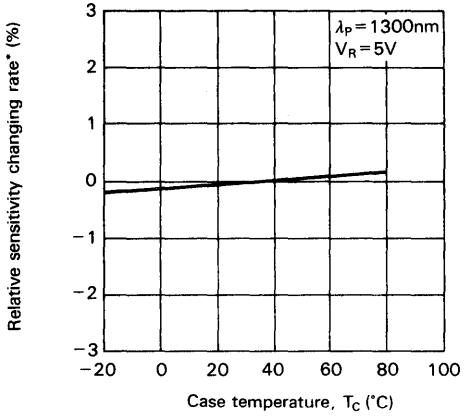
Sensitivity vs.
Case Temperature



(* At T_C=25°C)

HR1103TR

Photodiode

Description

HR1103TR is an InGaAs PIN photodiode for detecting 1.0 – 1.65 μm light.

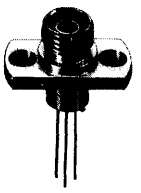
Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

This package, with a receptacle, is easily connected to fiber with FC-type connector.

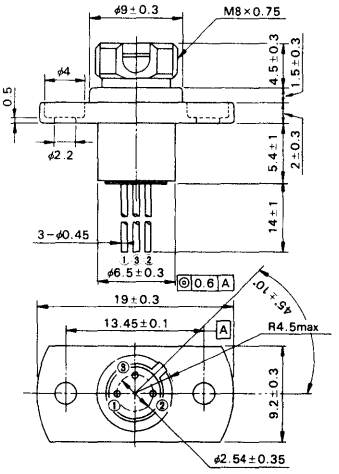
Hermetic sealing of the package achieves high reliability.

Features

- High sensitivity : S ≧ 0.6 mA/mW (λ_p = 1300 nm)
- Fast pulse response : t_r, t_f = 0.5 ns typ.
- Wide operating-temperature range : T_{opr} = −20 to +85°C
- Photodetectable area : 100 μm dia.

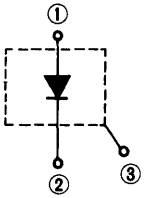


Package Dimensions



TR-type (Unit : mm)

Internal Circuit



① Anode
② Cathode
③ Case

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−45 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		1	20	nA	V_R = 5 V
Capacitance	C_t		1.0	1.5	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1*	0.6		0.7	mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2*		0.85		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		0.5		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

* At GI50/125 fiber

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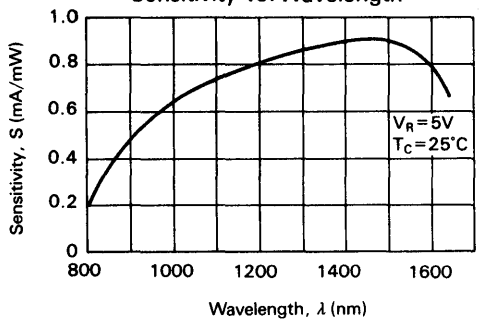
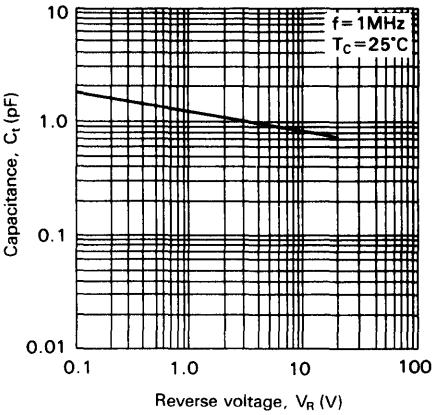
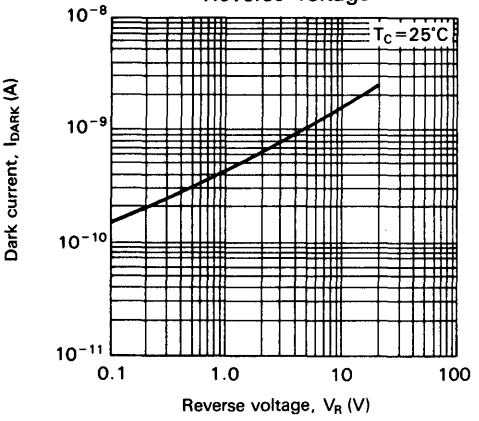
Sensitivity vs. Wavelength



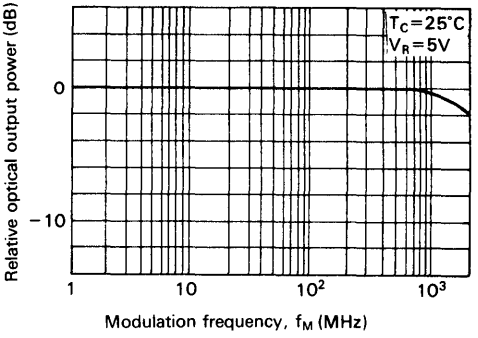
Capacitance vs. Reverse Voltage



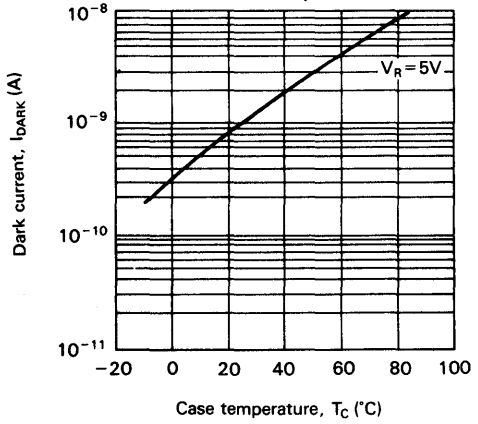
Dark Current vs. Reverse Voltage



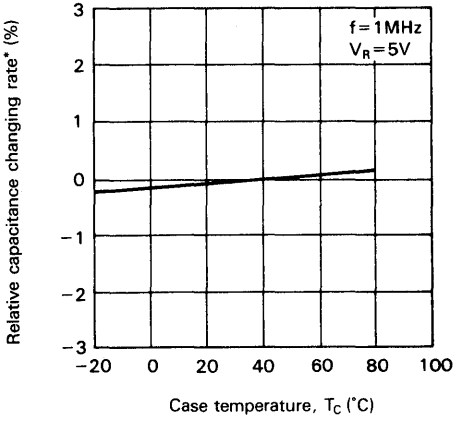
Frequency Response



Dark Current vs. Case Temperature

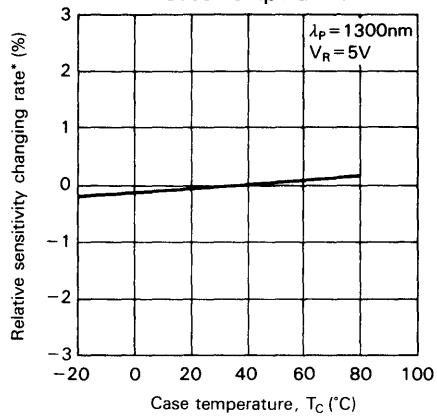


Capacitance vs. Case Temperature



(*Between terminal pins at $T_C = 25°C$)

Sensitivity vs.
Case Temperature



(*At T_C=25°C)

6

HR1104TG

Photodiode

Description

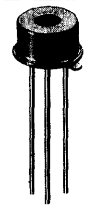
HR1104TG is an InGaAs PIN photodiode for detecting 1.0–1.65 μm light.

It is suitable as an optical monitor in high-bit-rate fiberoptic communications equipment.

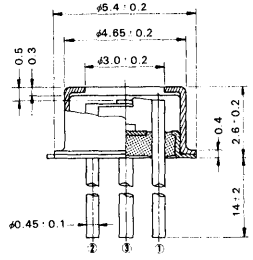
Hermetic sealing of the package achieves high reliability.

Features

- Fast pulse response : t_r, t_f = 1.0 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 5 nA typ.
- Small capacitance : C_t = 5 pF typ.
- Photodetectable area : 300 μm dia.



Package Dimensions



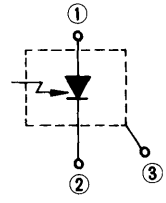
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

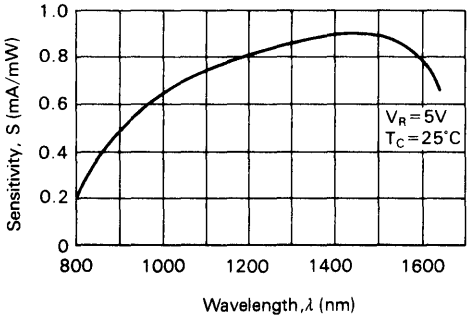
Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

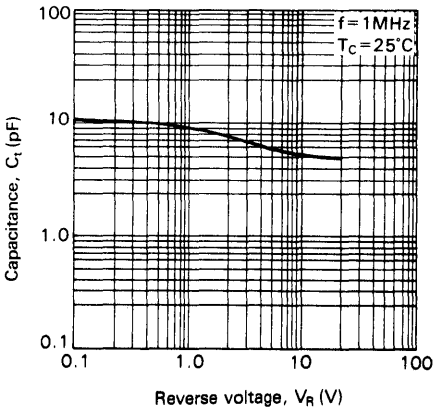
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		10	30	nA	V_R = 5 V
Capacitance	C_t		5	10	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		1.0		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		1.0		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

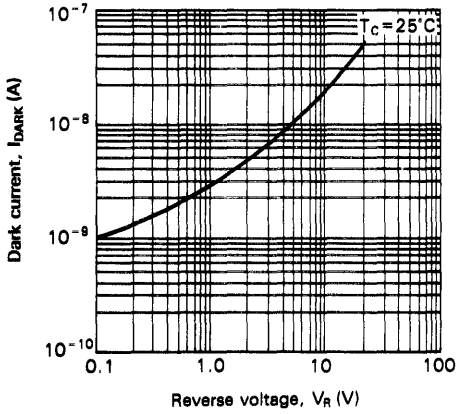
Sensitivity vs. Wavelength



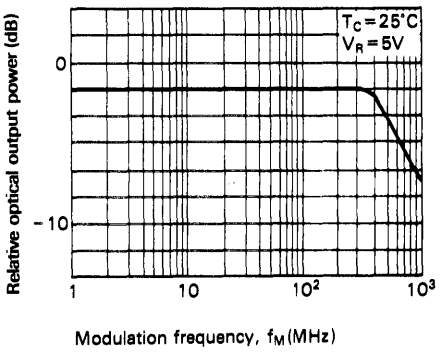
Capacitance vs. Reverse Voltage



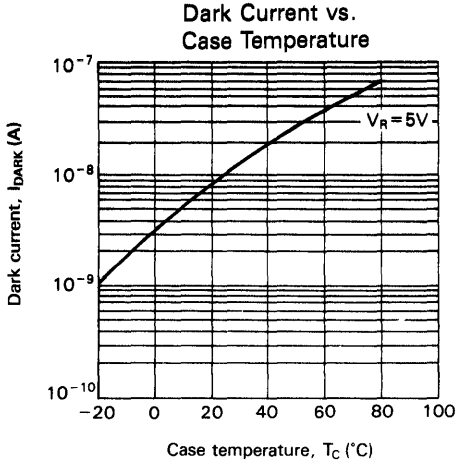
Dark Current vs. Reverse Voltage



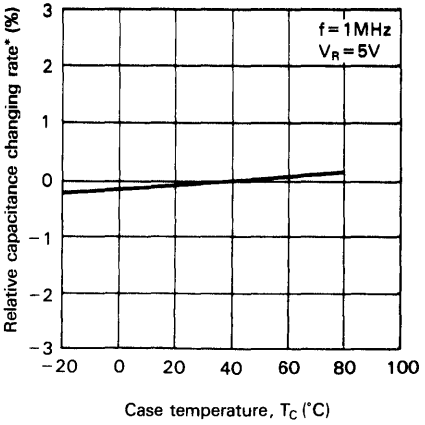
Frequency Response



Dark Current vs. Case Temperature



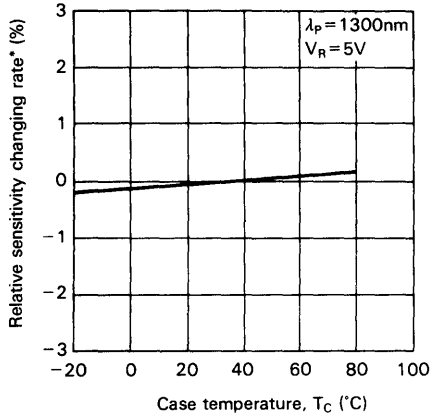
Capacitance vs. Case Temperature



(* Between terminal pins at T_C=25°C)

6

Sensitivity vs.
Case Temperature



(*At T_C=25°C)

HR1104CX

Photodiode

Description

HR1104CX is an InGaAs PIN photodiode for detecting 1.0–1.65 μm light.

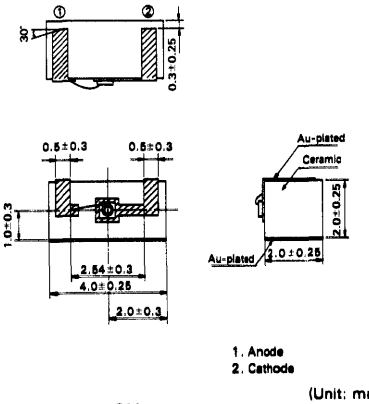
It is suitable as an optical monitor in high-bit-rate fiberoptic communications equipment.

The package is compact for ease in module assembly.

Features

- Fast pulse response : t_r, t_f = 1.0 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 5 nA typ.
- Small capacitance : C_t = 6 pF typ.
- Photodetectable area : 300 μm dia.

Package Dimensions



1. Anode
2. Cathode

(Unit: mm)

CX-type

Internal Circuit

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−40 to +100	°C

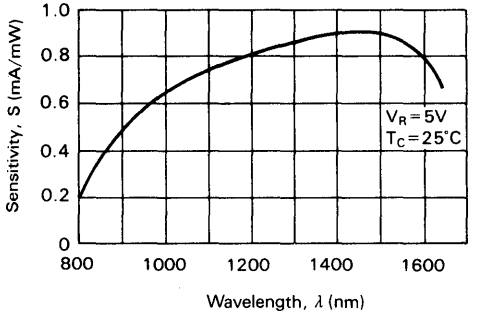
The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Optical and Electrical Characteristics (T_C = 25°C)

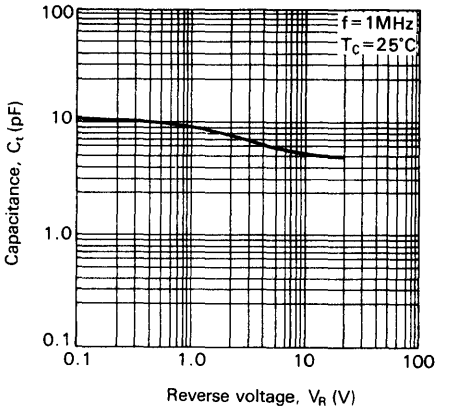
Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		10	30	nA	V_R = 5 V
Capacitance	C_t		6		pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		1.0		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		1.0		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

6

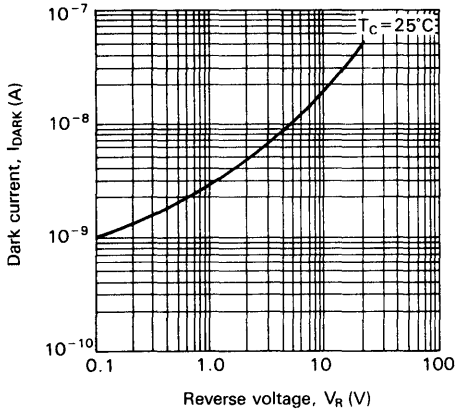
Sensitivity vs. Wavelength



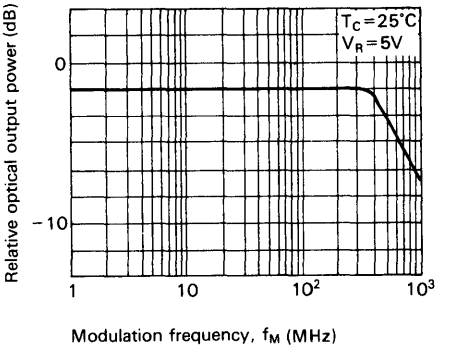
Capacitance vs. Reverse Voltage



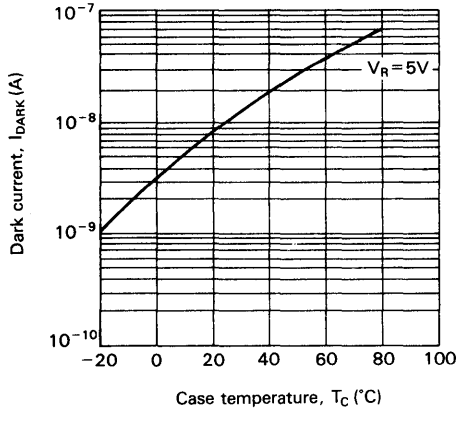
Dark Current vs. Reverse Voltage



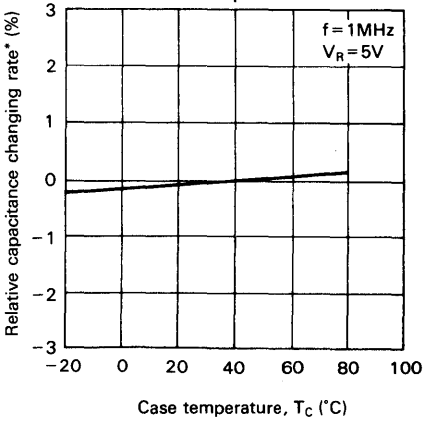
Frequency Response



Dark Current vs. Case Temperature

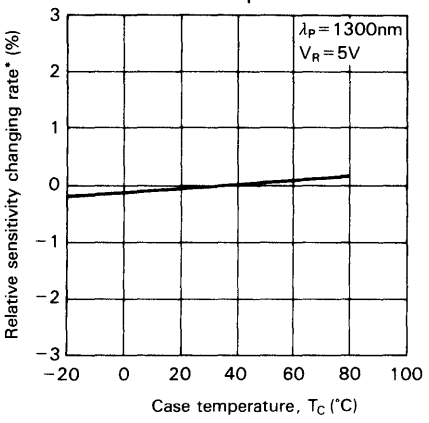


Capacitance vs. Case Temperature



(*Between terminal pins at T_C=25°C)

Sensitivity vs.
Case Temperature



(*At T_C=25°C)

6

HR1105TG

Photodiode

Description

HR1105TG is an InGaAs PIN photodiode for detecting 1.0–1.65 μm light.

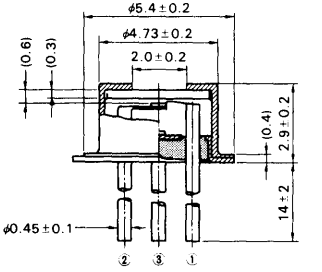
Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

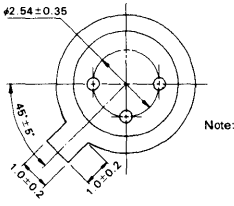
Hermetic sealing of the package achieves high reliability.

Features

- Fast pulse response : t_r, t_f = 0.3 ns typ.
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 1 nA typ.
- Small capacitance : C_t = 0.8 pF typ.
- Photodetectable area : 80 μm dia.

Package Dimensions





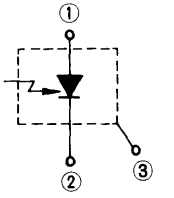
Note: Refraction index of window glass: 1.48

1. Anode
2. Cathode
3. Case

(Unit: mm)

TG-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

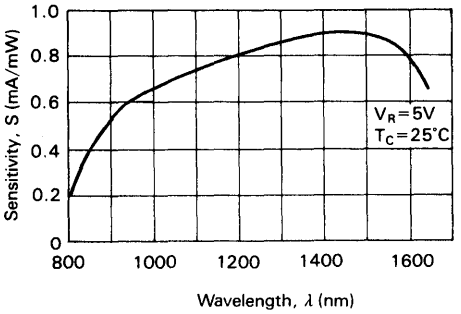
Items	Symbols	Values	Units
Reverse voltage	V_R	20	V
Forward current	I_F	1.0	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

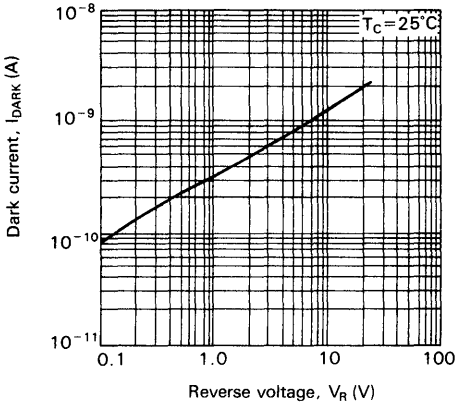
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		1.0	10	nA	V_R = 5 V
Capacitance	C_t		0.8	1.2	pF	V_R = 5 V, f = 1 MHz
Sensitivity	S_1	0.73	0.85		mA/mW	V_R = 5 V, λ_p = 1300 nm
	S_2		0.9		mA/mW	V_R = 5 V, λ_p = 1550 nm
Photosensitivity saturation voltage	$V_{R(S)}$			2	V	
Rise time	t_r		0.3		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω
Fall time	t_f		0.3		ns	V_R = 5 V, λ_p = 1300 nm, R_L = 50 Ω

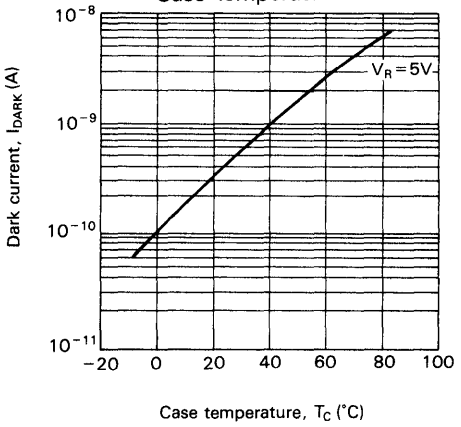
Sensitivity vs.
Wavelength



Dark Current vs.
Reverse Voltage



Dark Current vs.
Case Temperature



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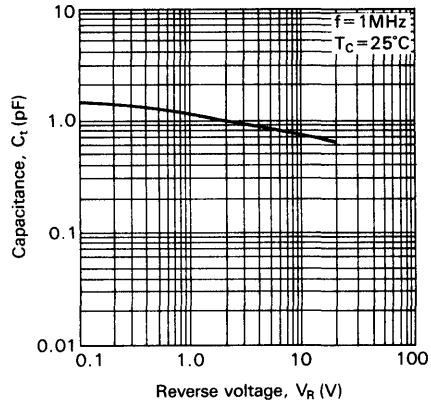
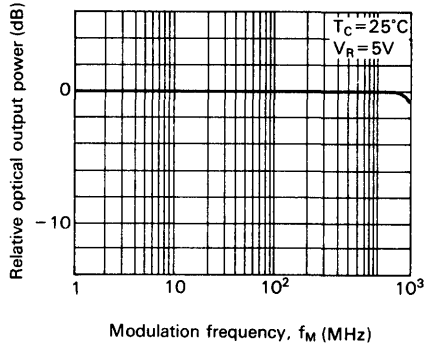
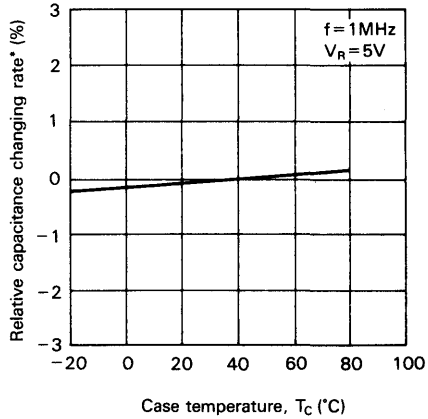
Capacitance vs.
Reverse Voltage



Frequency Response

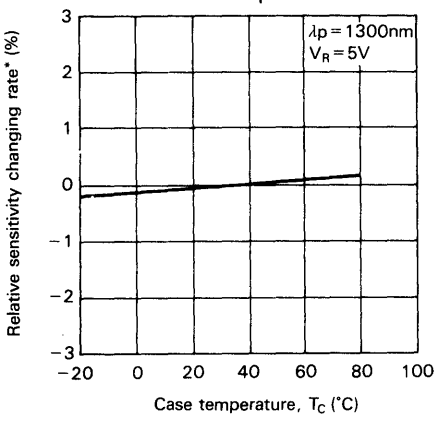


Capacitance vs.
Case Temperature



(*Between terminal pins at T_C=25°C)

Sensitivity vs.
Case Temperature



(*At T_C=25°C)

6

HR1201TG

Photodiode

Description

HR1201TG is an InGaAs avalanche photodiode for detecting 1.0 – 1.65 μm light.

Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

Hermetic sealing of the package achieves high reliability.

Features

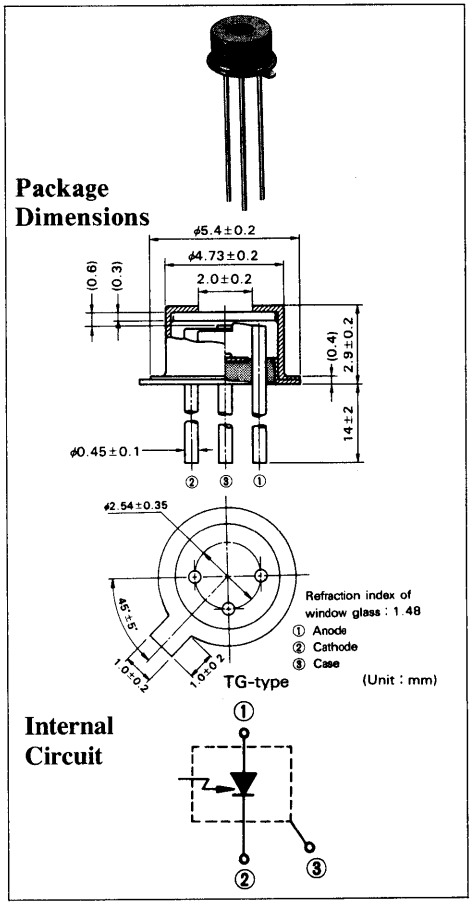
- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 2 nA typ.
- Small capacitance : C_t = 0.5 pF typ.
- Photodetectable area : 50 μm dia.
- High multiplication ratio : M = 40 typ.
- High cut-off frequency : $f_c \cdot G$ = 30 typ.

Absolute Maximum Ratings (T_C = 25°C)

Items	Symbols	Values	Units
Forward current	I_F	10	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Package Dimensions



Internal Circuit

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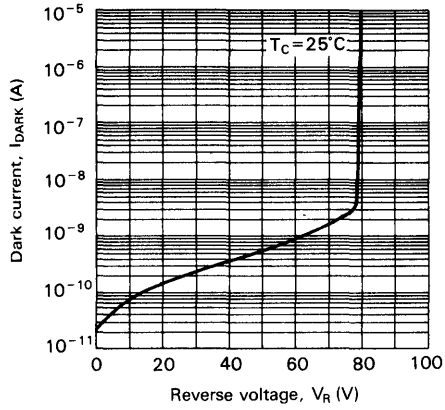
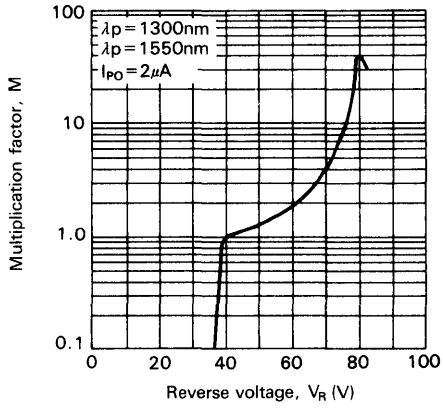
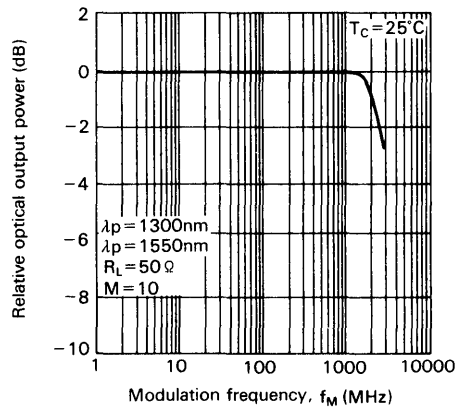
Dark Current vs. Reverse Voltage



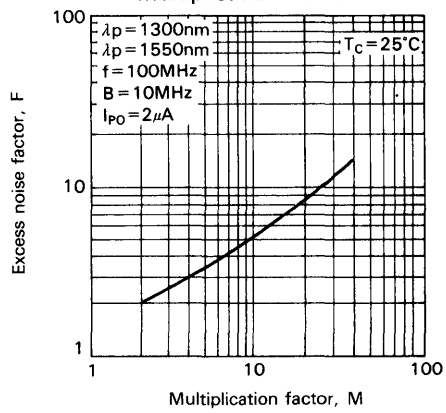
Multiplication Factor vs. Reverse Voltage



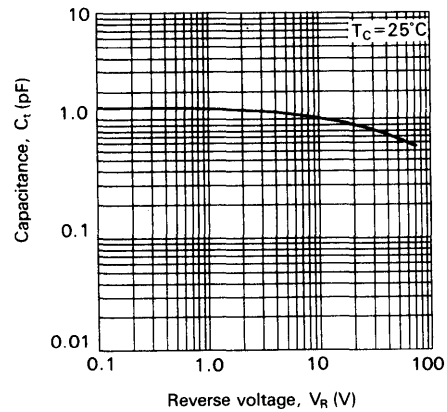
Frequency Response



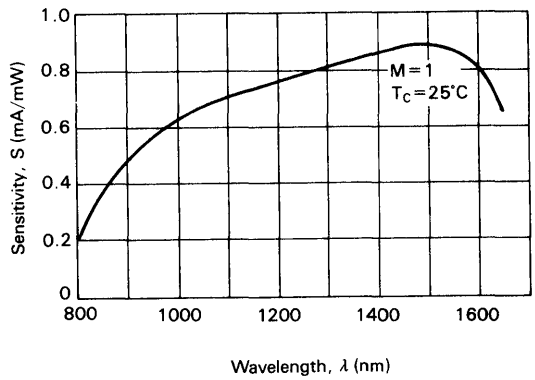
Excess Noise Factor vs. Multiplication Factor



Capacitance vs. Reverse Voltage



Sensitivity vs. Wavelength



Optical and Electrical Characteristics ($T_C = 25°C$)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		2	50	nA	$V_R = 0.9\ V_B$
Multiplicated dark current	I_{DM}		0.5	5	nA	$M = 1$
Capacitance	C_t		0.5	0.8	pF	$f = 1$ MHz, $V_R = 0.9\ V_B$
Sensitivity	S_1	0.73	0.85		mA/mW	$\lambda_p = 1300$ nm
	S_2		0.9		mA/mW	$\lambda_p = 1550$ nm
Breakdown voltage	V_B	60	80	100	V	$I_{DARK} = 100\ \mu A$
Cut-off frequency	f_c	1			GHz	$M = 5$ $\lambda_p = 1300$ nm, $R_L = 50\ \Omega$, Output: 500 kHz −3 dB
		1				$M = 10$
			1			$M = 30$
Excess noise factor	F		5			$\lambda_p = 1300$ nm, $M = 10$ $f = 100$ MHz, $B = 10$ MHz, $I_{PO} = 2\ \mu A$
	x		0.7			
Maximum multiplication factor	M_m	30	40			$\lambda_p = 1300$ nm, $I_{PO} = 2\ \mu A$

6

HR1201CX

Photodiode

Description

HR1201CX is an InGaAs avalanche photodiode for detecting 1.0–1.65 μm light.

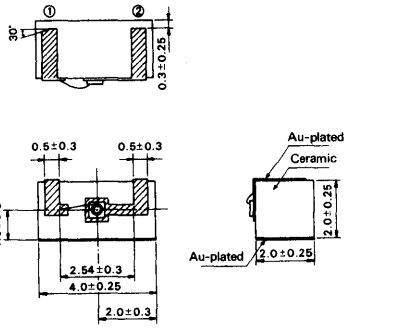
Its high speed pulse response makes it suitable as an optical signal detector in high-bit-rate fiber-optic communications equipment.

The package is compact for ease in module assembly.

Features

- High sensitivity : S = 0.9 mA/mW typ. (λ_p = 1550 nm)
- Low dark current : I_{DARK} = 2 nA typ.
- Small capacitance : C_t = 0.7 pF typ.
- Photodetectable area : 50 μm dia.
- High multiplication ratio : M = 40 typ.
- High cut-off frequency : $f_c \cdot G$ = 30 typ.

Package Dimensions

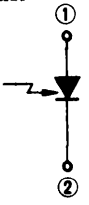


① Anode
② Cathode

(Unit : mm)

CX-type

Internal Circuit



Absolute Maximum Ratings (T_C = 25°C)

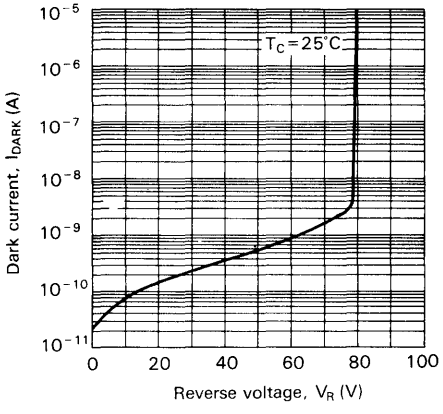
Items	Symbols	Values	Units
Forward current	I_F	10	mA
Reverse current	I_R	500	μA
Operating temperature	T_{opr}	−40 to +80	°C
Storage temperature	T_{stg}	−45 to +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

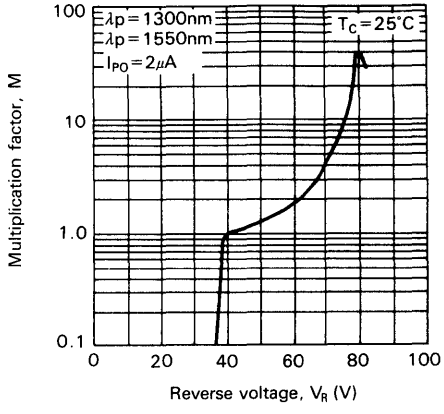
Optical and Electrical Characteristics (T_C = 25°C)

Items	Symbols	min.	typ.	max.	Units	Test conditions
Dark current	I_{DARK}		2	50	nA	$V_R = 0.9\ V_B$
Multiplicated dark current	I_{DM}		0.5	5	nA	M = 1
Capacitance	C_t		0.7	1.0	pF	f = 1 MHz, $V_R = 0.9\ V_B$
Sensitivity	S_1	0.73	0.85		mA/mW	λ_p = 1300 nm
	S_2		0.9		mA/mW	λ_p = 1550 nm
Breakdown voltage	V_B	60	80	100	V	I_{DARK} = 100 μA
Cut-off frequency	f_c	1			GHz	M = 5
		1				M = 10
			1			M = 30
						λ_p = 1300 nm, R_L = 50 Ω, Output: 500 kHz −3 dB
Excess noise factor	F		5			λ_p = 1300 nm, M = 10
	x		0.7			f = 100 MHz, B = 10 MHz, I_{PO} = 2 μA
Maximum multiplication factor	M_m	30	40			λ_p = 1300 nm, I_{PO} = 2 μA

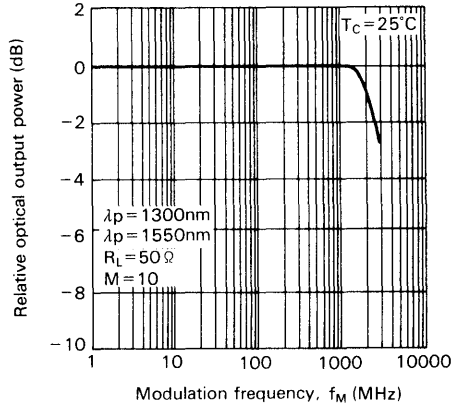
Dark Current vs. Reverse Voltage



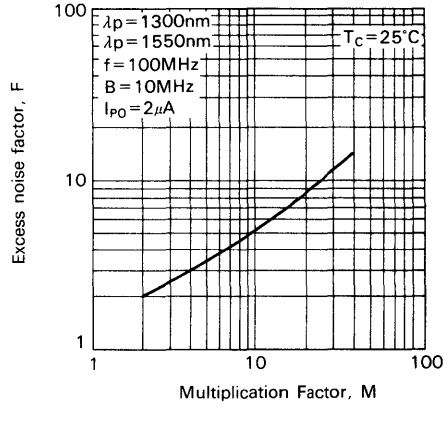
Multiplication Factor vs. Reverse Voltage



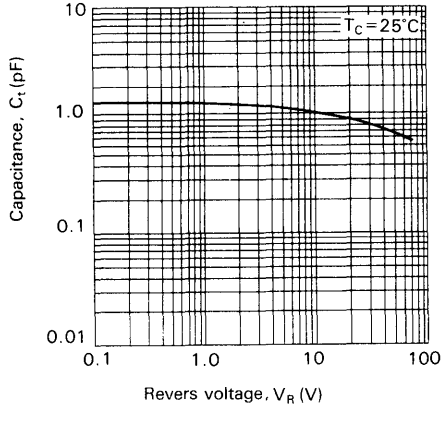
Frequency Response



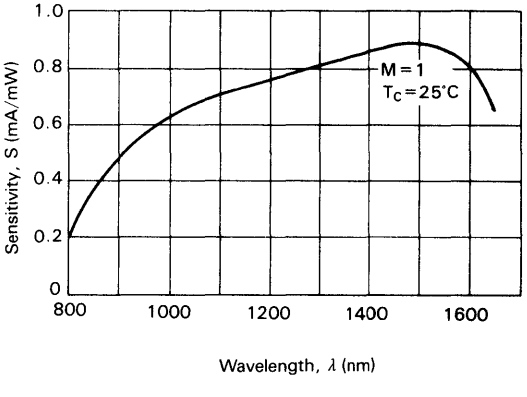
Excess Noise Factor vs. Multiplication Factor



Capacitance vs. Reverse Voltage



Sensitivity vs. Wavelength



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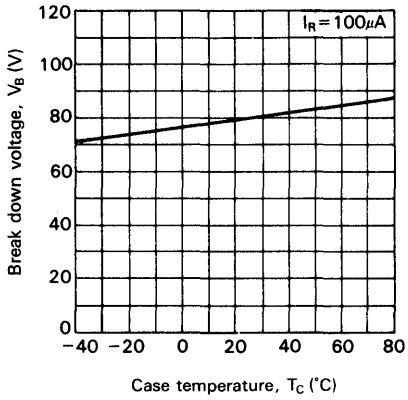
Break Down Voltage vs.
Case Temperature



Section Seven

Devices for Cellular Radio Applications

The absolute maximum ratings referenced in the data sheet sections of this manual are limiting values, to be applied individually and beyond which operation of the described circuits may be impaired. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the circuit's reliability.

The "Electrical Characteristics" of the circuits described in this manual are for reference only.

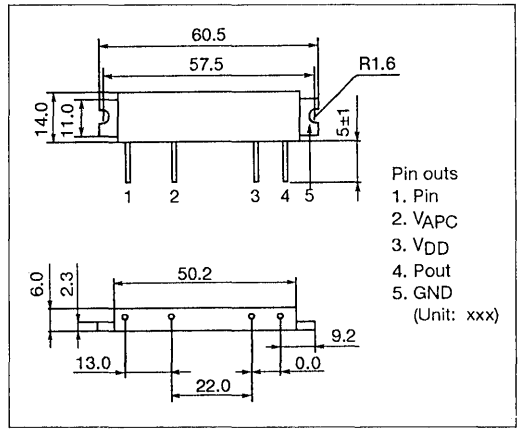
PF0010

MOS FET Power Amplifier
UHF BAND 820 ~ 850 MHz

■ FEATURES

- Included input and output matching circuit
- Easy to control output power
- Superior to stability at load mismatching

■ OUTLINE DRAWING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

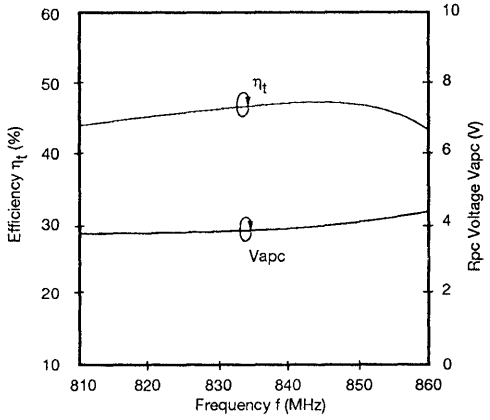
Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	17	V
Maximum Circuit Current	I_D	3.0	A
APC Voltage	V_{APC}	± 8	V
Maximum Input Power	P_{in}	20	mW
Operating Maximum Case Temperature	$T_{C(op)}$	-40 ~ +100	°C
Storage Temperature	T_{stg}	-45 ~ +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

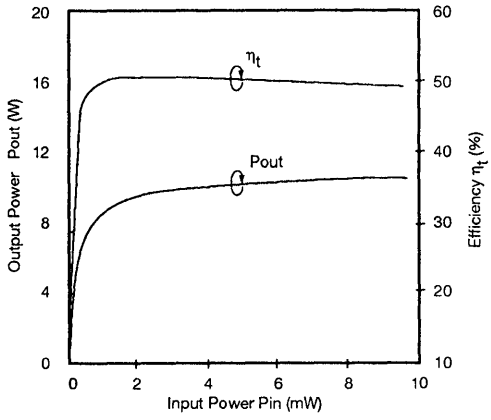
■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD} = 17V, V_{APC} = 0	—	—	500	μA
Total Efficiency	η_T	f = 820, 850 MHz, P_{in} = 2 mW, V_{DD} = 12.5V, P_{out} = 6W (at APC Control) $Z_{in} = Z_{out}$ = 50 Ω	35	40	—	%
2nd Harmonic Distortion	2nd H.D.		—	-50	-30	dB
3rd Harmonic Distortion	3rd H.D.		—	-50	-30	dB
Input VSWR	VSWR(in)		—	1.5	3.0	—
Output VSWR	VSWR(out)		—	1.5	—	—
Stability	—	V_{DD} = 12.5V, P_{in} = 2 mW, f = 820 MHz, P_{out} = 6W (at APC Control), R_g = 50 Ω, Output VSWR ≒ ∞ All Phase, t = 20 sec	No Parastic Oscillation			—

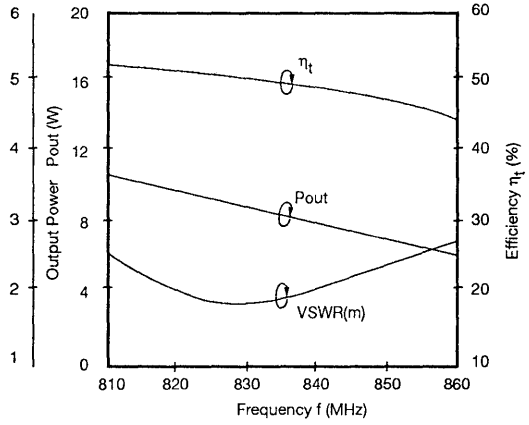
P1-2mW, Vdd-12.5V, Po-6W



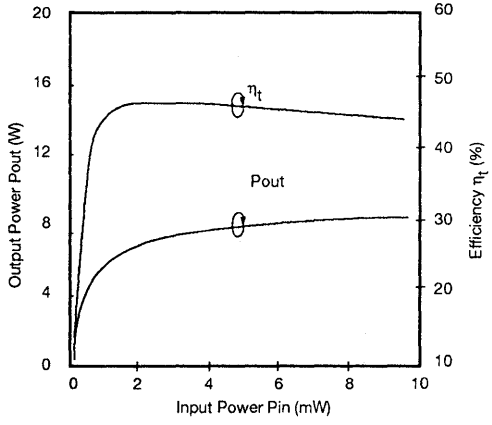
f-820MHz, Vdd-12.5V, Vapc 1-4V



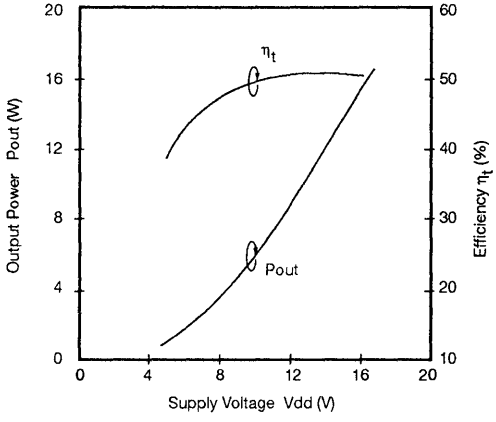
P1-2mW, Vdd-12.5V, Vapc 1-4V



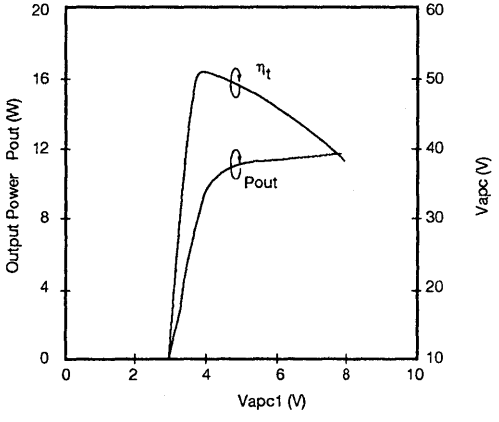
f-850MHz, Vdd-12.5V, Vapc 1-4V



f-820MHz, P1-2mW, Vapc1-4V



f-820MHz, P1-2mW, Vdd-12.5V



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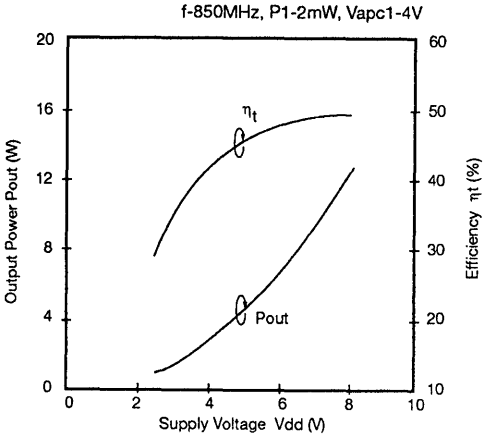
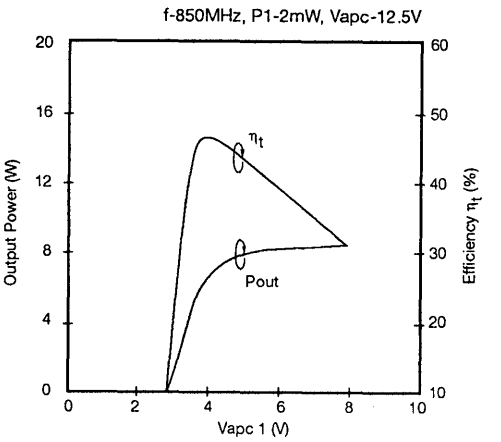
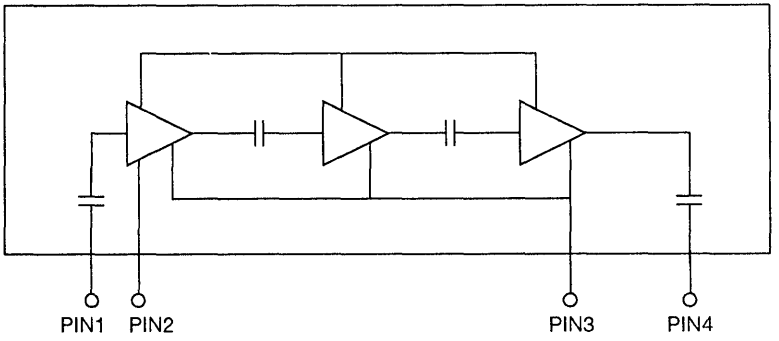
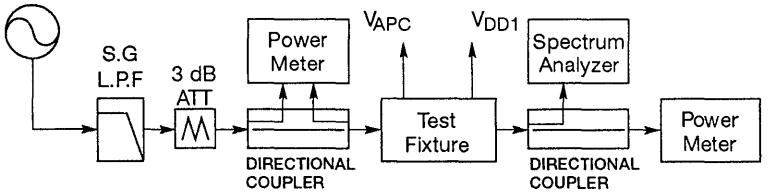




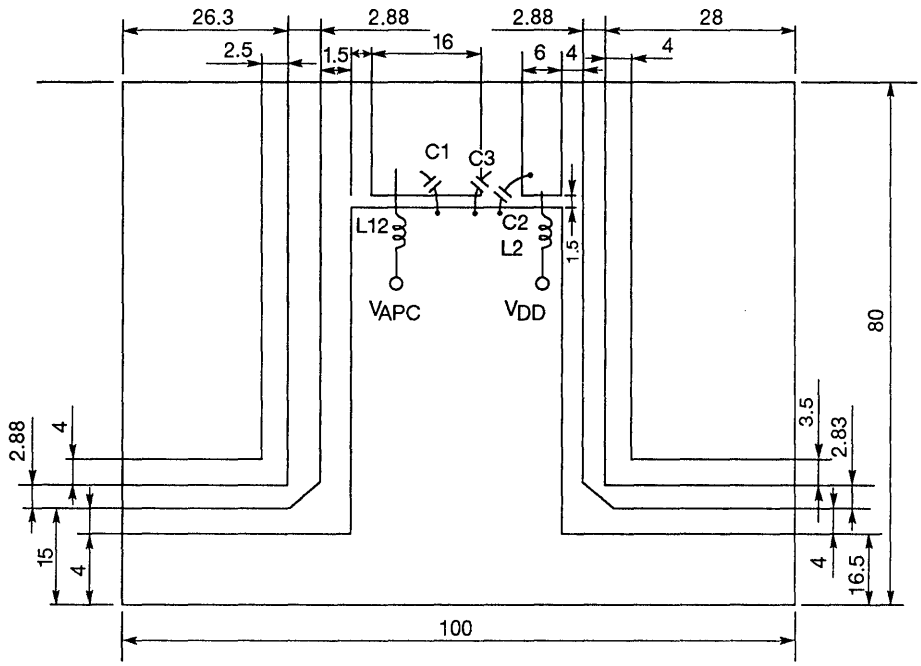
■ INTERNAL DIAGRAM



■ TEST SYSTEM DIAGRAM

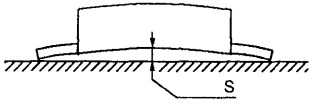


• **Test Fixture Pattern**



Grass Epoxy Double sided P.C.B.
(t = 1.6 mm, εr = 4.8)
Unit: mm
$C_1 = C_2 = 0.01\ \mu F$ (Ceramic Chip Capacitor)
$C_3 = 10\ \mu F$ (Aluminium Electrolyte Capacitor)
$L_1 = L_2$: BL02RN1-R62 (Manufacturer: MURATA) or equivalent (Ferrite Bead Inductor)

• **Mechanical Characteristics**

Item	Conditions	Spec.
Torque for screw up the heatsink flange	M3 Screw-Bolts	4 ~ 6 kg/cm
Warp size of the heatsink flange: S		S = O +0.3/-0 mm

Note for Use

1. Unevenness and distortion at the surface of the heatsink attached PF0010 should be less than 0.05 mm.
2. It should not be existed any dust between PF0010 and heatsink.
3. PF0010 should be separated from PCB more than 1.5 mm.
4. Soldering temperature and soldering time should be less than 230°C, 10 sec. (Soldering position spaced from the root point of the lead frame: 2 mm).
5. Recommendation of thermal joint compounds is TYPE G746 (Manufacturer: Shin-Etu Chemical, Co., Ltd.) or equivalent.
6. To protect devices from elecro-static damage, soldering iron, measuring-equipment and human body etc. should be grounded.

PF0015

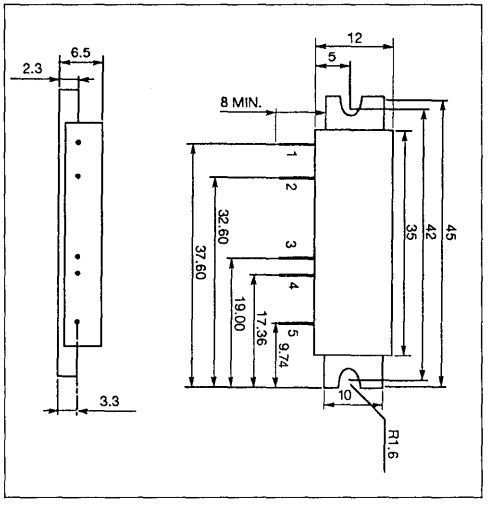
MOS FET Power Amplifier Module for Handy Mobile Phone

MOS FET Power Amplifier
FOR AMPS 824 ~ 849 MHz

■ FEATURES

- Small outline 12 × 45 × 6.5 mm^3
- Low voltage operation 6V
- Low power control current 300 μA
- High stability load VSWR ≥ 20

■ OUTLINE DRAWING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

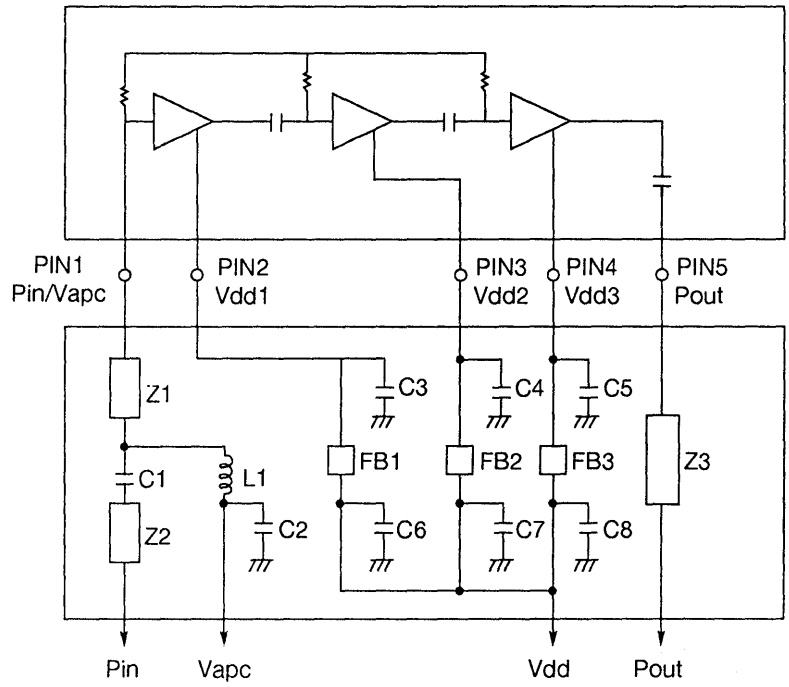
Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	12	V
Supply Current	I_{DD}	2	A
APC Voltage	V_{APC}	± 8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	$T_{C(op)}$	-30 ~ +100	°C
Storage Temperature	T_{stg}	-30 ~ +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

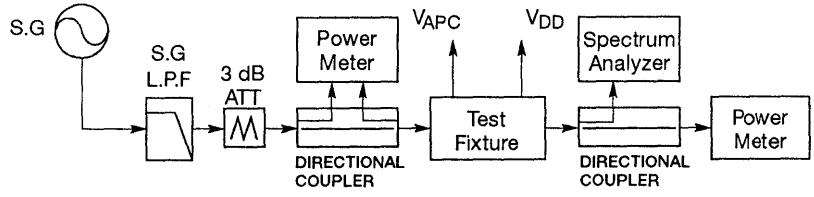
■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	$V_{DD1} = V_{DD2} = V_{DD3}$ = 12V, V_{apc} = 0V	—	—	100	μA
Total Efficiency	η_T	f = 824, 849 MHz, P_{in} = 1 mW, $V_{DD1} = V_{DD2} = V_{DD3}$ = 6V, P_{out} = 1.2W (at APC Control), $Z_{in} = Z_{out}$ = 50 Ω	35	40	—	%
2nd Harmonic Distortion	2nd H.D.		—	-40	-30	dB
3rd Harmonic Distortion	3rd H.D.		—	-50	-30	dB
Input VSWR	VSWR(in)		—	1.8	3	—
Output VSWR	VSWR(out)		—	2	—	—
Stability	—	$V_{DD1} = V_{DD2} = V_{DD3}$ = 6V, P_{in} = 1 mW, f = 824 MHz, R_g = 50 Ω, P_{out} = 1.2W (at APC Control), Output VSWR = 20 All Phases, t = 20 sec	No Parastic Oscillation			—

■ TEST SYSTEM DIAGRAM



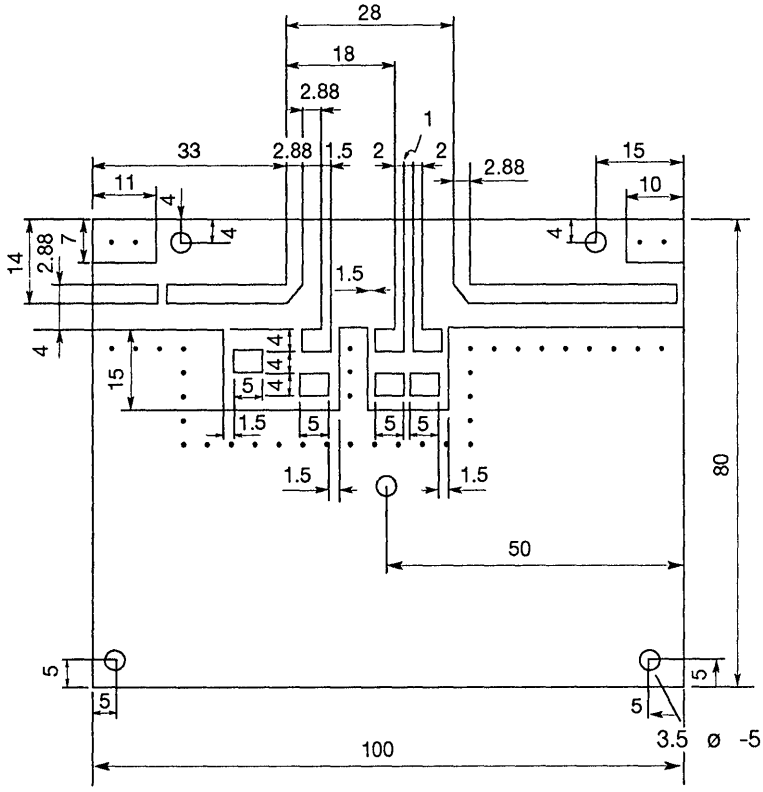
C_1 = 0.02 μF Ceramic Chip
C_2, C_3, C_4, C_5 = 0.01 μF Ceramic Dip
C_6, C_7, C_8 = 10 μF Tantalum
L_1 = RFC 1mm ϕ, 15 turns
FB = Ferrite Bead BL01RN1-A62-001 (MURATA) or equivalent
Z_1, Z_2, Z_3 = 50 Ω Microstrip Line



Output power P_{out} is defined at the root point of the module output pin P_{out}. The coefficient of output power loss in the PCB output line Z3 is shown below.

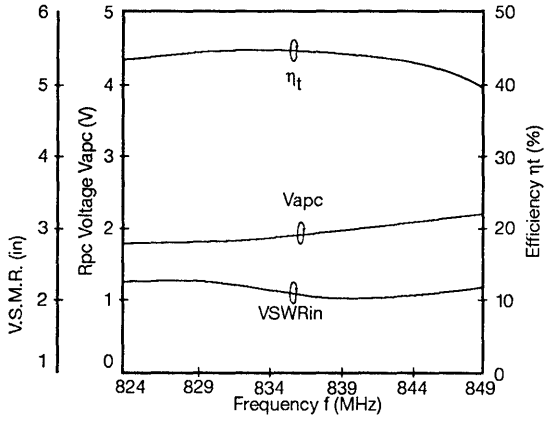
$$1/S_{21})^2 = 1/(0.9805)^2 = 1.04$$

■ TEST FIXTURE PATTERN

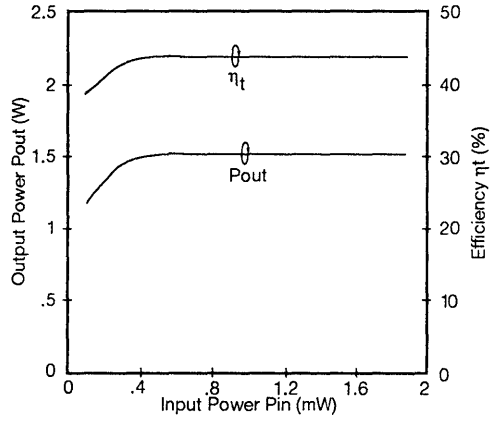


Grass Epoxy Double Sided PCB
(t = 1.6 mm, ϵr = 4.8)

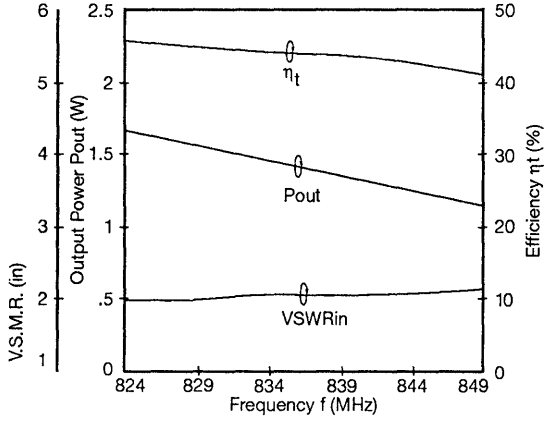
P1-1mW, Vdd-6V, Pout-1.2W, Tc-25°C



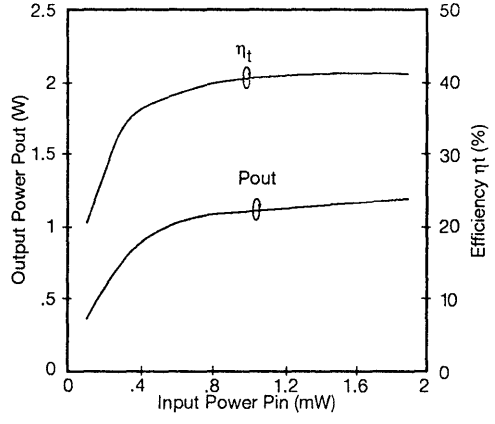
f-824MHz, Vdd-6V, Vapc-2V, Tc-25°



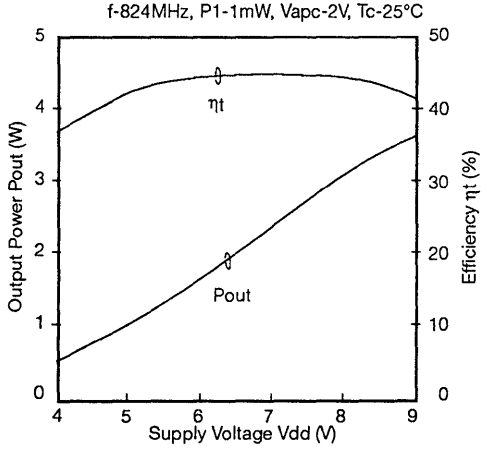
P1-1mW, Vdd-6V, Vapc-2V, Tc-25°C



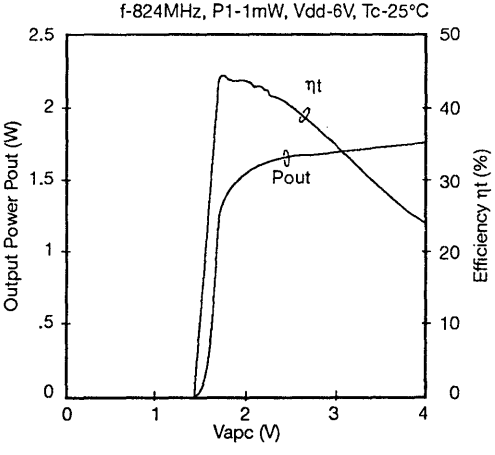
f-849MHz, Vdd-6V, Vapc-2V, Tc-25°C



f-824MHz, P1-1mW, Vapc-2V, Tc-25°C



f-824MHz, P1-1mW, Vdd-6V, Tc-25°C



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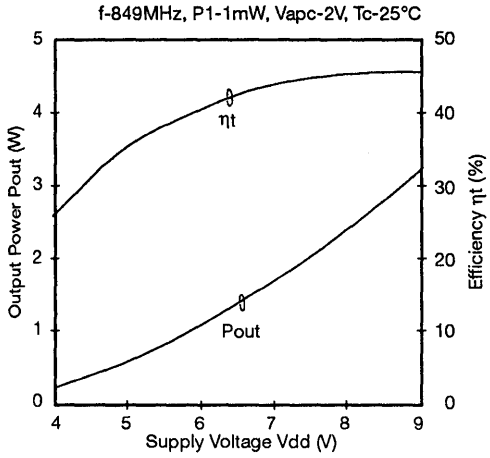
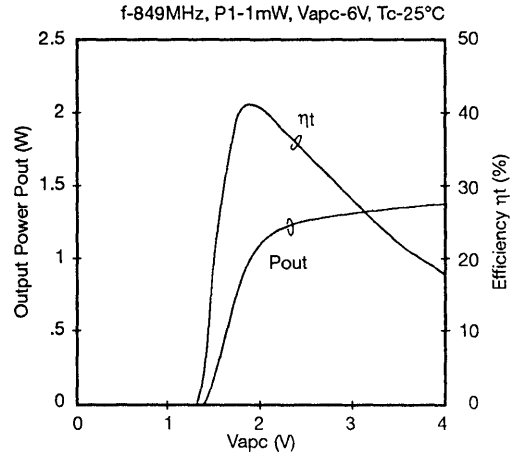
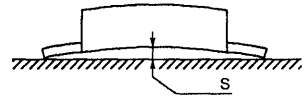




• Mechanical Characteristics

Item	Conditions	Spec.
Torque for screw up the heatsink flange	M3 Screw-Bolts	4 ~ 6 kg/cm
Warp size of the heatsink flange: S		S = O +0.3/-0 mm

Note for Use

1. Unevenness and distortion at the surface of the heatsink attached PF0015 should be less than 0.05 mm.
2. It should not be existed any dust between PF0015 and heatsink.
3. PF0015 should be separated from PCB more than 1.5 mm.
4. Soldering temperature and soldering time should be less than 230°C, 10 sec. (Soldering position spaced from the root point of the lead frame: 2 mm).
5. Recommendation of thermal joint compounds is TYPE G746 (Manufacturer: Shin-Etu Chemical, Co., Ltd.) or equivalent.
6. To protect devices from elecro-static damage, soldering iron, measuring-equipment and human body etc. should be grounded.

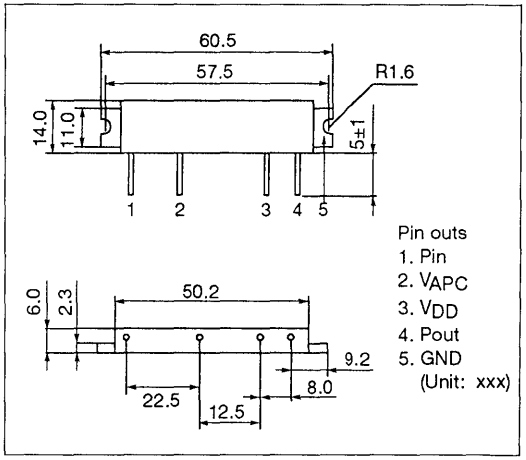
PF0020

MOS FET Power Amplifier
UHF BAND 820 ~ 850 MHz

■ FEATURES

- Included input and output matching circuit
- Easy to control output power
- Superior to stability at load mismatching

■ OUTLINE DRAWING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	17	V
Maximum Circuit Current	I_D	3.0	A
APC Voltage	V_{APC}	± 8	V
Maximum Input Power	P_{in}	20	mW
Operating Maximum Case Temperature	$T_{C(op)}$	-40 ~ +100	°C
Storage Temperature	T_{stg}	-45 ~ +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD} = 17V, V_{APC} = 0	—	—	500	μA
Total Efficiency	η_T	f = 820, 850 MHz, P_{in} = 2 mW, V_{DD} = 12.5V, P_{out} = 6W (at APC Control) $Z_{in} = Z_{out}$ = 50 Ω	35	40	—	%
2nd Harmonic Distortion	2nd H.D.		—	-50	-30	dB
3rd Harmonic Distortion	3rd H.D.		—	-50	-30	dB
Input VSWR	VSWR(in)		—	1.5	3.0	—
Output VSWR	VSWR(out)		—	1.5	—	—
Stability	—	V_{DD} = 12.5V, P_{in} = 2 mW, f = 820 MHz, P_{out} = 6W (at APC Control), R_g = 50 Ω, Output VSWR ≒ ∞ All Phase, t = 20 sec	No Parastic Oscillation			—

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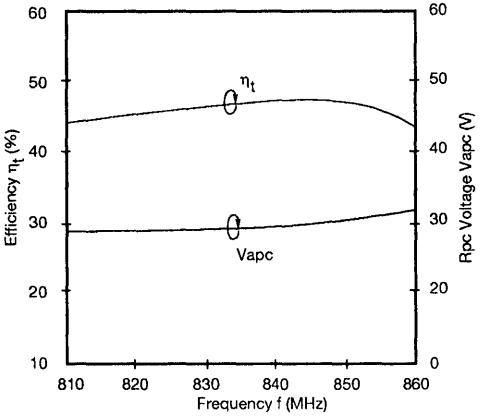
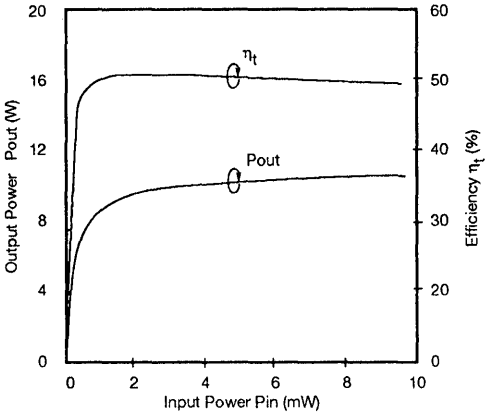
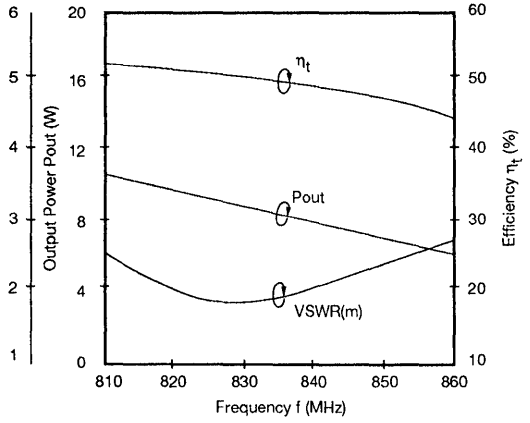
P1-2mW, Vdd-12.5V, Po-6W



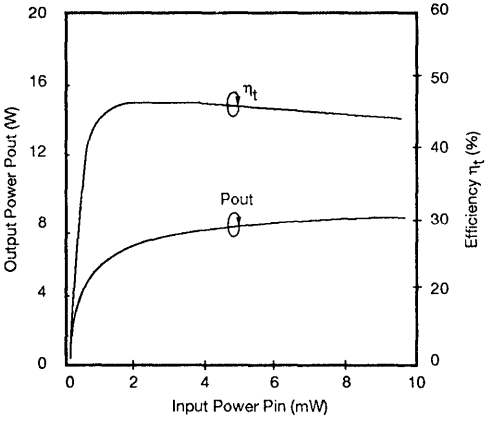
F-820MHz, Vdd-12.5V, Vapc 1-4V



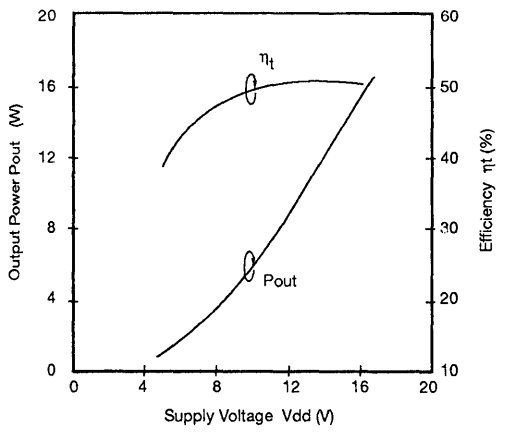
P1-2mW, Vdd-12.5V, Vapc1-4V



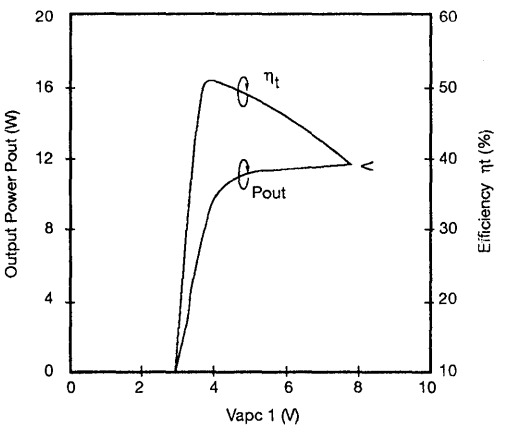
f-850MHz, Vdd-12.5V, Vapc1-4V

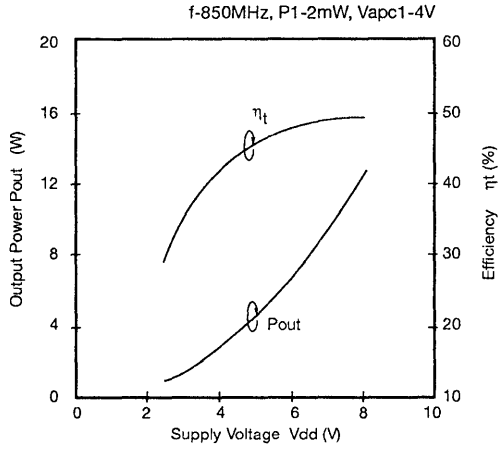


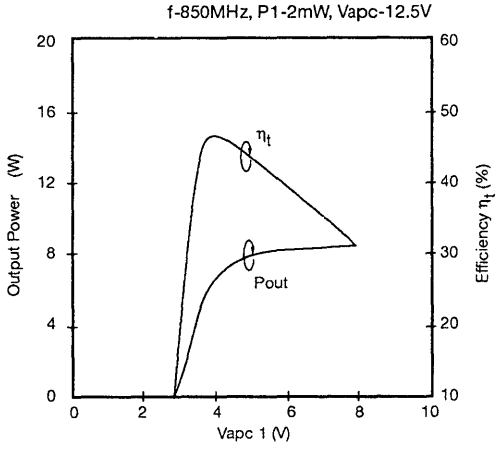
f-820MHz, P1-2mW, Vapc1-4V



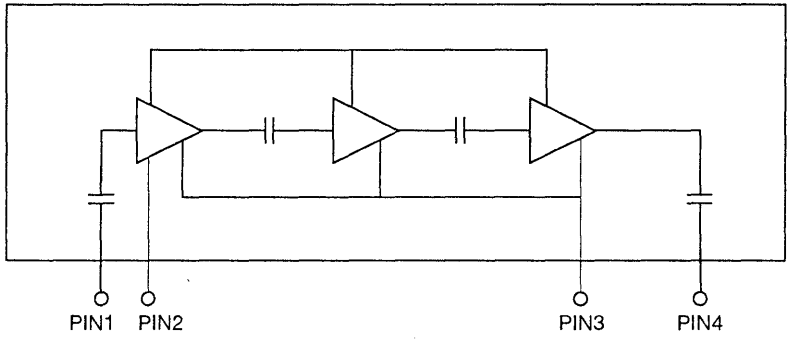
f-820MHz, P1-2mW, Vdd-12.5V



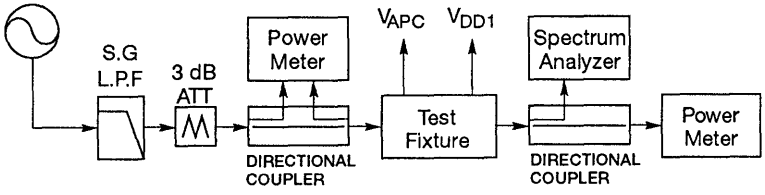




■ INTERNAL DIAGRAM



■ TEST SYSTEM DIAGRAM



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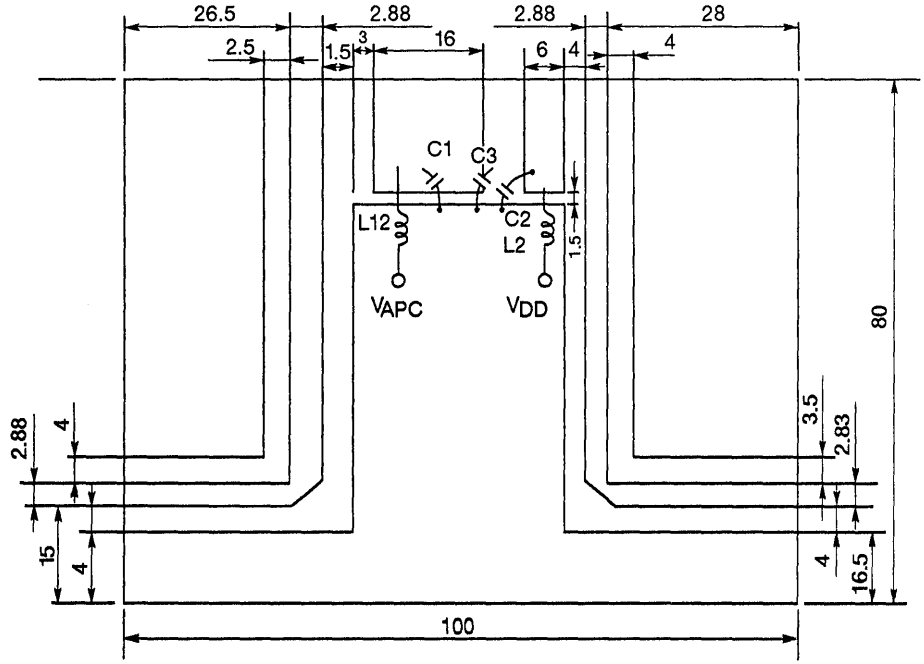
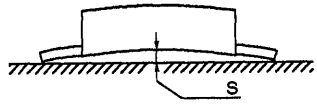
• **Test Fixture Pattern**



Grass Epoxy Double sided P.C.B.
(t = 1.6 mm, εr = 4.8)
Unit: mm
$C_1 = C_2 = 0.01\ \mu F$ (Ceramic Chip Capacitor)
$C_3 = 10\ \mu F$ (Aluminium Electrolyte Capacitor)
$L_1 = L_2$: BL02RN1-R62 (Manufacturer: MURATA) or equivalent (Ferrite Bead Inductor)

• **Mechanical Characteristics**

Item	Conditions	Spec.
Torque for screw up the heatsink flange	M3 Screw-Bolts	4 ~ 6 kg/cm
Warp size of the heatsink flange: S		S = O +0.3/-0 mm

Note for Use

1. Unevenness and distortion at the surface of the heatsink attached PF0020 should be less than 0.05 mm.
2. It should not be existed any dust between PF0020 and heatsink.
3. PF0020 should be separated from PCB more than 1.5 mm.
4. Soldering temperature and soldering time should be less than 230°C, 10 sec. (Soldering position spaced from the root point of the lead frame: 2 mm).
5. Recommendation of thermal joint compounds is TYPE G746 (Manufacturer: Shin-Etu Chemical, Co., Ltd.) or equivalent.
6. To protect devices from elecro-static damage, soldering iron, measuring-equipment and human body etc. should be grounded.

PF0025 Series

Product Preview

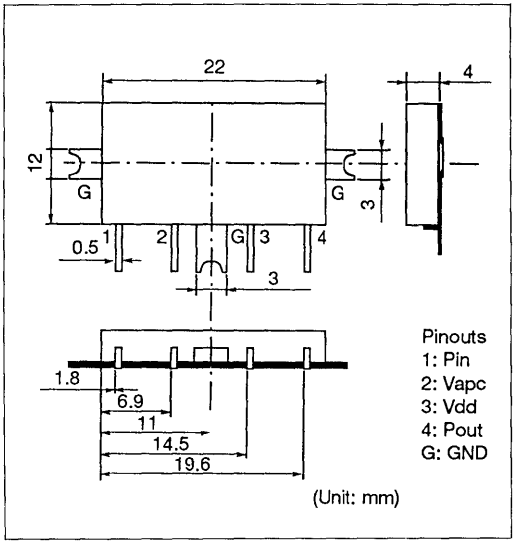
MOS FET Power Amplifier Module for Handy Mobile Phone

PF0025: For AMPS 824–849MHz
PF0026: For NMT-900 890–915MHz
PF0027: For E-TACS 872–905MHz

■ FEATURES

- Surface mounted small package 1cc, 3g
- Low voltage operation 6V (PF0026: 7.5V)
- Low power control current 300 μA
- High stability load VSWR $\geq$ 20

■ OUTLINE DRAWING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	12	V
Supply Current	I_{DD}	2	A
APC Voltage	V_{APC}	± 8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	$T_{C(op)}$	−30 ~ +100	°C
Storage Temperature	T_{stg}	−30 ~ +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition		min.	typ.	max.	Unit
		PF0025/27	PF0026				
Drain Cutoff Current	I_{DS}	V_{DD} = 12V, V_{apc} = 0V		—	—	100	μA
Total Efficiency	ηT	V_{DD} = 6V, P_{in} = 1mW, P_{out} = 1.2W, Z_{in} = Z_{out} = 50Ω	V_{DD} = 7.5V, P_{in} = 1mW, P_{out} = 2W, Z_{in} = Z_{out} = 50Ω	—	45	—	%
2nd Harmonic Distortion	2nd H.D.			—	—	-30	dB
3rd Harmonic Distortion	3rd H.D.			—	—	-30	dB
Input VSWR	VSWR(in)			—	—	3	—
Output VSWR	VSWR(out)			—	2	—	—
Stability	—	V_{DD} = 6V, P_{in} = 1mW, P_{out} = 1.2W	V_{DD} = 7.5V, P_{in} = 1mW, P_{out} = 2W	No Parastic Oscillation			—
		Output VSWR = 20 All Phases, t = 20 sec					

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PF0030 Series

Preliminary

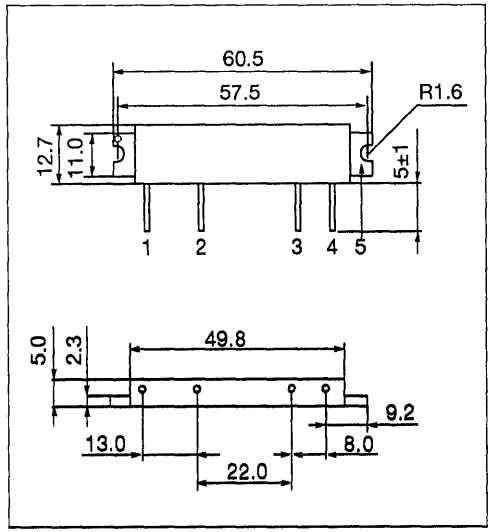
MOS FET Power Amplifier Module for Mobile Phone

PF0030: For AMPS 824–849MHz
PF0032: For E-TACS 872–905MHz

■ FEATURES

- High stability load VSWR ≒ ∞
- Low power control current 400 μA
- Thin package 5mm t

■ OUTLINE DRAWING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	17	V
Supply Current	I_{DD}	3	A
APC Voltage	V_{APC}	± 8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	$T_{C(op)}$	-30 ~ +110	°C
Storage Temperature	T_{stg}	-40 ~ +110	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

■ PIN OUTS

1: P_{in}, 2: V_{APC}, 3: V_{DD}, 4: P_{out}, 5: GND

■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD} = 17V, V_{APC} = 0V	—	—	500	μA
Total Efficiency	η_T	P_{in} = 2 mW, V_{DD} = 12.5V, P_{out} = 6W (at APC Controlled) Z_{in} = Z_{out} = 50 Ω	35	40	—	%
2nd Harmonic Distortion	2nd H.D.		—	-50	-30	dB
3rd Harmonic Distortion	3rd H.D.		—	-50	-30	dB
Input VSWR	VSWR(in)		—	1.5	3	—
Output VSWR	VSWR(out)		—	1.5	—	—
Stability	—	P_{in} = 2 mW, V_{DD} = 12.5V, P_{out} = 6W (at APC Controlled), Z_{in} = 50 Ω, Output VSWR ≒ ∞ All Phases, t = 20 sec	No Parastic Oscillation			—

PF0045 Series

Product Preview

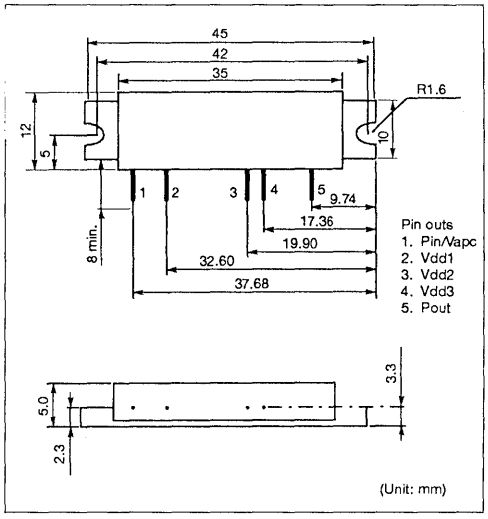
MOS FET Power Amplifier Module Mobile Phone

PF0045: For AMPS 824-849 MHz
PF0047: For E-TACS 872-905 MHz

■ FEATURES

- Light and thin package 5 g, 5.0 mm t
- Low voltage operation 6V
- Low power control current 300 μA
- High stability load VSWR ≥ 20

■ OUTLINE DRAWING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	12	V
Supply Current	I_{DD}	2	A
APC Voltage	V_{APC}	± 8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	$T_{C(op)}$	−30 ~ +100	°C
Storage Temperature	T_{stg}	−30 ~ +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD} = 12V, V_{APC} = 0V	—	—	100	μA
Total Efficiency	η_T	P_{in} = 1 mW, V_{DD} = 6V, P_{out} = 1.2W, $Z_{in} = Z_{out}$ = 50 Ω	45	48	—	%
2nd Harmonic Distortion	2nd H.D.		—	—	−30	dB
3rd Harmonic Distortion	3rd H.D.		—	—	−30	dB
Input VSWR	VSWR(in)		—	—	3	—
Output VSWR	VSWR(out)		—	2	—	—
Stability	—	P_{in} = 1 mW, V_{DD} = 6V, P_{out} = 1.2W, Z_{in} = 50 Ω, Output VSWR = 20 All Phases, t = 20 sec	No Parastic Oscillation			—

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PF0055

Preliminary

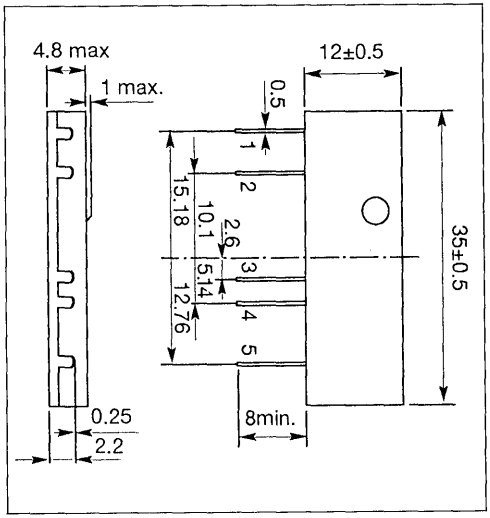
MOS FET Power Amplifier Module Handy Mobile Phone

MOS FET Power Amplifier
FOR AMPS 824 ~ 849 MHz

■ FEATURES

- Small outline 12 × 35 × 4.9 mm^3
- Low voltage operation 6V
- Low power control current 300 μA
- High stability load VSWR ≥ 20

■ OUTLINE DRAWING



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

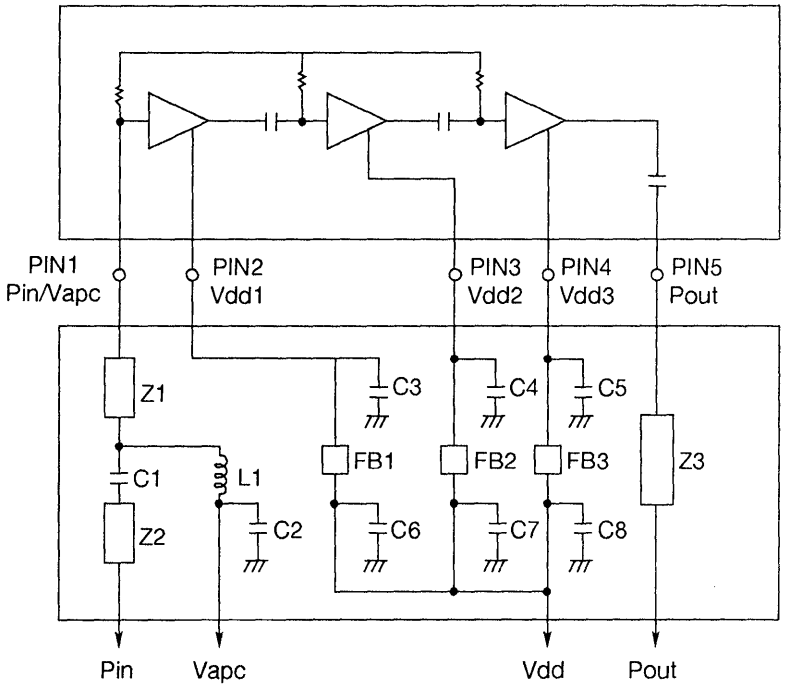
Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	12	V
Supply Current	I_{DD}	2	A
APC Voltage	V_{APC}	± 8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	$T_{C(op)}$	-30 ~ +100	°C
Storage Temperature	T_{stg}	-30 ~ +100	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

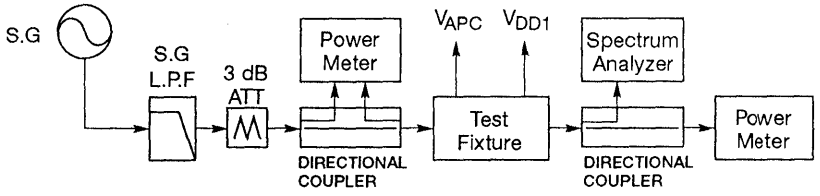
■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	$V_{DD1} = V_{DD2} = V_{DD3} = 12V$, $V_{APC} = 0V$	—	—	100	μA
Total Efficiency	ηT	f = 824, 849 MHz, P_{in} = 1 mW, $V_{DD1} = V_{DD2} = V_{DD3} = 6V$, P_{out} = 1.2W (at APC Control), $Z_{in} = Z_{out} = 50\ \Omega$	35	40	—	%
2nd Harmonic Distortion	2nd H.D.		—	-40	-30	dB
3rd Harmonic Distortion	3rd H.D.		—	-50	-30	dB
Input VSWR	VSWR(in)		—	1.8	3	—
Output VSWR	VSWR(out)		—	2	—	—
Stability	—	$V_{DD1} = V_{DD2} = V_{DD3} = 6V$, P_{in} = 1 mW, f = 824 MHz, $R_g = 50\ \Omega$, P_{out} = 1.2W (at APC Control), Output VSWR = 20 All Phases, t = 20 sec	No Parastic Oscillation			—

■ TEST SYSTEM DIAGRAM



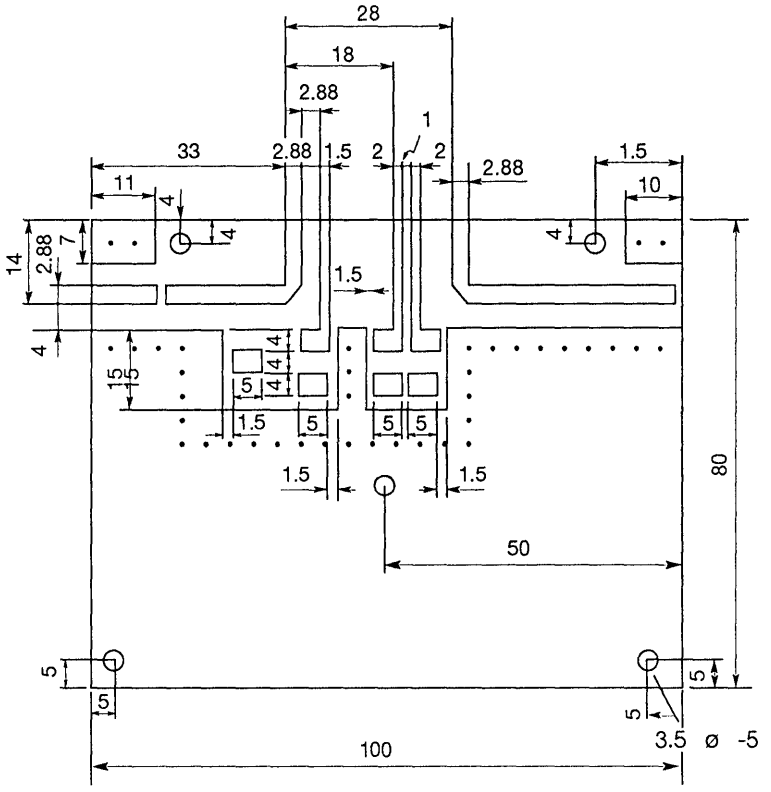
C_1 = 0.02 μF Ceramic Chip
C_2, C_3, C_4, C_5 = 0.01 μF Ceramic Dip
C_6, C_7, C_8 = 10 μF Tantalum
L_1 = RFC 1mm ϕ, 15 turns
FB = Ferrite Bead BL01RN1-A62-001 (MURATA) or equivalent
Z_1, Z_2, Z_3 = 50 Ω Microstrip Line



Output power P_{out} is defined at the root point of the module output pin P_{out}. The coefficient of output power loss in the PCB output line Z3 is shown below.

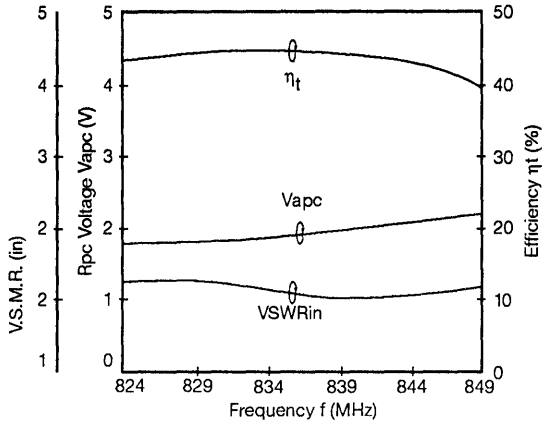
$$1/S_{21})^2 = 1/(0.9805)^2 = 1.04$$

■ TEST FIXTURE PATTERN

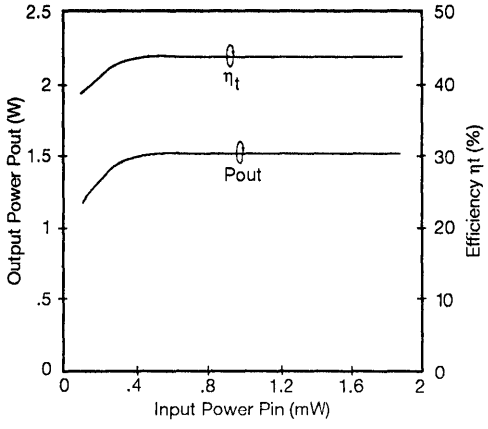


Grass Epoxy Double Sided PCB
(t = 1.6 mm, εr = 4.8)

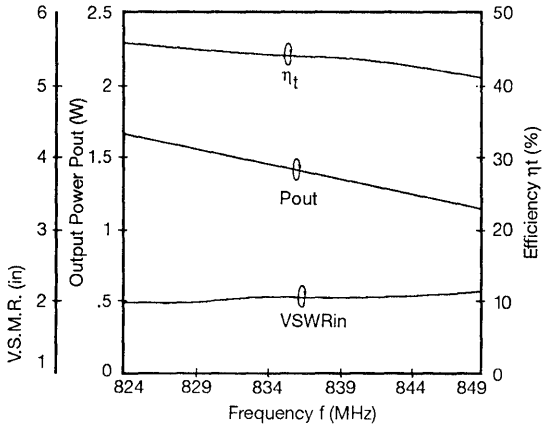
P1-1mW, Vdd-6V, Pout-1.2W, Tc-25°C



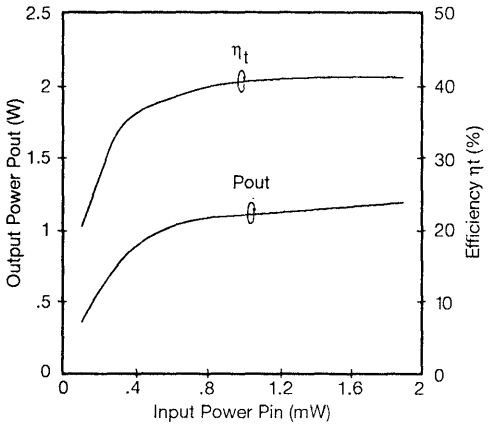
f-824MHz, Vdd-6V, Vapc-2V, Tc-25°C



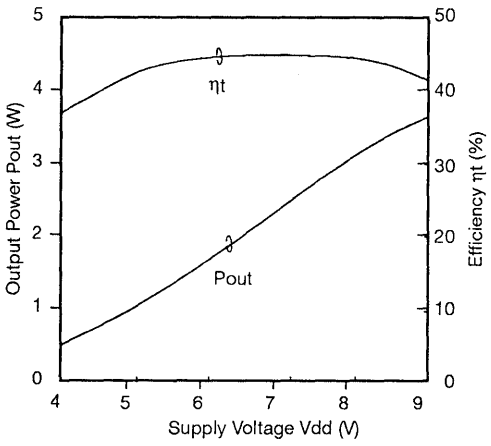
P1-1mW, Vdd-6V, Vapc-2V, Tc-25°C



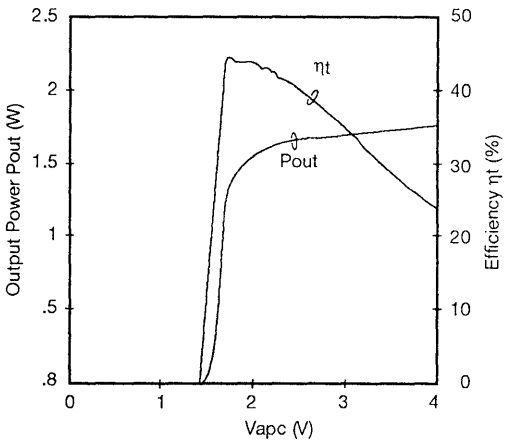
f-849MHz, Vdd-6V, Vapc-2V, Tc-25°C



f-824MHz, P1-1mW, Vapc-2V, Tc-25°C



f-824MHz, P1-1mW, Vdd-6V, Tc-25°C



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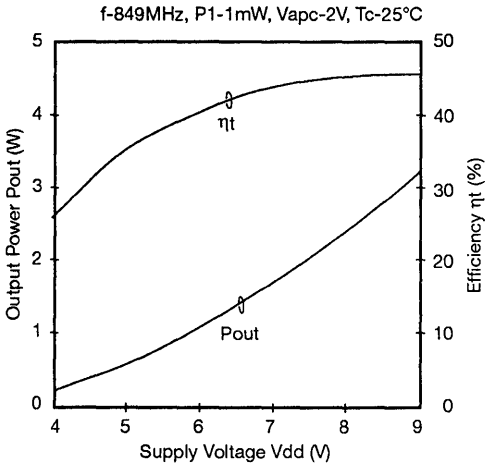
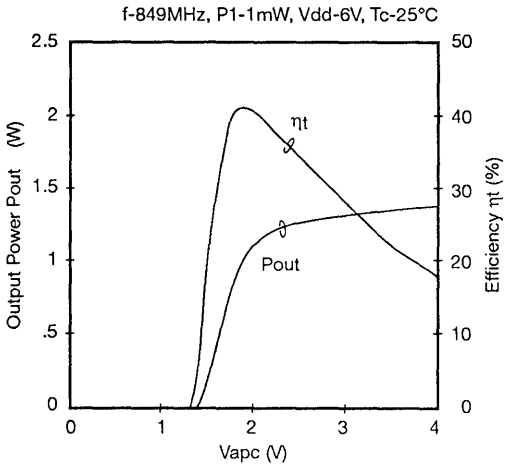
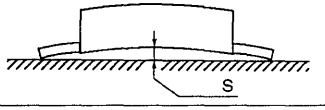




• **Mechanical Characteristics**

Item	Conditions	Spec.
Torque for screw up the heatsink flange	M3 Screw-Bolts	4 ~ 6 kg/cm
Warp size of the heatsink flange: S		S = O +0.3/-0 mm

Note for Use

1. Unevenness and distortion at the surface of the heatsink attached PF0055 should be less than 0.05 mm.
2. It should not be existed any dust between PF0055 and heatsink.
3. PF0055 should be separated from PCB more than 1.5 mm.
4. Soldering temperature and soldering time should be less than 230°C, 10 sec. (Soldering position spaced from the root point of the lead frame: 2 mm).
5. Recommendation of thermal joint compounds is TYPE G746 (Manufacturer: Shin-Etu Chemical, Co., Ltd.) or equivalent.
6. To protect devices from elecro-static damage, soldering iron, measuring-equipment and human body etc. should be grounded.

Section Eight

High Frequency Transistors for DBS and Satellite Applications

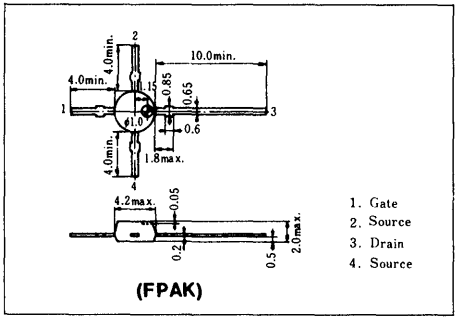
The absolute maximum ratings referenced in the data sheet sections of this manual are limiting values, to be applied individually and beyond which operation of the described circuits may be impaired. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the circuit's reliability.

The "Electrical Characteristics" of the circuits described in this manual are for reference only.

2SK457

GaAs N-channel MES FET
SHF CONVERTER RF AMPLIFIER

■ OUTLINE DRAWING



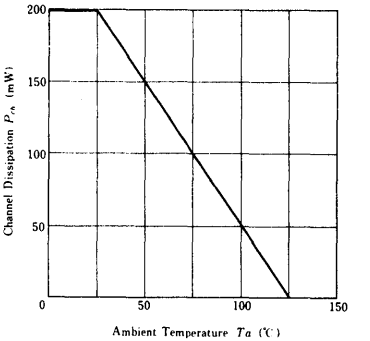
(FPAK)

■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	5	V
Gate to Source Voltage	V_{GS}	+0.5 −6.0	V
Drain Current	I_D	100	mA
Channel Dissipation	*Pch*	200	mW
Channel Temperature	*Tch*	125	°C
Storage Temperature	*Tstg*	−55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

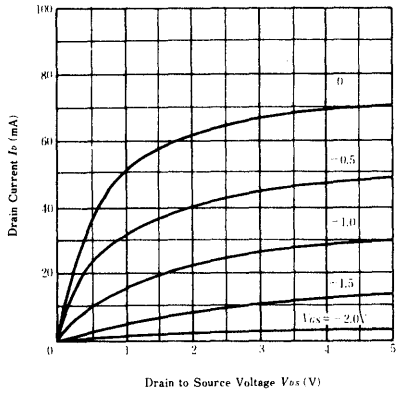
MAXIMUM CHANNEL DISSIPATION CURVE



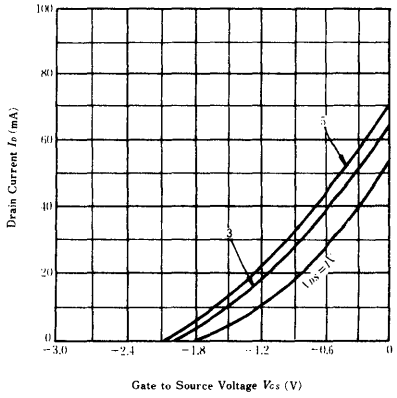
■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Leakage Current	I_{DSX}	V_{DS} = 6V, V_{GS} = −4V	–	–	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −6V, V_{DS} = 0	–	–	10	μA
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0	20	–	100	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 5V, I_D = 100 μA	–	–	−5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 5V, I_D = 20 mA, f = 1 kHz	15	35	–	mS
Power Gain	*PG*	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	–	2.1	–	dB
Minimum Noise Figure	*NF*	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	–	10	–	dB

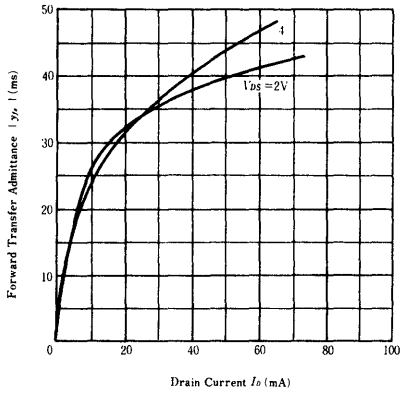
TYPICAL OUTPUT CHARACTERISTICS



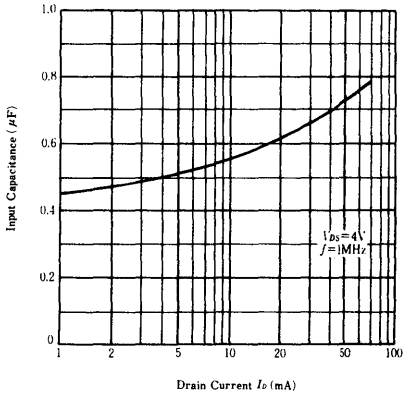
TYPICAL TRANSFER CHARACTERISTICS



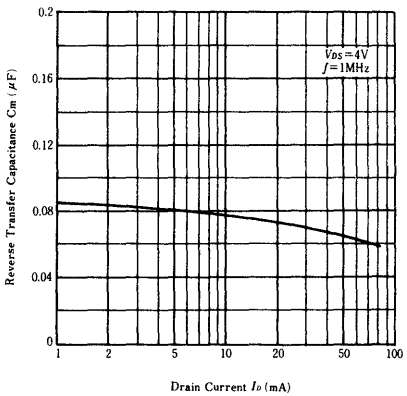
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



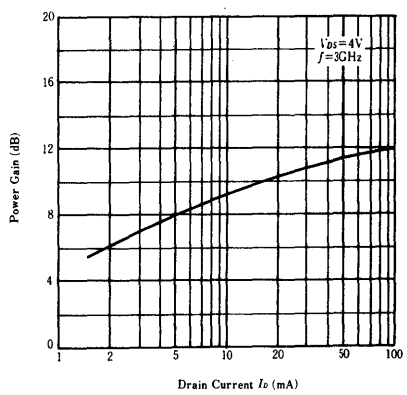
INPUT CAPACITANCE VS. DRAIN CURRENT



REVERSE TRANSFER CAPACITANCE VS.DRAIN CURRENT



POWER GAIN VS. DRAIN CURRENT



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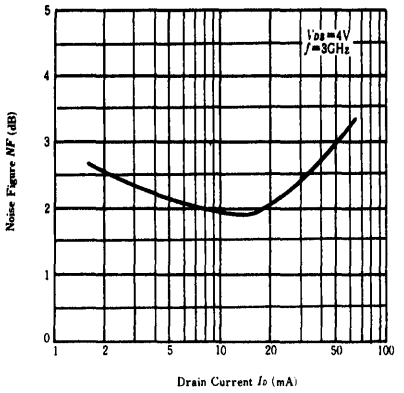
NOISE FIGURE VS. DRAIN CURRENT



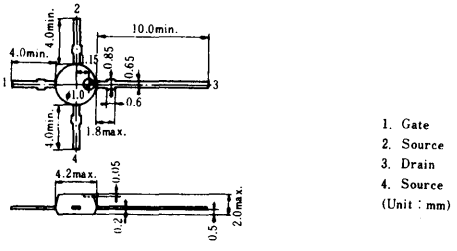
S PARAMETERS (V_{DS}=4V, I_D=20mA)

f	Return Loss		Transfer Loss		Transfer Loss		Return Loss	
	Input (S_{11})		Forward (S_{21})		Reverse (S_{12})		Output (S_{22})	
MHz	Ratio	Angle	Ratio	Angle	Ratio	Angle	Ratio	Angle
500	0.9656	−10.9	2.9479	165.8	0.0182	87.2	0.6394	− 3.6
1,000	0.9097	−21.8	2.8546	151.8	0.0352	85.2	0.6118	− 7.7
1,500	0.8503	−32.7	2.7889	139.5	0.0501	82.8	0.5879	−12.4
2,000	0.7782	−44.8	2.6831	128.0	0.0633	81.1	0.5682	−15.1
2,500	0.6904	−53.0	2.5648	115.2	0.0763	81.4	0.5562	−16.2
3,000	0.5994	−59.7	2.4482	103.2	0.0897	83.6	0.5441	−18.2
3,500	0.4919	−72.8	2.3873	91.8	0.1080	82.6	0.5105	−16.9
4,000	0.3836	−94.1	2.3424	82.0	0.1282	82.1	0.4410	−16.1

2SK666

Single Gate GaAs FET
VHF/UHF Wide Band Amplifier

■ OUTLINE DRAWING

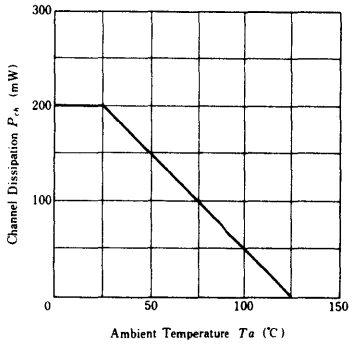


■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	4	V
Gate to Source Voltage	V_{GS}	-3	V
Drain Current	I_D	150	mA
Channel Dissipation	Pch	200	mW
Channel Temperature	Tch	125	°C
Storage Temperature	$Tstg$	-55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

MAXIMUM CHANNEL DISSIPATION CURVE

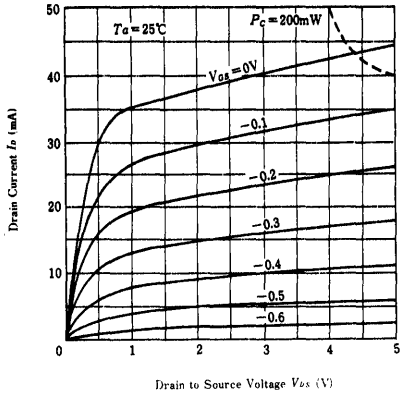


■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

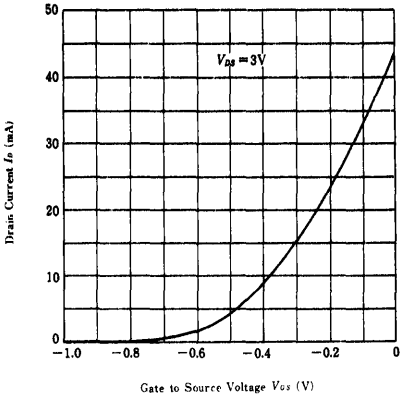
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Cutoff Current	I_{DSX}	V_{DS}=4V, V_{GS}=−1V	−	−	200	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=−3V, V_{DS}=0	−	−	−100	μA
Gate to Drain Leakage Current	I_{GSD}	V_{GS}=−7V, I_S=0 Pulse Test	−	−	−100	μA
Drain Current	I_{DSS}	V_{DS}=3V, V_{GS}=0	20	−	80	mA
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=3V, I_D=20mA, f=1kHz	50	85	−	mS
Power Gain	PG	V_{DS}=3V, I_D=20mA	8	12.5	−	dB
Noise Figure	NF	f=50MHz	−	2.8	3.5	dB
Power Gain	PG	V_{DS}=3V, I_D=20mA	6.5	8	−	dB
Noise Figure	NF	f=900MHz	−	2.7	3.5	dB

8

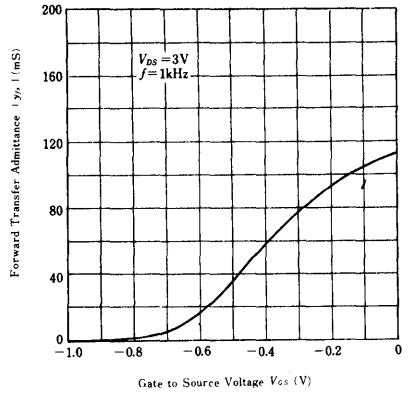
TYPICAL OUTPUT CHARACTERISTICS



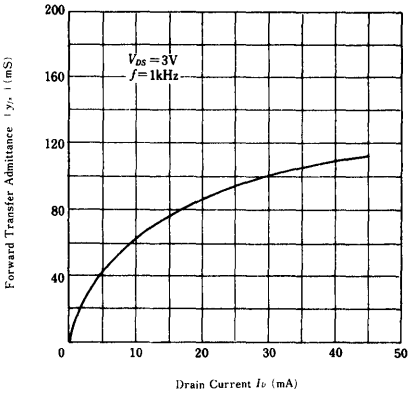
TYPICAL TRANSFER CHARACTERISTICS



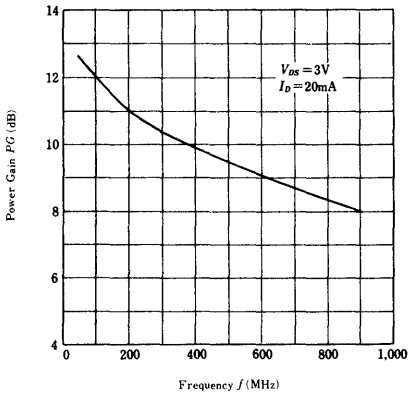
FORWARD TRANSFER ADMITTANCE VS. GATE TO SOURCE VOLTAGE



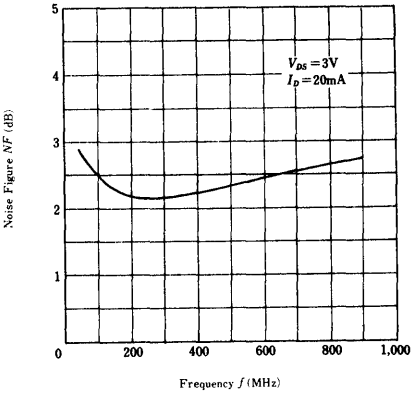
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



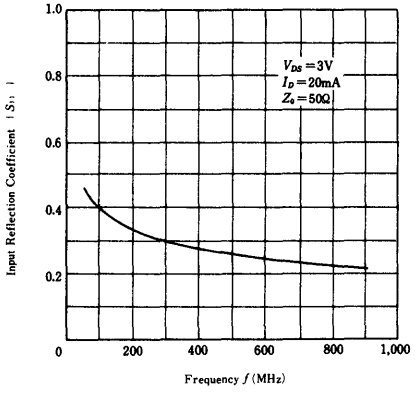
POWER GAIN VS. FREQUENCY



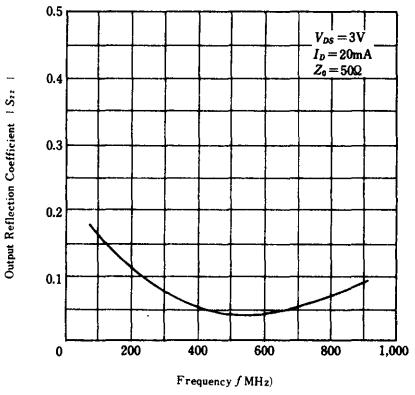
NOISE FIGURE VS. FREQUENCY



INPUT REFLECTION COEFFICIENT VS. FREQUENCY



OUTPUT REFLECTION COEFFICIENT VS. FREQUENCY



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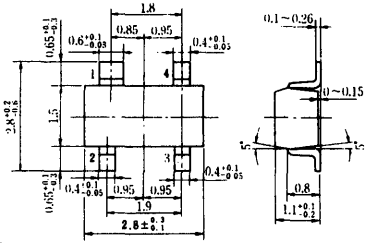
2SK668

N-Channel GaAs Single Gate MES FET
UHF/SHF Low Noise Amplifier

■ OUTLINE DRAWING



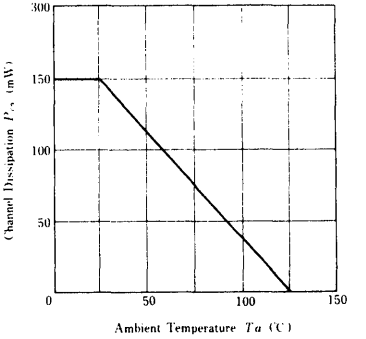
(MPAK–4)

■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	6	V
Gate to Source Voltage	V_{GS}	+0.5 −6.0	V
Drain Current	I_D	100	mA
Channel Dissipation	*Pch*	150	mW
Channel Temperature	*Tch*	125	°C
Storage Temperature	*Tstg*	−55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

MAXIMUM CHANNEL DISSIPATION CURVE



■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DSX}	V_{DS} = 6V, V_{GS} = −4V	–	–	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −6V, V_{DS} = 0	–	–	10	μA
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0, Pulse Test	20	–	100	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 5V, I_D = 100 μA	–	–	−5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 5V, I_D = 20 mA, f = 1 kHz	15	35	–	mS
Power Gain	*PG*	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	8	10	–	dB
Noise Figure	*NF*	V_{DS} = 4V, I_D = 20 mA, f = 3 GHz	–	2.5	3.5	dB

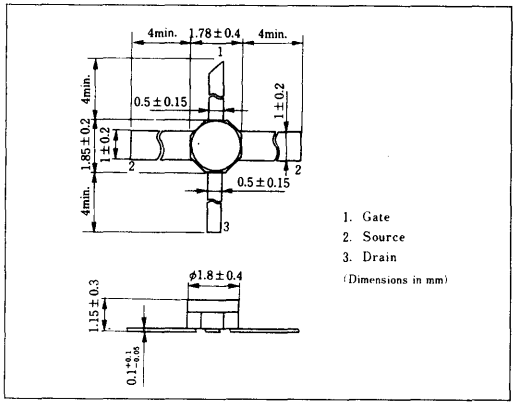
*Marking is 「IU-」

See characteristic curves of 2SK457

2SK779

GaAs N-channel MES FET
SHF Converter RF Amplifier

■ OUTLINE DRAWING

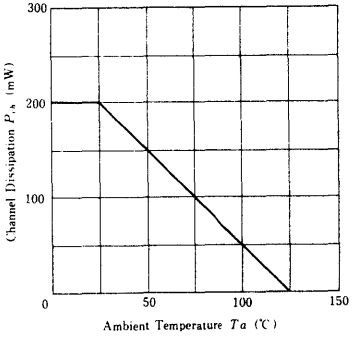


■ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	5	V
Gate to Source Voltage	V_{GS}	−6	V
Drain Current	I_D	120	mA
Channel Dissipation	*Pch*	200	mW
Channel Temperature	*Tch*	125	°C
Storage Temperature	*Tstg*	−55 ~ +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

MAXIMUM CHANNEL DISSIPATION CURVE

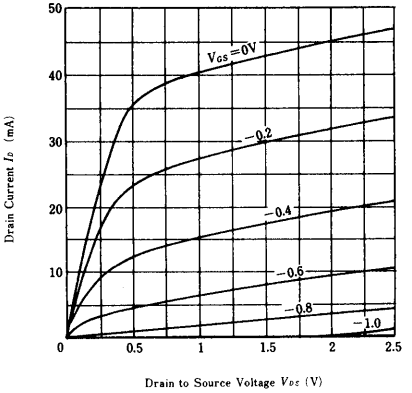


■ELECTRICAL CHARACTERISTICS (Ta = 25°C)

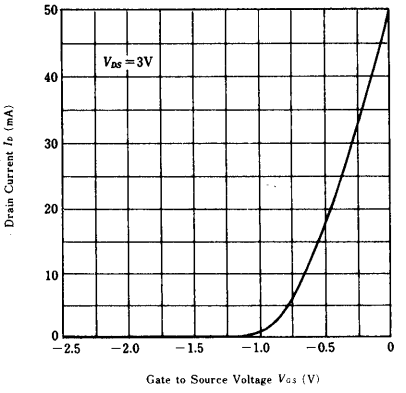
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −3V, V_{DS} = 0	–	–	−10	μA
Drain Current	I_{DSS}	V_{DS} = 3V, V_{GS} = 0	20	–	120	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 3V, I_D = 100 μA	−0.5	–	−3.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 3V, I_D = 10 mA, f = 1 kHz	30	50	–	mS
Minimum Noise Figure	*NF*	V_{DS} = 3V, I_D = 10 mA f = 12 GHz, (at NF MIN)	–	1.3	1.6	dB
Associated Gain	*Ga*		8	11	–	dB

■ S PARAMETER (Ta=25℃, V_{DS}=3V, I_D=10mA, Z=50Ω)

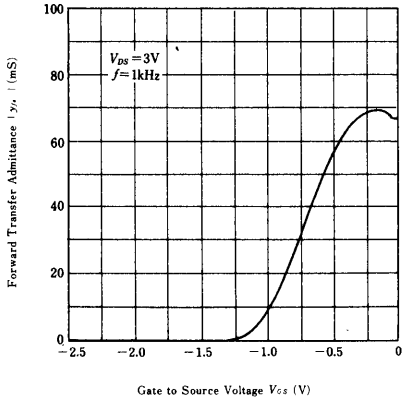
TYPICAL OUTPUT CHARACTERISTICS



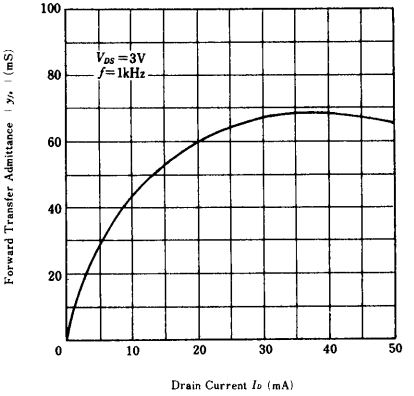
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



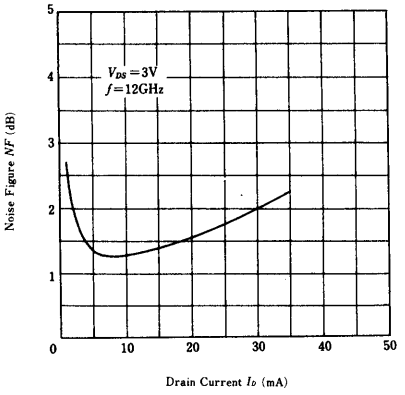
FORWARD TRANSFER ADMITTANCE VS. GATE TO SOURCE VOLTAGE



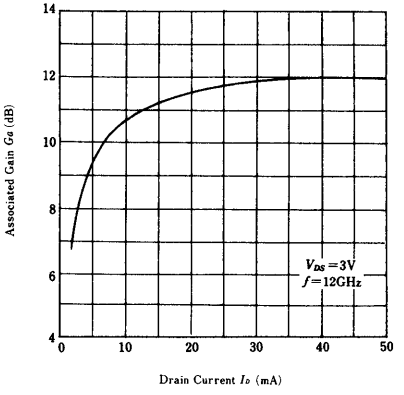
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



NOISE FIGURE VS. DRAIN CURRENT



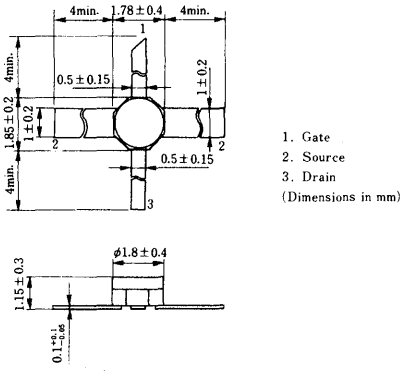
ASSOCIATED GAIN VS. DRAIN CURRENT



2SK780

GaAs N-channel MES FET
SHF Converter RF Amplifier

■ OUTLINE DRAWING

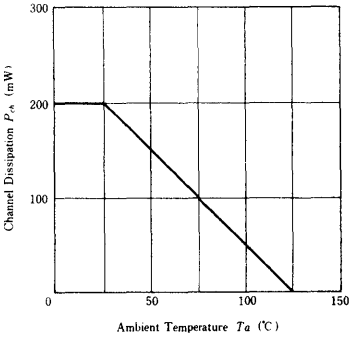


■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	5	V
Gate to Source Voltage	V_{GS}	−6	V
Drain Current	I_D	120	mA
Channel Dissipation	*Pch*	200	mW
Channel Temperature	*Tch*	125	°C
Storage Temperature	*Tstg*	−55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

MAXIMUM CHANNEL DISSIPATION CURVE

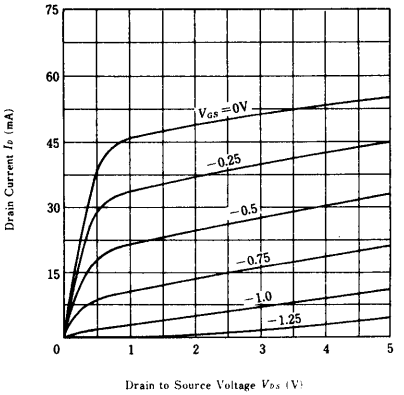


■ ELECTRICAL CHARACTERISTICS (Ta = 25°C)

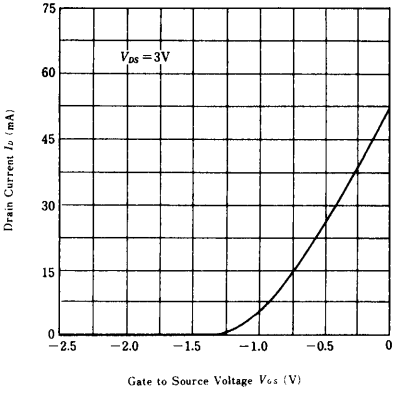
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Gate to Source Leakage Current	I_{GSS}	V_{GS} = −3V, V_{DS} = 0	–	–	−10	μA
Drain Current	I_{DSS}	V_{DS} = 3V, V_{GS} = 0	20	–	120	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 3V, I_D = 100 μA	−0.5	–	−3.5	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = 3V, I_D = 10 mA, f = 1 kHz	20	40	–	mS
Minimum Noise Figure	*NF*	V_{DS} = 3V, I_D = 10 mA f = 12 GHz, (at NF MIN)	–	1.8	2.1	dB
Associated Gain	*Ga*		8	10	–	dB

8

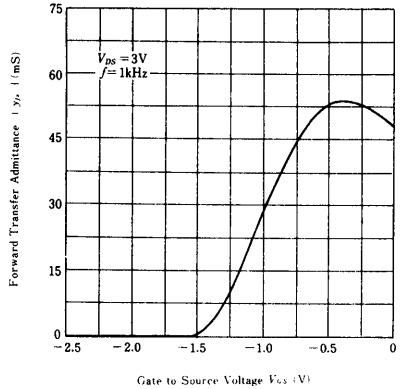
TYPICAL OUTPUT CHARACTERISTICS



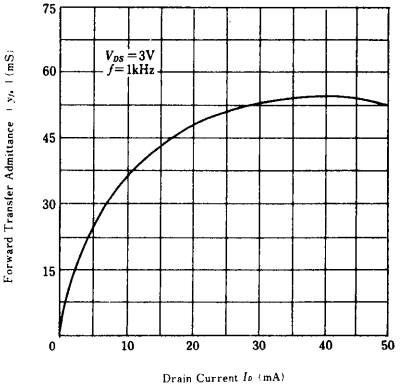
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



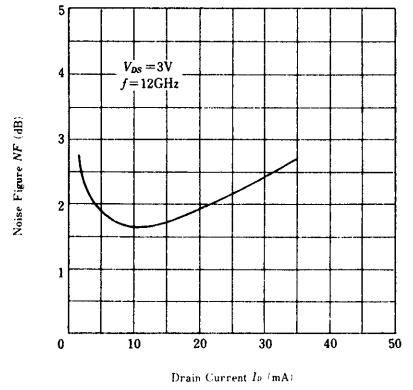
FORWARD TRANSFER ADMITTANCE VS. GATE TO SOURCE VOLTAGE



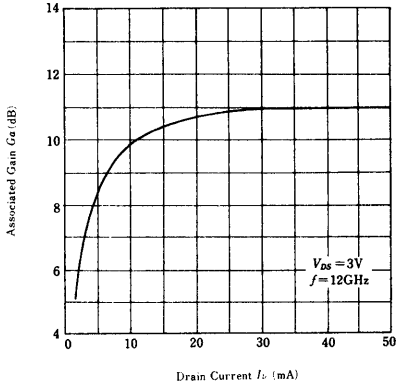
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



NOISE FIGURE VS. DRAIN CURRENT



ASSOCIATED GAIN VS. DRAIN CURRENT



■ S PARAMETER(Ta=25℃, V_{DS}=3V, I_D=10mA, Z_o=50Ω)

f(GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
2	0.950	−31.3	3.125	149.7	0.042	71.9	0.716	−16.7
4	0.838	−69.8	2.998	118.4	0.075	50.4	0.621	−35.6
6	0.742	−111.4	2.744	87.1	0.079	34.4	0.522	−61.8
8	0.708	−146.1	2.170	58.0	0.072	24.0	0.491	−92.4
10	0.722	−168.9	1.698	36.0	0.056	26.2	0.543	−116.6
12	0.690	175.1	1.248	14.3	0.048	30.8	0.577	−145.1

8

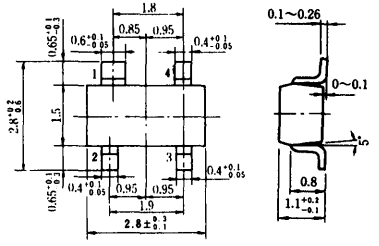
2SK1092

Preliminary

SINGLE GATE GaAs MES FET

VHF/UHF WIDE BAND AMPLIFIER

■ OUTLINE DRAWING



(MPAK-4)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	2SK1092	Unit
Drain to Source Voltage	V_{DS}	4	V
Gate to Source Voltage	V_{GS}	−3	V
Drain Current	I_D	150	mA
Channel Dissipation	P_{ch}	150	mW
Channel Temperature	T_{ch}	125	℃
Storage Temperature	T_{stg}	−55~+125	℃

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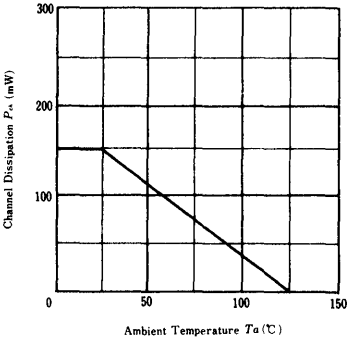
MAXIMUM CHANNEL DISSIPATION CURVE



■ ELECTRICAL CHARACTERISTICS (Ta=25℃)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DSX}	V_{DS}=4V, V_{GS}=−2V	−	−	200	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=−3V, V_{DS}=0	−	−	−100	μA
Gate to Drain Leakage Current	I_{GDO}	V_{GD}=−7V, I_S=0	−	−	−100	μA
Drain Current	I_{DSS}	V_{DS}=3V, V_{GS}=0, Pulse Test	20	−	80	mA
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS}=3V, I_D=20mA, f=1kHz	50	85	−	mS
Power Gain	PG	V_{DS}=3V, I_D=20mA, f=50MHz	8	−	−	dB
Noise Figure	NF		−	−	3.5	dB
Power Gain	PG	V_{DS}=2V, I_D=20mA, f=900MHz	6.5	−	−	dB
Noise Figure	NF		−	−	3.5	dB

*Marking is 「XE-」.

See characteristic curves of 2SK666

2SK1229

Preliminary

GaAsN-Channel HEMT

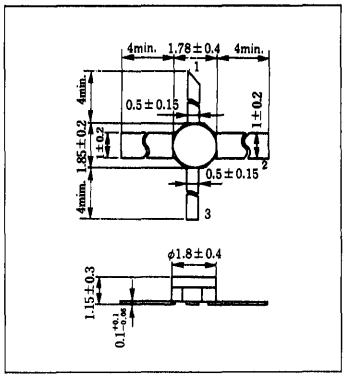
SHF Converter RF Amplifier

■ FEATURES

- Low Noise, High Gain

  NF = 1.0dB typ. Ga = 11dB typ. (f = 12GHz)

■ OUTLINE DRAWING



■ ABSOLUTE MAXMUM RATING ($Ta = 25°C$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	4	V
Gate to Source Voltage	V_{GSO}	− 3	V
Gate to Drain Voltage	V_{GDO}	− 3	V
Drain Current	I_D	60	mA
Channel Dissipation	Pch	160	mW
Channel Temperature	Tch	125	°C
Storage Temperature	$Tstg$	−55 ~ +125	°C

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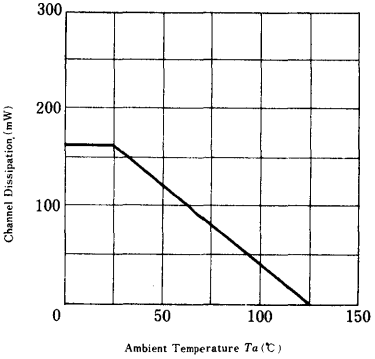
MUXIMUM CHANNEL DISSIPATION CURVE

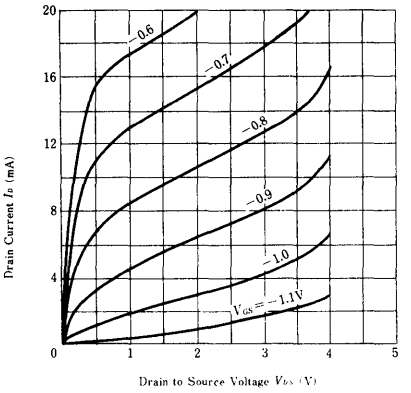


■ ELECTRICAL CHARACTERISTICS ($Ta = 25°C$)

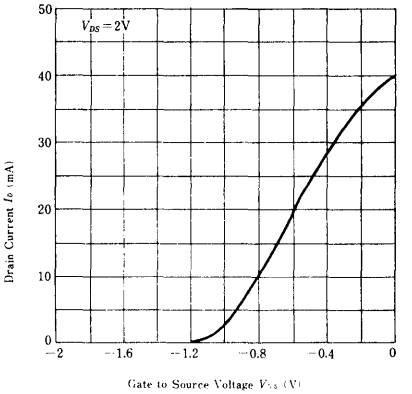
Item	Symbol	Test Condition	min.	typ.	max.	単位
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = -3$, $V_{DS} = 0$	—	—	−10	μA
Drain Current	I_{DSS}	$V_{DS} = 2$ V, $V_{GS} = 0$ (Pulse Test)	12	—	60	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 2$ V, $I_D = 100\mu$A	−0.3	—	−2.5	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	$V_{DS} = 2$ V, $I_D = 10$mA, $f = 1$kHz	30	45	—	mS
Noise Figure	NF	$V_{DS} = 2$ V, $I_D = 10$mA, $f = 12$GHz,	—	1.0	1.3	dB
Associated Gain	Ga		9	11	—	dB

8

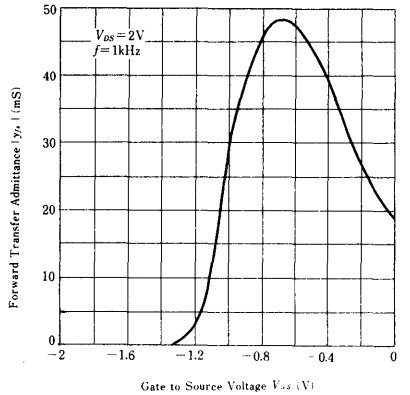
TYPICAL OUTPUT CHARACTERISTICS



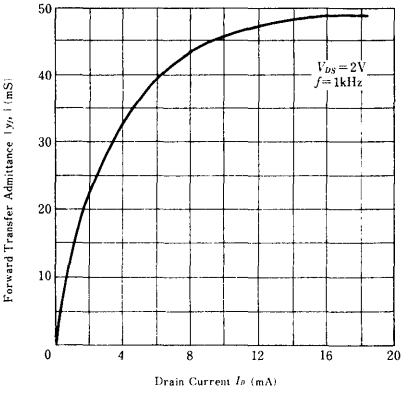
GATE TO SOURCE VOLTAGE



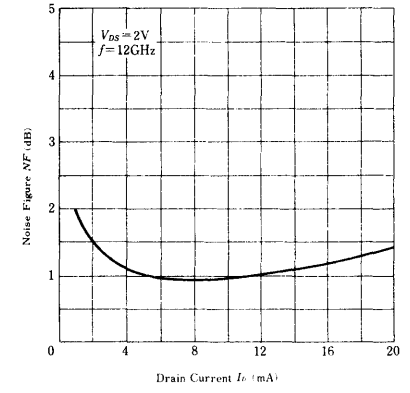
FORWARD TRANSFER ADMITTANCE VS. GATE TO SOURCE VOLTAGE



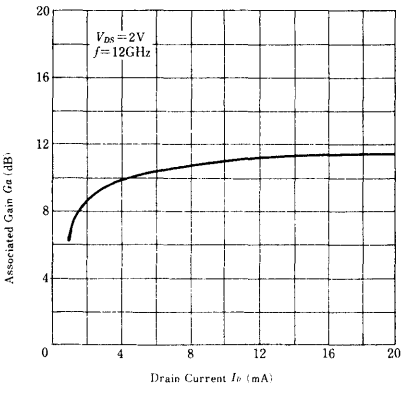
FORWARD TRANSFER ADMITTANCE VS. DRIN CURRENT



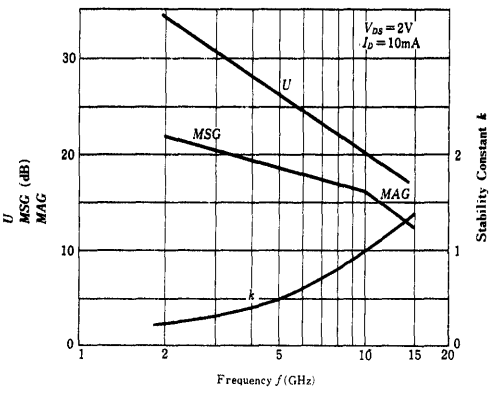
NOISE FIGURE VS. DRAIN CURRENT



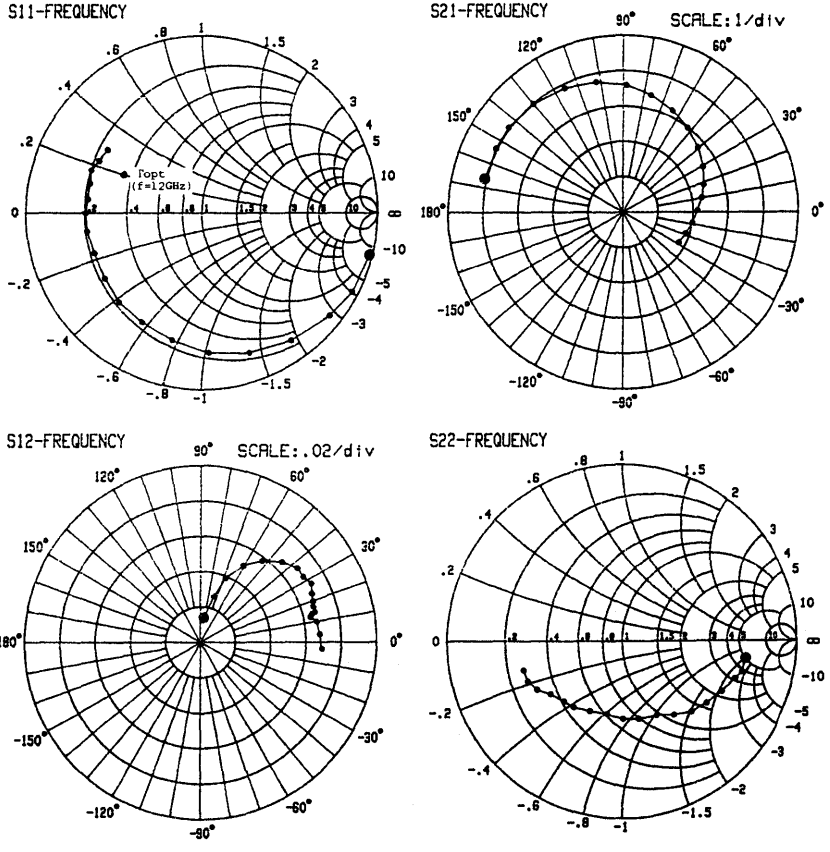
ASSOCIATED GAIN VS. DRAIN CURRENT



U, MSG, MAG, K VS. FREQUENCY



S PARAMETERS



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S-PARAMETERS ($Ta = 25°C$, $V_{DS} = 2V$, $I_D = 10mA$)

f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
1	0.983	− 13.9	4.054	166.4	0.014	82.8	0.710	− 8.0
2	0.966	− 27.6	4.034	153.6	0.027	73.3	0.706	− 14.4
3	0.933	− 38.5	4.046	143.9	0.039	68.6	0.679	− 18.1
4	0.884	− 54.7	3.990	130.0	0.050	60.7	0.634	− 26.4
5	0.838	− 71.0	3.884	115.7	0.058	52.6	0.594	− 35.9
6	0.793	− 86.8	3.754	102.0	0.065	44.4	0.561	− 45.1
7	0.739	−103.2	3.586	88.6	0.069	37.2	0.511	− 54.3
8	0.704	−118.8	3.396	76.7	0.069	32.2	0.463	− 64.7
9	0.688	−132.9	3.185	64.1	0.071	27.7	0.450	− 77.4
10	0.663	−146.0	2.992	52.4	0.069	23.3	0.440	− 89.0
11	0.651	−159.6	2.788	40.4	0.068	19.7	0.420	−101.6
12	0.660	−170.8	2.600	29.3	0.067	17.2	0.433	−114.9
13	0.663	−179.8	2.442	18.4	0.067	14.6	0.462	−126.5
14	0.653	173.2	2.272	10.2	0.065	13.9	0.472	−134.3
15	0.657	165.4	2.117	1.2	0.064	12.6	0.504	−143.9
16	0.673	159.2	2.005	− 8.5	0.067	9.8	0.556	−150.6
17	0.654	153.5	1.888	−18.4	0.068	3.7	0.581	−157.2
18	0.642	146.4	1.804	−28.2	0.069	− 3.0	0.584	−163.8

(Γopt)

Frequency (GHz)	| Γopt |	∠Γopt (deg.)
8	0.513	88.1
10	0.541	118.1
12	0.472	−154.5
14	0.477	−179.6
16	0.540	169.1
18	0.589	156.6

Section Nine

Telecommunications Glossary

TELECOMMUNICATIONS GLOSSARY

Term	Explanation
A/D (Analog to Digital) Converter	A device which converts analog wave to digital suitable form for digital processing and switching.
ADI (Alternate Digit Inversion)	Used with A law to ensure sufficient 1 → 0/0 → 1 transitions for clock extraction.
A law	Companding/encoding law mainly used in Europe.
Aliasing Noise	A distortion which occurs if the sampled signal's bandwidth is greater than half the sample rate.
AMI signal (Alternate Mark Inversion)	A pseudo-fernary signal in which successive marks are normally of alternate, + and – polarity but equal in amplitude and in which space is of zero amplitude.
Anti Aliasing Filter	A filter whose input signal band width is limited before sampling to less than half the sampling rate. This is to eliminate Aliasing Noise.
Asynchronous	State in which receive or transmit signal timings occur in the network with the same frequency and phase.
Auto Power Control (APC)	A terminal which controls output of Laser Diode.
Base-band Transmission Type	Transmission type which transmits the original forms of signals.
Baud Rate	Unit of modulating speed. One baud shows speed to modulate one element per second. This is not always same as transferred rate bit per second.
BCP (Byte Control Protocol)	A protocol in which sets of byte-wide data control the data link. One of the COP protocols.
Bit Stealing	Signalling in which least significant bit of time slots used for encoded speech are periodically used for switching information.
Blancing Network	A circuit connected bridges or Hybrids which compensate the impedance unmuching to restrain echo.
BOP (Bit Oriented Protocol)	A protocol in which sets of bits control the data link.
Carrier (Signal)	A signal suitable by modulation for an information signal.
CCITT (Comite Consultatif International Telegraphique et Telephonique)	International Telegraph and Telephone Consultative Committee, part of the Internation Telecommunication standard organization.
Channel Bank	PCM multiplexer/demultiplexer equipment. (called usually in North America)
24 Channel Bank	Early PCM multiplex equipment, 7 digit A law, 1 signalling bit with each time slot, transmission rate 1536k bps.
30 Channel Mux	CCITT recommended form PCM multiplex equipment. A law, 30 speech channels + 2 signalling channels, transmission rate 2048k bps.
C-message	A frequency weighting which evaluates the noise corresponding to typical subscriber's annoyance in standard telephone service.
C- notched	In C-message, the evaluation for the addition of a notch at 1010 to 1040 Hz.
CODEC	A device which converts an analog (300 Hz to 3.4 kHz) to a digital one, or vice versa.
Companding Law	A logarithmic type of conversion used in compression and expansion.

Term	Explanation
Compression	Characteristic conversion in which the digitized information is compressed to give digital output for a signals normal dynamic range.
COP (Character Oriented Protocol)	A Protocol in which sets of characters control the data link.
Crosstalk	Interference between transmission paths, caused by a signal traveling to another path.
D/A (Digital to Analog) Converter	A device which converts digital form to analog wave.
Decision Sensitivity	Minimum discriminatable input amplitude which discriminator can discriminate the "H", "L" of amplitude under fixed error rate ex): Condition $Pe = 10^{-9}$ Decision Sensitivity = 50 mV If amplitude is more than 50 mV, it can execute signals with error rate less than 10^{-9}/min.
Dial pulses	Sequence of pulses as created on a rotary dial telephone set. (cf. DTMF)
DPSK (Differential Phase Shift Keying)	Modulation technique for the transmission of digital information. Carrier is phase modulated to represent different information states.
Drop out	State in which some pulses become undetectable in successive pulses transmitted.
DTMF (Dual Tone Multi Frequency)	Dialling signal in telephony System. It consists of High and Low frequency.
Echo	The phenomena caused by reflected signals in the other direction.
Equalizer	A device in which attenuation varies with frequency and is used for a frequency-dependent transmission line.
Error Rate (Pe)	Rate of errors which is sent or received incorrectly during a unit time.
Expansion	Back to an original signal from compressed.
FDM (Frequency Division Multiplex)	To obtain several channels over a single path by sharing the frequency band. (cf. TDM)
Frame	A segment of a signal, it is a sequence of time slots each containing a sample in case of TDM.
FSK (Frequency Shift Keying)	A kind of modulation. (cf. DPSK)
Full duplex	Transmission type in both directions simultaneously.
Frequency Specification	A display of a signals constituent frequency components given in terms of frequency versus signal amplitude.
Gain Tracking	Loss deviation (1000 Hz reference commonly) over the range of levels.
Half duplex	Transmission type in one direction at a time over a single channel.
HDLC (High Level Data Link Control)	ISO version of a bit-oriented data link control. HDLC is a protocol for data transmission, and defines an OSI layer 2 communication scheme. HDLC is bit synchronous, supports data addressing of 8 or 16 bits, users a data valid checking scheme called FCS (Frame Check Sequence) embedded within the data, and contains a beginning and ending flag to delineate an HDLC frame. A unique feature of HDLC is zero insertion/deletion. By guaranteeing that any data that contains more than 51's will have at least one zero added, this feature allows the receiving device to differentiate between the delineating from which

Term	Explanation
	contains 61's, and an idle or lost data channel of all 1's that is treated as an about sequence. Also, by adding 0's clock recovery is simpler.
(PCM) Highway	A common path or a set of parallel paths over which signals pass with separation performed time division.
Hookswitch	A switch which detects the state that a handset on telephone whether operates or not.
Idle Channel Noise	The total signal energy measured at the output when the input is grounded in a device.
Impulse noise	The noise which are much higher than the normal peaks of the circuit noise.
Interpolation Filter	A low path (commonly) Filter which smoothes analog forms from decoder.
ISDN	Integrated Service Digital Network. ISDN is a public network system concept services for all types of voice, facsimile certain switched data, packet switch data, video will be integrated into are common digitally based network. In the future, network equipment will handle all types of data. Customer premise equipment will convert all data into a common network compatible digital channel(s) based around 64k bps. The network will keep the data in a digital format, and deliver the data digitally. ISDN delivery mechanisms are independent of media or speed. Media could include twisted pair, coop, fiber optics, satellite, microwave, and data transmission speeds will be in multiples of 64k bps bandwidth.
Jitter	Short term variations of pulses from their real position in time.
LAN (Local Area Network)	A data only communication between terminals on a private site using a standard interface.
Linear Quantizing	Quantizing in which all the intervals classified are equal.
Mark	Presence of a signal. Equivalent to a binary 1 signal state.
Master Clock	A clock which operates a system.
Master Frame	A set of some frames defined.
Modem	A device which modulates or demodulates signals.
Non-Linear Quantizing	Quantizing in which the intervals classified are not all equal.
0 TLP (Zero Transmission Level Point)	An arbitrary point to which all relative level at other points in the system are referred
PABX	Private Automatic Branch Exchange.
Packet-Switching	To transport and switch data in packet form.
PCM (Pulse Code Modulation)	A process in which an analog signal is sampled, quantized and converted to a digital signal.
Protocol	A formal set of conventions or rules governing format, timing, and error control to facilitate message exchanges between two communicating processors.
P/S (parallel to serial) Converter	A device which converts a group of digit, all of which are presented simultaneously, into a corresponding seauence of serial.

Term	Explanation
Psophmetric-weighted	A frequency weight which is similar to C-message. (Used commonly for European telephony system standard).
Quantizing	To be classified an instant swing value got by sampling.
Sampling	To get instant swing values of (continuous) analog wave at equal time intervals.
Sampling rate	The number of samples per unit time.
SDLC (Synchronous Data Link Control)	IBM computer networking protocol associated with BOP.
S & H (Sample and Hold)	To sample (see sampling) and to hold each instant swing values as a pulse of constant time width.
Signalling	The transmission of switching information between stations.
SLIC (Subscriber Line Interface Circuit)	The circuit which performs the interface between local loop and digital switching System.
Space	Absence of signal. Equivalent to a binary 0 signal state.
Space Division switch	Multiport switch in which ports are interconnected by use of different physical paths.
S/P (Serial to Parallel) Converter	A device which converts a sequence of signal into a corresponding group of digits (i.e. parallel data).
Speech Network	Speech Circuit which divides a single transmission channel into double.
STS switch (Space-Time-Space)	Large switch consisting of a time switch block between two space switch blocks.
Synchronization	State in which receive or transmit signal timings occur in the network with the same frequency and phase.
T1 Carrier System	PCM multiplex equipment using μ law, 24 channels. Signalling being performed by bit stealing.
T.D.M. (Time Division Multiplex)	Several information channels are time shared over a single channel and allocated each information by an assigned time slot.
Teletex	Intelligent text communication service which will gradually replace telex.
Teletext	Broad casting service of text on Television reception.
Telex	A message service enabling its subscribers to dial.
Time Division Mux Switch	Multiport switch in which all ports have same physical path because of TDM.
Time Slot	A digital character created by each sampling in PCM.
Tone ringer	A device which converts the ringing signal received from the station into voice frequency as ringing bell.
Trunk	A transmission area between two switching systems.
TST switch (Time Space Time)	Large switch consisting of a space block between two time switch blocks.
White noise	Random noise whose constant energy per unit bandwidth is independent of the frequency at the band.
X.21	A CCITT standard that defines the interface between public data network (DCE) and user terminating equipment (DTE).

Term	Explanation
X.25	A CCITT standard that defines the interface between a packet-switched public data network and packet-mode user device.
X.75	A CCITT standard between international communication. Using X.25.
μ law	Companding/encoding law used in North America and Japan.

• UNIT

Unit	Explanation
dB	Decibel-unit of measure of relative power level. $dB = 10\log_{10} P_1/P_2$
dBm	The transmission level which is referenced to a specified impedance value. 0 dBm = 1 mW
dBmp	Unit of dBm measurements made with a psophometrically weighted filter. $dBmp = 10\log_{10} pWp — 90$ = dBm — 87.5 (Under consideration of flat noise in 300 – 3400 Hz)
dBmO	dBm measurement referenced to a point of zero transmission level.
dBmOP	Relative power psophometrically weighted which is referenced to a point of zero transmission level.
dBr	The relative power level referenced to a point of zero transmission level. dBm = dBmO + dBr
dBrn	Unit of noise measurement on telephone lines. Reference noise is 1 pW (–90 dBm). OdBrn = 90 dBm
dBrnc	dBrn measurements used a C-message weighting filter.
dBrncO	dBrnc measurements referenced to a point of zero transmission level.

NOTES

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