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Configuring and Using the DCU3 and DCULite on the MPC5645S MCU

by: Steve McAslan
Freescale

Contents

1 Introduction

The MPC5645S features two independent display peripherals which allow it to drive up to two TFT LCD panels. The Display Control Unit (DCU3) features a rich set of capabilities that allow users to build engaging and dynamic graphic content from pre-rendered images and then display this content on a wide range of TFT LCD panels. The similar but independent DCULite module performs in an identical fashion but with a slightly reduced feature set. This application note explains the steps to configure and use the DCU and DCULite with TFT LCD panels and how to display and blend graphics on each panel. See www.freescale.com for more details on how to use these features in a typical application.

2 Hardware interface

In most cases both the DCU3 and DCULite connect directly to the TFT LCD panel through the MCU I/O pins. The DCULite requires that the panel include an on-chip timing controller (TCON) function which accepts a parallel RGB interface consisting of up to 24 bits of pixel data (RGB), a pixel clock, an optional data active (enable) line, and optional horizontal sync (HSYNC) and vertical sync (VSYNC) timing signals.

The DCU3 can also connect to a panel which includes a TCON and uses a parallel RGB interface. Alternatively, it can connect to a panel conforming to the RSDS™ (Reduced Swing Differential Signalling) interface standard. In this case the pin connections are different.

It is possible to use panels that accept fewer than 24-bit data input, and in this case it is normal to connect the most significant bits from the DCU3 (or DCULite) to the panel data pins. For example, in the case of an 18-bit panel (RGB each with 6 bits) it is normal to connect as shown in Table 1.

NOTE

The unused pins may be used as GPIO or other function where available.

Table 1. Recommended connection for 18-bit panels

MCU = Panel	MCU = Panel	MCU = Panel
R7 = R5	G7 = G5	B7 = B5
R6 = R4	G6 = G4	B6 = B4
R5 = R3	G5 = G3	B5 = B3
R4 = R2	G4 = G2	B4 = B2
R3 = R1	G3 = G1	B3 = B1
R2 = R0	G2 = G0	B2 = B0
R1 unused	G1 unused	B1 unused
R0 unused	G0 unused	B0 unused

Other timing signals are connected to the panel as required. For example, some panels do not require a horizontal sync signal — in this case the pin can be used as GPIO.

If the TCON RSDS function is used then the pin connections are as shown in Table 2.

Table 2. TCON RSDS pin connections

MCU pin	Panel pin
RSDS0P	RSDS0 Pair positive
RSDS0M	RSDS0 Pair negative
RSDS1P	RSDS1 Pair positive
RSDS1M	RSDS1 Pair negative
RSDS2P	RSDS2 Pair positive
RSDS2M	RSDS2 Pair negative
RSDS3P	RSDS3 Pair positive
RSDS3M	RSDS3 Pair negative
RSDS4P	RSDS4 Pair positive
RSDS4M	RSDS4 Pair negative
RSDS5P	RSDS5 Pair positive
RSDS5M	RSDS5 Pair negative
RSDS6P	RSDS6 Pair positive
RSDS6M	RSDS6 Pair negative
RSDS7P	RSDS7 Pair positive

Table continues on the next page...

Table 2. TCON RSDS pin connections (continued)

MCU pin	Panel pin
RSDS7M	RSDS7 Pair negative
RSDS8P	RSDS8 Pair positive
RSDS8M	RSDS8 Pair negative
RSDS9P	RSDS9 Pair positive
RSDS9M	RSDS9 Pair negative
RSDS10P	RSDS10 Pair positive
RSDS10M	RSDS10 Pair negative
RSDS11P	RSDS11 Pair positive
RSDS11M	RSDS11 Pair negative
RSDSCLKP	RSDS Clock positive
RSDSCLKM	RSDS Clock negative

3 Enabling the DCU3

Enabling the DCU3 on the MPC5645S microcontroller requires two main steps: the DCU3 must be made active in the current MCU mode (mode entry control) and an appropriate clock must be supplied to the DCU3.

3.1 Choosing a suitable clock source

The DCU3 takes an input clock and divides it inside the module to produce the pixel clock required by the connected TFT LCD panel. The DCU3 can choose from:

- Fast internal IRC clock (FIRC) which operates at approximately 16 MHz
- System clock FMPLL0/2
- Secondary PLL FMPLL1
- Fast external crystal oscillator FXOSC (4–16 MHz)

A typical TFT LCD panel needs to be refreshed at approximately 60 Hz. The greater the number of pixels on the panel, the faster the pixel clock has to be, in order to transfer each pixel in the available time.

Pick a clock source that can give the best match to the required pixel clock when divided by an integer value. For example, a QVGA panel requires a pixel clock of approximately 5.33 MHz. If the system clock is 125 MHz then a divider of 23 gives a close match to this value. A wide QVGA panel (480 × 272) requires a pixel clock of approximately 9 MHz. If the system clock is 125 MHz then a divider of 14 gives a close match. If the system clock is not 125 MHz or a more exact match is required, then it may be necessary to use an alternative clock source such as the FMPLL1.

The clock provided to the DCU3 to generate the pixel clock is one of the MCU auxiliary clock sources. Select the clock source required by the DCU3 by writing to the Auxiliary Clock 0 Select register (CGM_AC0_SC).

3.2 Making the DCU3 active on the MPC5645S

It is possible to have the DCU3 operating in all MCU RUN and Low Power modes except STANDBY. In a typical application the DCU3 will only be active in RUN modes (DRUN, RUN0..3) and so only these will be discussed here.

The following steps are needed to enable a module:

1. Identify which Peripheral Control Register controls its operating modes; for the DCU this is PCTL55.
2. Define the Run modes in which the DCU is active. This may depend on the clocks that are available in the modes (FIRC is always available in all Run modes). Choose or configure the modes so that the selected clock source is active.
3. Choose a Run Peripheral Configuration Register (RUN_PC 0..7) that has the required active mode and set the RUN_CFG field of PCTL55 to select that register.

See Table 3 for some examples of suitable values.

Table 3. Example values for RUN_PC and PCTL55 registers

Modes with DCU active	RUN_PC configured	Required RUN_PC setting	PCTL55 RUN_CFG value
DRUN, RUN2	1	0x48	1
RUN0, RUN1, RUN2	6	0x70	6
RUN3	0	0x80	0

It is possible to verify that the DCU3 is active by polling the S_DCU3 bit in the ME_PS1 register. Since the DCU also controls the I/O pins that are connected to the panel, the SIUL module must be enabled in a similar way. The SIUL is normally enabled early in the initialization process since that is required before the MCU can manipulate any I/O pins. The SIUL on the MPC5645S is enabled using PCTL68.

3.3 Making the TCON module active on the DCU3

When the external panel does not contain its own Timing Controller (TCON), use the MPC5645S TCON module. If the TCON module is not required then bypass it by setting the TCON_BYPASS bit in the TCON_CTRL1 register — at reset the module is not bypassed.

To make the TCON active:

1. Make the module active in the appropriate modes by using the PCTL63 register and other peripheral control registers.
2. Ensure that it is not bypassed (TCON_CTRL1[TCON_BYPASS] = 0).

The most common use of the TCON is the RSDS mode, which is the mode discussed in this application note. The TCON also has a TTL mode available, which is selected by setting the TCON_CTRL1[RSDS_MODE] bit to 0.

4 Enabling the DCULite

Enabling the DCULite on the MPC5645S microcontroller requires two main steps: the DCULite must be made active in the current MCU mode (mode entry control) and an appropriate clock must be supplied to the DCULite.

4.1 Choosing a suitable clock source

The DCULite clocking is similar in configuration to that of the DCU. It takes an input clock and divides it inside the module to produce the pixel clock required by the connected TFT LCD panel. The DCULite can choose from:

- Fast internal IRC clock (FIRC) which operates at approximately 16 MHz
- System clock FMPLL0/2
- Secondary PLL FMPLL1
- Fast external crystal oscillator FXOSC (4–16 MHz)

The clock provided to the DCULite to generate the pixel clock is one of the MCU auxiliary clock sources. Select the clock source required by the DCULite by writing to the Auxiliary Clock 4 Select register (CGM_AC4_SC).

4.2 Making the DCULite active on the MPC5645S

It is possible to have the DCULite operating in all MCU RUN and Low Power modes except STANDBY. In a typical application the DCULite will only be active in RUN modes (DRUN, RUN0..3) and so only these will be discussed here.

Follow the same steps described for the DCU in Making the DCU3 active on the MPC5645S except that the appropriate peripheral register is PCTL54.

See Table 4 for some examples of suitable values.

Table 4. Example values for RUN_PC and PCTL54 registers

Modes with DCU active	RUN_PC configured	Required RUN_PC setting	PCTL54 RUN_CFG value
DRUN, RUN2	1	0x48	1
RUN0, RUN1, RUN2	6	0x70	6
RUN3	0	0x80	0

It is possible to verify that the DCULite is active by polling the S_DCULITE bit in the ME_PS1 register. Since the DCULite also controls the I/O pins that are connected to the panelm the SIUL module must be enabled in a similar way. The SIUL is normally enabled early in the initialization process since that is required before the MCU can manipulate any I/O pins. The SIUL on the MPC5645S is enabled using PCTL68.

5 Configuring the DCU3

Once the DCU3 is enabled and has a suitable clock, it is possible to begin configuring the module for the TFT LCD panel being used and verify that the connections are operating as expected. Note that the TCON module is connected by default and therefore if it is not required it must be bypassed — see Making the TCON module active on the DCU3 for more details.

5.1 Configuring the DCU for a TFT LCD panel without TCON

The first step is to configure the SIUL pins so that the DCU3 function is selected. This will be done by modifying the PCR register associated with each pin.

The relevant fields in the PCR register are the alternate function (PA) field, the output buffer enable (OBE) field and possibly the slew rate control (SRC) field. Refer to the MPC5645S signal description chapter for details of the functions available on each of the pins.

To enable the DCU3 signals, configure the MPC5645S SIUL PCR registers as given in Table 3. The SMC function relates to SAFE mode recovery and is application dependent. The configuration values for input and pull resistors are disabled but can be enabled if required for some reason.

The SRC[1:0] function determines the slew rate control options on the pin and is dependent on the operating frequency of the panel and the layout of the board. Fast slew rates consume more peak current and can create more EMC problems so it is desirable to use the slowest rate required. The optimum slew rate can be calculated using the published specification, simulated using appropriate IBIS models, or experimentally derived by measuring the performance of the hardware. As a starting guideline assume that panels with an operating frequency above 8 MHz will require a setting of 1, panels with an operating frequency above 20 MHz require a setting of 2 and panels above 32 MHz a setting of 3.

Table 5. SIUL module PCR register recommended values

Signal	PCR no	SMC	PA[1:0]	OBE	IBE	ODE	SRC[1:0]	WPE	WPS
R0	0	x	1	0	0	0	x	0	0
R1	1	x	1	0	0	0	x	0	0
R2	2	x	1	0	0	0	x	0	0
R3	3	x	1	0	0	0	x	0	0
R4	4	x	1	0	0	0	x	0	0
R5	5	x	1	0	0	0	x	0	0
R6	6	x	1	0	0	0	x	0	0
R7	7	x	1	0	0	0	x	0	0
G0	8	x	1	0	0	0	x	0	0
G1	9	x	1	0	0	0	x	0	0
G2	10	x	1	0	0	0	x	0	0
G3	11	x	1	0	0	0	x	0	0
G4	12	x	1	0	0	0	x	0	0
G5	13	x	1	0	0	0	x	0	0
G6	14	x	1	0	0	0	x	0	0
G7	15	x	1	0	0	0	x	0	0
B0	86	x	1	0	0	0	x	0	0
B1	87	x	1	0	0	0	x	0	0
B2	88	x	1	0	0	0	x	0	0
B3	89	x	1	0	0	0	x	0	0
B4	90	x	1	0	0	0	x	0	0
B5	91	x	1	0	0	0	x	0	0
B6	92	x	1	0	0	0	x	0	0
B7	93	x	1	0	0	0	x	0	0
VSYNC	94	x	1	0	0	0	x	0	0
HSYNC	95	x	1	0	0	0	x	0	0
DE	96	x	1	0	0	0	x	0	0
PCLK	97	x	1	1	0	0	x	0	0

5.2 Configuring the DCU for a TFT LCD panel with TCON and RSDS

When the TCON RSDS option is used, ports PA[0:15], PG[0:7], PG[11], and PM[2] have the RSDS signalling option as a special function. The SIUL allocates pad control registers to these functions (PCR[270:282]), but because these pads share a common pin with the normal GPIO pins they do not operate in the same way as the normal GPIO ports. PG[11] in particular has a special configuration separate from the other pads.

The special-function pads are output-only, and the associated PCR[OBE] bit is controlled by the TCON_CTRL1 register (TCON_BYPASS and RSDS_MODE bits). However, the alternate function selection is taken from the associated normal GPIO pad. This allows selection of the DCU3 function as the alternate function of the pad, and then the TCON module selects whether the output style is TCON/RSDS or digital RGB format.

Therefore, when the TCON bypass is active (bypass disabled with or without RSDS active), it is important not to configure the normal GPIO ports for output operation with a non-DCU3 alternate function on ports PA[0:15] and PG[0:7].

For PG[11], the PCR[282] OBE bit is fully controlled by the TCON module and will become an output whenever the DCU3 alternate option is selected. Therefore, only select the DCU3 function on this pin when ready to configure it as a clock for a TFT panel.

To enable the TCON RSDS signals, configure the MPC5645S SIUL PCR registers as given in Table 6. The SMC function relates to Safe mode recovery and is application dependent. The configuration values for input and pull resistors are disabled but can be enabled if necessary.

The SRC[1:0] function determines the slew rate control options on the pin. It is dependent on the operating frequency of the panel and the layout of the board. Fast slew rates consume more peak current and can create more EMC problems, so it is best to use the slowest rate required. The optimum slew rate can be calculated using the published specification, simulated using appropriate IBIS models, or experimentally derived by measuring the performance of the hardware.

Table 6. SIUL module PCR register recommended values

Signal	Port Pin PCR		RSDS Pin PCR				
	No	PA[1:0]	No	ODE	SRC[1:0]	WPE	WPS
RSDS0P	0	1	270	0	x	0	0
RSDS0M	1	1		0	x	0	0
RSDS1P	2	1	271	0	x	0	0
RSDS1M	3	1		0	x	0	0
RSDS2P	4	1	272	0	x	0	0
RSDS2M	5	1		0	x	0	0
RSDS3P	6	1	273	0	x	0	0
RSDS3M	7	1		0	x	0	0
RSDS4P	8	1	274	0	x	0	0
RSDS4M	9	1		0	x	0	0
RSDS5P	10	1	275	0	x	0	0
RSDS5M	11	1		0	x	0	0
RSDS6P	12	1	276	0	x	0	0
RSDS6M	13	1		0	x	0	0
RSDS7P	14	1	277	0	x	0	0
RSDS7M	15	1		0	x	0	0
RSDS8P	86	1	278	0	x	0	0
RSDS8M	87	1		0	x	0	0
RSDS9P	88	1	279	0	x	0	0
RSDS9M	89	1		0	x	0	0

Table continues on the next page...

Table 6. SIUL module PCR register recommended values (continued)

Signal	Port Pin PCR		RSDS Pin PCR				
	No	PA[1:0]	No	ODE	SRC[1:0]	WPE	WPS
RSDS10P	90	1	280	0	x	0	0
RSDS10M	91	1		0	x	0	0
RSDS11P	92	1	281	0	x	0	0
RSDS11M	93	1		0	x	0	0
RSDSCLKP	97	1	282	0	x	0	0
RSDSCLKM	149	3		0	x	0	0

5.3 Configuring the timing parameters

The second step is to configure the DCU3 operating parameters to match the specification of the panel being used. The relevant configuration registers are given in Table 7.

Table 7. DCU3 panel configuration registers

Register	Function
DIV_RATIO	Divides the selected DCU3 auxiliary clock down to the required pixel clock value.
DISP_SIZE	Defines the number of horizontal and vertical pixels on the panel.
HSYN_PARA	Defines the horizontal (line) timing parameters.
VSYN_PARA	Defines the vertical (whole frame) timing parameters.
SYN_POL	Defines the polarity of the timing signals.

Start by providing the correct division ratio for the auxiliary clock provided to the DCU. This is a simple modulus division with the value in DIV_RATIO being one less than the divider required — for example, a value of zero gives a division of one.

Table 8 shows some example DIV_RATIO values for different panel sizes. The table assumes the following pixel clock requirements for the example panels:

- QVGA (240 × 320) = 5.33 MHz
- WQVGA (480 × 272) = 9 MHz

Note that the chosen DIV_RATIO value will typically not be able to match the target pixel clock frequency exactly, and so judgment must be used to verify that the value is suitable for the panel.

Table 8. Example DIV_RATIO values for different panels

Auxiliary clock	QVGA	WQVGA
64 MHz	11	6
56 MHz	9	5
48 MHz	8	4
32 MHz	5	3

Next configure the DISP_SIZE to match the panel size. The vertical dimension of the panel is entered directly in the DELTA_Y field. The horizontal dimension is configured differently. The DCU3 requires the width of the panel to be a multiple of 16 and the DELTA_X field indicates the number of multiples in the horizontal dimension. In other words, the DELTA_X field contains the width of the panel divided by 16. See Table 9 for some typical examples.

Table 9. Example DISP_SIZE values for different panels

Panel size	DELTA_Y	DELTA_X
320 H × 240 V	240	20
240 H × 320 V	320	15
480 H × 272 V	272	30
640 H × 240 V	240	40

Now the synchronization signals must be configured for the panel. Typically each panel has unique timing requirements and not all timing signals are required for all panels. However, manufacturers tend to specify the timing configuration in a consistent way that matches the parameter requirements for the DCU3. In most cases it is possible to read the timing parameter from a TFT LCD specification and then enter that number directly into the relevant DCU3 configuration register.

Begin the configuration with the HSYN_PARA register that configures the horizontal signals. Three values are required (as illustrated in Figure 1) and all are defined in multiples of the pixel clock:

- Horizontal pulse width: defines the number of pixel clocks for which the horizontal timing pulse is active (HSYNC signal).
- Horizontal back porch width: defines the number of pixel clocks after the horizontal pulse before the start of pixel data. Some manufacturers define the back porch starting from the start of the horizontal pulse rather than the end.
- Horizontal front porch width: defines the number of pixel clocks after the pixel data before the start of the horizontal pulse.

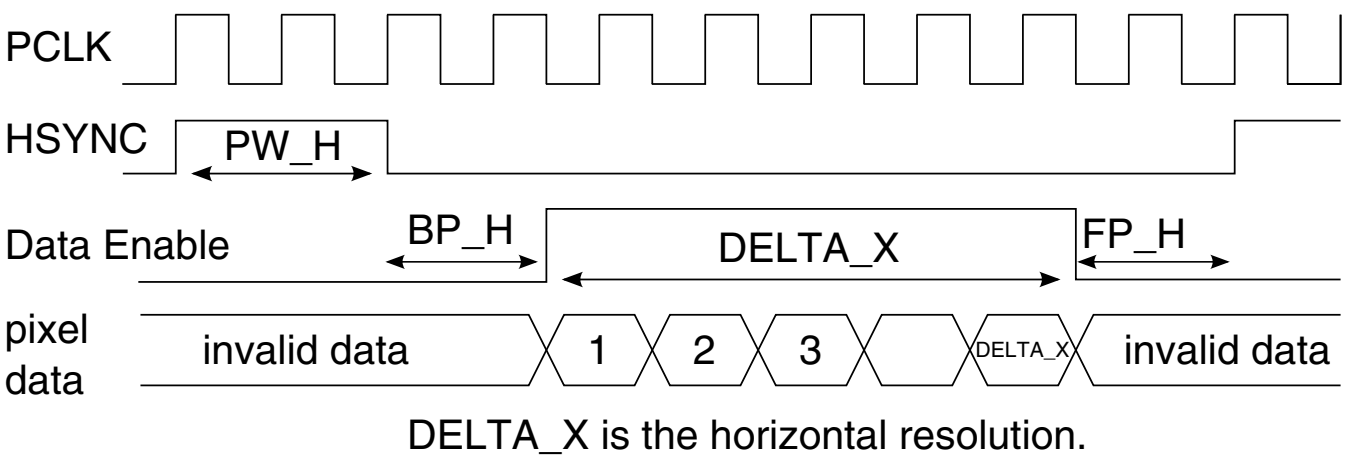

Figure 1. Horizontal timing diagram

Next configure the vertical timing signals using the VSYN_PARA register. Three values are required (as illustrated in Figure 2) and all are defined in multiples of horizontal lines:

- Vertical pulse width: defines the number of horizontal lines for which the vertical timing pulse is active (VSYNC signal).
- Vertical back porch width: defines the number of horizontal lines after the vertical pulse before the start of pixel data. Some manufacturers define the back porch starting from the start of the vertical pulse rather than the end.
- Vertical front porch width: defines the number of horizontal lines after the pixel data before the start of the vertical pulse.

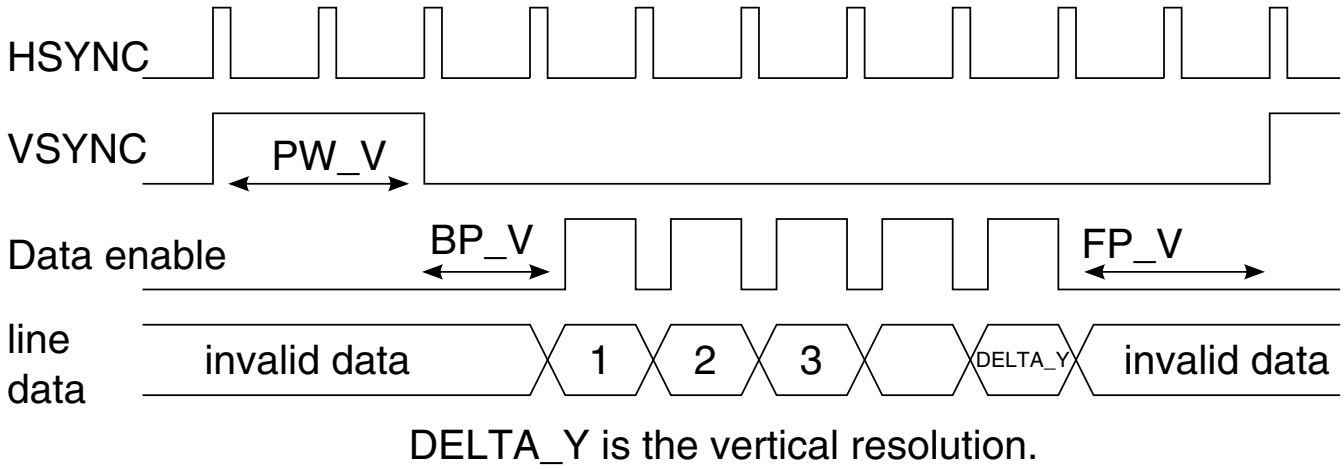

Figure 2. Vertical timing diagram

The polarity of the pixel clock (PCLK), the horizontal timing signal (HSYNC), and the vertical timing signal (VSYNC) may be inverted using the SYN_POL register.

5.4 Enabling and configuring TCON settings

If the TCON is in use, then there are further adjustments to be made. For RSDS functionality, set TCON_CTRL1[RSDS_MODE] = 1 — to enable the TCON, set TCON_CTRL1[TCON_EN] = 1.

There are many other options for the RSDS signal timing and polarity which can be adjusted to meet the panel requirements. These are discussed in detail in the MPC5645S reference manual.

5.5 Testing the hardware and software configuration

After the DCU3 is enabled and configured, it is possible to display graphics on the panel or perform verification tests. Using the DCU3 and DCULite describes the normal use of the panel and this section provides guidance on how to verify the hardware and software configuration of the system.

The DCU3 includes a special test card mode that displays bands of known colors on the panel. This mode allows verification so that the connection to the panel and the DCU3 timing configuration is correct.

At this stage the panel is connected and the DCU3 is configured to drive the panel, but no timing signals are being driven by the MPC5645S. It is possible to start the pixel clock before HSYNC, VSYNC, and the pixel data; this is a requirement for some panels. It is also possible to start all signals at the same time.

To start the pixel clock before other timing signals, use these steps:

1. In the DCU_MODE register, set the DCU_MODE field to three, which selects color bar mode.
2. In the DCU_MODE register set the RASTER_EN field to one, which enables the raster signals (HSYNC, VSYNC, pixel data).

To start all the signals together, perform this step:

- In the DCU_MODE register set the DCU_MODE field to three and the RASTER_EN field to one.

The DCU3 will begin sending pixel data which divides the panel into eight color bars horizontally. By default, each color bar is assigned a color as shown in Figure 3.

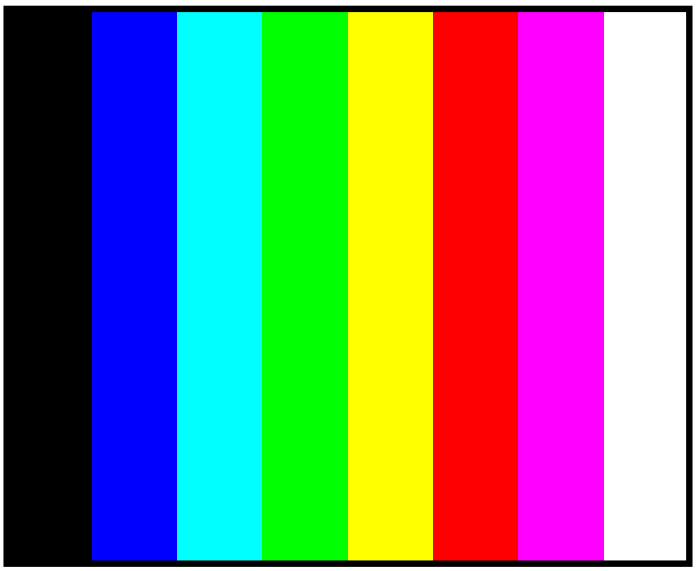

Figure 3. Default color bar mode configuration

This standard configuration can be used to verify that the connection to the panel and the timing is correct. Verify the timing by measuring the MPC5645S signals and comparing them to the values expected by the panel. The pixel data connection integrity can be verified by examining the content of the panel. This setting also allows testing and configuration of the panel backlight control.

It is possible to verify the connection of each of the pixel data lines by modifying the color bar color settings. This is done using the COLBAR_1 to COLBAR_8 registers. The registers are numbered to represent the bars from left to right so that the COLBAR_1 register contains the color setting of the left-hand bar (in the default case this is black) and COLBAR contains the color settings of the right-hand bar (white). Each COLBAR_*n* register contains an RGB888 value with 8 bits to define each of red, green, and blue content of the bar. It is possible to change these registers to any other value. As an example, it is possible to verify that each green data line is connected and that there are no short circuits by changing the COLBAR_*n* registers to contain only a single green data line value like this:

1. Set COLBAR_1 to 0x00008000.
2. Set COLBAR_2 to 0x00004000.
3. Set COLBAR_3 to 0x00002000.
4. Set COLBAR_4 to 0x00001000.
5. Set COLBAR_5 to 0x00000800.
6. Set COLBAR_6 to 0x00000400.
7. Set COLBAR_7 to 0x00000200.
8. Set COLBAR_8 to 0x00000100.

The resulting panel content is shown in Figure 4. Each color bar should be a different shade of green with no red or blue visible. This is not a comprehensive test on its own, but combined with other combinations and test approaches may be used to visually and electrically verify correct configuration.

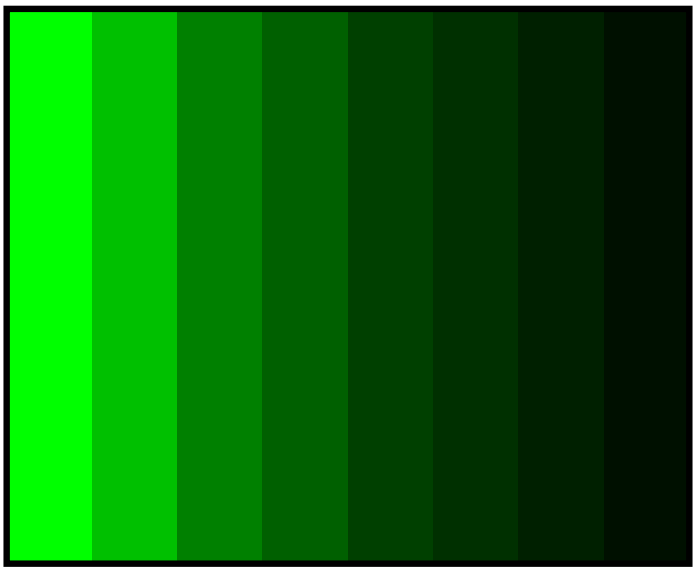

Figure 4. Green data line connection test (simulated)

6 Configuring the DCULite

Configuration of the DCULite follows a similar pattern to the RGB configuration for the DCU3. In this section the I/O pin configurations are identified, but since the timing and debug features are identical to that on the DCU3 please refer to Configuring the timing parameters and Enabling and configuring TCON settings for further details on the steps required.

6.1 Configuring the DCULite for a TFT LCD panel

The SIUL pins must be configured so that the DCULite function is selected. The relevant fields in the PCR register are the alternate function (PA) field, the output buffer enable (OBE) field, and possibly the slew rate control (SRC) field. Refer to the MPC5645S reference manual signal description chapter for details of the functions available on each of the pins.

To enable the DCULite signals, configure the MPC5645S SIUL PCR registers as given in Table 3. Note that unlike the DCU3, the DCULite has a choice of different I/O pins for some of the functions — choose one pin for each output function. The SMC function relates to SAFE mode recovery and is application-dependent. The configuration values for input and pull resistors are disabled but can be enabled if necessary.

The SRC[1:0] function determines the slew rate control options on the pin and is dependent on the operating frequency of the panel and the layout of the board. Fast slew rates consume more peak current and can create more EMC problems so it is best to use the slowest rate required. The optimum slew rate can be calculated using the published specification, simulated using appropriate IBIS models, or experimentally derived by measuring the performance of the hardware. As a starting guideline assume that panels with an operating frequency above 8 MHz will require a setting of one, panels with an operating frequency above 20 MHz require a setting of two, and panels above 32 MHz a setting of three.

Table 10. SIUL module PCR register recommended values

Signal	PCR no	SMC	PA[1:0]	OBE	IBE	ODE	SRC[1:0]	WPE	WPS
R0	163	x	1	0	0	0	x	0	0
R1	164	x	1	0	0	0	x	0	0

Table continues on the next page...

Table 10. SIUL module PCR register recommended values (continued)

Signal	PCR no	SMC	PA[1:0]	OBE	IBE	ODE	SRC[1:0]	WPE	WPS
R2	128	x	2	0	0	0	x	0	0
	165		1						
R3	129	x	2	0	0	0	x	0	0
	166		1						
R4	130	x	2	0	0	0	x	0	0
	167		1						
R5	147	x	2	0	0	0	x	0	0
	168		1						
R6	148	x	2	0	0	0	x	0	0
	169		1						
R7	149	x	2	0	0	0	x	0	0
	170		1						
G0	171	x	1	0	0	0	x	0	0
G1	172	x	1	0	0	0	x	0	0
G2	143	x	2	0	0	0	x	0	0
	173		1						
G3	144	x	2	0	0	0	x	0	0
	174		1						
G4	145	x	2	0	0	0	x	0	0
	175		1						
G5	146	x	2	0	0	0	x	0	0
	176		1						
G6	103 or 117	x	3	0	0	0	x	0	0
	177		1						
G7	121	x	3	0	0	0	x	0	0
	178		1						
B0	179	x	1	0	0	0	x	0	0
B1	180	x	1	0	0	0	x	0	0
B2	70 or 181	x	1	0	0	0	x	0	0
B3	71 or 182	x	1	0	0	0	x	0	0
B4	73 or 183	x	1	0	0	0	x	0	0
B5	74 or 184	x	1	0	0	0	x	0	0
B6	77 or 105	x	1	0	0	0	x	0	0
B7	98 or 159	x	1	0	0	0	x	0	0
VSYNC	126 or 162	x	1	0	0	0	x	0	0

Table continues on the next page...

Table 10. SIUL module PCR register recommended values (continued)

Signal	PCR no	SMC	PA[1:0]	OBE	IBE	ODE	SRC[1:0]	WPE	WPS
HSYNC	125 or 161	x	1	0	0	0	x	0	0
DE	124 or 149	x	3	0	0	0	x	0	0
PCLK	127 or 160	x	1	0	0	0	x	0	0

The second step is to configure the DCULite operating parameters to match the specification of the panel being used. The relevant configuration registers are given in Table 7.

7 Using the DCU3 and DCULite

Once the panel hardware and software configuration is verified it is possible to begin using the DCU3 or DCULite in its functional mode.

To enable the panel for normal use:

- In the DCU_MODE register set the DCU_MODE field to 1, which selects normal mode.
- In the DCU_MODE register set the RASTER_EN field to 1, which enables the raster signals (HSYNC, VSYNC, pixel data).
- OR to start all signals together, in the DCU_MODE register set the DCU_MODE field to 1 and the RASTER_EN field to 1.

At this point the panel should be active and displaying a single color. This color is configured in the BGND register and is black after reset. Like the COLBAR_n registers, this register can be modified to display any single color by modifying its value to another RGB888 value.

Functional content is placed on the panel by enabling graphic layers, the cursor, or the Parallel Data Interface (PDI) input, or any combination of those. These elements are discussed in the following sections with a focus on their basic properties. To see examples of how an application may use the different features, please refer to demonstration software, application notes, and video examples available at www.freescale.com.

7.1 Using the graphic layers

The most common way of presenting content on the panel is the layer. By configuring a layer it is possible to fetch a graphic directly from any memory mapped module and display it on the panel. The graphic data may be encoded in many different formats. There are 16 layers in total and each is configured using 7 registers. The layers are independent of each other and placed in a fixed priority on the panel. The steps to display a graphic on a layer are as follows:

1. Configure the size of the layer using CtrlDescLn_1. The width of the graphic must conform to configuration rules related to the graphic encoding as described in the MPC5645S reference manual.

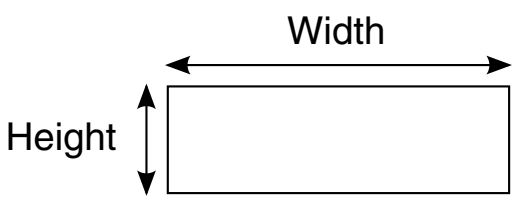

Figure 5. CTRLDESCLn_1 register

2. Place the layer on the panel using CtrlDescLn_2.

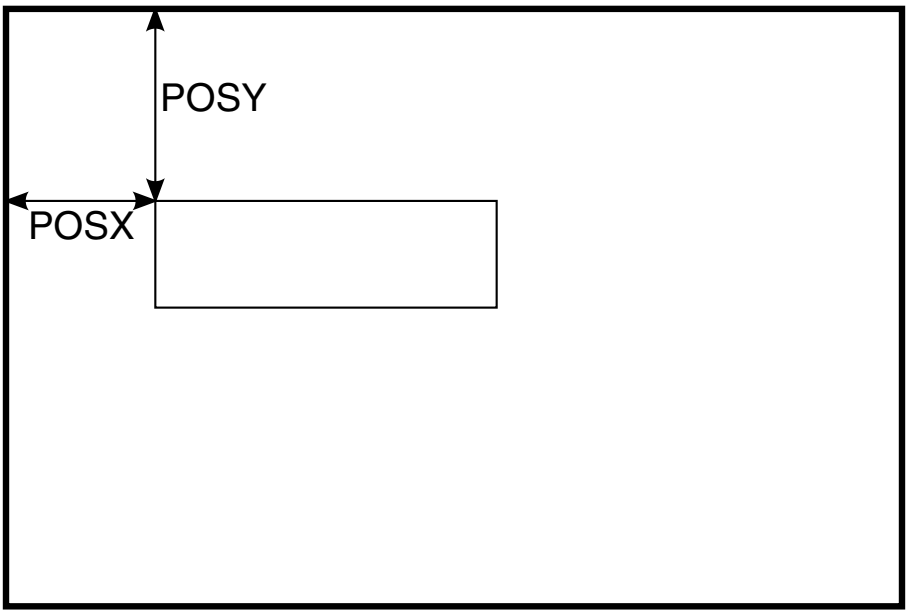

Figure 6. CTRLDESCLn_2 register

3. Point to the top left-hand pixel of the graphic in memory using CtrlDescLn_3. Note that if the graphic is stored in internal flash memory, then the access settings must be modified from the reset condition by clearing the flash PFSACC register to 0x00000000.

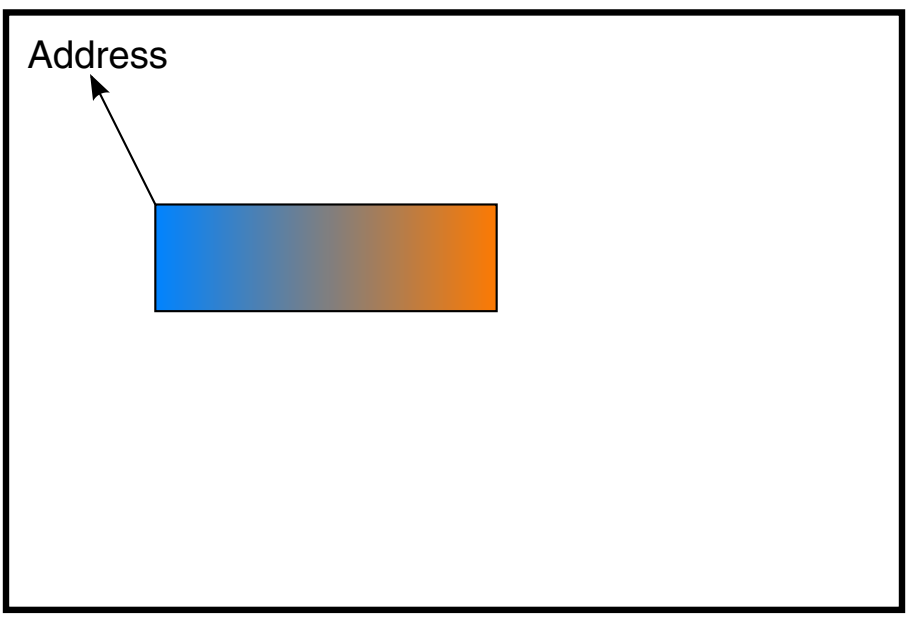

Figure 7. CTRLDESCLn_3 register

4. Choose the graphic encoding, blending, and tiling and then enable it using CtrlDescLn_4.

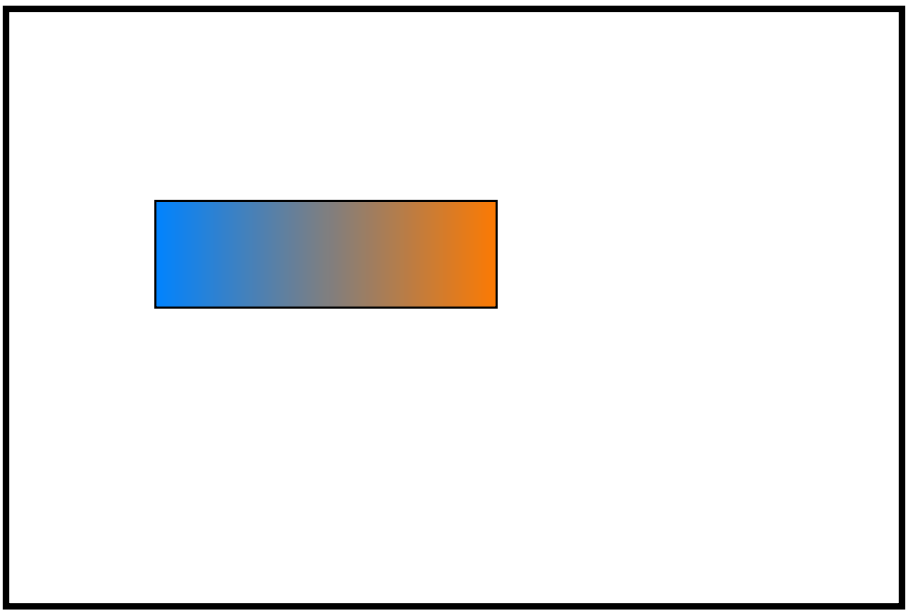

Figure 8. CTRLDESCLn_4 register

5. Configure the chroma-keying ranges using CtrlDescLn_5 and CtrlDescLn_6.

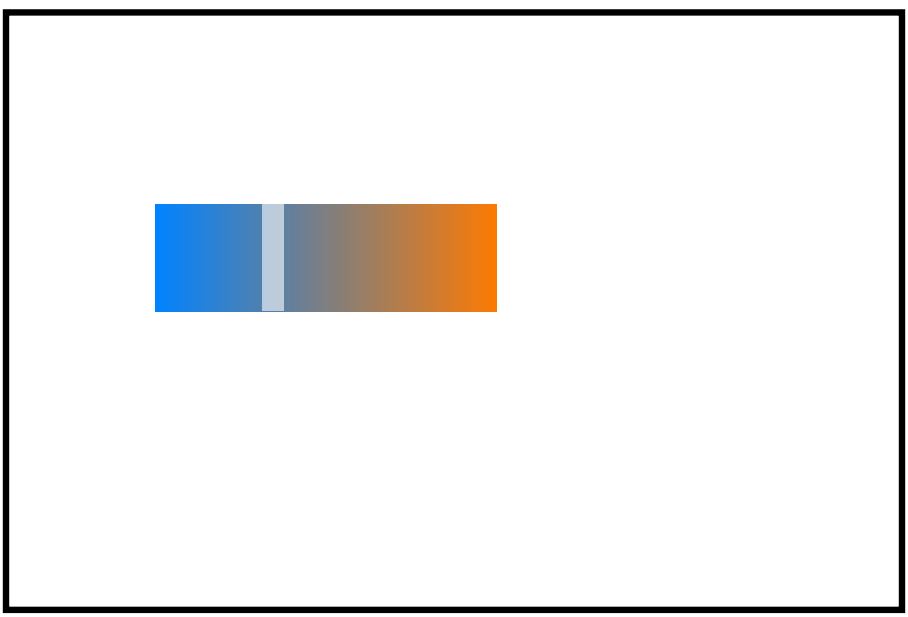

Figure 9. CTRLDESCLn_5 and CTRLDESCLn_6 registers

6. Configure the tile size using CtrlDescLn_7.

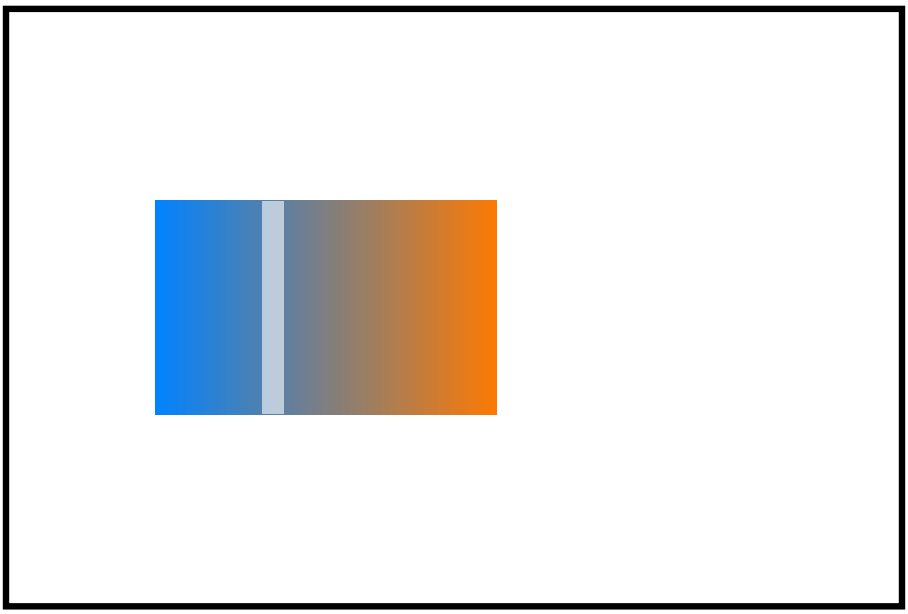

Figure 10. CTRLDESCLn_7 Register

CtrlDescLn_4 makes multiple blending and encoding combinations available, which are explored in more detail in video material available at http://www.youtube.com/freescale.

Errors in configuring the layers are reported in the PARR_ERR_STATUS register. Note that an error in the layer configuration registers will prevent the layer from being visible. If a layer is not visible as expected, check the flags in the PARR_ERR_STATUS register to see if an error has been detected.

The priority of the layers is fixed, so layer 0 is always higher priority than layer 1, which is higher than layer 2 and so on. This arrangement influences the effect of blending.

7.2 Using the cursor

The cursor is a graphic element independent from the graphic layers. It allows a single graphic to be placed on top of all the layers and does not support any blending or choice of graphic encoding. The cursor is always stored in a special area of RAM with the DCU3 or DCULite module.

The steps to display the cursor are as follows:

1. Configure the size of the cursor using CtrlDescCursor_1. The maximum size of the cursor is determined by the size of the internal RAM.

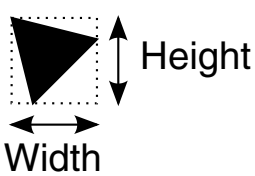

Figure 11. CtrlDescCursor_1 register

2. Place the layer on the panel using CtrlDescCursor_2.

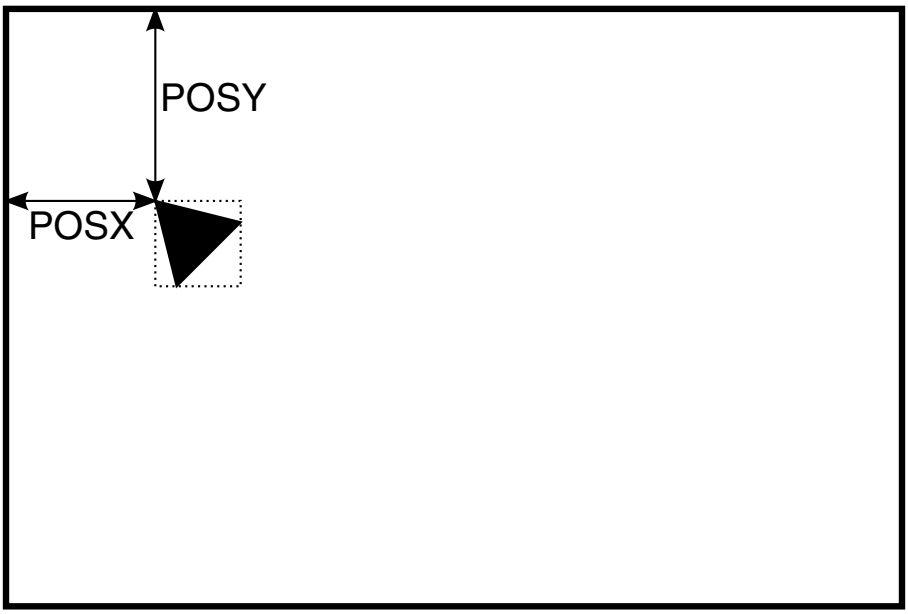

Figure 12. CtrlDescCursor_2 register

3. Choose the color of the cursor using CtrlDescCursor_3.

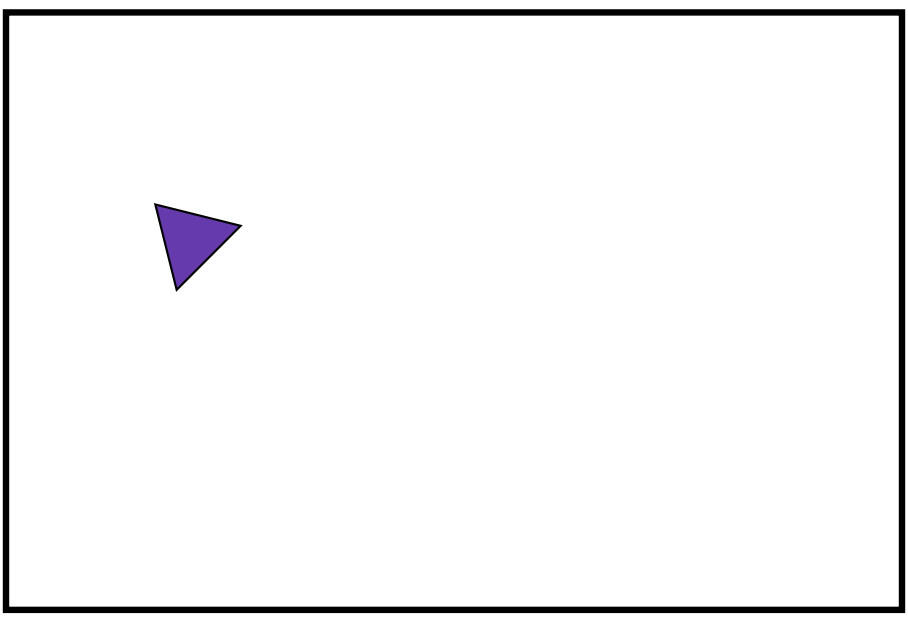

Figure 13. CtrlDescCursor_3 register

4. Choose the blinking options using CtrlDescCursor_4.

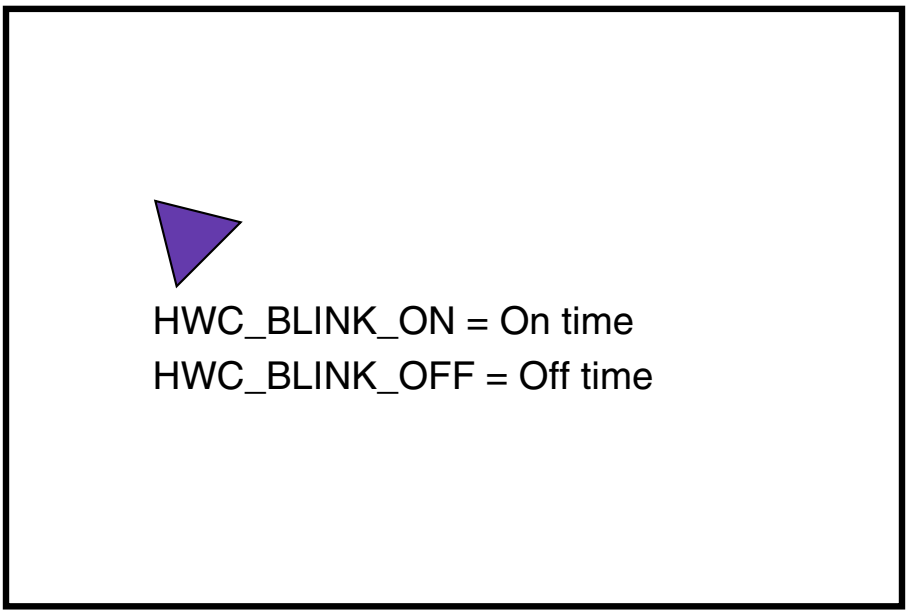

Figure 14. CtrlDescCursor_4 register

7.3 Using the Parallel Data Interface (PDI)

The Parallel Data Interface is intended to accept a video stream and display it on the panel, where it replaces the fixed background color. As such, any video or image will always be the lowest priority content on the panel.

The PDI input has the following strict requirements for correct operation:

- Incoming video must be non-interlaced.
- Incoming video must be formatted to match the panel size. For example, if the panel is QVGA (320 x 240) format then the incoming video must also be non-interlaced QVGA.
- The timing signals from the camera must match the requirements of the panel.

The PDI also provides the possibility of synchronizing the DCU3 or DCULite with an external reference, which may be convenient if multiple video sources are in use or if the DCU3 or DCULite output is being post-processed. This configuration is known as PDI slave mode, and uses timing signals provided by the PDI to display graphics stored internally in the DCU. Enable this mode using the PDI_SLAVE_MODE bit in the DCU_MODE register.

The PDI can accept either parallel data and timing signals (similar to those produced by the DCU3) or encoded video in the format specified by the ITU in standard ITU-R BT.656. The incoming data can be up to 18 bits in width, and for 16-bit input formats can be multiplexed onto 8 pins to reduce the number of pins required. This is described as narrow mode.

Configuration of the PDI input format is performed by the PDI_MODE field in the DCU_MODE register. This register also has fields to enable:

- Narrow mode (PDI_NARROW_MODE)
- Order of the bytes in this mode (PDI_BYTE_REV)
- Whether the data enable signal is used (PDI_DE_MODE)
- Enabling the PDI itself (PDI_EN)

DCU_MODE register also contains a control for the number of valid frames that must be received before incoming video is accepted as valid (PDI_SYNC_LOCK). The SYN_POL register also sets the expectations for the polarity of the PDI enable, clock, and synchronization signals. The status of the PDI is reported in the PDI_STATUS register.

8 Summary

This application note describes the steps needed to enable and use the DCU3 or DCULite on the MPC5645S. The nature of graphical user interfaces is such that layers of graphic software and individual image designs will be required to make use of the DCU3 or DCULite in a typical application. Examples of this software and design flow recommendations are available from the Freescale resource library at www.freescale.com.

How to Reach Us:

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Web Support:
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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
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Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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