Truly Innovative 28nm FDSOI Technology for Automotive Microcontroller Applications embedding 16MB Phase Change Memory

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Outline of Presentation

- Introduction
- Technology description
- CMOS devices suite
- PCM analytical cell
- 16MB PCM array results
- Conclusions

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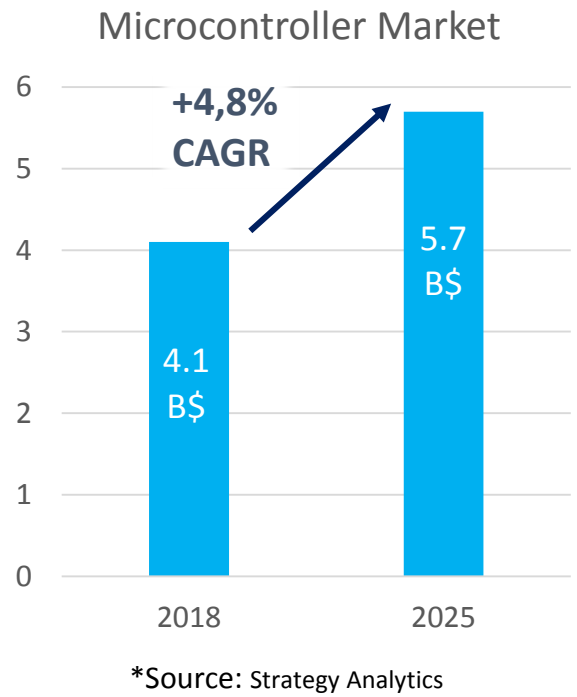
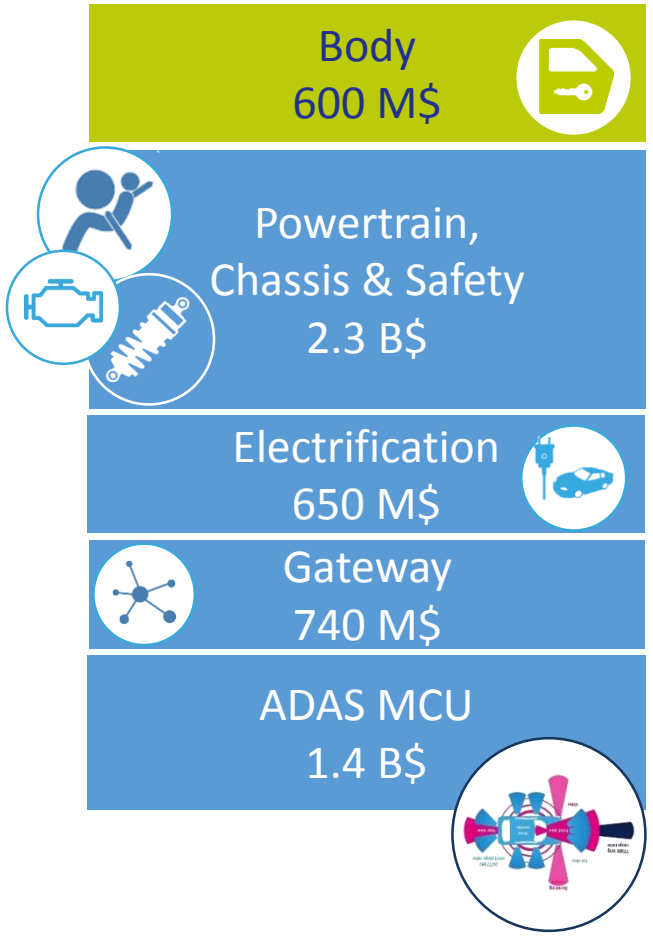
Automotive Microcontrollers



*Source: Strategy Analytics



Automotive MCU growth contributors:

Advanced Powertrain: combining Electric Motors, Thermal Engine and Transmission management

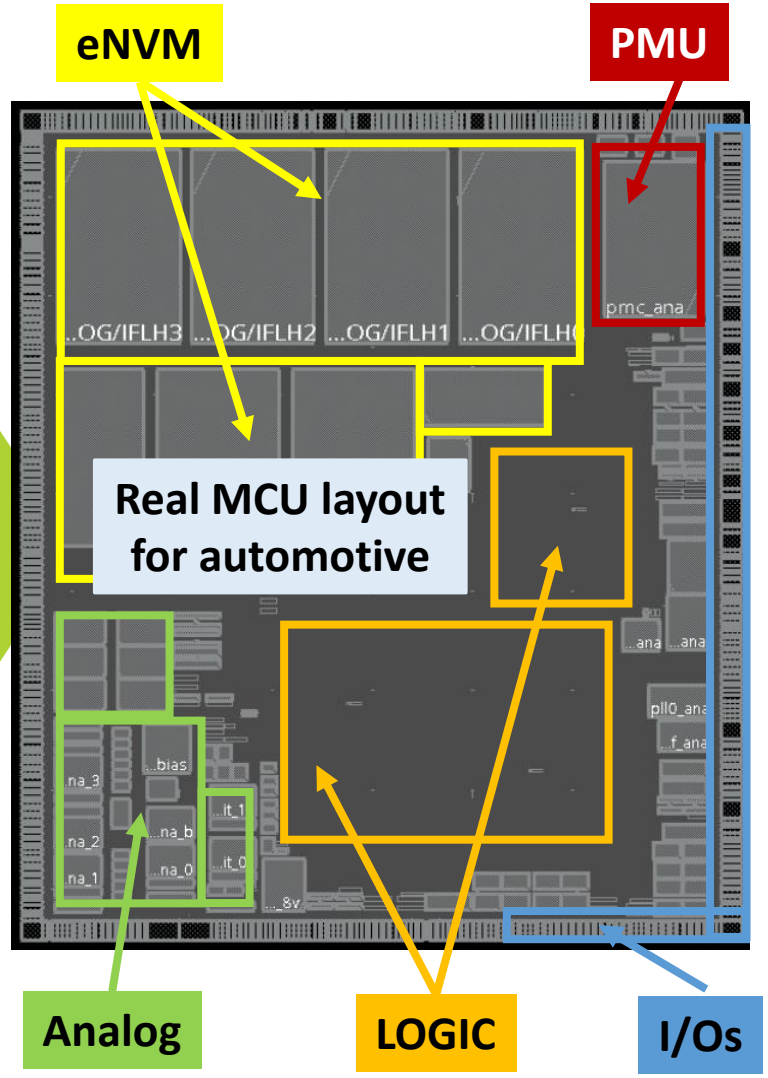
Electrification: smart power supporting electrification

Gateways: Secure communication interfaces

ADAS: safety microcontrollers

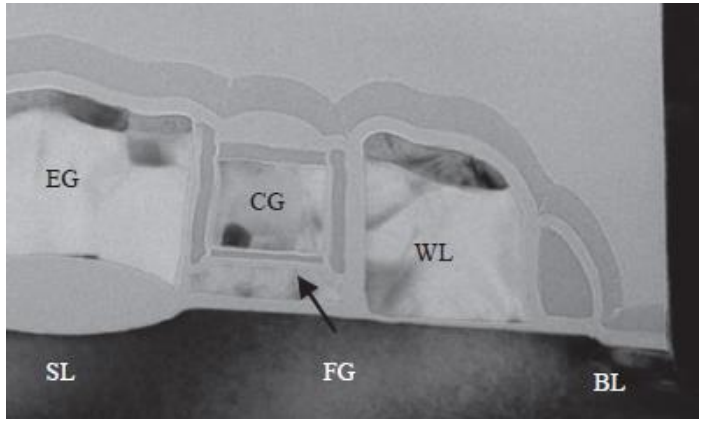
eNVM trend: increase memory size due to:
- increased software complexity
- multiple firmware image storage

Microcontroller Chips for Automotive



Physical Mechanisms for eNVM

Charges manipulation

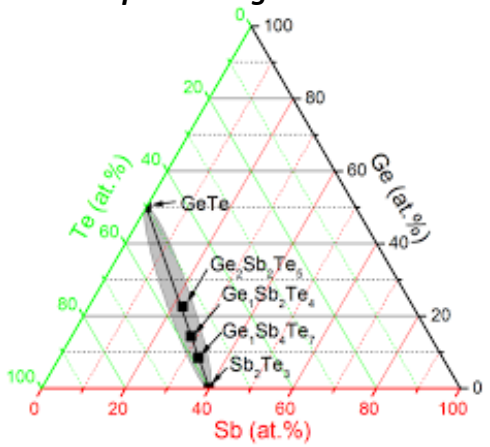


© ESF3 structure from SST

eFLASH

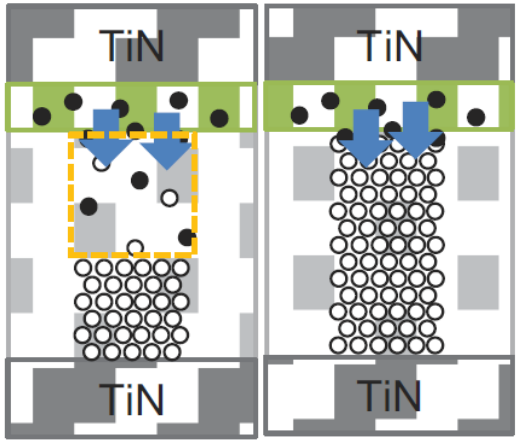
Atoms manipulation

GeSbTe phase diagram



PCRAM

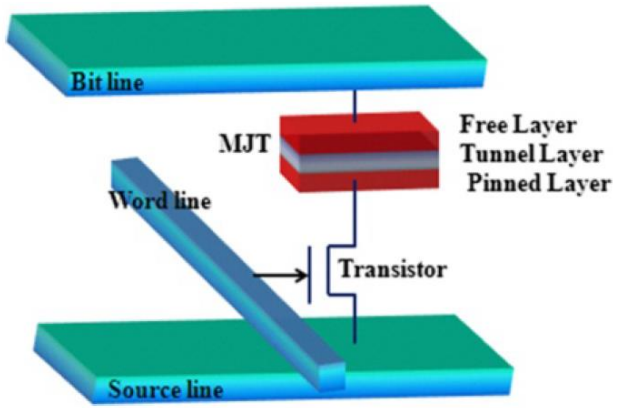
HRS ***LRS***



Y-H Lin et al, "Excellent high T° retention of In NOxNy ReRAM by interfacial layer engineering" VLSI-TSA, 2018

Ox.RAM

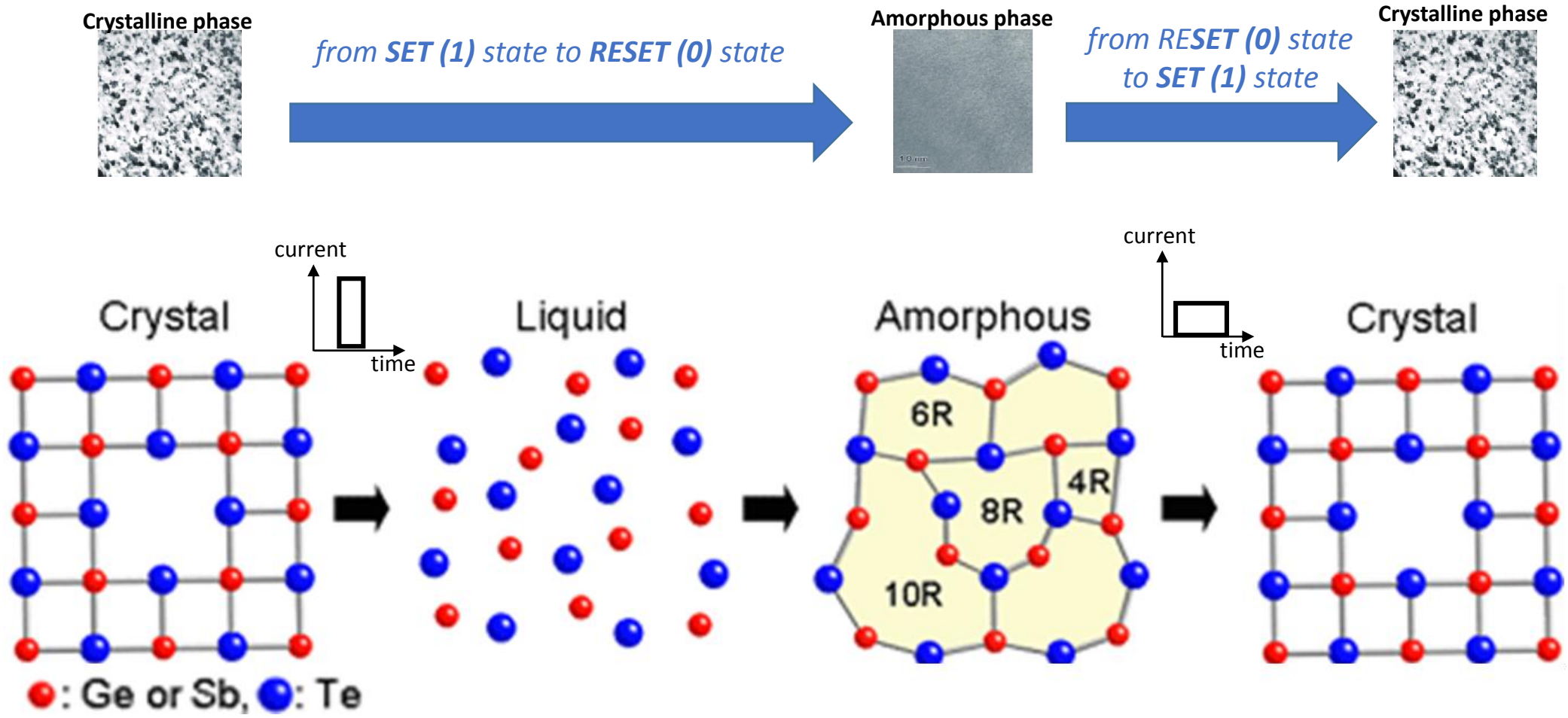
Spin manipulation



T. Kawahara et al, "Spin transfer torque RAM technology" Mircoelectron Reliability, 2012

STT MRAM

Phase Change Memory Principle



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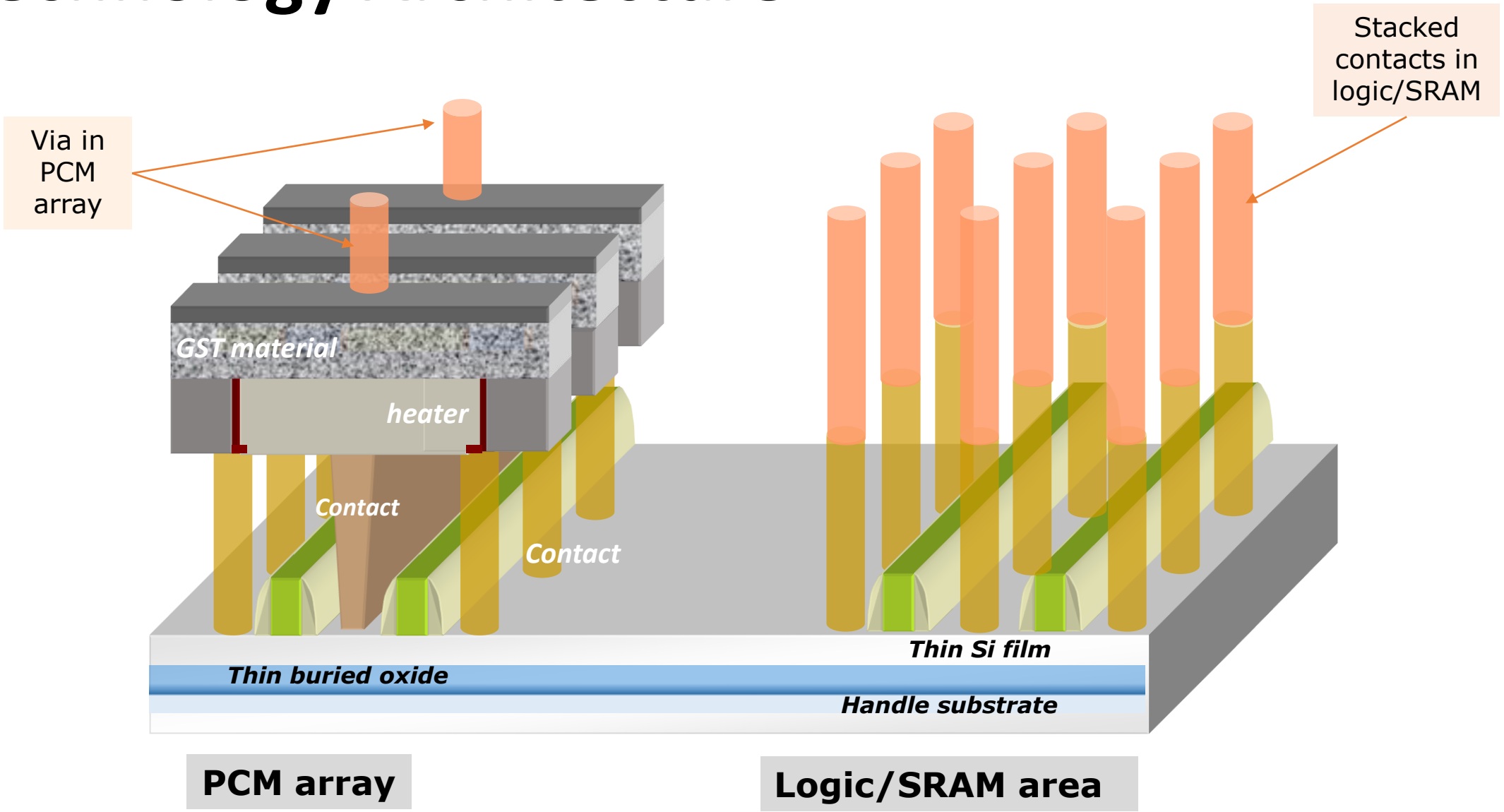
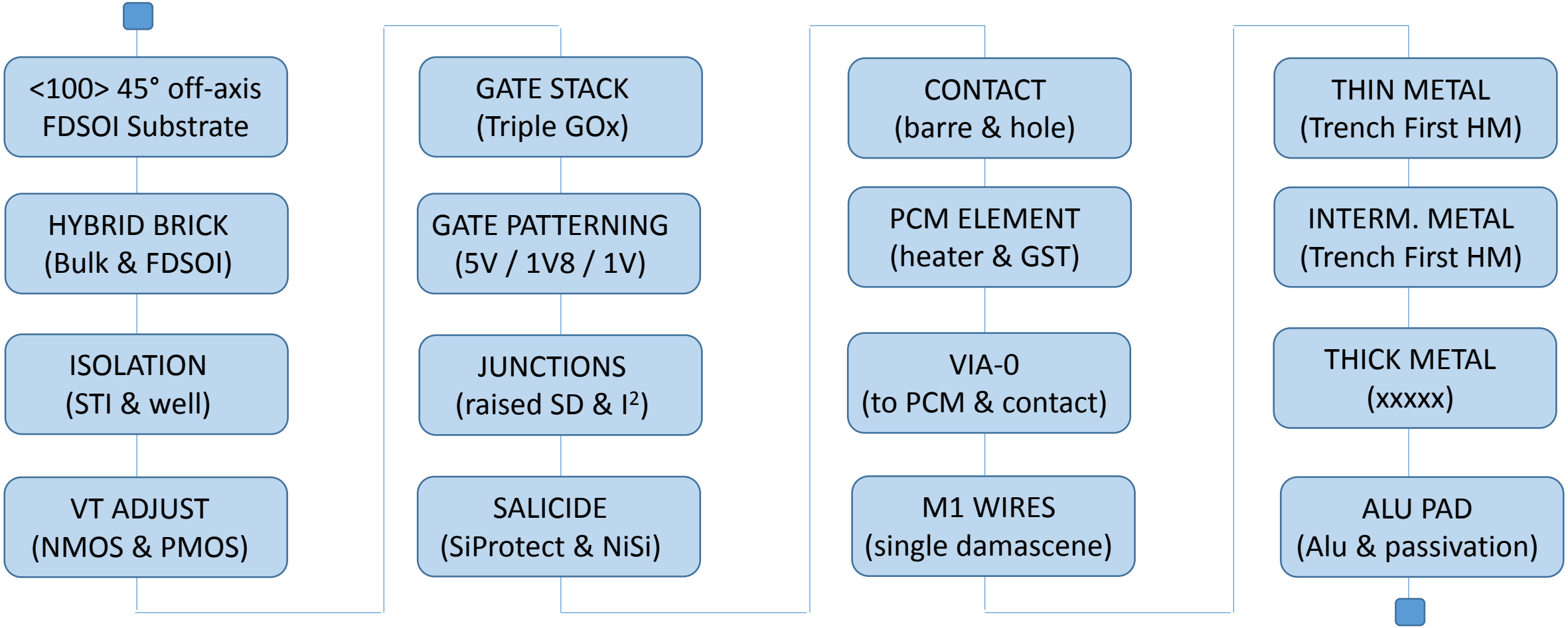
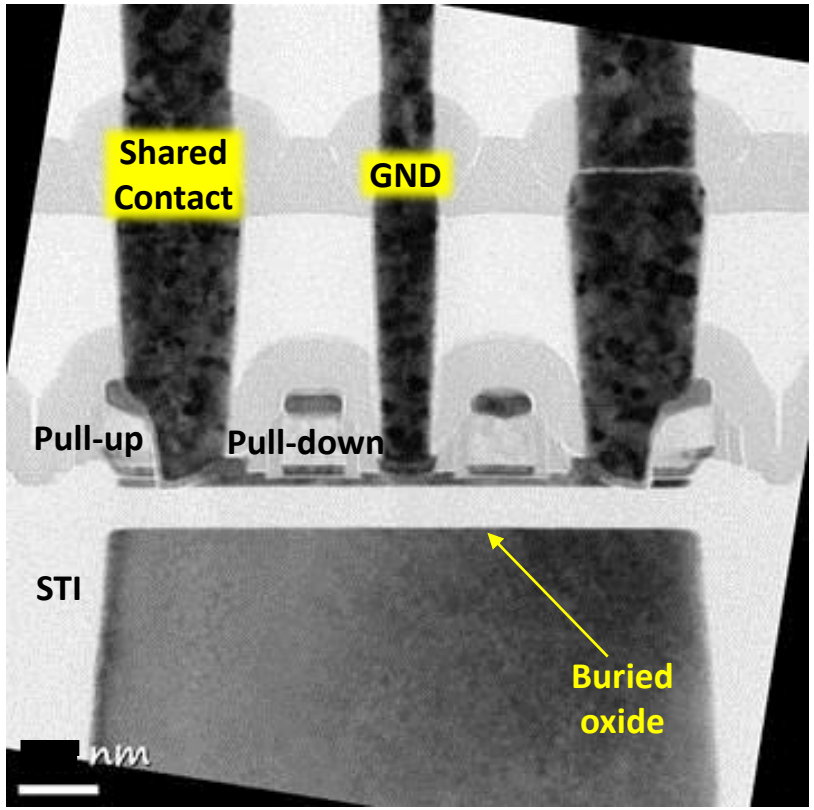
Technology Architecture



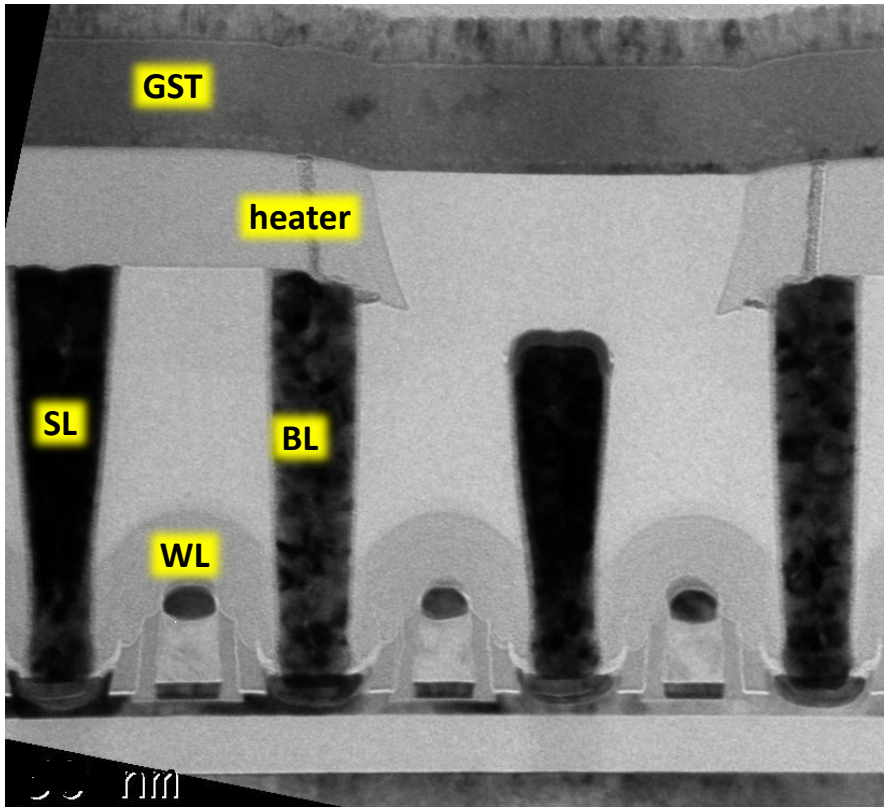
Process Integration Sequence



Co-Integrated Memories Morphology

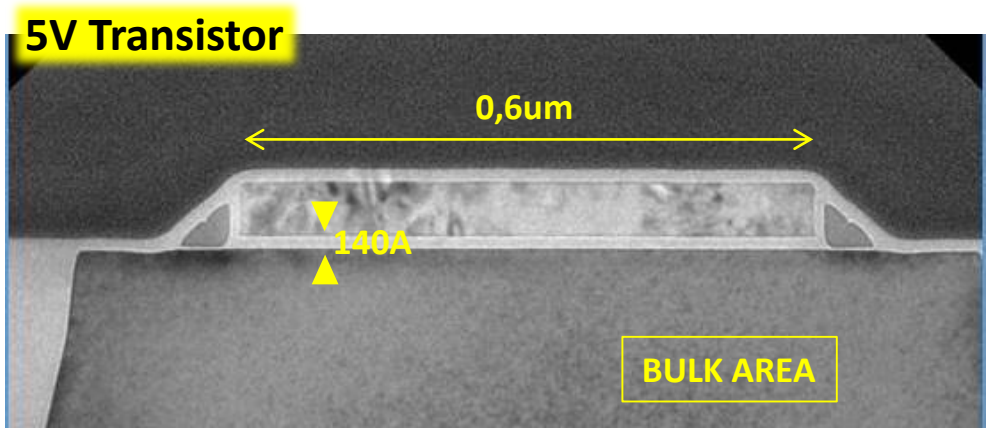


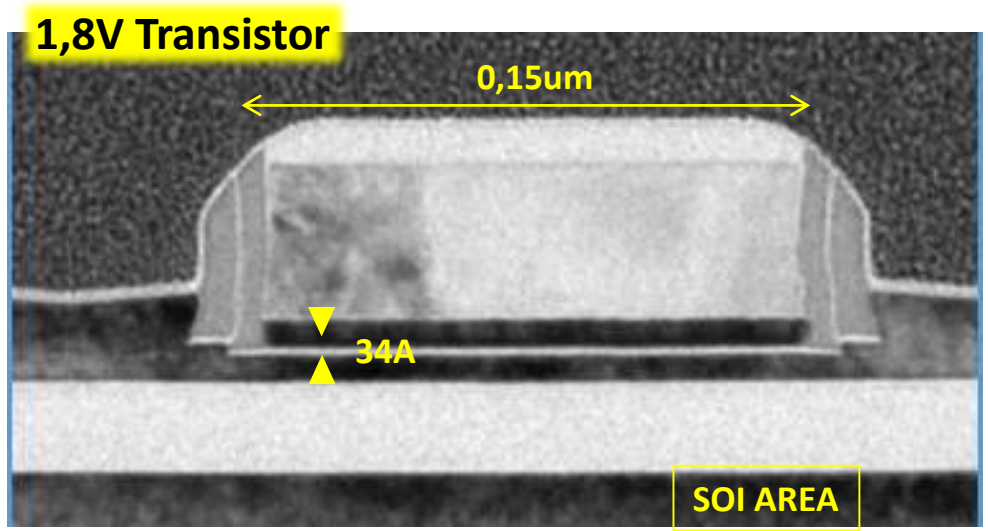
HD SRAM Cell (0,120um²)

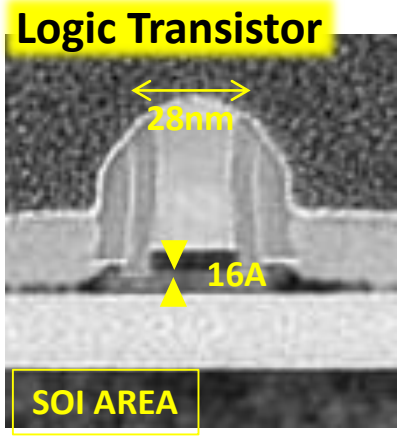


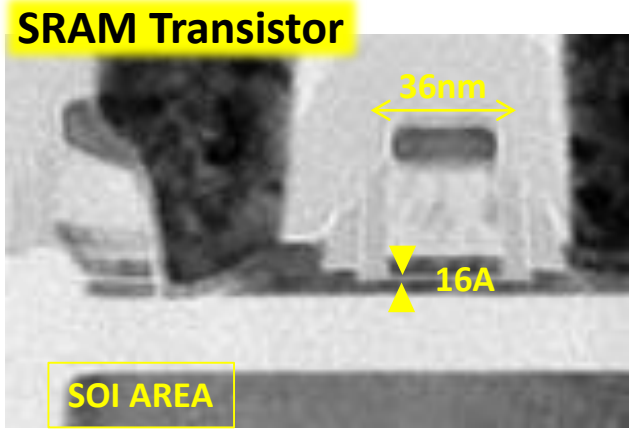
PCM Cell (0,036um²)

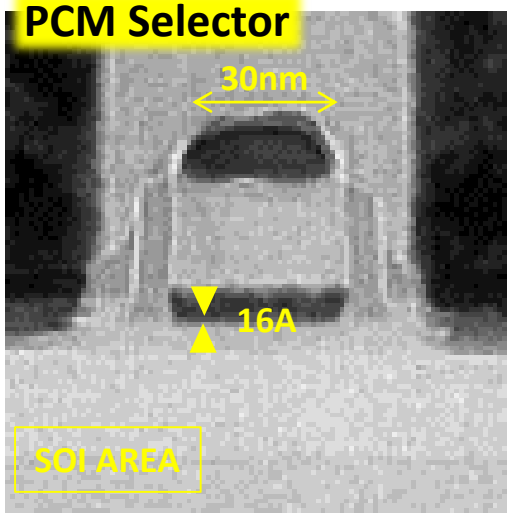
Devices Suite - Morphology





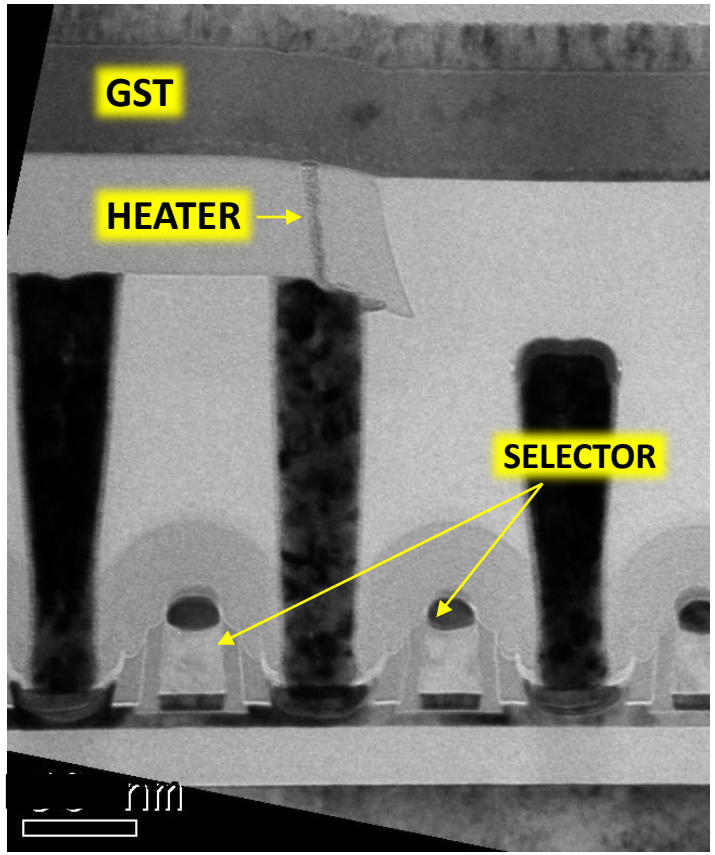




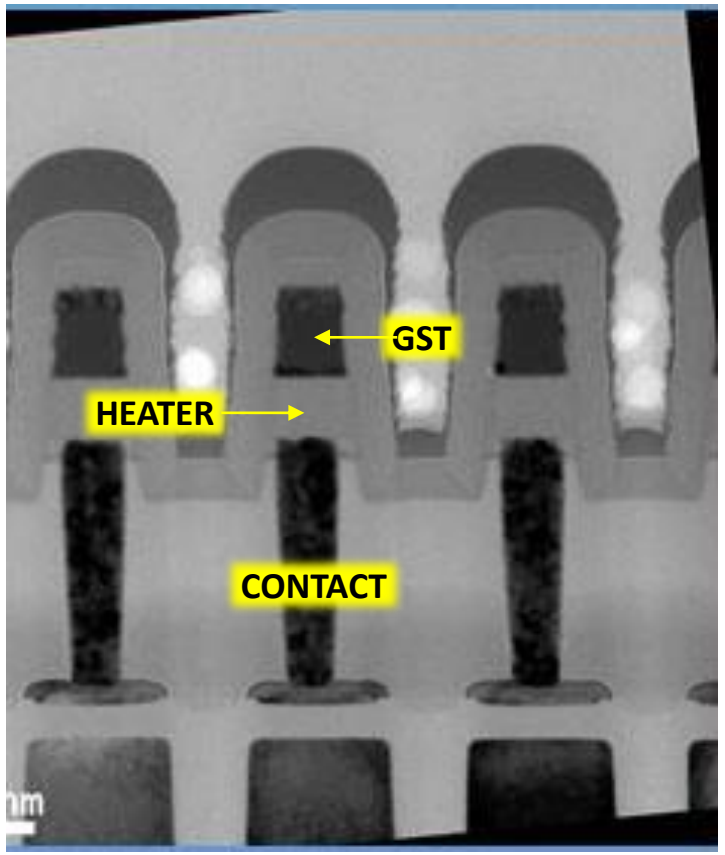


PCM Element Morphology

Cell in X direction



Cell in Y direction



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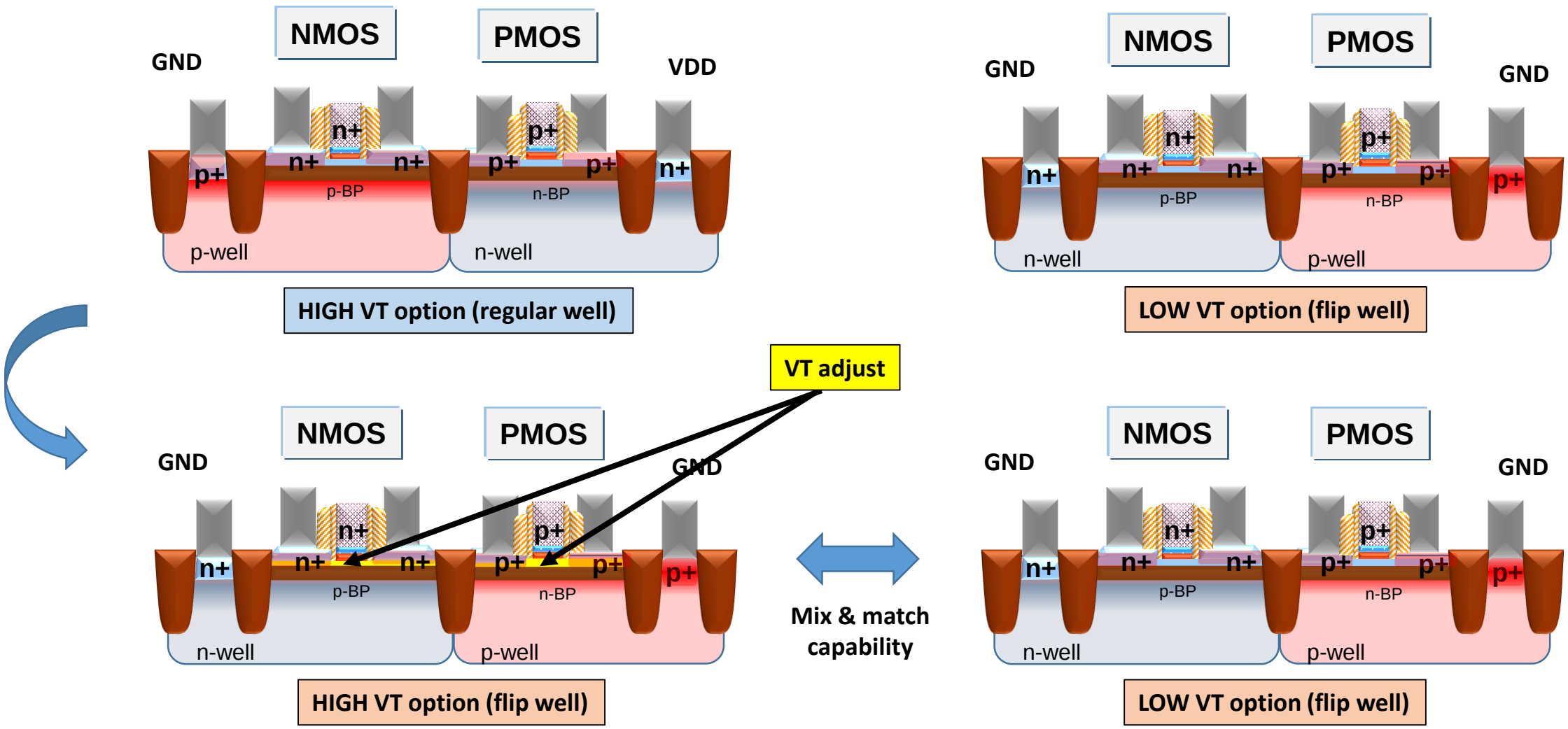
Devices Table

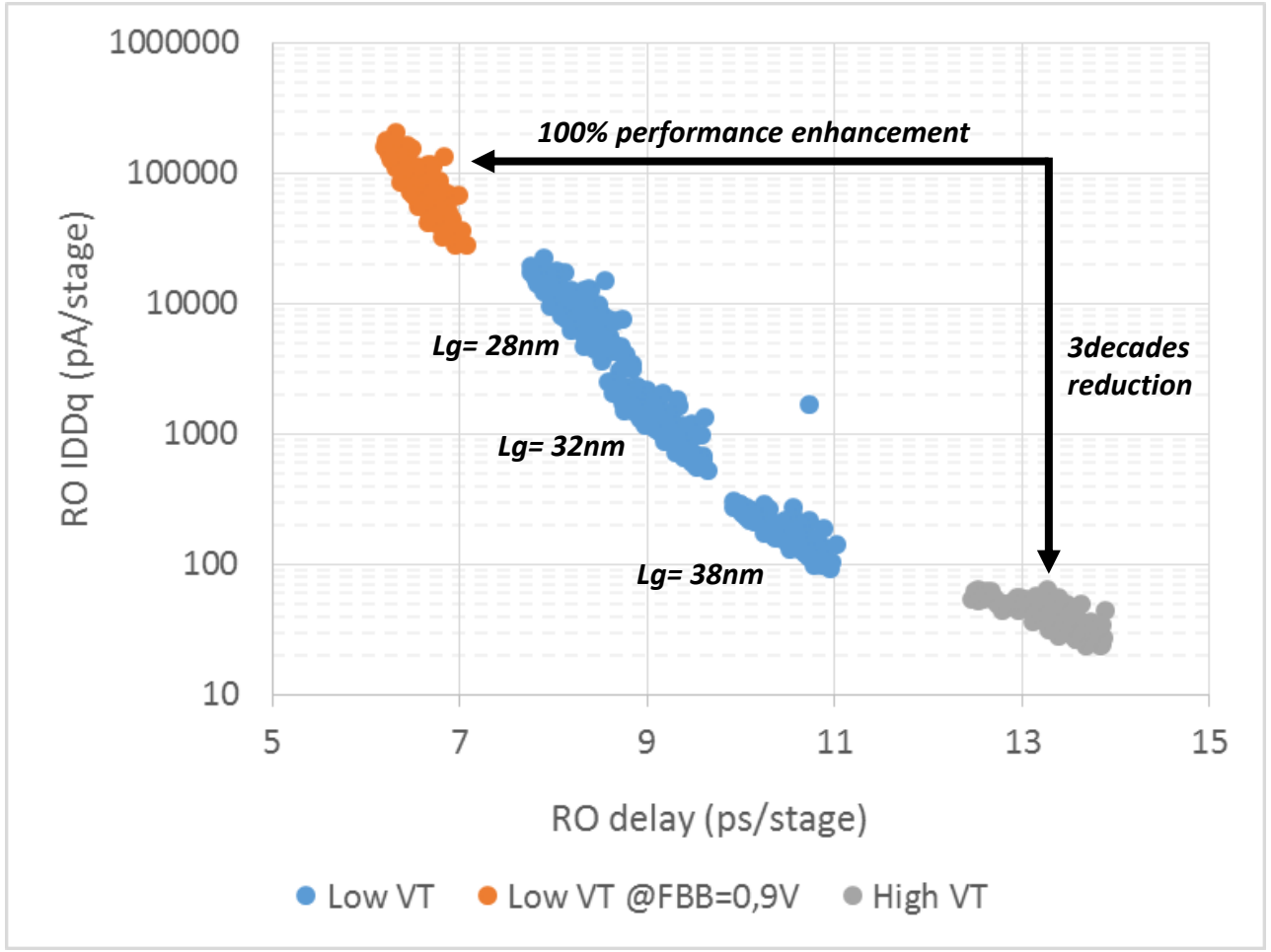
Devices	Logic devices	SRAM devices	I/O devices
VDDnom (Volt)	1	1	1,5 & 1,8
Lmin (um)	0,028	0,036	0,1 & 0,15
Tinv (nm)	1,6	1,6	3,4
VT options	HVT & LVT	LL & HS	RVT LVT
Substrate	FDSOI	FDSOI	FDSOI

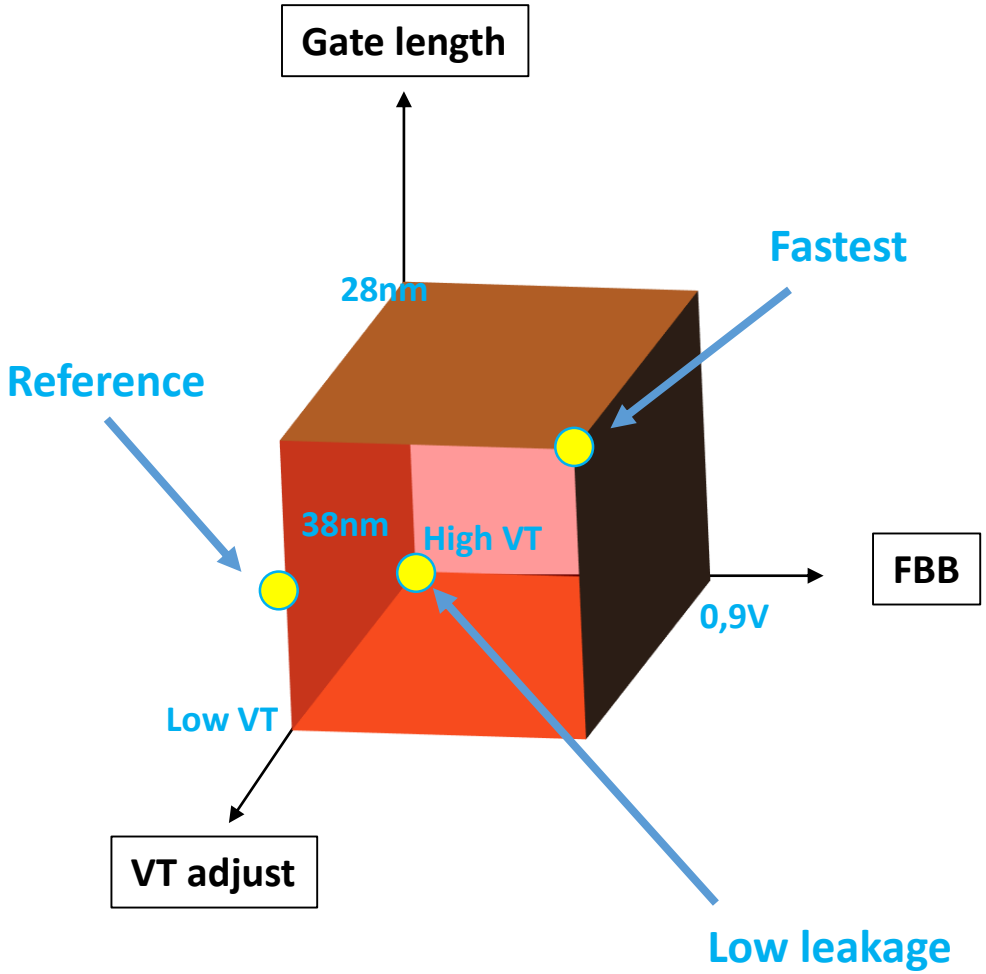
Devices	HV/Analog devices	ESD devices	
VDDnom (Volt)	5	1	1,8
Lmin (um)	0,6	0,048	0,15
Tinv (nm)	14	1,6	3,4
VT options	HVT	RVT	RVT
Substrate	BULK	FDSOI	BULK

Core Oxide Transistors – Well Scheme



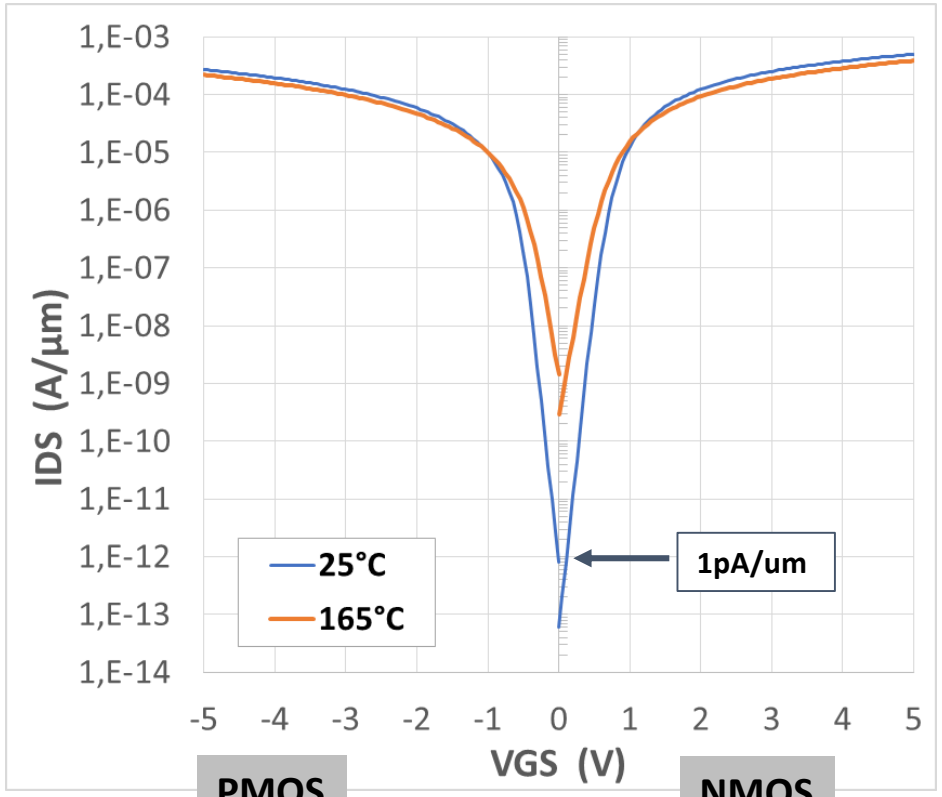
Digital Performance & Design Flexibility



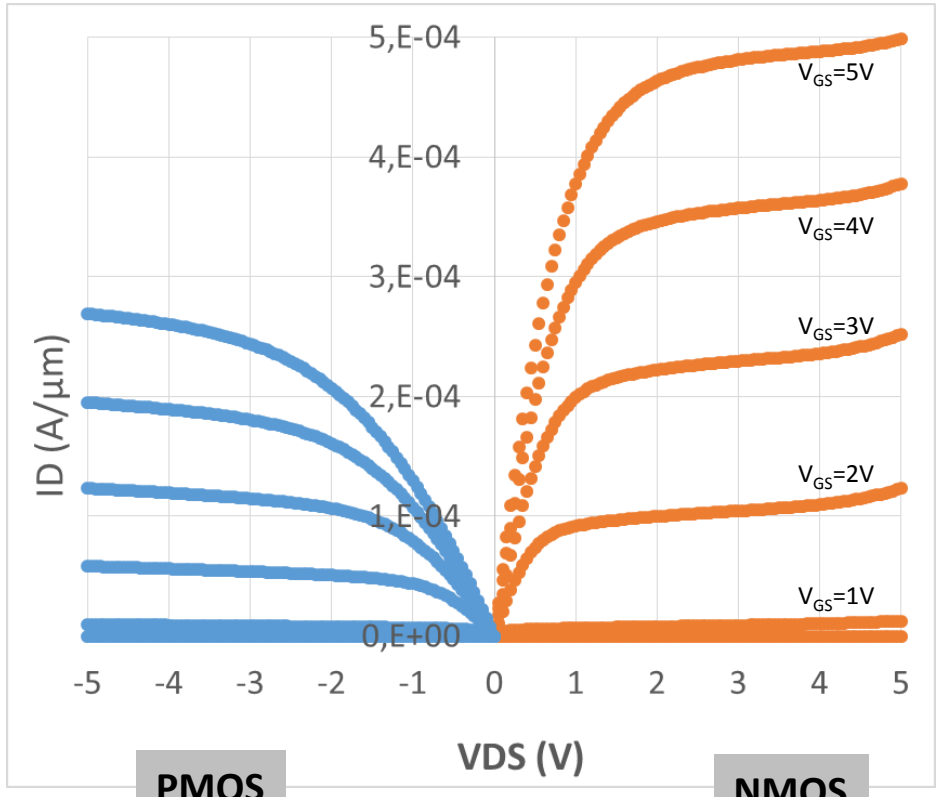


5V Transistors – Digital Characteristics

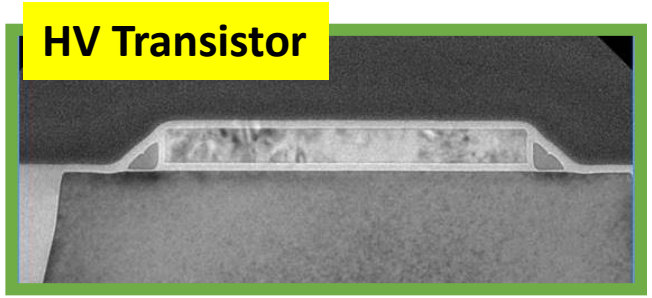
Transfer characteristic

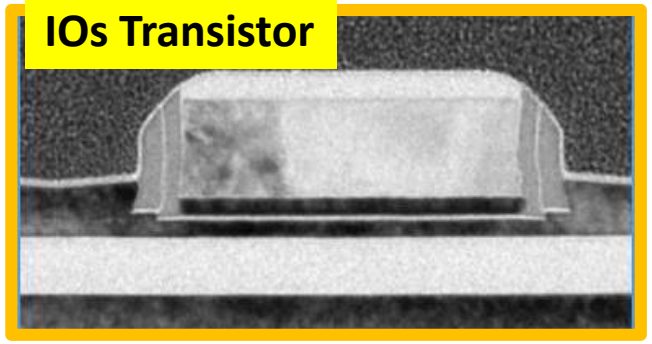


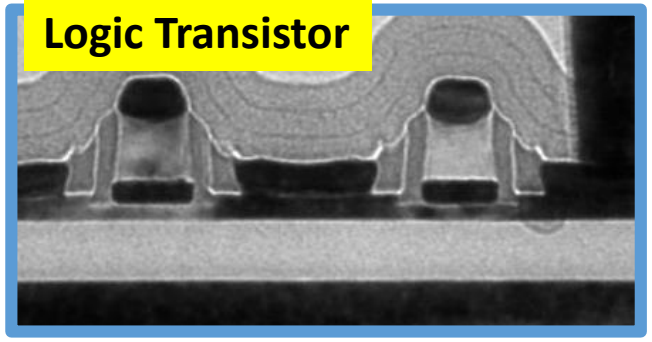
Output characteristic

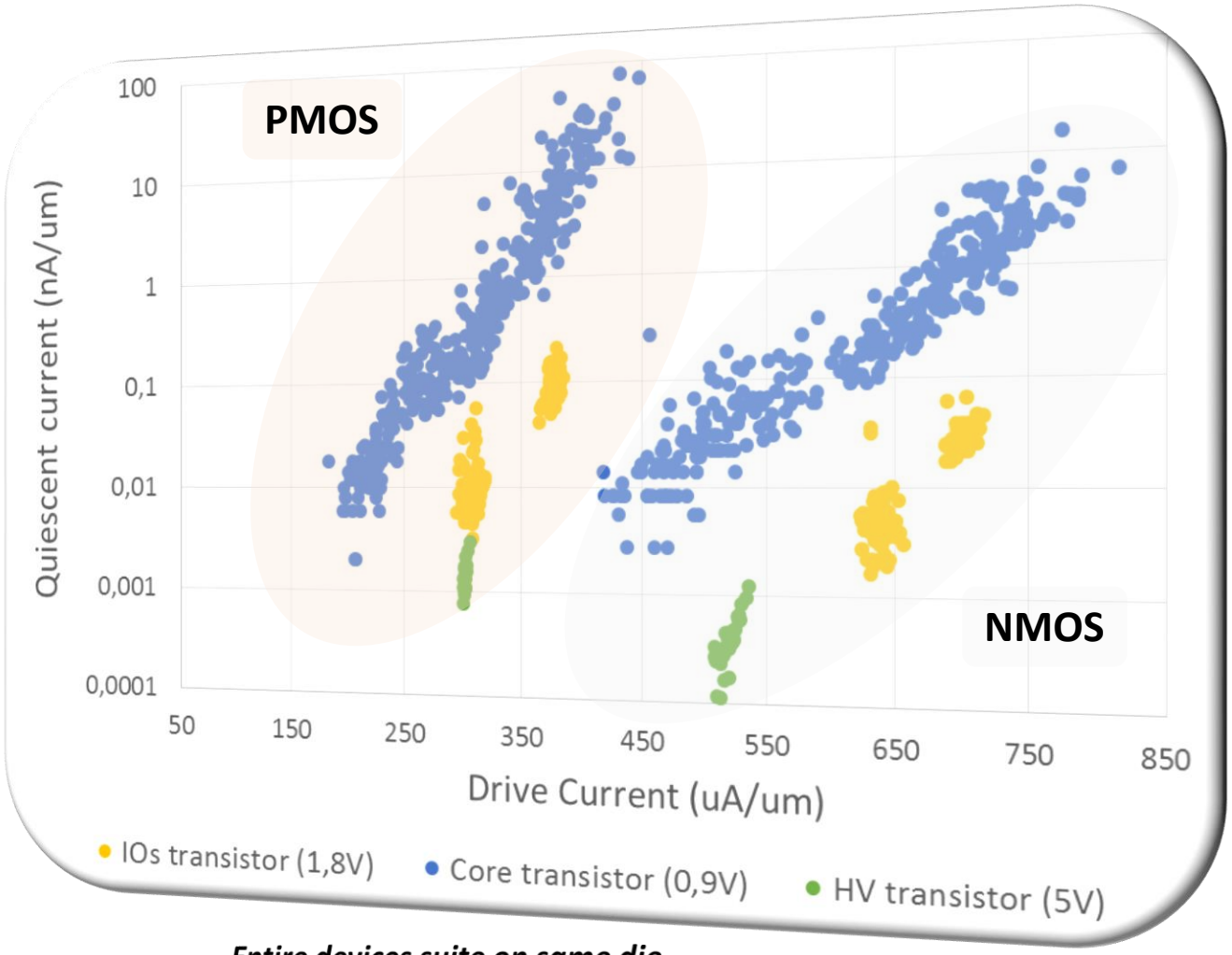


Triple Gate Oxide Devices Platform for Automotive Micro-Controllers



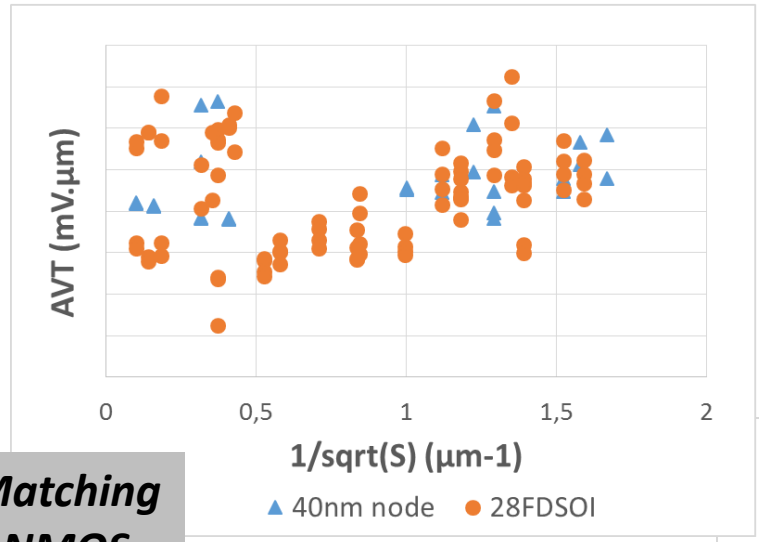




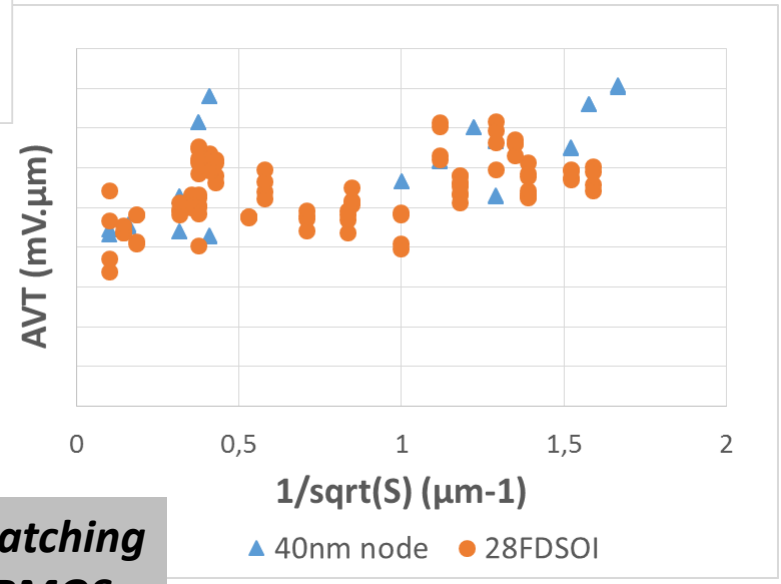


Entire devices suite on same die

5V Transistor – Analog Characteristics

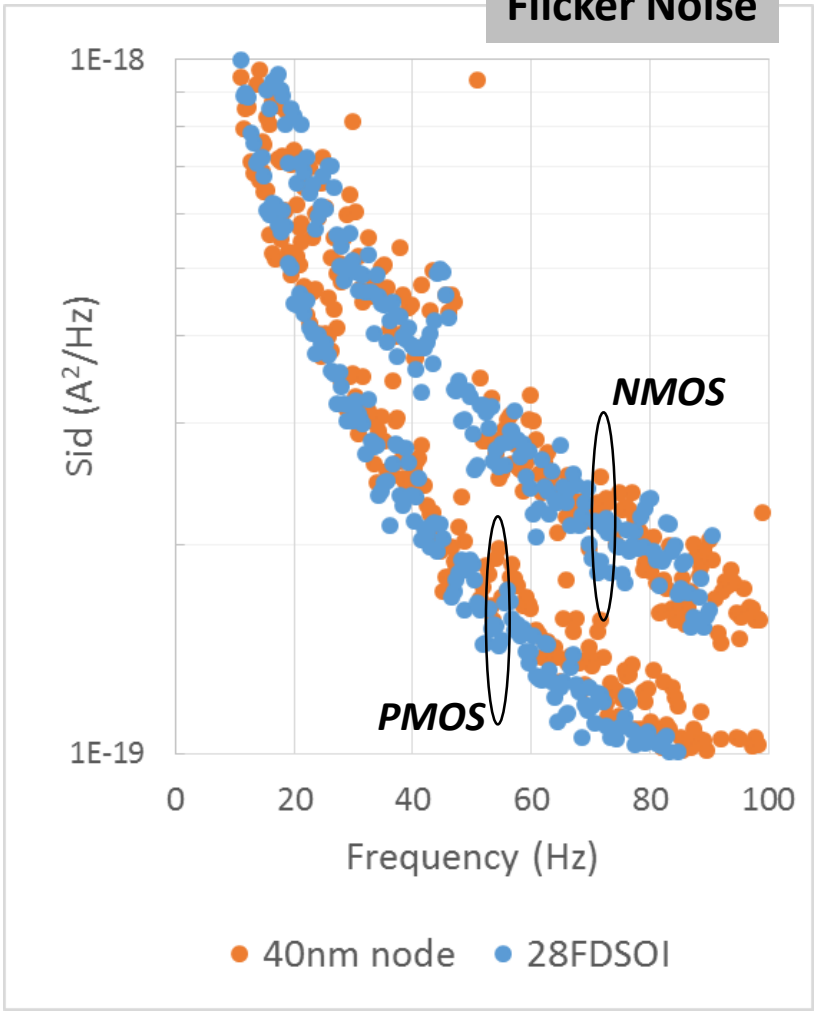


Matching NMOS

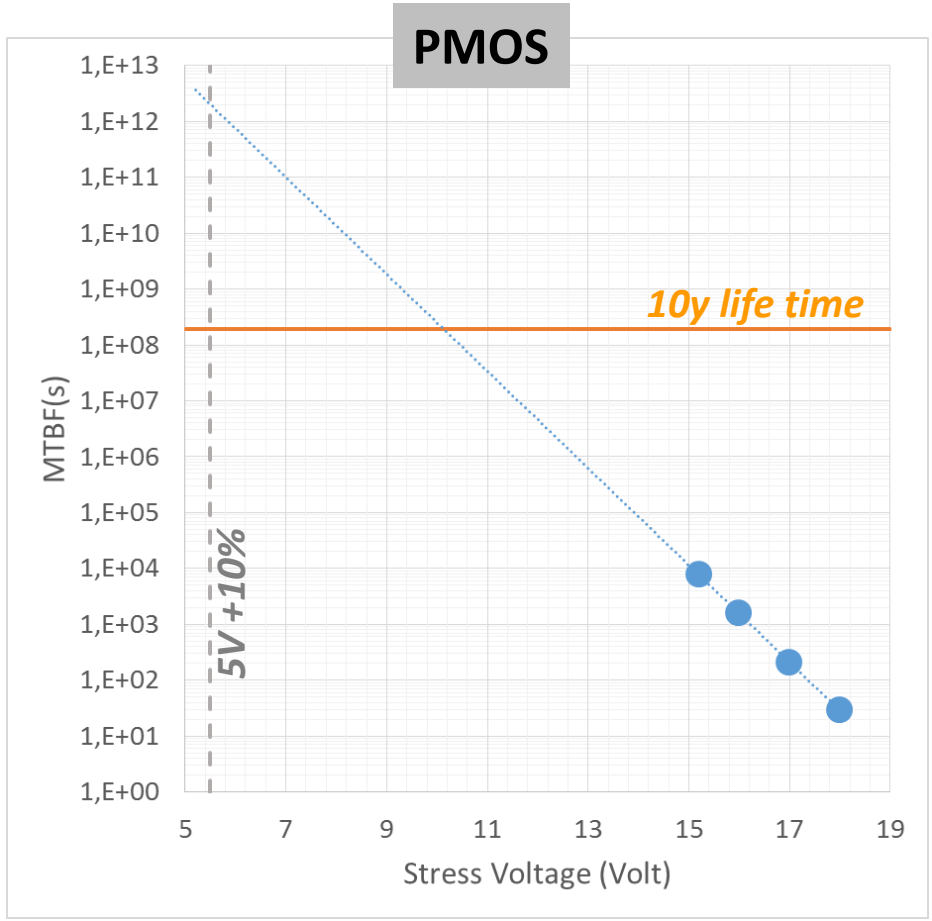


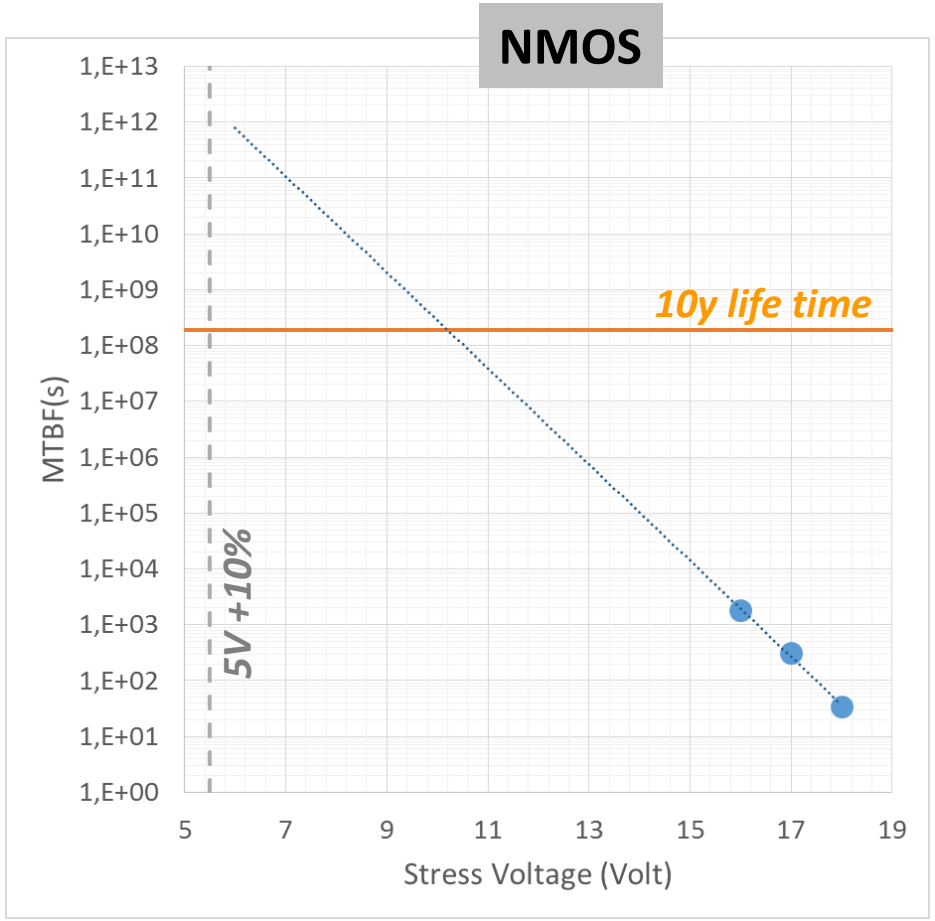
Matching PMOS

Flicker Noise

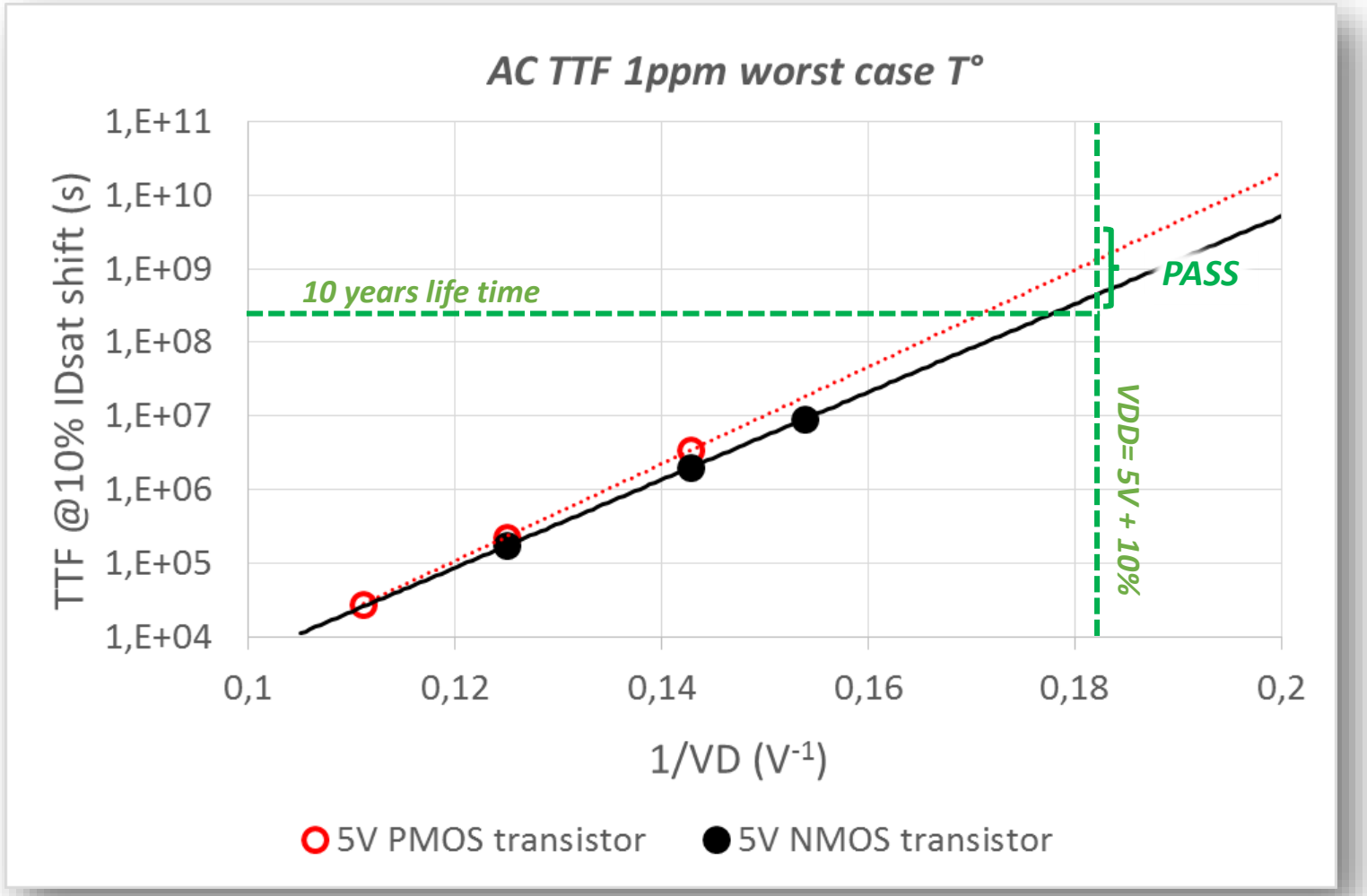


5V Transistor – Gate Oxide Reliability





5V Transistor – Hot Carrier Injection



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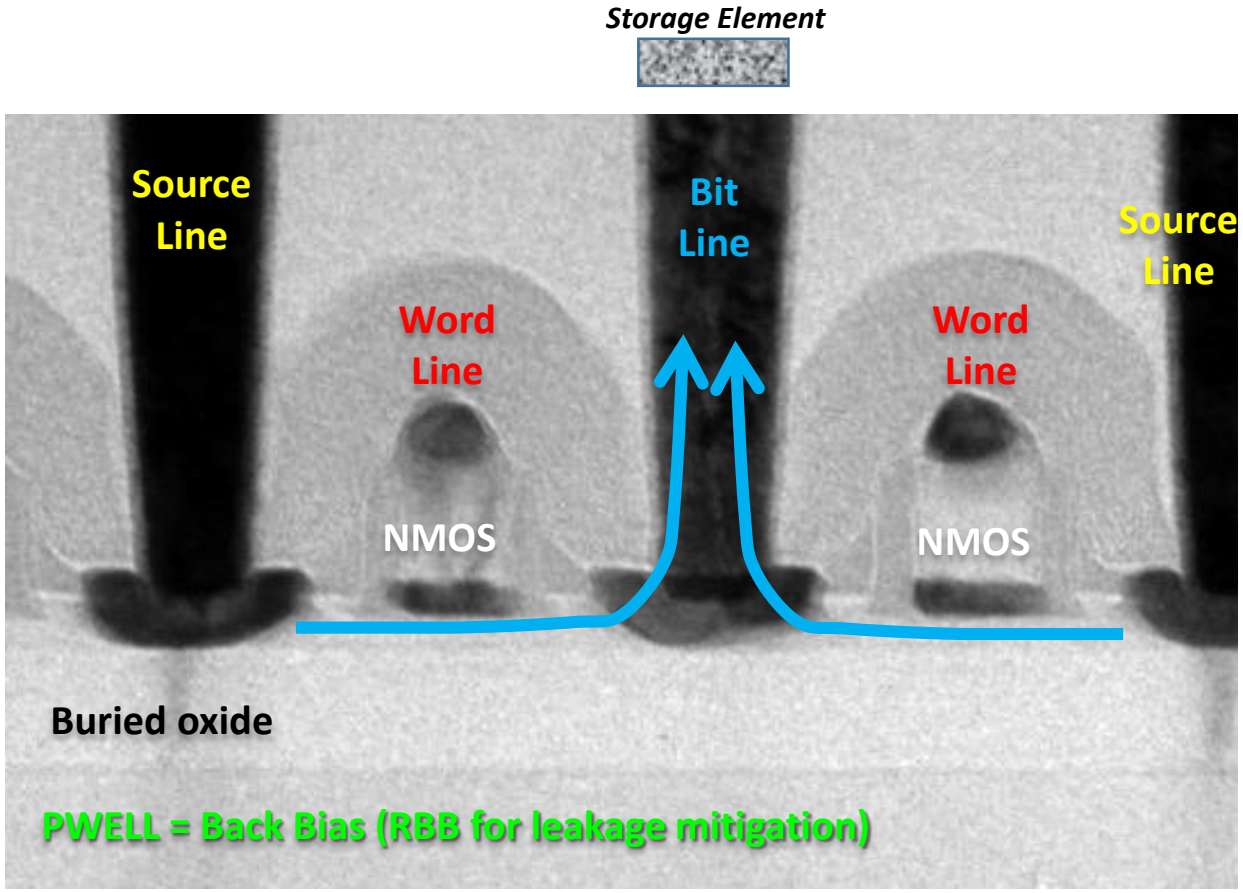
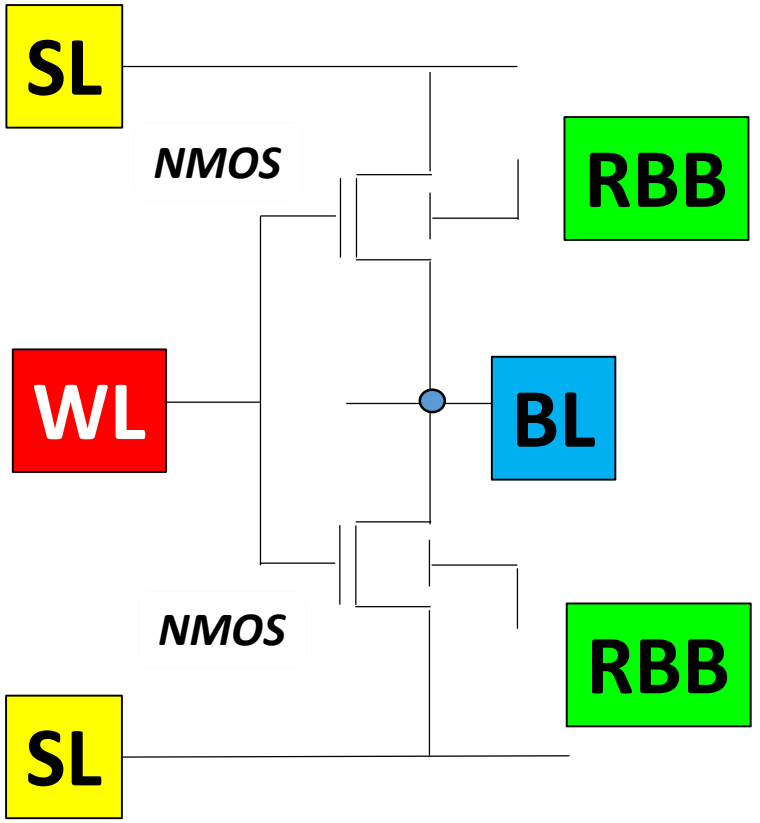
MOS Selector Requirements

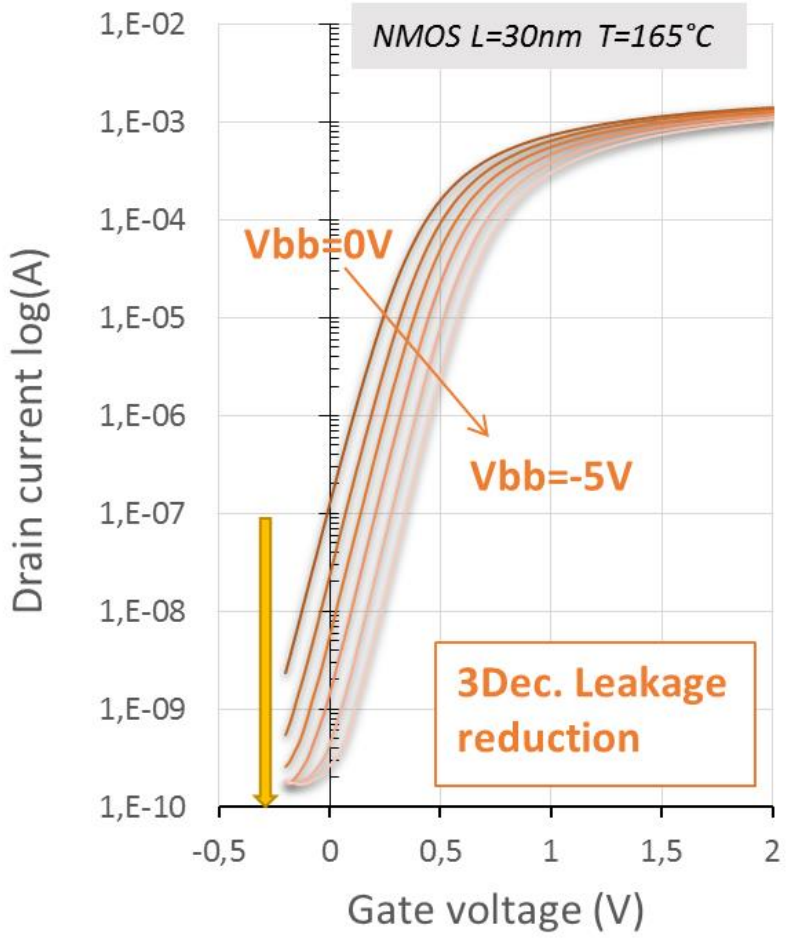
- Deliver high drive current for cell programming phase (reaching GST melting point)
- Use optimum W/L ratio reducing the cell area (cost effective solution)
- Reading operation at low Voltage
- Mitigate leakage current (IOFF) of un-selected Word-Line and selected Bit-Line during writing and reading steps

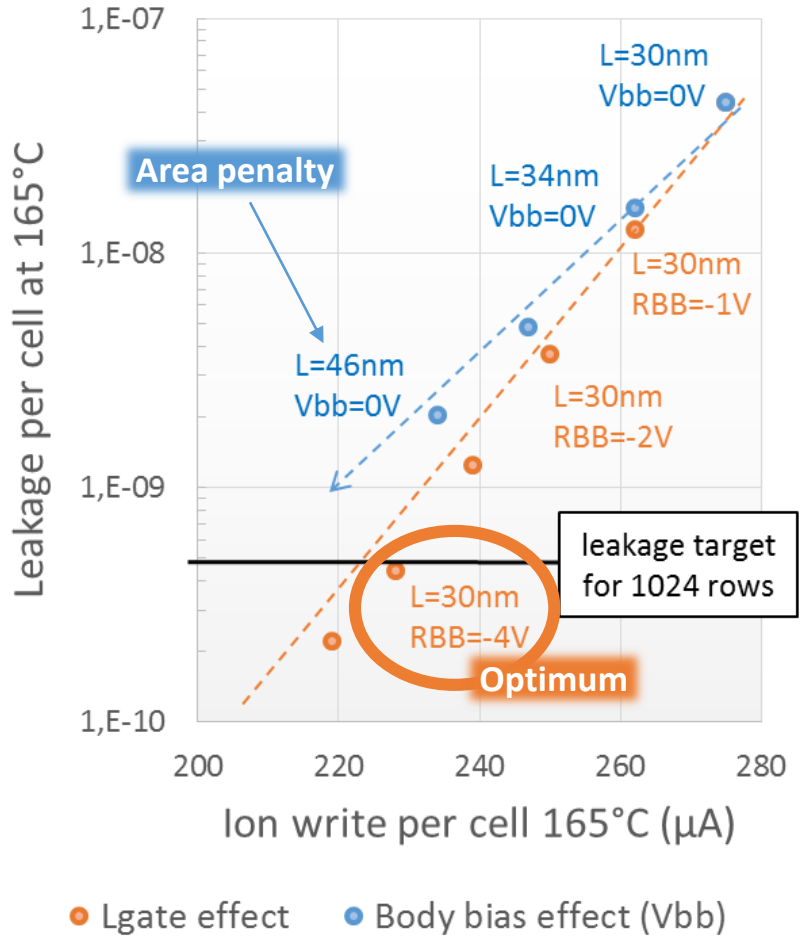
MOS Selector Structure



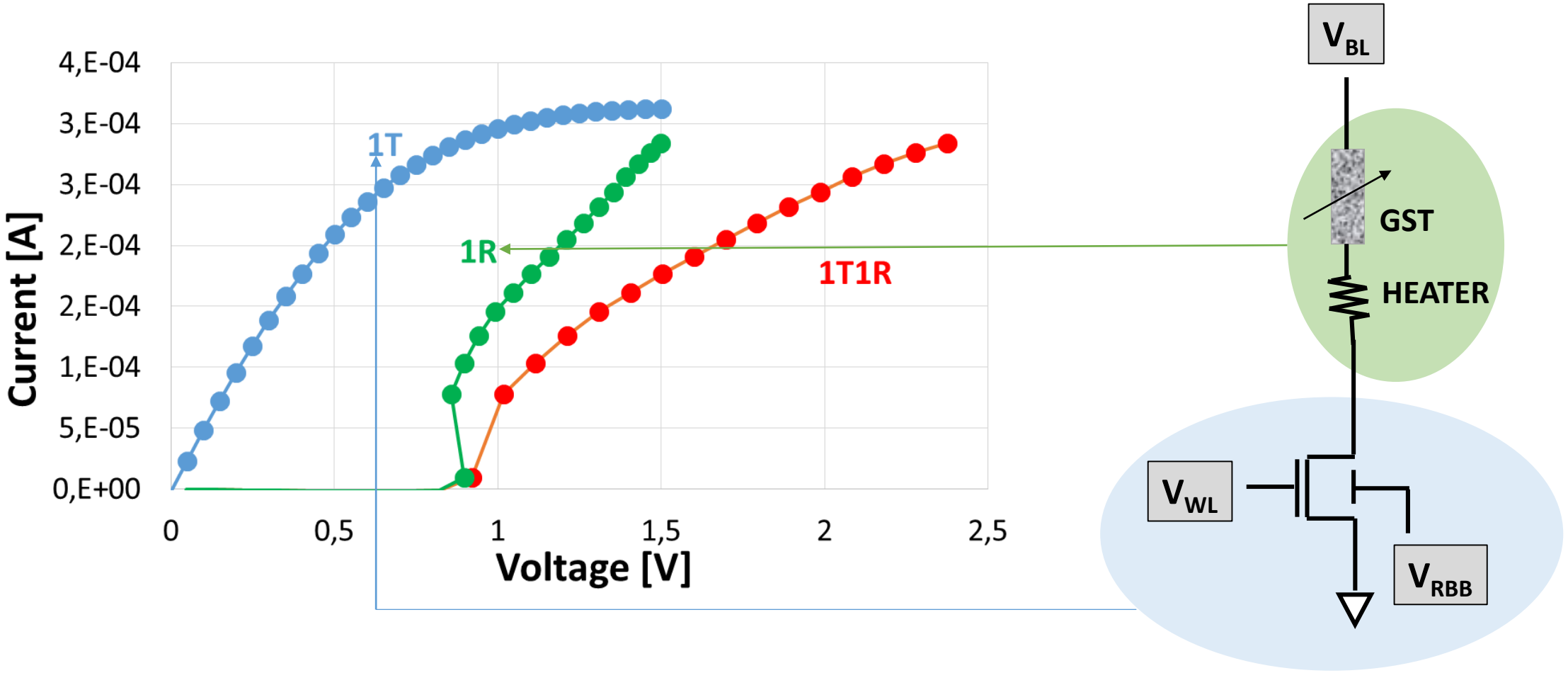


Enhanced MOS Selector with RBB Technique

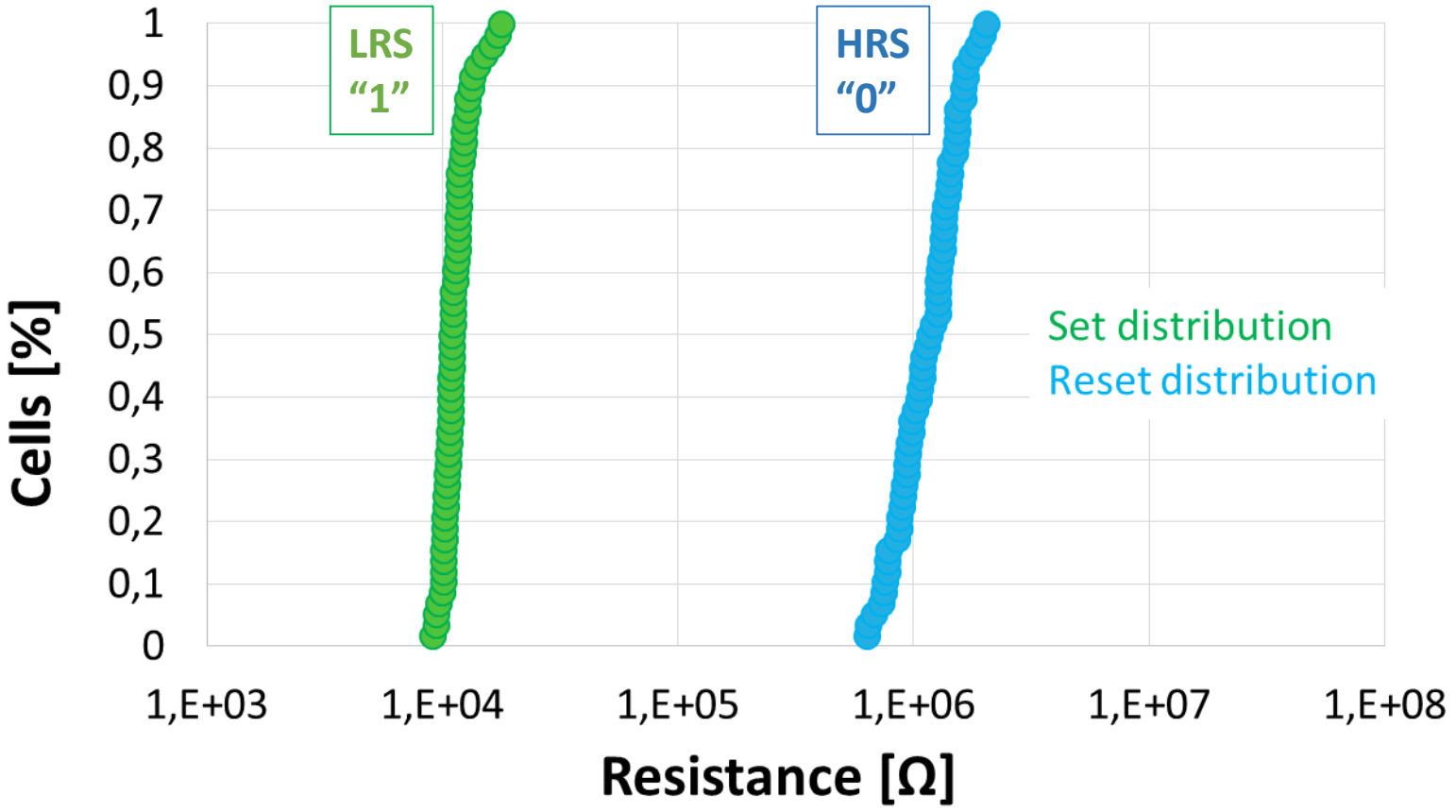




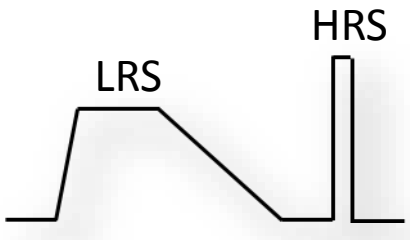
1T1R Analytical Cell Description

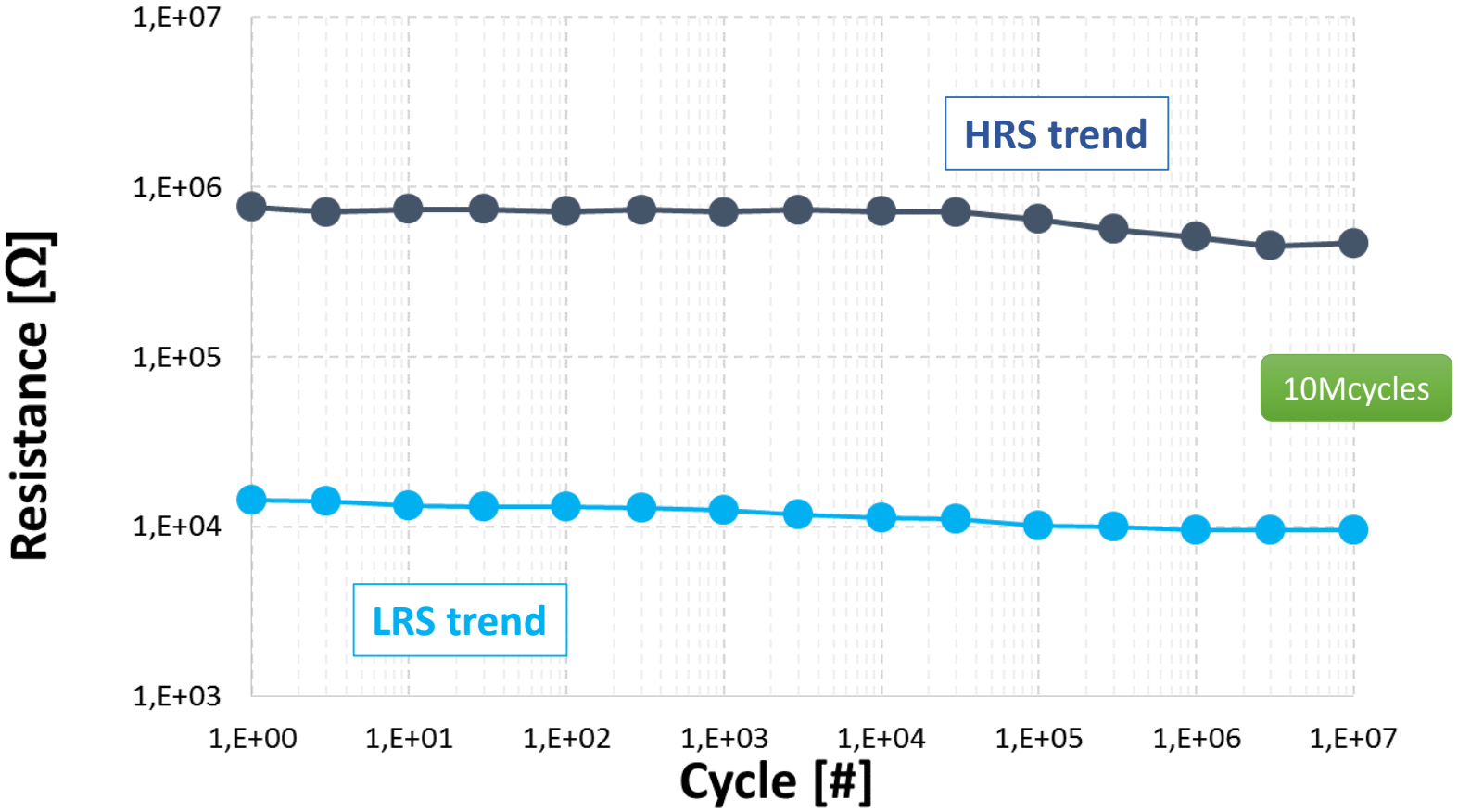


1T1R Analytical Cell Electrical Characteristics

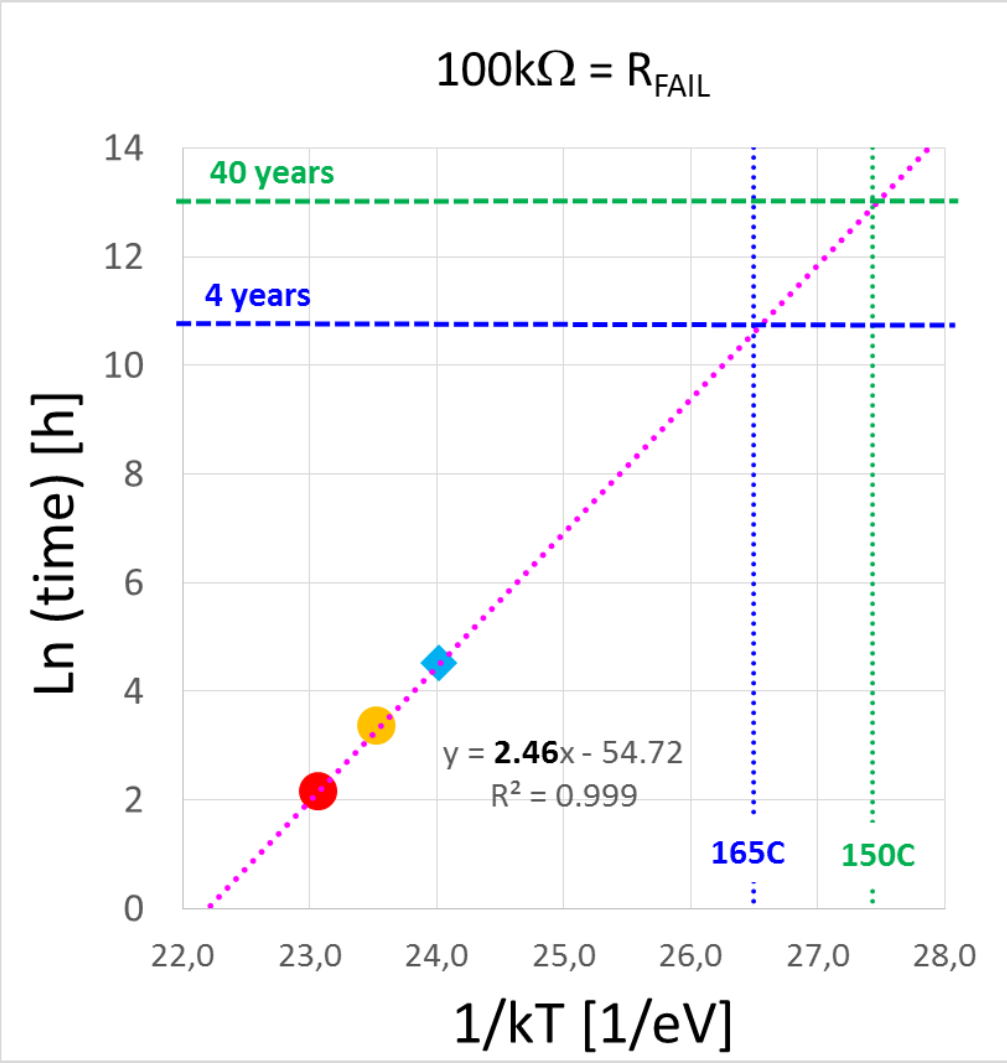


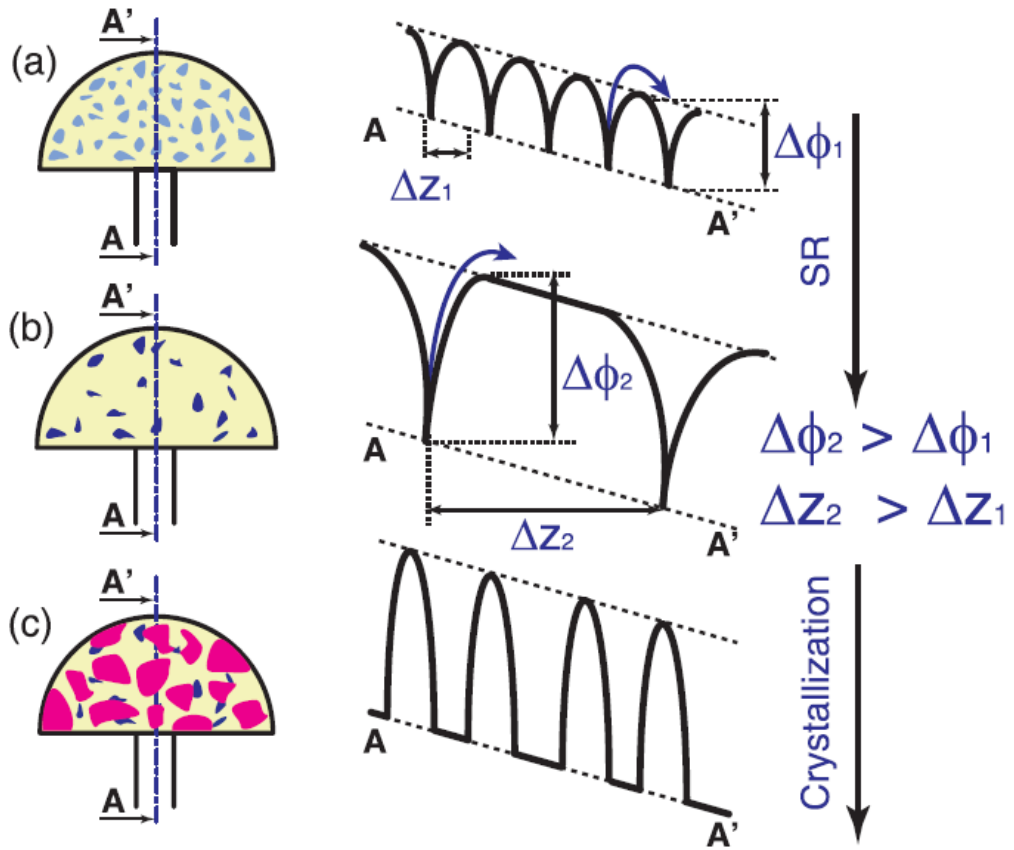
Analytical Cell Endurance





GST RESET Data Retention vs T°





N.Ciocchini et al
"Modeling Resistance Instabilities of SET and RESET States in Phase Change Memory with Ge-rich GeSbTe"
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 61, NO. 6, JUNE 2014

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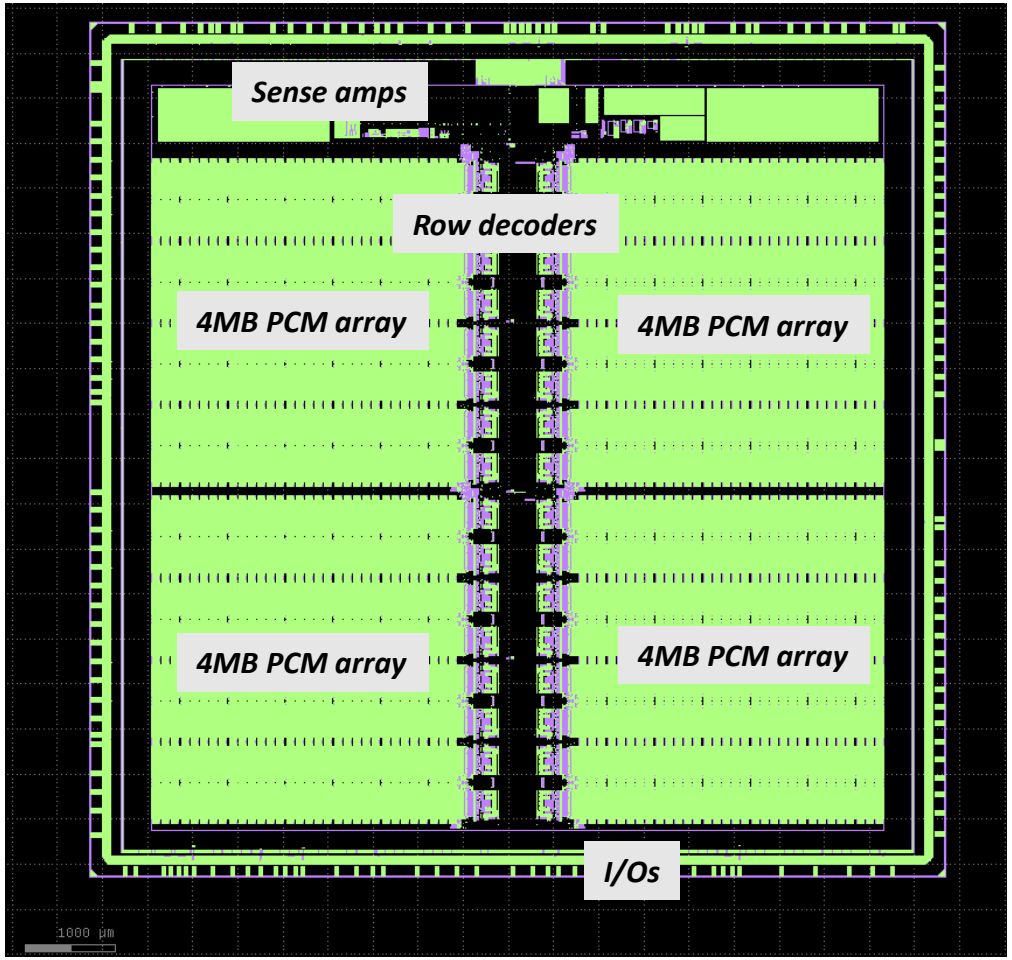
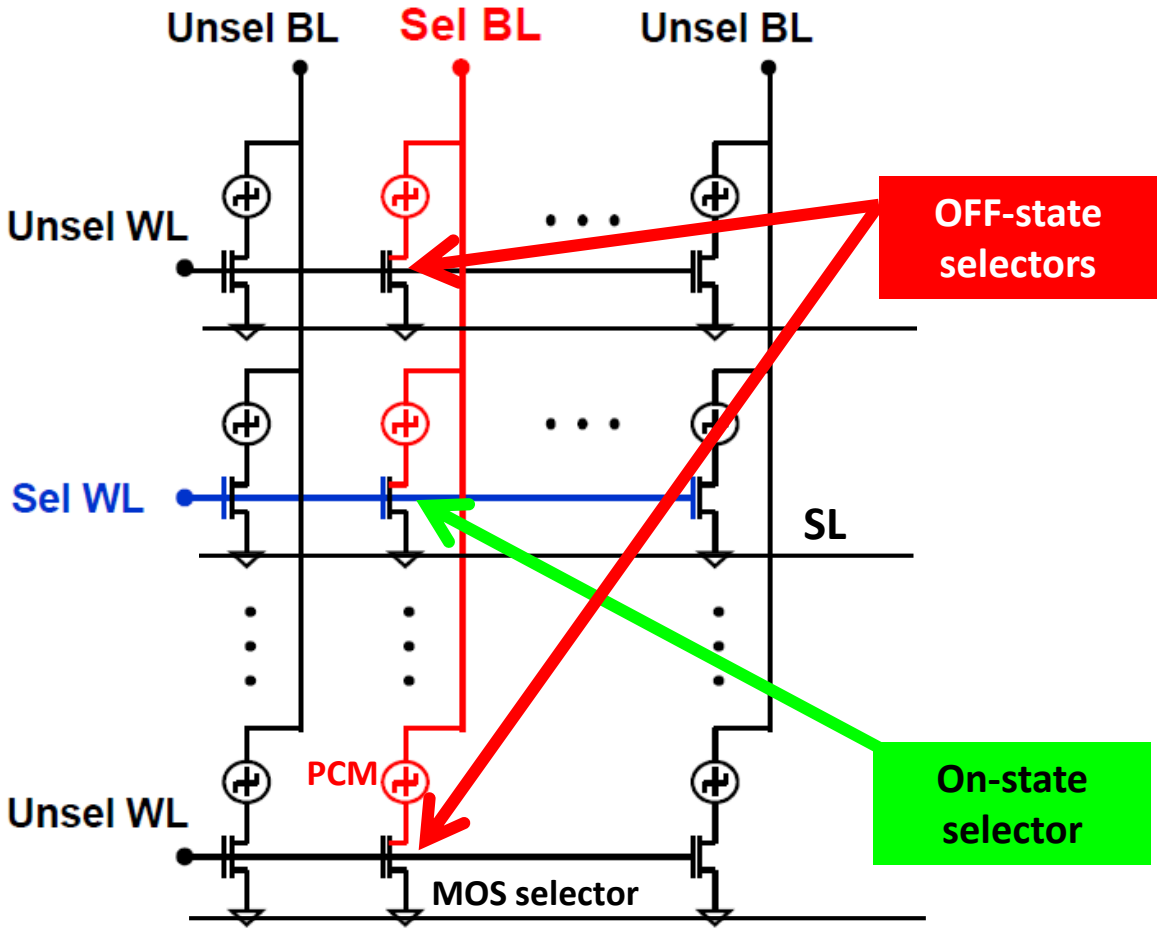
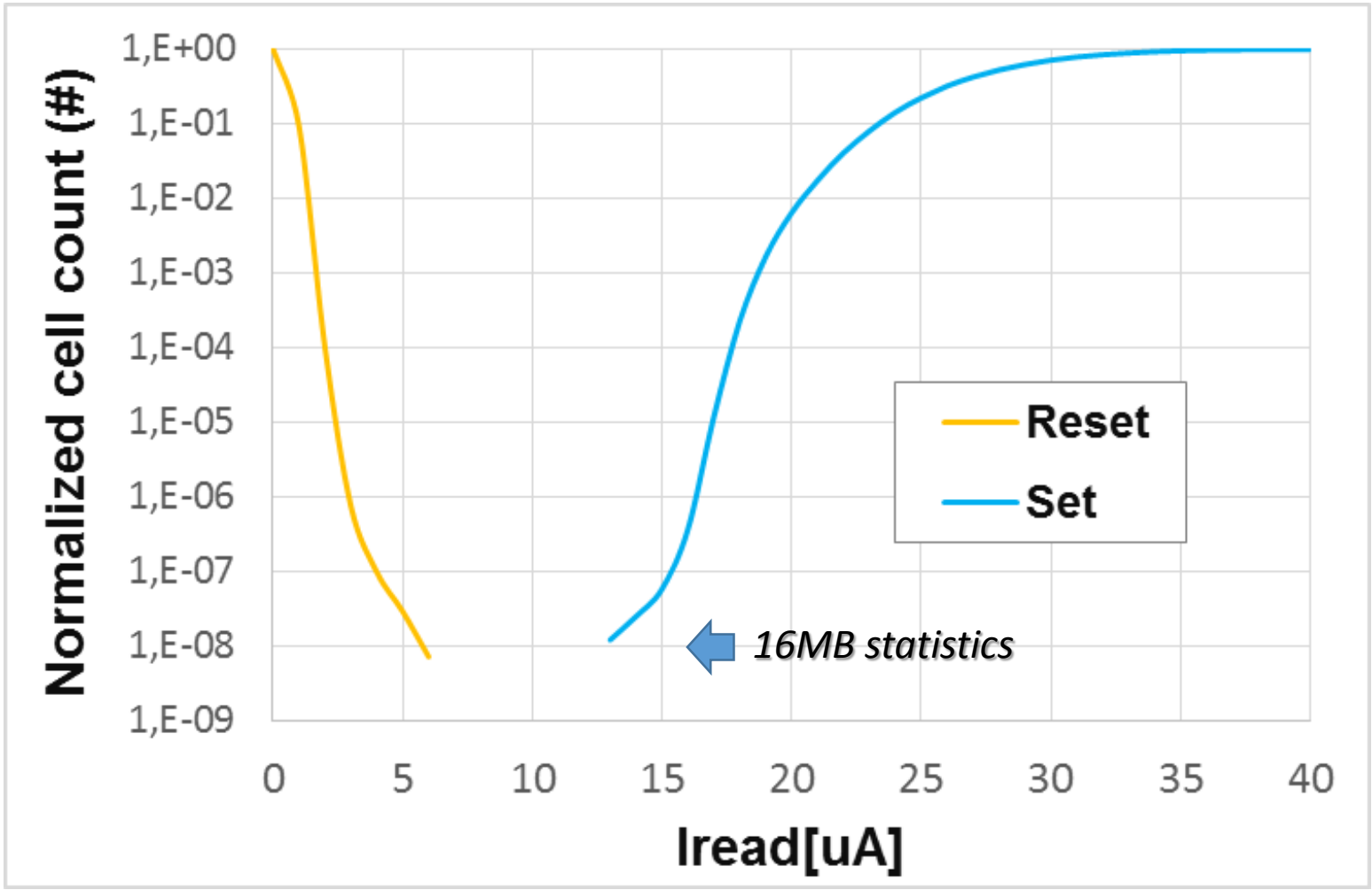
16MB Test Chip & Array Organization



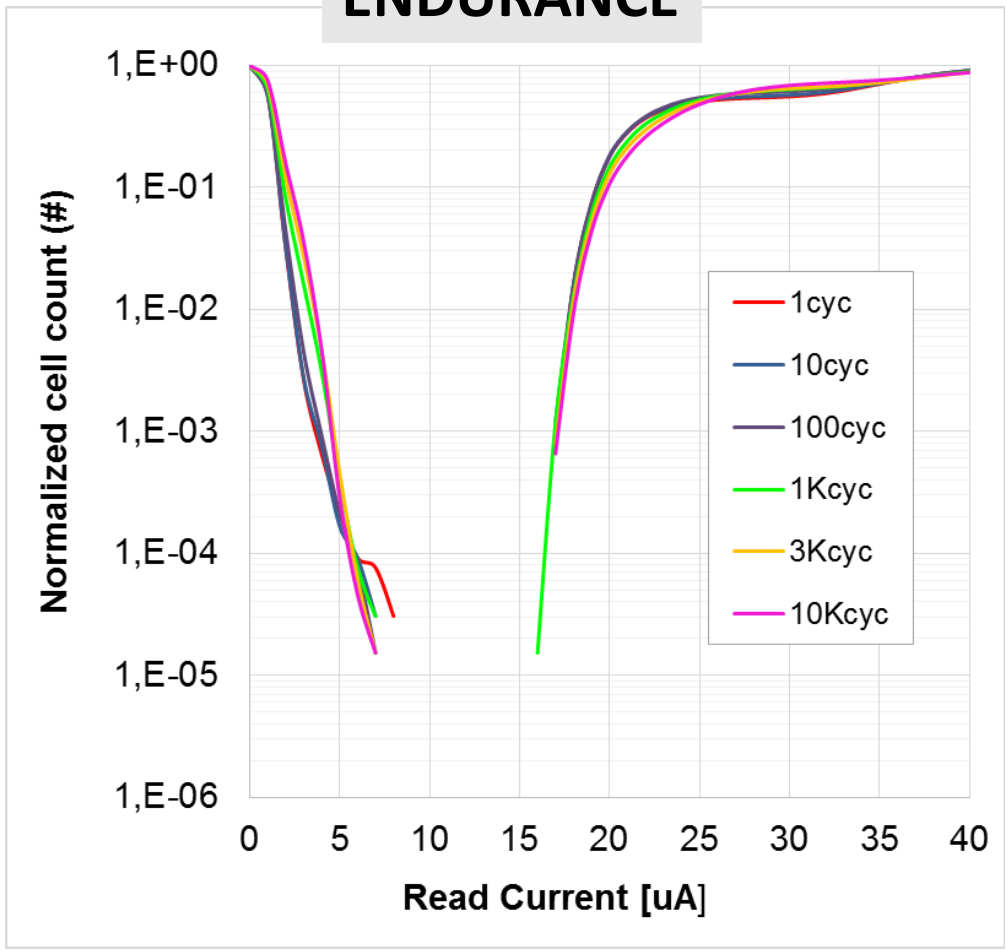


16MB SET & RESET States Distributions

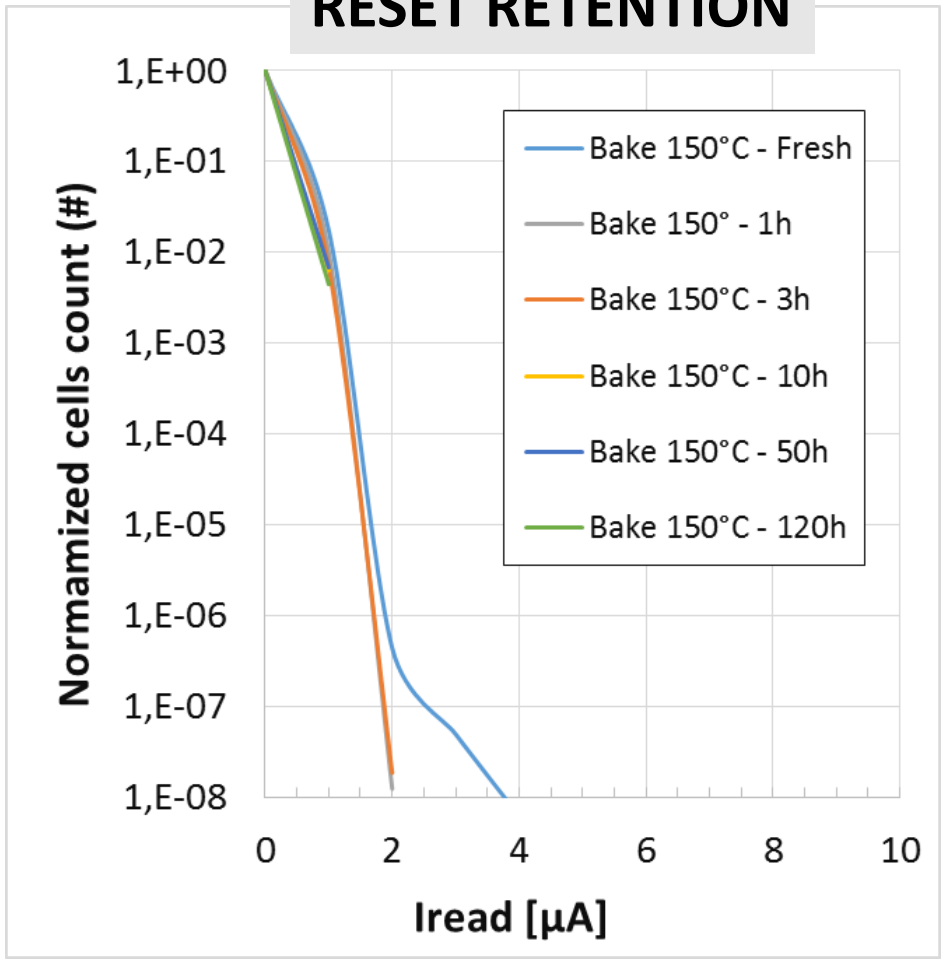


16MB Test Chip Reliability Figures

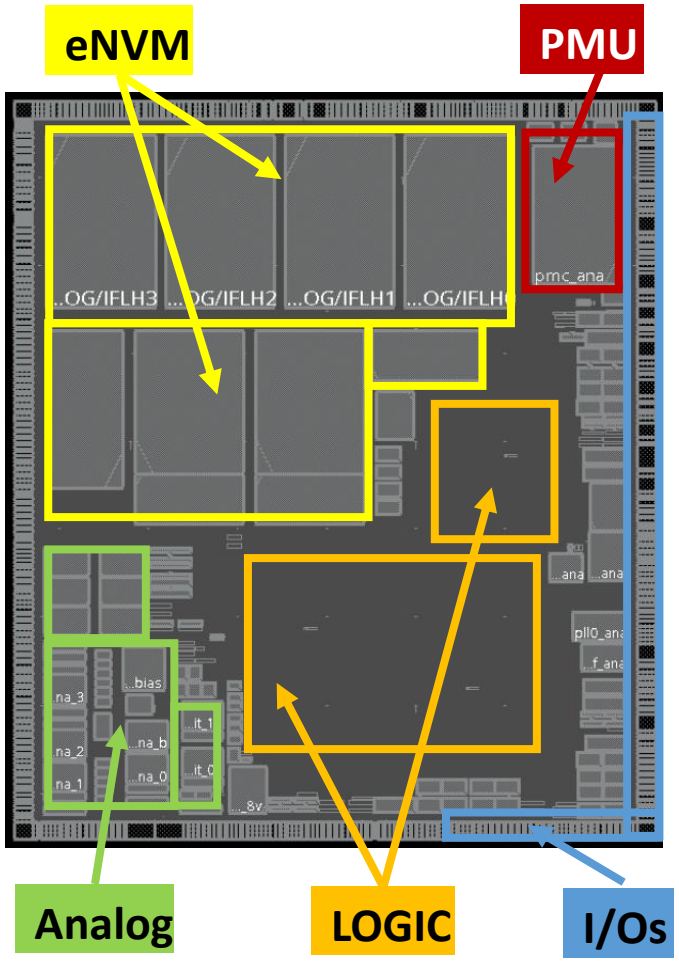
ENDURANCE



RESET RETENTION



MCU Demo Chip Preliminary Results



MCU content & specs	
Core	32b processor
SRAM	640KB
PCM	6MB
T range	-40C - 165C
Supply	0.9-1.1V / 4.5-5.5V

Preliminary reliability tests	
Soldering	Pass (30/30)
Data retention	Pass (30/30)
Endurance (10K)	Pass (30/30)

Outline of Presentation

- Introduction
- Technology description
- CMOS devices suite
- PCM analytical cell
- 16MB PCM array results
- Conclusions

Conclusions

- For the first time, Non volatile Phase Change Memory has been co-integrated with 28nm FDSOI technology for microcontroller applications in the Automotive market
- Triple gate oxide scheme enabling 5V transistor with FDSOI substrate for analog requirements in Automotive system
- Attractive leakage/drivability of FDSOI NMOS selector leveraging Reverse Body Biasing technique
- Fully validated 0,036um^2 PCM cell using optimized GST alloy showing robust endurance and good activation energy compatible with Automotive criteria (150°C achieved)
- Excellent PCM current distributions demonstrated on 16MB array before and after 150°C bake without degradation after 10k cycles

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Thank You for your attention !

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