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Application Note

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A Strategy for Routing the MPC8544E in a Six-Layer PCB

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This application note is a design guide to assist the customer in creating a low-layer, low-cost, PCB design when using the MPC8544E device. Key items of discussion include assumed PCB stackup, power delivery, and proper signal referencing. Additionally, layout plots for the device fan-out are also included.

NOTE

The schematic and Gerber data shown within this application note are intended merely to demonstrate the fan-out and power delivery strategy necessary to achieve a six-layer PCB. The schematic and Gerber data does not include all the decoupling, nor do they show all the necessary pull-ups and AC caps required outside the BGA fan-out area. This level of detail is captured as part of the MPC8544E development system.

Contents

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1 References

Table 1 lists references mentioned in this application note, as well as useful resources for further reading.

Table 1. References

Document	Source
IPC Standards: IPC-D-275 IPC-2221A IPC-2152	www.ipc.org
New Correlations Between Electrical Current and Temperature Rise in PCB Traces Johannes Adam, Flomerics Ltd.	20th IEEE SEMI-THERM Symposium 0-7803-8363-X/04/$20.00 ©2004 IEEE www.flomerics.com/flotherm/technical_papers/t341.pdf
Current-Carrying Capacity, Martin Tarr, University of Bolton	www.ami.ac.uk/courses/ami4817_dti/u02/pdf/meah0221.pdf
Interactive trace-width calculator	http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator

2 Ballmap Organization

The MPC8544E is a 783-pin, 28 × 28 BGA array. The bus organization of the device is shown in Figure 1.

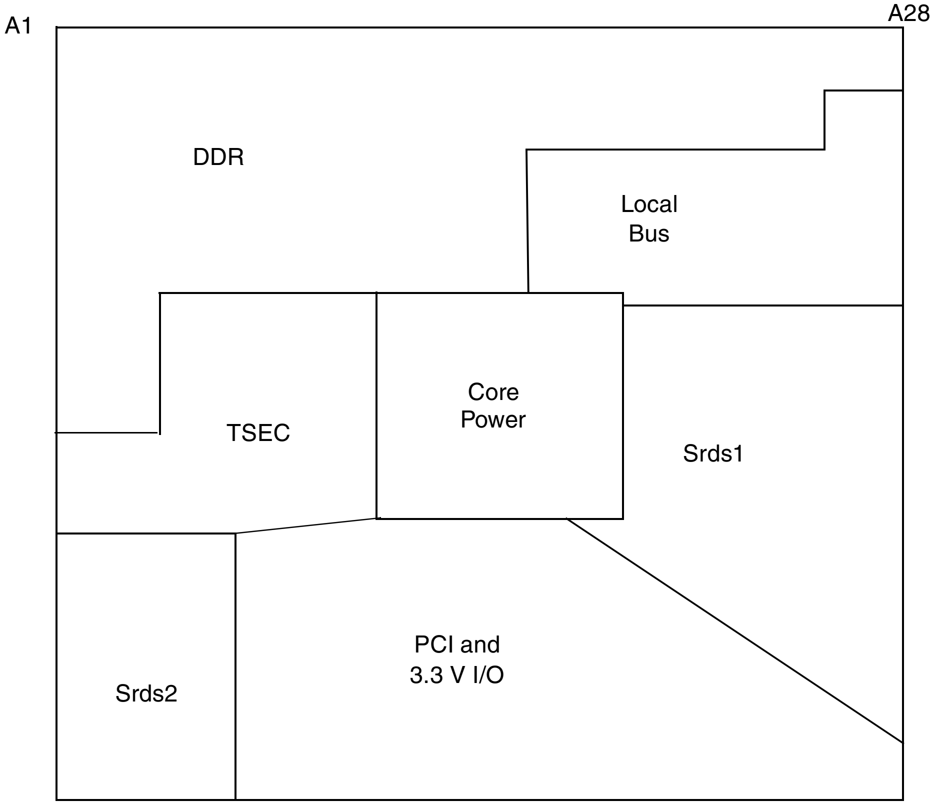


Figure 1. MPC8544E Bus Groupings (viewed from the top of the device)

3 Interface Support in Six Layers

Though the MPC8544E device can be fully broken out in six layers, there are a handful of signals that are not necessarily optimal from a signal integrity perspective, mainly due to splits in the reference plane. Such cases are very limited and are, therefore, manageable. Table 2 enumerates the MPC8544E interfaces and indicates whether there is proper signal referencing in the six-layer PCB fan-out example.

Table 2. Interface Support in Six Layers

Interface	Configuration	Reference Plane	Comment
DDR2	Full 64-bit + ECC	DDR Data—GND DDR ADDR—1.8 V DDR CLKs—1.8 V	Fully supported.
ETSEC	RGMII	RGMII I/O—2.5 V GTX_CLK125—GND	Both Ethernet ports can be fully broken out in RGMII mode. Some signals cross split boundaries; therefore, stitching caps would likely be beneficial.
POR Config	All user defined POR pins are accessible.	GND and PWR	Fully supported. Some POR pins cross split boundaries, but because they are static, there is no concern.
PCI	Full 32-bit PCI	GND and PWR	
LB	All signals are accessible	GND and PWR	LB_LAD[23:31] cross split boundaries. These signals are not edge sensitive, therefore imperfections in their transitions can be managed. Use of stitching caps could be used.
SERDES1	All eight lanes accessible	GND	Fully supported
SERDES2	Both lanes accessible	GND	Fully supported
IRQ	All IRQs (0–11) and IRQ_OUT usable	GND and PWR	Fully supported
JTAG/COP	All signals are accessible	GND and PWR	Fully supported
DUARTS	Both UART ports are fully accessible	GND and PWR	Fully supported
Power pins and AV_{DD} filters	All unique powers accessible	N/A	Fully supported
I2C	Both I2C port accessible	GND and PWR	Fully supported
Clocking	SYSCLK and RTC accessible	GND and PWR	Fully supported

4 Board Stackup Considerations

This section presents the considerations associated with the PCB and its stackup. Table 3 lists the target impedances needed in a six-layer design.

Table 3. Target Impedance for a Typical MPC8544E Design

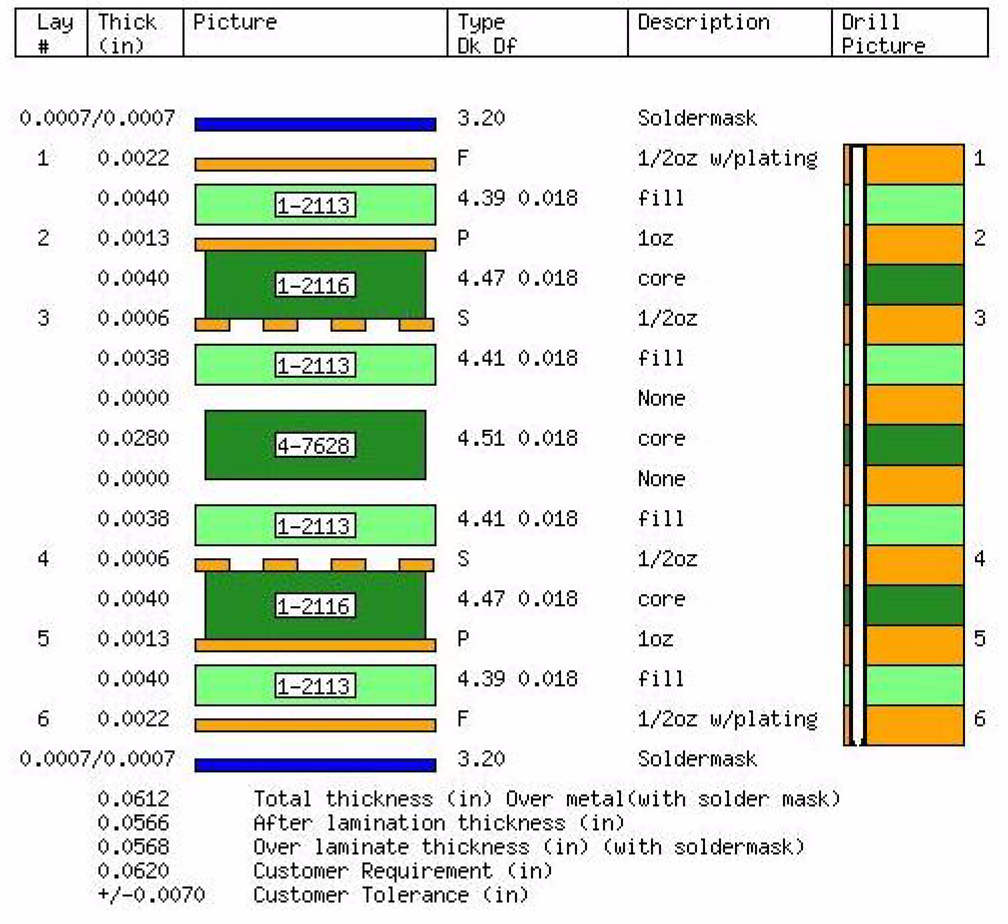
Interface	Connection	Target Impedance
DDR2	MPC8544E-to-DDR2 memory	Single-ended impedance = 55–60 Ω Differential impedance = 100 Ω ± 10%
SERDES1 (PCIe)	MPC8544E-to-PCIe connector or device	Microstrip Single-ended impedance = 60 ± 15% Differential impedance = 100 Ω ± 20% Stripline Single-ended impedance = 60 ± 15% Differential impedance = 100 Ω ± 15%
SERDES2 (SGMII/PCIe)	MPC8544E-to-connector or device	Microstrip Single-ended impedance = 60 ± 15% Differential impedance = 100 Ω ± 20% Stripline Single-ended impedance = 60 ± 15% Differential impedance = 100 Ω ± 15%
All other MPC8544E signals	MPC8544E-to-connector or device	Single-ended interface = 55–60 Ω
Other system Items:		
Ethernet differential	Ethernet Phy to connector	Differential impedance = 100 Ω ± 15%

Additional considerations for the stackup include

- Must utilize high-volume, low-cost, PCB technology
- Routing density
- Aspect ratio less than 10:1
- Drill size set at 10 mil
- Common core construction
- Proper signal referencing for all critical signals

4.1 Stackup Proposal

Figure 2 shows a viable stackup for achieving the target impedances noted in Table 3. The target card thickness used is 62 mils (±7 mils). All signal routing is done on the inner two signal layers, or on the top and bottom signal layers. No signal routing is performed on the power and ground layers.



Lay #	Thick (in)	Picture	Type Dk Df	Description	Drill Picture
	0.0007/0.0007		3.20	Soldermask	
1	0.0022		F	1/2oz w/plating	1
	0.0040	1-2113	4.39 0.018	fill	
2	0.0013		P	1oz	2
	0.0040	1-2116	4.47 0.018	core	
3	0.0006		S	1/2oz	3
	0.0038	1-2113	4.41 0.018	fill	
	0.0000			None	
	0.0280	4-7628	4.51 0.018	core	
	0.0000			None	
	0.0038	1-2113	4.41 0.018	fill	
4	0.0006		S	1/2oz	4
	0.0040	1-2116	4.47 0.018	core	
5	0.0013		P	1oz	5
	0.0040	1-2113	4.39 0.018	fill	
6	0.0022		F	1/2oz w/plating	6
	0.0007/0.0007		3.20	Soldermask	

0.0612	Total thickness (in) Over metal(with solder mask)
0.0566	After lamination thickness (in)
0.0568	Over laminate thickness (in) (with soldermask)
0.0620	Customer Requirement (in)
+/-0.0070	Customer Tolerance (in)

Figure 2. Example Six-Layer PCB Stackup (Provided by Sanmina-SCI; www.sanmina-sci.com)

Table 4. Impedance Information (Provided by Sanmina-SCI; www.sanmina-sci.com)

Layer	Type	Line Width	Center-to-Center	tpd (ps/in.)	Impedance (Ω)
1	Single-ended microstrip	5 mil	n/a	153	55.15
1	Differential microstrip	4 mil	8 mil	154	93.28
1	Differential microstrip	5 mil	12 mil	154	96.54
3	Single-ended stripline	4 mil	n/a	179	56.0
3	Differential stripline	4 mil	10 mil	181	96.38
4	Single-ended stripline	4 mil	n/a	179	56.0

Table 4. Impedance Information (Provided by Sanmina-SCI; www.sanmina-sci.com) (continued)

Layer	Type	Line Width	Center-to-Center	tpd (ps/in.)	Impedance (Ω)
4	Differential stripline	4 mil	10 mil	181	96.38
6	Single-ended microstrip	5 mil	n/a	153	55.15
6	Differential microstrip	4 mil	8 mil	154	93.28
6	Differential microstrip	5 mil	12 mil	154	96.54

5 Signal Breakout

5.1 Inside the BGA area

The key strategy used in breaking out the MPC8544E is centered on the use of inexpensive through-hole vias and two-track routing for the inner and bottom layers (see Figure 4). For all mainstream PCB fabrication shops, this approach is considered “production-level” technology and is capable of being produced in high volumes. Additionally, this approach produces a cheaper overall PCB design, avoiding the additional cost associated with blind- and buried-type approaches.

The key items of the strategy are as follows:

- 1-mm (39.3 mil) ball pitch
- Plastic substrate
- 22-mil attach pad on top layer
- 19-mil via pad
- 28-mil anti-pad
- Single-track routing on top layer (between attach pads)
- Two-track routing on inner layers and on the bottom layer
  - Using 4-mil traces and 4-mil space

Figure 3 and Figure 4 show the track routing strategy used for each of the signal layers.

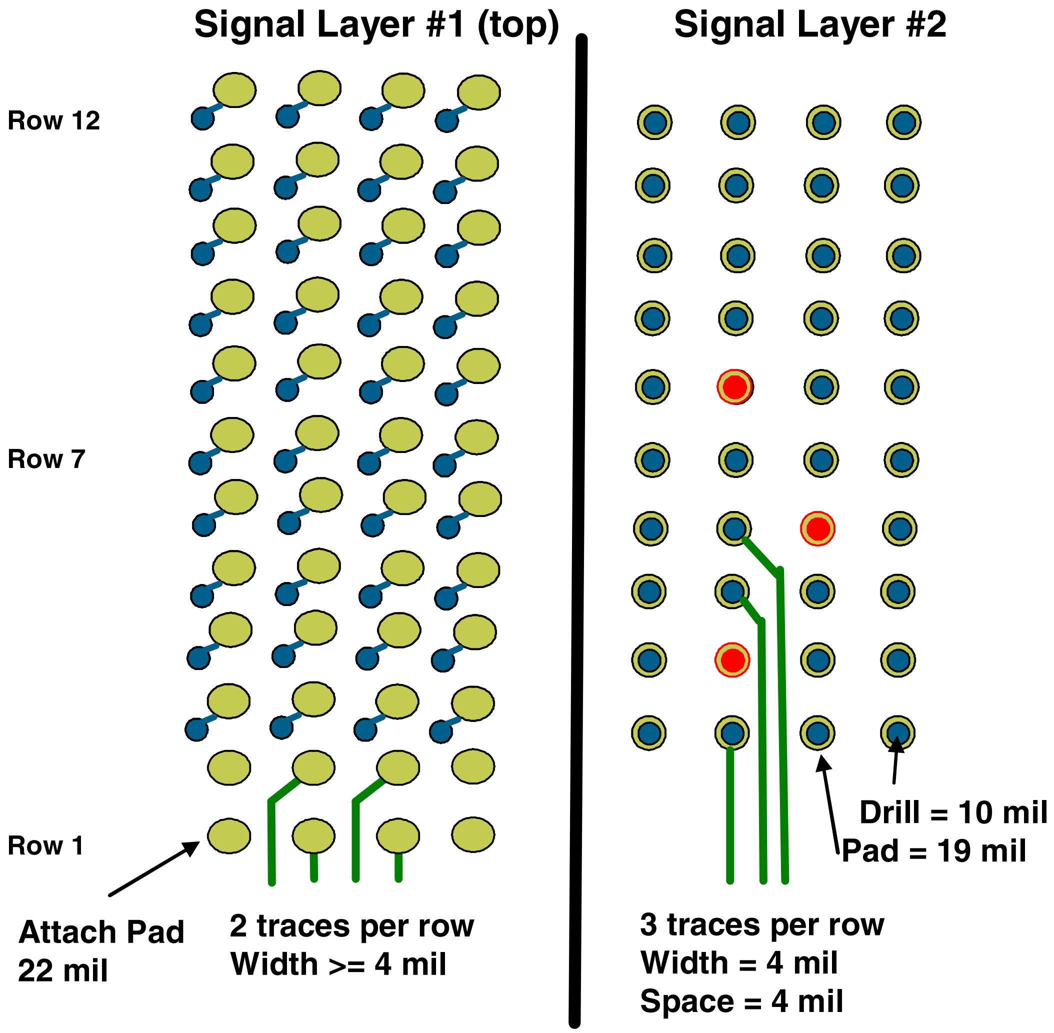


Figure 3. Signal Routing (Top and Layer #2)

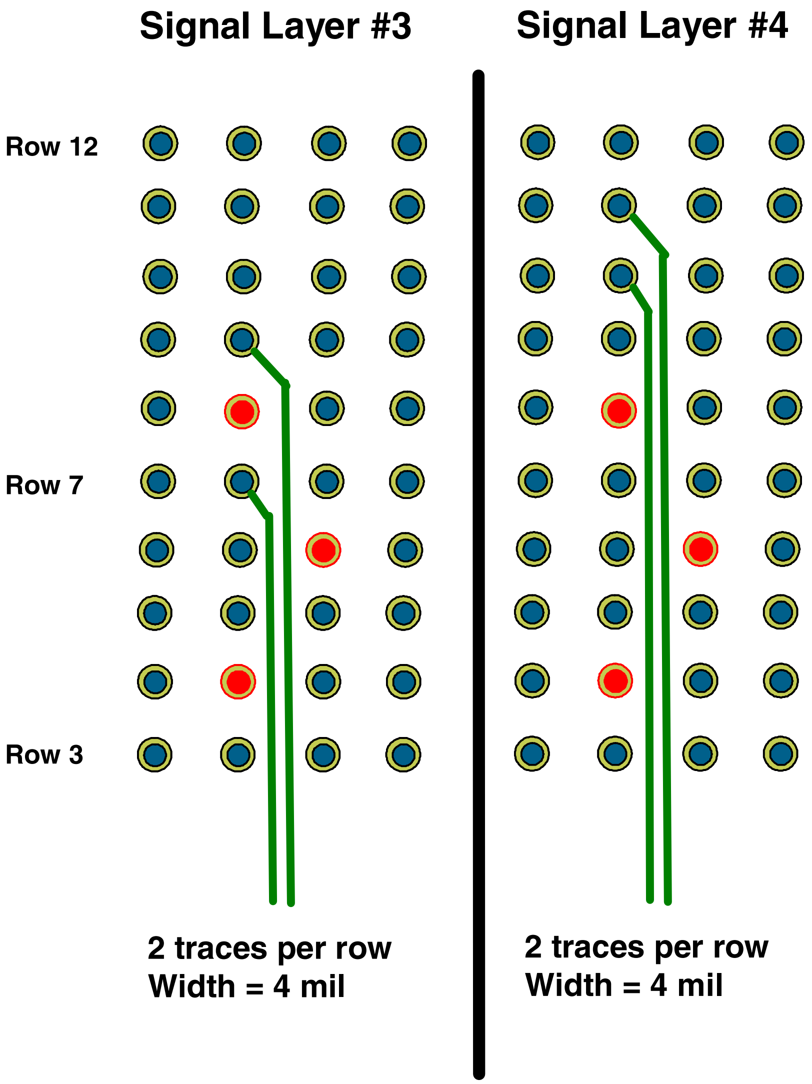


Figure 4. Signal Routing (Signal Layer 3 and Bottom)

5.2 Outside the BGA Area

Inside the BGA area, two-track routing limits the minimum trace width to 4 mils and the minimum spacing to 4 mils. Outside the BGA area, this is not the case. Since wider traces have less dielectric loss, the designer may find it useful to use larger trace widths once outside the via array. Similarly, in the cases of differential pairs, the air gaps can be adjusted as needed in order to hit desired impedance targets.

5.3 Trace Spacing Outside the BGA Area

To minimize crosstalk opportunities once outside the BGA area, the spacing between differing signal groups must be observed. This spacing, denoted as ‘S,’ is based on the dielectric thickness ‘H’ (shown in Figure 5). For the stackup shown in Figure 2, the dielectric thickness is 4.0. Using a 3:1 spacing rule, the air gap between differing signal groups should be at least 12 mil.

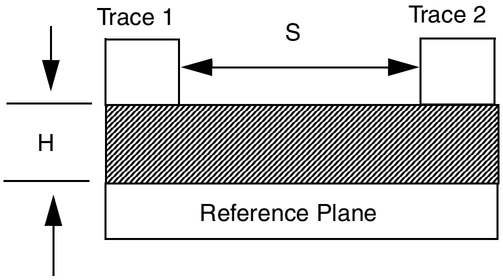


Figure 5. Trace Spacing Outside the BGA Area

6 Via Usage

For the six-layer PCB a 10-mil drill is used. A 10-mil drill has favorable cost advantages because smaller drill sizes incur additional cost. During fabrication, the drill tolerance is specified as +0/–3 mil, giving a finished hole size (FHS) of approximately 7–7.5 mil.

Using a 10-mil drill, an aspect ratio of ~ 6:1 is realized. This aspect ratio is based on an 0.062-inch board thickness and is well within the high-volume production capabilities of all mainstream PCB vendors. Figure 6 depicts the via model used for the six-layer PCB.

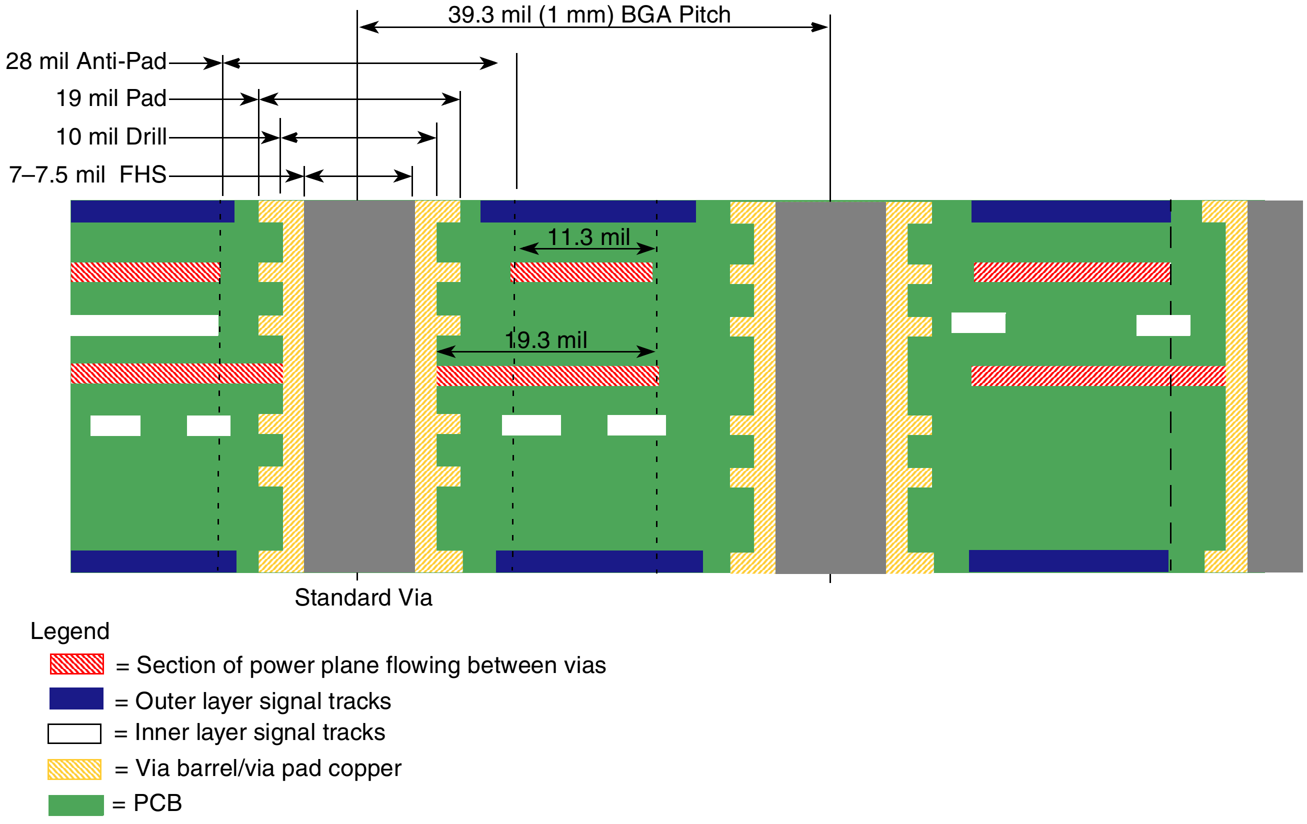


Figure 6. Cross Section of PCB

7 Power and Ground Strategy

The MPC8544E requires several power supplies for each subsystem (DDR, Ethernet, SerDes, and so forth) as well as the core itself. The total number of supplies a system needs depends on the interfaces, the interface voltages required to connect with external peripherals, and the number of those voltages that are common and sharable.

Consult the *MPC8544E PowerQUICC™ III Integrated Processor Hardware Specifications* for accurate voltage and current requirements. For convenience, Table 5 provides a snapshot of the MPC8544E power requirements at the date of this application note. The table also reflects the unique power splits constructed in the six-layer PCB example (refer to the Power Rails column). In short, a total of six unique power rails are used.

Table 5. MPC8544E Power Requirements [1]

Power Rails	Symbol	Typical Voltage	Tolerance	P_{MAX}
Core power	V_{DD_CORE} AV_{DD_CORE} AV_{DD_PLAT} AV_{DD_PCI} AV_{DD_LBIU} AV_{DD_SRDS} AV_{DD_SRDS2}	1.0 V	±50 mV	7.8 W
SerDes	SV_{DD} XV_{DD}	1.0 V	±50 mV	0.71W
DDR2 bus	GV_{DD}	1.8 V	±90 mV	2.5 W
Ethernet	LV_{DD} TV_{DD}	2.5 V	±125 mV	0.24 W
Local bus	BV_{DD}	3.3 V	±125 mV	0.33 W
Misc/PCI	OV_{DD}	3.3 V	±125 mV	0.33 W

[1] These figures are subject to change without notice. Consult the latest version of the *MPC8544E PowerQUICC™ III Integrated Processor Hardware Specifications.*

Note that Table 5 lists the power requirements for the MPC8544E only; it does not include requirements for external devices, memory, and so forth. At the very least, additional power is needed to drive connected I/O pins, and the internal logic of the other devices often shared with the MPC8544E supplies.

7.1 Power Planes

The following pictures, Figure 7 through Figure 8, highlight the power strategy used for the six-layer PCB. The ground reference for the PCB is a solid ground plane at layer 2. Since it is a solid plane with no splits, the ground layer is not shown.

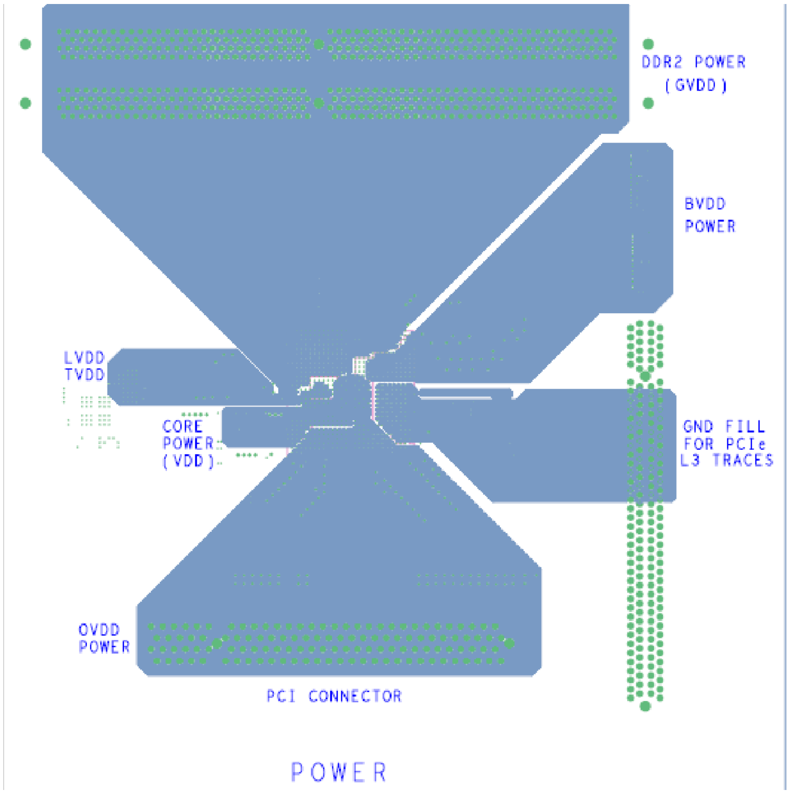


Figure 7. Power Plane (Layer 5 of 6)

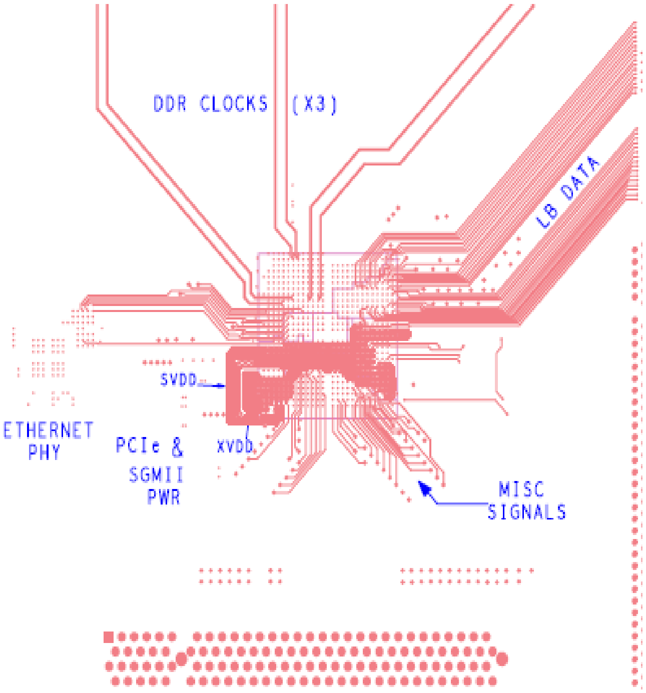


Figure 8. SV_{DD}, XV_{DD}(Layer 6 of 6—Bottom)

For sensitive supplies (such as XV_{DD} and SV_{DD}), a key requirement for power sharing is that the planes be relatively isolated. One effective strategy is to route the power planes separately and tie them together at the power source. See Figure 9.

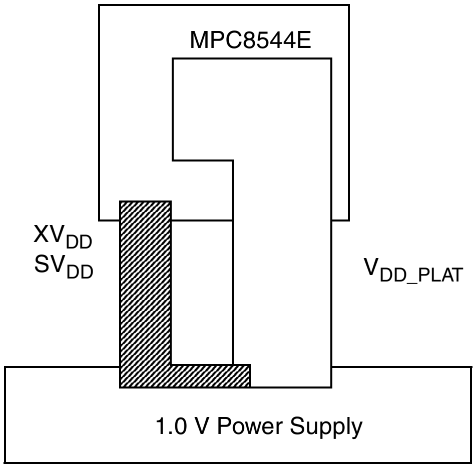


Figure 9. Common Source Split Planes

Another strategy is to use a low-pass filter to eliminate coupled noise, as long as there is sufficient current capacity in the components and connections. In either case, once separated, treat the two as independent power planes and route and bypass them separately.

7.2 Current Delivery

An important consideration in the six-layer PCB is ensuring all power rails have sufficient copper for proper current delivery. The highest power on the MPC8544E is V_{DD_CORE}. The max power requirement for V_{DD_CORE} is 7.8W.

Within a congested BGA array, the current travels down multiple 11-mil trace segments as it travels to the power pins, assuming the via stackup referenced in Figure 6 is used. The current-carrying capacity of these 11-mil traces is highly dependent on the current model chosen, either IPC2221A or the newer research performed by Johannes Adam of Flomerics Ltd. For greater detail on these two approaches see Section 10, “Current Delivery in the BGA Field.”

In short, Table 6 depicts the current capacity differences between the two approaches assuming a maximum temperature rise of 20°C. Additionally, the last column highlights the current capacity assumed for the MPC8544E six-layer PCB.

Table 6. Current Capacity of an 11-mil Trace Adam's Model vs. IPC

Location	Copper Plating (oz.)	11-mil Trace: Adam's Model (A)	11-mil Trace: IPC2221A (A)	11-mil Trace: Capacity Assumed for the MPC8544E Six-Layer PCB (A)
Outer	0.5	1.210	0.777	1.0
	1.0	1.711	1.285	1.5
	1.5	2.420	1.730	N/A
	2.0	3.422	2.130	N/A
Inner	0.5	1.149	0.390	0.75
	1.0	1.625	0.582	1.1
	1.5	2.299	0.865	N/A
	2.0	3.251	1.065	N/A

Taking the last column from Table 6 and the number of 11-mil channels achieved in the six-layer PCB, Table 7 highlights the current capacity for V_{DD_CORE}.

Table 7. Current Capacity Achieved in the Six-Layer PCB

Power Rail	Copper Weight Used (oz.)	No. of 11-mil Traces Supplying Power	Current per Trace (A)	Total Current Supplied in Six-Layer PCB (A)	Assumed Worst Case Current (A)
V_{DD_CORE}	1.0	10	1.1	11	7.8 (7.8 W/1.0 V)

7.3 PLL Filters

The MPC8544E has six PLLs which each require a filter circuit. The PLL pins are placed on the package in order to minimize noise and to allow ease during layout. An example layout for the filters are shown in Figure 10. This figure shows example layout for an AVDD filter. For the exact filter values refer to the *MPC8544E PowerQUICC™ III Integrated Processor Hardware Specifications*.

To ensure a high quality filter is realized, use the following rules:

- Place the components of the filter as close a possible to their respective pin
- Keep the traces as short as possible
- Use a 10-mil trace width or larger. An area fill is also a possibility.

- Maintain at least 20-mil clearance between the filter and other signals.

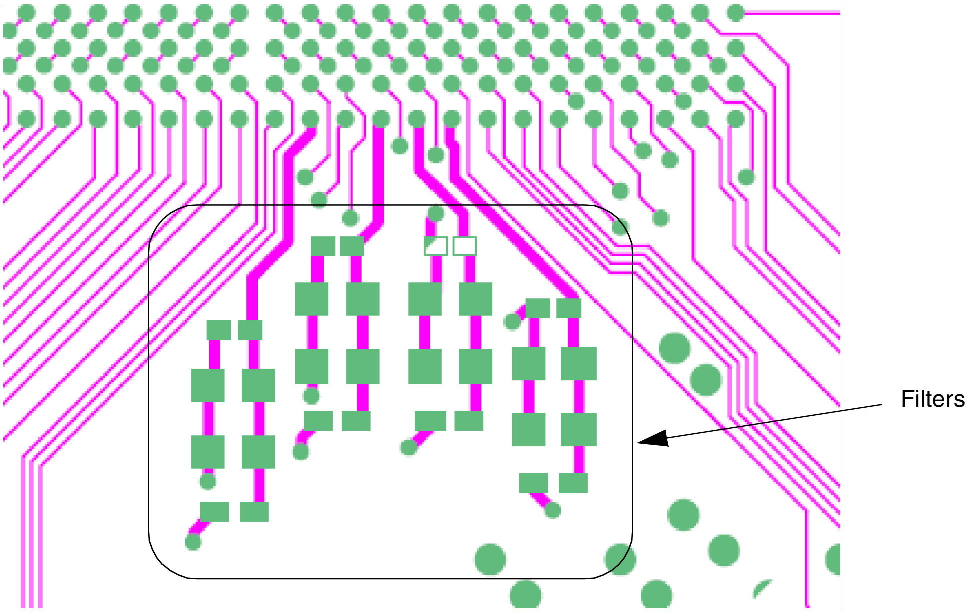


Figure 10. Example Layout for AV_{DD} Filters

7.4 Sharing Power Supplies

The six-layer design referenced in this application note assumes all processor powers referenced in Table 5 are supplied by unique power supplies. If the customer chooses, further sharing of power supplies can be achieved to reduce the number of supplies needed at the board level. Table 8 shows some acceptable options for sharing MPC8544E power rails.

Table 8. MPC8544E Power Requirements

Power Source	Symbol	Voltage	Comments
Core power + PLL filter	V_{DD_CORE} AV_{DD_CORE} AV_{DD_PCI} AV_{DD_PLAT} AV_{DD_LBIU} AV_{DD_SRDS} AV_{DD_SRDS2}	1.0 V	PLLs are sourced from RC filter circuit derived from 1.0-V rail.
SerDes	SV_{DD} XV_{DD}		Separate filtered plane but derived from the same 1.0-V power regulator.
Memory	GV_{DD}	1.8 V	Unique rail on the MPC8544E device. Could possibly be shared with another 1.8-V device on the board.
Ethernet	LV_{DD} TV_{DD}	2.5 V	2.5 V is readily usable by most PHYs; however, 3.3 V is not suitable for RGMII mode.
Local bus	BV_{DD}		2.5 V requires low-voltage flash memory and so forth
Or alternatively			

Table 8. MPC8544E Power Requirements (continued)

Power Source	Symbol	Voltage	Comments
Ethernet	LV_{DD} TV_{DD}	3.3 V	3.3 V is not suitable for RGMII mode
Local bus	BV_{DD}		
PCI/Misc	OV_{DD}		

7.5 Bypass Capacitor Placement

Because of the high current transients on the V_{DD_CORE} power pins, take care to bypass these power pins and to provide a good connection between the BGA pads and the power and ground planes. In particular, the SMD capacitors should have pads directly attached to the via ring (or even better, within it using via-in-pad methods).

Figure 11 shows the dispersion of V_{DD_CORE} power pins along with the ground pattern. This is a bottom view of the center portion of interest within the BGA array.

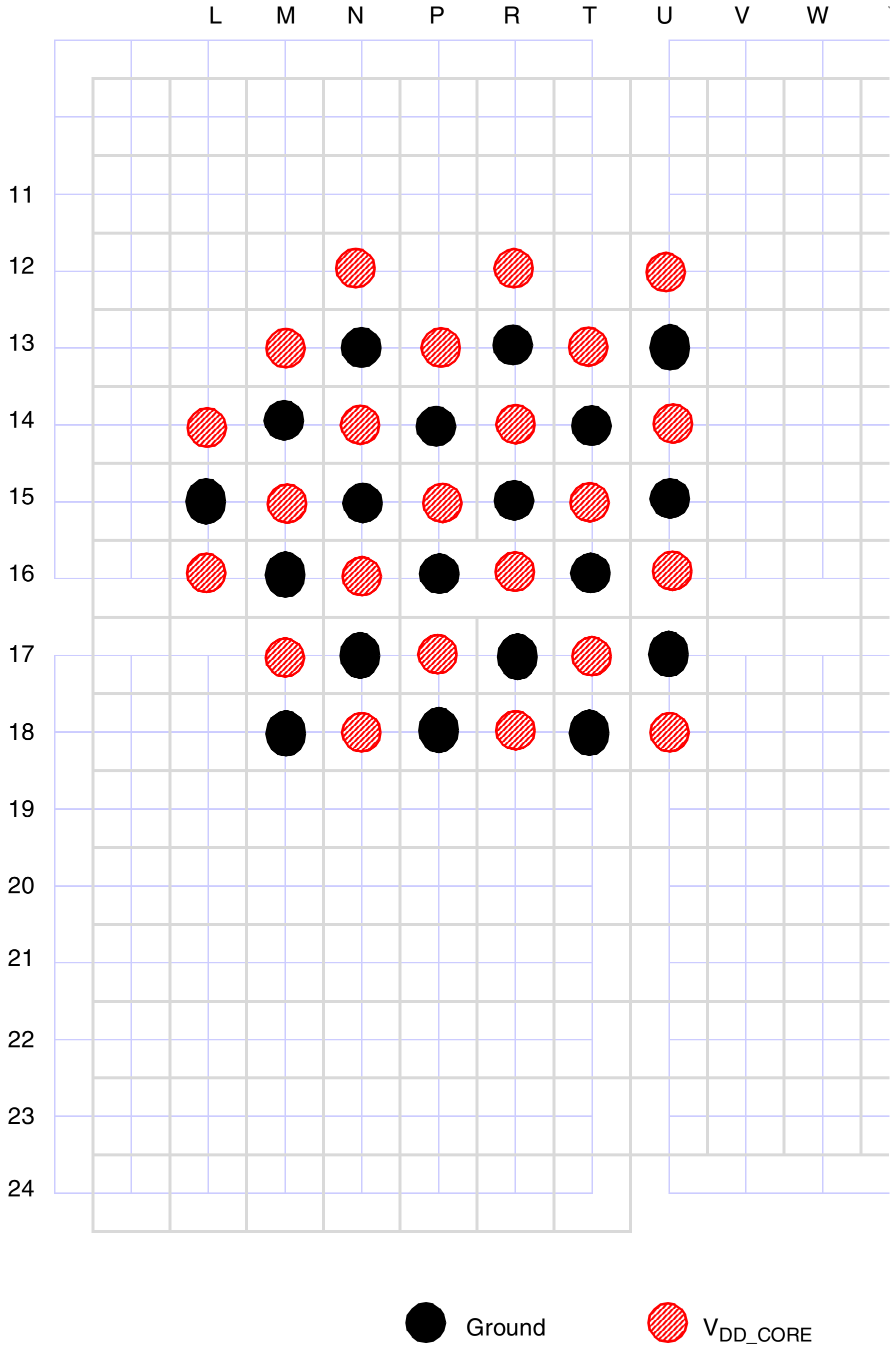


Figure 11. MPC8544E V_{DD_CORE} and Ground Pattern (Bottom View)

After the power and grounds are escaped, the SMD 0402 capacitors can be placed so that the capacitor pads attach directly to the power vias on the side. Minimize or eliminate the trace between the via and the capacitor pad. Figure 12 shows three possible attachment methods.

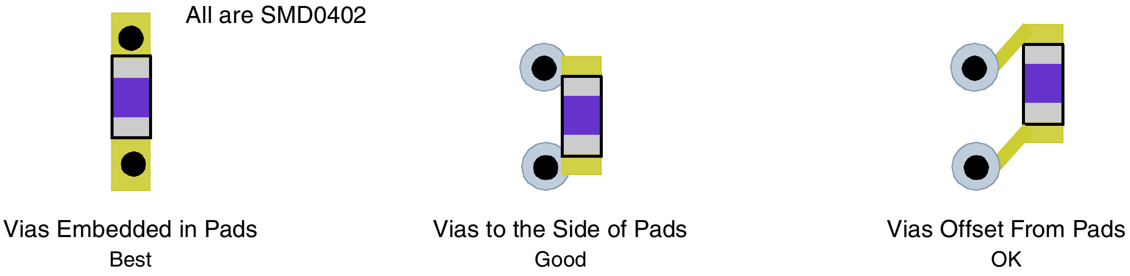


Figure 12. MPC8544E SMD Capacitor Via Placement

Figure 13 shows the relative attachment of the SMD 0402 capacitors using any of the methods shown in Figure 12. This is a view through the top of the board.

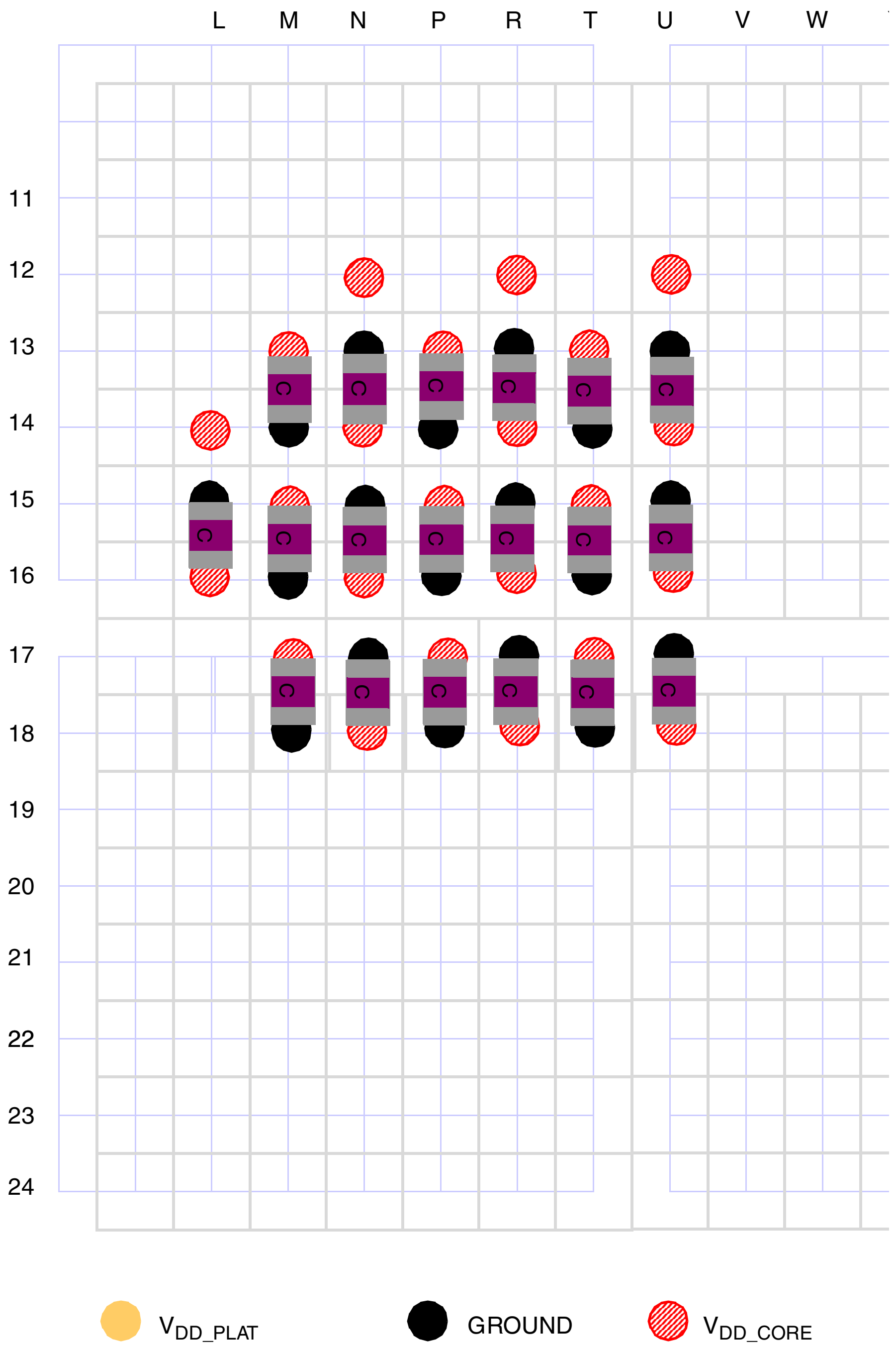


Figure 13. MPC8544E CORE and Ground SMD 0402 Capacitor Placement (Bottom View)

Other capacitors, such as those required for the other power rails, are not shown but can be attached in the same manner. If the PCB is not permitted to use via-in-pad connections, the capacitors can be shifted to attach to a pad in the area between the BGA pads. In that case, use the same relative pattern, but each capacitor shifts a little.

7.6 Bulk Capacitors

Bulk capacitors can be placed outside the periphery of the MPC8544E die, as close as reasonably possible. Systems with heatsinks and/or sockets probably need some additional spacing, but the high-frequency capacitors handle the fastest transients, allowing the bulk capacitors to be spaced a little further away. Keep them within 2 cm. Figure 14 shows the MPC8544E V_{DD_CORE} bulk capacitor placement.

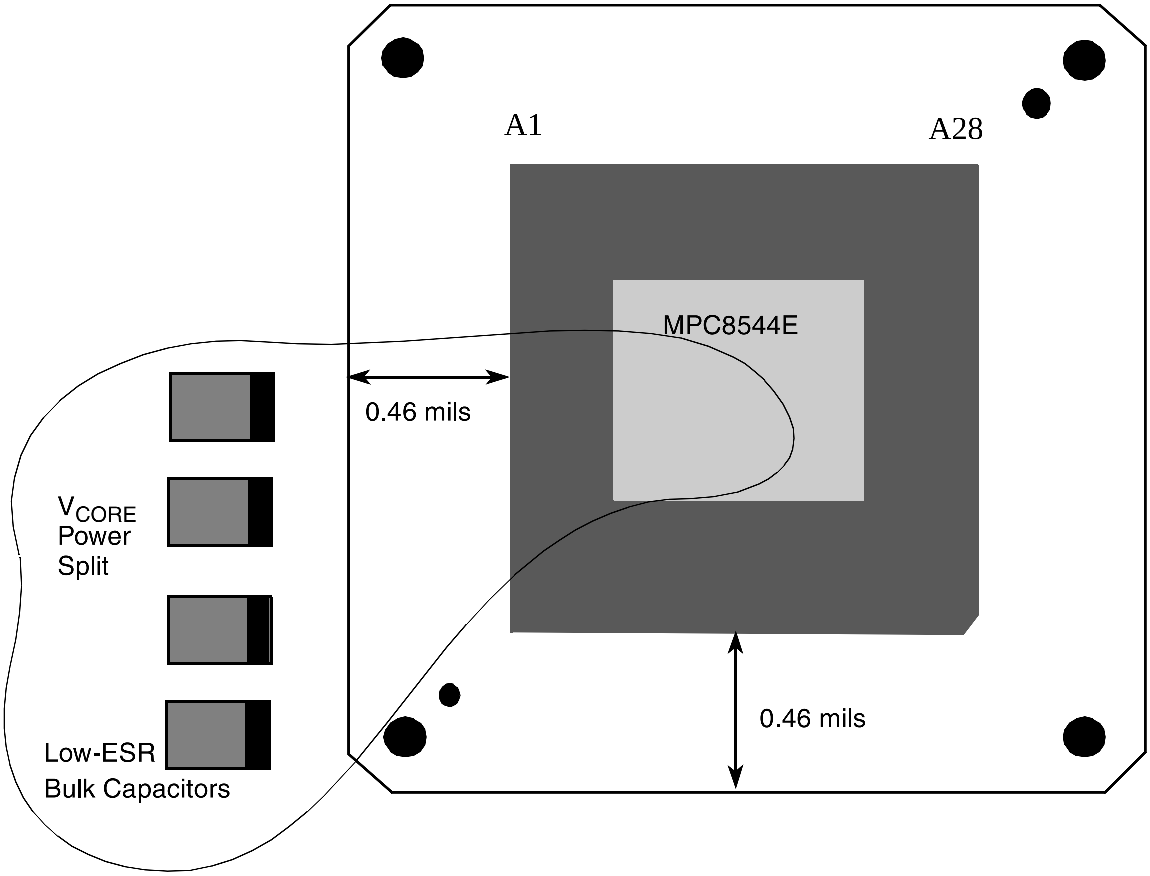


Figure 14. MPC8544E Bulk Capacitor Placement (Top View)

8 Signal Layer Gerber Plot

Figure 15 through Figure 18 show the signal layers for the six-layer PCB example. The intent is to demonstrate that the MPC8544E signals can be broken in a six-layer PCB; the figure does not include all the decoupling, nor does it show all the necessary pull-ups, AC caps, and other circuitry that would be required outside the BGA fan-out area. This level of detail is captured as part of the MPC8544E development system.

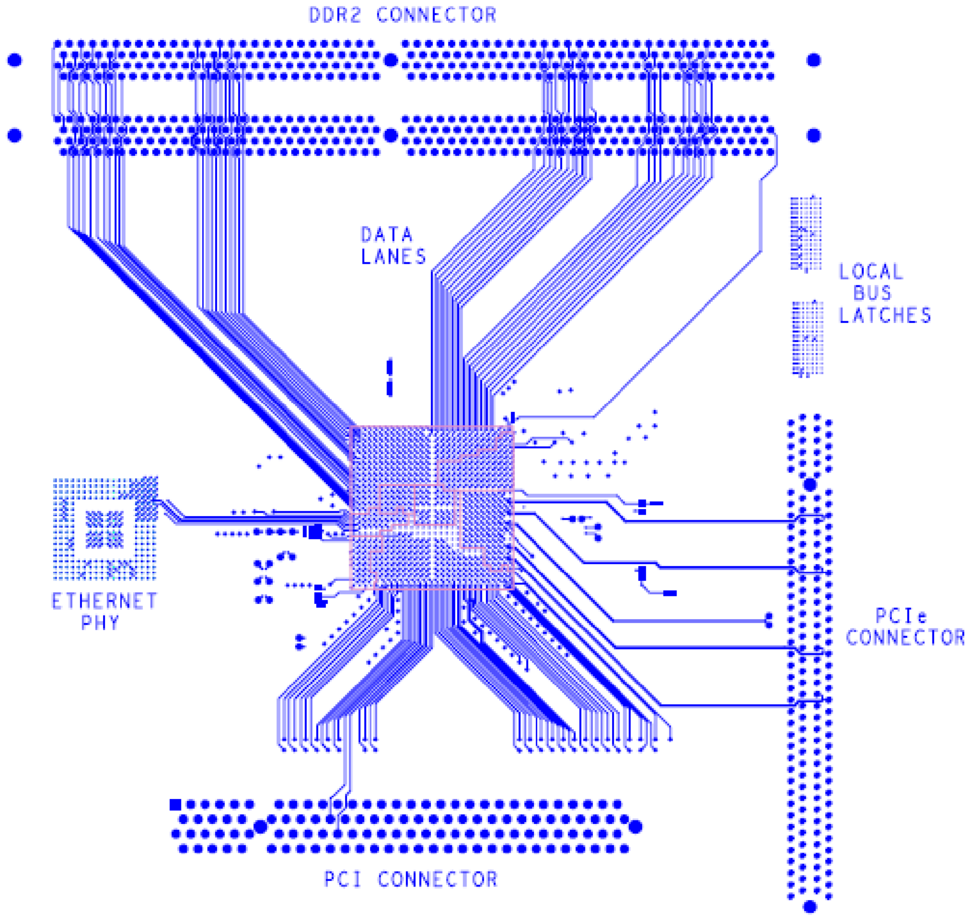


Figure 15. Top Gerber Plot (Layer 1 of 6)

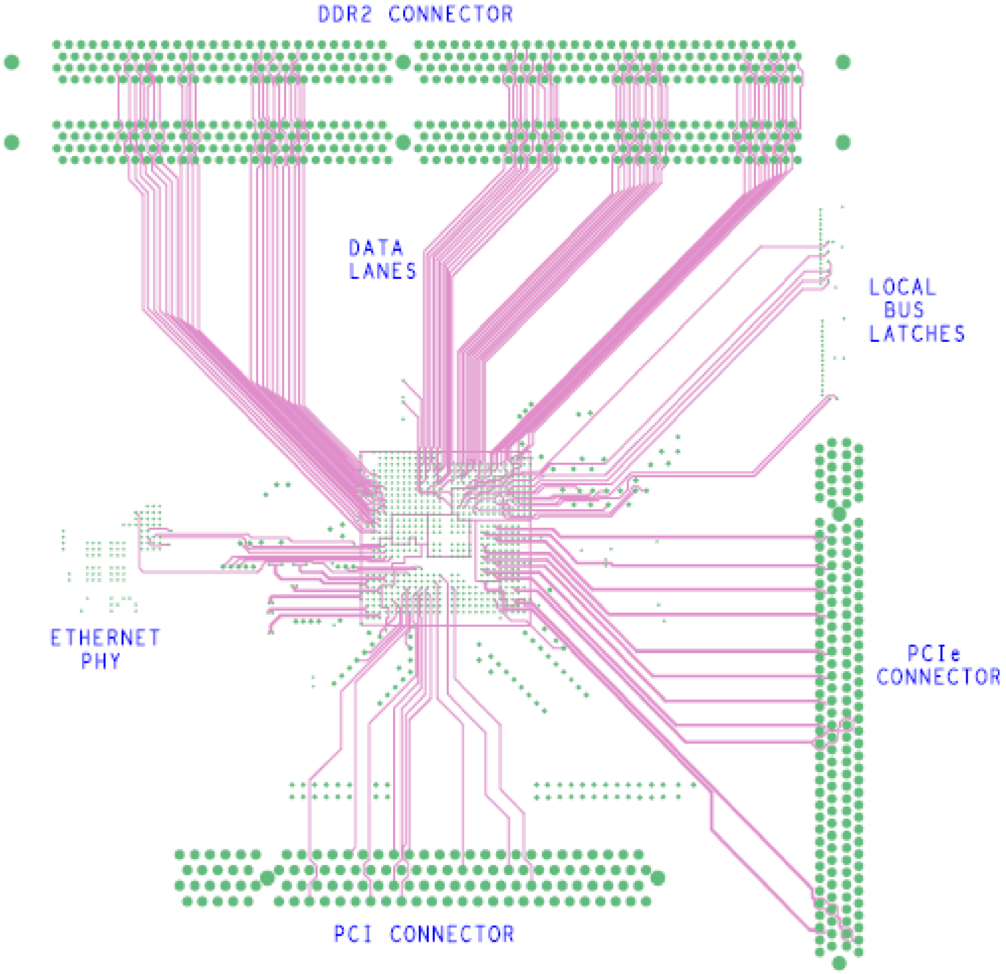


Figure 16. Signal 2 Gerber Plot (Layer 3 of 6)

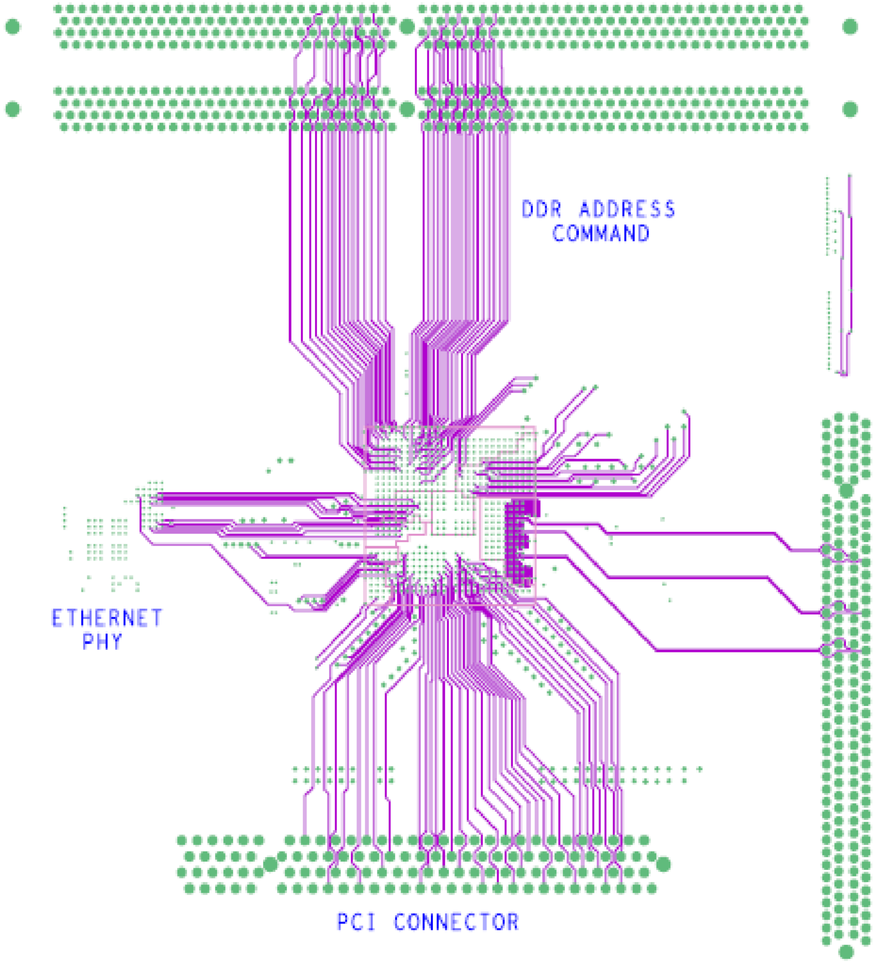


Figure 17. Signal 3 Gerber Plot (Layer 4 of 6)

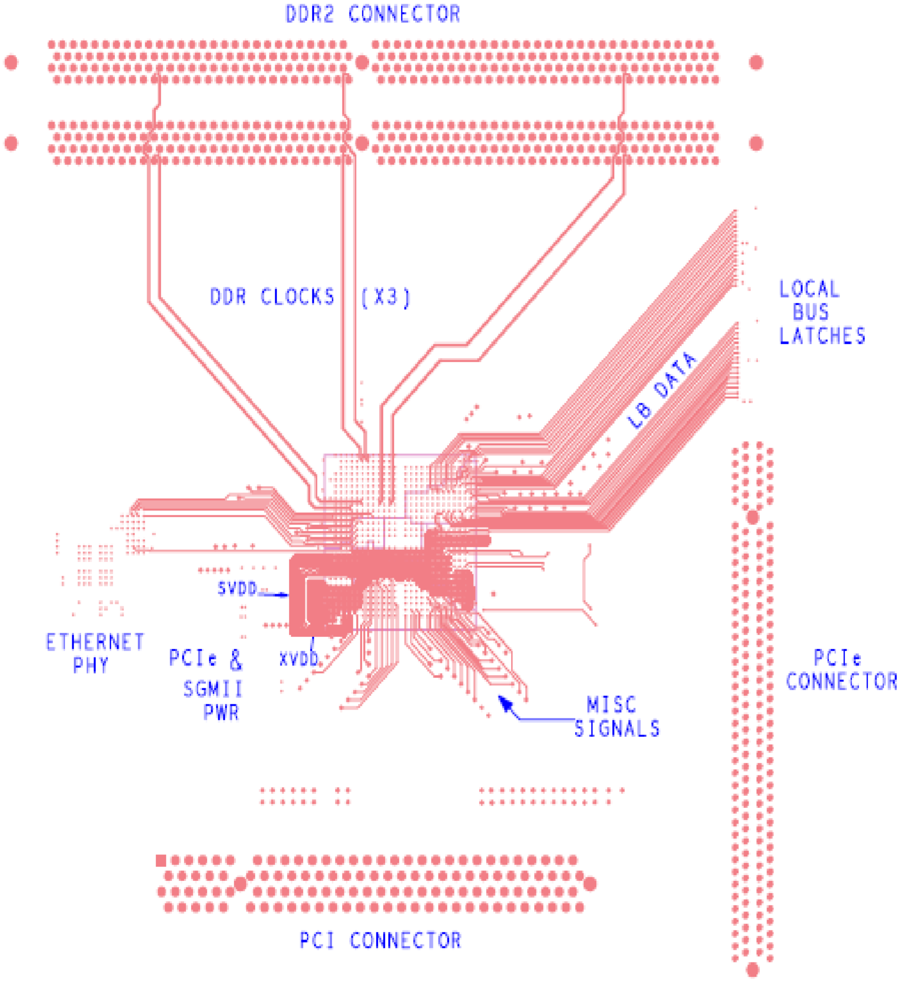


Figure 18. Bottom Gerber Plot (Layer 6 of 6)

9 Fan-Out Schematics

This section contains the fan-out schematics used to perform the six-layer PCB study. It does not include all the decoupling, nor does it show all the necessary pull-ups, AC caps, and other circuitry that would be required outside the BGA fan-out area. This level of detail is captured as part of the MPC8544E development system.

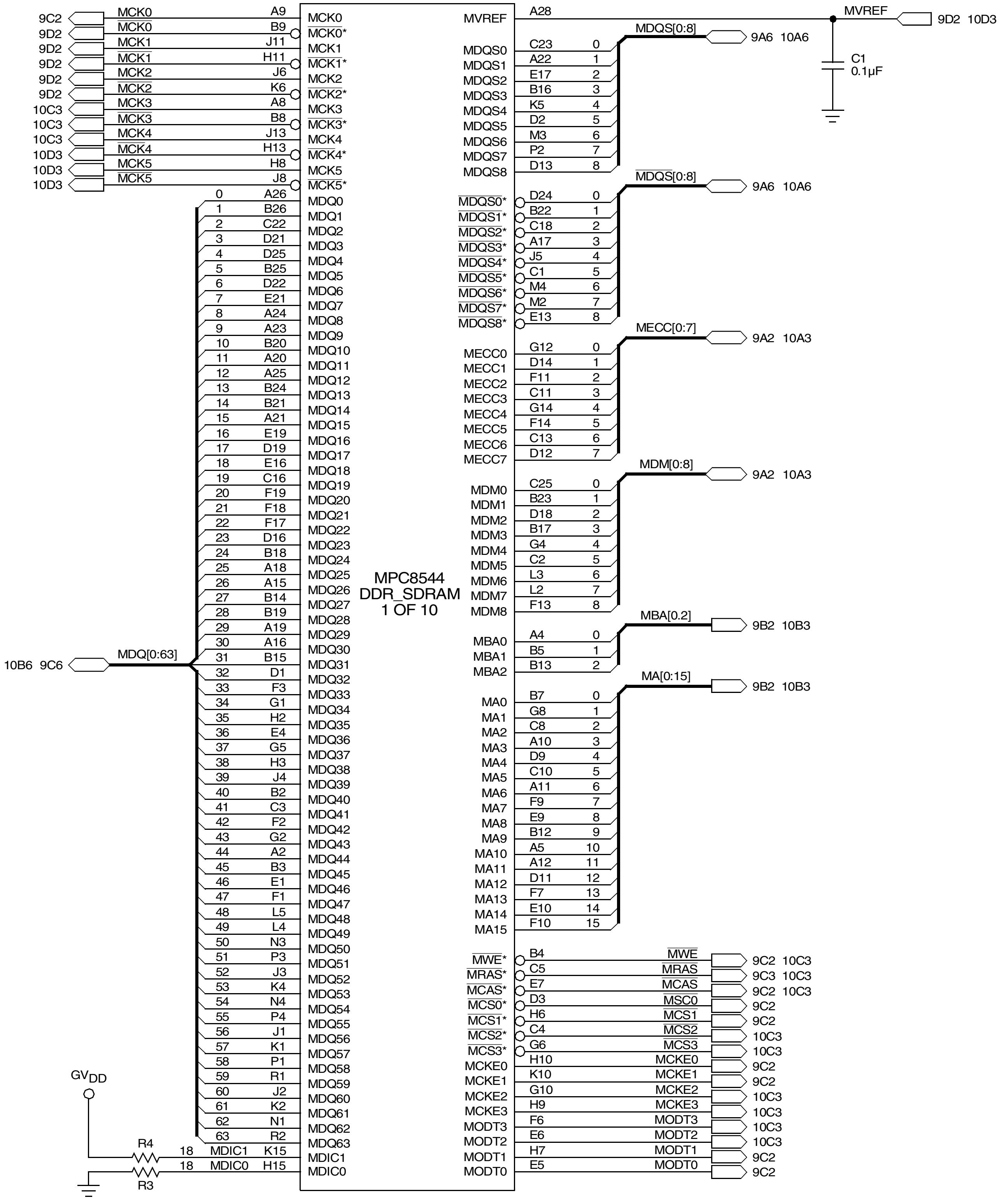


Figure 19. DDR Section

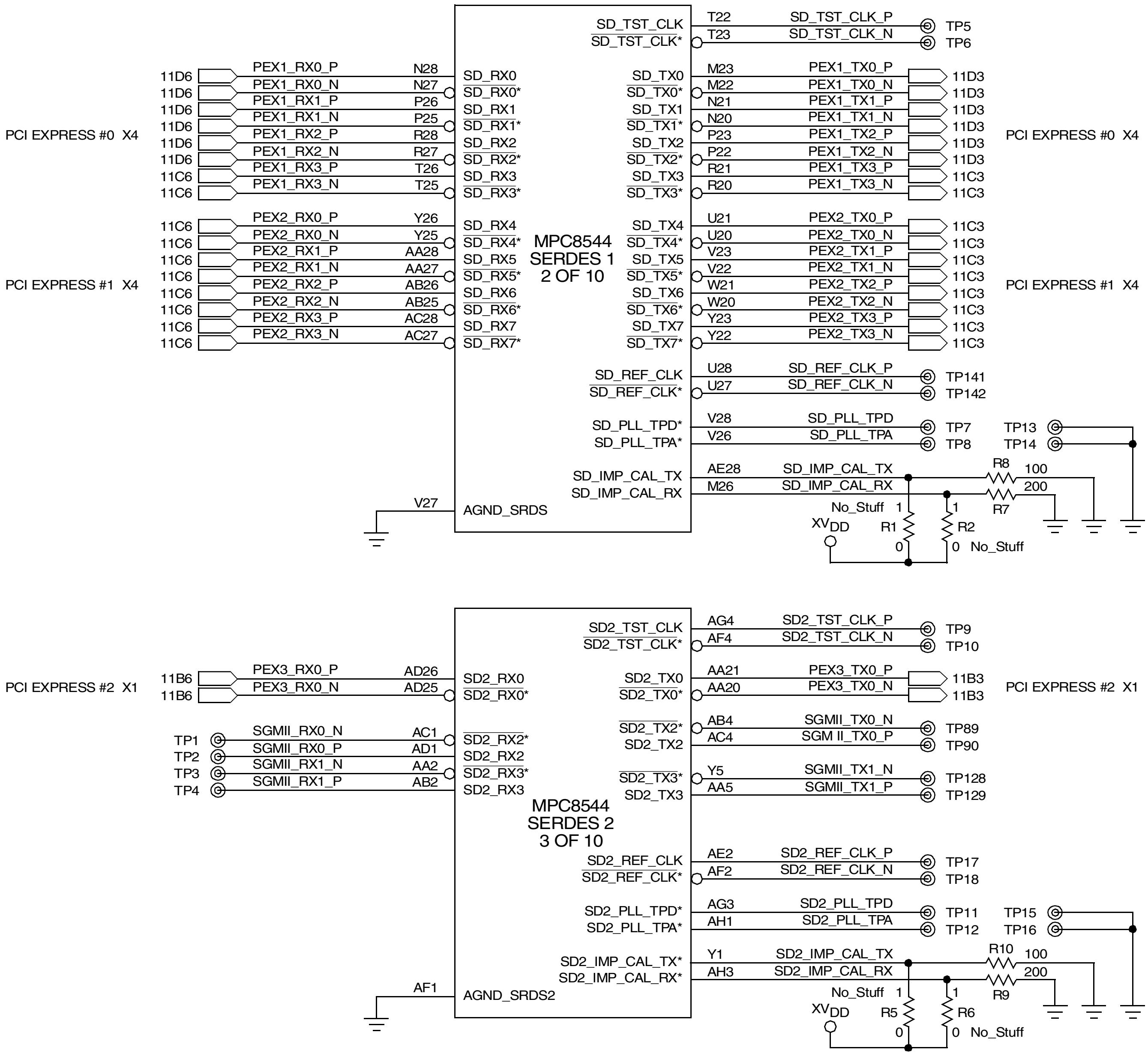


Figure 20. SerDes1 and SerDes2

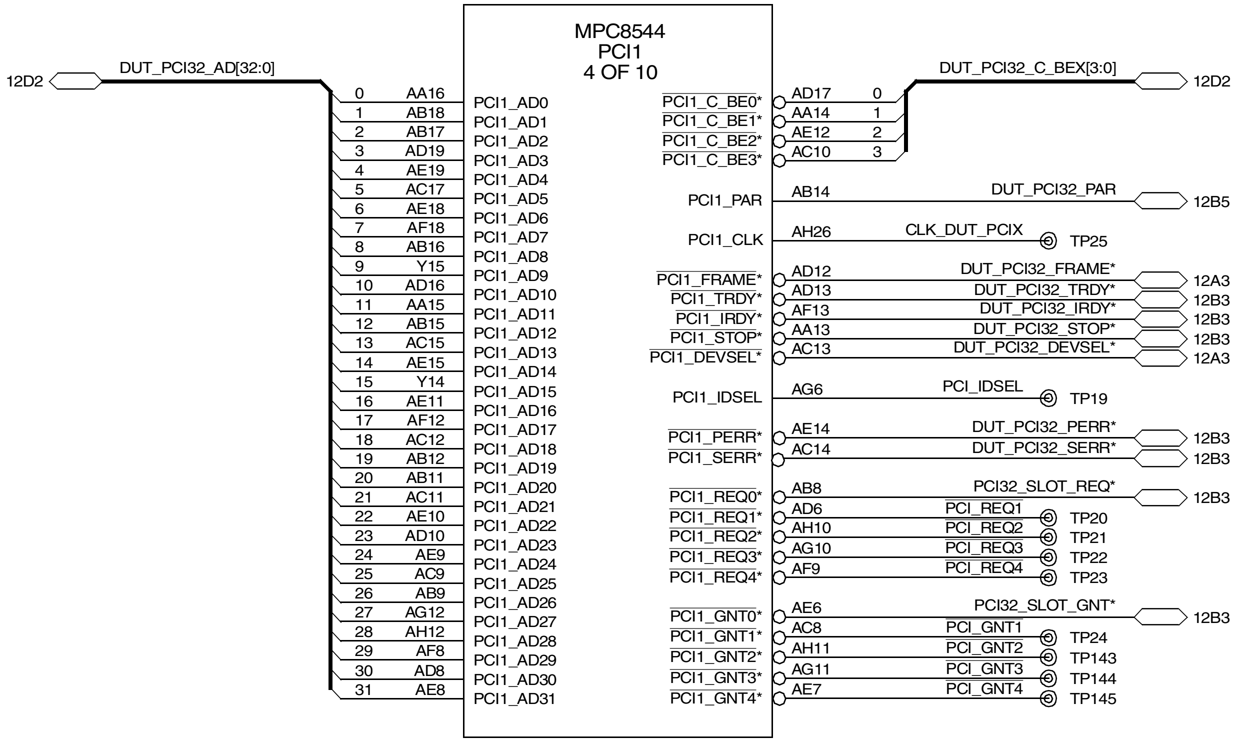


Figure 21. PCI 32-Bit

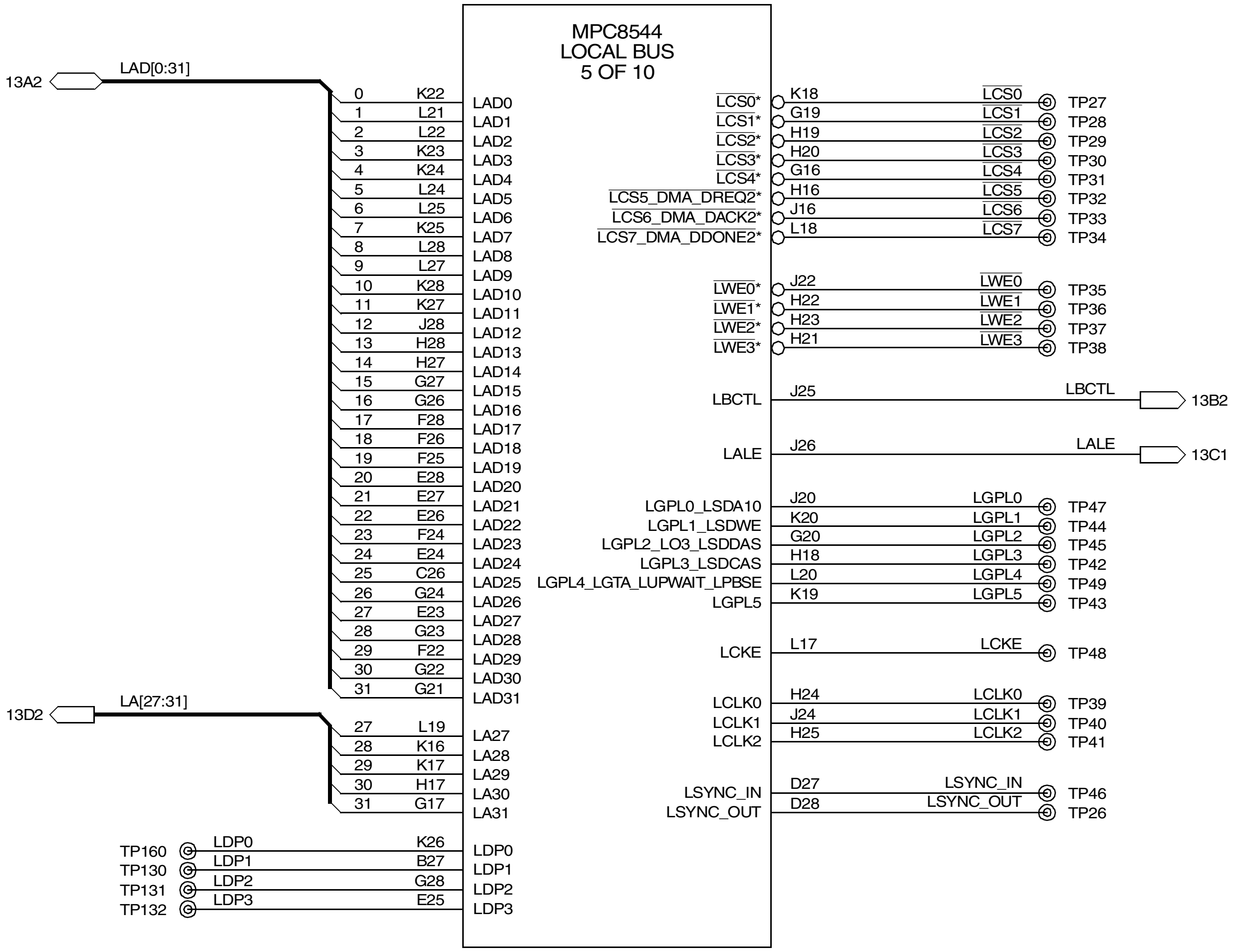


Figure 22. Local Bus

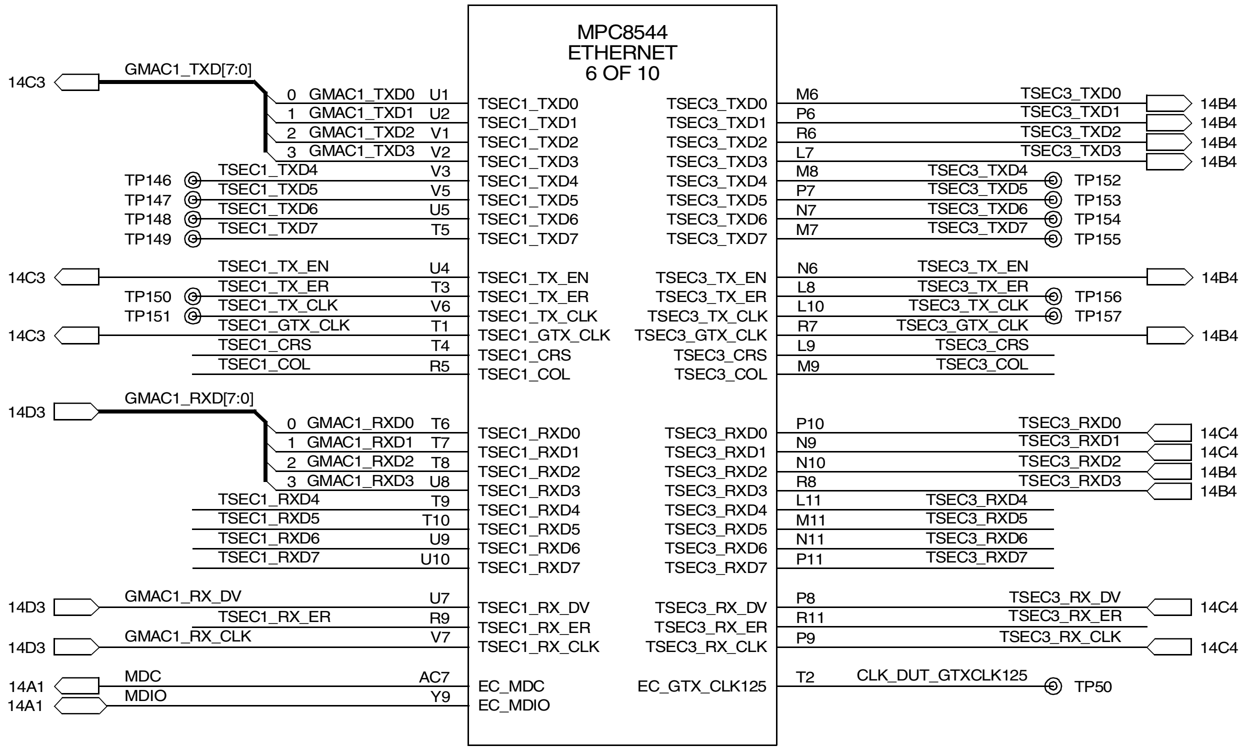


Figure 23. Gigabit Ethernet—RGMII

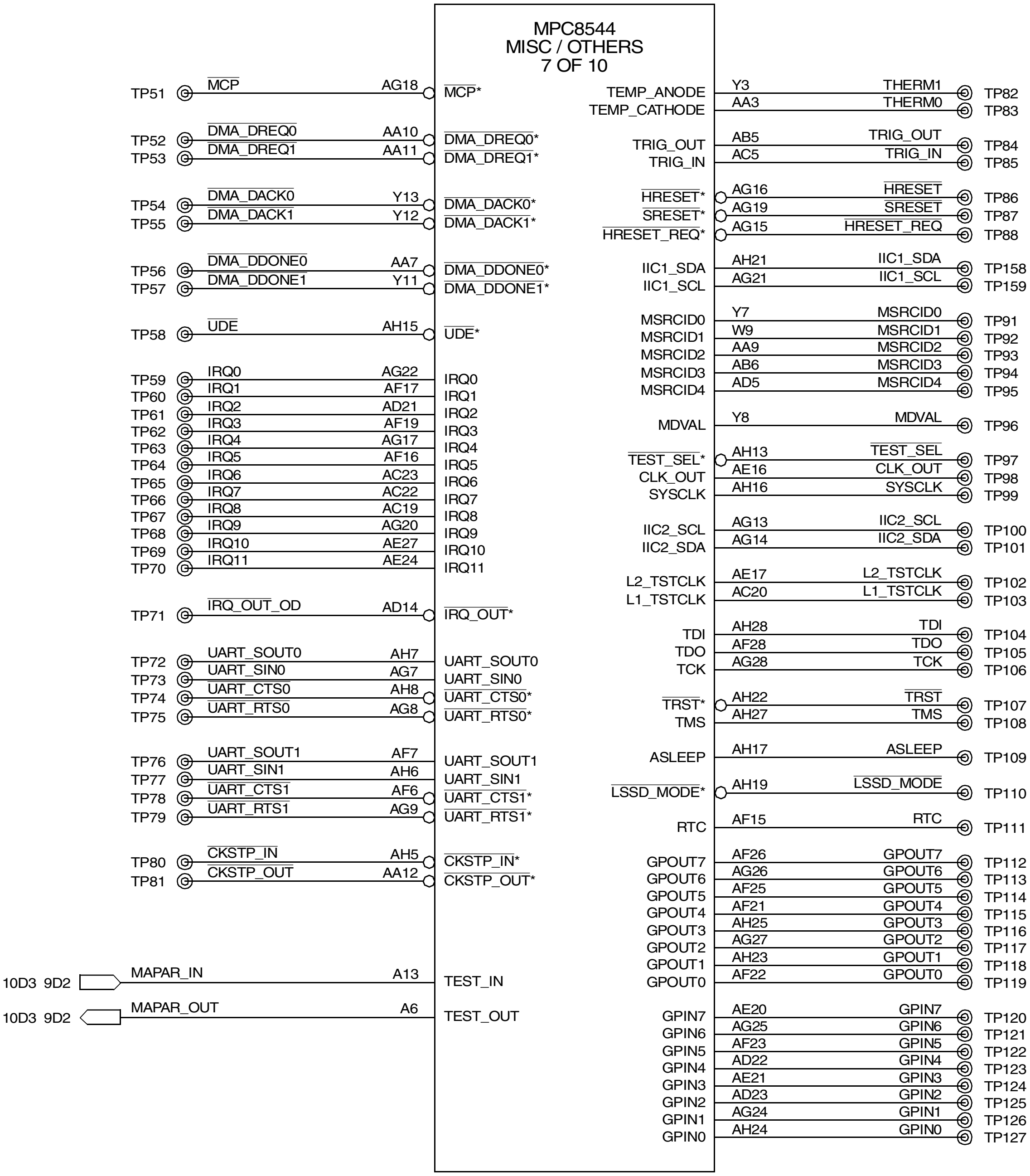


Figure 24. Miscellaneous Control

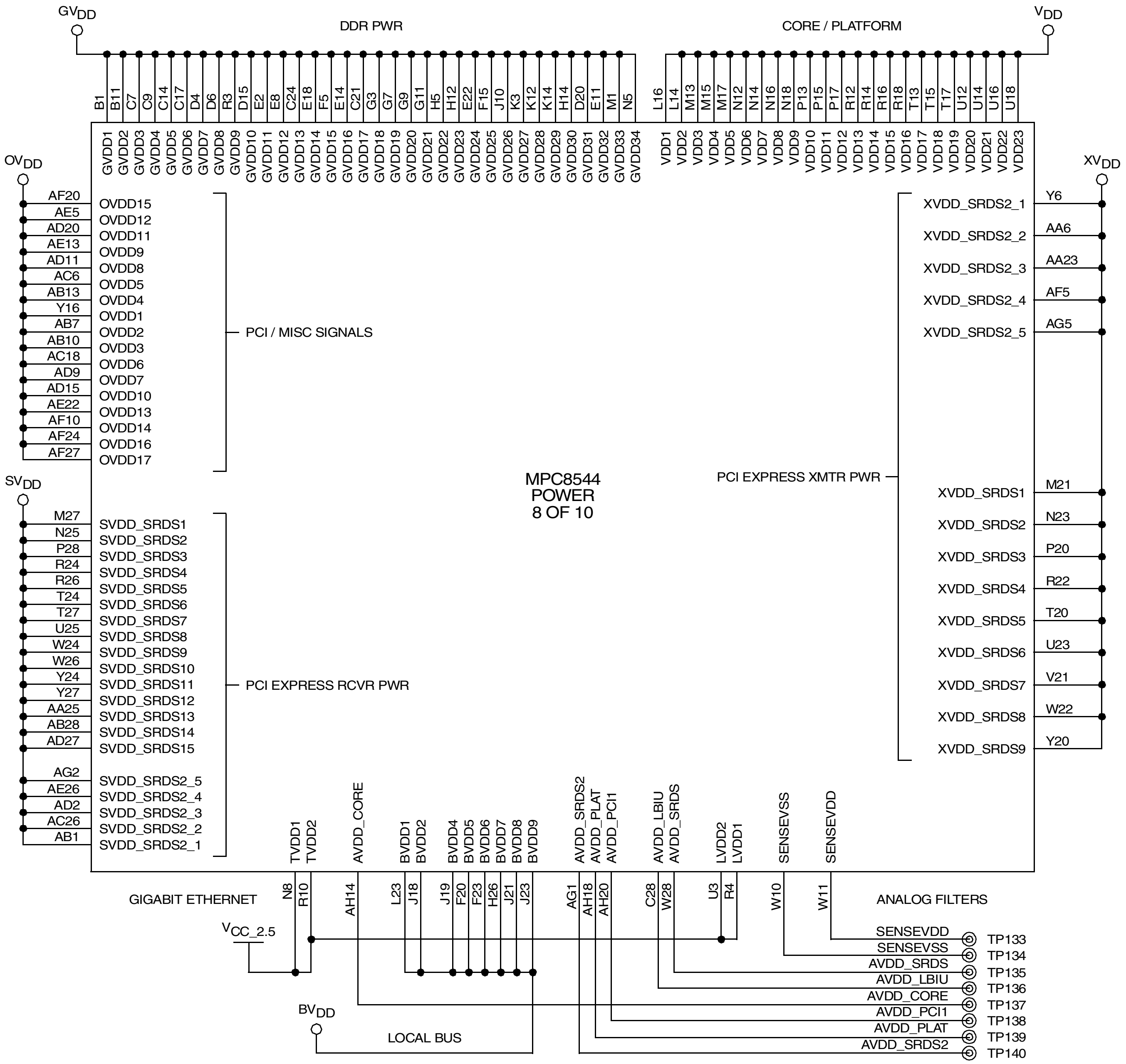


Figure 25. Power

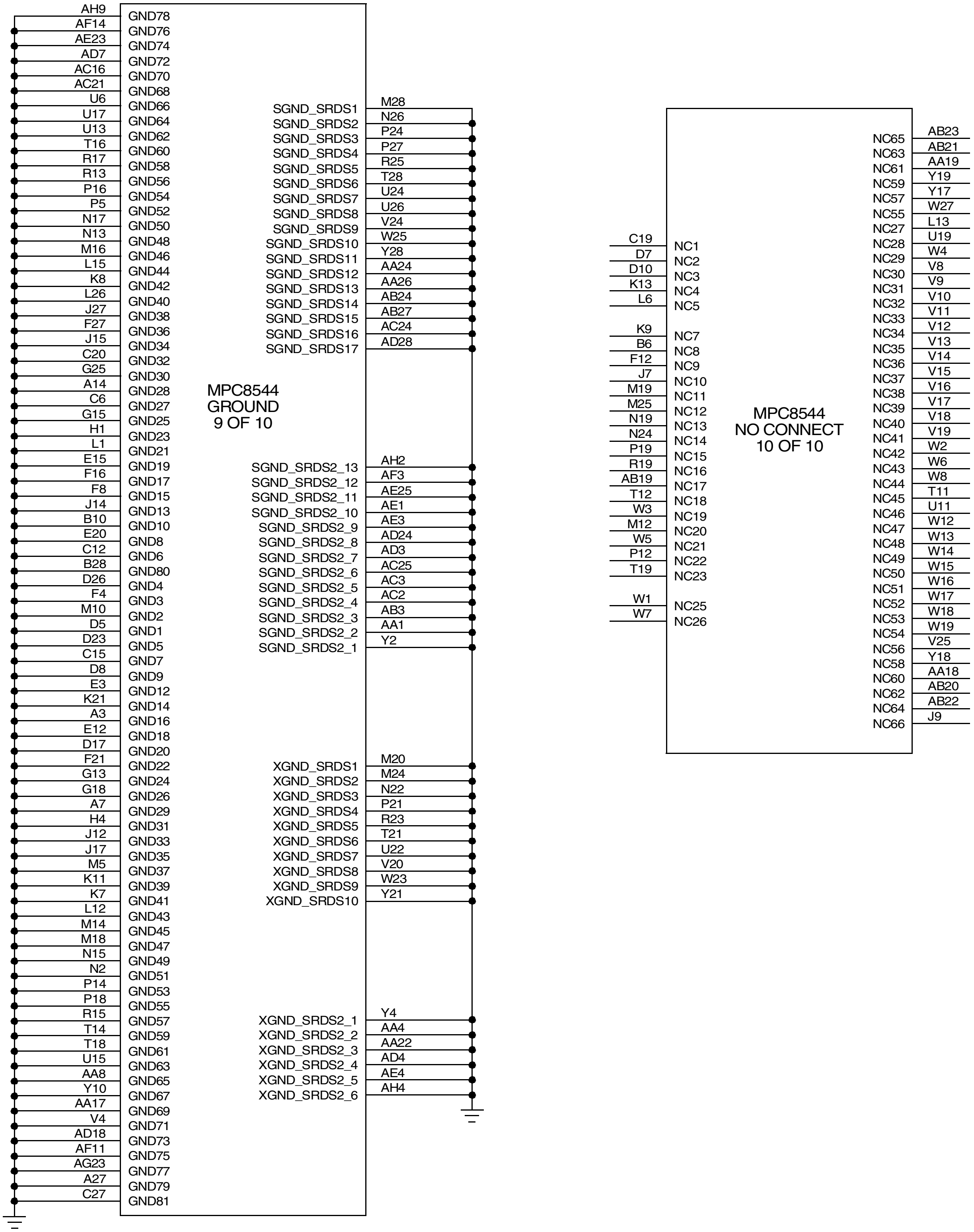


Figure 26. Ground and No-Connect

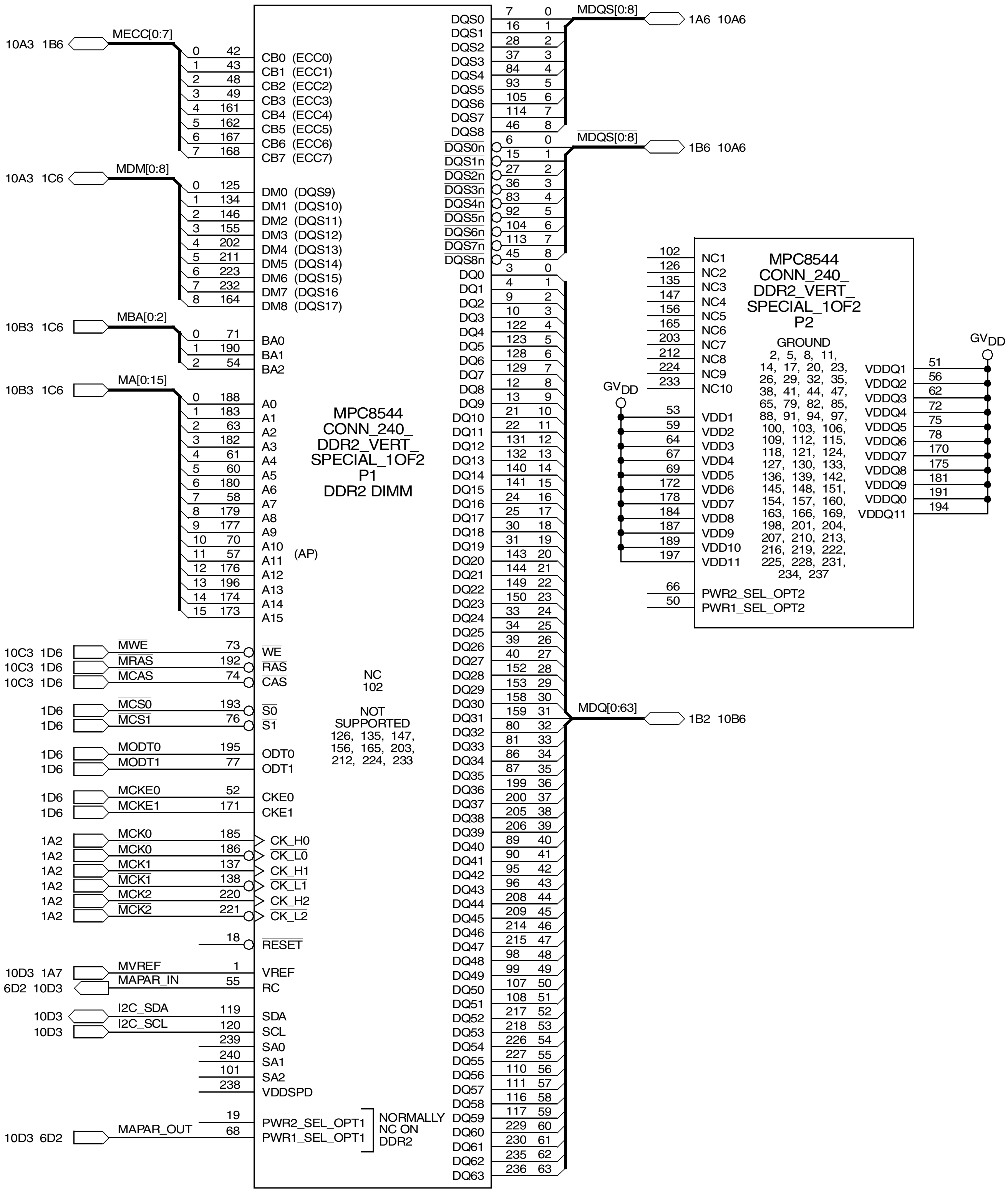


Figure 27. Memory Connector 1

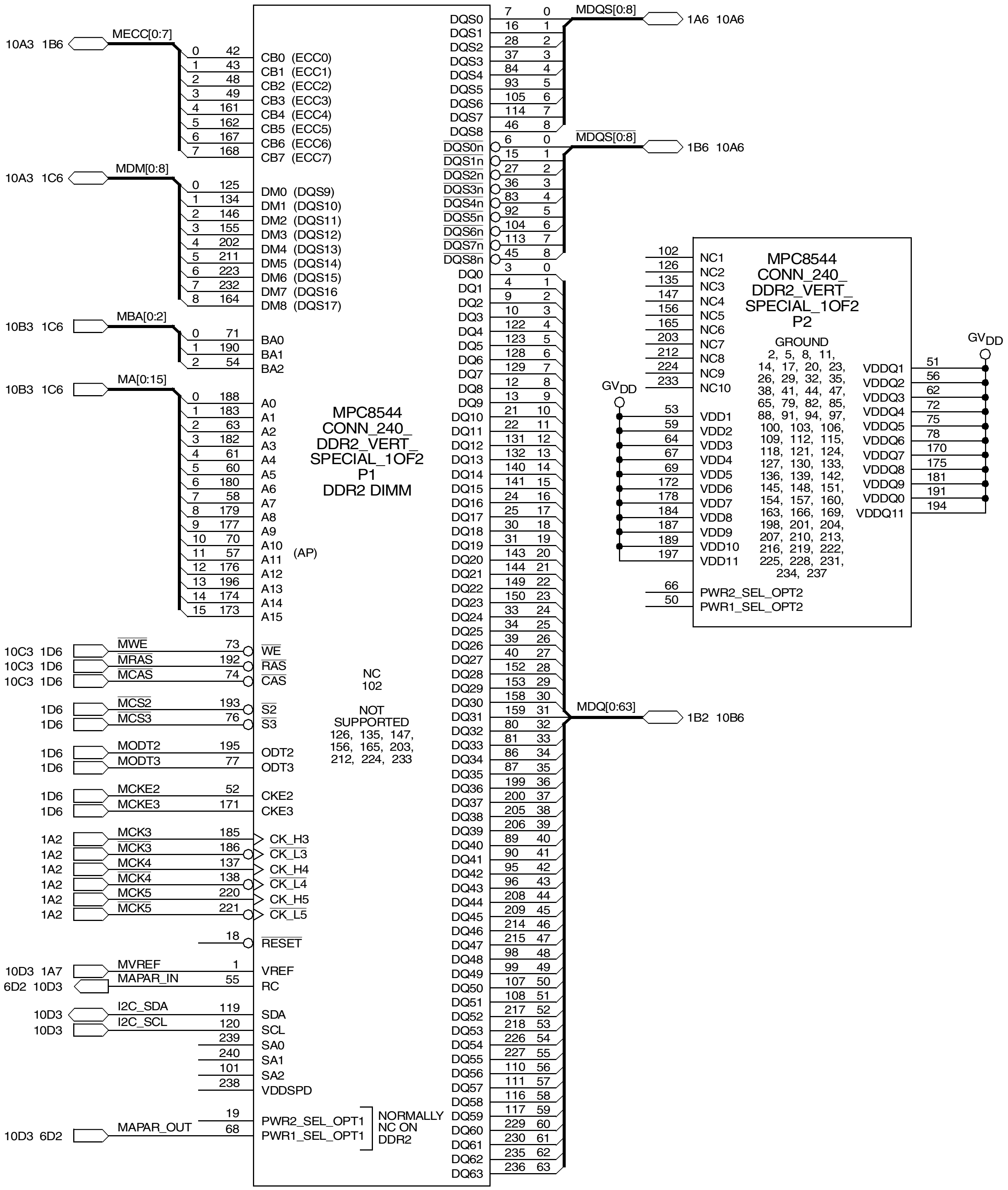


Figure 28. Memory Connector 2

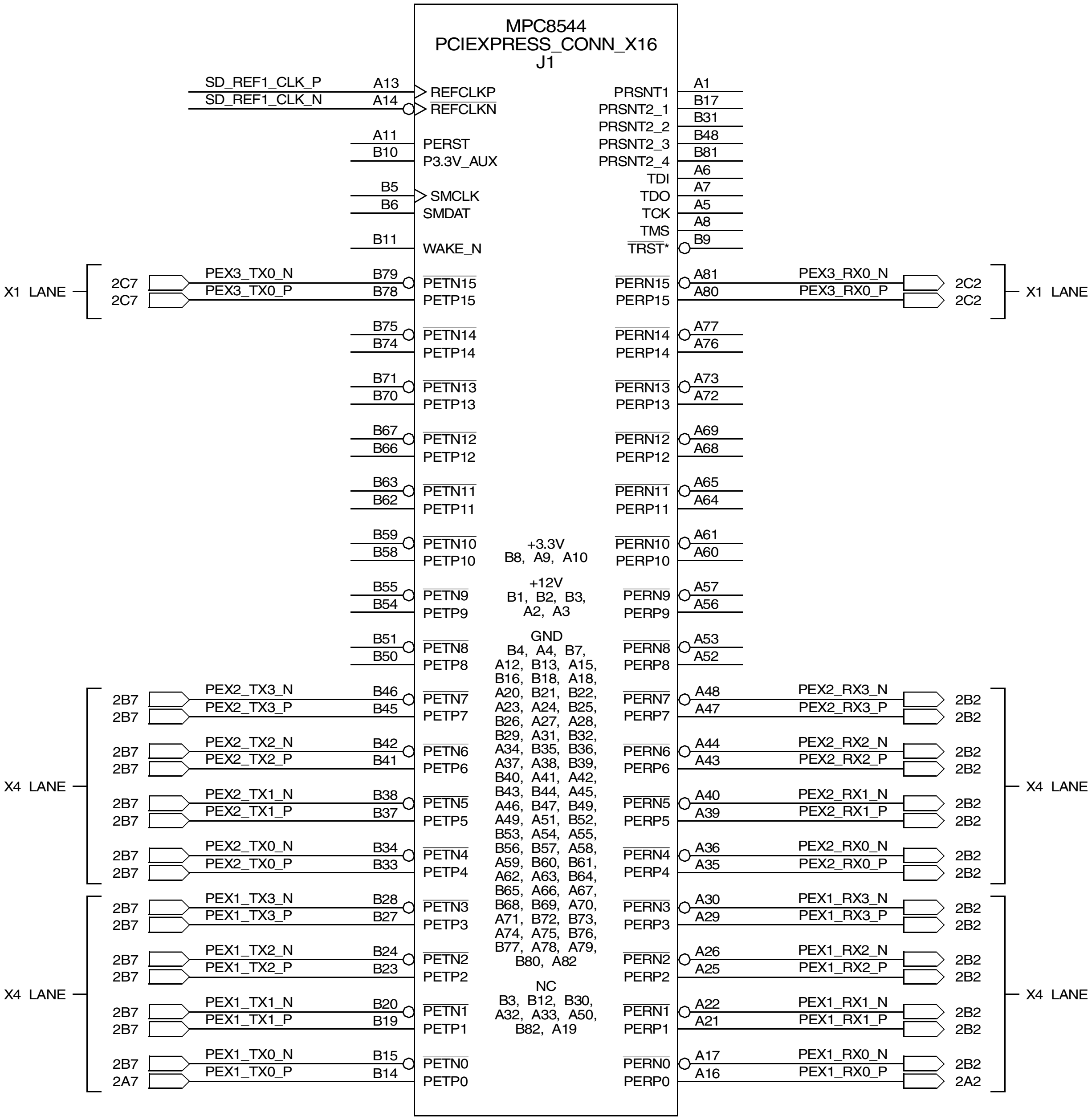


Figure 29. PCI Express Connector

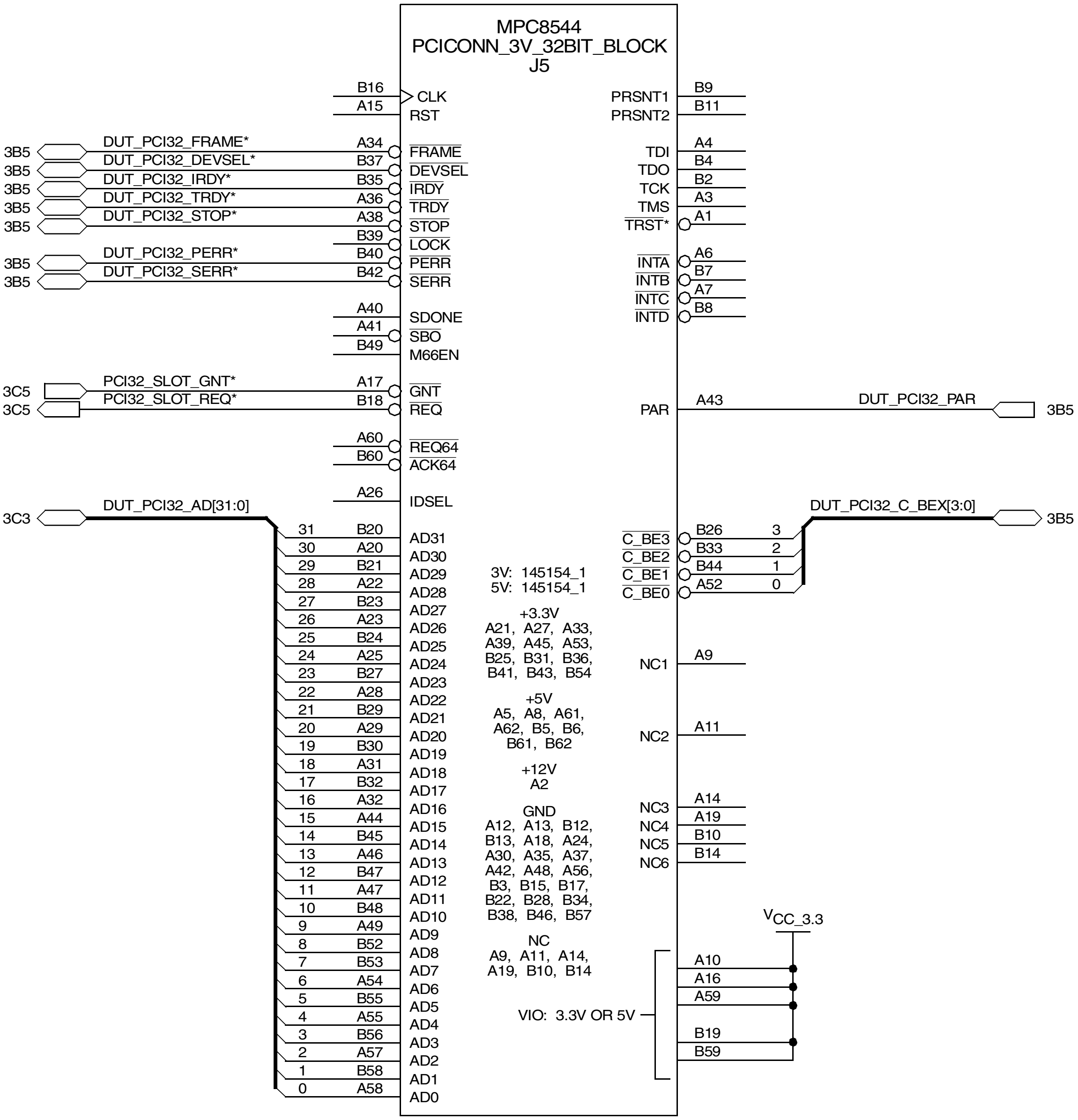


Figure 30. PCI 32-Bit Connector

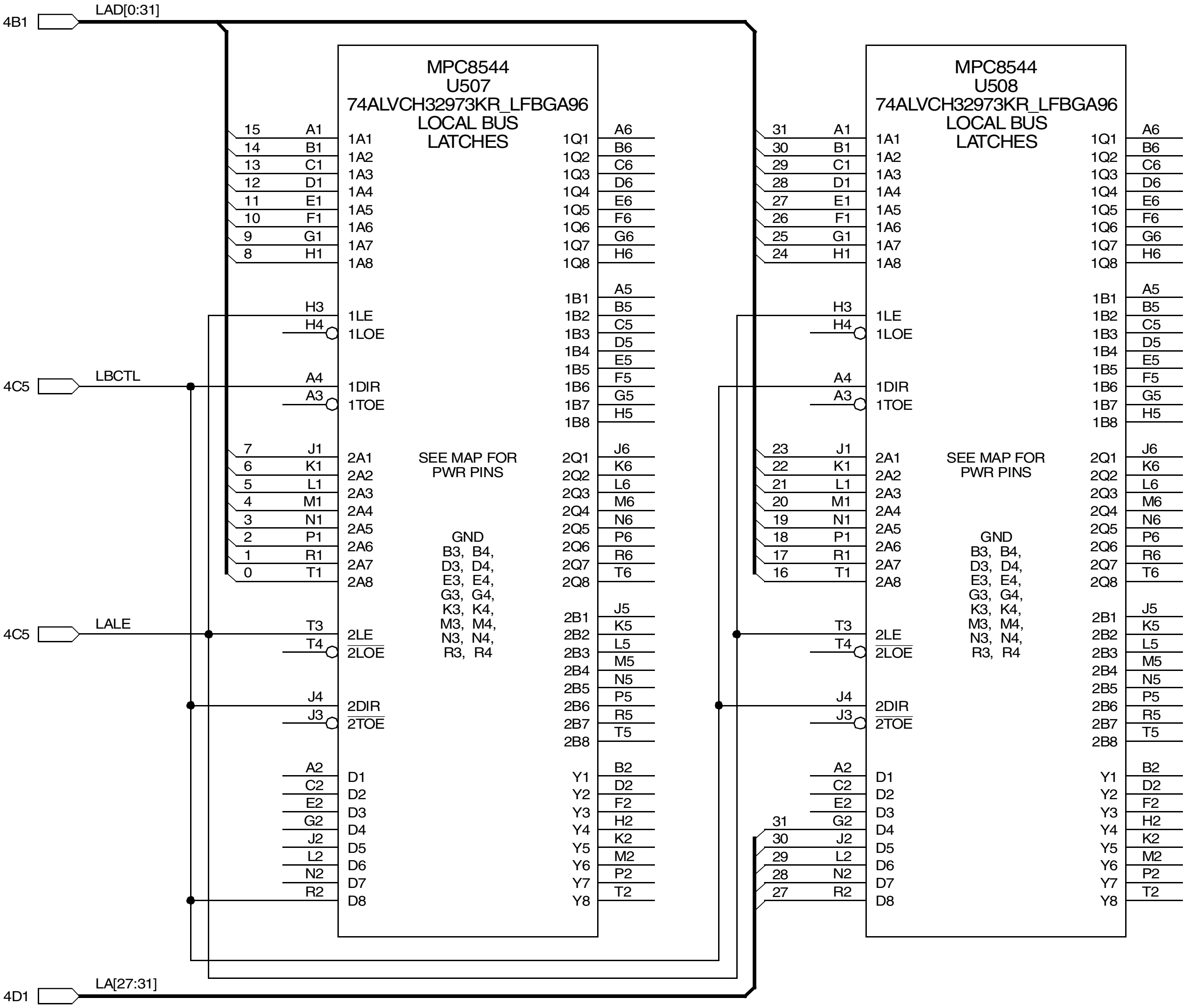


Figure 31. Local Bus Latches

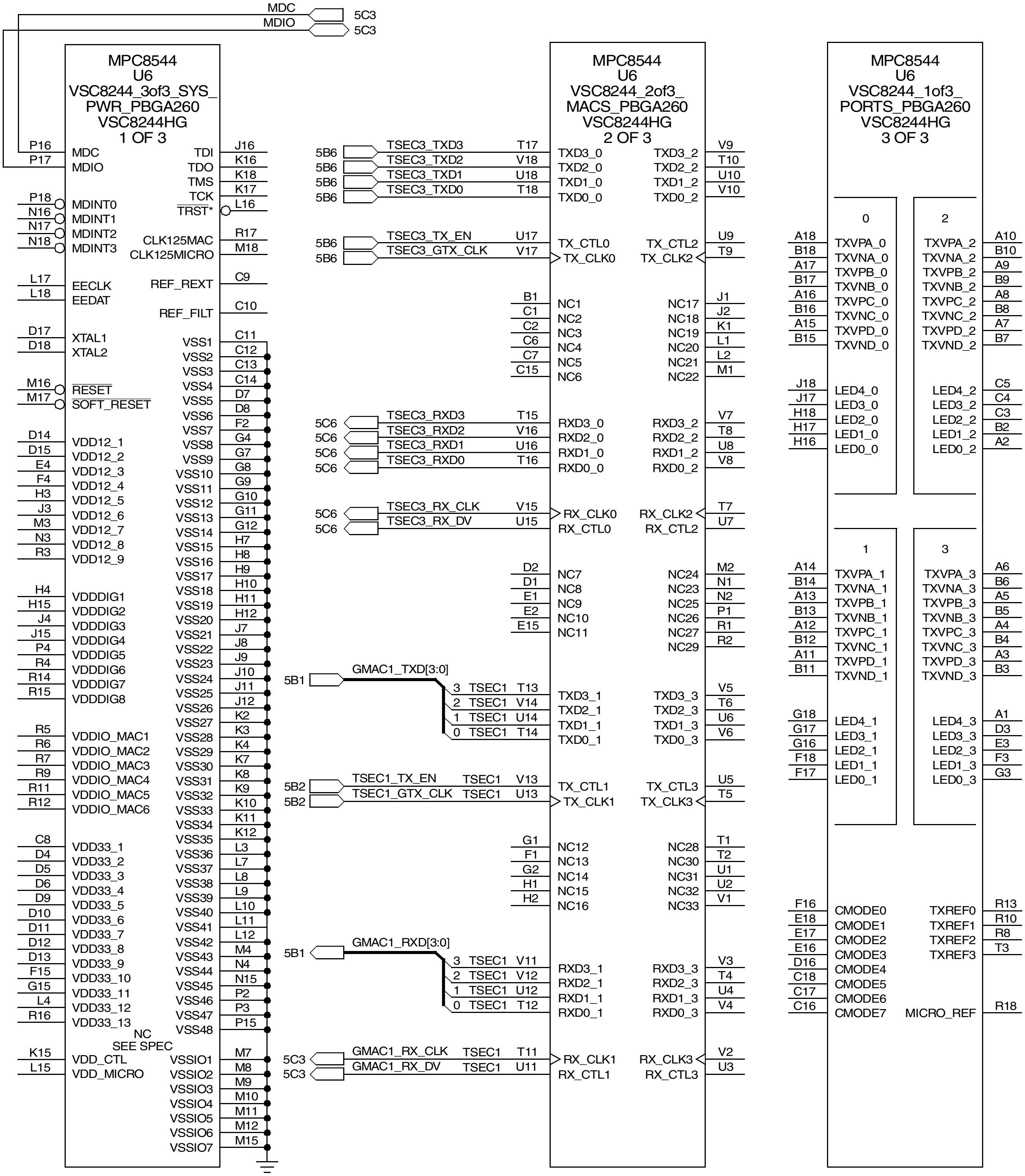


Figure 32. GBE PHYs

10 Current Delivery in the BGA Field

The MPC8544E comes in a 1 mm pitch, 783 BGA package arranged as a 28 × 28 array (with pin A1 missing). The BGA pads and vias usually have the physical parameters listed Table 9.

Table 9. MPC8544E Escape Dimensions

Dimension	Size	Notes
Drill diameter	10 mils	Via drill
Finished hole size (FHS)	7–7.5 mils	After plating
Pad	19 mils	
Anti-pad	28 mils	Clearance from via pads to adjacent plane area-fills
Thermal relief	33 mils^2	
Via keepout	23 mils	As above, but for traces on signal (inner) planes

Keep the following points in mind while reading this section:

- The remainder of this section is based on the padstack dimensions in Table 9. If a different padstack is used, most or all of the numbers derived probably need to be recalculated.
- It is assumed that each BGA connection carries current equally, no matter its proximity to the power supply and/or processor internal power pads. In reality, the current is non-uniformly distributed due to internal BGA-to-die substrate connections and other factors. There are no guaranteeable distributions among the power pins.

All comments in this section about power planes apply equally to the return ground. Multilayer PCBs often have multiple ground planes, so this restriction is occasionally overlooked; however, the ground return path requirements are exactly equal to the power source path requirements.

In addition to bypass capacitor placement, the designer must also consider the wholesale delivery of power to the V_{DD} pins. On most PCBs, the power plane is not actually solid, but is perforated by numerous vias. This is illustrated in Figure 33, where the wide plane is actually only as wide as its narrowest point.

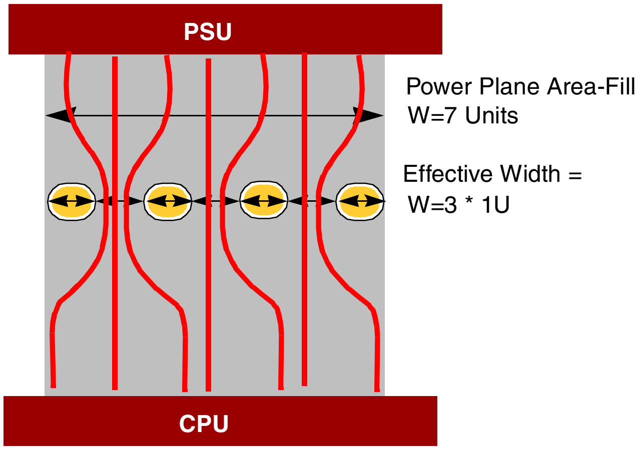


Figure 33. Restricted Current Flow

For many applications, the effect of the vias passing through the power plane on the flow of current is insignificant. However, as the power reaches the outer periphery of the MPC8544E, it must flow through the outer array of signal BGA vias. While some BGA pads may not need vias (outer BGA pads may be able to route out on the top layers); in most cases the number of interfering vias ranges from 8 to 11.

For many layouts, the outer one or two BGA pads do not require vias as these signals are usually “escaped” on the top layer of the PCB. Delivering power properly to the power pins requires planning the flow of current around these vias, or more properly, the antivias or antipads that surround the via and cause a hole on the power plane layer. When coupled with a 1-mm spacing, the cross section of the PCB typically resembles that shown in Figure 6.

The anti-pad is larger than the spacing between the via barrels, which in effect reduces the width and capacity of the trace. In effect, the power plane is not a solid plane but a parallel array of traces with one of the following widths:

- 11.3 mils, when planes must be isolated from both vias
- 19.3 mils, when planes connect to one of the vias

The standard formulae to determine the limits of the copper trace are described in the IPC-2221A standard and are given by:

$$\text{race, Outer)} = 0.048 \times (\text{maxTempRise})^{0.44} \times (\text{viaPlating} \times \text{viaDiameter} \times \pi)^{0.7} \qquad \textbf{Eqn. 1}$$

$$\text{race, Inner)} = 0.024 \times (\text{maxTempRise})^{0.44} \times (\text{viaPlating} \text{ ¥ } \text{viaDiameter} \times \pi)^{0.7} \qquad \textbf{Eqn. 2}$$

Using these formulae, and using an 11-mil trace as a standard (rounded down from the actual 11.3-mil max trace width), for various layout rules the amount of current that can be safely carried, assuming a maximum temperature rise of 20°C, is shown in Table 10.

Table 10. Current-Carrying Capacity per Standard IPC2221A

Location	Copper Plating (oz.)	11-mil Trace (A)
Outer	0.5	0.777
	1.0	1.285
	1.5	1.730
	2.0	2.130
Inner	0.5	0.390
	1.0	0.582
	1.5	0.865
	2.0	1.065

10.1 Via Current Capacity

Unless the power is delivered on the top plane and attaches directly to the BGA pad of the processor (which as noted is fairly difficult to accomplish), power is delivered from one or more PCB planes to the processor through vias. Given the padstack parameters in Table 9 and the number of vias allocated, the next step to ensure a quality PDS is to evaluate the individual and aggregate via current capacity using the following formula:

$$VIA = 0.048 \times (maxTempRise)^{0.44} \times (viaPlating \times viaDiameter \times \pi)^{0.72} \qquad \textbf{\textit{Eqn. 3}}$$

Table 11 shows a few via current capacities for given PCB process parameters.

Table 11. Via Capacity

maxTempRise (°C)	viaPlating (mil)	viaDiameter (mil)	I_{VIA} (A)	Notes
10	1	10	1.609	Standard
10	1	11	1.724	—
10	1	15	2.159	—
10	1.5	10	2.159	—
20	1	10	2.183	—

At 1.609 A/via, we have a maximum current capacity of 22.5 A for V_{DD_CORE} (14 vias * 1.609), and 16 A for V_{DD_PLAT} (10 * 1.609).

10.2 Alternate Plane Current Capacity

Research performed by Johannes Adam of Flomerics as preparatory work for a revision to one of the rules of the IPC2221 standard (specifically, design rule 2152), found that the formula for outer traces was based on materials and assumptions no longer prevalent. Additionally, he discovered that the 50-percent derating factor used for inner traces is wholly arbitrary and should be approximately 5 percent. In particular, thermal conduction to adjacent traces and power planes was found to be vastly more important than conduction to free space. Refer to Section 1, “References,” for details on this paper and associated historical data.

At the time of publication, the IPC2221 has not been updated based on these findings, so the designer can either follow the published standards and accept overly conservative numbers or incorporate the pending changes. Freescale cannot recommend one course over the other and advises designers to consult the original source documentation and decide for themselves. In *New Correlations Between Electrical Current and Temperature Rise in PCB Traces*, an examination of “Case 5” shows an outer trace of variable width over a 35-µm (1-oz. copper) plane (see Section 1, “References”). This correlates nicely with an external power connection residing over an inner ground plane immediately adjacent to it. Such a plane is desirable not only for power purposes but for routing differential pairs such as those on the SerDes or DDR interfaces. Extracting the data for a 0.3-mm trace (~11 mils) and applying a curve fitting process to the data produces the following formula, represented in Figure 34:

$$T(trace) = 19.473 + 3.228IMAX + 4.469IMAX^{2} + 0.385IMAX \qquad \textbf{\textit{Eqn. 4}}$$

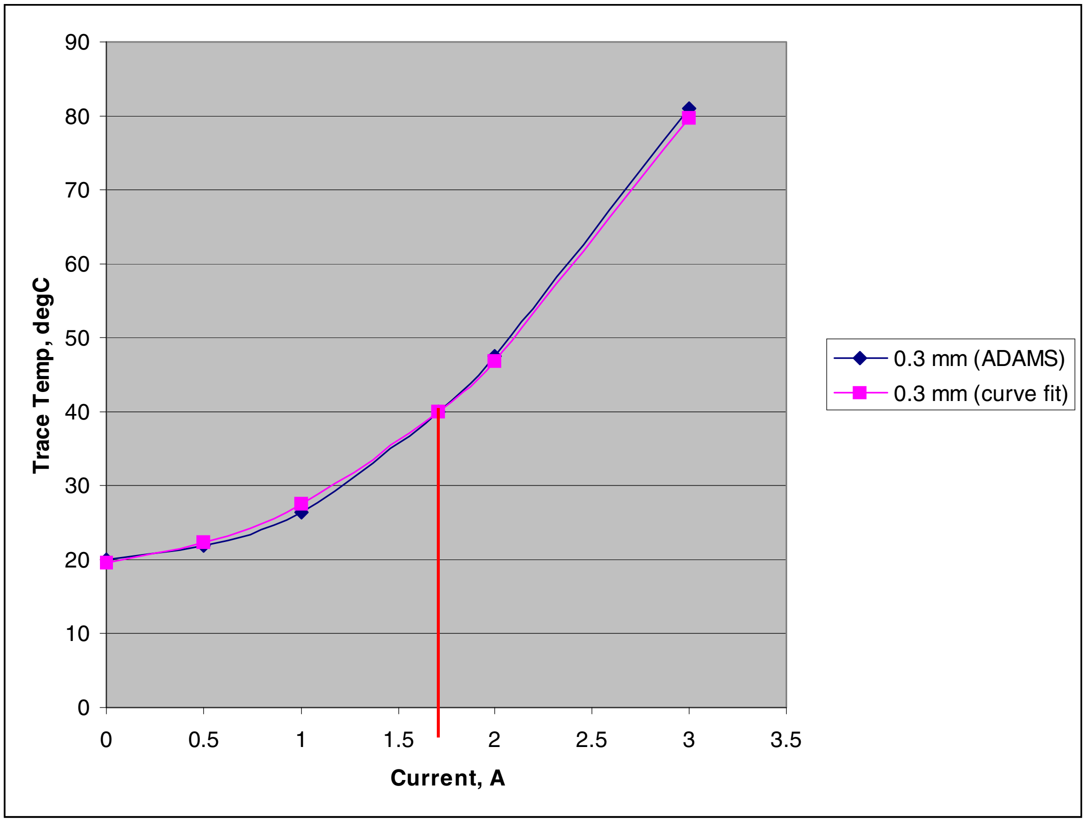


Figure 34. Extrapolated Current Flow

CAUTION

> This curve is valid only for the 0.3 mm trace. The IPC standard will likely include a more complicated curve equation that accepts both current and trace width as a parameter.

Note that the Y-axis is the total trace temperature. Because we are concerned with a maximum 20°C rise, the Y-axis starts at 20 as the ambient temperature is also assumed to be 20°C. The crossover point of 40°C occurs when I = 1.711 A. Using this new data, Table 10 can be updated as shown in Table 12:

Table 12. Current-Carrying Capacity Extrapolated from Adams

Location	Copper Plating (oz.)	A/11-mil Trace (A)
Outer	0.5	1.210
	1.0	1.711
	1.5	2.420
	2.0	3.422

Table 12. Current-Carrying Capacity Extrapolated from Adams (continued)

Location	Copper Plating (oz.)	A/11-mil Trace (A)
Inner	0.5	1.149
	1.0	1.625
	1.5	2.299
	2.0	3.251

New Correlations Between Electrical Current and Temperature Rise in PCB Traces explains why the classic IPC-275/IPC2221A values for inner current layers are extremely misleading. IPC-2152 is not published at the time of this application note.

11 Revision History

Table 13 provides a revision history for this application note.

Table 13. Document Revision History

Rev. Number	Date	Description
0	01/08	Initial release.

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