Configurable Logic Cell (CLC)

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets.

Please consult the note at the beginning of the **"Configurable Logic Cell (CLC)"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com.

This document supersedes the following PIC24 and dsPIC33 Family Reference Manual sections:

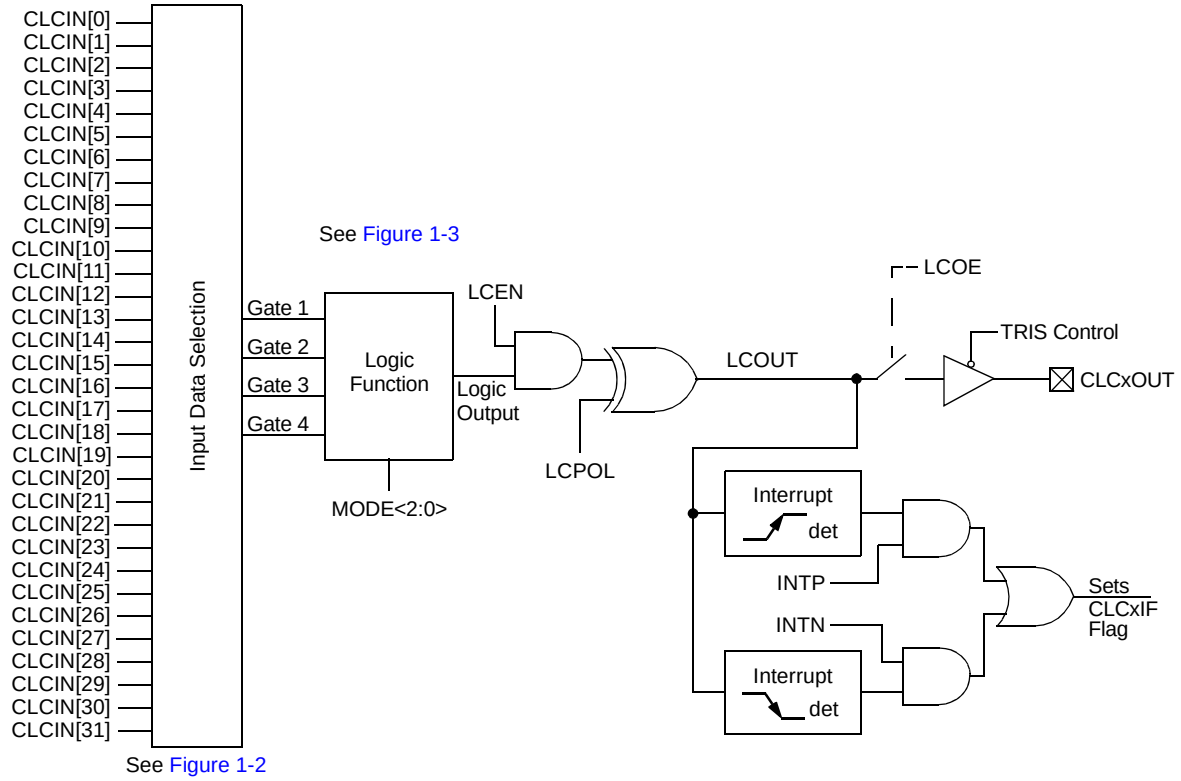
DS Number	Section Number	Title
DS33949A	63	Configurable Logic Cell (CLC)

1.0 INTRODUCTION

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function, and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs, since the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

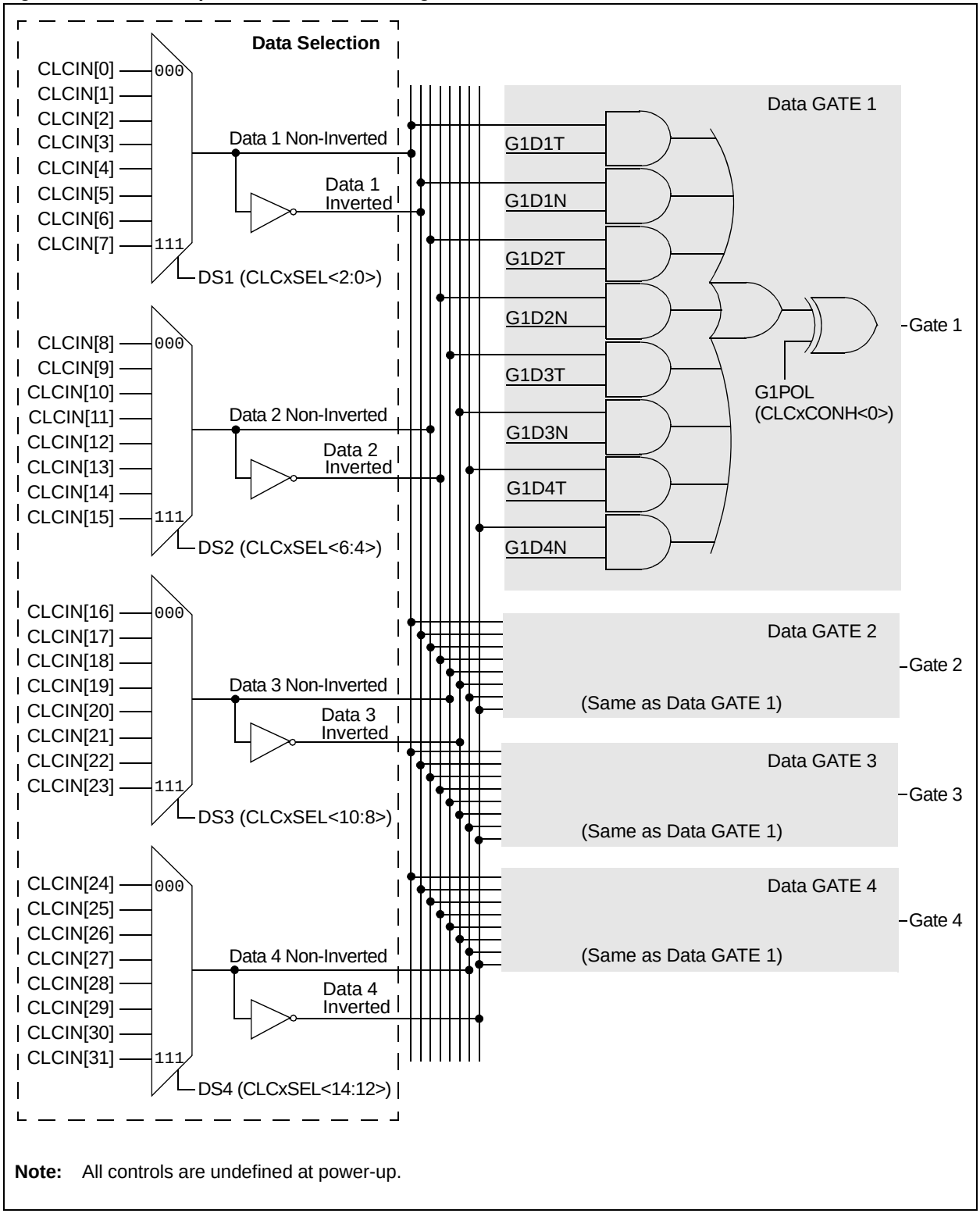
The CLC consists of four main sections, as shown in Figure 1-1. First, the input data selection MUXes route input signals to the four data gates, as shown in Figure 1-2. Each of the four data gates can then select any of the 32 input signals to pass along to the logic functions shown in Figure 1-3. The output of the logic function is then supplied to the internal logic and external pin, and can generate interrupts. The output of a CLC module can be routed to the input of another CLC module to create more complex logic functions.

Figure 1-1: Configurable Logic Cell



Note: All Configuration bits shown in this figure can be found in the CLCxCONL register.

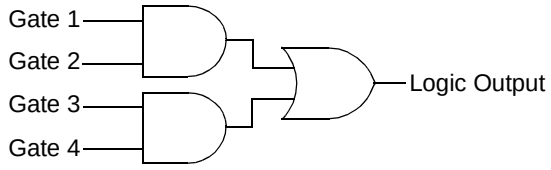
Figure 1-2: CLC Input Source Selection Diagram



Note: All controls are undefined at power-up.

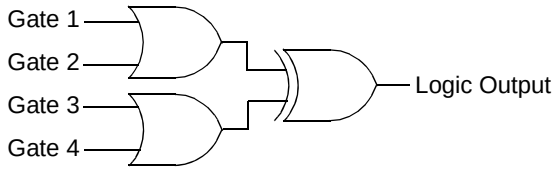
Figure 1-3: Logic Function Combinatorial Options

AND – OR



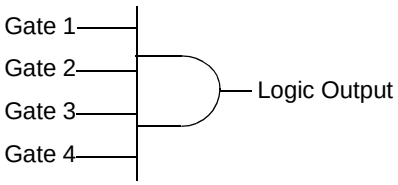
MODE<2:0> = 000

OR – XOR



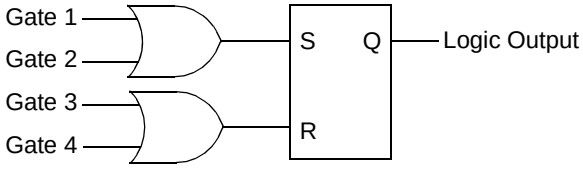
MODE<2:0> = 001

4-Input AND



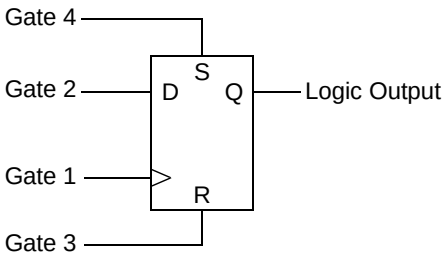
MODE<2:0> = 010

S-R Latch



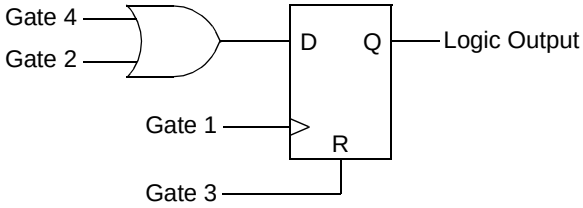
MODE<2:0> = 011

1-Input D Flip-Flop with S and R



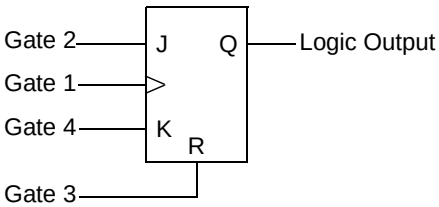
MODE<2:0> = 100

2-Input D Flip-Flop with R



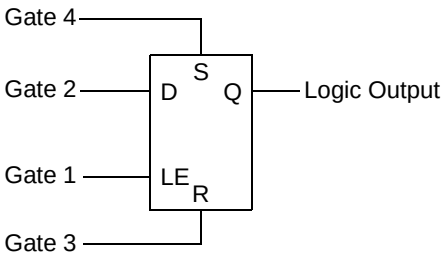
MODE<2:0> = 101

J-K Flip-Flop with R



MODE<2:0> = 110

1-Input Transparent Latch with S and R



MODE<2:0> = 111

2.0 REGISTERS

The CLC module is controlled by the following registers:

- CLCxCONL
- CLCxCONH
- CLCxSEL
- CLCxGLSL
- CLCxGLSH

The CLCx Control registers (CLCxCONL and CLCxCONH) are used to enable the module and interrupts, control the output enable bit, select output polarity, and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Input MUX Select register (CLCxSEL) allows the user to select one out of eight input signals for each of the four data selection multiplexers, pictured inside the dotted line in Figure 1-2. The output of each of the four data selection multiplexers is connected to the inputs of the logic function selected by the MODE<2:0> bits (CLCxCONL<2:0>), see Figure 1-3.

The CLCx Source Enable registers (CLCxGLSL and CLCxGLSH) allow the user to create any four variable boolean expressions from the four input data sources configured by CLCxSEL. Both the true and complimentary values for each of the four signals, chosen by the CLCx Input MUX Select register (CLCxSEL), are available to the sum-of-products circuit pictured in the data gate in Figure 1-2.

Register 2-1: CLCxCONL: Configurable Logic Cell x Control Register (Low)

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
LCEN	—	—	—	INTP	INTN	—	—
bit 15							bit 8

R-0	R-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
LCOE	LCOUT	LCPOL	—	—	MODE2	MODE1	MODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **LCEN:** Configurable Logic Cell Enable bit
1 = Configurable Logic Cell is enabled and mixing input signals
0 = Configurable Logic Cell is disabled and has logic zero outputs

bit 14-12 **Unimplemented:** Read as ‘0’

bit 11 **INTP:** Configurable Logic Cell Positive Edge Interrupt Enable bit
1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** Configurable Logic Cell Negative Edge Interrupt Enable bit
1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **LCOE:** Configurable Logic Cell Port Enable bit
1 = Configurable Logic Cell port pin output is enabled
0 = Configurable Logic Cell port pin output is disabled

Register 2-1: CLCxCONL: Configurable Logic Cell x Control Register (Low) (Continued)

bit 6 **LCOUT:** Configurable Logic Cell Data Output Status bit
1 = Configurable Logic Cell output high
0 = Configurable Logic Cell output low

bit 5 **LCPOL:** Configurable Logic Cell Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **MODE<2:0>:** Configurable Logic Cell Mode bits
111 = Cell is 1-input transparent latch with S and R
110 = Cell is JK flip-flop with R
101 = Cell is 2-input D flip-flop with R
100 = Cell is 1-input D flip-flop with S and R
011 = Cell is SR latch
010 = Cell is 4-input AND
001 = Cell is OR-XOR
000 = Cell is AND-OR

Register 2-2: CLCxCONH: Configurable Logic Cell x Control Register (High)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Gate 4 logic is inverted when applied to the logic cell
0 = The output of Gate 4 logic is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Gate 3 logic is inverted when applied to the logic cell
0 = The output of Gate 3 logic is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Gate 2 logic is inverted when applied to the logic cell
0 = The output of Gate 2 logic is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Gate 1 logic is inverted when applied to the logic cell
0 = The output of Gate 1 logic is not inverted

Register 2-3: CLCxSEL: Configurable Logic Cell x Input MUX Select Register

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS4<2:0>			—	DS3<2:0>		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS2<2:0>			—	DS1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 4

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 3

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 2

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 1

Register 2-4: CLCxGLSL: Configurable Logic Cell x Source Enable Register (Low)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **G2D4T:** Gate 2 Data 4 True Enable bit
1 = The Data 4 (non-inverted) signal is enabled for Gate 2
0 = The Data 4 (non-inverted) signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 2
0 = The Data 4 (inverted) signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 2
0 = The Data 3 (non-inverted) signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 2
0 = The Data 3 (inverted) signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 2
0 = The Data 2 (non-inverted) signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 2
0 = The Data 2 (inverted) signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 2
0 = The Data 1 (non-inverted) signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 2
0 = The Data 1 (inverted) signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data 4 True Enable bit
1 = The input_src4 (non-inverted) signal is enabled Gate 1
0 = The input_src4 (non-inverted) signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 1
0 = The Data 4 (inverted) signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 1
0 = The Data 3 (non-inverted) signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 1
0 = The Data 3 (inverted) signal is disabled for Gate 1

Register 2-4: CLCxGLSL: Configurable Logic Cell x Source Enable Register (Low) (Continued)

bit 3 **G1D2T:** Gate 1 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 1
0 = The Data 2 (non-inverted) signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 1
0 = The Data 2 (inverted) signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 1
0 = The Data 1 (non-inverted) signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 1
0 = The Data 1 (inverted) signal is disabled for Gate 1

Register 2-5: CLCxGLSH: Configurable Logic Cell x Source Enable Register (High)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **G4D4T:** Gate 4 Data 4 True Enable bit
1 = The Data 4 (non-inverted) signal is enabled for Gate 4
0 = The Data 4 (non-inverted) signal is disabled for Gate 4

bit 14 **G4D4N:** Gate 4 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 4
0 = The Data 4 (inverted) signal is disabled for Gate 4

bit 13 **G4D3T:** Gate 4 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 4
0 = The Data 3 (non-inverted) signal is disabled for Gate 4

bit 12 **G4D3N:** Gate 4 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 4
0 = The Data 3 (inverted) signal is disabled for Gate 4

bit 11 **G4D2T:** Gate 4 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 4
0 = The Data 2 (non-inverted) signal is disabled for Gate 4

bit 10 **G4D2N:** Gate 4 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 4
0 = The Data 2 (inverted) signal is disabled for Gate 4

bit 9 **G4D1T:** Gate 4 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 4
0 = The Data 1 (non-inverted) signal is disabled for Gate 4

Register 2-5: CLCxGLSH: Configurable Logic Cell x Source Enable Register (High) (Continued)

bit 8 **G4D1N:** Gate 4 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 4
0 = The Data 1 (inverted) signal is disabled for Gate 4

bit 7 **G3D4T:** Gate 3 Data 4 True Enable bit
1 = The Data 4 (non-inverted) signal is enabled Gate 3
0 = The Data 4 (non-inverted) signal is disabled for Gate 3

bit 6 **G3D4N:** Gate 3 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 3
0 = The Data 4 (inverted) signal is disabled for Gate 3

bit 5 **G3D3T:** Gate 3 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 3
0 = The Data 3 (non-inverted) signal is disabled for Gate 3

bit 4 **G3D3N:** Gate 3 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 3
0 = The Data 3 (inverted) signal is disabled for Gate 3

bit 3 **G3D2T:** Gate 3 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 3
0 = The Data 2 (non-inverted) signal is disabled for Gate 3

bit 2 **G3D2N:** Gate 3 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 3
0 = The Data 2 (inverted) signal is disabled for Gate 3

bit 1 **G3D1T:** Gate 3 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 3
0 = The Data 1 (non-inverted) signal is disabled for Gate 3

bit 0 **G3D1N:** Gate 3 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 3
0 = The Data 1 (inverted) signal is disabled for Gate 3

3.0 CLC SETUP

CLCxCONL selects the logic function, and determines and controls the I/O pins. CLCxCONH controls output signal polarity. LCEN (CLCxCONL<15>) must be set for the CLC to operate. All registers can be programmed while LCEN is clear.

The CLCxSEL (Register 2-3) register controls which input signals are routed to the input bus of Figure 1-2. Both the True (T) and Negated (N) values are made available in the data bus.

The CLCxGLSL (Register 2-4) and CLCxGLSH (Register 2-5) registers select which signals from the data bus are applied to the input OR gates. True and Negated inputs are separately enabled; do not enable both for the same signal.

The final polarity of the CLC module output is controlled by LCPOL (CLCxCONL<5>). The output is inverted when LCPOL = 1 and uninverted when LCPOL = 0. The GxPOL bits (CLCxCONH<3:0>) control the polarity of the logic function inputs.

The INTP and INTN pins (CLCxCONL<11:10>) enable interrupts on the rising and falling edge of the CLC output.

The LCOUT bit is read-only and reflects the status of the logic cell output. To output the CLCxOUT signal to an I/O pin, set the LCOE bit and configure the I/O as a digital output. On some devices, the CLCxOUT signal is made available through Peripheral Pin Select (PPS) and will need to be configured.

4.0 INPUT PROVIDERS

Each logic cell in the CLC takes four inputs, one from each of the four data gates. Each data gate is connected to eight input sources. The data gate allows the selection between the inverted or non-inverted polarity of each input source. Input sources available for use with the CLC vary by device. Refer to the specific device data sheet for available options.

4.1 Source Multiplexers

The module has four input source multiplexers. Multiplexer inputs are selected by setting control bits in the CLCxSEL register to define the data source selected through each of the four data selection multiplexers. Each of the four data selection multiplexers feeds one of the four logic function input gates, shown in Figure 1-3. The module has an internal data bus created from the output of each input source multiplexer (see Figure 1-2). The data bus has both True (T) and Negated (N) versions of each selected input source. Therefore, up to eight signals are available on the internal data bus to connect to the input gates of the logic function.

4.2 Logic Input Gates

Four logic input gates are used to route input sources from the data selection multiplexers into the four logic function inputs. The True and Negated forms of each input source signal are available for use by each logic gate. The input signal sources are enabled for use by each logic function input using the CLCxGLS registers. There are up to eight signals that can be enabled for use by each logic function input. Any number of the eight signal sources may be enabled for each of the four logic function inputs. Each logic gate provides a logical OR of the input signals. The selected (True or Negated) signals are OR'd to form the gate output data. The logical NAND is obtained by changing the output polarity with the GxPOL bits. If the logical AND is required instead, select negated inputs and invert the output polarity according to DeMorgan's theorem. If all inputs are negated and applied to a NOR, the result is identical to an AND operation. Written algebraically:

C = A AND B

is the same as:

C = NOT(NOT(A) OR NOT(B)).

Table 4-1 summarizes the basic functions that can be obtained by using the gate control bits. The table shows the use of all four input multiplexer sources, but the input gates can be configured to use less. If no inputs are selected (CLCxGLS = 0x00), the output will be zero or one, depending on the GxPOL bits.

Table 4-1: Example Logic Functions

CLCxGLS	GxPOL Bits	Function
0xAAAA	0	OR (D1, D2, D3, D4)
0xAAAA	1	NOR (D1, D2, D3, D4)
0x5555	0	NAND (D1, D2, D3, D4)
0x5555	1	AND (D1, D2, D3, D4)
0x0000	0	Logic '0'
0x0000	1	Logic '1'

If the output of a gate must be zero or one, the recommended method is to set all of the bits related to that gate in CLCxGLS to zero and use the Gate Polarity bit, GxPOL, to set the desired level.

4.3 Logic Function

There are eight available logic functions, including:

- AND-OR
- OR-XOR
- AND
- S-R Latch
- D Flip-Flop with Set and Reset
- D Flip-Flop with Reset
- J-K Flip-Flop with Reset
- Transparent Latch with Set and Reset

Logic functions are shown in Figure 1-3. Each logic function has four inputs and one output. The MODE<2:0> bits (CLCxCONL<2:0>) set the functional behavior of the logic cell. There are four combinatorial options and four state options. Three of the state options define Input Gate 1 as a rising edge clock, with the traditional meanings of D and J-K flip-flops. The 4th state option, MODE<2:0> bits = 111, is a transparent latch; Q follows D when Latch Enable (LE) is true; Q holds state when LE is false. For options with both S (Set) and R (Reset) inputs, the output changes asynchronously to the clock when S or R is a logic '1'; R is dominant.

4.4 Software Inputs

The gate data input to the logic function can be directly controlled by software by setting all of the CLCxGLSL/H bits associated with the logic gate to '0', and writing to the appropriate GxPOL bit (see Table 4-1). The gate output will be equal to the value of the GxPOL bit.

5.0 OUTPUT

LCOUT (CLCxCONL<6>) is the logic cell output and is routed to the I/O port pin or to other modules within the device. In all cases, the signal value is taken after the LCPOL inverter. To observe this output on an I/O pin, the user will need to set LCOE (CLCxCONL<7>).

6.0 APPLICATION LOGIC

The CLC provides both combinatorial and state (see Figure 1-3) logic function options. The outputs of the input gates are applied to the logic function. If CLCxGLS = 0x00, the function receives a logic '0' when the GxPOL bits (CLCxCONH<3:0>) are clear or a logic '1' when the GxPOL bits are set.

6.1 Combinatorial Logic

The combinatorial functions (MODE<2:0> = 010, 001, 000) build on the AND/OR logic of the input gate. The 4-input AND can provide an OR function by inverting the inputs and outputs using DeMorgan's theorem. Inverting the output of the XOR is the same as inverting one input (but not both).

The SR function (MODE<2:0> = 011) is not affected when LCEN (CLCxCONL<15>) is cleared, as is the case with the State Logic register. The latch is Reset-dominant, meaning that the Reset signal takes precedent over any Set signal that may be present.

6.2 State Logic

The state functions include both D and J-K flip-flops with asynchronous Set (S) and Reset (R). Input Gate 1 provides a rising edge clock. If a falling edge clock is required, Gate 1 can be inverted in the gate logic (G1POL). Input Gate 2, and sometimes also Gate 4, provide data to the register or latch input(s). When operating in Transparent Latch mode (MODE<2:0> = 111), the output, Q, follows D while LE is high and holds state while LE is low.

The various modes may or may not share state memory and switching modes may or may not change the state of the state variable. For all modes, the register is Reset-dominant.

7.0 CLC INTERRUPTS

The CLC module has two types of interrupts that can be enabled: rising edge interrupt events and falling edge interrupt events. These events are enabled by the INTP (CLCxCONL<11>) and INTN (CLCxCONL<10>) control bits, respectively.

A valid occurrence of either interrupt will set the CLC Interrupt Flag, CLCIF. This will occur when the module is enabled (LCEN = 1) and either a rising edge output occurs when INTP = 1, or a falling edge event occurs when INTN = 1.

If the initial output state of the CLC logic is '1' and INTP = 1, an interrupt will be generated when LCEN is set to '1'. Likewise, an interrupt will be generated if the initial output state of the CLC is '0' and INTN = 1. These conditions must be detected and cleared in software. Similarly, a false interrupt could be generated if INTP or INTN is set while the CLC module is enabled.

The user should be sure to clear any spurious interrupt events that may occur in the initialization process of the CLC module.

If the CLC Interrupt Enable bit, CLCIE, is cleared, an interrupt will not be generated. However, the CLCIF bit will still be set if an interrupt condition occurs. The user can clear the interrupt in the Interrupt Service Routine (ISR) by clearing CLCIF. See **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"* for more information.

8.0 OPERATION IN SLEEP MODE

The CLC module is not affected by Sleep mode, since it does not rely on system clock sources for operation. However, some input sources might be disabled during Sleep, so the function could be disrupted. If the source continues to operate, so will the module. Refer to the specific device data sheet for more information.

9.0 OPERATION IN IDLE MODE

The CLC module is not affected by Idle mode, since it does not rely on system clock sources for operation. However, some input sources might be disabled during Idle and the function could be disrupted. If the sources continues to operate, so will the module. Refer to the specific device data sheet for more information.

10.0 RESET

When the LCEN bit is written to '0', the output of all state logic functions will be reset to '0'. A system Reset returns the CLCxCONL, CLCxCONH, CLCxSEL, CLCxGLSL and CLCxGLSH registers to the default state and disables the module.

Asserting a device Reset returns all bits in the module registers to the default state. The output of all logic functions is '0' after a Reset; this includes both latch and flip-flop functions. When a device Reset is asserted, LCEN (CLCxCONL<15>) = 0, the state logic is reset and the output of the logic function is forced low.

11.0 REVISION HISTORY

Revision A (November 2016)

This is the initial released revision of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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