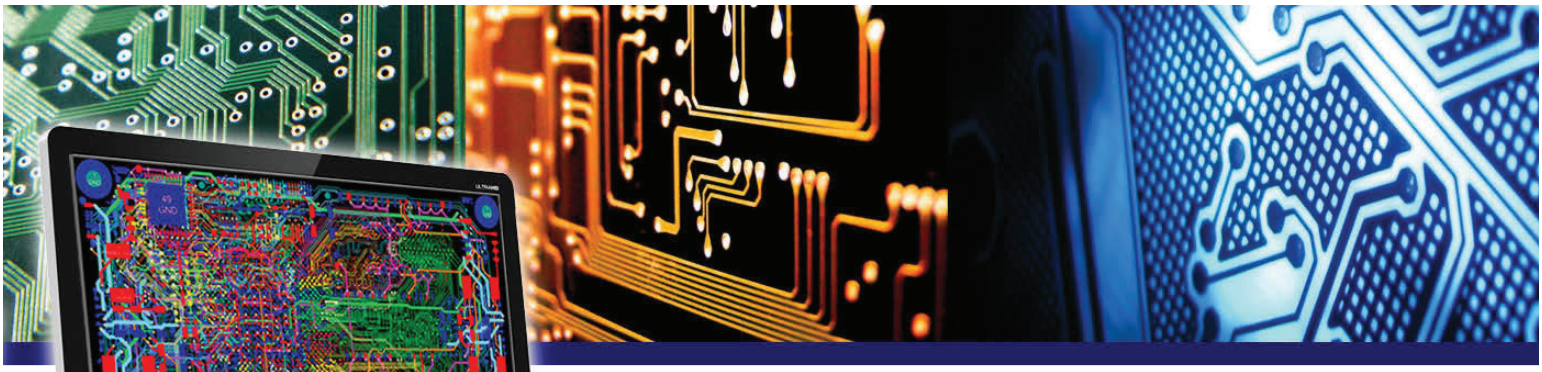

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COLUMN

Design Rules & DFM for High-Speed Design

by Barry Olney
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Summary: Rules are necessary for compatibility with target manufacturing equipment and processes. Guidelines, on the other hand, are nice to have, but not critical in getting the product out the door.

Requirements for PCB design can vary considerably from one design to the next. I specialize in high-speed design (HSD) but I am often asked to do a board that incorporates a switch-mode power supply. Or, there may be an analog section that needs to be laid out—so the design rules I use vary depending on the application.

Where to Start?

IPC was founded in 1957. The association has provided the worldwide electronics industry with guidelines for design and manufacture of PCBs, compiled over the years, with the support of both committee and industry members.

IPC-2221A is the foundational design standard for all documents in the IPC-2220 series. The series is built around the IPC-2221, *Generic Standard on Printed Board Design,* the base document that covers all generic requirements for printed board design, regardless of materials. From here, the designer chooses the appropriate sectional standard for a specific technology.

All five sectional standards are included with the series:

- IPC-2222: Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2223: Sectional Design Standard for Flexible Printed Boards
- IPC-2224: Sectional Standard for Design of PWBs for PC Cards
- IPC-2225: Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies
- IPC-2226: Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

This series provides coverage on material and final finish selection, current-carrying capacity and minimum electrical clearances, test-specimen design, guidelines for V-groove scoring, dimensioning requirements and conductor thickness requirements. Some of these standards are now published in Chinese and German.

Several documents apply to HSD and land-pattern design:

- IPC-2251: Design Guide for Electronic Packaging Utilizing High-Speed Techniques
- IPC-2141A: Design Guide for High-Speed Controlled Impedance Circuit Boards
- IPC-7351B: Generic Requirements for Surface Mount Design and Land Pattern Standard

These standards (and their predecessors) have been part of a well-used section of my technical library since 1987. They provide excellent reading and reference material for all PCB designers. These documents are available for purchase from www.ipc.org.

Design rules must keep up with the latest devices and fabrication processes—without losing sight of design for manufacturability (DFM), which is the practice of designing board products that can be produced in a cost-effective manner using *existing* manufacturing processes and equipment. If you follow the above IPC guidelines, you will be designing for both manufacturability and mass production. On the opposite end of the spectrum are the prod-

uct development cowboys—typically research groups whose main interest is proving a technology and not designing for production. I must admit that I, too, come from this background and had to learn my lessons the hard way. Now, I take the approach that it is best to implement DFM *during* the design process. This does not incur any additional time, and in fact can save time in reduced board iterations.

Reference designs are probably the best example of cowboys at work. I have seen some reference designs fail to adhere to current best practices, and that should never be implemented in a production board.

DFM is gaining more recognition as it becomes clear that the cost reduction of printed circuit assemblies cannot be controlled by manufacturing engineers alone—the PCB designer now plays a critical role.

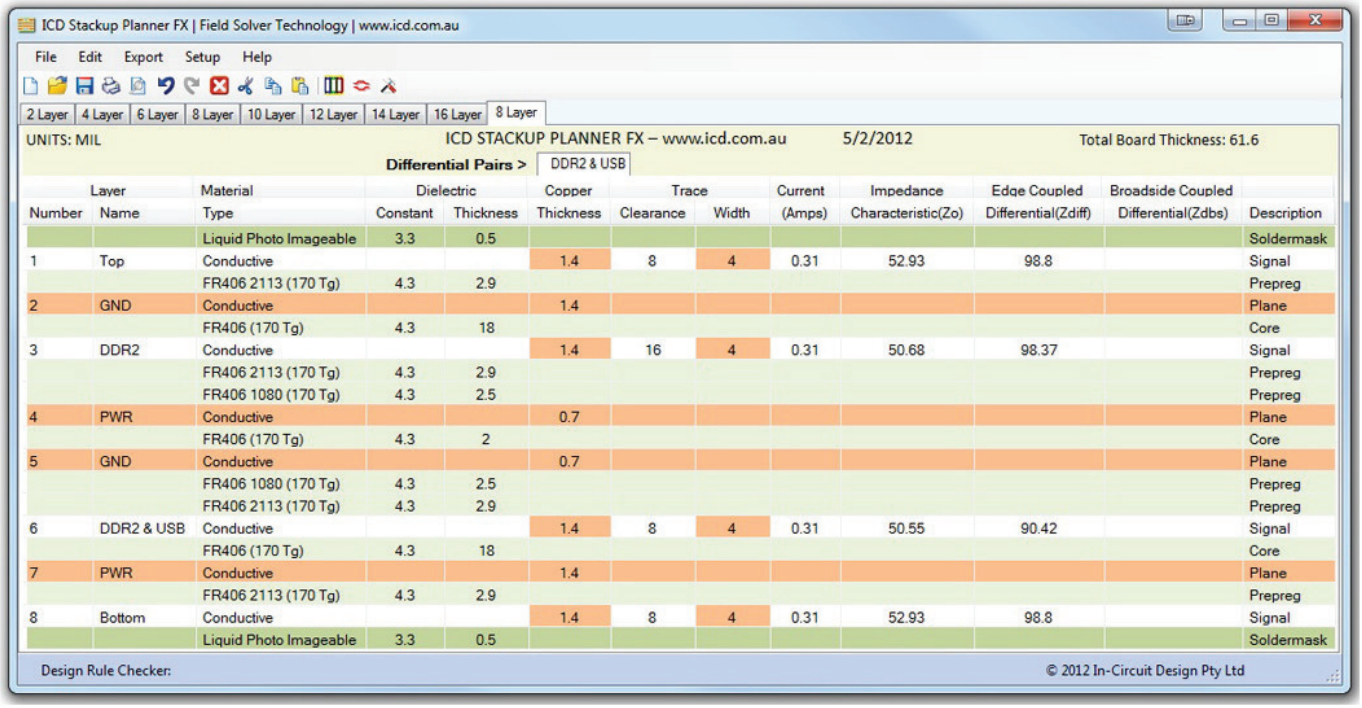
DFM requires an integrated effort throughout the entire design and production process. Design rules and guidelines should be established and adhered to. *Rules* are necessary for compatibility with planned manufacturing equipment and fabrication processes. *Guidelines,* on the other hand, are nice to have but are not critical in getting the product out the door.

Do a quick Google search of fabrication shop capabilities, and look for the common specifications. Printed Circuit Solutions, Inc. in Santa Ana, California (www.selectcircuits.com), provides a good example:

- Technology: 4/4 mil trace/clearance
- Min hole size: 7 mil
- Layers: multilayer up to 14
- Board Thickness: 20 to 125 mil
- Copper weight: ½ to 4 oz

Obviously, you can push these specifications, but it's seldom without a cost. Why go beyond these requirements if you do not have to? Remember, DFM is the practice of designing board products that can be *produced* in a cost-effective manner using *existing* manufacturing processes and equipment. For a typical DDRx board, I would not need to go beyond any of the above specifications.

Also, it is important to ask your chosen fabrication shop to provide a list of commonly stocked dielectric materials. This is important because if we use materials they do not stock, then we will incur additional cost and impact the schedule. Also, the selection of inappropri-



Layer Number	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Liquid Photo Imageable	3.3	0.5								Soldermask
1	Top	Conductive			1.4	8	4	0.31	52.93	98.8		Signal
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
2	GND	Conductive			1.4							Plane
		FR406 (170 Tg)	4.3	18								Core
3	DDR2	Conductive			1.4	16	4	0.31	50.68	98.37		Signal
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
		FR406 1080 (170 Tg)	4.3	2.5								Prepreg
4	PWR	Conductive			0.7							Plane
		FR406 (170 Tg)	4.3	2								Core
5	GND	Conductive			0.7							Plane
		FR406 1080 (170 Tg)	4.3	2.5								Prepreg
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
6	DDR2 & USB	Conductive			1.4	8	4	0.31	50.55	90.42		Signal
		FR406 (170 Tg)	4.3	18								Core
7	PWR	Conductive			1.4							Plane
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
8	Bottom	Conductive			1.4	8	4	0.31	52.93	98.8		Signal
		Liquid Photo Imageable	3.3	0.5								Soldermask

Figure 1: Stackup built using the fabricator's capabilities and stocked materials.

ate materials can vary the estimated impedance by up to 3%. If you plan ahead, knowing what a reputable fabricator has on hand, you can plan your board stackup—the foundation of every PCB design—with a high degree of certainty. Figure 1 illustrates a stackup built, incorporating the fabricator's capabilities and in-stock materials. This information can then be incorporated into the PCB specification and transferred to the fabricator, explicitly conveying the technical requirements of the engineering team.

If, for instance, we are designing a DDR2 board that also includes USB, then we need to use the 4/4 technology combined with the fabricators stocked dielectric materials to result in 50 ohms single ended and 100 ohms differential impedance for the DDR2, and 90 ohms differential for USB. The stackup in Figure 1 (determined by the ICD Stackup Planner Field Solver; downloadable from www.icd.com.au) accommodates both technologies on a single signal layer. For further details of DDR2 design rules (with specific implementation tips for Altium Designer), please see my previous article PCB Design Techniques for DDR, DDR2 and DDR3.

In order to select the appropriate via size, again we need to refer to the fabricator's capabilities. With a minimum hole size of 7 mil (0.1778mm), and considering the BGA's land pattern, we can determine the maximum size via pad and hole. The last DDR2 design I completed recently used a MCP831E processor in a 620 pin BGA of 1mm pitch. The recommended land size is 0.5mm (20 mil), so this gives us plenty of room (relatively speaking) to play with. The absolute maximum via size is 25/14 mil pad/hole. But keep in mind that if you use the maximum hole size, you also have to use the maximum antipad size, which would be 35 mil. Hmm…this does not leave a lot of copper between the antipads on the planes, so a good compromise might be a 20/10 mil via with a 30 mil antipad—still well within spec.

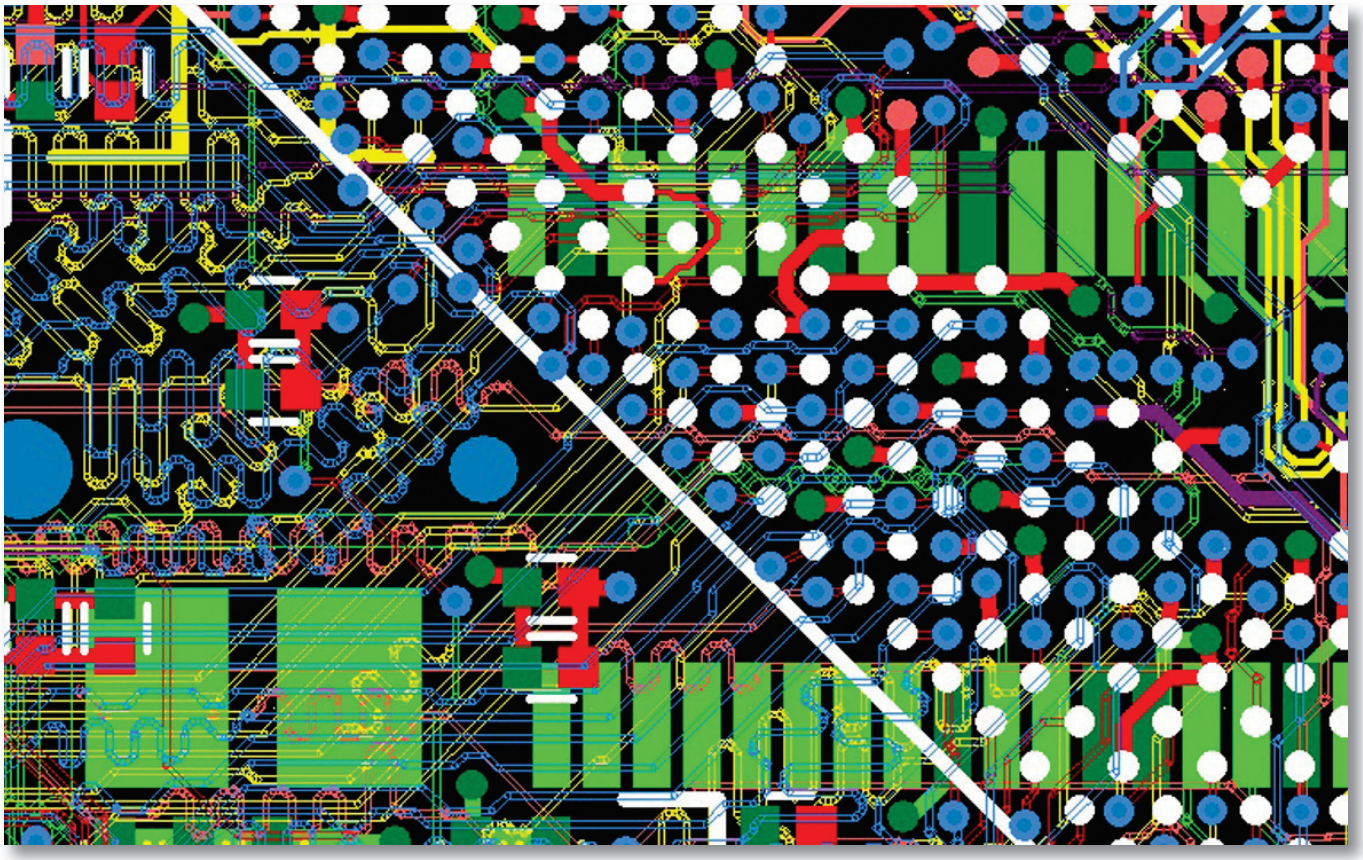


Figure 2: 1mm pitch BGA (highlighted) with 20/10 mil vias in between lands.

The technology used—directly impacting trace widths and clearances—can have an impact on the overall cost of the PCB, but this effect is relatively insignificant compared to the stackup cost. For instance, the use of blind and buried vias can add up to 30% to the total cost of fabrication (depending on batch size). However, adding two more layers to the stackup will only increase the cost by about 10%. So, although blind and buried vias are commonplace these days, there is still a big advantage in simply adding more layers. If you are designing the latest iPad, then no doubt the latest technologies will be called for. But for the majority of designs, standard manufacturing technologies can reduce overall costs.

To further reduce manufacturing costs, products should fit into a standard form factor, that is, a standard board shape and size, and with standardized hole locations for tooling.

But board size should not be confused with adhering to a standard form factor, as it relates to fabrication. Even if it is not possible to have a standard board size, a standard form-factor, or panelization strategy, can still be implemented in manufacturing. Standard panel sizes can be selected to accommodate various smaller boards in a "cracker board" panel, using the right "route and peck" profile. The most common panel size is 18" x 12". At least an inch around the perimeter must be left for handling during manufacture. If you have some flexibility in your board dimensions, and are developing a high-volume product, you can potentially save a lot of money by using as much real estate on a standard panel as possible. This, of course, requires some dutiful pre-layout planning, and communication with the manufacturing side of the operation.

Points to remember:

- IPC documents are recommended reading and an excellent reference material for all PCB designers
- Design rules must keep pace with the latest innovations in devices and fabrication processes
- Implement DFM proactively during the design process.
- The stackup should be pre-planned, in accordance with the fabricator's capabilities and stocked material
- DFM is the practice of designing board products that can be produced in a cost-effective manner using *existing* manufacturing processes and equipment
- Using maximum via holes sizes does not leave a lot of copper between the antipads on the planes
- For the majority of designs, standard manufacturing technologies can reduce overall costs

The benefits associated with concurrent DFM are as follows:

- Higher designed-in quality
- Fewer design revisions
- Faster time to market
- *Lower labor and material costs in fabrication*

All leading to increased profitability, as a result. **PCB**

References

1. Advanced Design for SMT—Barry Olney
2. PCB Design Techniques for DDR, DDR2 & DDR3—Barry Olney
3. Stackup Planning and the Manufacturing Process—Barry Olney
4. IPC-2220 series of Design Standards: www.ipc.org
5. The ICD Stackup Planner with 'Field Solver Technology' can be downloaded from www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd. (ICD), Australia, a PCB Design Service Bureau and board level simulation specialist. Among others, ICD was awarded "Top 2005 Asian Distributor Marketing," and "Top 2005 Worldwide Distributor Marketing" by Mentor Graphics, Board System Division. For more information, contact Olney at +61 4123 14441 or by e-mail: b.olney@icd.com.au.