AN3171
Application note

Comparing the M24C64-R, M24C64-F and M24C64-W devices to the M24LR64-R dual interface EEPROM

Introduction

The purpose of this application note is to explain the differences between the M24LR64-R dual interface EEPROM when controlled from the I²C bus, and the standard M24C64-F, M24C64-R, M24C64-W EEPROMs.

For simplification purposes, the M24C64-F, M24C64-R, M24C64-W will be referred to as M24C64 in the rest of the document.

For additional information, please refer to the M24LR64-R and M24C64 datasheets.

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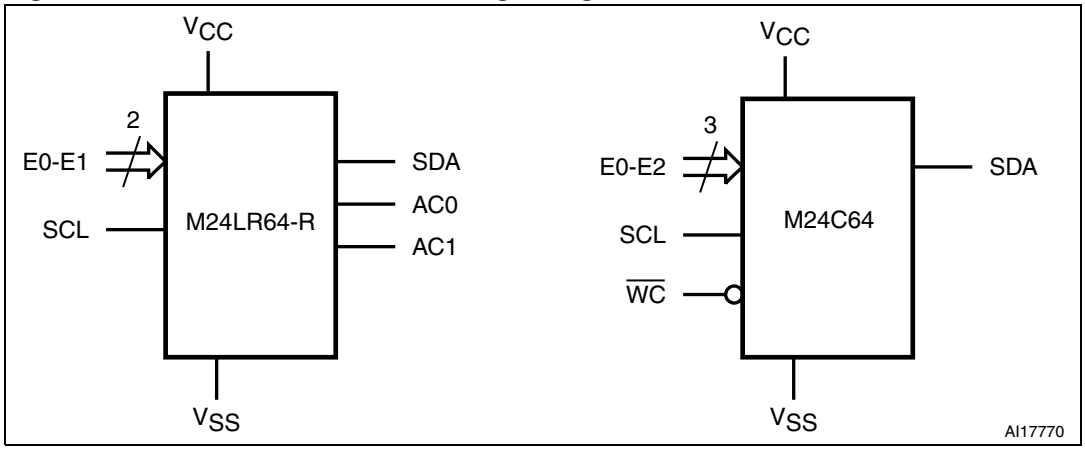
1 Hardware considerations

1.1 Pinout comparison

Figure 1 and *Figure 2* show the logic diagrams and the pinouts of the M24LR64-R and M24C64 devices, respectively.

Figure 1. M24LR64-R and M24C64 logic diagrams



M24LR64-R AC0/AC1 pins: due to its RF capability, the M24LR64-R dual interface EEPROM features two inputs (AC0 and AC1) to connect the RF antenna.

Consequently, two inputs present in the M24C64 are not offered in the M24LR64-R: these are E2 and Write Control ($\overline{WC}$).

Practically, this means that you will be able to use up to four M24LR64-R devices (defined by E0, E1) on the same I²C bus, compared to eight devices (defined by E0, E1, E2) for the M24C64.

The Write Control input ($\overline{WC}$) is used to write-protect the M24C64. The M24LR64-R can also be protected but in a different way, using the I2C_Write_Lock bits.

Figure 2. M24LR64-R and M24C64 pinouts

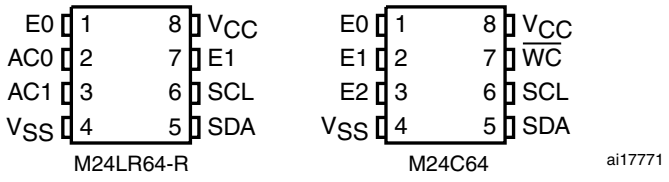


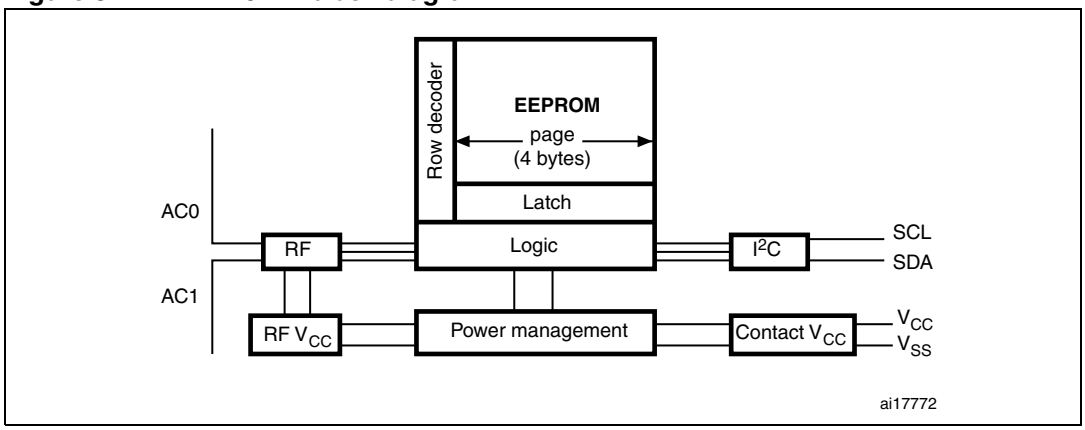
Figure 2 shows that the four mandatory pins for the I²C bus (V_{SS}, V_{CC}, SCL, SDA) are positioned likewise in the two devices.

AC0 and AC1 are connected to pin 2 and pin 3, respectively. They have to be next to each other for RF capability requirements. As a result, E1 was moved to pin 7 in the M24LR64-R, whereas it is connected to pin 2 in the M24C64.

1.2 Two ways of accessing the M24LR64-R: RF and I²C

Compared to the M24C64, the M24LR64-R has an additional capability: RF access, made possible by connecting the AC0 & AC1 pins to a tuned antenna. This modifies the block diagram of the M24LR64-R. *Figure 3* shows the new block diagram.

Figure 3. M24LR64-R block diagram



One difference between the M24LR64-R and the M24C64 is that the M24C64 can be accessed only through the I²C bus, whereas the M24LR64-R can be accessed through either the I²C bus or the RF interface.

Due to the M24LR64-R's dual access capability, a number of things have to be taken into account when accessing the device. If an RF request is made while an I²C communication is ongoing, it will not be served. Likewise, if an I²C request is made during an RF communication, it will not be served. This has to be taken into account in the system. A dedicated application note, AN3057, *explains "how to manage simultaneously I²C and RF data transfers with the M24LR64-R".*

2 Software considerations

Table 1 and *Table 2* show the device select codes of the M24LR64-R and M24C64, respectively. As explained earlier, the M24LR64-R does not offer the E2 pin. In the M24LR64-R's device select code, bit 3 is used to define access to EEPROM user data or system data:

- E2=0: User memory
- E2=1: System memory

Except for bit 3, the device select code is used in the same way for the two devices.

Table 1. M24LR64-R device select code

	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2(3)	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0 and E1 are compared to the respective external pins on the memory device.
3. E2 is not connected to any external pin. It is however used to address the M24LR64-R.

Table 2. M24C64 device select code

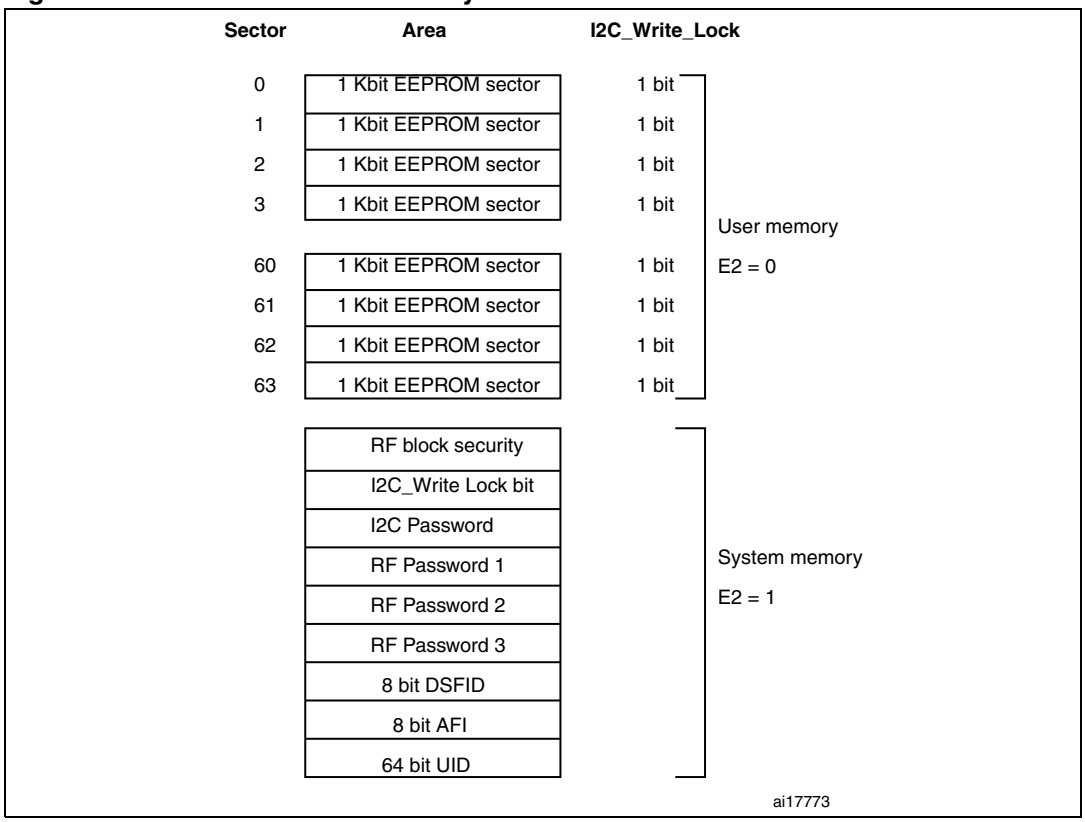
	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared to the respective external pins on the memory device.

3 M24LR64-R memory organization

Figure 4 shows the memory organization of the M24LR64-R.

Figure 4. M24LR64-R's user and system memories



3.1 User memory seen from the I²C bus (E2=0)

The M24LR64-R's user memory is a 64 Kbit EEPROM similar to the M24C64. To access the M24LR64-R's user memory area, E2 has to be reset to 0 in the device select byte.

3.1.1 Sectors

The M24LR64-R's user memory is organized as 32 sectors of 128 bytes each. The device has a feature specially added to write-protect sectors: each sector can be write-locked separately by setting the corresponding *I²C_Write_Lock bit*. When a sector is write-locked, the I²C password (see *Section 3.1.4: I²C Present Password*) has to be presented before the sector can be written.

3.1.2 Page Write

The page size of the M24LR64-R is 4 bytes, making it possible to write up to 4 bytes in a single write cycle.

With Page Write you can write up to 32 bytes to an M24C64 device in a single write cycle.

3.1.3 Read

The M24C64 and M24LR64-R are read identically (from the I²C bus).

3.1.4 I²C Present Password

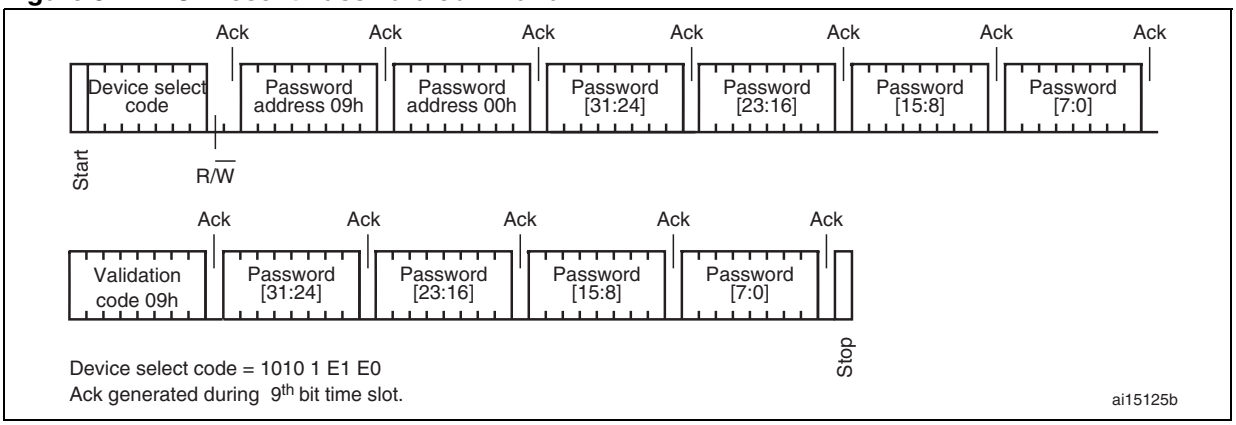
It is a command specific to the M24LR64-R. *Figure 5* shows the command sequence.

To write data to a locked sector or the system memory, the system has to present the correct password. This is done using the *I²C Present Password* command. With this command, you can:

- In User memory (see *Figure 4: M24LR64-R's user and system memories*):
  - write data to the write-protected sector(s)
- In System memory (see *Figure 4: M24LR64-R's user and system memories*):
  - modify each I²C_Write_Lock bit
  - modify each RF block Security bit
  - read the I²C password

The password is 32 bits long.

Figure 5. I²C Present Password command

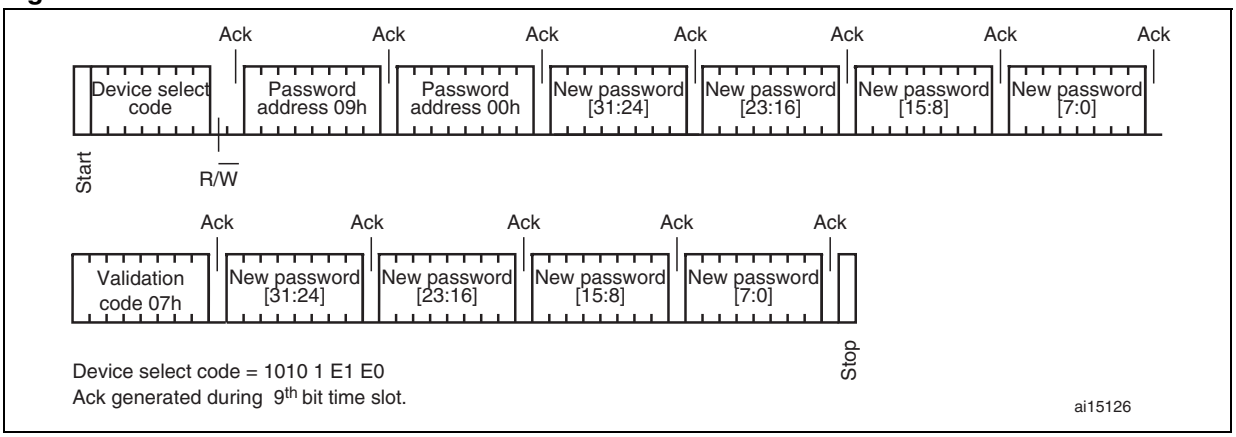


3.1.5 I²C Write Password

This command also is specific to the M24LR64-R. *Figure 6* shows the command sequence.

The *I²C Write Password* command is used to change the I²C password. It has to be preceded by a correct I²C Present Password sequence, otherwise it is not executed.

Figure 6. I²C Write Password command



3.2 System memory seen from the I²C bus (E2=1)

The M24LR64-R device offers an additional EEPROM memory area named the system memory (see *Figure 4: M24LR64-R's user and system memories*). The system memory can only be accessed in read or/and write mode through the I²C bus by setting the E2 bit to 1 in the device select byte.

3.2.1 M24LR64-R's RF block security status

The 64 bytes in the system memory store the RF block security status value of each RF sector (1 byte for 1 sector).

This RF block security status can be read from the I²C bus in order to verify the protection of the user memory, when accessed from the RF channel.

The data in the RF block security status can be erased or modified from the I²C bus only if the I²C password has been presented successfully.

Table 3. RF block security status

I²C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	0	SSS 3	SSS 2	SSS 1	SSS 0
E2 = 1	4	SSS 7	SSS 6	SSS 5	SSS 4
E2 = 1	8	SSS 11	SSS 10	SSS 9	SSS 8
E2 = 1	12	SSS 15	SSS 14	SSS 13	SSS 12
E2 = 1	16	SSS 19	SSS 18	SSS 17	SSS 16
E2 = 1	20	SSS 23	SSS 22	SSS 21	SSS 20
E2 = 1	24	SSS 27	SSS 26	SSS 25	SSS 24
E2 = 1	28	SSS 31	SSS 30	SSS 29	SSS 28
E2 = 1	32	SSS 35	SSS 34	SSS 33	SSS 32
E2 = 1	36	SSS 39	SSS 38	SSS 37	SSS 36
E2 = 1	40	SSS 43	SSS 42	SSS 41	SSS 40

Table 3. RF block security status (continued)

I²C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	44	SSS 47	SSS 46	SSS 45	SSS 44
E2 = 1	48	SSS 51	SSS 50	SSS 49	SSS 48
E2 = 1	52	SSS 55	SSS 54	SSS 53	SSS 52
E2 = 1	56	SSS 59	SSS 58	SSS 51	SSS 56
E2 = 1	60	SSS 63	SSS 62	SSS 61	SSS 60

3.2.2 I²C_Write_Lock bits

Eight bytes in the system memory area define the I²C_Write_Lock bit value of each sector in user memory (1 bit for 1 sector).

The I²C_Write_Lock bits can be read through the I²C bus to verify the protection of the user memory in RF mode.

The C_Write_Lock bits can be modified through the I²C bus only if the I²C password has been successfully presented.

Table 4. I2C_Write_Lock bits

I²C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
E2 = 1	2048	sectors 31-24	sectors 23-16	sectors 15-8	sectors 7-0
E2 = 1	2052	sectors 63-56	sectors 55-48	sectors 47-40	sectors 39-32

3.2.3 System parameters

The system parameters (in the system memory) are:

- I²C password
- three RF passwords
- DSFID
- AFI
- two RFU bytes
- eight UID bytes
- three Mem_Size bytes
- IC Ref

These parameters are read-only. *Table 5* shows there location in the system memory.

Table 5. System parameter sector

RF address	I^2C byte address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
-	E2 = 1	2304	I^2C password (default 0000 0000h)			
1	E2 = 1	2308	RF password 1 (default 0000 0000h)			
2	E2 = 1	2312	RF password 2 (default 0000 0000h)			
3	E2 = 1	2316	RF password 3 (default 0000 0000h)			
-	E2 = 1	2320	DSFID (FFh)	AFI (00h)	RFU (FFh)	RFU (FFh)
-	E2 = 1	2324	UID	UID	UID	UID
-	E2 = 1	2328	UID (E0h)	UID (02h)	UID	UID
-	E2 = 1	2332	Mem_Size (03 07FFh)			IC Ref (2Ch)

The RF passwords cannot be read (an I²C read operation to an RF password area sends back FFh data) or written through the I²C bus.

The I²C password can be read only if an I²C Present Password sequence was previously performed and the password matched. It is not possible to directly write the I²C password: to be able to modify the I²C password, the I²C Write Password command has to be used.

DSFID, AFI, RFU, UID, MemSize and I²C Ref are read-only data and cannot be modified from the I²C bus.

4 Revision history

Table 6. Document revision history

Date	Revision	Changes
08-Mar-2010	1	Initial release.

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