TB3133

Configurable Logic Cell on PIC® Microcontrollers

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INTRODUCTION

The Configurable Logic Cell (CLC) is an innovative peripheral that allows for the on-chip creation of custom logic functions for PIC® microcontrollers. The CLC provides programmable, combinational and sequential logic that operates independently of the CPU execution. The CLC can be used for interconnecting peripherals and designing general purpose logic, thus replacing the need for external circuitry.

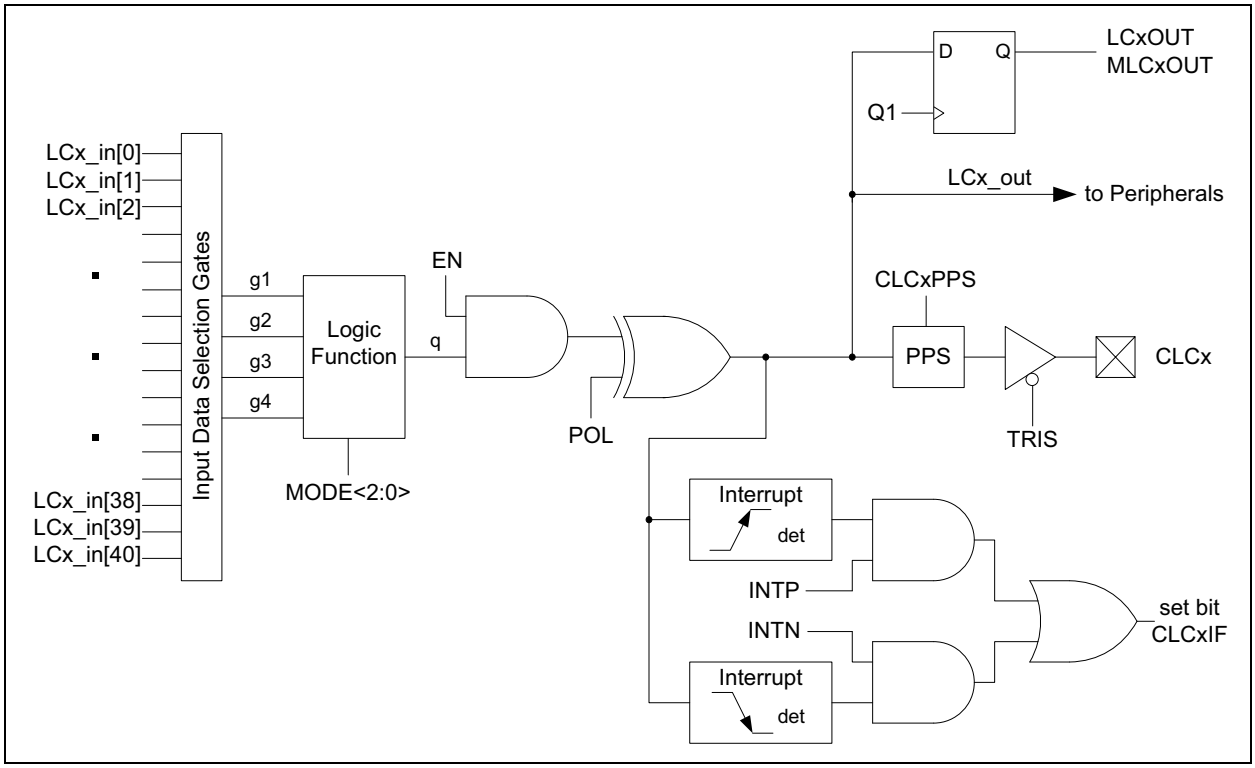
CONFIGURABLE LOGIC CELL (CLC) OVERVIEW

The CLC is user configurable similar to a Programmable Logic Device (PLD). The CLC can implement a variety of logic functions. A variety of inputs, internal and external, can be routed to this module. CLC receives inputs from other peripherals or from an input pin. It then performs the intended logic operation and provides output that can be used to control other peripherals or another I/O pin. Logic functions can be achieved via programming, using Special Function Registers associated with the peripheral. The CLC can be used to operate even when the microcontroller is in Sleep mode. CLC helps in simplifying on-chip interconnection of peripherals when it is configured. External glue logic functions on the PCB can be eliminated by using the CLC, thus reducing board space. In addition, the logic functions implemented using CLC also save code space.

The following four sections are used to configure the CLC module:

- Data Selection
- Data Gating
- Logic Function Selection
- Output Polarity

FIGURE 1: CONFIGURABLE LOGIC CELL BLOCK DIAGRAM



Data Selection

CLC receives a number of signals as inputs. Input sources are a combination of the following:

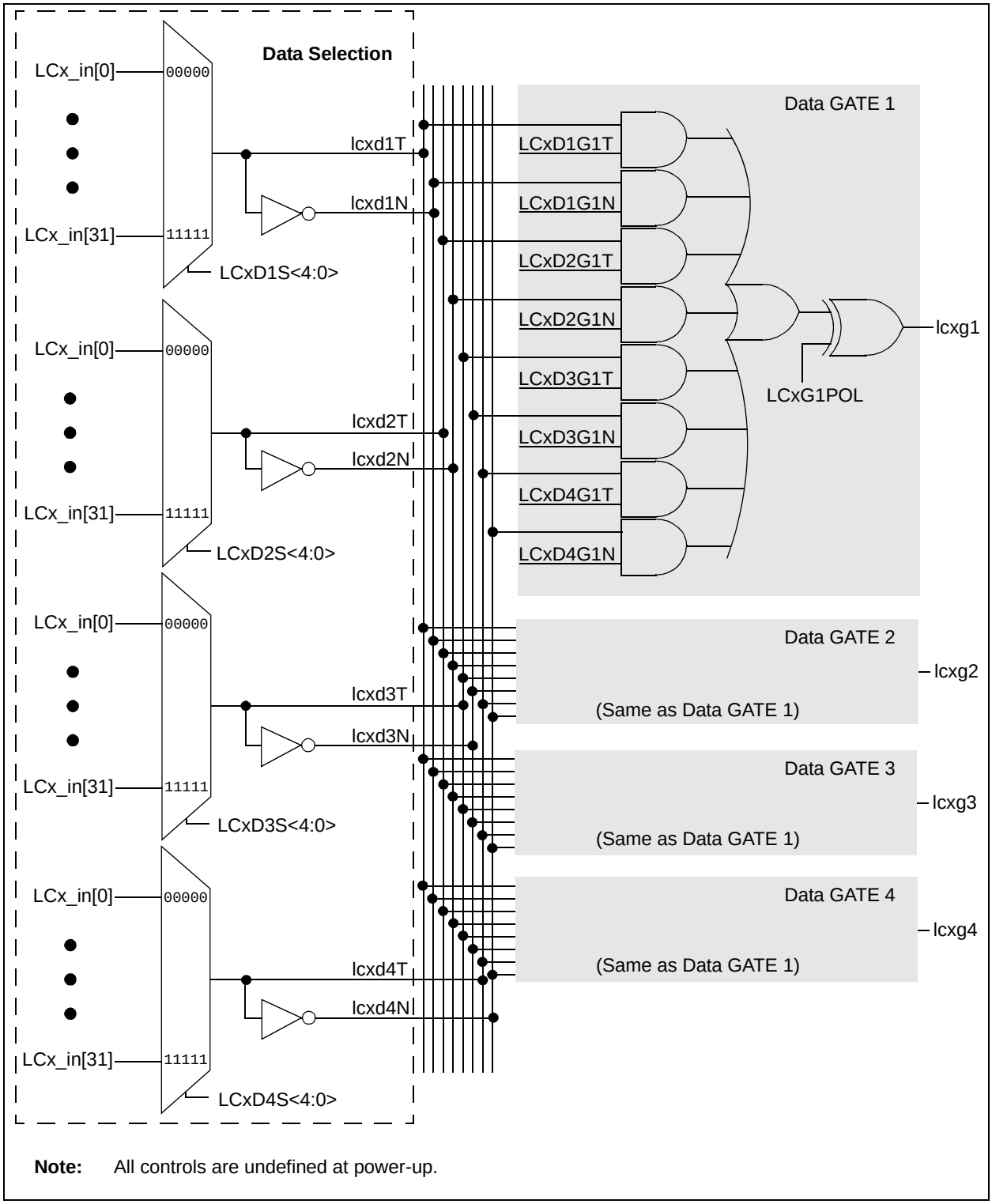
- I/O Pins
- Internal Clocks
- Peripherals
- Register Bits

Data selection is done through four multiplexers. Each multiplexer can have up to 32 inputs. The output of each of these multiplexers acts as an input to the logic functions. There are eight selectable single output logic functions to which the multiplexer outputs can be connected. The CLC input signals can be selected from the four registers, CLCxSEL0 through CLCxSEL3.

Data Gating

Output of the multiplexers from the input stage are directed to the desired logic function through the data-gating stage. Each data gate can direct any combination of the four multiplexer outputs. The data-gating stage can be used for directing the input signal and also for configuring the directed input as inverted or non-inverted data. Figure 2 displays the data-gating stage.

FIGURE 2: DATA SELECTION AND GATING STAGE



Note: All controls are undefined at power-up.

The output of the data selection stage provides both the true value and the negated value of the selected signal. It is at this stage that the user decides whether the true or the negated value of the signal is needed for the next stage. Each input to the data-gating section has a pair of bits in its respective CLCxGLSx register. The two bits include a non-inverted bit 'T' and an inverted bit 'N' that needs to be set up. If the 'N' bit is set, then the negated input is selected. The selected (true or negated) signals are ORed to form the data gate output. The CLCxPOL register bit, LCxGxPOL, will invert or non-invert the output of the gate.

Logic Function Selection

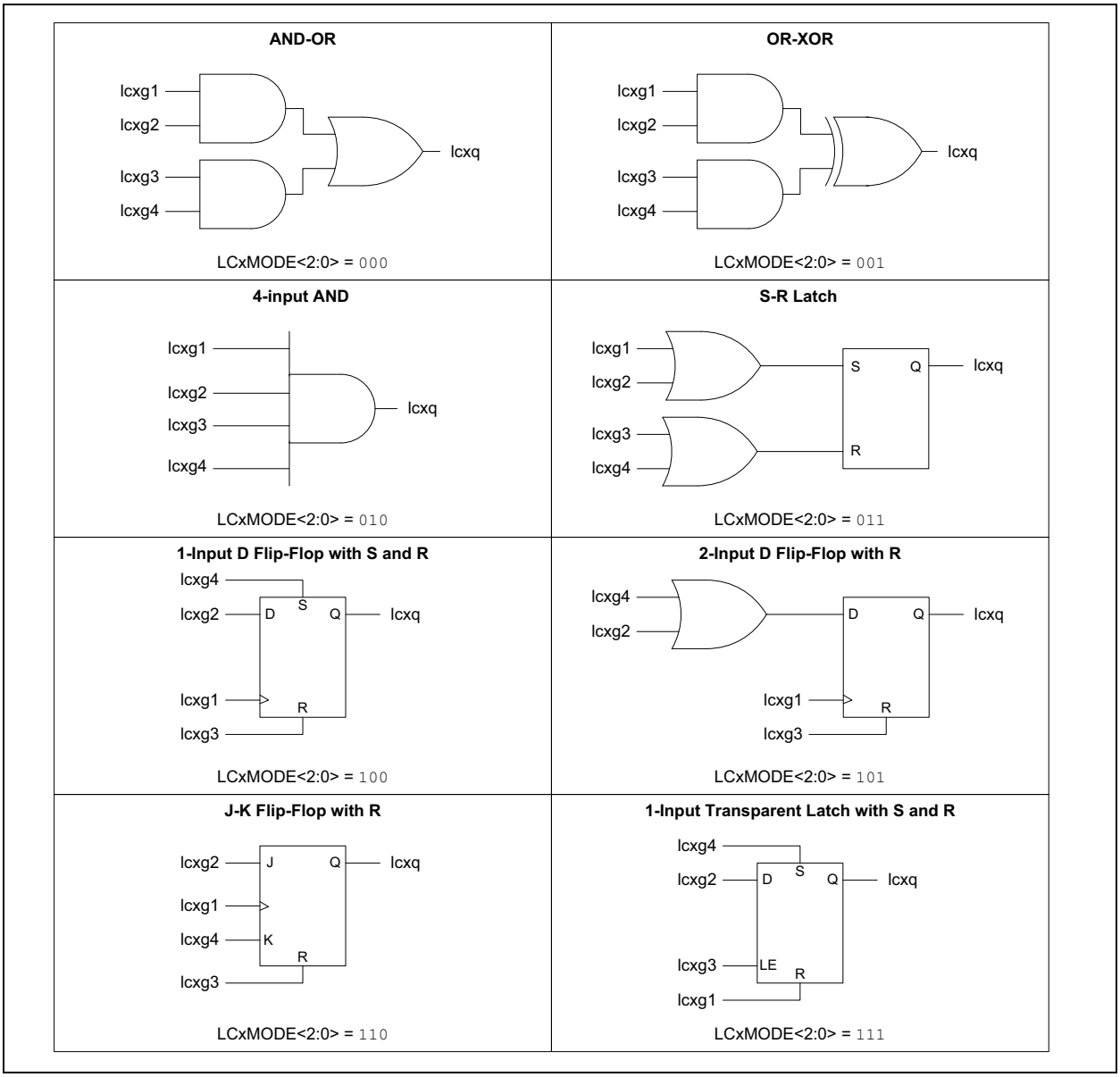
The outputs of the data-gating stage are inputs to the logic function selection stage. The four inputs are reduced to one output which can further be used as an input to any other peripheral or to drive an output pin. The desired logic function is selected with the LCMODE<2:0> bits of the CLCxCON register.

There are eight available logic functions:

- AND-OR (LCMODE<2:0>= 000)
- OR-XOR (LCMODE<2:0>= 001)
- AND (LCMODE<2:0>= 010)
- S-R Latch (LCMODE<2:0>= 011)
- D Flip-Flop with Set and Reset (LCMODE<2:0>= 100)
- D Flip-Flop with Reset (LCMODE<2:0>= 101)
- J-K Flip-Flop with Reset (LCMODE<2:0>= 110)
- Transparent Latch with Set and Reset (LCMODE<2:0>= 111)

Figure 3 shows the different programmable logic functions.

FIGURE 3: PROGRAMMABLE LOGIC FUNCTIONS



Output Polarity

The output polarity stage is the last stage in a CLC. We can select the desired polarity of the logic output with the LCxPOL bit of the CLCxCON register.

CONFIGURATION OF THE CLC PERIPHERAL

Operation of the peripheral is controlled by the following registers:

- CLCxCON: It is used to enable the module and, more importantly, to select the logic function
- CLCxPOL: It is used to control the logic polarity of both the cell output and the intermediate variables
- CLCxSELx: The inputs are selected by the LCxDxS<5:0> bits in this register. There might be up to four data select registers.
- CLCxGLSx: This register allows the user to form an input to the logic function stage from an OR or AND of the data bus signals derived from the data selection stage. Either the true or negated values of each data signal can be chosen.

Table 1 contains the summary of registers associated with the CLC.

TABLE 1: REGISTERS ASSOCIATED WITH CLC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLCxCON	LCxEN	LCxOE	LCxOUT	LCxINTP	LCxINTN	LCxMODE<2:0>		
CLCxPOL	LCxPOL	—	—	—	LCxG4POL	LCxG3POL	LCxG2POL	LCxG1POL
CLCxSEL0	—	—	LCxD1S<5:0>					
CLCxSEL1	—	—	LCxD2S<5:0>					
CLCxSEL2	—	—	LCxD3S<5:0>					
CLCxSEL3	—	—	LCxD4S<5:0>					
CLCxGLS0	LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N
CLCxGLS1	LC1G2D4T	LC1G2D4N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N
CLCxGLS2	LC1G3D4T	LC1G3D4N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N
CLCxGLS3	LC1G4D4T	LC1G4D4N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N

Example 1 is the code snippet used to demonstrate the ANDing of two signals using the CLC.

EXAMPLE 1: CODE SNIPPET FOR ANDING TWO SIGNALS USING THE CLC

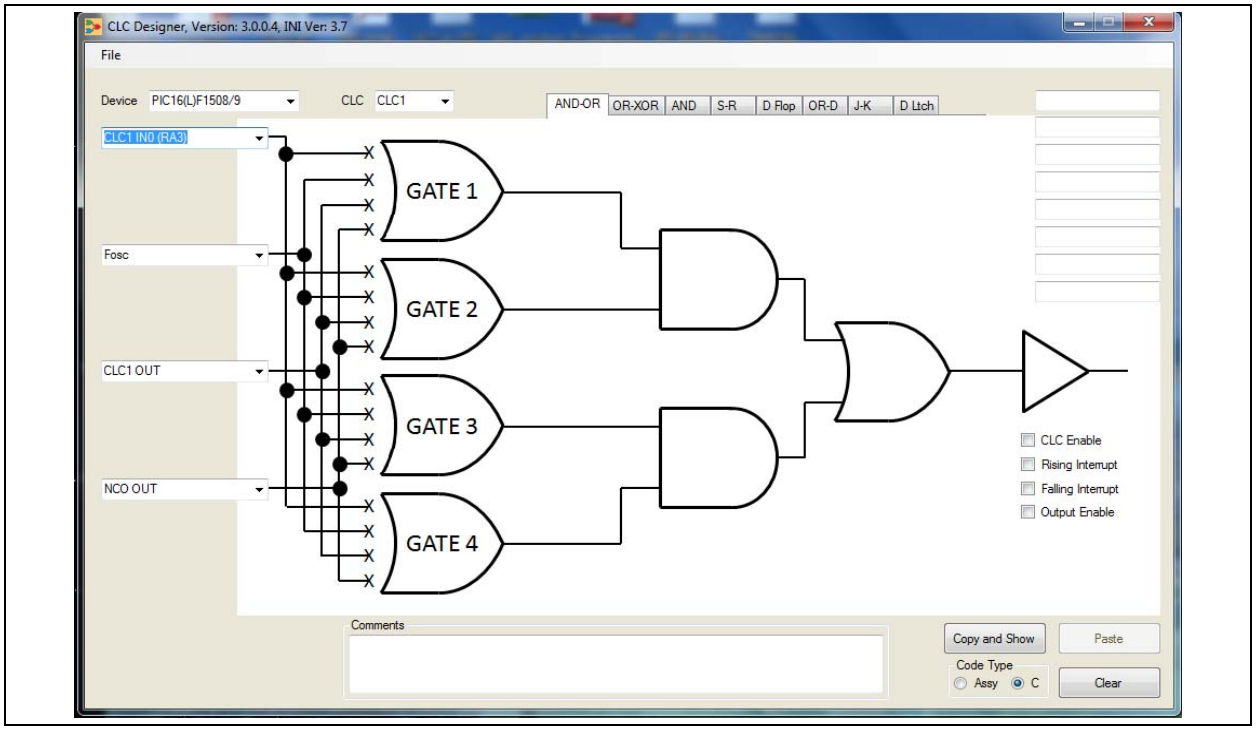
```
//CLC Setup
CLC1POL  = 0x00;//Output of the logic cell is not inverted
CLC1SEL0 = 0x06;//Input Data selection 0
CLC1SEL1 = 0x0C;//Input Data selection 1
CLC1SEL2 = 0x04;//Input Data selection 2
CLC1SEL3 = 0x06;//Input Data selection 3
CLC1GLS0 = 0x02;//Input 1 is not inverted
CLC1GLS1 = 0x20;//Input 2 is inverted
CLC1GLS2 = 0xAA;//Input 3 is not inverted
CLC1GLS3 = 0x80;//Input 4 is not inverted
CLC1CON  = 0x80;//CLC enabled; MODE AND-OR
```

CLC Configuration Tool and MPLAB® Code Configurator for CLC

Configuration of the CLC module can be easily done with the help of the GUI-based tools, which help the user visualize the CLC structure and generate the code for the settings. The CLC configuration tool and the MPLAB® Code Configurator are the tools that help in streamlining the setup process of the CLC module and simulate the register settings in a graphical user interface.

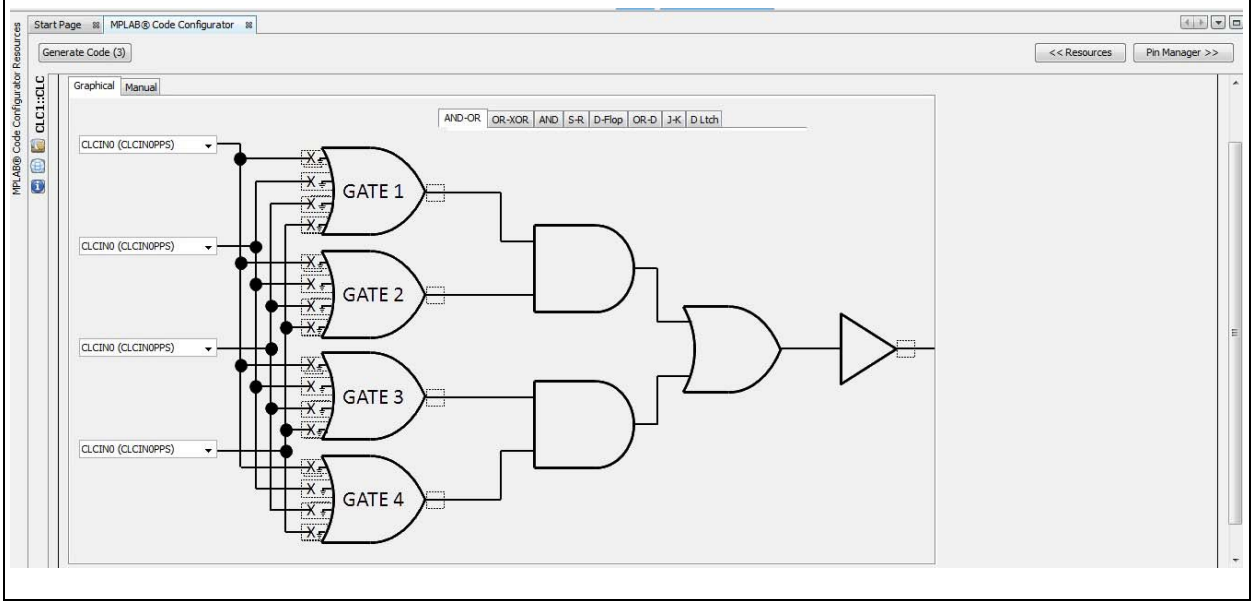
The CLC configuration tool generates the source code either in C or Assembly, which can be incorporated into the existing MPLAB® X project. Figure 4 shows the CLC configuration tool GUI. For further details refer to the "*Configurable Logic Cell (CLC) Configuration Tool User's Guide*"(DS41597).

FIGURE 4: CLC CONFIGURATION TOOL GUI



The MPLAB Code Configurator, which is a plug-in tool for MPLAB X IDE, generates the drivers based on the settings and selections made in the GUI. MCC incorporates the CLC configuration tool and it outputs only C code. Figure 5 shows the MPLAB Code Configurator GUI.

FIGURE 5: MPLAB® CODE CONFIGURATOR (MCC) FOR CONFIGURABLE LOGIC CELL



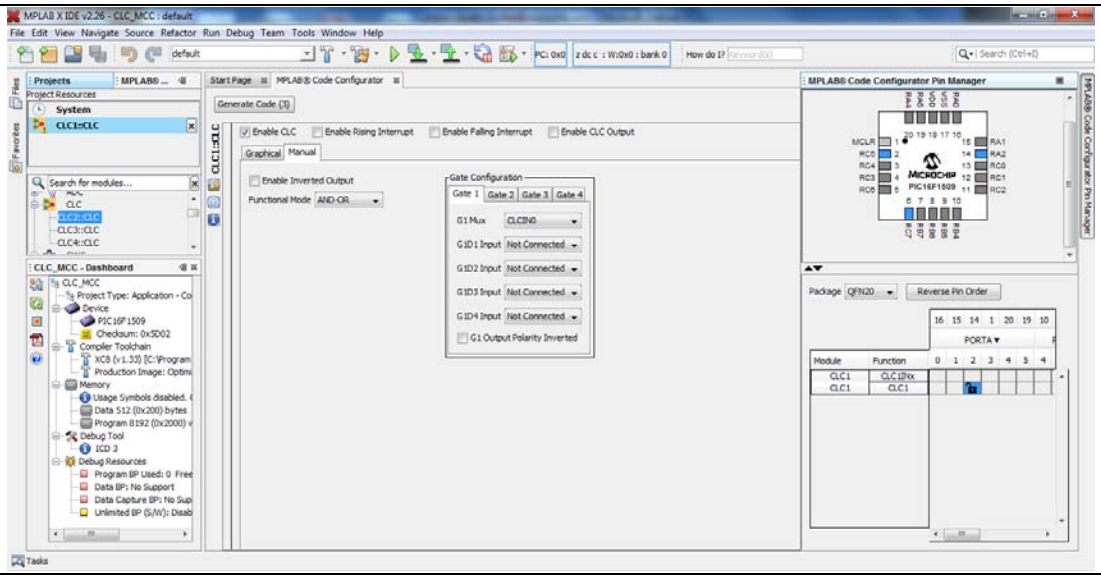
The composer area for the CLC has two tabs:

- Graphical
- Manual

In the Graphical tab (see Figure 5), the user can visualize the CLC structure and do the setup.

In the Manual tab (see Figure 6), the same settings can be done in the drop-down feature to configure all the Special Function Registers of the CLC. The tool generates the driver for the settings provided by the user. For further details refer to the "*MPLAB® Code Configurator User's Guide*" (DS40001725).

FIGURE 6: MANUAL TAB IN MPLAB® CODE CONFIGURATOR (MCC) FOR CONFIGURABLE LOGIC CELL



CLC API List

The following API is generated by MCC for the CLC module:

- `void CLC1_Initialize(void)`: This API initializes the CLCxCON, CLCxPOL, CLCxGLSx and CLCxSELx registers

CONCLUSION

Realization of various digital logic functions such as basic gates, flip-flops and latches can be achieved using the CLC peripheral on PIC microcontrollers. CLC offers the advantage of designing these logic functions on-chip, thereby eliminating a lot of additional circuitry on the board. In addition, many of the logic functions used for Fault activation, decision making and event handling that are conventionally done in software can easily be achieved using the CLC. This technical brief aims at familiarizing the reader with the functionality of the CLC and how programmable combinational and sequential logic can be achieved without intervention of the CPU. More details are available on the device-specific data sheet.

REFERENCES

1. *Configurable Logic Cell (CLC) Configuration Tool User's Guide* (DS41597)
2. *Configurable Logic Cell Tips'n Tricks* (DS41631)
3. *MPLAB® Code Configurator User's Guide* (DS40001725)

APPENDIX A: APPLICATIONS OF THE CONFIGURABLE LOGIC CELL

A.1 Servo Pulse Measurement Circuit

The pulse width of a periodic signal, such as that of a servo control signal, can be measured using the CLC along with other peripherals such as a Numerically Controlled Oscillator (NCO) and Timer0 on PIC microcontrollers (see Figure A-1). In the circuit exemplified in Figure A-1, Timer0 is used as an 8-bit counter. This circuit captures a pulse from the pulse stream and provides a measurement count. The NCO output is used as a clock for the 8-bit counter. An RC receiver typically generates servo control pulses of varying width every 20 ms. The width of the pulse is between 1 to 2 ms.

The NCO frequency is selected as 200 kHz. The circuit is reset by presetting the counter to 56 and strobing the Gate 3 Pol bits high. The rising edge of the pulse sets Q1 and the falling edge sets Q2. When Q1 is high and Q2 is low, the counter counts at the NCO frequency. The operation is illustrated in the waveform in Figure A-2. At 1 ms the counter rolls from 255 to 0, and at 2 ms the count is 200. Pulse is ready to be read when Q2 goes high. The count is held until the circuit is reset to capture another pulse. The circuit is reset to capture another pulse. CLC3 input from the CLC2 Q output synchronizes the pulse measurement after the asynchronous Reset.

FIGURE A-1: SERVO PULSE MEASUREMENT CIRCUIT USING THE CLC

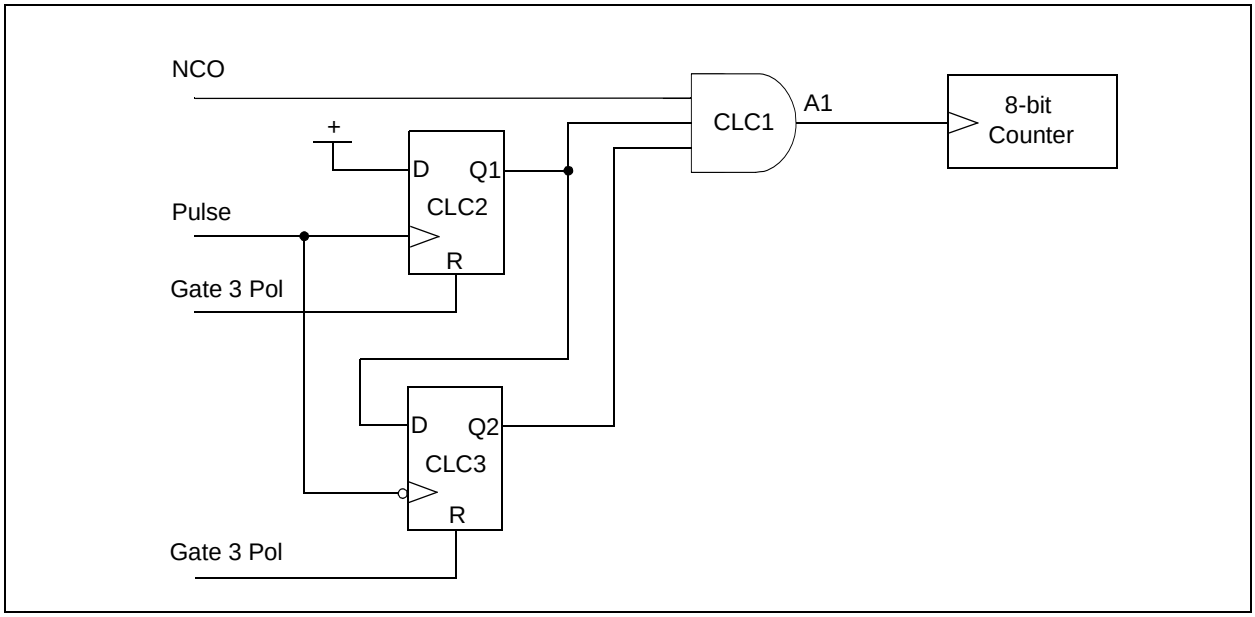
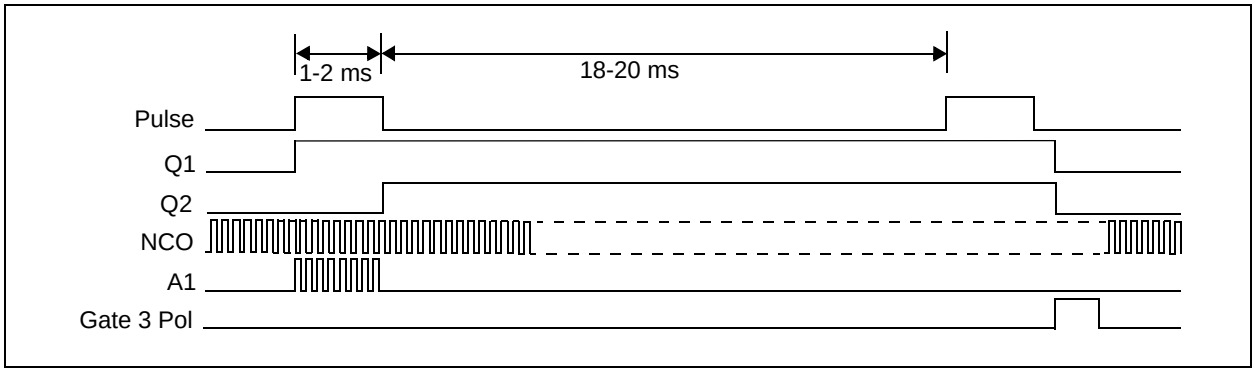


FIGURE A-2: TIMING DIAGRAM OF THE SERVO PULSE MEASUREMENT CIRCUIT

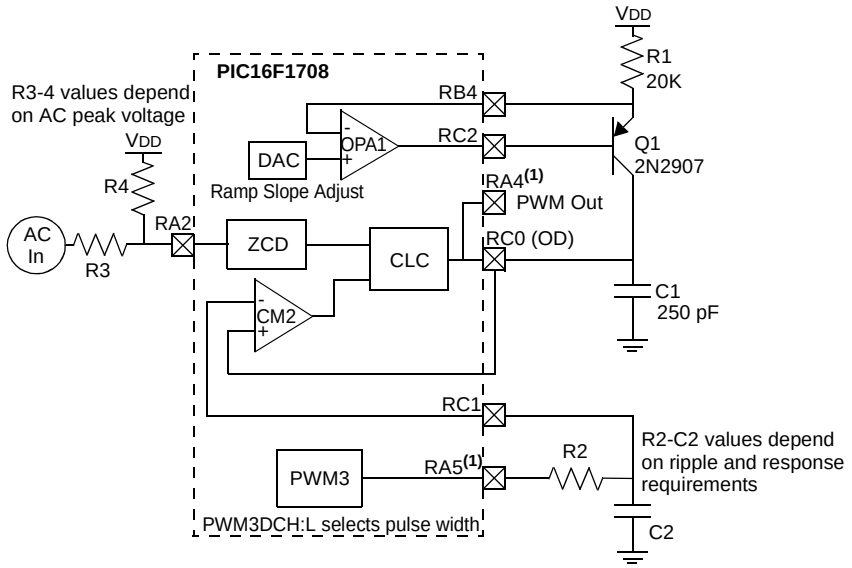


A.2 10-Bit PWM Synchronous with AC Input

The PWM output can be made synchronous with the AC input with the help of on-chip peripherals such as the CLC, Zero-Cross Detect (ZCD) and comparator (CM2). In the circuit illustrated in Figure A-3, the CLC block consists of two CLC instances (CLC1 and CLC2). CLC1 is implemented as an XOR gate of the CLC2 and ZCD outputs. The CLC2 output is implemented as a D flip-flop, with ZCD output at the D input, and the comparator output rising edge at clock input. A ZCD change triggers CLC1 output to go high. When CLC1 becomes high, it enables the constant-current charge of C1 through the open-drain configuration of RC0. When C1 voltage reaches the voltage on C2, CM2 triggers CLC2 to the same level as the ZCD output, thereby forcing CLC1 output low. CLC1 low output discharges C1 through RC0 open-drain output until the next ZCD change. C2 voltage is set by the PWM3 duty cycle. Figure A-4 illustrates the timing diagram of the circuit.

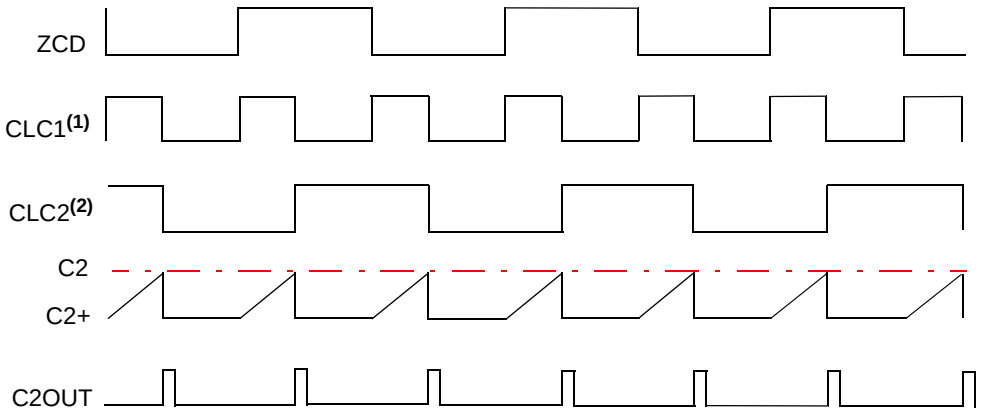
OPA1, R1 and Q1 form a constant-current source for the linear charge of C1. DAC is the current source adjustment to match the C1 voltage ramp to the AC input half cycle.

FIGURE A-3: CIRCUIT FOR MAKING PWM SYNCHRONOUS WITH AC INPUT



Note 1: Pin selected with PPS control.

FIGURE A-4: TIMING DIAGRAM OF THE CIRCUIT



Note 1: CLC1 = ZCD + CLC2

2: CLC2 = ZCD at C2OUT rising edge (D-flop with ZCD on D input and CM2 on clock input)

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