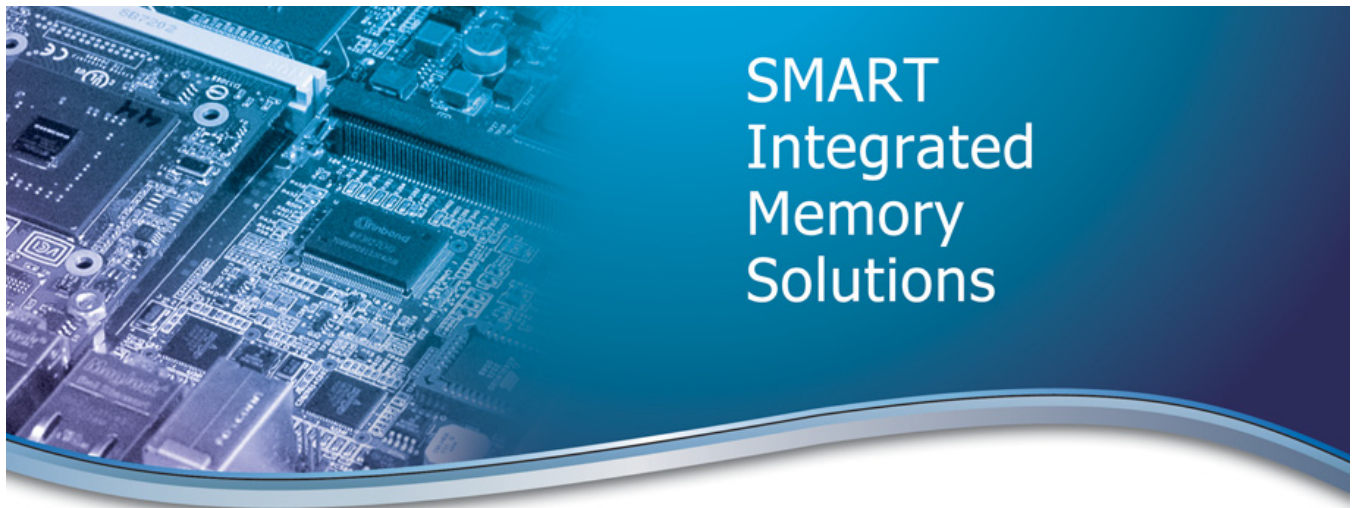




# SMART Integrated Memory Solutions

## Product Specification

### **SMART Modular eMMC v4.51+ Product Family**

March 2015, Rev B



[www.smartm.com](http://www.smartm.com)

## REVISION HISTORY

| Date        | Revision | Section(s) | Description                                            |
|-------------|----------|------------|--------------------------------------------------------|
| August 2014 | A        | All        | Initial production release.                            |
| March 2015  | B        | 5          | Added information for parts with version 2 of firmware |



### ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

This document is subject to change without notice.

### SMART Modular Technologies

39870 Eureka Dr.  
Newark, CA 94560  
(510) 623-1231 voice  
(510) 623-1434 fax  
info@smartm.com  
An ISO 9001 certified company.

## TABLE OF CONTENTS

|                                                |          |                                           |           |
|------------------------------------------------|----------|-------------------------------------------|-----------|
| <b>1.0 General Description . . . . .</b>       | <b>2</b> | <b>3.0 DC Specifications . . . . .</b>    | <b>13</b> |
| 1.1 Overview . . . . .                         | 2        | 3.0 DC Specifications . . . . .           | 13        |
| 1.2 Features . . . . .                         | 3        | 3.1 Operational Characteristics . . . . . | 15        |
| 1.3 MMC-Specific Features . . . . .            | 3        | 3.1.1 Current Consumption . . . . .       | 15        |
| 1.4 Performance . . . . .                      | 4        | <b>4.0 Registers . . . . .</b>            | <b>16</b> |
| <b>2.0 Package Information . . . . .</b>       | <b>5</b> | 4.1 CID Register . . . . .                | 16        |
| 2.1 Electrical Interface . . . . .             | 5        | 4.2 OCR Register . . . . .                | 17        |
| 2.1.1 100-Ball eMMC Ball-out Diagram . . . . . | 5        | 4.3 CSD Register . . . . .                | 18        |
| 2.1.2 169-Ball eMMC Ball-out Diagram . . . . . | 6        | 4.4 ECSD Register . . . . .               | 20        |
| 2.1.3 Signal Descriptions . . . . .            | 7        | <b>5.0 Part Numbers . . . . .</b>         | <b>27</b> |
| 2.2 eMMC Dimensions . . . . .                  | 8        | 5.1 Part Number Decoder . . . . .         | 27        |
| 2.2.1 100-Ball Package Dimensions . . . . .    | 8        | 5.2 Part Number Decoder . . . . .         | 28        |
| 2.2.2 169-Ball Package Dimensions . . . . .    | 9        | 5.3 Part Numbering Information . . . . .  | 28        |

## 1.0 GENERAL DESCRIPTION

### 1.1 Overview

SMART Modular's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed for applications requiring reliable code and data storage. The eMMC device includes NAND Flash Memory paired with an intelligent embedded MMC controller which runs advanced firmware to manage the NAND media and utilizes the industry standard eMMC interface for easy device integration into any system using a processor with an MMC host.

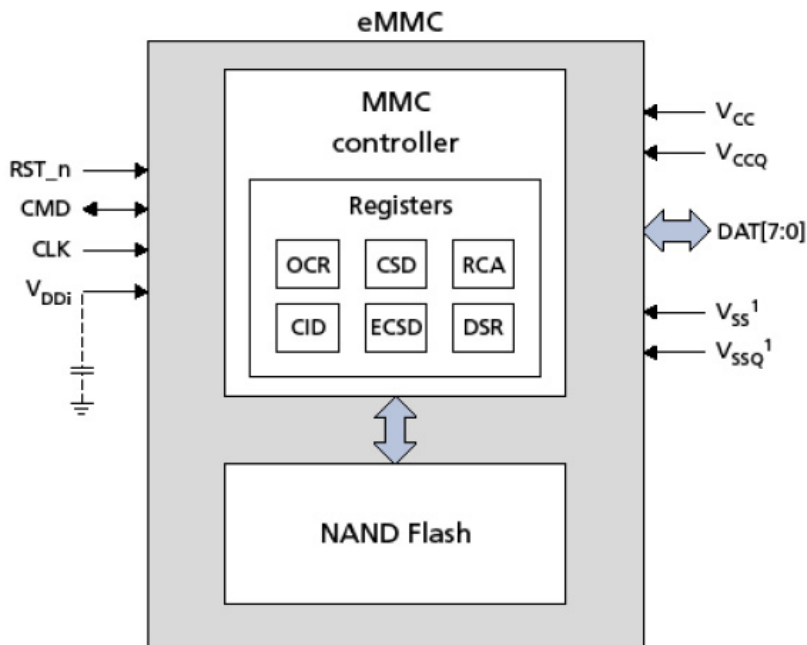
Designed specifically for the most demanding embedded and industrial applications, SMART's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, static and dynamic wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

SMART has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMART engineers its products to perform at the highest degree of reliability and compatibility while backing these products with outstanding services and technology expertise.

Target applications for SMART's eMMC solution include but are not limited to Automotive Infotainment and Navigation, Industrial systems, Medical devices, and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

Figure 1: eMMC Block Diagram



Note: 1. V<sub>SS</sub> and V<sub>SSQ</sub> are internally connected.

## 1.2 Features

- eMMC controller and NAND Flash
- Mechanical Form Factor: Fully compliant with JEDEC® MO-304 (100-Ball) or MO-276 (169-Ball)
- $V_{CC}$ : 2.7-3.6V
- $V_{CCQ}$  (dual voltage): 1.7-1.95V or 2.7-3.6V
- Temperature ranges
  - ◆ Operating temperature: -40°C to +85°C or -25°C to +85°C
  - ◆ Storage temperature: -40°C to +85°C

## 1.3 MMC-Specific Features

- JEDEC/MMC standard version 4.51-compliant (JEDEC Standard No. JESD84-B451) with additional firmware features included from version 5.01 (JEDEC Standard No. JESD84-B50-1)
  - NOTE: **HS400 Mode is NOT supported**
- Backward-compatible with previous MMC versions
- Advanced 11-signal interface
- Selectable x1, x4, and x8 I/O
- HS200 Mode
- SDR/DDR modes up to 52 MHz clock speed
- Replay-Protected Memory Block (RPMB)
- Hardware reset
- High-Priority Interrupt (HPI)
- Background operations
- Reliable Write
- Discard and Sanitize
- Packed Commands
- Secure Erase and Secure Trim support
- Field Firmware Update (FFU)

Note: Please refer to JEDEC standard documents No. JESD84-B451 and No. JESD84-B50-1 for details on all eMMC commands and features.

## 1.4 Performance

All listed values are typical unless otherwise stated.

**Table 1:** MLC Partition Performance

| Performance <sup>1</sup>      |       | 8GB  | 16GB | 32GB | Units |
|-------------------------------|-------|------|------|------|-------|
| Sequential Read <sup>2</sup>  | DDR52 | 90   | 90   | 90   | MB/s  |
|                               | HS200 | 90   | 160  | 160  | MB/s  |
| Sequential Write <sup>2</sup> | DDR52 | 12   | 24   | 48   | MB/s  |
|                               | HS200 | 12   | 24   | 48   | MB/s  |
| Random Read <sup>3</sup>      | DDR52 | 5800 | 7000 | 7100 | IOPS  |
|                               | HS200 | 6000 | 7200 | 7200 | IOPS  |
| Random Write <sup>4</sup>     | DDR52 | 1500 | 2000 | 2000 | IOPS  |
|                               | HS200 | 1500 | 2000 | 2100 | IOPS  |

<sup>1</sup> Testmetrix VTESA-3100E; bus in x8 I/O mode.

<sup>2</sup> Sequential access measured using 1GB chunk.

<sup>3</sup> Random Read measured using 4KB chunk after full-card sequential write operation (pre-conditioning).

<sup>4</sup> Random Write measured using 4KB chunk after full-card sequential write operation (pre-conditioning).

**Table 2:** Enhanced User Data Partition Performance

| Performance <sup>1</sup>      |       | 8GB  | 16GB | 32GB | Units |
|-------------------------------|-------|------|------|------|-------|
| Sequential Read <sup>2</sup>  | DDR52 | 90   | 90   | 90   | MB/s  |
|                               | HS200 | 90   | 170  | 170  | MB/s  |
| Sequential Write <sup>2</sup> | DDR52 | 33   | 62   | 71   | MB/s  |
|                               | HS200 | 33   | 65   | 109  | MB/s  |
| Random Read <sup>3</sup>      | DDR52 | 7100 | 7100 | 7100 | IOPS  |
|                               | HS200 | 7400 | 7200 | 7200 | IOPS  |
| Random Write <sup>4</sup>     | DDR52 | 1800 | 2000 | 2100 | IOPS  |
|                               | HS200 | 1800 | 2000 | 2200 | IOPS  |

<sup>1</sup> Testmetrix VTESA-3100E; bus in x8 I/O mode.

<sup>2</sup> Sequential access measured using 1GB chunk.

<sup>3</sup> Random Read measured using 4KB chunk after full-card sequential write operation (pre-conditioning).

<sup>4</sup> Random Write measured using 4KB chunk after full-card sequential write operation (pre-conditioning).

## 2.0 PACKAGE INFORMATION

### 2.1 Electrical Interface

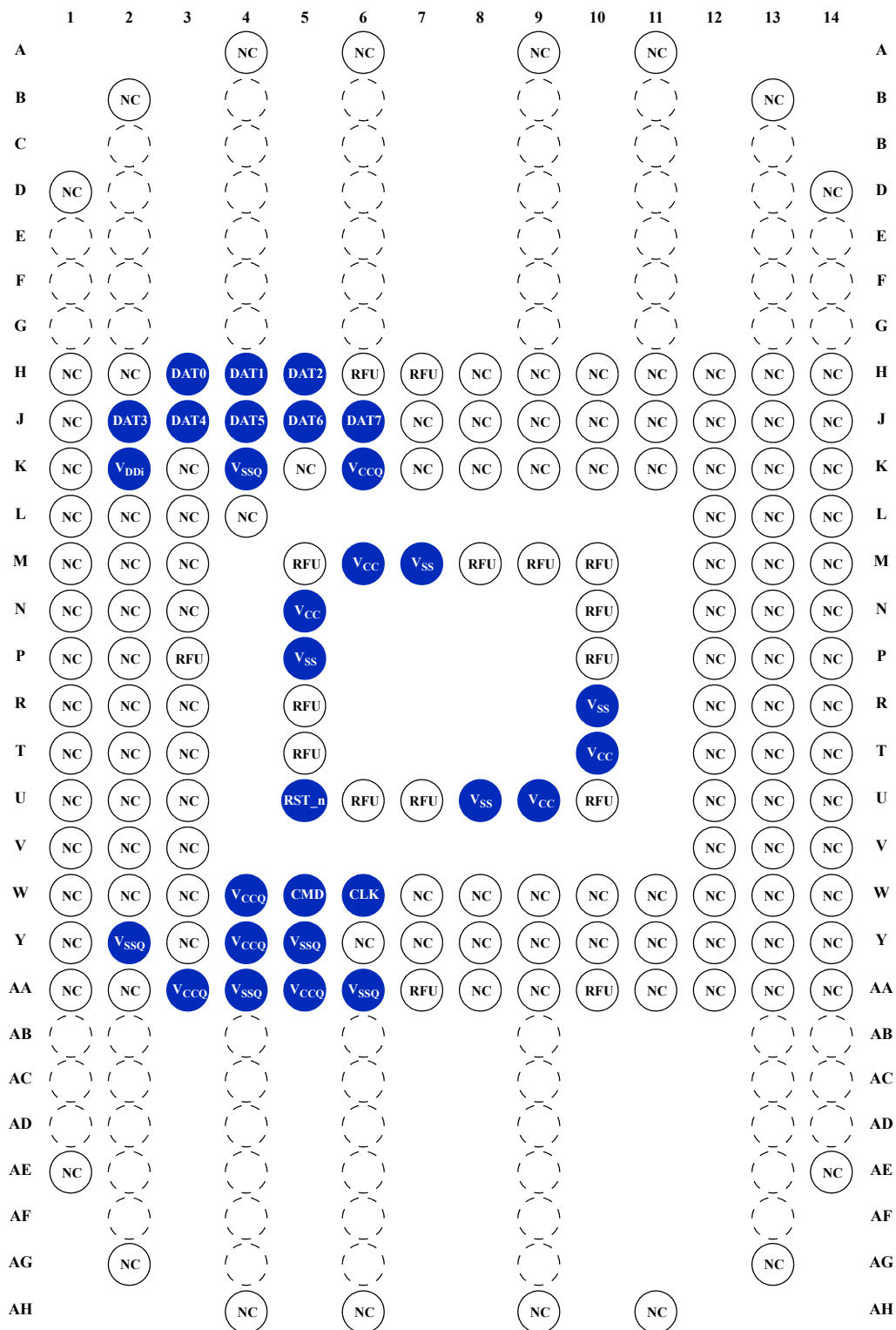
#### 2.1.1 100-Ball eMMC Ball-out Diagram

**Table 3:** 100-Ball LFBGA (Package Code: AE) (Top View, Ball Down)

|   | 1  | 2                | 3                | 4                | 5               | 6               | 7                | 8                | 9                | 10 |   |
|---|----|------------------|------------------|------------------|-----------------|-----------------|------------------|------------------|------------------|----|---|
| A | NC | NC               |                  |                  |                 |                 |                  |                  | NC               | NC | A |
| B | NC |                  |                  |                  |                 |                 |                  |                  |                  | NC | B |
| C |    |                  |                  |                  |                 |                 |                  |                  |                  |    | C |
| D |    | RFU              | RFU              | RFU              | RFU             | RFU             | RFU              | RFU              | RFU              |    | D |
| E |    | RFU              | RFU              | V <sub>DDi</sub> | RFU             | RFU             | RFU              | RFU              | RFU              |    | E |
| F |    | V <sub>CC</sub>  | V <sub>CC</sub>  | V <sub>CC</sub>  | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>CC</sub>  | V <sub>CC</sub>  | V <sub>CC</sub>  |    | F |
| G |    | V <sub>SS</sub>  | V <sub>SS</sub>  | V <sub>SS</sub>  | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>  | V <sub>SS</sub>  | V <sub>SS</sub>  |    | G |
| H |    | V <sub>SSQ</sub> | V <sub>CCQ</sub> | RFU              | RFU             | RFU             | RFU              | V <sub>CCQ</sub> | V <sub>SSQ</sub> |    | H |
| J |    | RFU              | RFU              | RFU              | RFU             | RFU             | RFU              | RFU              | RFU              |    | J |
| K |    | DAT0             | DAT2             | RFU              | RFU             | RFU             | RFU              | DAT5             | DAT7             |    | K |
| L |    | V <sub>CCQ</sub> | V <sub>SSQ</sub> | V <sub>CCQ</sub> | RFU             | RFU             | V <sub>CCQ</sub> | V <sub>SSQ</sub> | V <sub>CCQ</sub> |    | L |
| M |    | RFU              | RFU              | V <sub>SSQ</sub> | RST_n           | RFU             | V <sub>SSQ</sub> | RFU              | RFU              |    | M |
| N |    | DAT1             | DAT3             | RFU              | RFU             | RFU             | RFU              | DAT4             | DAT6             |    | N |
| P |    | V <sub>SSQ</sub> | V <sub>CCQ</sub> | RFU              | CMD             | CLK             | RFU              | V <sub>CCQ</sub> | V <sub>SSQ</sub> |    | P |
| R |    |                  |                  |                  |                 |                 |                  |                  |                  |    | R |
| T | NC |                  |                  |                  |                 |                 |                  |                  |                  | NC | T |
| U | NC | NC               |                  |                  |                 |                 |                  |                  | NC               | NC | U |

## 2.1.2 169-Ball eMMC Ball-out Diagram

**Table 4:** 169-Ball VFBGA / TFBGA / LFBGA (Package Code: CA / CC / CE) (Top View, Ball Down)



### 2.1.3 Signal Descriptions

**Table 5:** Signal Description

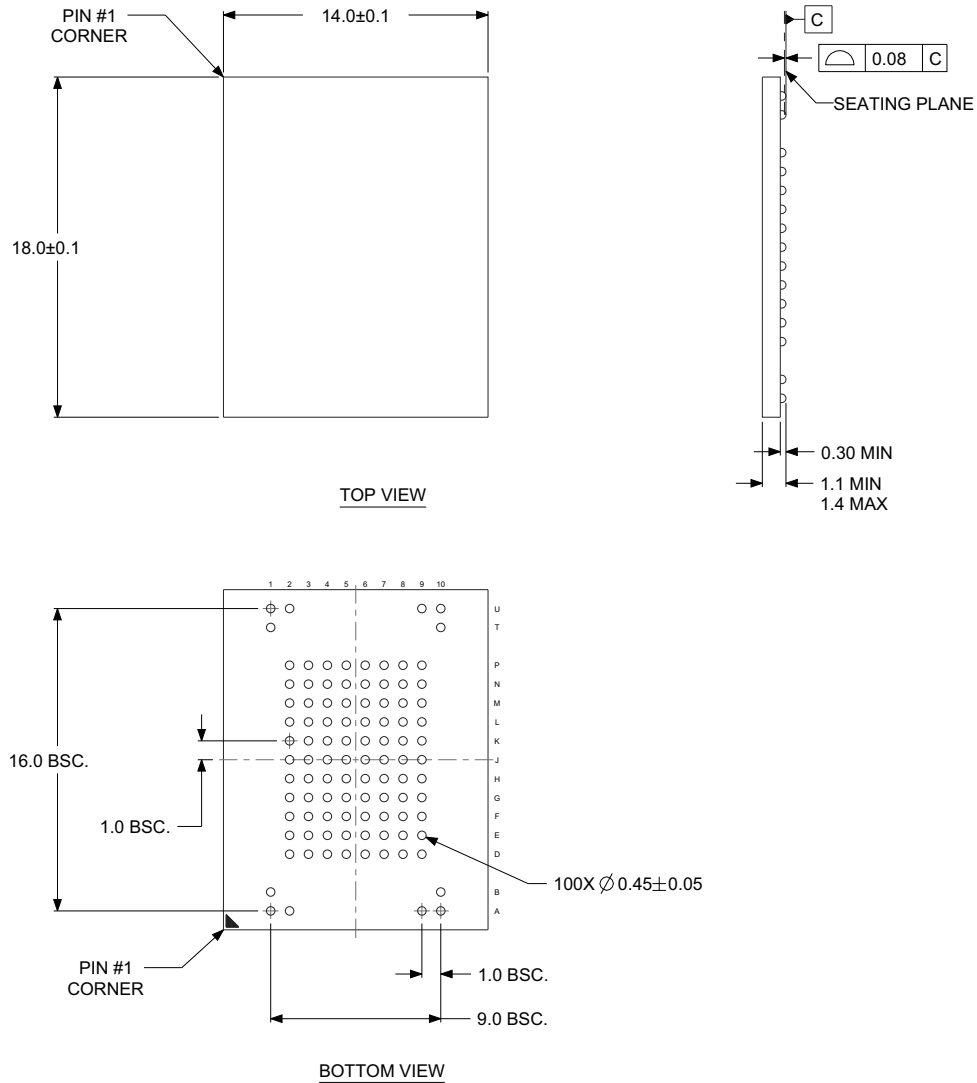
| Symbol                        | Type   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK                           | Input  | Clock: Each cycle of this signal directs a transfer on the command line and on the data lines. The frequency can vary between the minimum and the maximum clock frequency.                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| RST_n                         | Input  | Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it.                                                                                                                                                                                                                                                                                                                    |
| CMD                           | I/O    | Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain mode and push-pull. Commands are sent from the eMMC host controller to the eMMC device and responses are sent from the device to the host.                                                                                                                                                                                                                                                                                                            |
| DAT[7:0]                      | I/O    | Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). eMMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines. |
| V <sub>CC</sub>               | Supply | V <sub>CC</sub> : NAND interface (I/F) I/O and NAND Flash power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| V <sub>CCQ</sub>              | Supply | V <sub>CCQ</sub> : eMMC controller core and eMMC I/F I/O power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| V <sub>SS</sub> <sup>1</sup>  | Supply | V <sub>SS</sub> : NAND I/F I/O and NAND Flash ground connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| V <sub>SSQ</sub> <sup>1</sup> | Supply | V <sub>SSQ</sub> : eMMC controller core and eMMC I/F ground connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| V <sub>DDi</sub>              |        | Internal voltage node: At least a 0.1μF capacitor is required to connect V <sub>DDi</sub> to ground. A 1μF capacitor is recommended. Do not tie to supply voltage or ground.                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| NC                            | -      | No connect: No internal connection is present.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RFU                           | -      | Reserved for future use: No internal connection is present. Leave it floating externally.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

<sup>1</sup> V<sub>SS</sub> and V<sub>SSQ</sub> are connected internally.

## 2.2 eMMC Dimensions

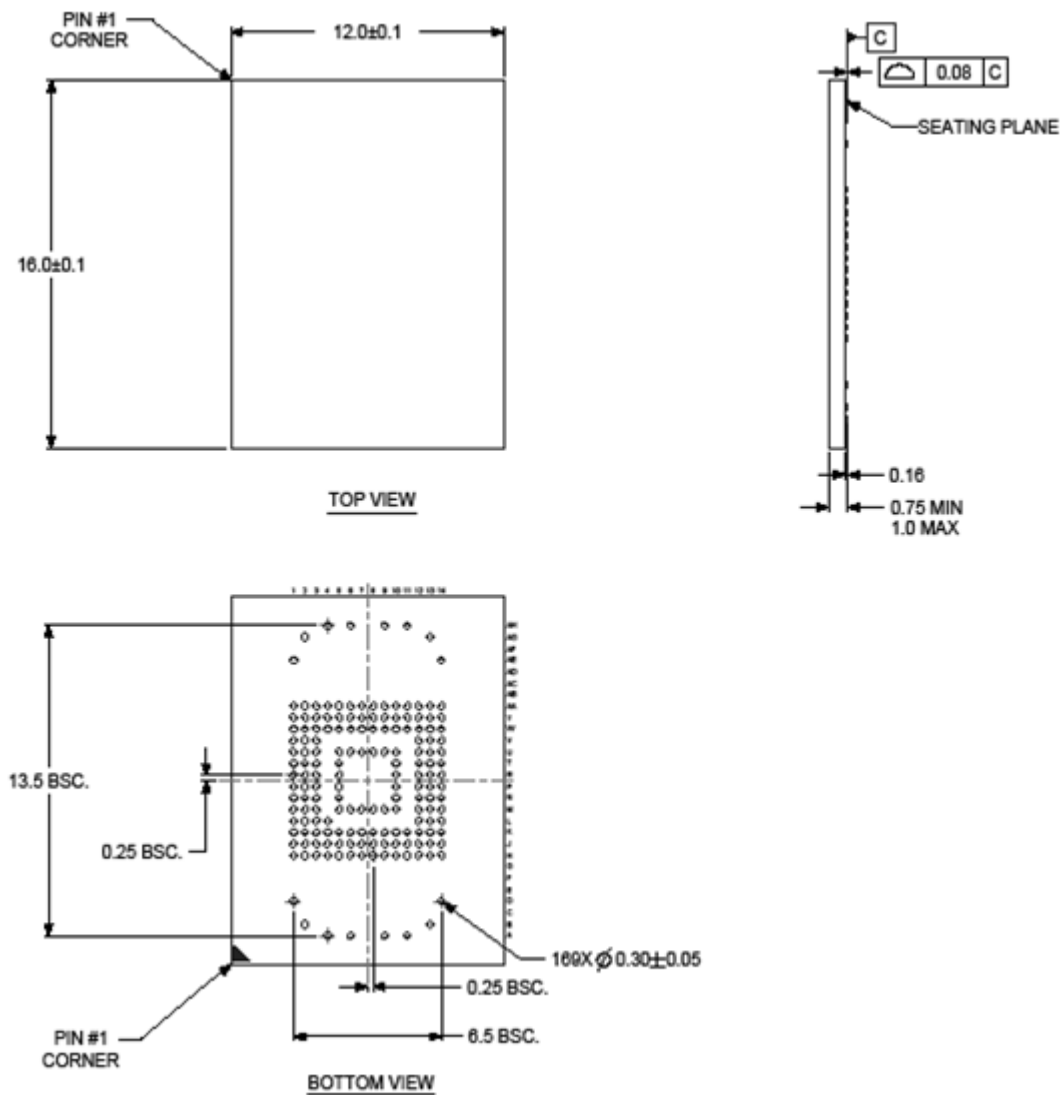
### 2.2.1 100-Ball Package Dimensions

**Figure 2:** 100-Ball LFBGA Dimensions - 14.0mm x 18.0mm x 1.4mm (Package Code: AE)

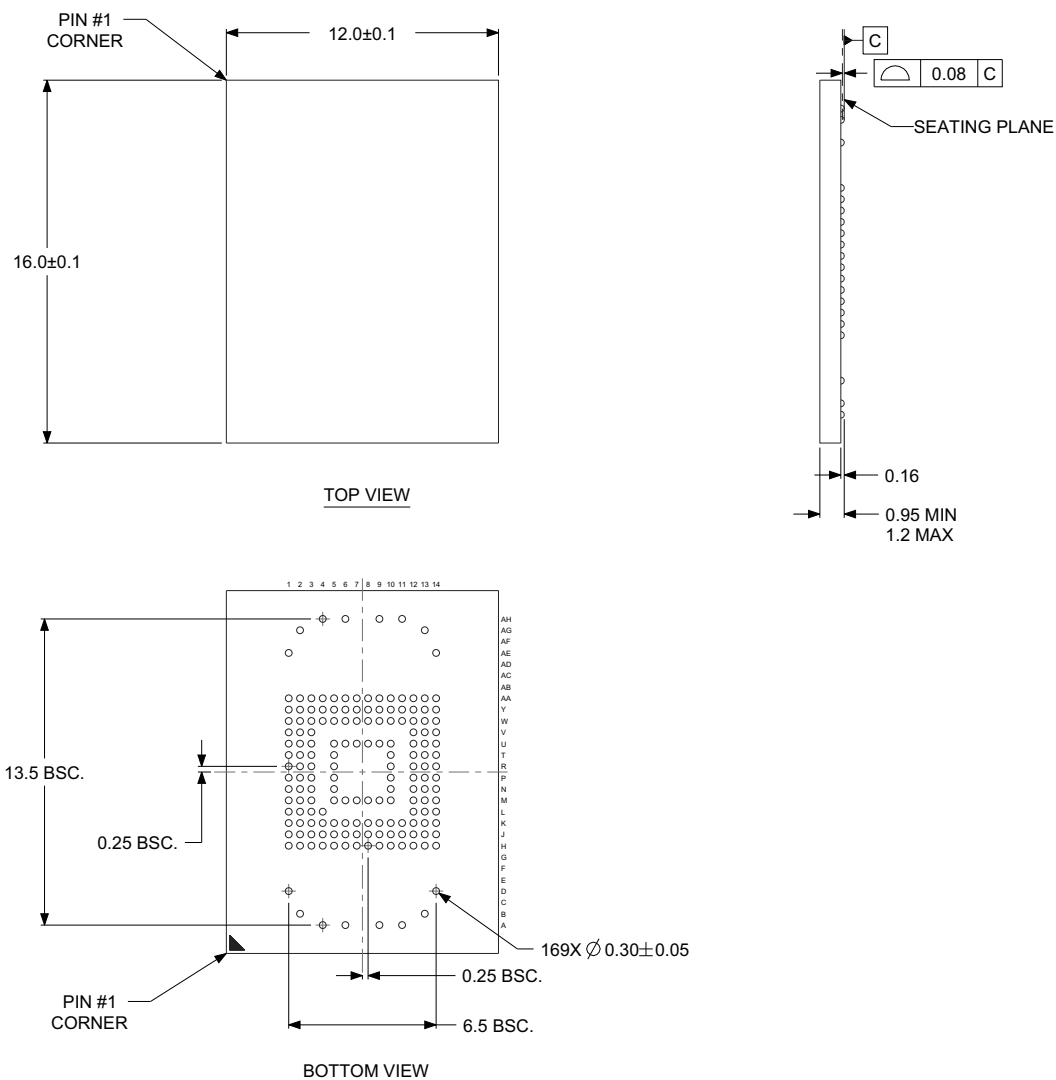


### 2.2.2 169-Ball Package Dimensions

**Figure 3:** 169-Ball VFBGA Dimensions - 12.0mm x 16.0mm x 1.0mm (Package Code: CA)



**Figure 4:** 169-Ball TFBGA Dimensions - 12.0mm x 16.0mm x 1.2mm (Package Code: CC)

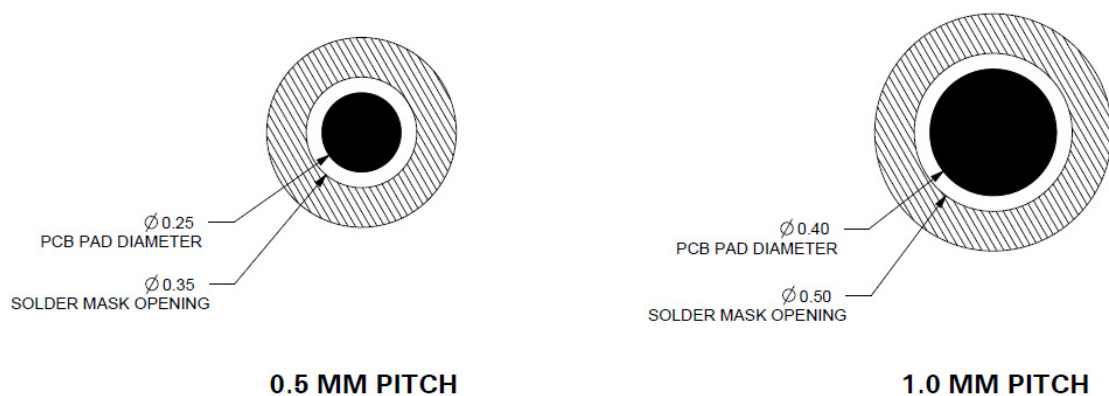


**Table 6:** Recommended Reflow Profile

| Reflow Parameters  | Suggested Range  |
|--------------------|------------------|
| Peak Temperature   | 235-250°C        |
| Time Above Liquids | 45 to 75 seconds |
| Cooling Rate       | < 4°C/sec        |

**Table 7:** Soldering Pad Dimension

| Package Type           | Pad Diameter | Pad Type |
|------------------------|--------------|----------|
| 169-Ball, 0.5 mm pitch | 0.25mm       | NSMD     |
| 100-Ball, 1.0 mm pitch | 0.40mm       | NSMD     |

**Figure 5:** Non Solder Mask Defined (NSMD) Pad Illustration


**Table 8:** Reliability

| Test Model                                  |                          | Result                 |              | Test Method        |
|---------------------------------------------|--------------------------|------------------------|--------------|--------------------|
| ESD                                         | Human Body Model (HBM)   | ESD Sensitivity Passed | ± 2000V      | AEC-Q100-002-E     |
|                                             |                          | AECQ Classification    | H2           |                    |
|                                             | Machine Model (MM)       | ESD Sensitivity Passed | ± 200V       | AEC-Q100-003-E     |
|                                             |                          | AECQ Classification    | M3           |                    |
|                                             | Charge Device Mode (CDM) | ESD Sensitivity Passed | ±750V        | AEC-Q100-011 Rev-C |
|                                             |                          | AECQ Classification    | C5           |                    |
| Latch-up Testing                            |                          | Latch-up condition     | 100mA @ 90°C | JESD78D,           |
|                                             |                          | JESD78D Classification | II           | AEC-Q100-004-D     |
| Moisture Resistance Test (MRT) <sup>1</sup> |                          | MSL 3                  |              | JESD22-A113        |

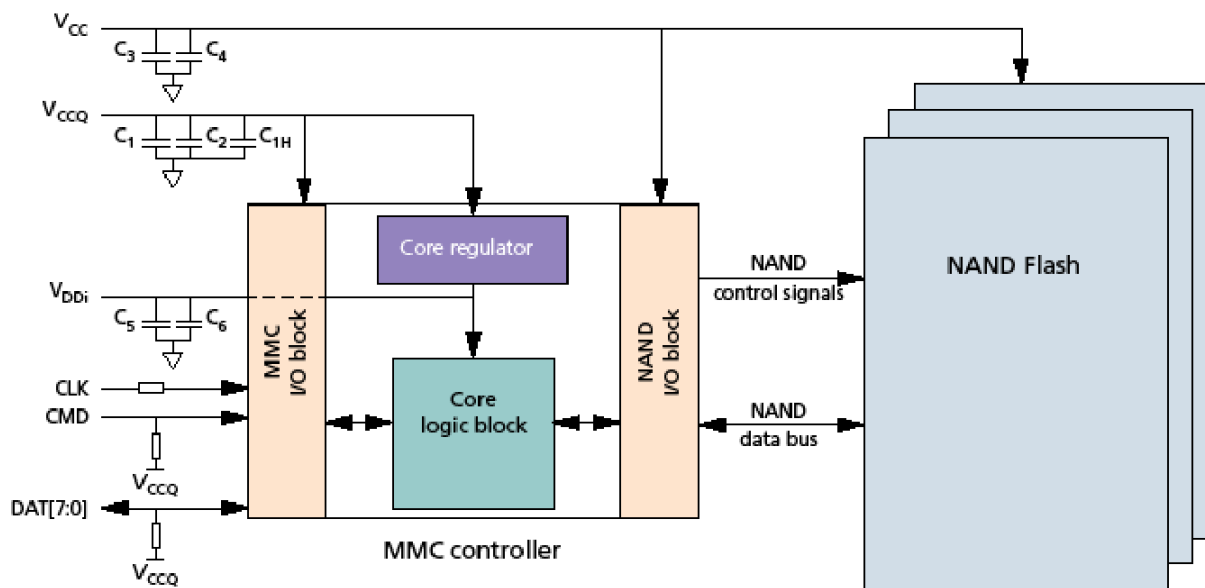
1. Recommended baking temperature: 90C (Refer to JEDEC J-STD-033 for corresponding baking time based on package thickness).

### 3.0 DC SPECIFICATIONS

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

$V_{CC}$  is used for the NAND Flash device and its interface voltage;  $V_{CCQ}$  is used for the controller and the eMMC interface voltage.

**Figure 6:** Device Power Diagram



**Table 9:** Power Domains

| Parameter      | Symbol    | Description                                                               |
|----------------|-----------|---------------------------------------------------------------------------|
| Host Interface | $V_{CCQ}$ | High voltage range = 3.3V (nominal)<br>Low voltage range = 1.8V (nominal) |
| Memory         | $V_{CC}$  | High voltage range = 3.3V (nominal)                                       |
| Internal       | $V_{DDi}$ | The internal regulator connection to an external decoupling capacitor     |

**Table 10:** Capacitor and Resistance Specifications

| Parameter                                      | Symbol                          | Min       | Typ | Max        | Units | Notes |
|------------------------------------------------|---------------------------------|-----------|-----|------------|-------|-------|
| Pull-up resistance: CMD                        | R_CMD                           | 4.7       | 10  | 50         | kΩ    | 1     |
| Pull-up resistance: DAT[7:0]                   | R_DAT                           | 10        | 50  | 50         | kΩ    | 1     |
| Pull-up resistance: RST_n                      | R-RSTn                          | 4.7       | 50  | 50         | kΩ    | 2     |
| CLK/CMD/DAT[7:0] impedance                     |                                 | 45        | 50  | 55         | Ω     | 3     |
| Serial resistance on CLK                       | SR_CLK                          | 0         | 22  | 47         | Ω     |       |
| V <sub>CCQ</sub> capacitor                     | C <sub>1H</sub>                 | 1 ± 0.05  | 1   | 2.2 ± 0.1  | μF    | 7     |
|                                                | C <sub>1</sub> , C <sub>2</sub> | 2.2 ± 0.1 | 2.2 | 4.7 ± 0.22 | μF    | 4     |
| V <sub>CC</sub> capacitor (≤8GB)               | C <sub>3</sub> , C <sub>4</sub> | 2.2 ± 0.1 | 2.2 | 4.7 ± 0.22 | μF    | 5     |
| V <sub>CC</sub> capacitor (>8GB)               |                                 |           | 4.7 |            | μF    |       |
| V <sub>DDi</sub> capacitor (C <sub>reg</sub> ) | C <sub>5</sub> , C <sub>6</sub> | 1 ± 0.05  | 1   | 2.2 ± 0.1  | μF    | 6     |

<sup>1</sup> Used to prevent bus floating.

<sup>2</sup> If host does not use H/W RESET (RST\_n), pull-up resistance is not needed on RST\_n line (Extended CSD register [162] = 0 b).

<sup>3</sup> Impedance match.

<sup>4</sup> The coupling capacitor should be connected with V<sub>DDQ</sub> and V<sub>SSQ</sub> as closely as possible.

<sup>5</sup> The coupling capacitor should be connected with V<sub>DD</sub> and V<sub>SS</sub> as closely as possible.

<sup>6</sup> The coupling capacitor should be connected with V<sub>DDi</sub> and V<sub>SSi</sub> as closely as possible.

<sup>7</sup> C<sub>1H</sub> should be adjacent to V<sub>CCQ</sub>-V<sub>SSQ</sub> balls (#K6/C6 and K4/C4 accordingly, next to DAT[7:0] balls). It should be located as close as possible to the balls defined in order to minimize parasitic effects.

### 3.1 Operational Characteristics

#### 3.1.1 Current Consumption

**Table 11:** Current Consumption

| Condition <sup>1</sup> |       | Typical Values ( $I_{CC}/I_{CCQ}$ ) |       |        | Units   |
|------------------------|-------|-------------------------------------|-------|--------|---------|
|                        |       | 8GB                                 | 16GB  | 32GB   |         |
| Write                  | DDR52 | 49/15                               | 79/19 | 121/21 | mA      |
|                        | HS200 | 49/17                               | 79/22 | 148/23 | mA      |
| Read                   | DDR52 | 61/26                               | 62/30 | 76/38  | mA      |
|                        | HS200 | 72/47                               | 97/33 | 126/65 | mA      |
| Sleep <sup>2</sup>     |       | 31/88                               | 49/94 | 81/100 | $\mu$ A |
| Auto-Standby           |       | 31/88                               | 49/94 | 81/100 | $\mu$ A |

<sup>1</sup> Bus in x8 I/O mode; 25°C;  $V_{CCQ} = 1.95V$ . Measurements done as average RMS current consumption over 100 milliseconds.

<sup>2</sup>  $V_{CC}$  Power switched off.

## 4.0 REGISTERS

### 4.1 CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by eMMC protocol. Each device is created with a unique identification number.

**Table 12:** CID Register Field Parameters

| Name                  | Field | Width | CID Bits  | CID Value      |
|-----------------------|-------|-------|-----------|----------------|
| Manufacturer ID       | MID   | 8     | [127:120] | F6h            |
| Reserved              | -     | 6     | [119:114] | -              |
| Card/BGA              | CBX   | 2     | [113:112] | 01h            |
| OEM/application ID    | OID   | 8     | [111:104] | 00h            |
| Product name          | PNM   | 8GB   | [103:56]  | 08GTEA         |
|                       |       | 16GB  |           | 16GTEA         |
|                       |       | 32GB  |           | 32GTEA         |
| Product revision      | PRV   | 8     | [55:48]   | 01h            |
| Product serial number | PSN   | 32    | [47:16]   | _ <sup>1</sup> |
| Manufacturing date    | MDT   | 8     | [15:8]    | _ <sup>2</sup> |
| CRC7 checksum         | CRC   | 7     | [7:1]     | _ <sup>3</sup> |
| Not used; always 1    | -     | 1     | 0         | 01h            |

<sup>1</sup> Unique for each device. 32-bit unsigned binary integer.

<sup>2</sup> 2 hex digits for device manufacturing month and year.

<sup>3</sup> CRC for CID register. Different for each device.

## 4.2 OCR Register

The 32-bit operations conditions register (OCR) stores the  $V_{DD}$  voltage profile of the device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the device power up procedure has been finished.

**Table 13:** OCR Register Definitions

| $V_{DD}$ Voltage Window | Width | OCR Bits | OCR Value                                    |
|-------------------------|-------|----------|----------------------------------------------|
| Ready/Busy              | 1     | [31]     | card power up status bit (busy) <sup>1</sup> |
| Access Mode             | 2     | [30:29]  | 02h                                          |
| Reserved                | 5     | [28:24]  | 00h                                          |
| 2.7-3.6V                | 9     | [23:15]  | 1FFh                                         |
| 2.0-2.6V                | 7     | [14:8]   | 00h                                          |
| 1.70-1.95V              | 1     | [7]      | 01h                                          |
| Reserved                | 7     | [6:0]    | 00h                                          |

<sup>1</sup> This bit is set to LOW if the device has not finished the power up routine.

### 4.3 CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM\_CSD (CMD27) command.

**Table 14:** CSD Register Field Parameters

| Name                                               | Field               | Width | Cell Type <sup>1</sup> | CSD Bits  | CSD Value |
|----------------------------------------------------|---------------------|-------|------------------------|-----------|-----------|
| CSD structure                                      | CSD_structure       | 2     | R                      | [127:126] | 03h       |
| System specification version                       | SPEC_VERS           | 4     | R                      | [125:122] | 04h       |
| Reserved <sup>2</sup>                              | -                   | 2     | -                      | [121:120] | -         |
| Data read access time 1                            | TAAC                | 8     | R                      | [119:112] | 4Fh       |
| Data read access time 2 in CLK cycles (NSAC x 100) | NSAC                | 8     | R                      | [111:104] | 01h       |
| Maximum bus clock frequency                        | TRAN_SPEED          | 8     | R                      | [103:96]  | 32h       |
| Card command classes                               | CCC                 | 12    | R                      | [95:84]   | 0F5h      |
| Maximum read data block length                     | READ_BL_LEN         | 4     | R                      | [83:80]   | 09h       |
| Partial blocks for reads supported                 | READ_BL_PARTIAL     | 1     | R                      | [79]      | 00h       |
| Write block misalignment                           | WRITE_BLK_MISALIGN  | 1     | R                      | [78]      | 00h       |
| Read block misalignment                            | READ_BLK_MISALIGN   | 1     | R                      | [77]      | 00h       |
| DS register implemented                            | DSR_IMP             | 1     | R                      | [76]      | 00h       |
| Reserved <sup>2</sup>                              | -                   | 2     | -                      | [75:74]   | -         |
| Device size                                        | C-SIZE              | 12    | R                      | [73:62]   | FFFh      |
| Maximum read current as $V_{DD,min}$               | VDD_R_CURR_MIN      | 3     | R                      | [61:59]   | 07h       |
| Maximum read current as $V_{DD,max}$               | VDD_R_CURR_MAX      | 3     | R                      | [58:56]   | 07h       |
| Maximum write current as $V_{DD,min}$              | VDD_W_CURR_MIN      | 3     | R                      | [55:53]   | 07h       |
| Maximum write current as $V_{DD,max}$              | VDD_W_CURR_MAX      | 3     | R                      | [52:50]   | 07h       |
| Device size multiplier                             | C-SIZE_MULT         | 3     | R                      | [49:47]   | 07h       |
| Erase group size                                   | ERASE_GRP_SIZE      | 5     | R                      | [46:42]   | 1Fh       |
| Erase group size multiplier                        | ERASE_GRP_SIZE_MULT | 5     | R                      | [41:37]   | 1Fh       |
| Write protect group size                           | WP_GRP_SIZE         | 8GB   | 5                      | [36:32]   | 0Fh       |
|                                                    |                     | 16GB  |                        |           | 1Fh       |
|                                                    |                     | 32GB  |                        |           | 1Fh       |
| Write protect group enable                         | WP_GRP_ENABLE       | 1     | R                      | [31]      | 01h       |
| Manufacturer default ECC                           | DEFAULT_ECC         | 2     | R                      | [30:29]   | 00h       |
| Write-speed factor                                 | R2W_FACTOR          | 3     | R                      | [28:26]   | 02h       |
| Maximum write data block length                    | WRITE_BL_LEN        | 4     | R                      | [25:22]   | 09h       |
| Partial blocks for writes supported                | WRITE_BL_PARTIAL    | 1     | R                      | [21]      | 00h       |
| Reserved <sup>2</sup>                              | -                   | 4     | -                      | [20:17]   | -         |

**Table 14:** CSD Register Field Parameters

| Name                           | Field              | Width | Cell Type <sup>1</sup> | CSD Bits | CSD Value |
|--------------------------------|--------------------|-------|------------------------|----------|-----------|
| Content protection application | CONTENT_PROT_APP   | 1     | R                      | [16]     | 00h       |
| File-format group              | FILE_FORMAT_GRP    | 1     | R/W                    | [15]     | 00h       |
| Copy flag (OTP)                | COPY               | 1     | R/W                    | [14]     | 00h       |
| Permanent write protection     | PERM_WRITE_PROTECT | 1     | R/W                    | [13]     | 00h       |
| Temporary write protection     | TEMP_WRITE_PROTECT | 1     | R/W/E                  | [12]     | 00h       |
| File format                    | FILE_FORMAT        | 2     | R/W                    | [11:10]  | 00h       |
| ECC                            | ECC                | 2     | R/W/E                  | [9:8]    | 00h       |
| CRC                            | CRC                | 7     | R/W/E                  | [7:1]    | Note 3    |
| Not used; always 1             | -                  | 1     | -                      | [0]      | -         |

<sup>1</sup> R = Read-only

R/W = One-time programmable and readable

R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST\_n signal, and any CMD0 reset, and readable

TBD = To be determined

<sup>2</sup> Reserved bits should be read as 0.

<sup>3</sup> CRC for CSD register. Different for each density

## 4.4 ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

**Table 15:** ECSD Register Field Parameters

| Name                                      | Field                                     | Size (Bytes) | Cell Type <sup>1</sup> | ECSD Bytes | ECSD Values |
|-------------------------------------------|-------------------------------------------|--------------|------------------------|------------|-------------|
| Reserved <sup>2</sup>                     | -                                         | 6            | -                      | [511:506]  | -           |
| Extended Security Commands Error          | EXT_SECURITY_ERR                          | 1            | R                      | [505]      | 00h         |
| Supported command sets                    | S_CMD_SET                                 | 1            | R                      | [504]      | 01h         |
| HPI features                              | HPI_FEATURES                              | 1            | R                      | [503]      | 01h         |
| Background operations support             | BKOPS_SUPPORT                             | 1            | R                      | [502]      | 01h         |
| Max packed read commands                  | MAX_PACKED_READS                          | 1            | R                      | [501]      | 3Ch         |
| Max packed write commands                 | MAX_PACKED_WRITES                         | 1            | R                      | [500]      | 3Ch         |
| Data tag support                          | DATA_TAG_SUPPORT                          | 1            | R                      | [499]      | 01h         |
| Tag unit size                             | TAG_UNIT_SIZE                             | 1            | R                      | [498]      | 03h         |
| Tag resources size                        | TAG_RES_SIZE                              | 1            | R                      | [497]      | 00h         |
| Context management capabilities           | CONTEXT_CAPABILITIES                      | 1            | R                      | [496]      | 05h         |
| Large unit size                           | LARGE_UNIT_SIZE_M1                        | 8GB          | 1                      | [495]      | 03h         |
|                                           |                                           | 16GB         |                        |            | 07h         |
|                                           |                                           | 32GB         |                        |            | 0Fh         |
| Extended partitions attribute support     | EXT_SUPPORT                               | 1            | R                      | [494]      | 03h         |
| Supported Modes                           | SUPPORTED_MODES                           | 1            | R                      | [493]      | 01h         |
| FFU features                              | FFU_FEATURES                              | 1            | R                      | [492]      | 00h         |
| Operations code timeout                   | OPERATION_CODE_TIMEOUT                    | 1            | R                      | [491]      | 00h         |
| FFU Argument                              | FFU_ARG                                   | 4            | R                      | [490:487]  | 00000000h   |
| Reserved <sup>2</sup>                     | -                                         | 181          | -                      | [486:306]  | -           |
| Number of FW sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4            | R                      | [305:302]  | 00000000h   |
| Vendor proprietary health report          | VENDOR_PROPRIETARY_HEALTH_REPORT          | 32           | R                      | [301:270]  | 00h (x32)   |
| Device life time estimation type B        | DEVICE_LIFE_TIME_EST_TYP_B                | 1            | R                      | [269]      | 01h         |

**Table 15:** ECSD Register Field Parameters

| Name                                                                      | Field                      | Size (Bytes) | Cell Type <sup>1</sup> | ECSD Bytes | ECSD Values           |
|---------------------------------------------------------------------------|----------------------------|--------------|------------------------|------------|-----------------------|
| Device life time estimation type A                                        | DEVICE_LIFE_TIME_EST_TYP_A | 1            | R                      | [268]      | 01h                   |
| Pre EOL information                                                       | PRE_EOL_INFO               | 1            | R                      | [267]      | 01h                   |
| Optimal read size                                                         | OPTIMAL_READ_SIZE          | 1            | R                      | [266]      | 01h                   |
| Optimal write size                                                        | OPTIMAL_WRITE_SIZE         | 1            | R                      | [265]      | 04h                   |
| Optimal trim unit size                                                    | OPTIMAL_TRIM_UNIT_SIZE     | 1            | R                      | [264]      | 01h                   |
| Reserved <sup>2</sup>                                                     | -                          | 2            | -                      | [263:262]  | -                     |
| Firmware version                                                          | FIRMWARE_VERSION           | 8            | R                      | [261:254]  | 64 or 67 <sup>4</sup> |
| Reserved <sup>2</sup>                                                     | -                          | 1            | -                      | [253]      | -                     |
| Cache size                                                                | CACHE_SIZE                 | 4            | R                      | [252:249]  | 00000000h             |
| Generic CMD6 timeout                                                      | GENERIC_CMD6_TIME          | 1            | R                      | [248]      | 19h                   |
| Power off notification (long) timeout                                     | POWER_OFF_LONG_TIME        | 1            | R                      | [247]      | FFh                   |
| Background operations status                                              | BKOPS_STATUS               | 1            | R                      | [246]      | 00h                   |
| Number of correctly programmed sectors                                    | CORRECTLY_PRG_SECTORS_NUM  | 4            | R                      | [245:242]  | 00000000h             |
| First initialization time after partitioning (first CMD1 to device ready) | INI_TIMEOUT_PA             | 1            | R                      | [241]      | 32h                   |
| Reserved <sup>2</sup>                                                     | -                          | 1            | -                      | [240]      | -                     |
| Power class for 52 MHz, DDR at 3.6V                                       | PWR_CL_DDR_52_360          | 1            | R                      | [239]      | 00h                   |
| Power class for 52 MHz, DDR at 1.95V                                      | PWR_CL_DDR_52_195          | 1            | R                      | [238]      | 00h                   |
| Power class for 200 MHz at 1.95V                                          | PWR_CL_200_195             | 1            | R                      | [237]      | 00h                   |
| Power class for 200 MHz at 1.3V                                           | PWR_CL_200_130             | 1            | R                      | [236]      | 00h                   |
| Minimum write performance for 8-bit at 52 MHz in DDR mode                 | MIN_PERF_DDR_W_8_52        | 1            | R                      | [235]      | 08h                   |
| Minimum read performance for 8-bit at 52 MHz in DDR mode                  | MIN_PERF_DDR_R_8_52        | 1            | R                      | [234]      | 08h                   |
| Reserved <sup>2</sup>                                                     | -                          | 1            | -                      | [233]      | -                     |
| TRIM multiplier                                                           | TRIM_MULT                  | 1            | R                      | [232]      | 0Fh                   |
| Secure feature support                                                    | SEC_FEATURE_SUPPORT        | 1            | R                      | [231]      | 55h                   |
| SECURE ERASE multiplier                                                   | SEC_ERASE_MULT             | 1            | R                      | [230]      | 06h                   |
| SECURE TRIM multiplier                                                    | SEC_TRIM_MULT              | 1            | R                      | [229]      | 09h                   |

**Table 15:** ECSD Register Field Parameters

| Name                                                              | Field                                   |      | Size<br>(Bytes) | Cell<br>Type <sup>1</sup> | ECSD<br>Bytes | ECSD<br>Values |
|-------------------------------------------------------------------|-----------------------------------------|------|-----------------|---------------------------|---------------|----------------|
| Boot information                                                  | BOOT_INFO                               |      | 1               | R                         | [228]         | 07h            |
| Reserved <sup>2</sup>                                             | -                                       |      | 1               | -                         | [227]         | -              |
| Boot partition size                                               | BOOT_SIZE_MULT                          |      | 1               | R                         | [226]         | 80h            |
| Access size                                                       | ACC_SIZE                                | 8GB  | 1               | R                         | [225]         | 06h            |
|                                                                   |                                         | 16GB |                 |                           |               | 07h            |
|                                                                   |                                         | 32GB |                 |                           |               | 08h            |
| High-capacity erase unit size                                     | HC_ERASE_GRP_SIZE                       | 8GB  | 1               | R                         | [224]         | 08h            |
|                                                                   |                                         | 16GB |                 |                           |               | 10h            |
|                                                                   |                                         | 32GB |                 |                           |               | 20h            |
| High-capacity erase timeout                                       | ERASE_TIMEOUT_MULT                      |      | 1               | R                         | [223]         | 01h            |
| Reliable write-sector count                                       | REL_WR_SEC_C                            |      | 1               | R                         | [222]         | 01h            |
| High-capacity write protect group size                            | HC_WP_GRP_SIZE                          |      | 1               | R                         | [221]         | 02h            |
| Sleep current (V <sub>CC</sub> )                                  | S_C_VCC                                 |      | 1               | R                         | [220]         | 08h            |
| Sleep current (V <sub>CCQ</sub> )                                 | S_C_VCCQ                                |      | 1               | R                         | [219]         | 08h            |
| Production state awareness timeout                                | PRODUCTION_STATE_AWARE-<br>NESS_TIMEOUT |      | 1               | R                         | [218]         | 14h            |
| Sleep/awake timeout                                               | S_A_TIMEOUT                             |      | 1               | R                         | [217]         | 10h            |
| Sleep Notification Timeout                                        | SLEEP_NOTIFICATION_TIME                 |      | 1               | R                         | [216]         | 0Fh            |
| Sector count                                                      | SEC-COUNT                               | 8GB  | 4               | R                         | [215:212]     | 00E68000h      |
|                                                                   |                                         | 16GB |                 |                           |               | 01CD0000h      |
|                                                                   |                                         | 32GB |                 |                           |               | 039A0000h      |
| Reserved <sup>2</sup>                                             | -                                       |      | 1               | -                         | [211]         | -              |
| Minimum write performance for 8-bit at 52 MHz                     | MIN_PERF_W_8_52                         |      | 1               | R                         | [210]         | 08h            |
| Minimum read performance for 8-bit at 52 MHz                      | MIN_PERF_R_8_52                         |      | 1               | R                         | [209]         | 08h            |
| Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz | MIN_PERF_W_8_26_4_52                    |      | 1               | R                         | [208]         | 08h            |
| Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz  | MIN_PERF_R_8_26_4_52                    |      | 1               | R                         | [207]         | 08h            |
| Minimum write performance for 4-bit at 26 MHz                     | MIN_PERF_W_4_26                         |      | 1               | R                         | [206]         | 08h            |
| Minimum read performance for 4-bit at 26 MHz                      | MIN_PERF_R_4_26                         |      | 1               | R                         | [205]         | 08h            |

**Table 15:** ECSD Register Field Parameters

| Name                                | Field                 | Size (Bytes) | Cell Type <sup>1</sup> | ECSD Bytes | ECSD Values      |
|-------------------------------------|-----------------------|--------------|------------------------|------------|------------------|
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [204]      | -                |
| Power class for 26 MHz at 3.6V      | PWR_CL_26_360         | 1            | R                      | [203]      | 00h              |
| Power class for 52 MHz at 3.6V      | PWR_CL_52_360         | 1            | R                      | [202]      | 00h              |
| Power class for 26 MHz at 1.95V     | PWR_CL_26_195         | 1            | R                      | [201]      | 00h              |
| Power class for 52 MHz at 1.95V     | PWR_CL_52_195         | 1            | R                      | [200]      | 00h              |
| Partition switching timing          | PARTITION_SWITCH_TIME | 1            | R                      | [199]      | 03h              |
| Out-of-interrupt busy timing        | OUT_OF_INTERRUPT_TIME | 1            | R                      | [198]      | 04h              |
| I/O driver strength                 | DRIVER_STRENGTH       | 1            | R                      | [197]      | 0Fh              |
| Card type                           | CARD_TYPE             | 1            | R                      | [196]      | 17h              |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [195]      | -                |
| CSD structure version               | CSD_STRUCTURE         | 1            | R                      | [194]      | 02h              |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [193]      | -                |
| Extended CSD revision               | EXT_CSD_REV           | 1            | -                      | [192]      | 06h              |
| Command set                         | CMD_SET               | 1            | R/W/E_P                | [191]      | 00h              |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [190]      | -                |
| Command set revision                | CMD_SET_REV           | 1            | R                      | [189]      | 00h              |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [188]      | -                |
| Power class                         | POWER_CLASS           | 1            | R/W/E_P                | [187]      | 00h              |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [186]      | -                |
| High-speed interface timing         | HS_TIMING             | 1            | R/W/E_P                | [185]      | 00h <sup>3</sup> |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [184]      | -                |
| Bus width mode                      | BUS_WIDTH             | 1            | W/E_P                  | [183]      | 00h <sup>3</sup> |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [182]      | -                |
| Erased memory content               | ERASED_MEM_CONT       | 1            | R                      | [181]      | 00h              |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [180]      | -                |
| Partition configuration             | PARTITION_CONFIG      | 1            | R/W/E,<br>R/W/E_P      | [179]      | 00h              |
| Boot configuration protection       | BOOT_CONFIG_PROT      | 1            | R/W, R/<br>W/C_P       | [178]      | 00h              |
| Boot bus width                      | BOOT_BUS_CONDITIONS   | 1            | R/W/E                  | [177]      | 00h              |
| Reserved <sup>2</sup>               | -                     | 1            | -                      | [176]      | -                |
| High-density erase group definition | ERASE_GROUP_DEF       | 1            | R/W/E_P                | [175]      | 00h              |

Table 15: ECSD Register Field Parameters

| Name                                   | Field                          | Size (Bytes) | Cell Type <sup>1</sup> | ECSD Bytes | ECSD Values |
|----------------------------------------|--------------------------------|--------------|------------------------|------------|-------------|
| Boot write protection status registers | BOOT_WP_STATUS                 | 1            | R                      | [174]      | 00h         |
| Boot area write protection register    | BOOT_WP                        | 1            | R/W, R/W/C_P           | [173]      | 00h         |
| Reserved <sup>2</sup>                  | -                              | 1            | -                      | [172]      | -           |
| User write protection register         | USER_WP                        | 1            | R/W, R/W/C_P, R/W/E_P  | [171]      | 00h         |
| Reserved <sup>2</sup>                  | -                              | 1            | -                      | [170]      | -           |
| Firmware configuration                 | FW_CONFIG                      | 1            | R/W                    | [169]      | 00h         |
| RPMB size                              | RPMB_SIZE_MULT                 | 1            | R                      | [168]      | 01h         |
| Write reliability setting register     | WR_REL_SET                     | 1            | R/W                    | [167]      | 00h         |
| Write reliability parameter register   | WR_REL_PARAM                   | 1            | R                      | [166]      | 05h         |
| Start sanitize operation               | SANITIZE_START                 | 1            | W/E_P                  | [165]      | 00h         |
| Manually start background operations   | BKOPS_START                    | 1            | W/E_P                  | [164]      | 00h         |
| Enable background operations handshake | BKOPS_EN                       | 1            | R/W                    | [163]      | 00h         |
| Hardware reset function                | RST_n_FUNCTION                 | 1            | R/W                    | [162]      | 00h         |
| HPI management                         | HPI_MGMT                       | 1            | R/W/E/P                | [161]      | 00h         |
| Partitioning support                   | PARTITIONING_SUPPORT           | 1            | R/W/E, R/W/E_P         | [160]      | 07h         |
| Maximum enhanced area size             | MAX_ENH_SIZE_MULT              | 3            | R                      | [159:157]  | 0001CDh     |
| Partitions attribute                   | PARTITIONS_ATTRIBUTE           | 1            | R/W                    | [156]      | 00h         |
| Partitioning setting                   | PARTITIONING_SETTING-COMPLETED | 1            | R/W                    | [155]      | 00h         |
| General-purpose partition size         | GP_SIZE_MULT_GP4               | 12           | R/W                    | [154:152]  | 000000h     |
|                                        | GP_SIZE_MULT_GP3               |              |                        | [151:149]  | 000000h     |
|                                        | GP_SIZE_MULT_GP2               |              |                        | [148:146]  | 000000h     |
|                                        | GP_SIZE_MULT_GP1               |              |                        | [145:143]  | 000000h     |
| Enhanced user data area size           | ENH_SIZE_MULT                  | 3            | R/W                    | [142:140]  | 000000h     |
| Enhanced user data start address       | ENH_START_ADDR                 | 4            | R/W                    | [139:136]  | 00000000h   |
| Reserved <sup>2</sup>                  | -                              | 1            | -                      | [135]      | -           |
| Bad block management mode              | SEC_BAD_BLK_MGMNT              | 1            | R/W                    | [134]      | 00h         |

**Table 15:** ECSD Register Field Parameters

| Name                                                     | Field                       |      | Size (Bytes) | Cell Type <sup>1</sup> | ECSD Bytes | ECSD Values |
|----------------------------------------------------------|-----------------------------|------|--------------|------------------------|------------|-------------|
| Production state awareness                               | PRODUCTION_STATE_AWARENESS  |      | 1            | R/W/E                  | [133]      | 00h         |
| Package case temperature is controlled                   | TCASE_SUPPORT               |      | 1            | W/E_P                  | [132]      | 00h         |
| Periodic wake-up                                         | PERIODIC_WAKEUP             |      | 1            | R/W/E                  | [131]      | 00h         |
| Program CID/CSD in DDR mode support                      | PROGRAM_CID_CSD_DDR_SUPPORT |      | 1            | R                      | [130]      | 01h         |
| Reserved <sup>2</sup>                                    | -                           |      | 2            | -                      | [129:128]  | -           |
| Vendor specific fields                                   | VENDOR_SPECIFIC_NFIELD      |      | 64           | <vendor specific>      | [127:64]   | 00h (x64)   |
| Native sector size                                       | NATIVE_SECTOR_SIZE          |      | 1            | R                      | [63]       | 00h         |
| Sector size emulation                                    | USE_NATIVE_SECTOR           |      | 1            | R/W                    | [62]       | 00h         |
| Sector size                                              | DATA_SECTOR_SIZE            |      | 1            | R                      | [61]       | 00h         |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU             |      | 1            | R                      | [60]       | 0Ah         |
| Class 6 command control                                  | CLASS_6_CTRL                |      | 1            | R/W/E_P                | [59]       | 00h         |
| Number of addressed groups to be released                | DYNCAP_NEEDED               |      | 1            | R                      | [58]       | 00h         |
| Exception events control                                 | EXCEPTION_EVENTS_CTRL       |      | 2            | R/W/E_P                | [57:56]    | 00h         |
| Exception events status                                  | EXCEPTION_EVENTS_STATUS     |      | 2            | R                      | [55:54]    | 00h         |
| Extended partitions attribute                            | EXT_PARTITIONS_ATTRIBUTE    |      | 2            | R/W                    | [53:52]    | 00h         |
| Context configuration                                    | CONTEXT_CONF                |      | 15           | R/W/E_P                | [51:37]    | 00h         |
| Packed command status                                    | PACKED_COMMAND_STATUS       |      | 1            | R                      | [36]       | 00h         |
| Packed command failure index                             | PACKED_FAILURE_INDEX        |      | 1            | R                      | [35]       | 00h         |
| Power off notification                                   | POWER_OFF_NOTIFICATION      |      | 1            | R/W/E_P                | [34]       | 00h         |
| Control to turn the cache on/off                         | CACHE_CTRL                  |      | 1            | R/W/E_P                | [33]       | 00h         |
| Flushing of the cache                                    | FLUSH_CACHE                 |      | 1            | W/E_P                  | [32]       | 00h         |
| Reserved <sup>2</sup>                                    | -                           |      | 1            | -                      | [31]       | -           |
| Mode config                                              | MODE_CONFIG                 |      | 1            | R/W/E_P                | [30]       | 00h         |
| Mode operation codes                                     | MODE_OPERATION_CODES        |      | 1            | W/E_P                  | [29]       | 00h         |
| Reserved <sup>2</sup>                                    | -                           |      | 2            | -                      | [28:27]    | -           |
| FFU status                                               | FFU_STATUS                  |      | 1            | R                      | [26]       | 00h         |
| Pre loading data size                                    | PRE_LOADING_DATA_SIZE       |      | 4            | R/W/E_P                | [25:22]    | 00000000h   |
| Max pre loading data size                                | MAX_PRE_LOADING_DATA_SIZE   | 8GB  | 4            | R                      | [21:18]    | 734000h     |
|                                                          |                             | 16GB |              |                        |            | E68000h     |
|                                                          |                             | 32GB |              |                        |            | 1CD0000h    |

**Table 15:** ECSD Register Field Parameters

| Name                               | Field                              | Size (Bytes) | Cell Type <sup>1</sup> | ECSD Bytes | ECSD Values |
|------------------------------------|------------------------------------|--------------|------------------------|------------|-------------|
| Product state awareness enablement | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1            | R/W/E & R              | [17]       | 01h         |
| Secure removal type                | SECURE_REMOVAL_TYPE                | 1            | R/W & R                | [16]       | 00h         |
| Reserved <sup>2</sup>              | -                                  | 16           | -                      | [15:0]     | -           |

<sup>1</sup> R = Read-only

R/W = One-time programmable and readable

R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST<sub>n</sub> signal, and any CMD0 reset, and readable

R/W/C\_P = Writable after the value is cleared by a power cycle and assertion of the RST<sub>n</sub> signal (the value not cleared by CMD0 reset) and readable

R/W/E\_P = Multiple writable with the value reset after a power cycle, assertion of the RST<sub>n</sub> signal, and any CMD0 reset, and readable

W/E\_P = Multiple writable with the value reset after power cycle, assertion of the RST<sub>n</sub> signal, and any CMD0 reset, and not readable

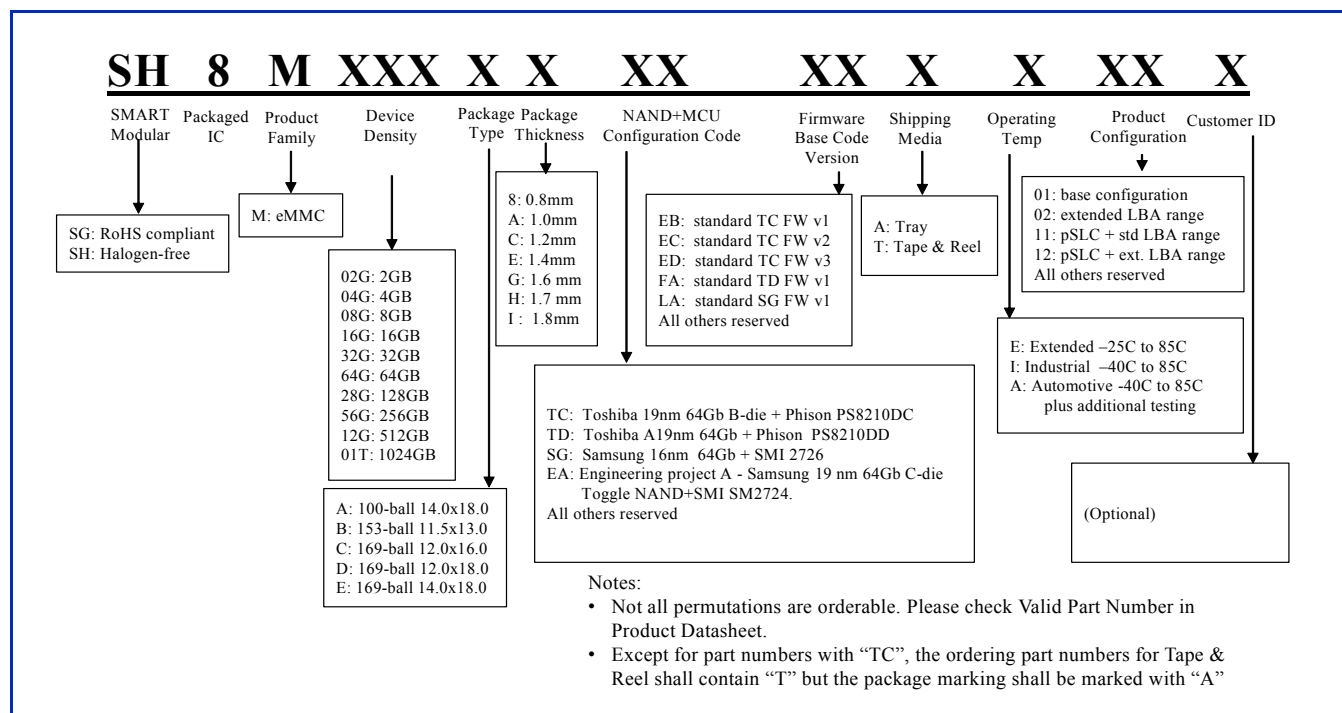
<sup>2</sup> Reserved bits should be read as 0.

<sup>3</sup> Set by host during device initialization. Default is 00h.

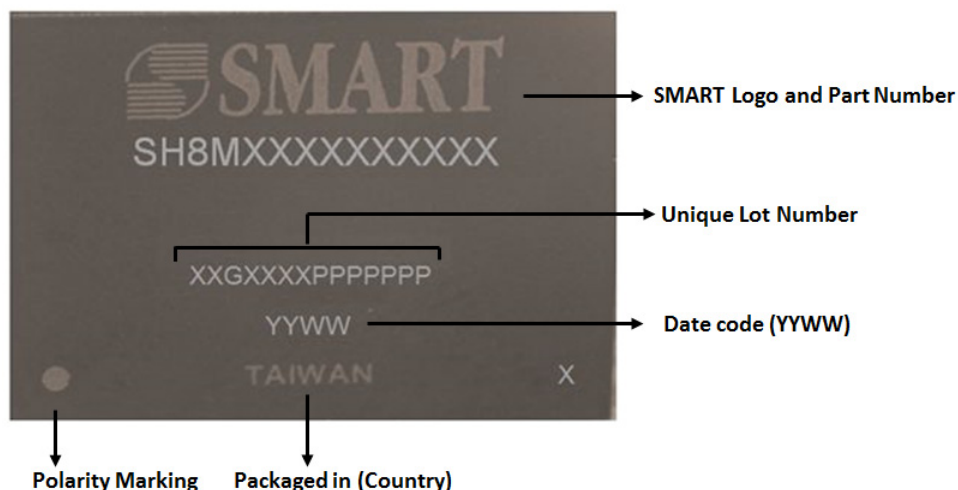
<sup>4</sup> Firmware version = 64 for FW6.64 and 67 for FW6.67

## 5.0 PART NUMBERS

### 5.1 Part Number Decoder



### 5.2 Marking Decoder



### 5.3 Part Numbering Information

**Table 16:** Automotive eMMC - JEDEC 0.5mm 169-Ball

| Part Number       | Density | NAND Vendor | NAND Litho | Tech | NAND Die | # of Die | Package               | Temp              | Controller | eMMC Spec |
|-------------------|---------|-------------|------------|------|----------|----------|-----------------------|-------------------|------------|-----------|
| SH8M08GCATCEyxA01 | 8GB     | Toshiba     | 19nm       | MLC  | 64Gb     | 1        | 169-Ball<br>12x16x1.0 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M16GCATCEyxA01 | 16GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 2        | 169-Ball<br>12x16x1.0 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M32GCCTCEyxA01 | 32GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 4        | 169-Ball<br>12x16x1.2 | -40°C to<br>+85°C | PS8210     | 4.51+     |

y = C for v4.51+ firmware v2 (FW v6.64)

y = D for v4.51+ firmware v3 (FW v6.67)

x = A for tray

x = T for tape & reel

**Table 17:** Automotive eMMC - 1.0mm 100-Ball

| Part Number       | Density | NAND Vendor | NAND Litho | Tech | NAND Die | # of Die | Package               | Temp              | Controller | eMMC Spec |
|-------------------|---------|-------------|------------|------|----------|----------|-----------------------|-------------------|------------|-----------|
| SH8M08GAETCEyxA01 | 8GB     | Toshiba     | 19nm       | MLC  | 64Gb     | 1        | 100-Ball<br>14x18x1.4 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M16GAETCEyxA01 | 16GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 2        | 100-Ball<br>14x18x1.4 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M32GAETCEyxA01 | 32GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 4        | 100-Ball<br>14x18x1.4 | -40°C to<br>+85°C | PS8210     | 4.51+     |

y = C for v4.51+ firmware v2 (FW v6.64)

y = D for v4.51+ firmware v3 (FW v6.67)

x = A for tray

x = T for tape & reel

## PRODUCT SPECIFICATION

**Table 18:** Industrial Temperature eMMC - JEDEC 0.5mm 169-Ball

| Part Number       | Density | NAND Vendor | NAND Litho | Tech | NAND Die | # of Die | Package               | Temp              | Controller | eMMC Spec |
|-------------------|---------|-------------|------------|------|----------|----------|-----------------------|-------------------|------------|-----------|
| SH8M08GCATCEyxl01 | 8GB     | Toshiba     | 19nm       | MLC  | 64Gb     | 1        | 169-Ball<br>12x16x1.0 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M16GCATCEyxl01 | 16GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 2        | 169-Ball<br>12x16x1.0 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M32GCCTCEyxl01 | 32GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 4        | 169-Ball<br>12x16x1.2 | -40°C to<br>+85°C | PS8210     | 4.51+     |

y = C for v4.51+ firmware v2 (FW v6.64)

y = D for v4.51+ firmware v3 (FW v6.67)

x = A for tray

x = T for tape &amp; reel

**Table 19:** Industrial Temperature eMMC - 1.0mm 100-Ball

| Part Number       | Density | NAND Vendor | NAND Litho | Tech | NAND Die | # of Die | Package               | Temp              | Controller | eMMC Spec |
|-------------------|---------|-------------|------------|------|----------|----------|-----------------------|-------------------|------------|-----------|
| SH8M08GAETCEyxl01 | 8GB     | Toshiba     | 19nm       | MLC  | 64Gb     | 1        | 100-Ball<br>14x18x1.4 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M16GAETCEyxl01 | 16GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 2        | 100-Ball<br>14x18x1.4 | -40°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M32GAETCEyxl01 | 32GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 4        | 100-Ball<br>14x18x1.4 | -40°C to<br>+85°C | PS8210     | 4.51+     |

y = C for v4.51+ firmware v2 (FW v6.64)

y = D for v4.51+ firmware v3 (FW v6.67)

x = A for tray

x = T for tape &amp; reel

**Table 20:** Extended Temperature eMMC - JEDEC 0.5mm 169-Ball

| Part Number       | Density | NAND Vendor | NAND Litho | Tech | NAND Die | # of Die | Package               | Temp              | Controller | eMMC Spec |
|-------------------|---------|-------------|------------|------|----------|----------|-----------------------|-------------------|------------|-----------|
| SH8M08GCATCEyxE01 | 8GB     | Toshiba     | 19nm       | MLC  | 64Gb     | 1        | 169-Ball<br>12x16x1.0 | -25°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M16GCATCEyxE01 | 16GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 2        | 169-Ball<br>12x16x1.0 | -25°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M32GCCTCEyxE01 | 32GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 4        | 169-Ball<br>12x16x1.2 | -25°C to<br>+85°C | PS8210     | 4.51+     |

y = C for v4.51+ firmware v2 (FW v6.64)

y = D for v4.51+ firmware v3 (FW v6.67)

x = A for tray

x = T for tape & reel

**Table 21:** Extended Temperature eMMC - 1.0mm 100-Ball

| Part Number       | Density | NAND Vendor | NAND Litho | Tech | NAND Die | # of Die | Package               | Temp              | Controller | eMMC Spec |
|-------------------|---------|-------------|------------|------|----------|----------|-----------------------|-------------------|------------|-----------|
| SH8M08GAETCEyxE01 | 8GB     | Toshiba     | 19nm       | MLC  | 64Gb     | 1        | 100-Ball<br>14x18x1.4 | -25°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M16GAETCEyxE01 | 16GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 2        | 100-Ball<br>14x18x1.4 | -25°C to<br>+85°C | PS8210     | 4.51+     |
| SH8M32GAETCEyxE01 | 32GB    | Toshiba     | 19nm       | MLC  | 64Gb     | 4        | 100-Ball<br>14x18x1.4 | -25°C to<br>+85°C | PS8210     | 4.51+     |

y = C for v4.51+ firmware v2 (FW v6.64)

y = D for v4.51+ firmware v3 (FW v6.67)

x = A for tray

x = T for tape & reel

**Disclaimer:**

No part of this document may be copied or reproduced in any form or by any means, or transferred to any third party, without the prior written consent of an authorized representative of SMART Modular Technologies, Inc. ("SMART"). The information in this document is subject to change without notice. SMART assumes no responsibility for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein. SMART makes no commitments to update or to keep current information contained in this document. The products listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. Moreover, SMART does not recommend or approve the use of any of its products in life support devices or systems or in any application where failure could result in injury or death. If a customer wishes to use SMART products in applications not intended by SMART, said customer must contact an authorized SMART representative to determine SMART's willingness to support a given application. The information set forth in this document does not convey any license under the copyrights, patent rights, trademarks or other intellectual property rights claimed and owned by SMART. The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by SMART.

ALL PRODUCTS SOLD BY SMART ARE COVERED BY THE PROVISIONS APPEARING IN SMART'S TERMS AND CONDITIONS OF SALE ONLY, INCLUDING THE LIMITATIONS OF LIABILITY, WARRANTY AND INFRINGEMENT PROVISIONS. SMART MAKES NO WARRANTIES OF ANY KIND, EXPRESS, STATUTORY, IMPLIED OR OTHERWISE, REGARDING INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED PRODUCTS FROM INTELLECTUAL PROPERTY INFRINGEMENT, AND EXPRESSLY DISCLAIMS ANY SUCH WARRANTIES INCLUDING WITHOUT LIMITATION ANY EXPRESS, STATUTORY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

©2015 SMART Modular Technologies, Inc. All rights reserved.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

## SMART Modular Technologies:

[SH8M08GCATCEDAA01](#) [SH8M16GCATCEDAA01](#) [SH8M32GCCTCEDAA01](#) [SH8M08GAETCEDAA01](#)  
[SH8M16GAETCEDAA01](#) [SH8M32GAETCEDAA01](#) [SH8M08GCATCEDAI01](#) [SH8M16GCATCEDAI01](#)  
[SH8M32GCCTCEDAI01](#) [SH8M08GAETCEDAI01](#) [SH8M16GAETCEDAI01](#) [SH8M32GAETCEDAI01](#)  
[SH8M08GCATCEDAE01](#) [SH8M16GCATCEDAE01](#) [SH8M32GCCTCEDAE01](#) [SH8M08GAETCEDAE01](#)  
[SH8M16GAETCEDAE01](#) [SH8M32GAETCEDAE01](#)