CELLULAR

TOBY-L4 series

LTE Advanced (Cat 6) modules with 3G and 2G fallback

System Integration Manual

Abstract

This document describes the features and the system integration of TOBY-L4 series multi-mode cellular modules.

The modules are a complete and cost efficient LTE-FDD, LTE-TDD, DC-HSPA+, (E)GPRS multi-mode and multi-band solution with uCPU embedded Linux programming capability. The modules offer up to 301.5 Mb/s download and up to 51.0 Mb/s upload data rates with Category 6 LTE-Advanced carrier aggregation technology in the compact TOBY form factor.

www.u-blox.com

UBX-16024839 - R04

Document Information		
Title	**TOBY-L4 series**	
Subtitle	LTE Advanced (Cat 6) modules with 3G and 2G fallback	
Document type	System Integration Manual	
Document number	UBX-16024839	
Revision, date	R04	08-Feb-2018
Disclosure restriction		

Product Status	Corresponding content status	
Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
In Development / Prototype	Objective Specification	Target values. Revised and supplementary data will be published later.
Engineering Sample	Advance Information	Data based on early testing. Revised and supplementary data will be published later.
Initial Production	Early Prod. Information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production Information	Final product specification.

This document applies to the following products:

Name	Type number	Modem version	Application version	PCN reference	Product status
TOBY-L4006	TOBY-L4006-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4006-50A-00	40.24	A00.02	UBX-18007908	Engineering Sample
TOBY-L4106	TOBY-L4106-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4106-50A-00	40.24	A00.02	UBX-18007908	Engineering Sample
TOBY-L4206	TOBY-L4206-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4206-50A-00	TBD	TBD	TBD	Functional Sample
TOBY-L4906	TOBY-L4906-00A-00	TBD	TBD	TBD	Functional Sample
	TOBY-L4906-50A-00	40.19	A00.02	UBX-17058711	Engineering Sample

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **AT Commands Manual**: This document provides the description of the AT commands supported by the u-blox cellular modules.
- **System Integration Manual**: This document provides the description of u-blox cellular modules' system from the hardware and the software point of view, it provides hardware design guidelines for the optimal integration of the cellular modules in the application device and it provides information on how to set up production and final product tests on application devices integrating the cellular modules.
- **Application Note**: These documents provide guidelines and information on specific hardware and/or software topics on u-blox cellular modules. See Related documents for a list of Application Notes related to your Cellular Module.

How to use this Manual

The TOBY-L4 series System Integration Manual provides the necessary information to successfully design and configure the u-blox cellular modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox Cellular Integration:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com/

Technical Support

Worldwide Web

Our website (http://www.u-blox.com/) is a rich pool of information. Product information, technical documents can be accessed 24h a day.

By E-mail

Contact the closest Technical Support office by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support, have the following information ready:

- Module type (TOBY-L4106) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

The TOBY-L4 series modules support multi-band LTE-FDD, LTE-TDD, DC-HSPA+, and (E)GPRS radio access technologies (see Table 1) in the very small TOBY 248-pin LGA form-factor (35.6 x 24.8 mm), which is easy to integrate in compact designs.

TOBY-L4 series modules are form-factor compatible with the other u-blox cellular module families (including SARA, LISA, LARA, and TOBY form-factors): this allows customers to take maximum advantage of their hardware and software investments, and provides very short time-to-market.

With LTE-Advanced carrier aggregation category 6 data rates up to 301.5 Mbit/s (downlink) / 51.0 Mbit/s (uplink), the modules are ideal for applications requiring the highest data-rates and high-speed internet access. Reduced cost variants supporting LTE Cat 4 or LTE Cat 1 will be available for lower speed or "pure" telematics devices.

TOBY-L4 series include the following LTE Cat 6 modules with 3G and 2G fallback:

- TOBY-L4006 modules, mainly designed for operation in North America
- TOBY-L4106 modules, mainly designed for operation in Europe
- TOBY-L4206 modules, mainly designed for operation in Asia-Pacific and South America
- TOBY-L4906 modules, mainly designed for operation in China

TOBY-L4 series modules include the following product versions:

- The "00" product versions, integrating the u-blox uCPU on-chip processor to allow customers to run their dedicated applications on an embedded Linux distribution based on Yocto, with RIL-Core connectivity APIs
- The "50" product versions, which can be controlled by an external application processor through standard and u-blox proprietary AT commands described in the u-blox AT Commands Manual [2]

TOBY-L4 series modules are the ideal product for the development of all kinds of automotive devices, such as smart antennas and in-dash telematics / infotainment devices, supporting a comprehensive set of HW interfaces (including RGMII/RMII for Ethernet and analog audio) over a very extended temperature range that allow the establishment of an emergency call up to +95 °C, complemented by a set of state-of-the art security features.

TOBY-L4 series modules are also the perfect choice for consumer fixed-wireless terminals, mobile routers and gateways, applications requiring video streaming and many other industrial (M2M) applications.

TOBY-L4 series modules are manufactured in ISO/TS 16949 certified sites, with the highest production standards and the highest quality and reliability. Each module is fully tested and inspected during production. The modules are qualified according to the automotive requirements as for systems installed in vehicles.

Table 1 summarizes the main features and interfaces of the TOBY-L4 series modules.

Model	Region	Bands				Interfaces														Features									Grade		
		LTE FDD bands	LTE TDD bands	UMTS FDD bands	GSM bands	UART	USB 2.0 device/host*	USB 3.0 device**	SPI	RGMII / RMII	eMMC	SDIO	DDC (I^2C)	SIM	GPIO	ADC	Antenna supervisor	CA / MIMO / Rx Diversity	Analog audio	Digital Audio	uCPU for customer applications	GNSS via modem	Wi-Fi via modem	Network indication	Jamming detection	Embedded TCP/UDP stack	Embedded HTTP, FTP, SSL	FOTA	Dual stack IPv4/IPv6	Standard	Professional	Automotive
TOBY-L4006-00	North America	2,4,5 7,12 13,29		2 4,5	850 1900	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•	•		
TOBY-L4006-50	North America	2,4,5 7,12 13,29		2 4,5	850 1900		1	1						2	9		•	•	•	•					•			•	•		
TOBY-L4106-00	EMEA	1,3 7,8 20	38	1,8	900 1800	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•	•		
TOBY-L4106-50	EMEA	1,3 7,8 20	38	1,8	900 1800		1	1						2	9		•	•	•	•					•			•	•		
TOBY-L4206-00	APAC, South America	1,3,5 7,8,9 19,28		1 5,8	Quad	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•	•		
TOBY-L4206-50	APAC, South America	1,3,5 7,8,9 19,28		1 5,8	Quad		1	1						2	9		•	•	•	•					•			•	•		
TOBY-L4906-00	China	1,3	39 40,41	1,8	900 1800	4	1	1	2	1	1	1	2	2	14	2	•	•	•	•	•	•	•	•	•	•	•	•	•	•		
TOBY-L4906-50	China	1,3	39 40,41	1,8	900 1800		1	1						2	9		•	•	•	•					•			•	•		

* USB 2.0 host role not supported by the "50" product versions

** USB 3.0 interface supported by future firmware versions

Table 1: TOBY-L4 series main features summary

TOBY-L4 series modules provide multi-band 4G / 3G / 2G multi-mode radio access technologies, based on the 3GPP Release 10 protocol stack, with the main characteristics summarized in Table 2 and Table 3.

LTE	3G	2G
LTE-Advanced Carrier Aggregation Frequency Division Duplex (LTE FDD) Time Division Duplex (LTE TDD) Down-Link CA / MIMO / Rx diversity	Dual-Cell High Speed Packet Access Frequency Division Duplex (UMTS FDD) Down-Link Rx diversity	Enhanced Data rate GSM Evolution (EDGE) Time Division Multiple Access (TDMA) DL Advanced Rx Performance Phase 1
LTE FDD Power Class • Class 3 (23 dBm) LTE TDD Power Class • Class 3 (23 dBm)	UMTS FDD Power Class • Class 3 (24 dBm)	GMSK Power Class • Class 4 (33 dBm) for GSM/E-GSM bands • Class 1 (30 dBm) for DCS/PCS bands 8-PSK Power Class • Class E2 (27 dBm) for GSM/E-GSM bands • Class E2 (26 dBm) for DCS/PCS bands

Data rate
• LTE category 6:
  • up to 301.5 Mbit/s DL
  • up to 51.0 Mbit/s UL
	Data rate
	• FDD UE categories:
	  • DL cat.24, up to 42.2 Mbit/s
	  • UL cat.6, up to 5.76 Mbit/s
		Data rate
		• GPRS multi-slot class 33, CS1-CS4:
		  • up to 107.0 kbit/s DL
		  • up to 85.6 kbit/s UL
		• EDGE multi-slot class 33, MCS1-MCS9
		  • up to 296.0 kbit/s DL
		  • up to 236.8 kbit/s UL

Table 2: TOBY-L4 series LTE, 3G and 2G characteristics summary

Module	Region	LTE FDD bands	LTE TDD bands	LTE CA	UMTS FDD bands	GSM bands
TOBY-L4006	North America	12 (700 MHz) 17 (700 MHz) 29 (700 MHz) 13 (750 MHz) 5 (850 MHz) 4 (1700 MHz) 2 (1900 MHz) 7 (2600 MHz)		4 + 17 2 + 13 2 + 17 2 + 29 4 + 5 4 + 4 4 + 13 4 + 29	5 (850 MHz) 4 (1700 MHz) 2 (1900 MHz)	GSM 850 PCS 1900
TOBY-L4106	EMEA, APAC	20 (800 MHz) 8 (900 MHz) 3 (1800 MHz) 1 (2100 MHz) 7 (2600 MHz)	38 (2600 MHz)	3 + 20 7 + 20 3 + 3 3 + 7	8 (900 MHz) 1 (2100 MHz)	E-GSM 900 DCS 1800
TOBY-L4206	APAC, South America	28 (750 MHz) 19 (850 MHz) 5 (850 MHz) 8 (900 MHz) 9 (1800 MHz) 3 (1800 MHz) 1 (2100 MHz) 7 (2600 MHz)		3 + 28 3 + 7 7 + 28 3 + 3 1 + 8 3 + 19 1 + 19	5 (850 MHz) 8 (900 MHz) 1 (2100 MHz)	GSM 850 E-GSM 900 DCS 1800 PCS 1900
TOBY-L4906	China	3 (1800 MHz) 1 (2100 MHz)	39 (1900 MHz) 40 (2300 MHz) 41 (2500 MHz)	3 + 3 40 + 40 41 + 41 39 + 41	8 (900 MHz)[1] 1 (2100 MHz)	E-GSM 900 DCS 1800

Table 3: TOBY-L4 series supported bands[2] and Carrier Aggregation combinations summary

[1] Down-Link Rx diversity not supported on this band
[2] TOBY-L4 series modules support all the E-UTRA channel bandwidths for each operating band according to 3GPP TS 36.521-1 [13].

1.2 Architecture

Figure 1 summarizes the internal architecture of the TOBY-L4 series modules.

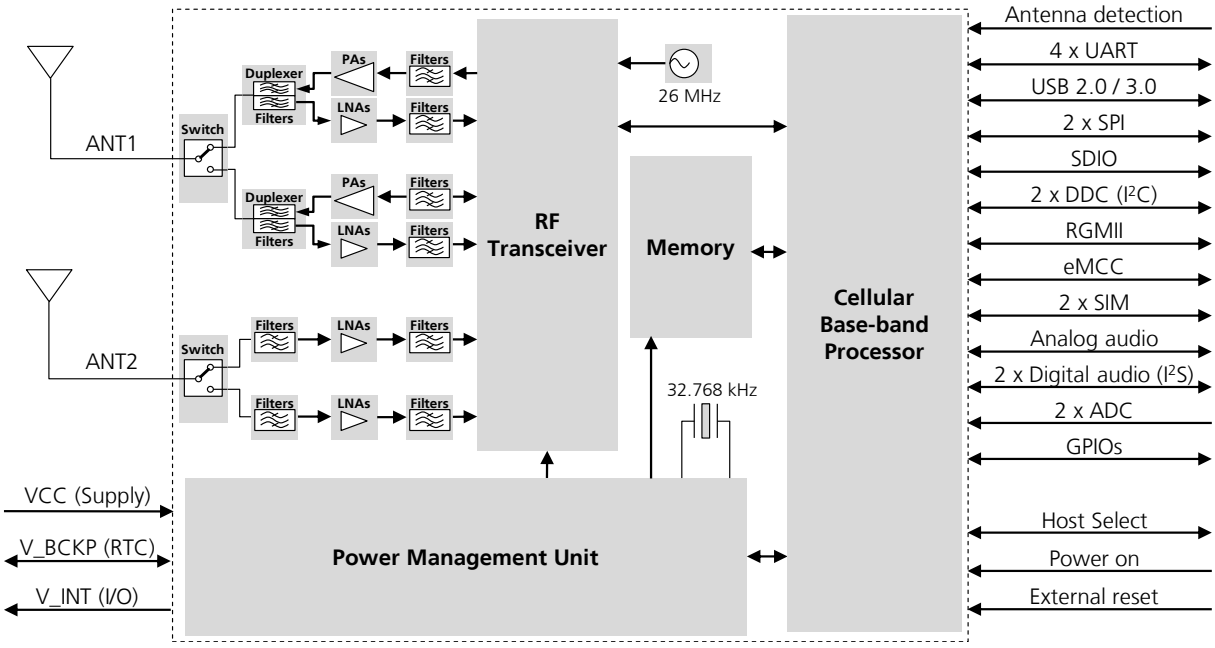

Figure 1: TOBY-L4 series modules simplified block diagram

TOBY-L4 series modules internally consist of the RF, Baseband and Power Management sections described herein with more details than the simplified block diagrams of Figure 1.

RF section

The RF section is composed of an RF transceiver, PAs, LNAs, crystal oscillator, filters, duplexers and RF switches.

The Tx signal is pre-amplified by the RF transceiver, then output to the primary antenna input/output port (**ANT1**) of the module via power amplifier (PA), SAW band pass filters band, specific duplexer and antenna switch.

Dual receiving paths are implemented according to Carrier Aggregation, MIMO, and Receiver Diversity radio technologies supported by the modules as LTE category 6 and HSDPA category 24 User Equipments: incoming signals are received through the primary (**ANT1**) and the secondary (**ANT2**) antenna input ports which are connected to the RF transceiver via specific antenna switch, diplexer, duplexer, LNA, SAW band pass filters.

- RF transceiver performs modulation, up-conversion of the baseband I/O signals for Tx, down-conversion and demodulation of the dual RF signals for Rx. The RF transceiver contains:
  - Single chain high linearity receivers with integrated LNAs for multi-band multi-mode CA operation,
  - Highly linear RF demodulator / modulator capable GMSK, 8-PSK, QPSK, 16-QAM, 64-QAM
  - RF synthesizer,
  - VCO.
- Power Amplifiers (PA) amplify the Tx signal modulated by the RF transceiver
- RF switches connect the primary (**ANT1**) and secondary (**ANT2**) antenna ports to the suitable Tx / Rx path
- SAW duplexers and band pass filters separate the Tx and Rx signal paths and provide RF filtering
- 26 MHz voltage-controlled temperature-controlled crystal oscillator (VC-TCXO) generates the clock reference in active mode or connected mode.

Baseband and power management section

The Baseband and Power Management section is composed of the following main elements:

- A mixed signal ASIC, which integrates
  - Microprocessor for control functions
  - DSP core for cellular Layer 1 and digital processing of Rx and Tx signal paths
  - Memory interface controller
  - Dedicated peripheral blocks for control of the USB, SIM and generic digital interfaces
  - Interfaces to the RF transceiver ASIC
- Memory system, which includes NAND flash and LPDDR2 RAM
- Voltage regulators to derive all the subsystem supply voltages from the module supply input **VCC**
- Voltage source for external use: **V_INT**
- Hardware power on
- Hardware reset
- Low power idle mode support
- 32.768 kHz crystal oscillator to provide the clock reference in the low power idle mode, which can be set by enabling the power saving configuration.

1.3 Pin-out

Table 4 lists the pin-out of the TOBY-L4 series modules, with pins grouped by function.

Function	Pin Name	Pin No	I/O	Description	Remarks
Power	**VCC**	70,71,72	I	Module supply input	**VCC** supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description / requirements. See section 2.2.1 for external circuit design-in.
	GND	2, 30, 32, 44, 46, 69, 73, 74, 76, 78, 79, 80, 82, 83, 85, 86, 88-90, 92-152, 209, 219, 226, 229, 232, 235, 238, 241	N/A	Ground	**GND** pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_BCKP	3	I/O	RTC back-up supply	If the VCC voltage is below the operating range, the RTC block can be externally supplied through the V_BCKP pin. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
	V_INT	5	O	Generic digital interfaces supply output	**V_INT** = 1.8 V (typical) generated by internal DC/DC regulator when the module is switched on. Test-Point for diagnostic access is recommended. See section 1.5.3 for functional description. See section 2.2.3 for external circuit design-in.
System	**PWR_ON**	20	I	Power-on input	Internal 35 kΩ pull-up resistor to internal 1.3 V supply rail. Test-Point for diagnostic access is recommended. See section 1.6.1 for functional description. See section 2.3.1 for external circuit design-in.
	RESET_N	23	I	External reset input	Internal 100 kΩ pull-up resistor to **V_INT**. Test-Point for diagnostic access is recommended. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.
	HOST_SELECT0	26	I/O / I	GPIO / External Interrupt	1.8 V GPIO or External Interrupt configurable by uCPU API. See sections 1.6.4, 1.13 for functional description. See sections 2.3.3, 2.10 for external circuit design-in.
	HOST_SELECT1	62	I/O / I	GPIO / External Interrupt	1.8 V GPIO or External Interrupt configurable by uCPU API. See sections 1.6.4, 1.13 for functional description. See sections 2.3.3, 2.10 for external circuit design-in.
Antennas	**ANT1**	81	I/O	Primary antenna	Main Tx / Rx antenna interface. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description / requirements. See section 2.4 for external circuit design-in.
	ANT2	87	I	Secondary antenna	Rx only for Down-Link CA, MIMO and Rx diversity. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description / requirements. See section 2.4 for external circuit design-in.
	ANT_DET	75	I	Antenna detection	ADC for antenna presence detection function. See section 1.7.2 for functional description. See section 2.4.2 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
SIM0	**VSIM**	59	O	SIM0 supply output	**VSIM** = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	57	I/O	SIM0 data	Data input/output for 1.8 V / 3 V SIM. Internal 4.7 kΩ pull-up to **VSIM**. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	56	O	SIM0 clock	3.9 MHz clock output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	58	O	SIM0 reset	Reset output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
SIM1	**VSIM1**	172	O	SIM1 supply output	**VSIM1** = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM1_IO	178	I/O	SIM1 data	Data input/output for 1.8 V / 3 V SIM. Internal 4.7 kΩ pull-up to **VSIM1**. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM1_CLK	182	O	SIM1 clock	3.9 MHz clock output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM1_RST	177	O	SIM1 reset	Reset output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
USB	**VUSB_DET**	4	I	USB detect input	VBUS (5 V typical) generated by the host must be connected to this pin to enable the module USB device interface. Test-Point for diagnostic / FW update access is recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_D–	27	I/O	USB High-Speed 2.0 diff. transceiver (–)	90 Ω nominal differential impedance (Z_0). 30 Ω nominal common mode impedance (Z_{CM}). Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [3] are part of the USB pin driver and need not be provided externally. Test-Point for diagnostic / FW update access is recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_D+	28	I/O	USB High-Speed 2.0 diff. transceiver (+)	90 Ω nominal differential impedance (Z_0). 30 Ω nominal common mode impedance (Z_{CM}). Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [3] are part of the USB pin driver and need not be provided externally. Test-Point for diagnostic / FW update access is recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_ID	168	I	USB device identification	Pin for ID resistance measurement. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	USB_SSTX+	175	O	USB Super-Speed 3.0 diff. transmitter (+)	90 Ω nominal differential characteristic impedance. Internal series 100 nF capacitor for AC coupling. Compliant with USB Revision 3.0 specification [4]. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_SSTX–	176	O	USB Super-Speed 3.0 diff. transmitter (–)	90 Ω nominal differential characteristic impedance. Internal series 100 nF capacitor for AC coupling. Compliant with USB Revision 3.0 specification [4]. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_SSRX+	170	I	USB Super-Speed 3.0 diff. receiver (+)	90 Ω nominal differential characteristic impedance. Compliant with USB Revision 3.0 specification [4]. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_SSRX–	171	I	USB Super-Speed 3.0 diff. receiver (–)	90 Ω nominal differential characteristic impedance. Compliant with USB Revision 3.0 specification [4]. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
UART0	**RXD**	17	O	UART0 data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24. Test-Point for diagnostic access recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	TXD	16	I	UART0 data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24. Internal active pull-up to **V_INT**. Test-Point for diagnostic access recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	CTS	15	O	UART0 clear to send output	1.8 V output, Circuit 106 (CTS) in ITU-T V.24. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	RTS	14	I	UART0 ready to send input	1.8 V input, Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to **V_INT**. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	DSR	10	I/O / I	GPIO / External Interrupt	1.8 V GPIO or External Interrupt configurable by uCPU API. See sections 1.9.2, 1.13 for functional description. See sections 2.6.1, 2.10 for external circuit design-in.
	RI	11	O / I/O / I	UART0 ring indicator / GPIO / External Interrupt	1.8 V output, Circuit 125 (RI) in ITU-T V.24. Configurable as GPIO or External Interrupt. See sections 1.9.2, 1.13 for functional description. See sections 2.6.1, 2.10 for external circuit design-in.
	DTR	13	I/O / I	GPIO / External Interrupt	1.8 V GPIO or External Interrupt configurable by uCPU API. See sections 1.9.2, 1.13 for functional description. See sections 2.6.1, 2.10 for external circuit design-in.
	DCD	12	I/O / I	GPIO / External Interrupt	1.8 V GPIO or External Interrupt configurable by uCPU API. See sections 1.9.2, 1.13 for functional description. See sections 2.6.1, 2.10 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
UART1	**RXD1**	160	O / O	UART1 data output / SPI1 MOSI	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, alternatively configurable as SPI1 MOSI by uCPU API. See section 1.9.2 / 1.9.3 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.
	TXD1	159	I / I	UART1 data input / SPI1 MISO	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, alternatively configurable as SPI1 MISO by uCPU API. Internal pull-up to **V_INT** enabled when UART1 data input. See section 1.9.2 / 1.9.3 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.
	CTS1	195	O / O	UART1 CTS output / SPI1 Chip Select	1.8 V output, Circuit 106 (CTS) in ITU-T V.24, alternatively configurable as SPI1 Chip Select by uCPU API. See section 1.9.2 / 1.9.3 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.
	RTS1	193	I / O	UART1 RTS input / SPI1 Clock	1.8 V input, Circuit 105 (RTS) in ITU-T V.24, alternatively configurable as SPI1 Clock by uCPU API. Internal pull-up to **V_INT** enabled when UART1 RTS input. See section 1.9.2 / 1.9.3 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.
UART2	**RXD2**	162	O	UART2 data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	TXD2	161	I	UART2 data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24. Internal active pull-up to **V_INT**. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
UART3	**RXD3**	19	O	UART3 data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	TXD3	18	I	UART3 data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24. Internal active pull-up to **V_INT**. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
SPI0	**SPI_MOSI**	174	O	SPI0 Master Output Slave Input	1.8 V, SPI0 data output. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	SPI_MISO	169	I	SPI0 Master Input Slave Output	1.8 V, SPI0 data input. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	SPI_SCLK	179	O	SPI0 Shift Clock	1.8 V, SPI0 clock. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	SPI_CS	173	O	SPI0 Chip Select 0	1.8 V, SPI0 chip select 0. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
I2C0	**SCL**	54	O	I2C0 clock	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
	SDA	55	I/O	I2C0 data	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
I2C1	**SCL1**	54	O	I2C1 clock	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
	SDA1	55	I/O	I2C1 data	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
SDIO	**SDIO_D0**	66	I/O	SDIO serial data [0]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D1	68	I/O	SDIO serial data [1]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D2	63	I/O	SDIO serial data [2]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D3	67	I/O	SDIO serial data [3]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_CLK	64	O	SDIO serial clock	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_CMD	65	I/O	SDIO command	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
Ethernet	**V_ETH**	221	O	Ethernet Interface supply output	Ethernet (RGMII / RMII) interface supply output. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_TX_CLK	29	O	Ethernet Transmission Clock	RGMII: Transmit reference clock (TXC). RMII: Reference clock (REF_CLK). See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_TX_CTL	33	O	Ethernet Transmit Control	RGMII: Control signal for the transmit data (TXEN on TXC rising edge; TXEN xor TXER on TXC falling edge). RMII: Control signal for the transmit data (TX_EN). See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_TXD0	37	O	Ethernet Transmit Data [0]	RGMII: Tx data bit 0 / 4 on TXC rising / falling edges. RMII: Tx data bit 0 in sync with REF_CLK. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_TXD1	36	O	Ethernet Transmit Data [1]	RGMII: Tx data bit 1 / 5 on TXC rising / falling edges. RMII: Tx data bit 1 in sync with REF_CLK. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_TXD2	35	O	Ethernet Transmit Data [2]	RGMII: Tx data bit 2 / 6 on TXC rising / falling edges. RMII: Not used. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_TXD3	34	O	Ethernet Transmit Data [3]	RGMII: Tx data bit 3 / 7 on TXC rising / falling edges. RMII: Not used. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	ETH_RX_CLK	43	I	Ethernet Receive Clock	RGMII: Receive reference clock (RXC). RMII: Not used. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_RX_CTL	42	I	Ethernet Receive Control	RGMII: Control signal for receive data (RXDV on RXC rising edge; RXDV xor RXER on RXC falling edge). RMII: Control signal for receive data, contains carrier sense (CRS) and data valid (RX_DV) information. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_RXD0	38	I	Ethernet Receive Data [0]	RGMII: Rx data bit 0 / 4 on RXC rising / falling edges. RMII: Rx data bit 0 in sync with REF_CLK. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_RXD1	39	I	Ethernet Receive Data [1]	RGMII: Rx data bit 1 / 5 on RXC rising / falling edges. RMII: Rx data bit 1 in sync with REF_CLK. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_RXD2	40	I	Ethernet Receive Data [2]	RGMII: Rx data bit 2 / 6 on RXC rising / falling edges. RMII: Not used. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_RXD3	41	I	Ethernet Receive Data [3]	RGMII: Rx data bit 3 / 7 on RXC rising / falling edges. RMII: Not used. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_INTR	220	I	Ethernet Interrupt Input	Input for the detection of an interrupt event in the PHY. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_MDIO	222	I/O	Ethernet Management Data Input Output	Ethernet management data input / output. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_MDC	223	O	Ethernet Management Data Clock	Ethernet management data clock output. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
eMMC	**V_MMC**	210	O	Multi-Media Card Interface supply output	Embedded Multi-Media / SD Card memory supply. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D0	214	I/O	Multi-Media Card Data [0]	Embedded Multi-Media / SD Card memory data [0]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D1	212	I/O	Multi-Media Card Data [1]	Embedded Multi-Media / SD Card memory data [1]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D2	217	I/O	Multi-Media Card Data [2]	Embedded Multi-Media / SD Card memory data [2]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D3	213	I/O	Multi-Media Card Data [3]	Embedded Multi-Media / SD Card memory data [3]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_CMD	215	I/O	Multi-Media Card Command	Embedded Multi-Media / SD Card memory command. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_CLK	216	O	Multi-Media Card Clock	Embedded Multi-Media / SD Card memory clock. See section 1.10 for functional description. See section 2.7 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	MMC_RST_N	211	O	Multi-Media Card Reset	Embedded Multi-Media / SD Card memory reset. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_CD_N	218	I	Multi-Media Card Detect	Embedded Multi-Media / SD Card detect. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
I2S0	**I2S_TXD**	51	O	I2S0 transmit data	I^2S transmit data output. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S_RXD	53	I	I2S0 receive data	I^2S receive data input. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S_CLK	52	I/O	I2S0 clock	I^2S serial clock. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S_WA	50	I/O	I2S0 word alignment	I^2S word alignment. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
I2S1	**I2S1_TXD**	206	O	I2S1 transmit data	I^2S transmit data output. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S1_RXD	207	I	I2S1 receive data	I^2S receive data input. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S1_CLK	208	I/O	I2S1 clock	I^2S serial clock. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S1_WA	205	I/O	I2S1 word alignment	I^2S word alignment. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
Analog audio	**MIC_BIAS**	231	O	Microphone supply output	Supply output for external microphones. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	MIC_GND	230	I	Microphone analog reference	Local ground for the external microphone. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	MIC1_P	237	I	MIC1 differential analog audio input (+)	MIC1 differential analog audio signal input (positive). See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	MIC1_N	236	I	MIC1 differential analog audio input (–)	MIC1 differential analog audio signal input (negative). See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	MIC2_P	234	I	MIC2 differential analog audio input (+)	MIC2 differential analog audio signal input (positive). See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	MIC2_N	233	I	MIC2 differential analog audio input (–)	MIC2 differential analog audio signal input (negative). See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	SPK_P	227	O	Differential analog audio output (+)	Differential analog audio signal output (positive). See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	SPK_N	228	O	Differential analog audio output (–)	Differential analog audio signal output (negative). See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
ADC	**ADC1**	240	I	ADC input	See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	ADC2	239	I	ADC input	See section 1.12 for functional description. See section 2.9 for external circuit design-in.
GPIO	**GPIO1**	21	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO2	22	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO3	24	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. Configurable as External Interrupt by uCPU API. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO4	25	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. Configurable as SPI0 Chip Select 1 by uCPU API. See sections 1.13, 1.9.3 for functional description. See sections 2.10, 2.6.3 for external circuit design-in.
	GPIO5	60	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO6	61	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO7	248	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO8	247	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
Reserved	**RSVD**	6	N/A	Reserved pin	This pin must be connected to ground. See sections 1.14 and 2.11
	RSVD	1, 7-9, 31, 45, 47-49, 77, 84, 91, 153-158, 163-167, 180, 181, 183-192, 194, 196-202, 224, 225, 242, 243, 244-246	N/A	Reserved pin	Leave unconnected. See sections 1.14 and 2.11

Table 4: TOBY-L4 series module pin definition, grouped by function

1.4 Operating modes

TOBY-L4 series modules have several operating modes. The operating modes are defined in Table 5 and described in detail in Table 6, providing general guidelines for operation.

General Status	Operating Mode	Definition
Power-down	**Not-powered mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-off mode	**VCC** supply within operating range and module is switched off.
Normal Operation	**Idle mode**	Module processor core runs with 32 kHz reference generated by the internal oscillator.
	Active mode	Module processor core runs with 26 MHz reference generated by the internal oscillator.
	Connected mode	RF Tx/Rx data connection enabled and processor core runs with 26 MHz reference.

Table 5: TOBY-L4 series modules operating modes definition

Mode	Description	Transition between operating modes
Not-powered	Module is switched off. Application interfaces are not accessible.	When **VCC** supply is removed, the modules enter not-powered mode. When in not-powered mode, the modules do not switch on by applying **VCC** supply, or by using the **PWR_ON** pin. When in not-powered mode, the modules go to power-off mode by applying **VCC** supply.
Power-off	Module is switched off: normal shutdown by an appropriate power-off event (see 1.6.2). Application interfaces are not accessible.	When the modules are switched off by an appropriate power-off event (see 1.6.2), the modules enter power-off mode from active mode. When in power-off mode, the modules can be switched on by means of the **PWR_ON** pin (see 1.6.1). When in power-off mode, the modules enter not-powered mode by removing **VCC** supply.
Idle	Module is switched on with application interfaces temporarily disabled or suspended to reduce the current consumption (see 1.5.1.5) due to power saving configuration enabled by AT+UPSV command or uCPU API	The modules automatically switch from the active mode to low power idle mode whenever possible if power saving is enabled. The modules wake up from low power idle mode to active mode due to any necessary network related activity, external wake-up through the operating interfaces, or wake-up by means of dedicated uCPU API.
Active	Module is switched on with application interfaces enabled or not suspended: the module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by AT+UPSV command or uCPU API.	When the modules are switched on by an appropriate power-on event (see 1.6.1), the module enter active mode from power-off mode. If power saving configuration is enabled by the AT+UPSV command or uCPU API, the module automatically switches from active to idle mode whenever possible and the module wakes up from idle to active mode in the events listed above (see idle mode to active mode transition description above). When a RF Tx/Rx data or voice connection is initiated or when RF Tx/Rx is required due to a connection previously initiated, the module switches from active to connected mode.
Connected	RF Tx/Rx data connection is in progress. The module is prepared to accept data signals from an external device unless power saving configuration is enabled by AT+UPSV command or uCPU API.	When a data or voice connection is initiated, the module enters connected mode from active mode. Connected mode is suspended if Tx/Rx data or voice is not in progress. In such case, the module automatically switches from connected to active mode and then, if power saving configuration is enabled by the AT+UPSV command or uCPU API, the module automatically switches to idle mode whenever possible. Vice-versa, the module wakes up from idle to active mode and then connected mode if RF Tx/Rx is necessary. When a data connection is terminated, the module returns to the active mode.

Table 6: TOBY-L4 series modules operating modes descriptions

Figure 2 describes the transition between the various operating modes.

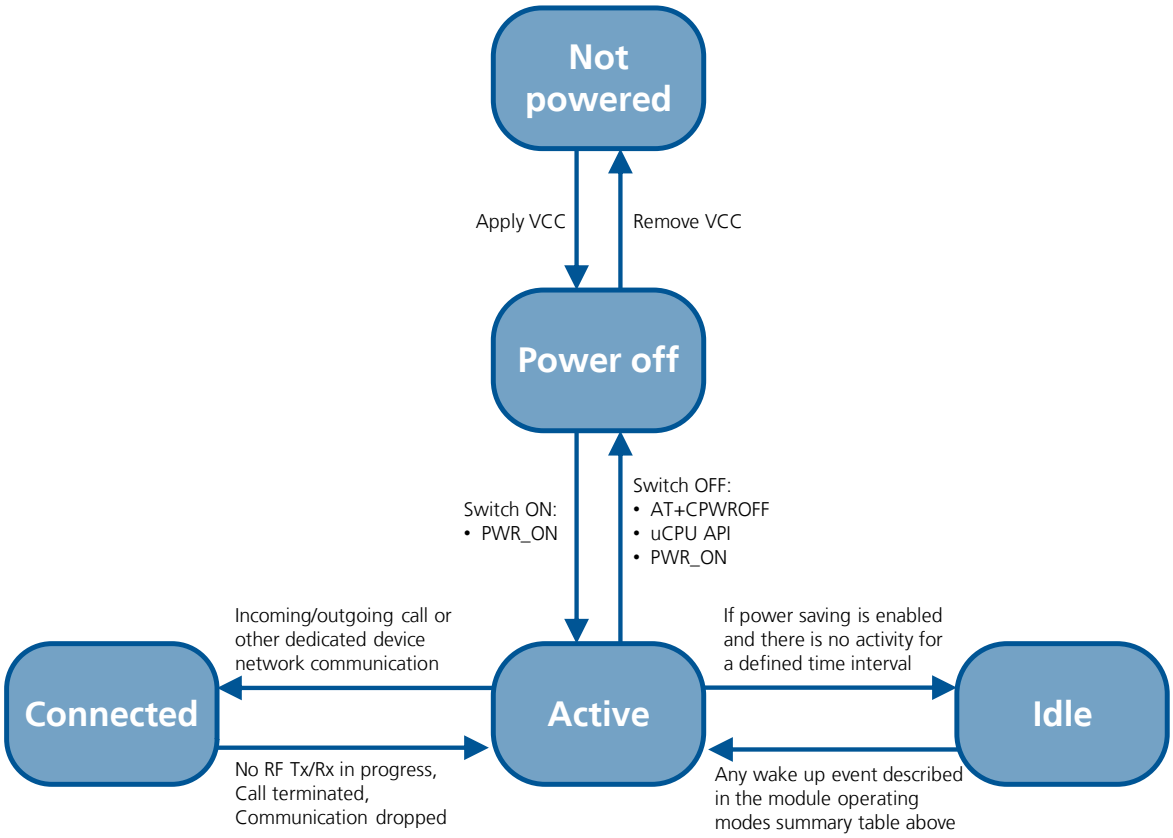

Figure 2: TOBY-L4 series modules operating modes transitions

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, including the Real Time Clock supply, **V_INT** generic digital interfaces supply, **VSIM** SIM card supply, **V_ETH** RGMII interface supply, **V_MMC** eMMC interface supply, and any other internal rail.

During operation, the current drawn by the TOBY-L4 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the pulse of current consumption during GSM transmitting bursts at maximum power level in connected mode (as described in section 1.5.1.2) to the low current consumption during low power idle mode with power saving enabled (as described in section 1.5.1.5).

Figure 3 provides a simplified block diagram of the TOBY-L4 series modules' internal VCC supply routing.

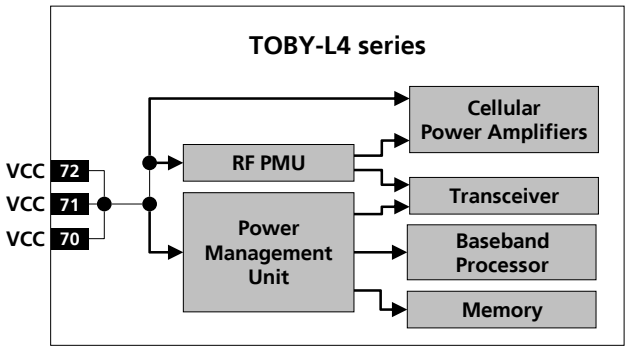

Figure 3: TOBY-L4 series modules' internal VCC supply routing simplified block diagram

1.5.1.1 VCC supply requirements

Table 7 summarizes the requirements for the **VCC** modules supply. See section 2.2.1 for suggestions on how to properly design a **VCC** supply circuit compliant with the requirements listed in Table 7.

The supply circuit affects the RF compliance of the device integrating TOBY-L4 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the requirements summarized in Table 7 are fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.40 V min. / 4.40 V max.	RF performance is guaranteed when **VCC** PA voltage is inside the normal operating range limits. RF performance may be affected when **VCC** PA voltage is outside the normal operating range limits, though the module is still fully functional until the **VCC** voltage is inside the extended operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.00 V min. / 4.50 V max.	**VCC** voltage must be above the extended operating range minimum limit to switch-on the module. The module may switch-off when the **VCC** voltage drops below the extended operating range minimum limit. Operation above **VCC** extended operating range is not recommended and may affect device reliability.
VCC average current	Support with adequate margin the highest averaged **VCC** current consumption value in connected mode conditions	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Sections 1.5.1.2, 1.5.1.3 and 1.5.1.4 describe the current consumption profiles in 2G, 3G and LTE connected modes.
VCC peak current	Support with margin the highest peak **VCC** current consumption value in connected mode conditions	The specified maximum peak of current consumption occurs during the GSM single transmit slot in 850/900 MHz connected mode, in case of a mismatched antenna. Section 1.5.1.2 describes 2G Tx peak/pulse current.
VCC voltage drop during 2G Tx slots	Lower than 400 mV	Supply voltage drop values greater than recommended during 2G TDMA transmission slots directly affect the RF compliance with the applicable certification schemes. Figure 5 describes supply voltage drop during 2G Tx slots.
VCC voltage ripple during 2G/3G/LTE Tx	Noise in the supply must be minimized	High supply voltage ripple values during LTE/3G/2G RF transmissions in connected mode directly affect the RF compliance with applicable certification schemes. Figure 5 describes supply voltage ripple during RF Tx.
VCC under/over-shoot at start/end of Tx slots	Absent or at least minimized	Supply voltage under-shoot or over-shoot at the start or the end of 2G TDMA transmission slots directly affect the RF compliance with the applicable certification schemes. Figure 5 describes supply voltage under/over-shoot

Table 7: Summary of VCC modules supply requirements

1.5.1.2 VCC current consumption in 2G connected mode

When a GSM call is established, the **VCC** module current consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The peak of current consumption during a transmission slot is strictly dependent on the RF transmitted power, which is regulated by the network (the current base station). The transmitted power in the transmit slot is also the more relevant factor for determining the average current consumption.

If the module is transmitting in 2G single-slot mode in the 850 or 900 MHz bands, at the maximum RF power level (approximately 2 W or 33 dBm in the allocated transmit slot/burst) the current consumption can reach an upper peak for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access).

If the module is transmitting in 2G single-slot mode in the 1800 or 1900 MHz bands, the current consumption figures are considerably lower than the one in the low bands, due to the 3GPP transmitter output power specifications.

During a GSM call, current consumption is not so significantly high in receiving or in monitor bursts and is low in the inactive unused bursts.

Figure 4 shows an example of the module current consumption profile versus time in 2G single-slot mode.

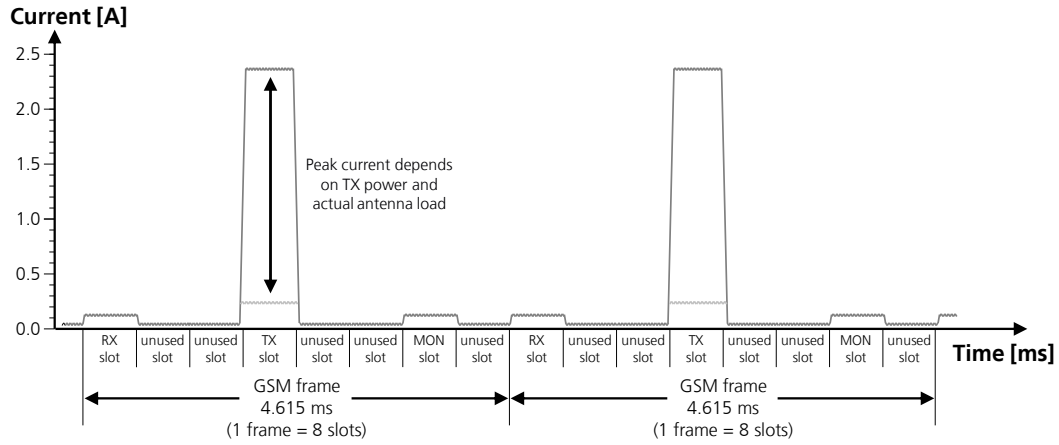

Figure 4: VCC current consumption profile versus time during a 2G single-slot call (1 TX slot, 1 RX slot)

Figure 5 illustrates **VCC** voltage profile versus time during a 2G single-slot call, according to the relative **VCC** current consumption profile illustrated in Figure 4.

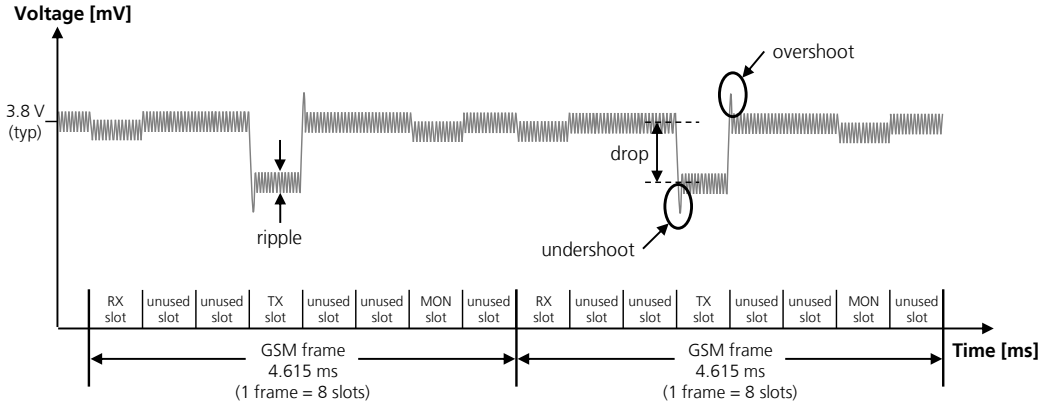

Figure 5: VCC voltage profile versus time during a 2G single-slot call (1 TX slot, 1 RX slot)

When a GPRS connection is established, more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on the network conditions, which set the peak current consumption, but following the 3GPP specifications, the maximum Tx RF power is reduced if more than one slot is used to transmit, so the maximum peak of current is not as high as can be the case with a 2G single-slot call.

If the module transmits in GPRS class 12 in the 850 or 900 MHz bands, at the maximum RF power control level, the current consumption can reach a quite high peak but lower than the one achievable in 2G single-slot mode. This happens for 2.307 ms (width of the 4 transmit slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/2 duty cycle, according to 2G TDMA.

If the module is in GPRS connected mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to 3GPP transmitter output power specifications.

Figure 6 reports the current consumption profiles in GPRS class 12 connected mode, in the 850 or 900 MHz bands, with 4 slots used to transmit and 1 slot used to receive.

It must be noted that the actual current consumption of the module in 2G connected mode depends also on the specific concurrent activities performed by the integrated CPU, beside the actual Tx power and antenna load.

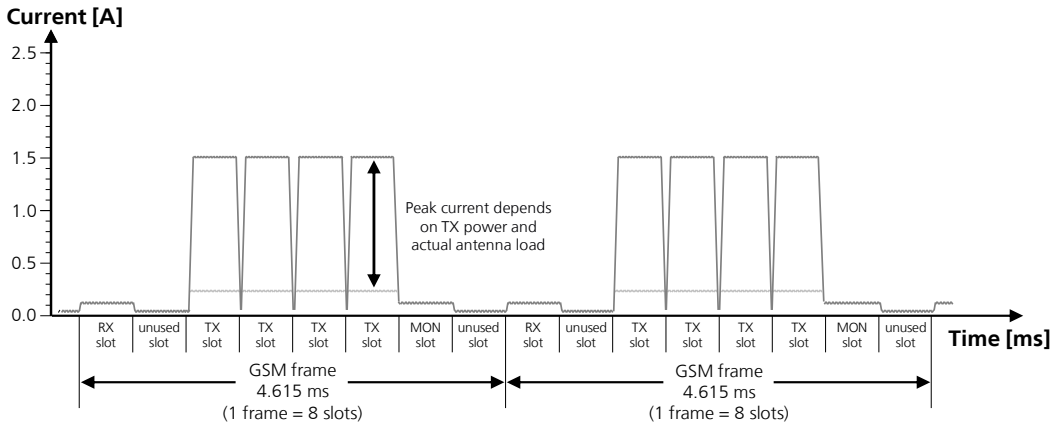

Figure 6: VCC current consumption profile during a 2G GPRS/EDGE multi-slot connection (4 TX slots, 1 RX slot)

For EDGE connections, the VCC current consumption profile is very similar to the GPRS current profile, so the image shown in Figure 6, representing the current consumption profile in GPRS class 12 connected mode, is valid for the EDGE class 12 connected mode as well.

1.5.1.3 VCC current consumption in 3G connected mode

During a 3G connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation with the Wideband Code Division Multiple Access (WCDMA).

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 666 µs, so the rate of power change can reach a maximum rate of 1.5 kHz.

There are no high current peaks as in the 2G connection, since transmission and reception are continuously enabled due to FDD WCDMA implemented in the 3G that differs from the TDMA implemented in the 2G case.

In the worst case scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is considerable. At the lowest output RF power (approximately 0.01 µW or –50 dBm), the current drawn by the internal power amplifier is strongly reduced. The total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 7 shows an example of the current consumption profile of the module in 3G WCDMA/DC-HSPA+ continuous transmission mode.

It must be noted that the actual current consumption of the module in 3G connected mode depends also on the specific concurrent activities performed by the integrated CPU, beside the actual Tx power and antenna load.

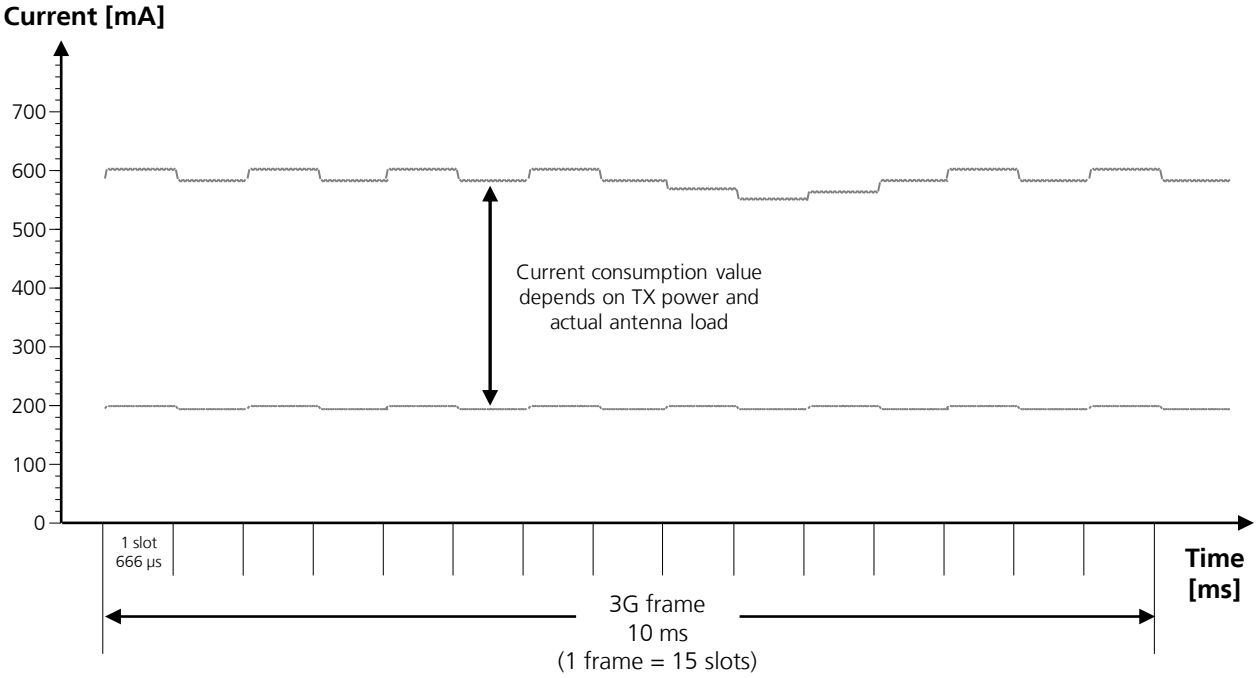

Figure 7: VCC current consumption profile versus time during a 3G connection (TX and RX continuously enabled)

1.5.1.4 VCC current consumption in LTE connected mode

During an LTE connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation used in LTE radio access technology.

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

The current consumption profile is similar to that in 3G radio access technology. Unlike the 2G connection mode, which uses the TDMA mode of operation, there are no high current peaks since transmission and reception are continuously enabled in FDD.

In the worst case scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is considerable. At the lowest output RF power (approximately 0.1 µW or –40 dBm), the current drawn by the internal power amplifier is greatly reduced and the total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 8 shows an example of the module current consumption profile versus time in LTE connected mode.

It must be noted that the actual current consumption of the module in LTE connected mode depends also on the specific concurrent activities performed by the integrated CPU, beside the actual Tx power and antenna load.

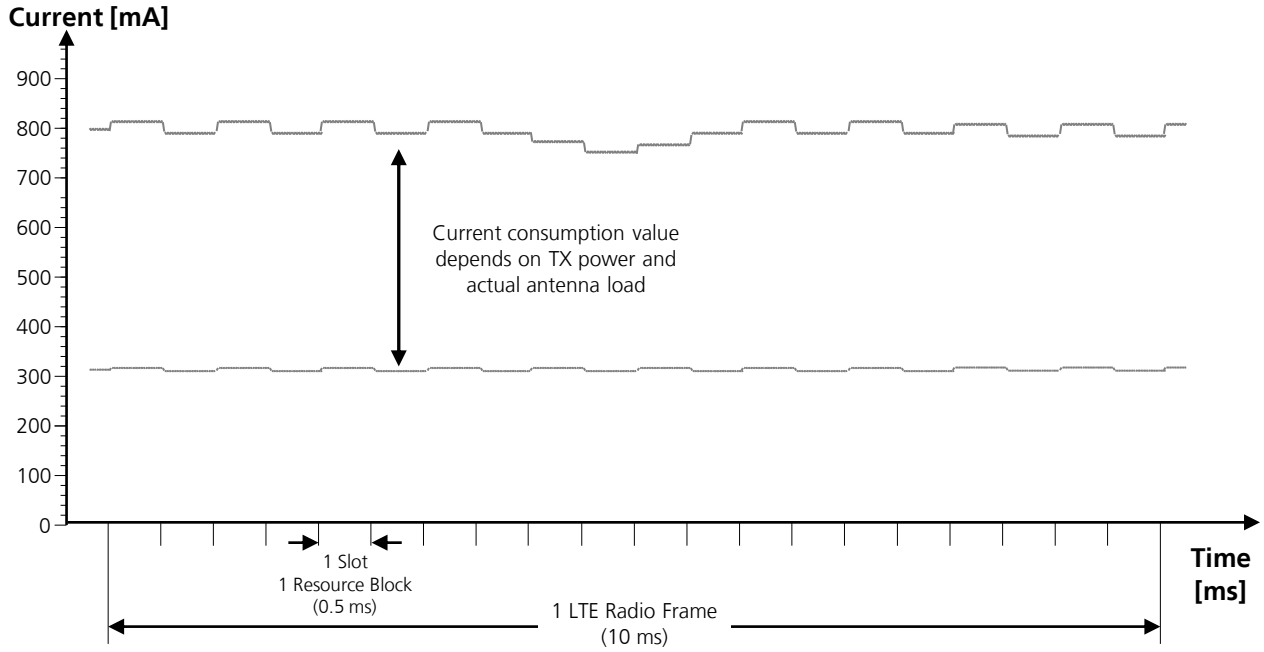

Figure 8: VCC current consumption profile versus time during LTE connection (TX and RX continuously enabled)

1.5.1.5 VCC current consumption in cyclic idle/active mode (power saving enabled)

The power saving configuration is disabled by default, but it can be enabled using the AT+UPSV command (see the u-blox AT Commands Manual [2]) or the dedicated uCPU API. When power saving is enabled, the module automatically enters the low power idle mode whenever possible, reducing current consumption.

During low power idle mode, the module processor runs with 32 kHz reference clock frequency.

When the power saving configuration is enabled and the module is registered or attached to a network, the module automatically enters the low power idle mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance with the 2G/3G/LTE system requirements, even if connected mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active mode to enable the reception of the paging block. In between, the module switches to low power idle mode. This is known as discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 26 MHz used in active mode.

The time period between two paging block receptions is defined by the network. This is the paging period parameter, fixed by the base station through the broadcast channel sent to all users on the same serving cell:

- For 2G radio access technology, the paging period can vary from 470.8 ms (DRX = 2, length of 2 x 51 2G frames = 2 x 51 x 4.615 ms) up to 2118.4 ms (DRX = 9, length of 9 x 51 2G frames = 9 x 51 x 4.615 ms)
- For 3G radio access technology, the paging period can vary from 640 ms (DRX = 6, i.e. length of 2^6 3G frames = 64 x 10 ms) up to 5120 ms (DRX = 9, length of 2^9 3G frames = 512 x 10 ms).
- For LTE radio access technology, the paging period can vary from 320 ms (DRX = 5, i.e. length of 2^5 LTE frames = 32 x 10 ms) up to 2560 ms (DRX = 8, length of 2^8 LTE frames = 256 x 10 ms).

Figure 9 illustrates a typical example of the module current consumption profile when power saving is enabled. The module is registered with the network, automatically enters the low power idle mode and periodically wakes up to active mode to monitor the paging channel for the paging block reception.

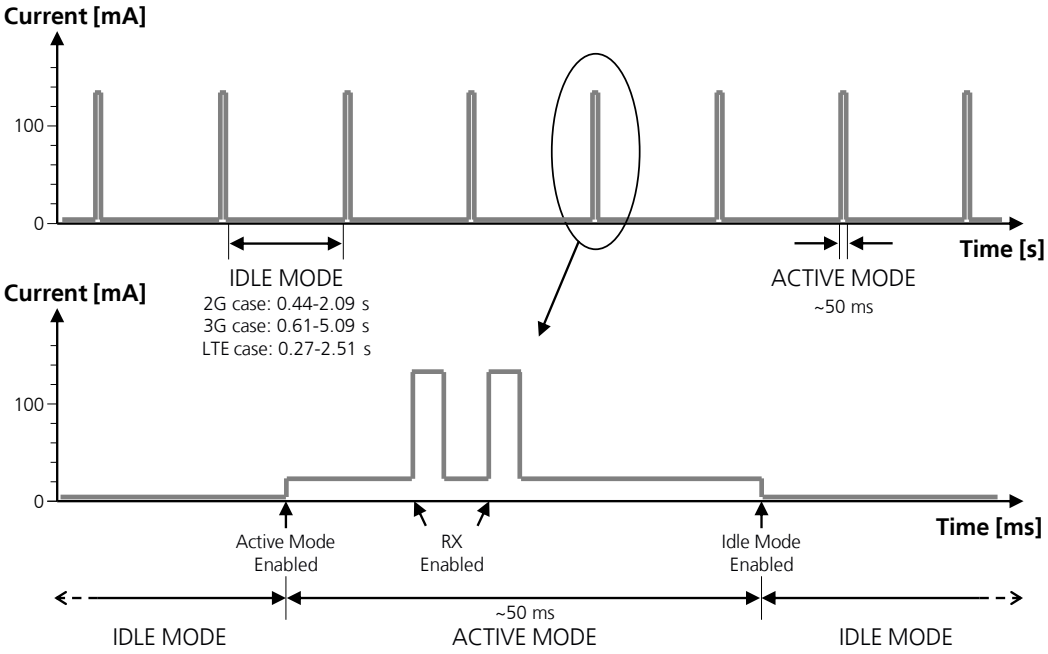

Figure 9: VCC current consumption profile with power saving enabled and module registered with the network: the module is in low-power idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception

1.5.1.6 VCC current consumption in fixed active mode (power saving disabled)

When power saving is disabled, the module does not automatically enter the low power idle mode whenever possible: the module remains in active mode. Power saving configuration is by default disabled. It can also be disabled using the AT+UPSV command (see the u-blox AT Commands Manual [2]) or the dedicated uCPU API.

The module processor core is activated during idle mode, and the 26 MHz reference clock frequency is used. It would draw more current during the paging period than that in the power saving mode.

Figure 10 illustrates a typical example of the module current consumption profile when power saving is disabled. In such a case, the module is registered with the network and while active mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception.

It must be noted that the actual current consumption of the module in active mode depends on the specific concurrent activities performed by the integrated CPU.

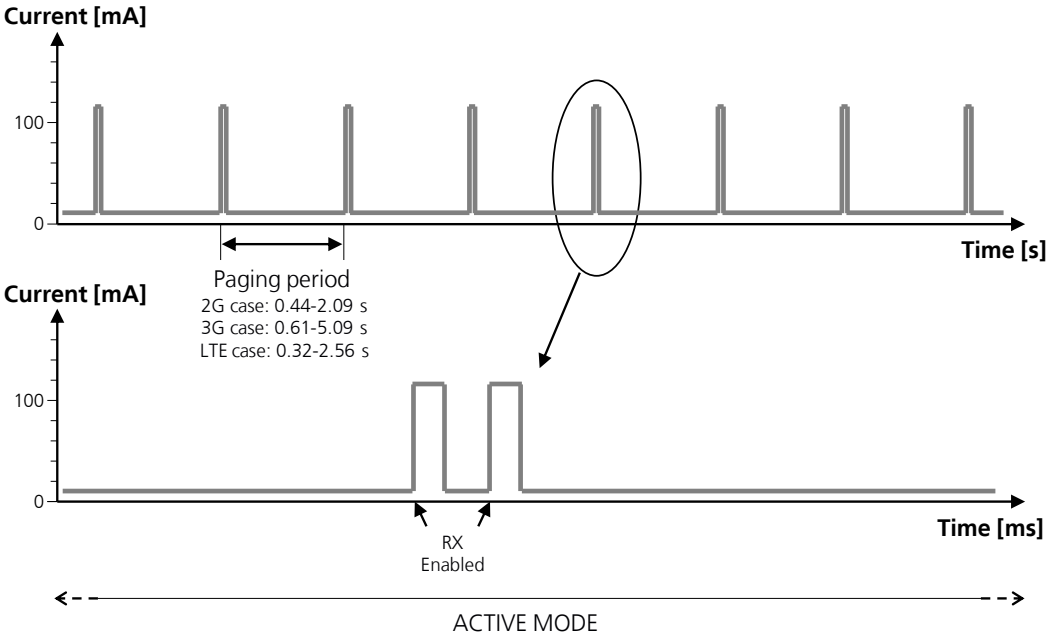

Figure 10: VCC current consumption profile with power saving disabled and module registered with the network: active mode is always held and the receiver is periodically activated to monitor the paging channel for paging block reception

1.5.2 RTC back-up supply (V_BCKP)

When the **VCC** module supply input voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the Real Time Clock (RTC) through the rail available at the **V_BCKP** pin.

The RTC provides the module time reference (date and time) that is used to set the wake-up interval during the low power idle mode periods, and is able to make the programmable alarm functions available.

If the **VCC** module supply input voltage is under the minimum operating limit (e.g. during the not powered mode), the RTC can be externally supplied through the **V_BCKP** pin. This lets the time reference (date and time) run until the **V_BCKP** voltage is within its valid range, even when the main supply is not provided to the module.

Consider that the module cannot switch on if a valid voltage is not present on **VCC** even when the RTC is supplied through **V_BCKP** (meaning that **VCC** is mandatory to switch on the module).

The RTC has a very low current consumption, but is highly temperature dependent.

If **V_BCKP** is left unconnected and the module main supply is not applied to the **VCC** pins, the RTC is supplied from a small bypass capacitor mounted inside the module. However, this small capacitor is not able to provide a long buffering time: within a few milliseconds the voltage on **V_BCKP** will drop below the valid range. This has no impact on cellular connectivity, as all the module functionalities do not rely on date and time settings.

1.5.3 Generic digital interfaces supply output (V_INT)

The **V_INT** output pin of the TOBY-L4 series modules is connected to an internal 1.8 V supply. This supply is internally generated by a switching step-down regulator integrated in the Power Management Unit and it is internally used to source the generic digital I/O interfaces of the cellular module, as illustrated in Figure 11. The output of this regulator is enabled when the module is switched on and it is disabled when the module is switched off.

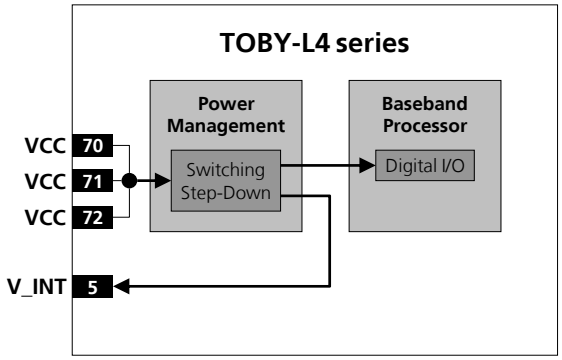

Figure 11: TOBY-L4 series generic digital interfaces supply output (V_INT) simplified block diagram

The switching regulator operates in Pulse Width Modulation (PWM) mode for greater efficiency at high output loads and it automatically switches to Pulse Frequency Modulation (PFM) power save mode for greater efficiency at low output loads.

1.6 System function interfaces

1.6.1 Module power-on

TOBY-L4 series modules can be switched on in the following way:

- Low pulse on the **PWR_ON** pin, which is normally set high by an internal pull-up, for a valid time period, when the applied **VCC** voltage is stable at its nominal value within the valid operating range.

As illustrated in Figure 12, the TOBY-L4 series **PWR_ON** input is equipped with an internal active pull-up resistor to an internal 1.3 V supply rail: the **PWR_ON** input voltage thresholds are different from the other generic digital interfaces, and the line should be driven by an open drain, by an open collector or by a contact switch, without an external pull-up resistor.

Detailed electrical characteristics and specifications are described in TOBY-L4 series Data Sheet [1].

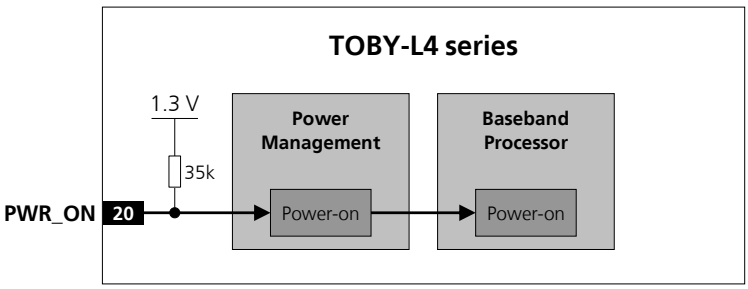

Figure 12: TOBY-L4 series PWR_ON input description

☞ TOBY-L4 series modules do not switch on by applying the **VCC** supply only: a low pulse must be forced on the **PWR_ON** pin when the **VCC** voltage is stable at its nominal value within the valid operating range.

Figure 13 shows the module power-on sequence, describing the following phases:

- The **VCC** module supply is stable at its nominal value within the normal operating range
- The **PWR_ON** input pin is set low for a valid time period, representing the switch-on event.
- All the generic digital pins of the modules are tri-stated until the switch-on of their supply source (**V_INT**): any external signal connected to the generic digital pins must be tri-stated or set low at least until the activation of the **V_INT** supply output to avoid latch-up of circuits and allow a clean boot of the module.
- The **V_INT** generic digital interfaces supply output is enabled by the integrated power management unit.
- The **RESET_N** line rises suddenly to the high logic level due to internal pull-up to **V_INT**.
- The internal reset signal is held low by the integrated power management unit: the baseband processor core and all the digital pins of the modules are held in reset state.
- When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this pins' configuration phase differs within the generic digital interfaces and the USB interface due to host / device enumeration timings (see section 1.9.1).
- The module is fully ready to operate after all interfaces are configured.

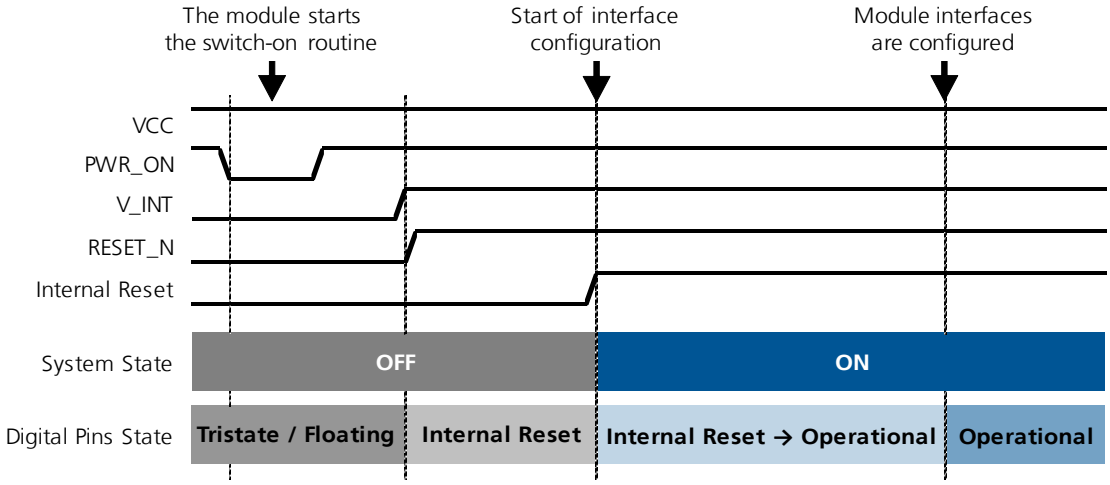

Figure 13: TOBY-L4 series power-on sequence description

☞ The Internal Reset signal is not available on a module pin, but the host application can monitor the **V_INT** pin to sense the start of the TOBY-L4 series module power-on sequence.

☞ Before the switch-on of the generic digital interface supply source (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the module.

☞ Before the TOBY-L4 series module is fully ready to operate, the host application processor should not send any AT command over the AT communication interface (USB) of the module.

☞ The duration of the TOBY-L4 series modules' switch-on routine can vary depending on the application / network settings and any concurrent module activities.

1.6.2 Module power-off

TOBY-L4 series can be properly switched off by:

- AT+CPWROFF command[3] (see the u-blox AT Commands Manual [2])
- uCPU application[4]
- Low pulse on the **PWR_ON** pin, which is normally set high by an internal pull-up, for a valid time period (see the TOBY-L4 series Data Sheet [1]), module normal switch-off: the internal switch-off sequence of the module starts when the external application releases the **PWR_ON** line from the low logic level, after that it has been set low for an appropriate time period.

The methods listed above represent the appropriate normal switch-off events, triggering an appropriate normal switch-off procedure of the module: the current parameter settings are saved in the module's non-volatile memory and a clean network detach is performed.

An abrupt under-voltage shutdown occurs on TOBY-L4 series modules when the **VCC** module supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform a clean network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during TOBY-L4 series modules normal operations: the switch-off procedure must be started by an appropriate switch-off event (see above), and then a suitable **VCC** supply must be held at least until the end of the modules' internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

An abrupt emergency shutdown procedure is triggered on TOBY-L4 series modules when a long enough low pulse is set at the **PWR_ON** input pin (see the TOBY-L4 series Data Sheet [1], module emergency switch-off). In this case, storage of the current parameter settings in the module's non-volatile memory and the clean network detach are not performed.

This abrupt emergency shutdown procedure is intended only for use for emergency, e.g. if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [2], or if shutdown via a normal switch-off procedure fails.

An over-temperature shutdown occurs on TOBY-L4 series modules when the temperature measured within the cellular module reaches a critical range.

[3] Not supported by "00" product version
[4] Not supported by "50" product version

Figure 14 describes the TOBY-L4 series modules' switch-off sequence started by means of the **PWR_ON** input pin, allowing storage of current parameter settings in the module's non-volatile memory and a clean network detach, with the following phases

- A low pulse with the appropriate time duration is applied at the **PWR_ON** input pin, which is normally set high by an internal pull-up: the module starts the switch-off routine when the **PWR_ON** signal is released from the low logical level.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in power-off mode as long as a switch-on event does not occur (i.e. applying a suitable low level pulse to the **PWR_ON** input pin), and enters not-powered mode if the supply is removed from the **VCC** pins.

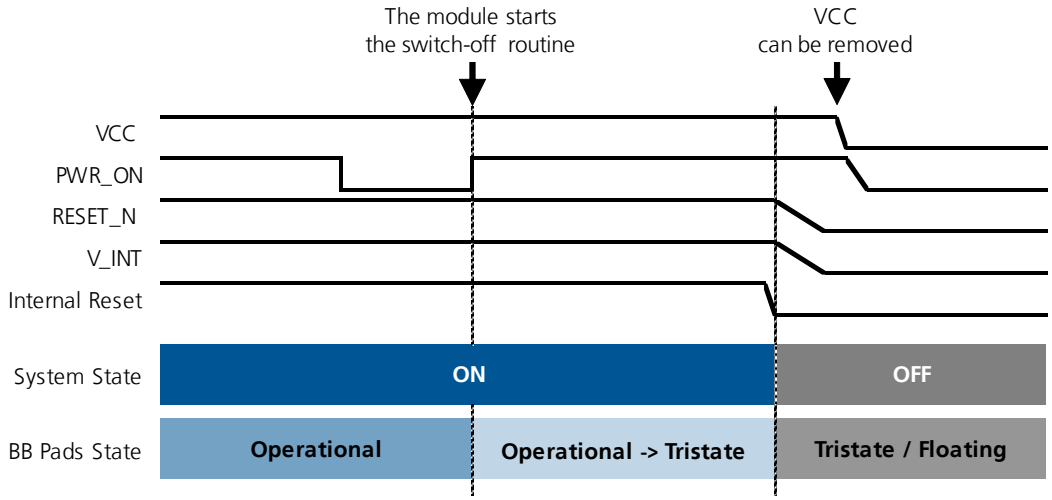

Figure 14: TOBY-L4 series power-off sequence description

The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the end of the power-off sequence.

The **VCC** supply can be removed only after the end of the module internal switch-off routine, i.e. only after that the **V_INT** voltage level has gone low.

The duration of each phase in the TOBY-L4 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

TOBY-L4 series modules can be properly reset (rebooted) by:

- AT+CFUN command[5] (see the u-blox AT Commands Manual [2])
- uCPU application[6]

The methods listed above represent appropriate reset (reboot) events, triggering an appropriate "internal" or "software" reset of the module: the current parameter settings are saved in the module's non-volatile memory and a clean network detach is performed.

An abrupt hardware reset occurs on TOBY-L4 series modules when a low level is applied on the **RESET_N** input pin. In this case, the current parameter settings are not saved in the module's non-volatile memory and a clean network detach is not performed.

☞ It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET_N** input during modules normal operation: the **RESET_N** line should be set low only if reset via AT commands or if the uCPU application fails.

As illustrated in Figure 15, the **RESET_N** input pins are equipped with an internal pull-up to the **V_INT** supply.

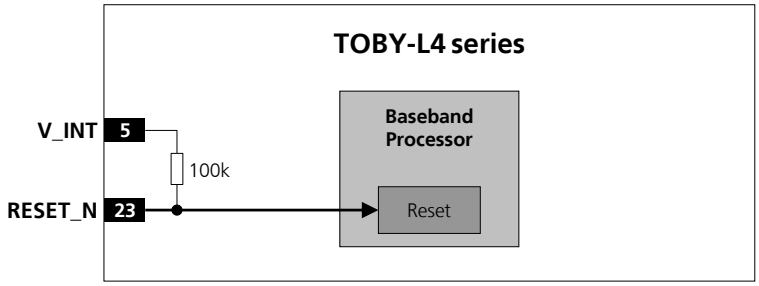

Figure 15: TOBY-L4 series RESET_N input equivalent circuit description

1.6.4 Module / host configuration selection

☞ Host Select pins are not supported by the "50" product version.

TOBY-L4 series modules include two 1.8 V digital pins (**HOST_SELECT0**, **HOST_SELECT1**), which can be configured for External Interrupt detection or as GPIO by means of the uCPU API.

[5] Not supported by "00" product version
[6] Not supported by "50" product version

1.7 Antenna interfaces

1.7.1 Antenna RF interfaces (ANT1 / ANT2)

TOBY-L4 series modules provide two RF interfaces for connecting the external antennas:

- The **ANT1** represents the primary RF input/output for transmission and reception of LTE/3G/2G RF signals.

  The **ANT1** pin has a nominal characteristic impedance of 50 Ω and must be connected to the primary Tx / Rx antenna through a 50 Ω transmission line to allow clean RF transmission and reception.
- The **ANT2** represents the secondary RF input for the reception of the RF signals for CA, MIMO and Rx diversity configurations supported by TOBY-L4 series modules as a required feature for LTE category 6 UEs.

  The **ANT2** pin has a nominal characteristic impedance of 50 Ω and must be connected to the secondary Rx antenna through a 50 Ω transmission line to allow for clean RF reception.

1.7.1.1 Antenna RF interfaces requirements

Table 8, Table 9 and Table 10 summarize the requirements for the antennas' RF interfaces (**ANT1** / **ANT2**). See section 2.4.1 for suggestions on how to correctly design antennas circuits which are compliant with these requirements.

The antenna circuits affect the RF compliance of the device integrating TOBY-L4 series modules with the applicable required certification schemes (for more details see section 4). Compliance is guaranteed if the antenna RF interfaces (ANT1 / ANT2) requirements summarized in Table 8, Table 9 and Table 10 are fulfilled.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT1** port.
Frequency Range	See the TOBY-L4 series Data Sheet [1]	The required frequency range of the antenna connected to the **ANT1** port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT1** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT1** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT1** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum Gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT1** port must not exceed the herein stated value to comply with regulatory agencies' radiation exposure limits.
Input Power	> 33 dBm (> 2 W)	The antenna connected to the **ANT1** port must support with adequate margin the maximum power transmitted by the modules.

Table 8: Summary of primary Tx/Rx antenna RF interface (ANT1) requirements

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT2** port.
Frequency Range	See the TOBY-L4 series Data Sheet [1]	The required frequency range of the antennas connected to **ANT2** port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT2** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT2** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT2** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as the TIS, specified by applicable related certification schemes.

Table 9: Summary of secondary Rx antenna RF interface (ANT2) requirements

Item	Requirements	Remarks
Efficiency imbalance	< 0.5 dB recommended < 1.0 dB acceptable	The radiation efficiency imbalance is the ratio of the primary (**ANT1**) antenna efficiency to the secondary (**ANT2**) antenna efficiency: the efficiency imbalance is a measure of how much better an antenna receives or transmits compared to the other antenna. The radiation efficiency of the secondary antenna needs to be roughly the same as the radiation efficiency of the primary antenna for good RF performance.
Envelope Correlation Coefficient	< 0.4 recommended < 0.5 acceptable	The Envelope Correlation Coefficient (ECC) between the primary (**ANT1**) and the secondary (**ANT2**) antenna is an indicator of 3D radiation pattern similarity between the two antennas: low ECC results from antenna patterns with radiation lobes in different directions. The ECC between the primary and secondary antennas needs to be low enough to comply with the radiated performance requirements specified by related certification schemes.
Isolation	> 15 dB recommended > 10 dB acceptable	The antenna to antenna isolation is the loss between the primary (**ANT1**) and the secondary (**ANT2**) antenna: high isolation results from low coupled antennas. The isolation between primary and secondary antenna needs to be high for good RF performance.

Table 10: Summary of primary (ANT1) and secondary (ANT2) antennas relationship requirements

1.7.2 Antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it.

The **ANT_DET** pin generates a DC current and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.2 for the antenna detection circuit on the application board and the diagnostic circuit in the antenna assembly design-in guidelines.

1.8 SIM interfaces

1.8.1 SIM interfaces

TOBY-L4 series modules provide two SIM interfaces for the direct connection of two external SIM cards/chips, which can be used alternatively (only one SIM at a time can be used for network access):

- SIM0 interface (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins), which is enabled by default
- SIM1 interface (**VSIM1**, **SIM1_IO**, **SIM1_CLK**, **SIM1_RST** pins), which can be alternatively enabled by dedicated AT command[7] (see the u-blox AT Commands Manual [2]), or by means of the uCPU application[8].

Both 1.8 V and 3 V SIM types are supported by the SIM interfaces. Activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented according to ISO-IEC 7816-3 specifications.

High-speed SIM/ME interface and the PPS procedure for baud-rate selection is implemented according to the values proposed by the SIM card/chip.

Both the **VSIM** supply output and the **VSIM1** supply output provide internal short circuit protection to limit the start-up current and protect the SIM from short circuits.

1.8.2 SIM detection interface

The **GPIO5** pin of TOBY-L4 series modules can be configured to detect the mechanical / physical presence of an external SIM card connected to the SIM0 interface. The pin can sense SIM card presence as intended to be properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card not present
- High logic level at **GPIO5** input pin is recognized as SIM card present

The SIM card detection function provided by **GPIO5** pin is an optional feature that can be implemented / used or not according to the application requirements: an Unsolicited Result Code (URC) is generated each time that there is a change of status.

The optional function "SIM card hot insertion/removal" can be additionally configured on the **GPIO5** pin, in order to enable / disable the SIM0 interface upon detection of external SIM card physical insertion / removal.

[7] Not supported by the "00" product version
[8] Not supported by the "50" product version

1.9 Data communication interfaces

TOBY-L4 series modules provide the following serial communication interfaces:

- USB interface (see section 1.9.1):
  - USB Super-Speed 3.0 compliant interface[9], with the module acting as a USB device:
  - USB High-Speed 2.0 compliant interface, with the module acting as a USB device or host[11], providing:
    - AT command[10]
    - Data communication
    - Ethernet-over-USB virtual channel (CDC-NCM)
    - FW upgrades
    - Trace log capture (diagnostic purposes)
    - Auxiliary channel to tune internal audio parameters using a dedicated external tool
    - Linux console for uCPU API development and debug[11]
    - Communication with external processor / device by means of uCPU API[11]
- Up to four UART interfaces (see section 1.9.2):
  - UART0 interface, providing:
    - Communication with external serial devices by means of uCPU API[11]
    - Trace log capture (diagnostic purposes)
    - Ring Indicator functionality
  - UART1 interface[12], providing:
    - Communication with external serial devices by means of uCPU API[11]
  - UART2 interface, providing:
    - Communication with external serial devices by means of uCPU API[11]
  - UART3 interface, providing:
    - Linux console for uCPU API development and debug[11]
- Up to two SPI interfaces[11] (see section 1.9.3):
  - SPI0 interface, with the module acting as SPI master, providing:
    - Communication with external SPI slave devices by means of uCPU API
  - SPI1 interface[12], with the module acting as SPI master, providing:
    - Communication with external SPI slave devices by means of uCPU API
- Two DDC I^2C bus compatible interfaces[11] (see section 1.9.4):
  - I2C0 interface, with the module acting as I^2C master, providing:
    - Communication with u-blox GNSS positioning chips / modules
    - Communication with external I^2C slave devices by means of uCPU API
  - I2C1 interface, with the module acting as I^2C master, providing:
    - Communication with external I^2C slave devices by means of uCPU API
- SDIO interface[11], with the module acting as SDIO host, providing (see section 1.9.5):
    - Communication with compatible u-blox short range radio modules by means of uCPU API
    - Communication with external SDIO devices by means of uCPU API
- RGMII / RMII interface[11], with the module acting as Ethernet MAC, providing (see section 1.9.6):
    - Ethernet connection enabled by means of uCPU API, through the external Ethernet PHY

[9] Supported by future FW versions
[10] Not supported by the "00" product version
[11] Not supported by the "50" product version
[12] UART1 and SPI1 interfaces can be used alternatively, in mutually exclusive way, by means of uCPU API

1.9.1 USB interface

☞ The USB Super-Speed 3.0 compliant interface will be supported by future firmware versions.

☞ The USB High-Speed 2.0 host role is not supported by the "50" product versions.

TOBY-L4 series modules include a USB Super-Speed 3.0 compliant interface, supporting up to 5 Gbit/s data rate, and also including a USB High-Speed 2.0 compliant interface, supporting up to 480 Mbit/s data rate.

The USB High-Speed 2.0 compliant interface consists of the following pins:

- **USB_D+/USB_D–**, USB High-Speed differential transceiver data lines as per USB 2.0 specification [3]
- **VUSB_DET** input pin, which senses the VBUS USB supply presence (nominally 5 V at the source) to detect the host connection and enable the USB 2.0 interface with the module acting as a USB device.

  Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input pin, which senses the VBUS USB supply voltage presence and absorbs few microamperes.
- **USB_ID** pin, available for USB ID resistance measurement:
  - if the **USB_ID** pin is externally connected to GND, then the module acts as a USB host
  - if the **USB_ID** pin is externally left unconnected (floating), then the module acts as a USB device

The USB High-Speed 2.0 compliant interface, with the module acting as a USB device, provides:

- AT command[13]
- Data communication
- Ethernet-over-USB virtual channel
- Trace log capture (diagnostic purposes)
- Auxiliary channel to tune internal audio parameters using a dedicated external tool
- Linux console for uCPU applications development and debug[14]
- FW upgrades

The module, acting as a USB device, identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor according to the USB 2.0 specifications [3].

If the module, acting as a USB device, is connected to the USB host before the module is switched on, or if the module is reset (rebooted) with the USB connected to the host, the VID and PID are automatically updated during the boot of the module. First, the VID and PID are the following:

- VID = 0x8087
- PID = 0x0801

This VID and PID combination identifies a USB profile where no USB function described above is available: the AT commands must not be sent to the module over the USB profile identified by this VID and PID combination.

Then, after a time period (depending on the host / device enumeration timings), the VID and PID are updated to the one where the normal operative functions (AT, Data, Ethernet-over-USB, Trace, Linux console) are available. VID and PID for normal operative functions are the following:

- VID = 0x1546
- PID = 0x1010

The USB High-Speed 2.0 compliant interface, with the module acting as USB host (OTG), provides:

- Communication with external device by means of the uCPU application

[13] Not supported by the "00" product version
[14] Not supported by the "50" product version

The USB Super-Speed 3.0 compliant interface as per USB 3.0 specifications [4], with the module acting as a USB device, consists of the following additional pins:

- **USB_SSTX+/USB_SSTX–**, USB Super-Speed differential transmitter data lines
- **USB_SSRX+/USB_SSRX–**, USB Super-Speed differential receiver data lines

USB drivers are available for Windows operating system platforms. TOBY-L4 series modules are compatible with standard Linux/Android USB kernel drivers.

1.9.2 UART interfaces

☞ UART interfaces are not supported by the "50" product version, except for trace logging (diagnostic purposes) and Ring Indicator functionality over the UART0 interface.

1.9.2.1 UART0 interface

The UART0 Universal Asynchronous Receiver/Transmitter serial interface has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), providing:

- Communication with external devices by means of the uCPU API, over the following pins:
  - **RXD** module output and **TXD** module input data lines
  - **CTS** module output and **RTS** module input hardware flow control lines
- Trace logging (diagnostic purpose), over the following pins:
  - **RXD** module output and **TXD** module input data lines
- Ring Indicator functionality, over the following pin:
  - **RI** module output line

The UART0 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format (illustrated in Figure 16), and with hardware flow control output (**CTS** line) driven to the OFF state when the module is not prepared to accept data by the UART0 interface.

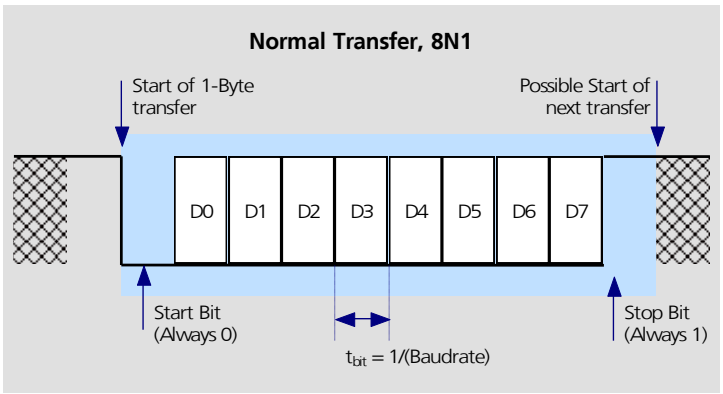

Figure 16: Description of UART 8N1 frame format (8 data bits, no parity, 1 stop bit)

The **RI** line can notify an incoming call: the **RI** line is switched from the OFF state to the ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 17), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

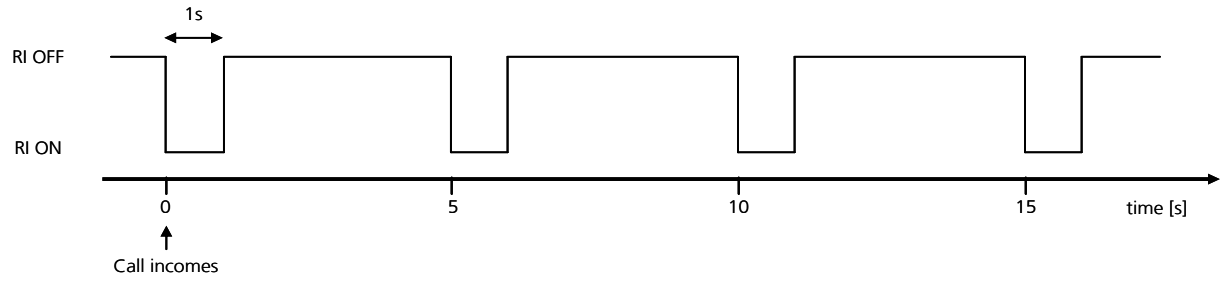

Figure 17: RI behavior during an incoming call

The **RI** output line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 18), if the feature is enabled by the AT+CNMI command (see the u-blox AT Commands Manual [2]).

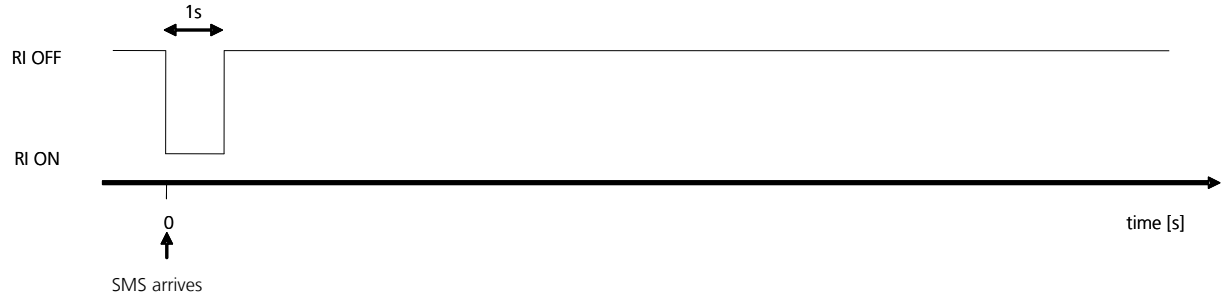

Figure 18: RI behavior at SMS arrival

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.
For SMS arrival, if several events coincidently occur or in quick succession, each event independently triggers the **RI** line, although the line will not be deactivated between each event. As a result, the **RI** line may stay to ON for more than 1 s, if an incoming call is answered within less than 1 s (with ATA or if auto-answering is set to ATS0=1) then the **RI** line is set to OFF earlier, so that:

- **RI** line monitoring cannot be used by the DTE to determine the number of received SMSs.
- For multiple events (incoming call plus SMS received), the **RI** line cannot be used to discriminate the two events, but the DTE must rely on subsequent URCs and interrogate the DCE with the suitable commands.

The **RI** line can additionally notify URCs and/or incoming data, if the feature is enabled by the specific AT+URING command (for more details, see the u-blox AT Commands Manual [2]): the **RI** line is asserted when one of the configured events occur and it remains asserted for 1 s unless another configured event will happen, with the same behavior illustrated in Figure 18.

The **DTR**, **DSR**, **DCD** and **RI** pins can be alternatively configured for External Interrupt detection or as GPIO by means of the uCPU API. The **RI** pin can be alternatively configured as GPIO by an AT command.

1.9.2.2 UART1 interface

The UART1 Universal Asynchronous Receiver/Transmitter serial interface, with CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), can operate as a

- serial interface for communication with external devices by means of the uCPU API, with the following pins:
  - **RXD1** module output and **TXD1** module input data lines
  - **CTS1** module output and **RTS1** module input hardware flow control lines

The UART1 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format (illustrated in Figure 16), and with hardware flow control output (**CTS1** line) driven to the OFF state when the module is not prepared to accept data by the UART1 interface.

The UART1 interface can be alternatively, in mutually exclusive way, configured as SPI1 interface by means of the uCPU API, for communication with external devices with the following pins:

- **RXD1** pin, alternatively configured as SPI1 Master Output Slave Input (module output)
- **TXD1** pin, alternatively configured as SPI1 Master Input Slave Output (module input)
- **CTS1** pin, alternatively configured as SPI1 Chip Select (module output)
- **RTS1** pin, alternatively configured as SPI1 Clock (module output)

1.9.2.3 UART2 interface

The UART2 Universal Asynchronous Receiver/Transmitter serial interface, with CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), can operate as a

- serial interface for communication with external devices by means of the uCPU API, with the following pins:
  - **RXD2** module output and **TXD2** module input data lines

The UART2 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format (illustrated in Figure 16).

1.9.2.4 UART3 interface

The UART3 Universal Asynchronous Receiver/Transmitter serial interface, with CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), can operate as

- Linux console for uCPU API development and debug, with the following pins:
  - **RXD3** module output and **TXD3** module input data lines

The UART3 interface can operate at 9.6 kbit/s, 19.2 kbit/s, 38.4 kbit/s, 57.6 kbit/s, 115.2 kbit/s, 230.4 kbit/s, 460.8 kbit/s, 921.6 kbit/s, 3 Mbit/s, 3.25 Mbit/s and 6.5 Mbit/s baud rates, with 8N1 frame format (illustrated in Figure 16).

1.9.3 SPI interfaces

☞ SPI interfaces are not supported by the "50" product version.

1.9.3.1 SPI0 interface

The SPI0 1.8 V Serial Peripheral Interface supports communication with an external SPI slave devices, with the module acting as SPI master, by means of the uCPU API, with the following pins:

- **SPI_MOSI** pin, SPI0 Master Output Slave Input (module output)
- **SPI_MISO** pin, SPI0 Master Input Slave Output (module input)
- **SPI_SCLK** pin, SPI0 Serial Clock (module output)
- **SPI_CS** pin, SPI0 Chip Select 0 (module output)
- **GPIO4** pin, alternatively configured as SPI0 Chip Select 1 (module output)

The SPI0 Serial Clock signal can be configured to different operating frequencies: 26 MHz (maximum frequency), and 26 / n MHz, where n is 2, 3, 4, etc.

1.9.3.2 SPI1 interface

The SPI1 1.8 V Serial Peripheral Interface supports communication with an external SPI slave devices, with the module acting as SPI master, by means of the uCPU API, with the following UART1 pins configured as alternative functions, in a mutually exclusive way:

- **RXD1** pin, alternatively configured as SPI1 Master Output Slave Input (module output)
- **TXD1** pin, alternatively configured as SPI1 Master Input Slave Output (module input)
- **RTS1** pin, alternatively configured as SPI1 Serial Clock (module output)
- **CTS1** pin, alternatively configured as SPI1 Chip Select (module output)

The SPI1 Serial Clock signal can be configured at various operating frequencies: 26 MHz (maximum frequency), and 26 / n MHz, where n is 2, 3, 4, etc.

1.9.4 DDC (I²C) interfaces

☞ DDC (I²C) interfaces are not supported by the "50" product version.

1.9.4.1 I2C0 interface

The **SDA** and **SCL** pins represent the I2C0 1.8 V I²C bus compatible Display Data Channel (DDC) interface, with the module acting as I²C master, available for

- communication with u-blox GNSS chips / modules
- communication with other external I²C devices by means of the uCPU API

The I2C0 interface pins of the module are open drain outputs conforming to the I²C bus specifications [6], supporting up to 100 kbit/s data rate in Standard mode, and up to 400 kbit/s data rate in Fast mode. External pull-up resistors to suitable 1.8 V supply (e.g. **V_INT**) are required for operations.

u-blox has implemented special features to ease the design effort required for the integration of a u-blox cellular module with a u-blox GNSS receiver.

Combining a u-blox cellular module with a u-blox GNSS receiver allows designers to have full access to the positioning receiver directly via the cellular module: it relays control messages to the GNSS receiver via a dedicated DDC (I²C) interface. An interface connected to the positioning receiver is not necessary: the cellular module allows full control of the GNSS receiver.

The modules provide embedded GNSS aiding that is a set of specific features developed by u-blox to improve the cellular / GNSS system power consumption and the GNSS performance, decreasing the Time-To-First-Fix (TTFF), thus allowing to calculate the position in a shorter time with higher accuracy.

1.9.4.2 I2C1 interface

The **SDA** and **SCL** pins represent the I2C1 I²C bus compatible Display Data Channel (DDC) interface, with the module acting as the I²C master, available for

- communication with other external I²C devices by means of uCPU API

The I2C1 interface pins of the module are open drain outputs conforming to the I²C bus specifications [6], supporting up to 100 kbit/s data rate in Standard mode, and up to 400 kbit/s data rate in Fast mode. External pull-up resistors to a suitable 1.8 V supply (e.g. **V_INT**) are required for operations.

1.9.5 SDIO interface

☞ SDIO interface is not supported by the "50" product version.

TOBY-L4 series modules include a 4-bit Secure Digital Input Output interface (**SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD**), where the module acts as an SDIO host controller designed to

- communicate with compatible u-blox short range radio communication modules by means of the uCPU API
- communicate with external SDIO devices by means of the uCPU API

The SDIO interface supports up to 832 Mbit/s data rate with SD 3.0 SDR104 mode at 208 MHz clock frequency.

Combining a u-blox cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary. The cellular module allows a full control of the Wi-Fi module, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface.

u-blox has implemented special features in the cellular modules to ease the design effort for the integration of a u-blox cellular module with a u-blox short range Wi-Fi module to provide Router functionality.

1.9.6 RGMII interface

☞ RGMII interface is not supported by the "50" product version.

TOBY-L4 series modules include an Ethernet Media Access Control (MAC) block supporting up to 1 Gbit/s data rate via a Reduced Gigabit Media-Independent Interface compliant with the RGMII Version 1.3 specification [7] and the RMII Revision 1.2 specification [8].

The module represents an Ethernet MAC controller, which can be connected to an external Ethernet physical transceiver (PHY) chip for communication with a remote processor over Ethernet.

The following signals are provided for communication and management of an external Ethernet PHY:

- **V_ETH** Interface supply output
- **ETH_TX_CLK** RGMII Transmit reference Clock (TXC) output
  RMII Reference Clock (REF_CLK) output
- **ETH_TX_CTL** RGMII Transmit Control output, driven on both edges of the Transmit clock (TXC)
  RMII Transmit Enable (TXEN) output, synchronous with Reference Clock (REF_CLK)
- **ETH_TXD0** RGMII / RMII Transmit Data [0], from MAC to PHY (module output)
- **ETH_TXD1** RGMII / RMII Transmit Data [1], from MAC to PHY (module output)
- **ETH_TXD2** RGMII Transmit Data [2], from MAC to PHY (module output)
- **ETH_TXD3** RGMII Transmit Data [3], from MAC to PHY (module output)
- **ETH_RX_CLK** RGMII Receive reference Clock (RXC) input
- **ETH_RX_CTL** RGMII Receive Control input, sampled on both edges of the Receive clock (RXC)
  RMII Carrier Sense (CRS) / Receive Data Valid (RX_DV) input
- **ETH_RXD0** RGMII / RMII Receive Data [0], from PHY to MAC (module input)
- **ETH_RXD1** RGMII / RMII Receive Data [1], from PHY to MAC (module input)
- **ETH_RXD2** RGMII Receive Data [2], from PHY to MAC (module input)
- **ETH_RXD3** RGMII Receive Data [3], from PHY to MAC (module input)
- **ETH_INTR** Ethernet Interrupt Input, from PHY to MAC (module input)
  When this signal is high, it indicates an interrupt event in the PHY
- **ETH_MDIO** Management Data Input Output, bidirectional signal (module input/output)
- **ETH_MDC** Management Data Clock, from MAC to PHY (module output)

1.10 eMMC interface

☞ The eMMC interface is not supported by the "50" product version.

TOBY-L4 series modules include a 4-bit embedded Multi-Media Card interface compliant with the JESD84-B451 Embedded Multimedia Card (eMMC) Electrical Standard 4.51 [9].

The following signals are provided for connection and management of an external eMMC / SD memory by means of the uCPU API:

- **V_MMC** Interface supply output (module output)
- **MMC_D0** Multi-Media Card Data [0], bidirectional signal (module input/output)
- **MMC_D1** Multi-Media Card Data [1], bidirectional signal (module input/output)
- **MMC_D2** Multi-Media Card Data [2], bidirectional signal (module input/output)
- **MMC_D3** Multi-Media Card Data [3], bidirectional signal (module input/output)
- **MMC_CMD** Multi-Media Card Command, bidirectional signal (module input/output)
- **MMC_CLK** Multi-Media Card Clock (module output)
- **MMC_RST_N** Multi-Media Card Reset (module output)
- **MMC_CD_N** Multi-Media Card Detect (module input)

1.11 Audio interfaces

1.11.1 Analog audio interfaces

TOBY-L4 series modules provide the following analog audio interfaces:

- Analog audio inputs (analog audio uplink path)[15]:
  - First differential analog audio input (**MIC1_P**, **MIC1_N**), which can be connected to the output of an external analog audio device, or an external microphone for voice call or eCall purposes.

    The **MIC1_P** / **MIC1_N** pins are internally directly connected to a differential input (positive/negative) of the Audio Front-End, consisting of a Low Noise Amplifier integrated in a dedicated IC, without any internal series capacitor for DC blocking. The LNA is internally followed by an integrated sigma-delta ADC connecting the analog Audio Front-End to the digital audio processing system.
  - Second differential analog audio input (**MIC2_P**, **MIC2_N**), which can be connected to the output of an external analog audio device, or an external microphone for voice call or eCall purposes.

    The **MIC2_P** / **MIC2_N** pins are internally directly connected to a differential input (positive/negative) of the Audio Front-End, consisting of a Low Noise Amplifier integrated in a dedicated IC, without any internal series capacitor for DC blocking. The LNA is internally followed by an integrated sigma-delta ADC connecting the analog Audio Front-End to the digital audio processing system.
  - Supply output for external microphones (**MIC_BIAS**), which can provide the bias / supply for external microphones by means of a simple circuit implemented on the application board.

    The **MIC_BIAS** pin is internally connected to the output of a low noise LDO linear regulator integrated in a dedicated IC, with appropriate internal bypass capacitor provided to guarantee stable operation of the linear regulator.
  - Local ground for the external microphone (**MIC_GND**)

    The **MIC_GND** pin is internally connected to ground as a sense line, representing a clean ground reference for the analog audio input.
- Analog audio output (analog audio downlink path):
  - Differential analog audio output (**SPK_P**, **SPK_N**), which can be connected to the input of an external analog audio device, or an external speaker.

    The **SPK_P** / **SPK_N** pins are internally directly connected to a differential output (positive/negative) of the Audio Front-End, consisting of a low power audio amplifier integrated in a dedicated IC, without any internal series capacitor for DC blocking. The low power audio amplifier is internally preceded by an integrated DAC connecting the analog Audio Front-End to the digital audio processing system.

[15] The first differential analog audio input (**MIC1_P**, **MIC1_N**) and the second differential analog audio input (**MIC2_P**, **MIC2_N**) interfaces can be used alternatively, in mutually exclusive way.

1.11.2 Digital audio interface

TOBY-L4 series modules include two 4-wire I²S digital audio interfaces:

- I2S0 digital audio interface, consisting of the following pins:
  - **I2S_TXD** data output
  - **I2S_RXD** data input
  - **I2S_CLK** bit clock input/output
  - **I2S_WA** world alignment / synchronization signal input/output
- I2S1 digital audio interface consisting of the following pins:
  - **I2S1_TXD** data output
  - **I2S1_RXD** data input
  - **I2S1_CLK** bit clock input/output
  - **I2S1_WA** world alignment / synchronization signal input/output

☞ The second digital audio interface (I2S1) will be supported by future firmware versions.

Both I2S0 and I2S1 digital audio interfaces are suitable to transfer digital audio data with an external compatible digital audio device, as an audio codec or as an audio digital signal processor.

The I²S interfaces can be alternatively set in different modes:

- PCM mode (short synchronization signal): I²S word alignment signal is set high for 1 or 2 clock cycles for the synchronization, and then is set low for 16 clock cycles according to the 17 or 18 clock cycles frame length.
- Normal I²S mode (long synchronization signal): I²S word alignment is set high / low with a 50% duty cycle (high for 16 clock cycles / low for 16 clock cycles, according to the 32 clock cycles frame length).

The I²S interface can be alternatively set in 2 different roles:

- Master mode
- Slave mode

The sample rate of transmitted/received words, which corresponds to the I²S word alignment / synchronization signal frequency (<I2S_sample_rate>), can be alternatively set to:

- 8 kHz
- 11.025 kHz
- 12 kHz
- 16 kHz
- 22.05 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz
- 96 kHz
- 192 kHz

The modules support I²S transmit and I²S receive data 16-bit words long, linear. Data is transmitted and read in 2's complement notation. The MSB is transmitted and read first.

I²S clock signal frequency depends on the frame length, the sample rate and the selected mode of operation:

- 17 x <I2S_sample_rate> or 18 x <I2S_sample_rate> in PCM mode (short synchronization signal)
- 16 x 2 x <I2S_sample_rate> in Normal I2S mode (long synchronization signal)

1.12 ADC interfaces

☞ The ADC pins are not supported by the "50" product version.

TOBY-L4 series modules include Analog to Digital Converter inputs (**ADC1**, **ADC2**), which can be handled by means of the dedicated uCPU API.

1.13 General Purpose Input/Output

TOBY-L4 series modules "00" product versions include 14 pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4**, **GPIO5**, **GPIO6**, **GPIO7**, **GPIO8**, **HOST_SELECT0**, **HOST_SELECT1**, **DTR**, **DSR**, **DCD**, and **RI**) that can be configured by the uCPU application as general purpose input/output or to provide custom functions as summarized in Table 11.

Function	Description	Configurable GPIOs
External Interrupt	External Interrupt detection (module input)	GPIO3, HOST_SELECT0, HOST_SELECT1, DTR, DSR, DCD, RI
SPI Chip Select	SPI0 Chip Select 1 (module output)	GPIO4
GNSS supply enable	Enable/disable the supply of u-blox GNSS receiver connected to the cellular module over the I2C0 interface	GPIO2
GNSS data ready	Sense when u-blox GNSS receiver connected to the module is ready for sending data over the I2C0 interface	GPIO3
GNSS RTC sharing	RTC synchronization signal to the u-blox GNSS receiver connected to the cellular module over the I2C0 interface	GPIO4
SIM card detection	External SIM card physical presence detection	GPIO5
SIM card hot insertion/removal	Enable / disable SIM interface upon detection of external SIM card physical insertion / removal	GPIO5
Wi-Fi enable	Switch-on/off the external u-blox Wi-Fi module connected to the cellular module over the SDIO interface	GPIO1
Wake-up	Wake-up the module from Suspend to RAM state	GPIO3
Core dump	Indicates core dump sent over Ethernet RGMII / RMII interface	GPIO8
Input	Input to sense high or low digital level	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, DTR, DSR, DCD, RI
Output	Output to set the high or the low digital level	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, DTR, DSR, DCD, RI
Pin disabled	Output tri-stated with an internal active pull-down enabled	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, DTR, DSR, DCD, RI

Table 11: TOBY-L4 series modules "00" product versions GPIO custom functions summary

TOBY-L4 series modules "50" product versions include 9 pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4**, **GPIO5**, **GPIO6**, **GPIO7**, **GPIO8**, and **RI**) that can be configured by AT commands as general purpose input/output or to provide custom functions as summarized in Table 12.

Function	Description	Configurable GPIOs
Ring Indicator	UART0 Ring Indicator functionality (Circuit 125 in ITU-T V.24)	RI
SIM card detection	External SIM card physical presence detection	GPIO5
SIM card hot insertion/removal	Enable / disable SIM interface upon detection of external SIM card physical insertion / removal	GPIO5
Input	Input to sense high or low digital level	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, RI
Output	Output to set the high or the low digital level	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, RI
Pin disabled	Output tri-stated with an internal active pull-down enabled	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, RI

Table 12: TOBY-L4 series modules "50" product versions GPIO custom functions summary

1.14 Reserved pins (RSVD)

TOBY-L4 series modules have pins reserved for future use, marked as **RSVD**: they can all be left unconnected on the application board, except

- the **RSVD** pin number **6** that must be externally connected to ground

2 Design-in

2.1 Overview

For optimal integration of the modules in the application PCB, follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the relative interface, but a number of points require greater attention during the design of the application device.

The following list provides a rank of importance in the application design, starting with the most significant:

1. Module antenna connection:
   Antenna circuit directly affects the RF compliance of the device integrating a TOBY-L4 series module with applicable certification schemes. Very carefully follow the suggestions provided in section 2.4 for the schematic and layout design.
2. Module supply:
   The supply circuit affects the RF compliance of the device integrating a TOBY-L4 series module with applicable required certification schemes as well as the antenna circuit design. Very carefully follow the suggestions provided in section 2.2.1 for the schematic and layout design.
3. USB interface:
   Accurate design is required to guarantee USB functionality. Carefully follow the suggestions provided in section 2.6.1 for the schematic and layout design.
4. SIM interface:
   Accurate design is required to guarantee SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in section 2.5 for the schematic and layout design.
5. System functions:
   Accurate design is required to guarantee well defined voltage level during operation at Reset and Power-on inputs. Carefully follow the suggestions provided in section 2.3 for the schematic and layout design.
6. Analog audio:
   Accurate design is required to obtain clear and high quality audio reducing the risk of noise from audio lines due to both supply burst noise coupling and RF detection. Carefully follow the suggestions provided in section 2.8.1 for the schematic and layout design.
7. SDIO, RGMII, eMMC interfaces:
   Accurate design is required to guarantee SDIO, RGMII, eMMC interfaces functionality. Carefully follow the suggestions provided in section 2.6.5, 2.6.6, 2.7 for the schematic and layout design.
8. ADC interfaces:
   Accurate design is required to guarantee ADC interfaces functionality. Carefully follow the suggestions provided in section 2.9 for the schematic and layout design.
9. Other digital interfaces: (UART, SPI, I^2C, I^2S, Host Select, GPIOs, and Reserved pins).
   Accurate design is required to guarantee correct functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6.1, 2.6.3, 2.6.4, 2.8.2, 2.3.3, 2.10, 2.11.
10. Other supplies: **V_BCKP** RTC supply and **V_INT** generic digital interfaces supply.
    Correct design is required to guarantee functionality. Follow the suggestions provided in 2.2.2 and 2.2.3.

☞ It is recommended to also follow the specific design guidelines provided by each manufacturer of any external part selected for the application board that integrates the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins must be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

TOBY-L4 series modules must be sourced through the **VCC** pins with a suitable DC power supply that should meet the following prerequisites to comply with the modules' **VCC** requirements summarized in Table 7.

The suitable DC power supply can be selected according to the application requirements (see Figure 19) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

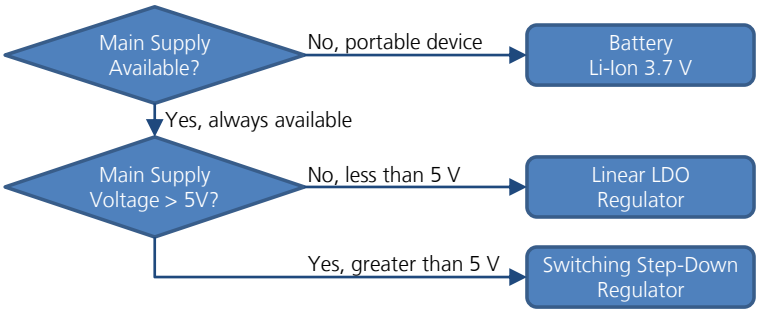

Figure 19: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of TOBY-L4 series. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See sections 2.2.1.2, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See sections 2.2.1.3, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

If TOBY-L4 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit which is not included in the modules. The charger circuit must be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements: a DC/DC switching charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is the

typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a suitable charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.7, 2.2.1.8, and 2.2.1.4, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected taking into account the maximum current specified in the TOBY-L4 series Data Sheet [1] during connected mode, considering that primary cells might have weak power capability. See sections 2.2.1.5, and 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

The usage of more than one DC supply at the same time should be evaluated carefully: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The usage of a regulator or a battery not able to support the highest peak of **VCC** current consumption specified in the TOBY-L4 series Data Sheet [1] is generally not recommended. However, if the selected regulator or battery is not able to support the highest peak current of the module, it must be able to support with adequate margin at least the highest averaged current consumption value specified in the TOBY-L4 series Data Sheet [1]. The additional energy required by the module during a 2G Tx slot can be provided by an appropriate bypass tank capacitor or a super-capacitor with very large capacitance and very low ESR placed close to the module **VCC** pins. Depending on the actual capability of the selected regulator or battery, the required capacitance can be considerably larger than 1 mF and the required ESR can be in the range of few tens of mΩ. Carefully evaluate the super-capacitor characteristics since aging and temperature may affect the actual characteristics.

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 7.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in the TOBY-L4 series Data Sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications it is recommended to select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be evaluated carefully since this can produce noise in the **VCC** voltage profile and therefore negatively impact LTE/3G/2G modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple at the input of the module, but adds extra voltage drop due to resistive losses on series inductors.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the idle/active modes to connected mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 20 and Table 13 show an example of a high reliability power supply circuit, where the module **VCC** input is supplied by a step-down switching regulator capable of delivering maximum current with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

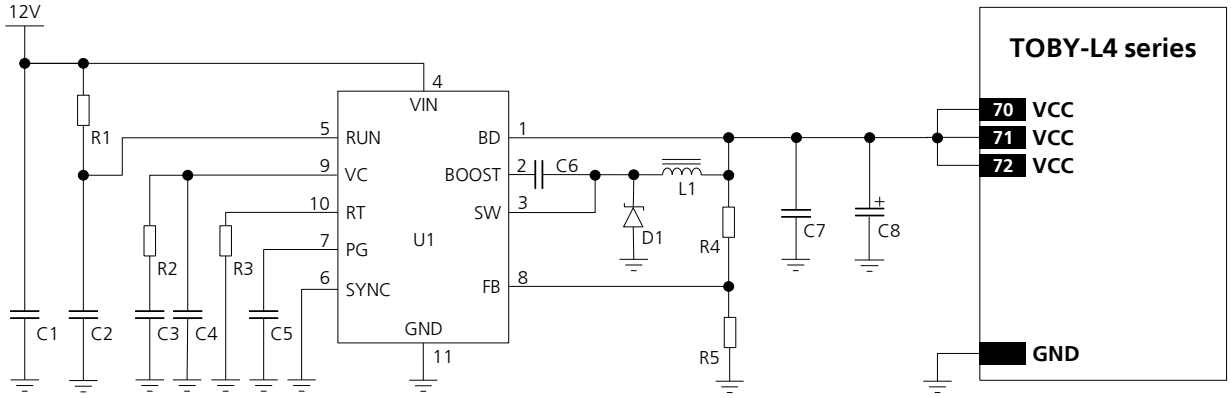

Figure 20: Example of high reliability VCC supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 kΩ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	22 kΩ Resistor 0402 5% 0.1 W	2322-705-87223-L - Yageo
R4	390 kΩ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 kΩ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step-Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 13: Components for high reliability VCC supply application circuit using a step-down regulator

Figure 21 and the components listed in Table 14 show an example of a low-cost power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable of delivering to **VCC** pins the specified maximum peak / pulse current, transforming a 12 V supply input.

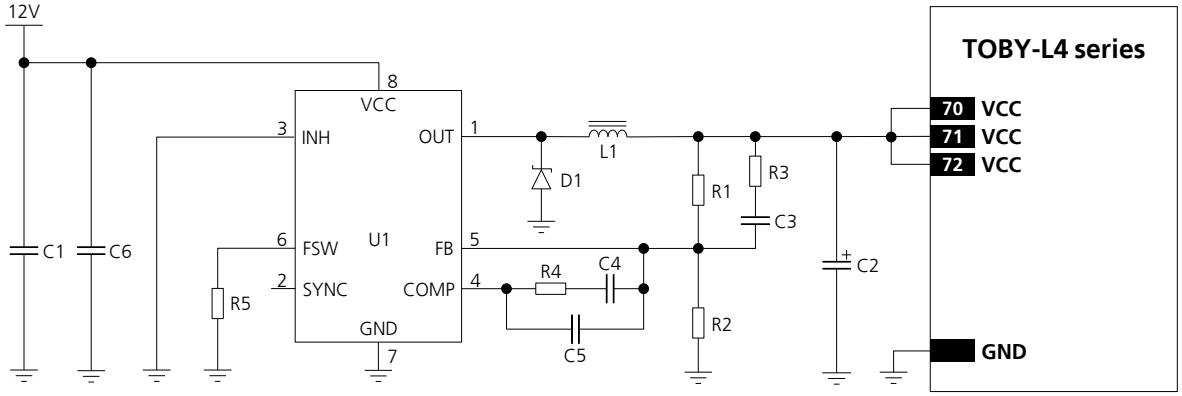

Figure 21: Example of low cost VCC supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 – Murata
C2	100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 – Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 – Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H560JA01 – Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 – Murata
D1	Schottky Diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ Resistor 0402 1% 0.063 W	RC0402FR-074K7L – Yageo
R2	910 Ω Resistor 0402 1% 0.063 W	RC0402FR-07910RL – Yageo
R3	82 Ω Resistor 0402 5% 0.063 W	RC0402JR-0782RL – Yageo
R4	8.2 kΩ Resistor 0402 5% 0.063 W	RC0402JR-078K2L – Yageo
R5	39 kΩ Resistor 0402 5% 0.063 W	RC0402JR-0739KL – Yageo
U1	Step-Down Regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 14: Components for low cost VCC supply application circuit using a step-down regulator

2.2.1.3 Guidelines for VCC supply circuit design using a Low Drop-Out linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low. The linear regulators provide high efficiency when transforming a 5 VDC supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to the **VCC** pins the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in the TOBY-L4 series Data Sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 22 and the components listed in Table 15 show an example of a power supply circuit where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the required current with a suitable power handling capability.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V for the **VCC**, as in the circuits illustrated in Figure 22 and Table 15). This reduces the power on the linear regulator and improves the thermal design of the circuit.

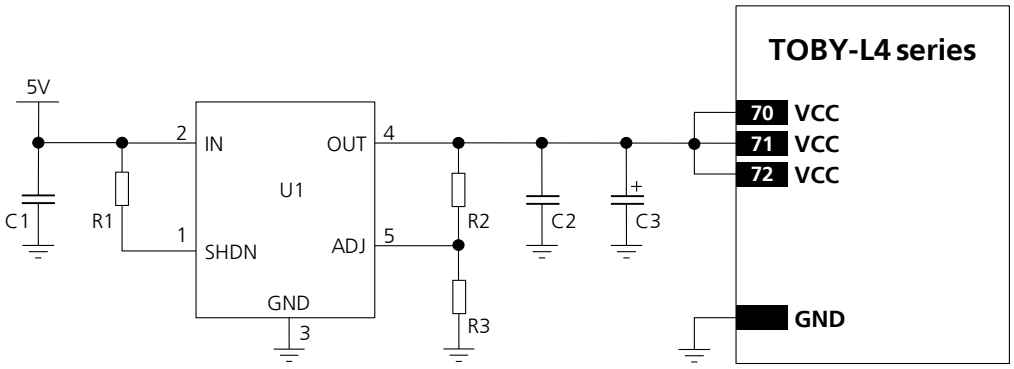

Figure 22: Example of high reliability VCC supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C3	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	9.1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-079K1L - Yageo Phycomp
R3	3.9 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K9L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 15: Components for high reliability VCC supply application circuit using an LDO linear regulator

Figure 23 and the components listed in Table 16 show an example of a low-cost power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with suitable power handling capability. The regulator illustrated in this example supports a limited input voltage range and it includes internal circuitry for current and thermal protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module's VCC normal operating range (e.g. ~4.1 V as in the circuit illustrated in Figure 23 and Table 16). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

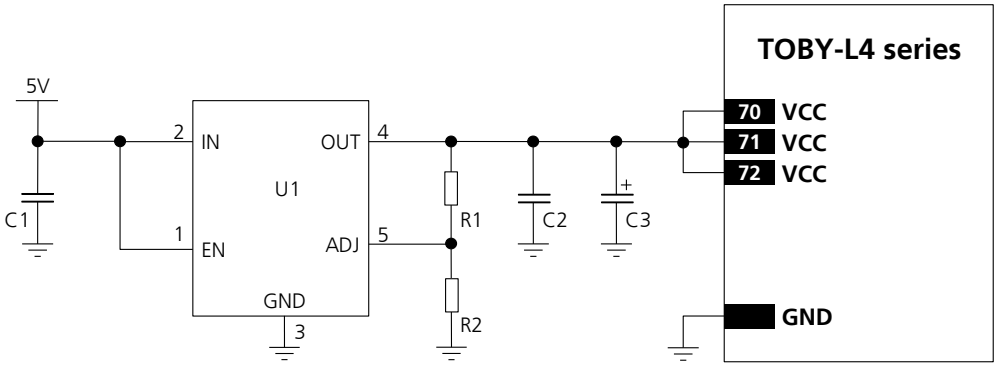

Figure 23: Example of a low cost VCC supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C3	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
R1	27 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0727KL - Yageo Phycomp
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LP38501ATJ-ADJ/NOPB - Texas Instrument

Table 16: Components for a low cost VCC supply application circuit using an LDO linear regulator

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module's **VCC** requirements as summarized in Table 7:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak / pulse current consumption during Tx burst at the maximum Tx power specified in the TOBY-L4 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption as specified in the TOBY-L4 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 7 during transmit bursts.

2.2.1.5 Guidelines for VCC supply circuit design using a primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to the **VCC** pins should meet the following prerequisites to comply with the module's **VCC** requirements as summarized in Table 7:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak current consumption during Tx burst at the maximum Tx power specified in the TOBY-L4 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption as specified in the TOBY-L4 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range as summarized in Table 7 during transmit bursts.

2.2.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the power supply lines (connected to the modules' **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated to the **VCC** supply. Several pins are designated for **GND** connection. It is recommended to correctly connect all of them to supply the module to minimize series resistance losses.

For modules supporting 2G radio access technology, to avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a GSM call (when current consumption on the **VCC** supply can rise up as specified in the TOBY-L4 series Data Sheet [1]), place a bypass capacitor with large capacitance (at least 100 µF) and low ESR near the **VCC** pins, for example:

- 330 µF capacitance, 45 mΩ ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 68 pF capacitor with Self-Resonant Frequency in the 800/900 MHz range (e.g. Murata GRM1555C1H680J)
- 15 pF capacitor with Self-Resonant Frequency in 1800/1900 MHz range (e.g. Murata GRM1555C1E150J)
- 8.2 pF capacitor with Self-Resonant Frequency in 2500/2600 MHz range (e.g. Murata GRM1555C1H8R2D)
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 100 nF capacitor (e.g. Murata GRM155R61C104K) to filter digital logic noise from clocks and data sources

A suitable series ferrite bead can be correctly placed on the **VCC** line for additional noise filtering if required by the specific application according to the whole application board design.

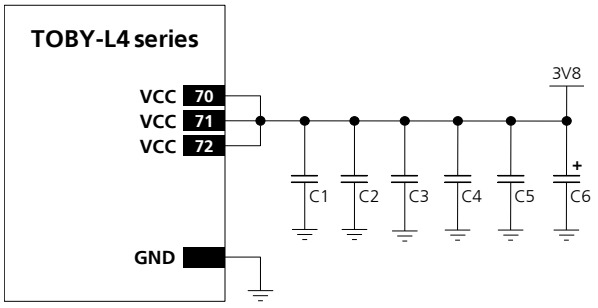

Figure 24: Suggested schematic for the VCC bypass capacitors to reduce ripple / noise on the supply voltage profile

Reference	Description	Part Number - Manufacturer
C1	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C2	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C3	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C6	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET

Table 17: Suggested components to reduce ripple / noise on the VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the bypass capacitors illustrated in Figure 24 / Table 17 if the application device integrates an internal antenna.

☞ The ESD sensitivity rating of the **VCC** supply pins is 1 kV (HBM as per JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board, e.g. if the accessible battery connector is directly connected to the supply pins. A higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

2.2.1.7 Guidelines for the external battery charging circuit

TOBY-L4 series modules do not have an on-board charging circuit. Figure 25 provides an example of a battery charger design which is suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features the correct pulse and DC discharge current capabilities and the correct DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges the battery as a linear charger, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA).
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s.

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The L6924U, as a linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see the following section 2.2.1.8 for the specific design-in).

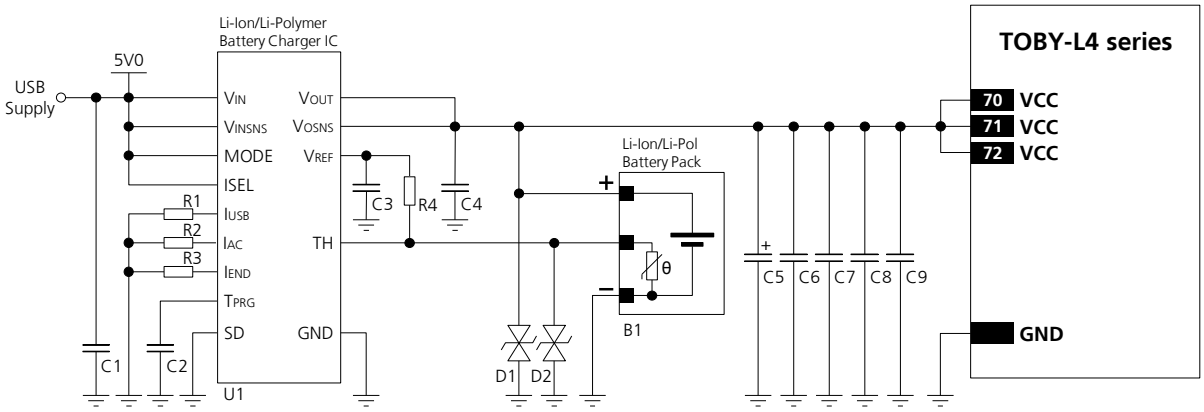

Figure 25: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Various manufacturer
C1, C4	1 µF Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C9	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R2	24 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0724KL - Yageo Phycomp
R3	3.3 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K3L - Yageo Phycomp
R4	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC	L6924U - STMicroelectronics

Table 18: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit

2.2.1.8 Guidelines for external battery charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 26 reports a simplified block diagram circuit showing the working principle of a charger / regulator with an integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system: the power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system current.

A power management IC should meet the following prerequisites to comply with the module's **VCC** requirements as summarized in Table 7:

- High efficiency internal step down converter, compliant with the performances specified in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

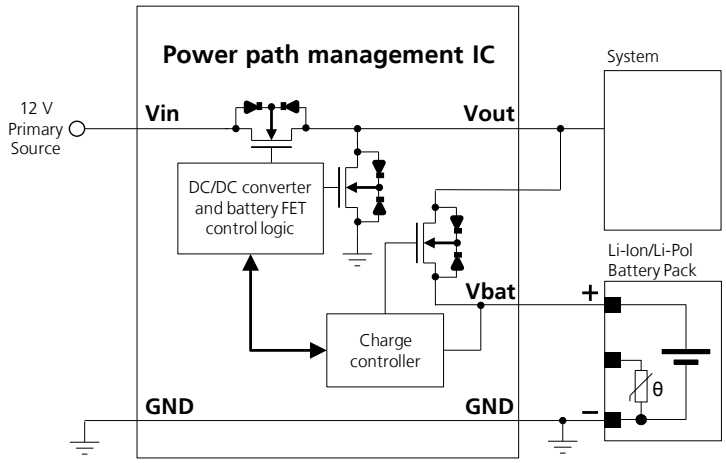

Figure 26: Charger / regulator with integrated power path management circuit block diagram

Figure 27 and the components listed in Table 19 provide an application circuit example where the MPS MP2617 switching charger / regulator with integrated power path management function provides the supply to the cellular module while concurrently and autonomously charging a suitable Li-Ion (or Li-Polymer) battery with the correct pulse and DC discharge current capabilities and the correct DC series resistance according to the rechargeable battery recommendations as described in section 2.2.1.4.

The MP2617 IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as the supply source for the module, and starts a charging phase accordingly.

The MP2617 IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from the battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor.

Using a battery pack with an internal NTC resistor, the MP2617 can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters, such as the charging current, the charging timings, the input current limit, the input voltage limit, and the system output voltage, can be easily set according to the specific application requirements to the actual electrical characteristics of the battery and the external supply / charging source: suitable resistors or capacitors must be accordingly connected to the related pins of the IC.

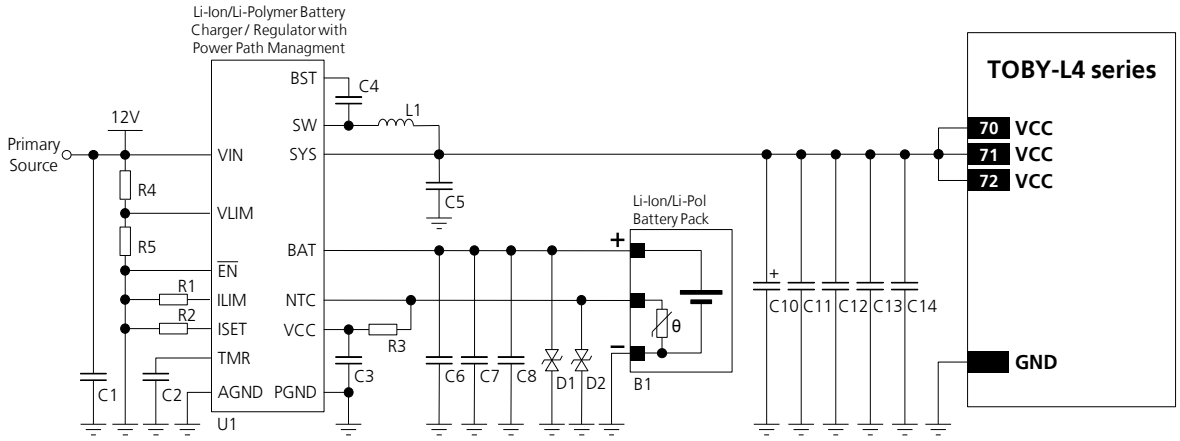

Figure 27: Li-Ion (or Li-Polymer) battery charging and power path management application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC	Various manufacturer
C1, C5, C6	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C7, C13	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C8, C14	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C10	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C12	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R3, R5	10 kΩ Resistor 0402 5% 1/16 W	RC0402JR-0710KL - Yageo Phycomp
R2	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
R4	22 kΩ Resistor 0402 5% 1/16 W	RC0402JR-0722KL - Yageo Phycomp
L1	1.2 µH Inductor 6 A 21 mΩ 20%	7447745012 - Wurth
U1	Li-Ion/Li-Polymer Battery DC/DC Charger / Regulator with integrated Power Path Management function	MP2617 - Monolithic Power Systems (MPS)

Table 19: Suggested components for a Li-Ion (or Li-Polymer) battery charging and power path management application circuit

2.2.1.9 Guidelines for removing VCC supply

As described in section 1.6.2 and Figure 14, the **VCC** supply can be removed after the end of the TOBY-L4 series module's internal power-off sequence, which must be properly started as described in section 1.6.2.

Removing the **VCC** power can be useful in order to minimize the current consumption when the TOBY-L4 series modules are switched off. Then, the modules can be switched on again by re-applying the **VCC** supply.

If the **VCC** supply is generated by a switching or an LDO regulator, the application processor may control the input pin of the regulator which is provided to enable / disable the output of the regulator (as for example, the RUN input pin for the regulator illustrated in Figure 20, the INH input pin for the regulator illustrated in Figure 21, the SHDNn input pin for the regulator illustrated in Figure 22, or the EN input pin for the regulator illustrated in Figure 23), in order to apply / remove the **VCC** supply.

If the regulator that generates the **VCC** supply does not provide an on / off pin, or for other applications such as the battery-powered ones, the **VCC** supply can be switched off using an appropriate external p-channel MOSFET controlled by the application processor by means of a suitable inverting transistor as shown in Figure 28, given that the external p-channel MOSFET has provided:

- Very low $R_{DS(ON)}$ (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum Drain current (see the TOBY-L4 series Data Sheet [1] for module consumption figures)
- Low leakage current, to minimize the current consumption

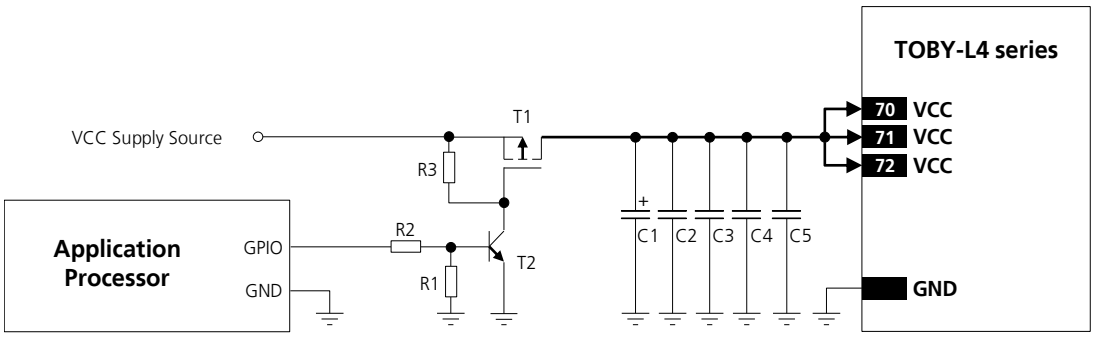

Figure 28: Example of application circuit for VCC supply removal

Reference	Description	Part Number - Manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R3	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
T1	P-Channel MOSFET Low On-Resistance	AO3415 - Alpha & Omega Semiconductor Inc.
T2	NPN BJT Transistor	BC847 - Infineon
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata

Table 20: Components for VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during the TOBY-L4 series module's normal operations: the power off procedure must be started as described in section 1.6.2, and then a suitable **VCC** supply must be held at least until the end of the modules' internal power off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

2.2.1.10 Guidelines for VCC supply layout design

A clean connection of the module **VCC** pins with a DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- Coupling between **VCC** and digital lines, especially USB, must be avoided.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.6 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for the DC-DC converter and module tank capacitor.
- The bypass capacitors in the pF range illustrated in Figure 24 and Table 17 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF noise rejection in the band centered on the Self-Resonant Frequency of the pF capacitors. This is highly recommended if the application device integrates an internal antenna.
- Since **VCC** input provides the supply to the RF Power Amplifiers, any voltage ripple at high frequency may result in unwanted spurious modulation of the transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the TOBY-L4 series modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If the **VCC** is protected by a transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection functionality may be compromised).

2.2.1.11 Guidelines for grounding layout design

A clean connection of the module **GND** pins with the application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with the application board solid GND layer. It is strongly recommended that each **GND** pad surrounding the **VCC** pins has one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to the main DC source through GND as the ground current: provide an adequate return path with a suitable uninterrupted ground plane to the main DC source.
- It is recommended to implement one layer of the application board as a ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with a complete via stack down to the main ground layer of the board.
- If the whole application device is composed of more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the multiple PCBs.
- Good grounding of the **GND** pads also ensures the thermal heat sink. This is critical during connection, when the real network commands the module to transmit at maximum power: correct grounding helps prevent module overheating.

2.2.2 RTC back-up supply (V_BCKP)

2.2.2.1 Guidelines for V_BCKP circuit design

TOBY-L4 series modules provide the **V_BCKP** pin, which can be used to:

- power the Real Time Clock (RTC) only when the voltage value at **VCC** main module supply input is too low

The RTC can be supplied from an external back-up battery or capacitor through the **V_BCKP** pin, when the main module voltage supply is not applied to the **VCC** pins. This lets the time reference (date and time) run as long as the **V_BCKP** voltage is within its valid range, even when the main supply is not provided to the module.

Figure 29 and Table 21 describe possible application circuits for **V_BCKP** Real Time Clock (RTC) back-up supply:

a. 100 µF capacitor, to let the RTC run for ~1 minute after the **VCC** removal
b. 70 mF super-capacitor with a 4.7 kΩ series resistor, to let the RTC run for ~1 hour after the **VCC** removal
c. Coin non-rechargeable battery with series diode, to let the RTC run for days after the **VCC** removal

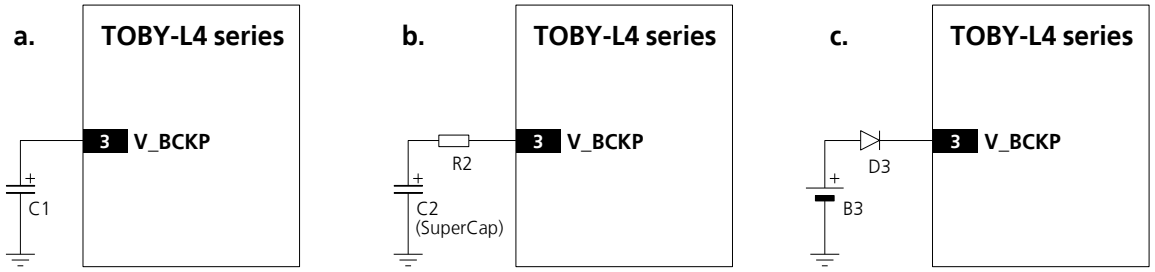

Figure 29: RTC back-up supply (V_BCKP) application circuits using a capacitor, a super-capacitor, or a non-rechargeable battery

Reference	Description	Part Number - Manufacturer
C1	100 µF Tantalum Capacitor	GRM43SR60J107M - Murata
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C2	70 mF Capacitor	XH414H-IV01E - Seiko Instruments

Table 21: Example of components for RTC back-up supply (V_BCKP)

The **V_BCKP** supply output pin provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ The **V_BCKP** pin can be left unconnected if the RTC timing is not required when the **VCC** supply is removed.

☞ The internal regulator for **V_BCKP** is optimized for low leakage current and very light loads. Do not apply loads which might exceed the limit for the maximum available current from **V_BCKP** supply, as this can cause malfunctions in the module. The TOBY-L4 series Data Sheet [1] describes the detailed electrical characteristics.

☞ The ESD sensitivity rating of the **V_BCKP** supply pin is 1 kV (HBM according to JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible back-up battery connector is directly connected to the **V_BCKP** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

2.2.2.2 Guidelines for V_BCKP layout design

The **V_BCKP** supply requires careful layout: avoid injecting noise on this voltage domain, as it may affect the stability of the internal circuitry.

2.2.3 Generic digital interfaces supply output (V_INT)

2.2.3.1 Guidelines for V_INT circuit design

TOBY-L4 series provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on (as described in sections 1.6.1, 1.6.2)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply voltage translators to connect 1.8 V module generic digital interfaces to 3.0 V devices (e.g. see 2.6.1)
- Pull-up DDC (I^2C) interface signals (see section 2.6.4 for more details)
- Supply a 1.8 V u-blox GNSS receiver (see section 2.6.4 for more details)
- Supply an external device as an external 1.8 V audio codec (see section 2.8.2 for more details)

The **V_INT** supply output pin provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ Do not apply loads which might exceed the limit for the maximum available current from **V_INT** supply as this can cause malfunctions in the internal circuitry.

☞ Since the **V_INT** supply is generated by an internal switching step-down regulator, it is not recommended to supply sensitive analog circuitry without adequate filtering for digital noise.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ The ESD sensitivity rating of the **V_INT** supply pin is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

☞ It is recommended to monitor the **V_INT** pin to sense the end of the internal switch-off sequence of TOBY-L4 series modules: the **VCC** supply can be removed only after **V_INT** goes low

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible test point directly connected to the **V_INT** pin, for diagnostic purposes.

2.2.3.2 Guidelines for V_INT layout design

The **V_INT** supply output is generated by an integrated switching step-down converter. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

TOBY-L4 series **PWR_ON** input is equipped with an internal active pull-up resistor to an internal 1.3 V supply rail as illustrated in Figure 30: an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as illustrated in Figure 30 and Table 22.

The ESD sensitivity rating of the **PWR_ON** pin is 1 kV (Human Body Model according to JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **PWR_ON** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as the pin is equipped with an internal active pull-up resistor, as illustrated in Figure 30.

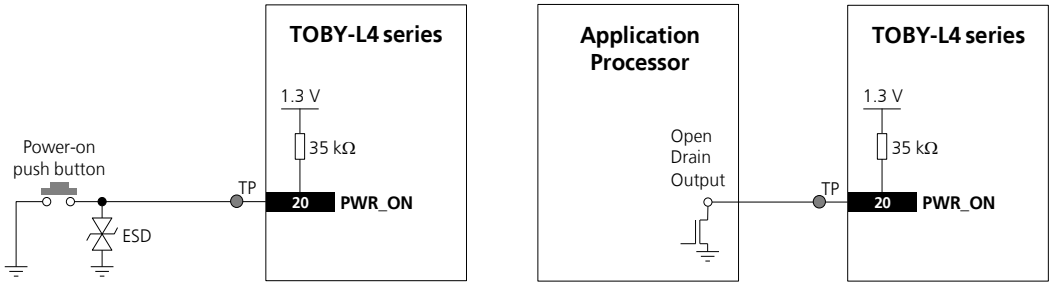

Figure 30: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 22: Example ESD protection component for the PWR_ON application circuit

It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of an accessible test point directly connected to the **PWR_ON** pin, for diagnostic purposes.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout since it is the sensitive input available to switch on the TOBY-L4 series modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

TOBY-L4 series **RESET_N** line is equipped with an internal pull-up to the **V_INT** supply as illustrated in Figure 31. An external pull-up resistor is not required.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to the EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to the accessible point on the line connected to this pin, as illustrated in Figure 31 and Table 23.

☞ The ESD sensitivity rating of the **RESET_N** pin is 1 kV (HBM according to JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **RESET_N** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain output is suitable to drive the **RESET_N** input from an application processor as it is equipped with an internal pull-up to **V_INT** supply, as illustrated in Figure 31.

A compatible push-pull output of an application processor can also be used. In any case, take care to set the correct level in all the possible scenarios to avoid an inappropriate module reset.

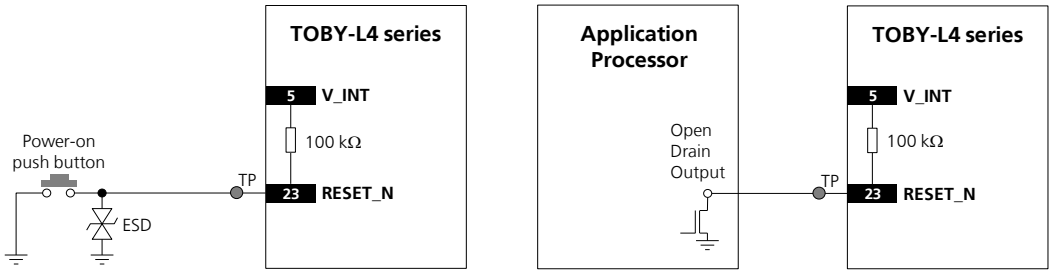

Figure 31: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 23: Example of ESD protection component for the RESET_N application circuits

☞ If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended to provide direct access on the application board by means of an accessible test point directly connected to the **RESET_N** pin.

2.3.2.2 Guidelines for RESET_N layout design

The **RESET_N** circuit requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to the **RESET_N** pin as short as possible.

2.3.3 Module / host configuration selection

☞ Host Select pins are not supported by the "50" product version.

2.3.3.1 Guidelines for HOST_SELECTx circuit design

TOBY-L4 series modules include two 1.8 V digital pins (**HOST_SELECT0**, **HOST_SELECT1**), which can be configured for External Interrupt detection or as GPIO by means of the uCPU API: the pins can be connected to external devices following the guidelines provided in section 2.10.

☞ Do not apply voltage to the **HOST_SELECT0** and **HOST_SELECT1** pins before the switch-on of their supply source (**V_INT**), to avoid latch-up of circuits and allow a correct boot of the module.

☞ The ESD sensitivity rating of the **HOST_SELECT0** and **HOST_SELECT1** pins is 1 kV (HBM as per JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the functionality of the **HOST_SELECT0** and **HOST_SELECT1** pins is not required, the pins can be left unconnected on the application board.

2.3.3.2 Guidelines for HOST_SELECTx layout design

The design for the **HOST_SELECT0** and **HOST_SELECT1** pins functions is generally not critical for layout.

2.4 Antenna interface

TOBY-L4 series modules provide two RF interfaces for connecting the external antennas:

- The **ANT1** pin represents the primary RF input/output for LTE/3G/2G RF signals transmission and reception.
- The **ANT2** pin represents the secondary RF input for MIMO and Rx diversity RF signals reception.

Both the **ANT1** and the **ANT2** pins have a nominal characteristic impedance of 50 Ω and must be connected to the related antenna through a 50 Ω transmission line to allow correct transmission / reception of RF signals.

☞ Two antennas (one connected to **ANT1** pin and one connected to **ANT2** pin) must be used to support the CA, MIMO and Rx diversity configurations. This is a required feature for LTE category 6 User Equipments (up to 301.5 Mbit/s Down-Link data rate) according to the 3GPP specifications.

2.4.1 Antenna RF interfaces (ANT1 / ANT2)

2.4.1.1 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antennas from all perspectives at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating TOBY-L4 series modules with all the applicable required certification schemes depends on the antenna radiating performance.

LTE/3G/2G antennas are typically available in the types of linear monopole or PCB antennas such as patches or ceramic SMT elements.

- External antennas (e.g. linear monopole)
  - External antennas basically do not imply a physical restriction to the design of the PCB where the TOBY-L4 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides suitable PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. patch-like antennas):
  - Internal integrated antennas imply a physical restriction to the design of the PCB:

    An integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that must be radiated, given that the orientation of the ground plane relative to the antenna element must be considered.

    The isolation between the primary and the secondary antennas must be as high as possible and the correlation between the 3D radiation patterns of the two antennas must be as low as possible. In general, a separation of at least a quarter wavelength between the two antennas is required to achieve a good isolation and low pattern correlation.

    As a numerical example, the physical restriction to the PCB design can be considered as following:

    Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm

- Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
- It is recommended to select a pair of custom antennas designed by an antennas' manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process.
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both cases, selecting external or internal antennas, these recommendations should be observed:

- Select antennas providing optimal return loss (or VSWR) figures over all the operating frequencies.
- Select antennas providing optimal efficiency figures over all the operating frequencies.
- Select antennas providing similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- Select antennas providing appropriate gain figures (i.e. combined antenna directivity and efficiency figures) so that the electromagnetic field radiation intensity does not exceed the regulatory limits specified in certain countries (e.g. by the FCC in the United States).
- Select antennas capable of providing a low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antenna: the 3D antenna radiation patterns should have lobes in different directions.

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for ANT1 / ANT2 pins RF connection design

Correct transition between the **ANT1** / **ANT2** pads and the application board PCB must be provided, implementing the following design-in guidelines for the application PCB layout close to the **ANT1** / **ANT2** pads:

- On a multilayer board, the whole layer stack below the RF connection should be free of digital lines.
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT1** / **ANT2** pads, on the top layer of the application PCB, to at least 250 µm up to the adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as illustrated in the left example of Figure 32.
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT1** / **ANT2** pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as illustrated in the right example of Figure 32.

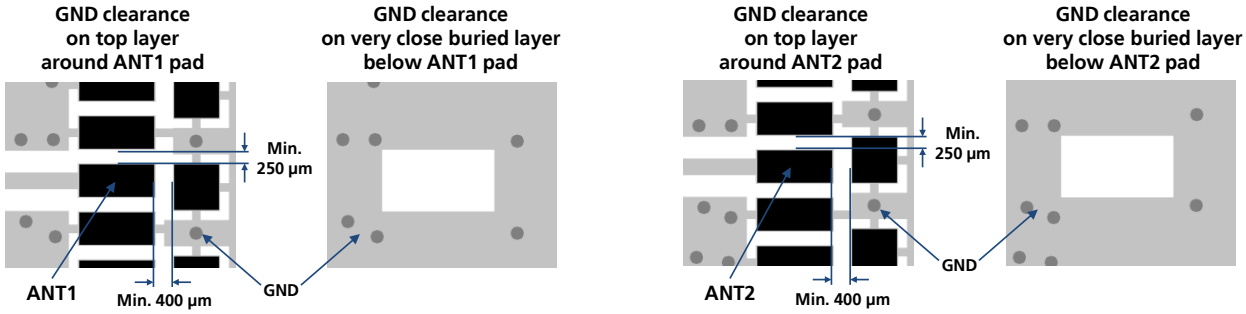

Figure 32: GND keep-out area on top layer around ANT1 / ANT2 pads and on very close buried layer below ANT1 / ANT2 pads

Guidelines for RF transmission line design

Any RF transmission line, such as the ones from the **ANT1** and **ANT2** pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit boards.

Figure 33 and Figure 34 provide two examples of suitable 50 Ω coplanar waveguide designs. The first example of an RF transmission line can be implemented for a 4-layer PCB stack-up herein illustrated, and the second example of an RF transmission line can be implemented for a 2-layer PCB stack-up herein illustrated.

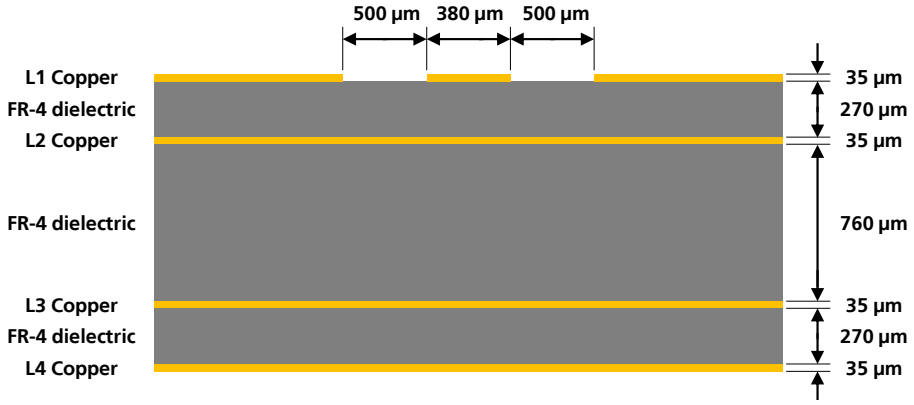

Figure 33: Example of a 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

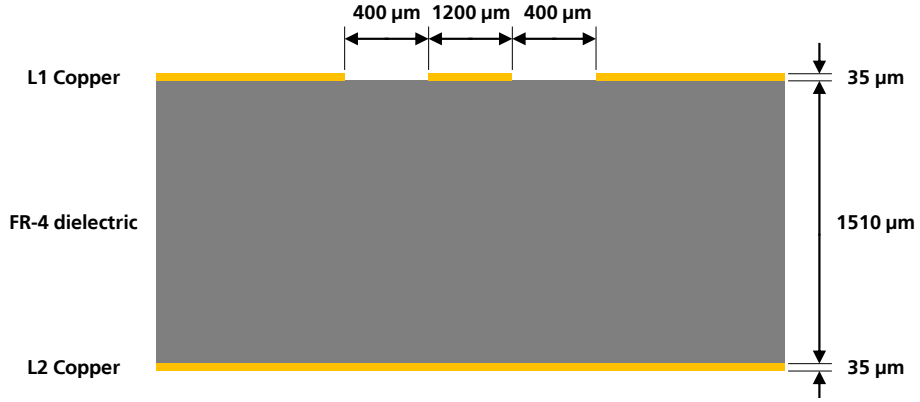

Figure 34: Example of a 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent (www.agilent.com) or TXLine from Applied Wave Research (www.mwoffice.com), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the examples of Figure 33 and Figure 34)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 33, 1510 µm in Figure 34)

- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 33 and Figure 34)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 33, 400 µm in Figure 34)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of a component present on the RF transmission lines, if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND stitching vias around the transmission lines, as illustrated in Figure 35.
- Ensure a solid metal connection of the adjacent metal layer on the PCB stack-up to the main ground layer, providing enough vias on the adjacent metal layer, as illustrated in Figure 35.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB).
- Avoid stubs on the transmission lines.
- Avoid signal routing in parallel to the transmission lines or crossing the transmission lines on a buried metal layer.
- Do not route the microstrip lines below discrete components or other mechanics placed on the top layer.

An example of a suitable RF circuit design is illustrated in Figure 35. In this case, the **ANT1** and **ANT2** pins are directly connected to SMA connectors by means of suitable 50 Ω transmission lines, designed with a suitable layout.

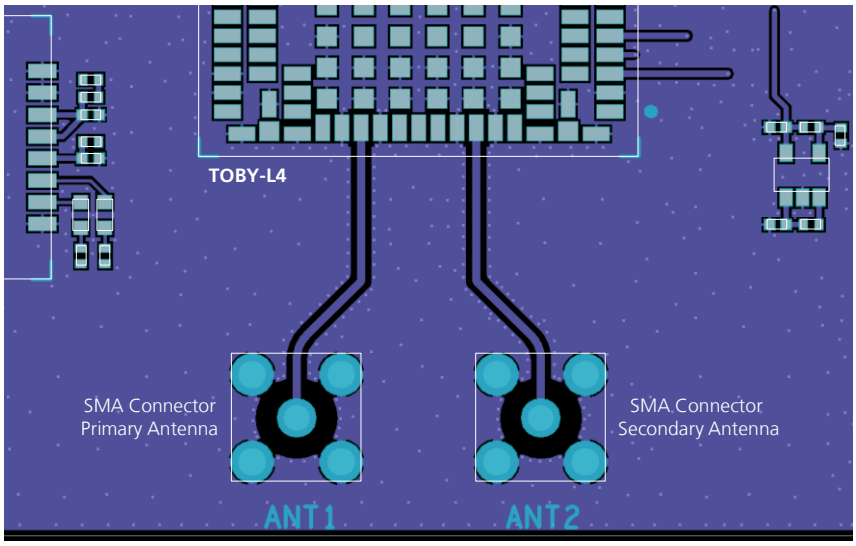

Figure 35: Example of the circuit and layout for antenna RF circuits on the application board

Guidelines for RF termination design

RF terminations must provide a characteristic impedance of 50 Ω as well as the RF transmission lines up to the RF terminations themselves, to match the characteristic impedance of the **ANT1** / **ANT2** ports of the modules.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible any performance degradation due to antennas mismatch, the RF terminations must provide optimal return loss (or VSWR) figures over all the operating frequencies, as summarized in Table 8 and Table 9.

If external antennas are used, the antenna connectors represent the RF termination on the PCB:

- Use suitable 50 Ω connectors providing a correct PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to the annular pads of the four GND posts, as shown in Figure 35.
  - U.FL surface-mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under RF connectors and close to buried vias, in order to remove stray capacitance and thus keep the RF line 50 Ω, e.g. the active pad of U.FL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

If integrated antennas are used, the RF terminations are represented by the integrated antennas themselves. The following guidelines should be followed:

- Use antennas designed by an antenna manufacturer, providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of a wavelength of the minimum frequency that must be radiated. As a numerical example,

  Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna matching relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place antennas within a closed metal case.
- Do not place the antennas in close vicinity to the end user since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antennas far from sensitive analog systems or employ countermeasures to reduce EMC issues.
- Take care of interaction between co-located RF systems since the LTE/3G/2G transmitted power may interact or disturb the performance of companion systems.
- Place the two LTE antennas providing low Envelope Correlation Coefficient (ECC) between the primary (**ANT1**) and secondary (**ANT2**) antenna: the antenna 3D radiation patterns should have lobes in different directions. The ECC between the primary and secondary antennas needs to be low enough to comply with the radiated performance requirements specified by related certification schemes, as indicated in Table 10.
- Place the two LTE antennas providing enough high isolation (see Table 10) between the primary (**ANT1**) and secondary (**ANT2**) antennas. The isolation depends on the distance between antennas (separation of at least a quarter wavelength required for good isolation), antenna type (using antennas with different polarization improves isolation), and the antenna 3D radiation patterns (uncorrelated patterns improve isolation).

Examples of antennas

Table 24 lists some examples of possible internal on-board surface-mount antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PA.711.A	Warrior II	GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm

Table 24: Examples of internal surface-mount antennas

Table 25 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part Number	Product Name	Description
Taoglas	FXUB66.07.0150C	Maximus	GSM / WCDMA / LTE PCB Antenna with cable and U.FL 698..960 MHz, 1390..1435 MHz, 1575.42 MHz, 1710..2170 MHz, 2300..2700 MHz, 3400..3600 MHz, 4800..6000 MHz 120.2 x 50.4 mm
Ethertronics	5001537	Prestta	GSM / WCDMA / LTE PCB Antenna with cable 704..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 80.0 x 18.0 mm

Table 25: Examples of internal antennas with cable and connector

Table 26 lists some examples of possible external antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE adhesive-mount antenna with cable and SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 105 x 30 x 7.7 mm
Taoglas	MA241.BI.001	Genesis	GSM / WCDMA / LTE MIMO 2-in-1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2690 MHz 205.8 x 58 x 12.4 mm
Laird Tech.	TRA6927M3PW-001		GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Laird Tech.	CMD69273-30NM		GSM / WCDMA / LTE ceiling-mount MIMO antenna with cables & N-type(M) 698..960 MHz, 1710..2700 MHz 43.5 x Ø 218.7 mm
Pulse Electronics	WA700/2700SMA		GSM / WCDMA / LTE clip-mount MIMO antenna with cables and SMA(M) 698..960 MHz,1710..2700 MHz 149 x 127 x 5.1 mm

Table 26: Examples of external antennas

2.4.2 Antenna detection interface (ANT_DET)

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 36 and Table 27 describe the recommended schematic / components for the antennas detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antennas' assembly to achieve primary and secondary antenna detection functionality.

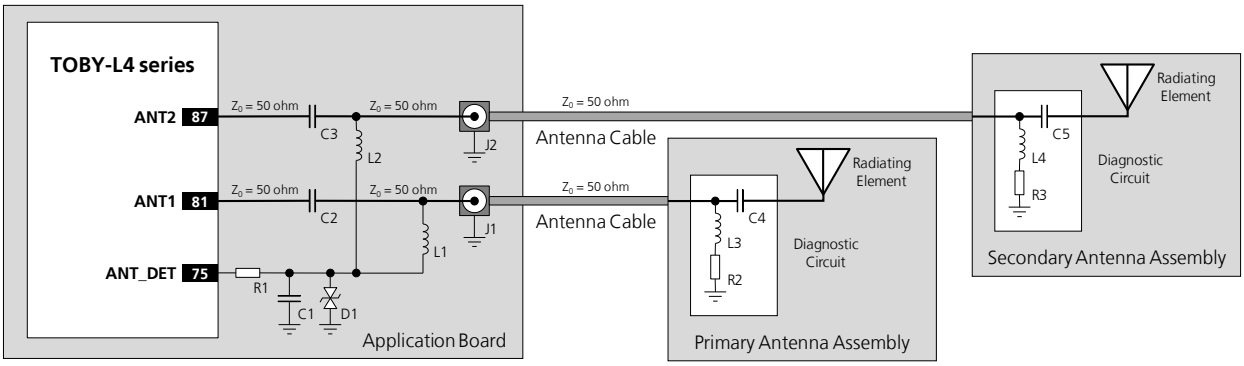

Figure 36: Suggested schematic for the antenna detection circuit on the application board and the diagnostic circuit on the antennas assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2, C3	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1, L2	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1, J2	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C4, C5	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3, L4	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2, R3	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 27: Suggested components for the antenna detection circuit on the application board and the diagnostic circuit on the antennas assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 36 and Table 27 are explained here:

- When antenna detection is forced by the AT+UANTR command, **ANT_DET** generates a DC current measuring the resistance (R2 // R3) from the antenna connectors (J1, J2) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT1** / **ANT2** pins (C2, C3) and at the antenna radiating element (C4, C5) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1, L2) and in series at the diagnostic resistor (L3, L4), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 36) are needed at the **ANT_DET** pin as ESD protection.
- The **ANT1** / **ANT2** pins must be connected to the antenna connector by means of a transmission line with a nominal characteristic impedance as close as possible to 50 Ω.

The DC impedance at the RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas without the diagnostic circuit of Figure 36, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no means to distinguish between a defect on the antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for a PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from an ANT connector to a radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of the load resistor.

For example:

Consider an antenna with a built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see the u-blox AT Commands Manual [2]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) indicate a short to GND at the antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an incorrect connection, damaged antenna or wrong value of antenna load resistor for diagnostics.
- The reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to the antenna cable length, the antenna cable capacity or the measurement method used.

☞ If the primary / secondary antenna detection function is not required by the customer application, the **ANT_DET** pin can be left unconnected and the **ANT1** / **ANT2** pins can be directly connected to the related antenna connector by means of a 50 Ω transmission line as illustrated in Figure 35.

2.4.2.2 Guidelines for ANT_DET layout design

The recommended layout for the primary antenna detection circuit to be provided on the application board to achieve the primary antenna detection functionality, implementing the recommended schematic illustrated in Figure 36 and Table 27, is explained here:

- The **ANT1** / **ANT2** pins must be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT1** / **ANT2** pins (C2, C3) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductors in series at the **ANT_DET** pin (L1, L2) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT_DET** line must be placed as ESD protection.

2.5 SIM interfaces

2.5.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

TOBY-L4 series modules provide two SIM interfaces for the direct connection of two external SIM cards/chips, which can be used alternatively (only one SIM at a time can be used for network access):

- SIM0 interface (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins), enabled by default
- SIM1 interface (**VSIM1**, **SIM1_IO**, **SIM1_CLK**, **SIM1_RST** pins), alternatively enabled

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE/3G/2G network.

Removable UICC / SIM card contact mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM** / **VSIM1**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST** / **SIM1_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK** / **SIM1_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO** / **SIM1_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 6 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product's lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without an integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as:

- Case Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to **VSIM** / **VSIM1**
- Case Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to **SIM_RST** / **SIM1_RST**
- Case Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK** / **SIM1_CLK**
- Case Pin 5 = UICC Contact C4 = AUX1 (Aux.contact) → It must be left not connected
- Case Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to **GND**
- Case Pin 2 = UICC Contact C6 = VPP (Progr. supply) → It can be left not connected
- Case Pin 3 = UICC Contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO** / **SIM1_IO**
- Case Pin 4 = UICC Contact C8 = AUX2 (Aux. contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM0 or the SIM1 interface of TOBY-L4 series modules as illustrated in Figure 37, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** or the **VSIM1** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** or the **SIM1_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** or the **SIM1_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** or the **SIM1_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. The ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, a higher protection level can be required if the lines are externally accessible on the application device.
- Limit the capacitance and series resistance on each SIM signal to match the SIM requirements (27.7 ns is the maximum allowed rise time on the clock line, 1.0 µs is the maximum allowed rise time on the data and reset lines).

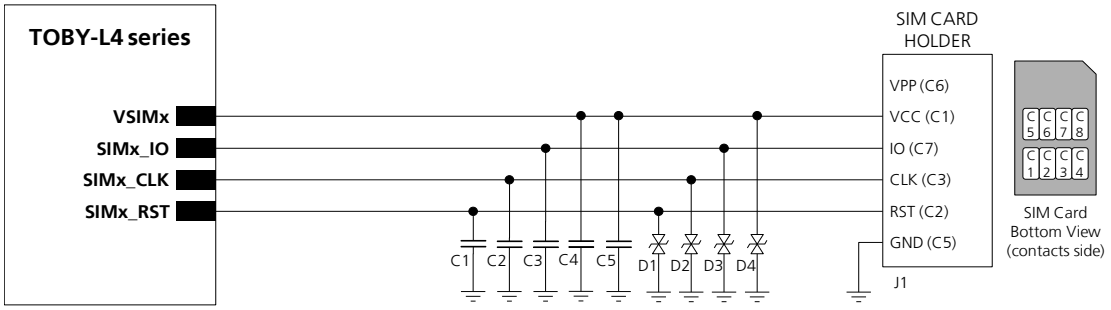

Figure 37: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder, 6 p, without card presence switch	Various manufacturers, as C707 10M006 136 2 - Amphenol

Table 28: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

Guidelines for single SIM chip connection

A solderable SIM chip (M2M UICC Form Factor) must be connected the SIM0 / SIM1 interface of TOBY-L4 series modules as illustrated in Figure 38.

Follow these guidelines to connect the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** or the **VSIM1** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** or the **SIM1_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** or the **SIM1_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** or the **SIM1_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM lines.
- Limit the capacitance and series resistance on each SIM signal to match the SIM requirements (20.5 ns is the maximum rise time on the clock line, 1.0 µs is the maximum rise time on the data and reset lines).

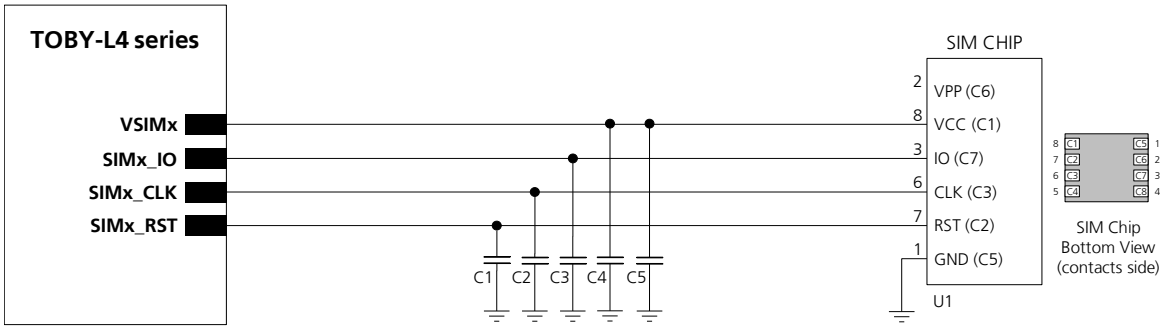

Figure 38: Application circuits for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 29: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

Guidelines for single SIM card connection with detection

If the optional SIM card detection feature is required by the application, then a removable SIM card placed in a SIM card holder must be connected to the SIM0 interface of TOBY-L4 series modules as illustrated in Figure 39:

Follow these guidelines to connect the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW2 pin as illustrated in Figure 39) to the **GPIO5** input pin of the module.
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW1 pin as illustrated in Figure 39) to the **V_INT** 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 resistor in Figure 39.
- Provide a weak (e.g. 470 kΩ) pull-down resistor at the SIM detection line, as the R2 resistor in Figure 39.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line, close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (HBM), so that, according to the EMC/ESD requirements of the custom application, a higher protection level can be required if the lines are externally accessible on the application device.
- Limit the capacitance and series resistance on each SIM signal to match the SIM requirements (20.5 ns is the maximum rise time on the clock line, 1.0 µs is the maximum rise time on the data and reset lines).

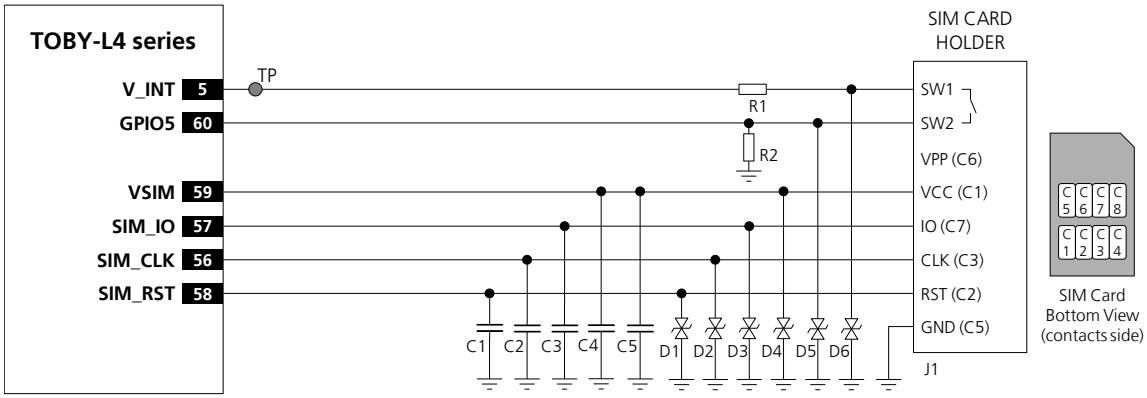

Figure 39: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, … , D6	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM Card Holder, 6 + 2 p, with card presence switch	Various manufacturers, as CCM03-3013LFT R102 - C&K

Table 30: Example of components for the connection to a single removable SIM card, with SIM detection implemented

Guidelines for dual SIM card / chip connection

Two SIM cards / chips can be connected to the SIM interfaces of TOBY-L4 modules as illustrated in Figure 40.

TOBY-L4 series modules do not support the usage of two SIMs at the same time, but two SIMs can be populated on the application board:

- connecting the first SIM to the SIM0 interface of the module and connecting the second SIM to the SIM1 interface of the module, as illustrated in Figure 40 top side

  In this case, the SIM interface and the related external SIM card / chip to be used can be selected by means of the AT+XSIMSWITCH command (see u-blox AT Commands Manual [2]) or by means of uCPU application, performing the SIM switch operation
- providing a suitable switch to connect only the first or only the second SIM at a time to the SIM0 interface of the module, as illustrated in Figure 40 bottom side

  In this case, if the SIM hot insertion / removal feature is enabled on the **GPIO5** pin by AT commands (see sections 1.8.2 and 1.13, and the u-blox AT Commands Manual [2], +UGPIOC, +UDCONF=50 commands) or by means of uCPU application, than the switch from the first to the second external SIM can be properly done when a Low logic level is present on the **GPIO5** pin ("SIM not inserted" = SIM interface not enabled), without the necessity of a module re-boot, so that the SIM interface will be re-enabled by the module to use the second SIM when a high logic level is re-applied on the **GPIO5** pin. The application processor will drive the SIM switch using its own GPIO to properly select the SIM that is used by the module. Another GPIO may be used to handle the SIM hot insertion / removal function of TOBY-L4 series modules, which can also be handled by other external circuits or by the cellular module GPIO according to the application requirements.

The dual SIM connection circuit illustrated in Figure 40 can be implemented for SIM chips as well.

If it is required to switch between more than 2 SIMs, a circuit similar to the one illustrated in Figure 40 bottom side can be implemented, using suitable switches.

Follow these guidelines to connect the module to two external UICC / SIM:

- Connect the contact C1 (VCC) of the first external UICC / SIM to the **VSIM** pin of the module and the one of the second external UICC / SIM to the **VSIM1** pin of the module.
- Connect the contact C7 (I/O) of the first external UICC / SIM to the **SIM_IO** pin of the module and the one of the second external UICC / SIM to the **SIM1_IO** pin of the module.
- Connect the contact C3 (CLK) of the first external UICC / SIM to the **SIM_CLK** pin of the module and the one of the second external UICC / SIM to the **SIM1_CLK** pin of the module.
- Connect the contact C2 (RST) of the first external UICC / SIM to the **SIM_RST** pin of the module and the one of the second external UICC / SIM to the **SIM1_RST** pin of the module.
- Connect the contact C5 (GND) of each external UICC / SIM to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply (**VSIM** / **VSIM1**), close to the related pad of each external UICC / SIM, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of each external SIM connector, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM card holders.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each pad of each external SIM connector, according to the EMC/ESD requirements of the custom application.
- Limit the capacitance and series resistance on each SIM signal to match the SIM requirements (20.5 ns is the maximum rise time on the clock line, 1.0 µs is the maximum rise time on the data and reset lines).
- If a circuit as the one illustrated in Figure 40 bottom side is implemented, use a suitable low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) 2-throw analog switch (e.g. Fairchild FSA2567) as SIM switch to ensure high-speed data transfer according to SIM requirements.

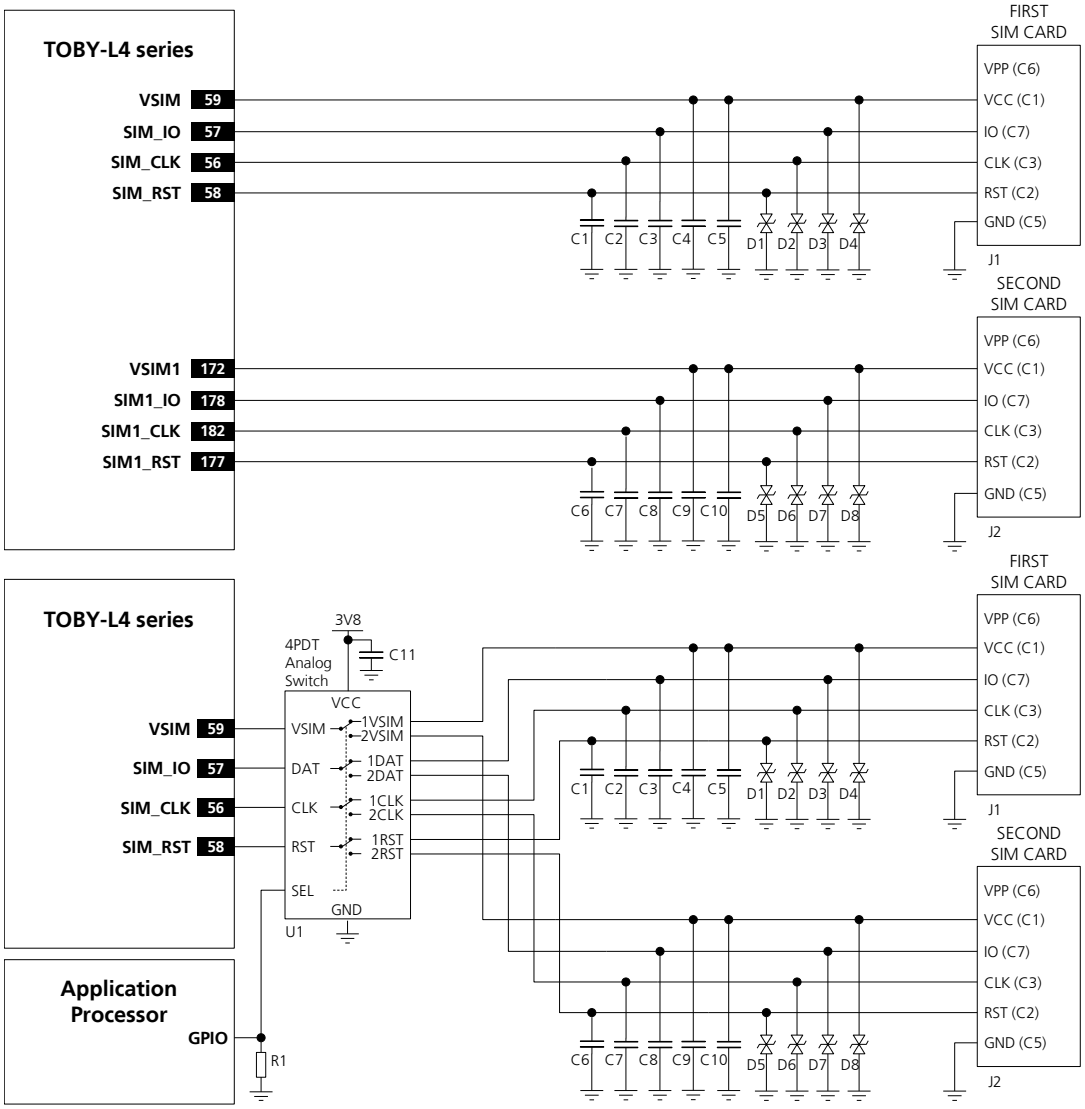

Figure 40: Application circuits for the connection to two removable SIM cards, with SIM detection not implemented

Reference	Description	Part Number – Manufacturer
C1 – C4, C6 – C9	33 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H330JZ01 – Murata
C5, C10, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 – Murata
D1 – D8	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL- Yageo Phycomp
J1, J2	SIM Card Holder, 6 + 2 p., with card presence switch	CCM03-3013LFT R102 - C&K Components
U1	4PDT Analog Switch, with Low On-Capacitance and Low On-Resistance	FSA2567 - Fairchild Semiconductor

Table 31: Example of components for the connection to two removable SIM cards, with SIM detection not implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interfaces lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** for the SIM0 interface, and **VSIM1**, **SIM1_IO**, **SIM1_CLK**, **SIM1_RST** for the SIM1 interface) may be critical if the SIM card is placed far away from the TOBY-L4 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with the RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE/3G/2G receiver channels whose carrier frequency is coincidental with the harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 37 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect the module SIM pins near the SIM connector.

Limit the capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 USB interface

2.6.1.1 Guidelines for USB circuit design

Different application circuits can be implemented for the USB interface according to specific use-case:

- USB 2.0 interface, with the module acting as USB device, as illustrated in Figure 41 and Table 32
- USB 2.0 interface, with the module acting as USB host, as illustrated in Figure 42 and Table 33
- USB 3.0 interface, with the module acting as USB device, as illustrated in Figure 43 and Table 34

USB pull-up or pull-down resistors and external series resistors on the **USB_D+** and **USB_D–** lines as required by the USB 2.0 specification [3] are part of the module USB pins driver and do not need to be externally provided.

Series DC decoupling capacitors are internally provided on the **USB_SSTX+** and **USB_SSTX–** lines as required by the USB 3.0 specification [4] and do not need to be externally provided.

The **USB_SSTX+/USB_SSTX–** USB Super-Speed differential transmitter data output lines of the module must be connected to the USB Super-Speed differential receiver data input lines of the external USB 3.0 host.

The **USB_SSRX+/USB_SSRX–** USB Super-Speed differential receiver data input lines of the module must be connected to the USB Super-Speed differential transmitter data output lines of the external USB 3.0 host, with series DC decoupling capacitors being provided on the host side as per the USB 3.0 specification [4].

Routing the USB pins to a connector, they will be externally accessible on the application device. According to the EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to the accessible point on the line connected to this pin.

☞ The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins, close to the accessible points.

The USB pins of the modules can be directly connected to the USB host application processor without additional ESD protections if they are not externally accessible or according to EMC/ESD requirements.

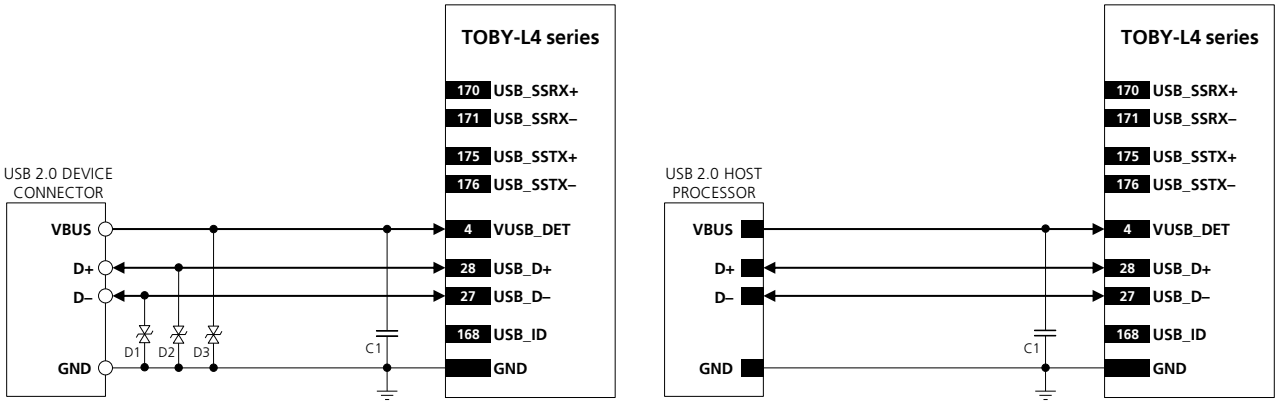

Figure 41: USB 2.0 interface application circuits, with TOBY-L4 series module acting as a USB device

Reference	Description	Part Number - Manufacturer
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics

Table 32: Component for USB 2.0 interface application circuits, with TOBY-L4 series module acting as a USB device

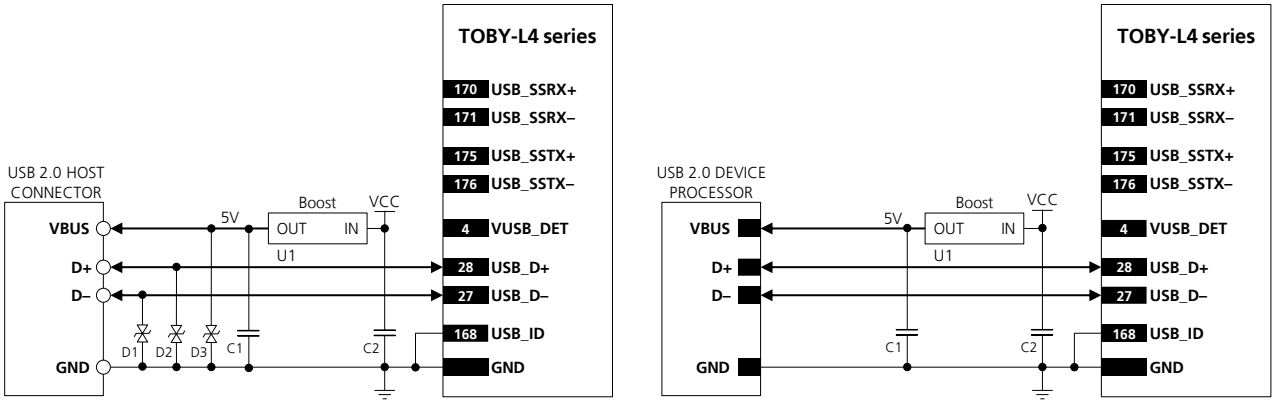

Figure 42: USB 2.0 interface application circuits, with TOBY-L4 series module acting as a USB host

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
U1	DC/DC Boost Regulator	Various Manufacturer

Table 33: Component for USB 2.0 interface application circuits, with TOBY-L4 series module acting as a USB host

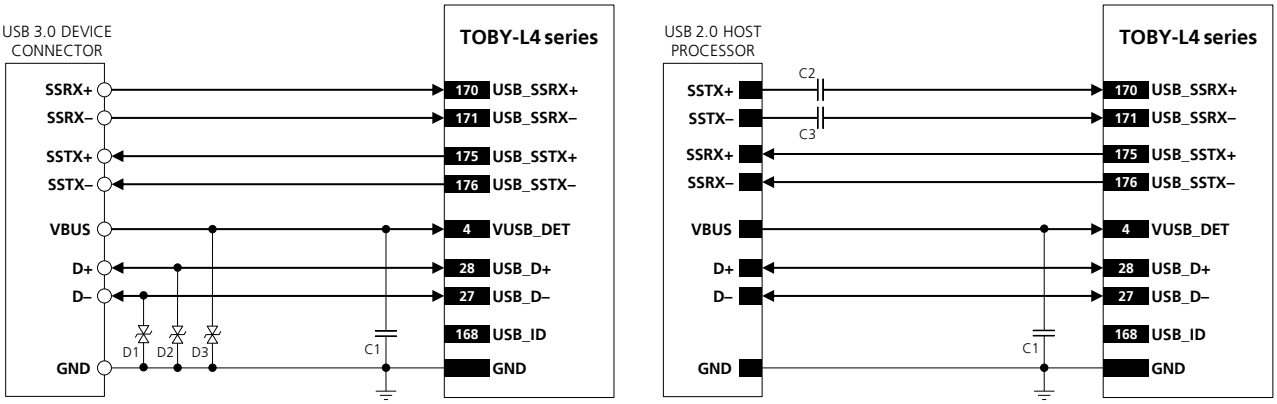

Figure 43: USB 3.0 interface application circuits, with TOBY-L4 series module acting as a USB device

Reference	Description	Part Number - Manufacturer
C1, C2, C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics

Table 34: Component for USB 3.0 interface application circuits, with TOBY-L4 series module acting as a USB device

☞ USB High-Speed 2.0 host role is not supported by the "50" product versions.

☞ USB Super-Speed 3.0 compliant interface will be supported by future firmware versions.

☞ If the USB interface pins are not used, they can be left unconnected on the application board, but it is recommended to provide accessible test points directly connected to the **VUSB_DET**, **USB_D+**, **USB_D–** pins, for diagnostic and FW update purposes.

2.6.1.2 Guidelines for USB layout design

The **USB_D+/USB_D–**, **USB_SSTX+/USB_SSTX–** and **USB_SSRX+/USB_SSRX–** lines require accurate layout design to achieve reliable signaling at the high speed data rates (up to 480 Mbit/s or up to 5 Gbit/s) supported by the USB 2.0 or USB 3.0 interface.

The characteristic impedance of the **USB_D+/USB_D–**, **USB_SSTX+/USB_SSTX–** and **USB_SSRX+/USB_SSRX–** lines is specified by the USB 2.0 specification [3] and the USB 3.0 specification [4]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if the PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route **USB_D+/USB_D–**, **USB_SSTX+/USB_SSTX–** and **USB_SSRX+/USB_SSRX–** lines as a differential pair
- Route **USB_D+/USB_D–**, **USB_SSTX+/USB_SSTX–** and **USB_SSRX+/USB_SSRX–** lines as short as possible
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω
- Consider design rules for **USB_D+/USB_D–**, **USB_SSTX+/USB_SSTX–** and **USB_SSRX+/USB_SSRX–** similar to RF transmission lines, these being coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area

Figure 44 and Figure 45 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented for a 4-layer PCB stack-up herein illustrated; the second transmission line can be implemented for a 2-layer PCB stack-up herein illustrated.

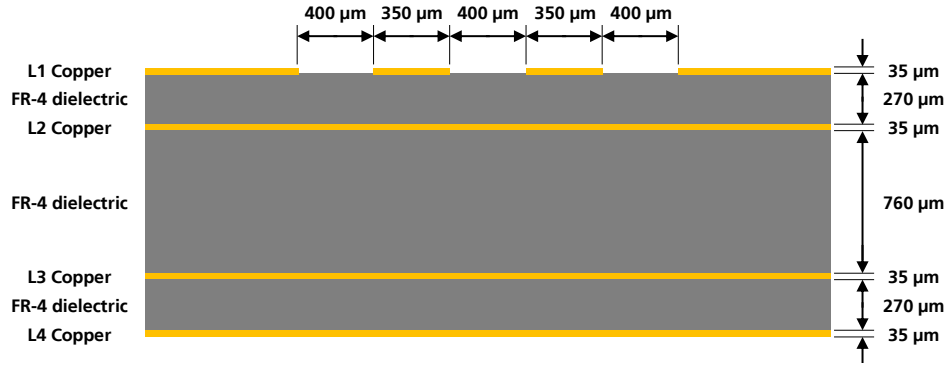

Figure 44: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

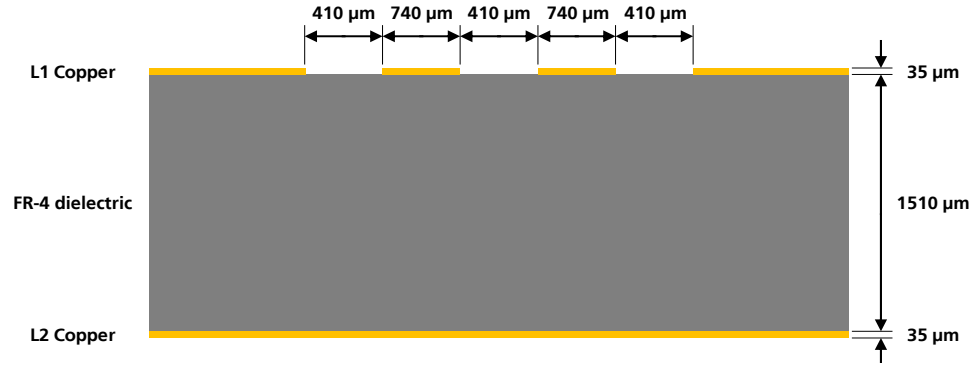

Figure 45: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.6.2 UART interfaces

UART interfaces are not supported by the "50" product version, except for trace logging (diagnostic purposes) and Ring Indicator functionality over the UART0 interface.

2.6.2.1 Guidelines for UART circuit design

4-wire UART

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V external Processor / Device is used, the circuit should be implemented as illustrated in Figure 46.

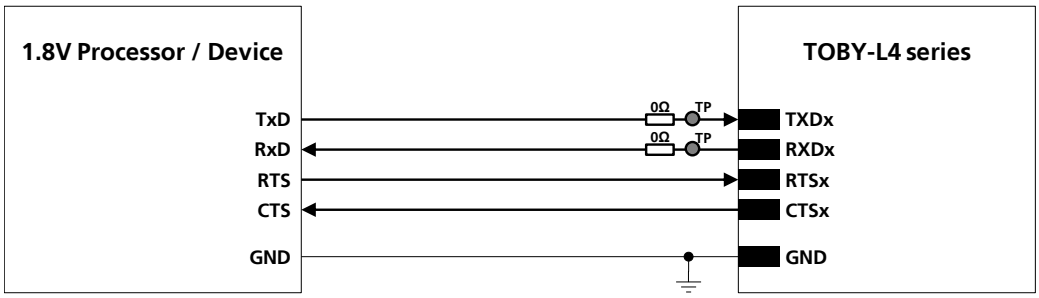

Figure 46: 4-wire UART interface application circuit to connect an external 1.8 V processor / device

If a 3.0 V external Processor / Device is used, then it is recommended to connect the 1.8 V UART interface of the module by means of appropriate unidirectional voltage translators using the module **V_INT** output as a 1.8 V supply for the voltage translators on the module side, as illustrated in Figure 47.

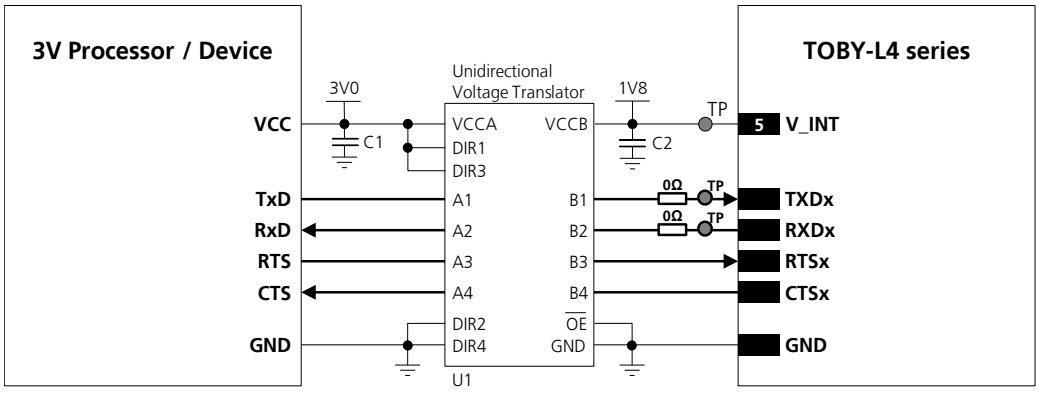

Figure 47: 4-wire UART interface application circuit to connect an external 3.0V processor / device

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774[16] - Texas Instruments

Table 35: Component for 4-wire UART interface application circuit to connect an external 3.0V processor / device

Test-Points for diagnostic access are recommended to be provided on the UART0 **TXD** and **RXD** lines. They are not required on other UART lines.

[16] Voltage translator providing partial power down feature so that the external 3.0 V supply can be ramped up before the **V_INT** 1.8 V supply

2-wire UART

If the functionality of the **CTSx** and **RTSx** are not required in the application, or the lines are not available, then:

- Consider to connect the module **RTSx** input line to GND or to the **CTSx** output line of the module, since the module requires **RTSx** active (low electrical level) if HW flow-control is enabled

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V external Processor / Device is used, the circuit that should be implemented as illustrated in Figure 48.

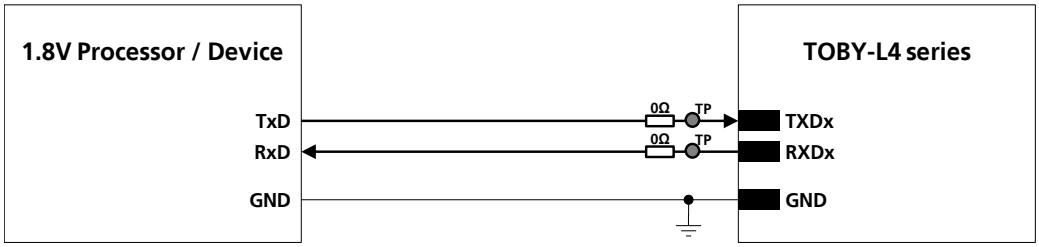

Figure 48: 2-wire UART interface application circuit to connect an external 1.8V processor / device

If a 3.0 V external Processor / Device is used, then it is recommended to connect the 1.8 V UART interface of the module by means of appropriate unidirectional voltage translators using the module **V_INT** output as a 1.8 V supply for the voltage translators on the module side, as illustrated in Figure 49.

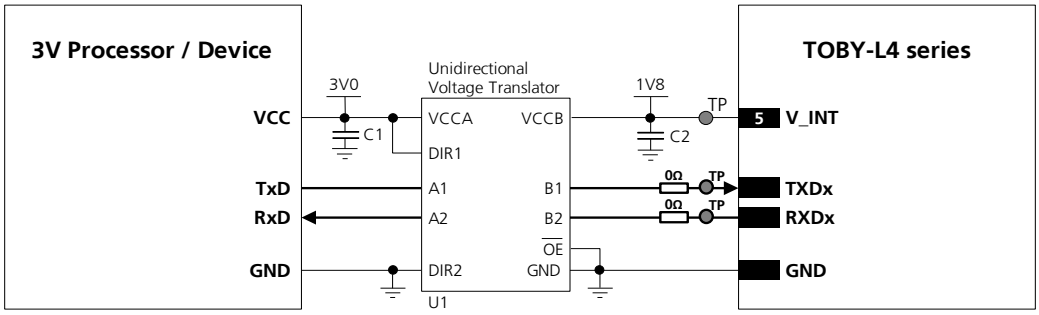

Figure 49: 2-wire UART interface application circuit to connect an external 3.0 V processor / device

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245[17] - Texas Instruments

Table 36: Component for 2-wire UART interface application circuit to connect an external 3.0 V processor / device

☞ Test-Points for diagnostic access are recommended to be provided on the UART0 **TXD** and **RXD** lines for diagnostic purposes. Test-Points are not required on other UART lines.

[17] Voltage translator providing partial power down feature so that the external 3.0 V supply can be ramped up before **V_INT** 1.8 V supply

Ring Indicator

If a 1.8 V external Processor / Device is used, the Ring Indicator circuit should be implemented as illustrated in Figure 50.

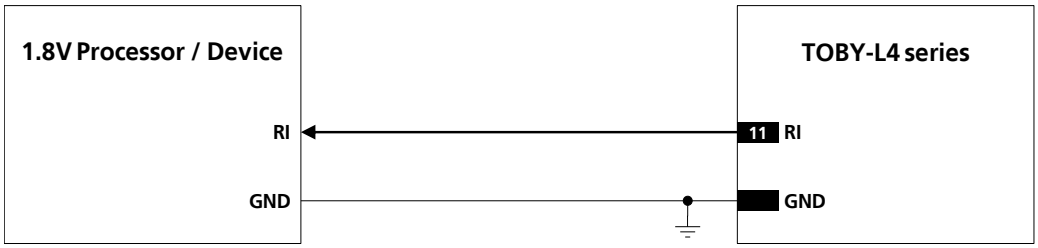

Figure 50: Ring Indicator application circuit to connect an external 1.8V processor / device

If a 3.0 V external Processor / Device is used, then it is recommended to connect the 1.8 V Ring Indicator output of the module by means of appropriate unidirectional voltage translators using the module **V_INT** output as a 1.8 V supply for the voltage translator on the module side, as illustrated in Figure 51.

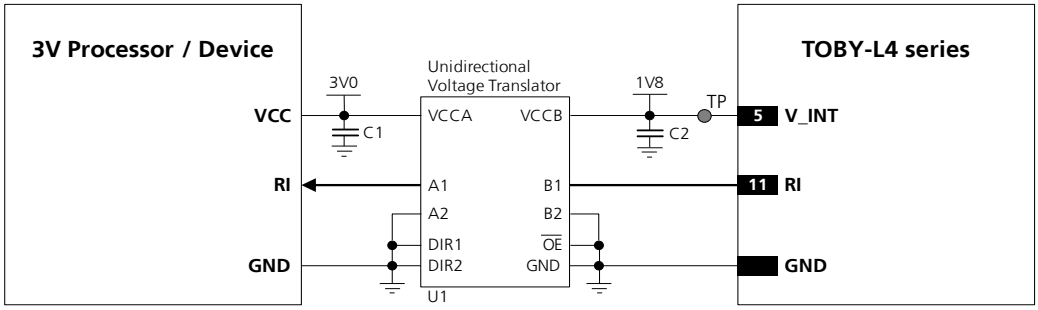

Figure 51: Ring Indicator application circuit to connect an external 3.0V processor / device

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245[18] - Texas Instruments

Table 37: Component for the Ring Indicator application circuit to connect an external 3.0V processor / device

[18] Voltage translator providing partial power down feature so that the external 3.0 V supply can be ramped up before the **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V external Processor / Device is used, the voltage scaling from any 3.0 V output of the external Processor / Device to the corresponding 1.8 V input of the module can be implemented as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the module for the correct selection of the voltage divider resistance values and mind that any DTE signal connected to the module must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a clean boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module to the corresponding 3.0 V input of the external Processor / Device can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the external Processor / Device (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

☞ Do not apply voltage to any UART interfaces pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.

☞ The ESD sensitivity rating of UART interfaces pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the UART interfaces pins are not used, they can be left unconnected on the application board, but it is recommended to provide accessible test points directly connected to the UART0 **TXD** and **RXD** pins for diagnostic purposes.

2.6.2.2 Guidelines for UART layout design

The UART serial interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.3 SPI interfaces

SPI interfaces are not supported by the "50" product version.

2.6.3.1 Guidelines for SPI circuit design

TOBY-L4 series modules include up to two 1.8 V Serial Peripheral Interfaces to communicate with external SPI slave devices, with the module acting as SPI master, by means of the uCPU API.

Figure 52 describes a possible application circuit for the SPI0 interface, where two SPI slave devices are connected to the module using the two SPI0 Chip Select 0 (**SPI_CS** pin) and SPI0 Chip Select 1 (**GPIO4** pin) to select the specific SPI slave device.

The external SPI slave device must provide compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V SPI interface of the module to the external 3.0 V (or similar) SPI device by means of appropriate unidirectional voltage translators (e.g. TI SN74AVC4T774 or SN74AVC2T245, providing partial power down feature so that the digital audio device 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply), using the module's **V_INT** output as a 1.8 V supply for the voltage translators on the module side.

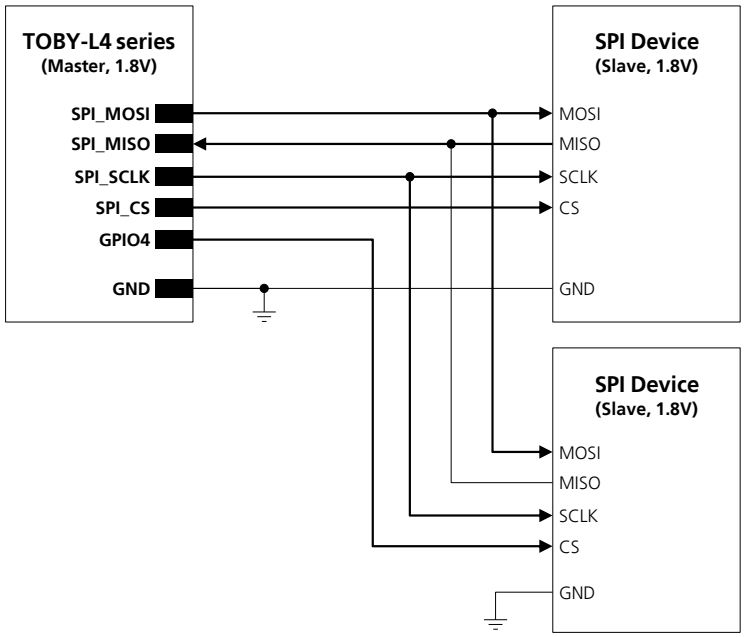

Figure 52: SPI interface application circuit for connecting two external SPI slave devices

Do not apply voltage to any SPI interface pins before the switch-on of the SPI supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.

The ESD sensitivity rating of SPI interfaces pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

If the SPI interfaces pins are not used, they can be left unconnected on the application board.

2.6.3.2 Guidelines for SPI layout design

The SPI serial interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.4 DDC (I²C) interfaces

DDC (I²C) interfaces are not supported by the "50" product version.

2.6.4.1 General guidelines for DDC (I²C) circuit design

The DDC I²C-bus pins of the module are open drain outputs conforming to the I²C bus specifications [6]. External pull-up resistors to a suitable 1.8 V supply (e.g. **V_INT**) are required for operations: for example, 4.7 kΩ resistors can be commonly used.

Connect the DDC (I²C) pull-ups to the **V_INT** 1.8 V supply source, or another 1.8 V supply source enabled after **V_INT** (e.g., as the GNSS 1.8 V supply present in Figure 54 application circuit), as any external signal connected to the DDC (I²C) interface must not be set high before the switch-on of the **V_INT** supply of DDC (I²C) pins, to avoid latch-up of circuits and allow a clean boot of the module.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus will increase the capacitance. If the bus capacitance is increased, use pull-up resistors with a nominal resistance value lower than 4.7 kΩ, to match the I²C bus specifications [6] regarding the rise and fall times of the signals.

Figure 53 and Table 38 describe typical application circuits for connecting TOBY-L4 series modules to 1.8 V I2C devices (see Figure 53 top side) or 3 V I2C devices (see Figure 53 bottom side).

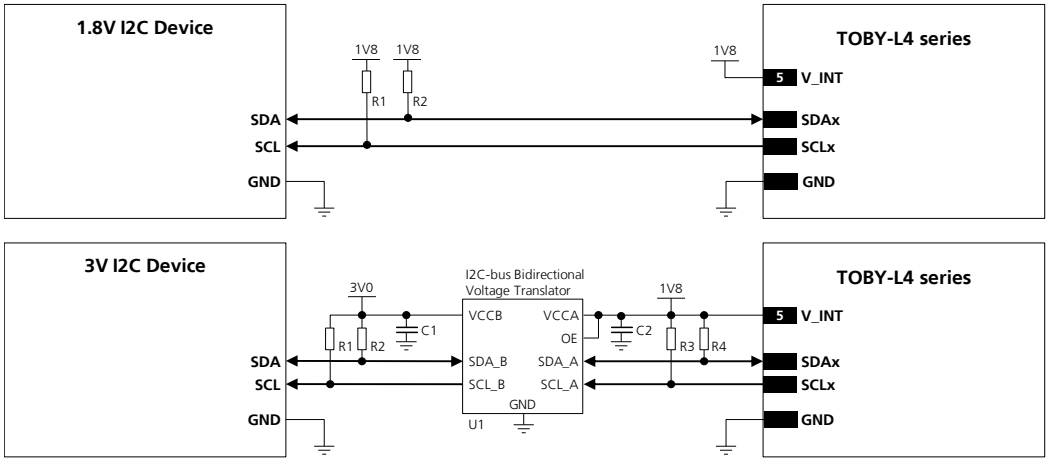

Figure 53: Application circuit for connecting TOBY-L4 series modules to 1.8 V or 3 V I2C devices

Reference	Description	Part Number - Manufacturer
R1, R2, R3, R4	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR[19] - Texas Instruments

Table 38: Components for connecting TOBY-L4 series modules to 1.8 V or 3 V I2C devices

The ESD sensitivity rating of the DDC (I²C) pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

If the pins are not used as DDC bus interface, they can be left unconnected.

[19] Voltage translator providing partial power down feature so that the external 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Connection with u-blox 1.8 V GNSS receivers

Figure 54 shows an application circuit for connecting the cellular modules to a u-blox 1.8 V GNSS receiver.

- **SDA** / **SCL** pins of the cellular module are directly connected to the relative I^2C pins of the u-blox 1.8 V GNSS receiver, with appropriate pull-up resistors connected to the 1.8 V GNSS supply enabled after the **V_INT** supply of the I^2C pins of the cellular module.
- **GPIO2** pin is connected to the shutdown input pin (**SHDNn**) of the LDO regulators providing the 1.8 V supply rail for the u-blox 1.8 V GNSS receiver implementing the "GNSS enable" function, with an appropriate pull-down resistor mounted on the **GPIO2** line to avoid an improper switch-on of the u-blox GNSS receiver.
- **GPIO3** and **GPIO4** pins are directly connected respectively to the **TXD1** and **EXTINT0** pins of the u-blox 1.8 V GNSS receiver providing "GNSS Tx data ready" and "GNSS RTC sharing" functions.

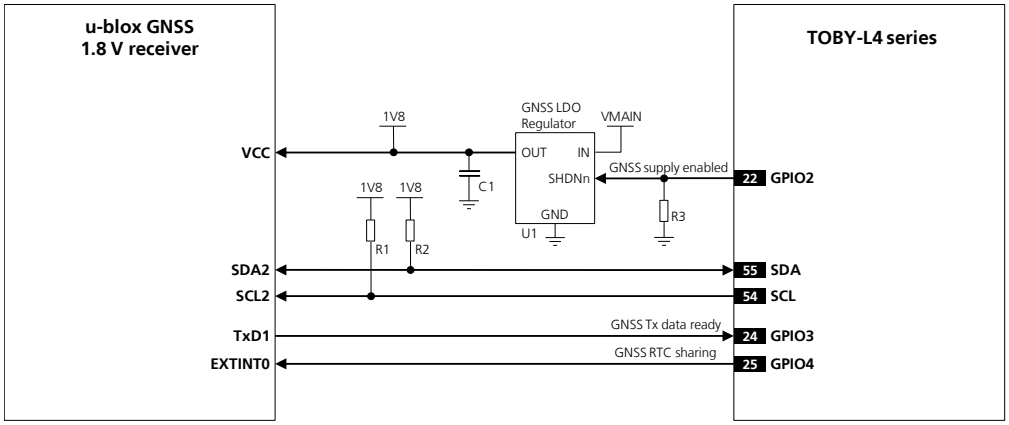

Figure 54: Application circuit for connecting TOBY-L4 series modules to u-blox 1.8 V GNSS receivers

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1, C1	Voltage Regulator for GNSS receiver and capacitor	See GNSS receiver Hardware Integration Manual

Table 39: Components for connecting TOBY-L4 series modules to u-blox 1.8 V GNSS receivers

☞ Custom functions over GPIO pins, to improve the integration with u-blox positioning chips and modules, will be supported by future firmware versions.

Figure 55 illustrates an alternative application circuit solution in which the cellular module supplies a u-blox 1.8 V GNSS receiver. The **V_INT** 1.8 V regulated supply output of the cellular module can be used as supply source for a u-blox 1.8 V GNSS receiver (u-blox 6 generation receiver or newer) instead of using an external voltage regulator, as shown in Figure 54. The **V_INT** supply is able to support the maximum current consumption of these positioning receivers.

The internal switching step-down regulator that generates the **V_INT** supply is set to 1.8 V (typical) when the cellular module is switched on and it is disabled when the module is switched off.

The supply of the u-blox 1.8 V GNSS receiver can be switched off using an external p-channel MOS controlled by the **GPIO2** pin of the cellular modules by means of a suitable inverting transistor as shown in Figure 55, implementing the "GNSS supply enable" function. If this feature is not required, the **V_INT** supply output can be directly connected to the u-blox 1.8 V GNSS receiver, so that it will switch on when **V_INT** output is enabled.

According to the **V_INT** supply output voltage ripple characteristic specified in the TOBY-L4 series Data Sheet [1]:

- Additional filtering may be needed to properly supply an external LNA, depending on the characteristics of the used LNA, adding a series ferrite bead and a bypass capacitor (e.g. the Murata BLM15HD182SN1 ferrite bead and the Murata GRM1555C1H220J 22 pF capacitor) at the input of the external LNA supply line.

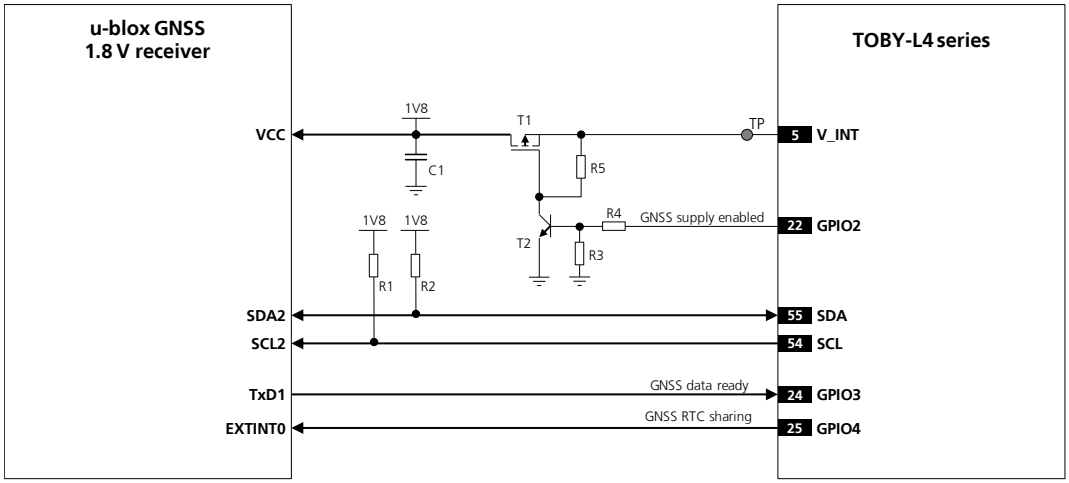

Figure 55: Application circuit for connecting TOBY-L4 series modules to u-blox 1.8 V GNSS receivers using V_INT as supply

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R4	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R5	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
T1	P-Channel MOSFET Low On-Resistance	IRLML6401 - International Rectifier or NTZS3151P - ON Semi
T2	NPN BJT Transistor	BC847 - Infineon
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata

Table 40: Components for connecting TOBY-L4 series modules to u-blox 1.8 V GNSS receivers using V_INT as supply

☞ Custom functions over GPIO pins, to improve the integration with u-blox positioning chips and modules, will be supported by future firmware versions.

Connection with u-blox 3.0 V GNSS receivers

Figure 56 shows an application circuit for connecting the cellular modules to a u-blox 3.0 V GNSS receiver:

- As the **SDA** and **SCL** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related I²C pins of the u-blox 3.0 V GNSS receiver must be provided using a suitable I²C-bus Bidirectional Voltage Translator with appropriate pull-up resistors (e.g. the TI TCA9406 additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V_INT** 1.8 V cellular supply).
- **GPIO2** pin is connected to the shutdown input pin (**SHDNn**) of the LDO regulators providing the 3.0 V supply rail for the u-blox 3.0 V GNSS receiver implementing the "GNSS enable" function, with an appropriate pull-down resistor mounted on the **GPIO2** line to avoid an improper switch-on of the u-blox GNSS receiver.
- As the **GPIO3** and **GPIO4** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related pins of the u-blox 3.0 V GNSS receiver must be provided using a suitable Unidirectional General Purpose Voltage Translator (e.g. TI SN74AVC2T245, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V_INT** 1.8 V cellular supply).

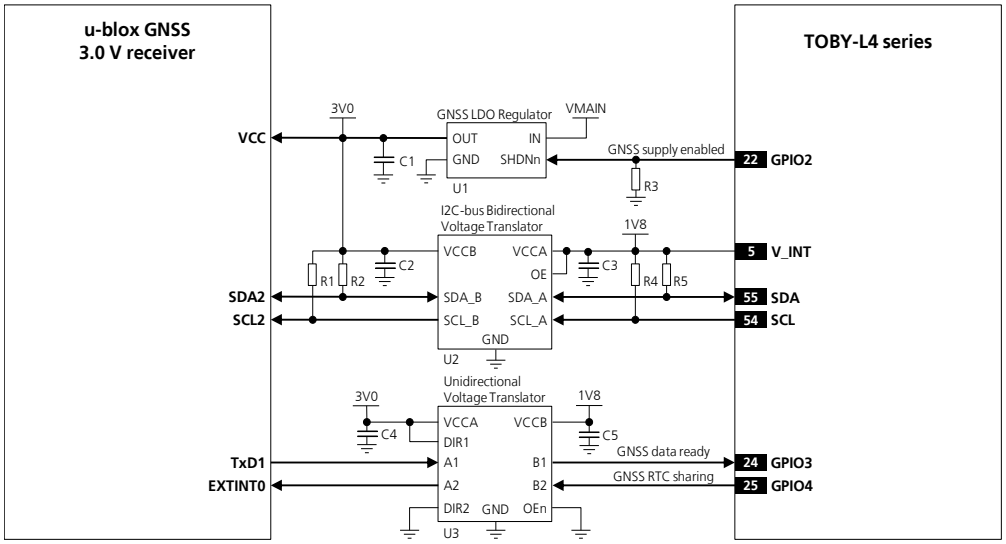

Figure 56: Application circuit for connecting TOBY-L4 series modules to u-blox 3.0 V GNSS receivers

Reference	Description	Part Number - Manufacturer
R1, R2, R4, R5	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3, C4, C5	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1, C1	Voltage Regulator for GNSS receiver and capacitor	See GNSS receiver Hardware Integration Manual
U2	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR - Texas Instruments
U3	Generic Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 41: Components for connecting TOBY-L4 series modules to u-blox 3.0 V GNSS receivers

☞ Custom functions over GPIO pins, to improve the integration with u-blox positioning chips and modules, will be supported by future firmware versions.

2.6.4.2 Guidelines for DDC (I²C) layout design

The DDC (I²C) serial interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.5 SDIO interface

☞ The SDIO interface is not supported by the "50" product version.

2.6.5.1 Guidelines for SDIO circuit design

TOBY-L4 series modules include a 4-bit Secure Digital Input Output interface (**SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD**), where the module acts as an SDIO host controller designed to

- communicate with compatible u-blox short range radio communication modules by means of the uCPU API
- communicate with external SDIO devices by means of the uCPU API

Connection with u-blox short range radio communication modules

Figure 58 and Table 43 show an application circuit for connecting TOBY-L4 series cellular modules to u-blox EMMY-W161 short range radio communication modules supporting IEEE 802.11a/b/g/n/ac data rates for Wi-Fi:

- The SDIO pins of the cellular module are connected to the related SDIO pins of the u-blox EMMY-W161 short range radio communication module, with appropriate low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

  The most appropriate value for the series damping resistors on the SDIO lines depends on the specific line lengths and layout implemented. In general, the SDIO series resistors are not strictly required, but it is recommended to slow the SDIO signal, for example with 22 Ω or 33 Ω resistors, and avoid any possible ringing problem without violating the rise / fall time requirements.
- The **V_INT** supply output pin of the cellular module is connected to the shutdown input pin (**SHDNn**) of the two LDO regulators providing the 3.3 V and 1.8 V supply rails for the u-blox EMMY-W161 module, with appropriate pull-down resistors to avoid an improper switch-on of the Wi-Fi module before the switch-on of the **V_INT** supply source of the cellular module SDIO interface pins.
- The **GPIO1** pin of the cellular module is connected to the active low full power down input pin (**PDn**) of the u-blox EMMY-W161 module, implementing the Wi-Fi enable function.
- The WLAN antenna RF input/output (**ANT1**) of the u-blox EMMY-W161 Wi-Fi module is directly connected to a Wi-Fi antenna considering that the u-blox EMMY-W161 module integrates a 2.4 GHz BAW band pass filter that enables co-existence with LTE RF signals.

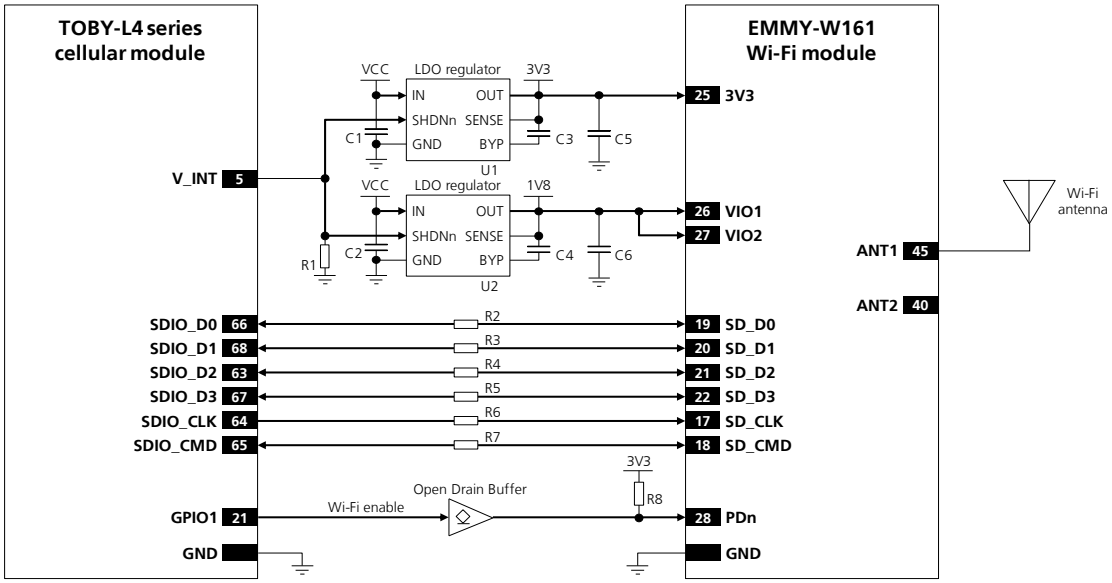

Figure 57: Application circuit for TOBY-L4 cellular module and u-blox EMMY-W161 short range radio communication module

Reference	Description	Part Number - Manufacturer
C1, C2	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C3, C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5, C6	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	470 kΩ Resistor 0402 5% 0.1 W	RK73B1ETTD474J - KOA
R2, R3, R4, R5, R6, R7	22 Ω Resistor 0402 5% 0.1 W	RK73B1ETTP220J - KOA
R8	47 kΩ Resistor 0402 5% 0.1 W	RK73B1ETTD473J - KOA
R9	47 kΩ Resistor 0402 5% 0.1 W	RK73B1ETTD473J - KOA
U1	LDO Linear Regulator 3.3 V 0.5 A	LT1963CS8-3.3 - Linear Technology
U2	LDO Linear Regulator 1.8 V 0.3 A	LT1962EMS8-1.8 - Linear Technology

Table 42: Components for connecting TOBY-L4 cellular modules and u-blox EMMY-W161 short range communication modules

Connection with external SDIO devices

Figure 58 and Table 43 show an application circuit example for connecting the SDIO interface of TOBY-L4 series modules to a 1.8 V SDIO device: the SDIO pins of the cellular module are connected to the related SDIO pins of the SDIO device, with appropriate low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

The most appropriate value for the series damping resistors on the SDIO lines depends on the specific line lengths and layout implemented. In general, the SDIO series resistors are not strictly required, but it is recommended to slow the SDIO signal, for example with 22 Ω or 33 Ω resistors, and avoid any possible ringing problem without violating the rise / fall time requirements.

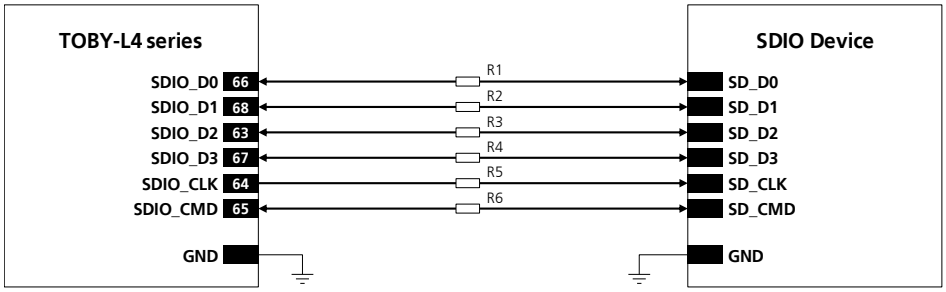

Figure 58: Application circuit for connecting TOBY-L4 series modules to a 1.8 V SDIO device

Reference	Description	Part Number - Manufacturer
R1, R2, R3, R4, R5, R6	22 Ω Resistor 0402 5% 0.1 W	RK73B1ETTP220J - KOA

Table 43: Components for connecting TOBY-L4 series modules to a 1.8 V SDIO device

The ESD sensitivity rating of SDIO interface pins is 1 kV (HMB according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and this can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD) close to the accessible points.

If the SDIO interface pins are not used, they can be left unconnected on the application board.

2.6.5.2 Guidelines for SDIO layout design

The SDIO serial interface requires the same considerations regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

2.6.6 RGMII interface

The RGMII interface is not supported by the "50" product version.

2.6.6.1 Guidelines for RGMII circuit design

TOBY-L4 series modules include an Ethernet Media Access Control (MAC) block supporting up to 1 Gbit/s data rate via a Reduced Gigabit Media-Independent Interface compliant with the RGMII Version 1.3 specification [7] and the RMII Revision 1.2 specification [8].

The module represents an Ethernet MAC controller, which can be connected to a compatible external Ethernet physical transceiver (PHY) chip to provide communication over Ethernet as illustrated in Figure 59.

Recommended compatible Ethernet PHY chips are:

- Marvell 88E1510
- Marvell 88E1512

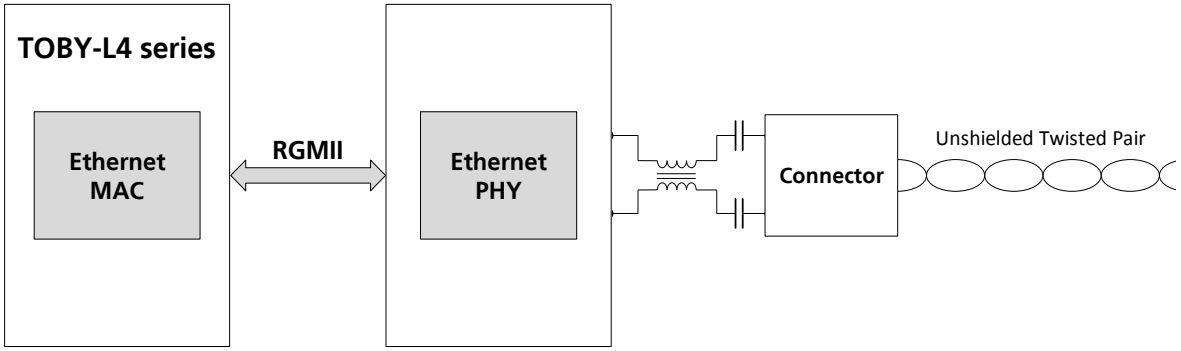

Figure 59: RGMII interface application circuit block diagram

The ESD sensitivity rating of RGMII interface pins is 1 kV (HMB according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD) close to the accessible points.

If the RGMII interface pins are not used, they can be left unconnected on the application board.

2.6.6.2 Guidelines for RGMII layout design

The RGMII / RMII interface requires the same considerations regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

2.7 eMMC interface

☞ The eMMC interface is not supported by the "50" product version.

2.7.1.1 Guidelines for eMMC circuit design

TOBY-L4 series modules include a 4-bit embedded Multi-Media Card interface compliant with JESD84-B451 Embedded Multimedia Card (eMMC) Electrical Standard 4.51 [9], which can be handled by means of the uCPU API.

The eMMC interface can be connected to an external eMMC / SD memory as defined by the standard.

Pull-up resistors can be added on **MMC_D0**, **MMC_D1**, **MMC_D2** and **MMC_D3** data lines, the **MMC_CLK** clock line and the **MMC_CMD** command line, to increase the rise time on the signals so as to compensate for any capacitance on the board, even if not strictly required.

☞ The ESD sensitivity rating of eMMC interface pins is 1 kV (HMB according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD) close to the accessible points.

☞ If the eMMC interface pins are not used, they can be left unconnected on the application board.

2.7.1.2 Guidelines for eMMC layout design

The eMMC interface requires the same considerations regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

2.8 Audio interface

2.8.1 Analog audio interface

2.8.1.1 Guidelines for analog audio uplink path circuit design

Guidelines for connecting two external microphones

Figure 60 and Table 44 show an application circuit connecting the uplink path of the analog audio interface of TOBY-L4 series modules to two electret microphones:

- One external 2.2 kΩ electret microphone is connected to the **MIC1_P** / **MIC1_N** analog audio uplink path
- One external 2.2 kΩ electret microphone is connected to the **MIC2_P** / **MIC2_N** analog audio uplink path

The first differential analog audio input (**MIC1_P**, **MIC1_N**) and the second differential analog audio input (**MIC2_P**, **MIC2_N**) interfaces can be used alternatively, in mutually exclusive way. For example, one can be used for voice call purposes, the other can be used for eCall purposes.

As in the example circuit in Figure 60 and Table 44, the following general guidelines are recommended for the design of an analog audio circuit connecting two external electret microphones:

- Provide a correct supply to the used electret microphones, as for example providing a clean connection from the **MIC_BIAS** supply output to the microphones. It is suggested to implement a bridge structure:
  - The microphones, with their nominal intrinsic resistance value, represent one resistor of the bridge.
  - To achieve good supply noise rejection, the ratio of the two resistances in one leg (e.g. R2 / R3 resistors in Figure 60) should be equal to the ratio of the two resistances in the other leg (e.g. R4 / MIC1), meaning that R2 must be equal to R4 (e.g. 2.2 kΩ) and R3 must be equal to the microphone nominal intrinsic resistance value (e.g. 2.2 kΩ for MIC1).
- Using the **MIC_BIAS** supply output of the module, provide a suitable series resistor at the **MIC_BIAS** supply output and then mount a suitable large bypass capacitor to provide additional supply noise filtering. See the R1 and R5 series resistors (1.5 kΩ) and the C1 and C5 bypass capacitors (10 µF).
- Do not place a bypass capacitor directly at the **MIC_BIAS** supply output, since a suitable internal bypass capacitor is already provided to guarantee stable operation of the internal regulator.
- Connect the reference of the microphone circuit to the **MIC_GND** pin of the module as a sense line.
- Provide a suitable series capacitor at both **MIC1_P** / **MIC1_N** and **MIC2_P** / **MIC2_N** analog uplink inputs for DC blocking (as the C2 / C3 and C7 / C8 100 nF Murata GRM155R71C104K capacitors in Figure 60). This provides a high-pass filter for the microphone DC bias with the correct cut-off frequency according to the value of the resistors of the microphone supply circuit. Then connect the signal lines to the microphone.
- Provide the correct parts on each line connected to the external microphone as noise and EMI improvements, to minimize RF coupling and TDMA noise, according to the custom application requirements.
  - Mount an 82 nH series inductor with a Self Resonance Frequency ~1 GHz (e.g. the Murata LQG15HS82NJ02) on each microphone line (L1 / L2 and L3 / L4 inductors in Figure 60).
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each microphone line to the solid ground plane (C4 / C5 and C9 / C10 capacitors in Figure 60).
- Use microphones designed for GSM applications, which typically have internal built-in bypass capacitor(s) with Self-Resonant Frequency in the cellular frequency range(s).
- Provide additional ESD protection (e.g. Bourns CG0402MLE-18G varistor) if the analog audio lines will be externally accessible on the application device, according to the EMC/ESD requirements of the custom application. Mount the protection close to an accessible point of the line (D1 / D2 and D3 / D4 in Figure 60).

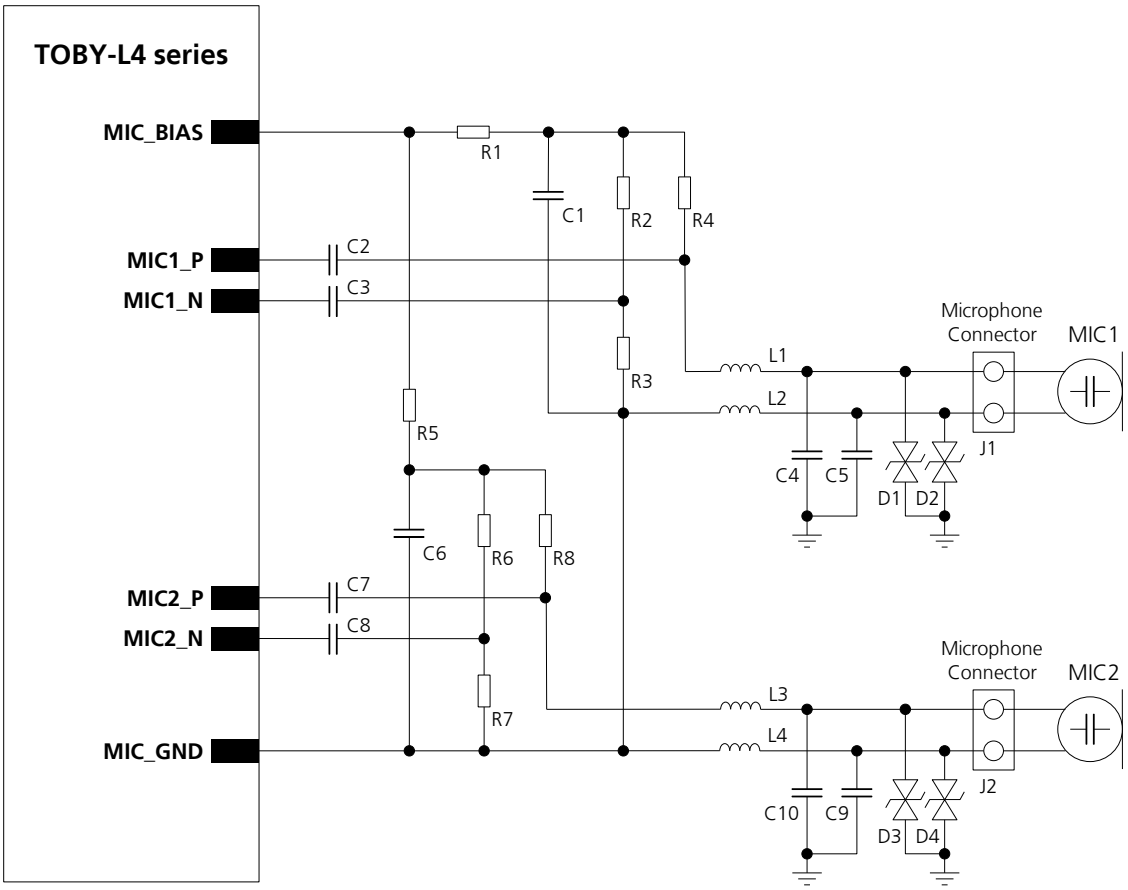

Figure 60: Application circuit connecting the analog audio interface to two external electret microphones

Reference	Description	Part Number – Manufacturer
C1, C6	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C2, C3, C7, C8	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA88 – Murata
C4, C5, C9, C10	27 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H270JA01 – Murata
D1, D2, D3, D4	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
J1, J2	Microphone Connector	Various Manufacturers
L1, L2, L3, L4	82 nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
MIC1, MIC2	2.2 kΩ Electret Microphone	Various Manufacturers
R1, R5	1.5 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K5L – Yageo Phycomp
R2, R3, R4, R6, R7, R8	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp

Table 44: Example of components for connecting the analog audio interface to two electret microphones

Guidelines for connecting one external microphone

Figure 61 and Table 45 show an application circuit connecting the uplink path of the analog audio interface of TOBY-L4 series modules to one electret microphone:

- One external 2.2 kΩ electret microphone is connected to an analog audio uplink path of the module

The same circuit can be implemented for the **MIC1_P** / **MIC1_N** and **MIC2_P** / **MIC2_N** differential analog audio inputs of the module.

As in the example circuit in Figure 61 and Table 45, the following general guidelines are recommended for the design of an analog audio circuit connecting an external electret microphone:

- Provide a correct supply to the used electret microphone, as for example providing a clean connection from the **MIC_BIAS** supply output to the microphone. It is suggested to implement a bridge structure:
  - The electret microphone, with its nominal intrinsic resistance value, represents one resistor of the bridge.
  - To achieve good supply noise rejection, the ratio of the two resistances in one leg (R2 / R3) should be equal to the ratio of the two resistances in the other leg (R4 / MIC), i.e. R2 must be equal to R4 (e.g. 2.2 kΩ) and R3 must be equal to the microphone nominal intrinsic resistance value (e.g. 2.2 kΩ).
- Using the **MIC_BIAS** supply output of the module, provide a suitable series resistor at the **MIC_BIAS** supply output and then mount a suitable large bypass capacitor to provide additional supply noise filtering. See the R1 series resistor (2.2 kΩ) and the C1 bypass capacitor (10 µF).
- Do not place a bypass capacitor directly at the **MIC_BIAS** supply output, since a suitable internal bypass capacitor is already provided to guarantee stable operation of the internal regulator.
- Connect the reference of the microphone circuit to the **MIC_GND** pin of the module as a sense line.
- Provide a suitable series capacitor at both **MIC1_P** / **MIC1_N** and/or **MIC2_P** / **MIC2_N** analog uplink inputs for DC blocking (as the C2 and C3 Murata GRM155R71C104K 100 nF capacitors in Figure 61). This provides a high-pass filter for the microphone DC bias with the correct cut-off frequency according to the value of the resistors of the microphone supply circuit. Then connect the signal lines to the microphone.
- Provide the correct parts on each line connected to the external microphone as noise and EMI improvements, to minimize RF coupling and TDMA noise, according to the custom application requirements.
  - Mount an 82 nH series inductor with a Self Resonance Frequency ~1 GHz (e.g. the Murata LQG15HS82NJ02) on each microphone line (L1 and L2 inductors in Figure 61).
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each microphone line to the solid ground plane (C4 and C5 capacitors in Figure 61).
- Use a microphone designed for GSM applications, which typically has internal built-in bypass capacitor(s) with Self-Resonant Frequency in the cellular frequency range(s).
- Provide additional ESD protection (e.g. Bourns CG0402MLE-18G varistor) if the analog audio lines will be externally accessible on the application device, according to the EMC/ESD requirements of the custom application. Mount the protection close to an accessible point of the line (D1-D2 in Figure 61).

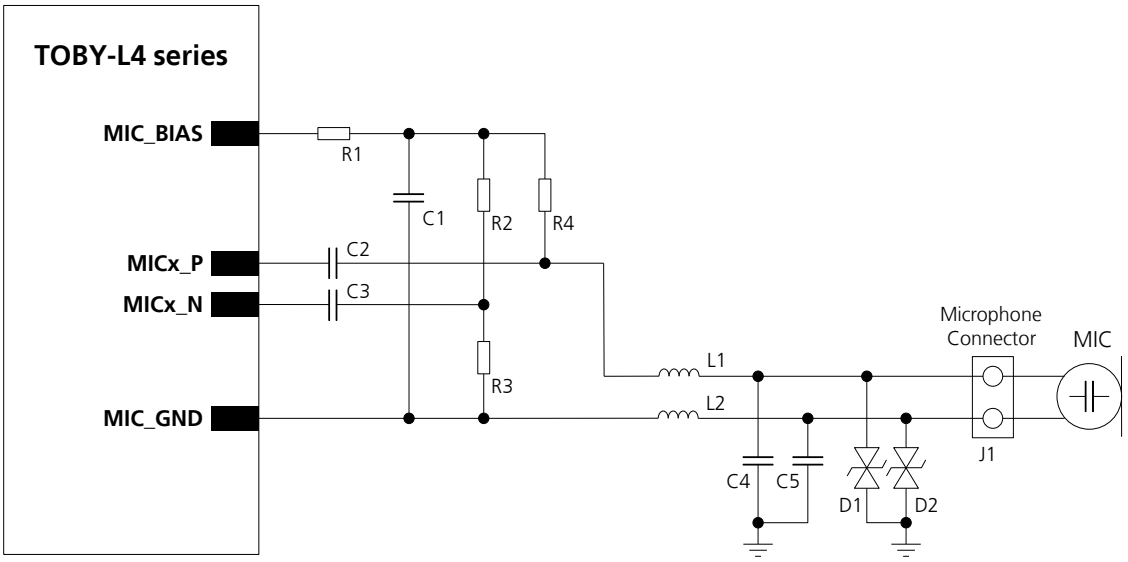

Figure 61: Application circuit connecting the analog audio interface to one external electret microphone

Reference	Description	Part Number – Manufacturer
C1	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C2, C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA88 – Murata
C4, C5	27 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H270JA01 – Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
J1	Microphone Connector	Various Manufacturers
L1, L2	82 nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
MIC	2.2 kΩ Electret Microphone	Various Manufacturers
R1, R2, R3, R4	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp

Table 45: Example of components for connecting the analog audio interface to one external electret microphone

Guidelines for connecting one external analog audio device output

Figure 62 and Table 46 describe application circuits connecting the uplink path of the analog audio interface of TOBY-L4 series modules to analog audio output of generic external analog audio devices:

- One differential analog audio output is connected to an analog audio uplink path of the module
- One single-ended analog audio output is connected to an analog audio uplink path of the module

The same circuits can be implemented for the **MIC1_P** / **MIC1_N** and **MIC2_P** / **MIC2_N** differential analog audio inputs of the module.

Guidelines for the connection to a differential analog audio output:

- The **MIC1_P** / **MIC1_N** and/or **MIC2_P** / **MIC2_N** balanced input of the module must be connected to the differential output of the external audio device by means of series capacitors for DC blocking (e.g. 10 µF) to decouple the bias present at the module input, as illustrated in the Figure 62 left side.

Guidelines for the connection to a single-ended analog audio output:

- A suitable single-ended to differential circuit must be inserted from the single-ended output of the external audio device to the **MIC1_P** / **MIC1_N** and/or **MIC2_P** / **MIC2_N** balanced input of the module, as illustrated in the Figure 62 right side: 10 µF series capacitors are provided to decouple the bias present at the module input, and a voltage divider is provided to adapt the signal level from the external device to the module.

Additional guidelines for any connection:

- Audio devices with differential analog I/O are preferable, as they are more immune to external disturbances.
- The DC-block series capacitor acts as a high-pass filter for audio signals, with a cut-off frequency depending on both the values of the capacitor and on the input impedance of the device. For example: for differential input impedance of 600 Ω , the two 10 µF capacitors will set the -3 dB cut-off frequency to 53 Hz, while for a single-ended connection to a 600 Ω external device, the cut-off frequency with just the single 10 µF capacitor will be 103 Hz. In both cases, the high-pass filter has a low enough cut-off for the correct frequency response.
- Use a suitable power-on sequence to avoid audio bump due to charging of the capacitor: the final audio stage should be always enabled as the last one.
- The signal levels can be adapted by setting the internal gains, but additional circuitry must be inserted if the audio device output level is too high for **MIC1_P** / **MIC1_N** and/or **MIC2_P** / **MIC2_N**, as the voltage dividers present in the circuits illustrated in Figure 62 right side to properly adapt the signal level.

Figure 62: Application circuits to connect the module to audio devices with suitable differential or single-ended output

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	10 µF Capacitor X5R 0603 5% 6.3 V	GRM188R60J106M – Murata
R1	0 Ω Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
R2	Not populated	

Table 46: Example of components for connecting audio devices with suitable analog differential or single-ended output

2.8.1.2 Guidelines for analog audio downlink path circuit design

Guidelines for connecting an external low-power receiver / speaker

Figure 63 and Table 47 show an application circuit connecting the downlink path of the analog audio interface of TOBY-L4 series modules to a low-power receiver / speaker:

- A 16 Ω receiver / speaker is connected to the analog audio downlink path of the module

As in the example circuit in Figure 63 and Table 47, the following general guidelines are recommended for the design of an analog audio circuit connecting a low-power receiver / speaker:

- Connect the **SPK_P** and **SPK_N** analog downlink outputs directly to the receiver / speaker (which resistance rating must be greater than 14 Ω).
- Provide suitable parts on each line connected to the receiver / speaker as noise and EMI improvements, to minimize RF coupling, according to EMC requirements of the custom application.
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each speaker line to the solid ground plane (C1 and C2 capacitors in Figure 63).
- Provide additional ESD protection (e.g. Bourns CG0402MLE-18G varistor) if the analog audio lines will be externally accessible on the application device, according to the EMC/ESD requirements of the custom application. Mount the protection close to an accessible point of the line (D1 and D2 in Figure 63).

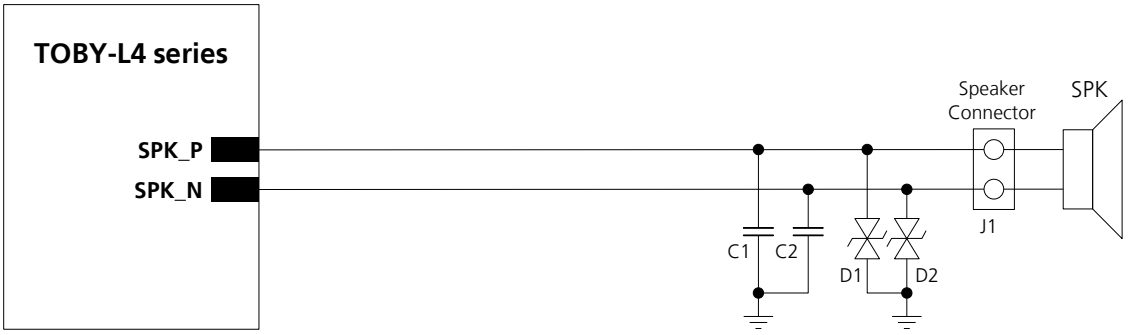

Figure 63: Application circuit connecting the analog audio interface to a low-power speaker

Reference	Description	Part Number – Manufacturer
C1, C2	27 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H270JA01 – Murata
D1, D2,	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
J1	Speaker Connector	Various Manufacturers
SPK	16 Ω Speaker	Various Manufacturers

Table 47: Example of components for connecting the analog audio interface to a low-power speaker

Guidelines for connecting an external high-power loudspeaker

Figure 64 and Table 48 show an application circuit connecting the downlink path of the analog audio interface of TOBY-L4 series modules to a high-power loudspeaker:

- An external 8 Ω or 4 Ω loudspeaker is connected to the analog audio downlink path of the module through an external audio amplifier, which must be provided on the application board to amplify the low power audio signal provided by the downlink path of the module.

As in the example circuit in Figure 64 and Table 48, the following general guidelines are recommended for the design of an analog audio circuit connecting a high-power loudspeaker:

- Provide a DC blocking series capacitor at both **SPK_P** and **SPK_N** analog downlink outputs (C1 and C2 Murata GRM155R71C473K 47 nF capacitors in Figure 64). Then connect the lines to the differential input of a suitable external audio amplifier, the differential output of which must be connected to the 8 Ω or 4 Ω loudspeaker. (See the Analog Devices SSM2305CPZ filter-less mono 2.8 W class-D Audio Amplifier in the circuit illustrated in Figure 64.)
- Provide suitable parts on each line connected to the external loudspeaker as noise and EMI improvements, to minimize RF coupling, according to the EMC requirements of the custom application.
  - Mount a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each loudspeaker line to the solid ground plane (C3 and C4 capacitors in Figure 64).
- Provide additional ESD protection (e.g. Bourns CG0402MLE-18G varistor) if the analog audio lines will be externally accessible on the application device, according to the EMC/ESD requirements of the custom application. The protection should be mounted close to an accessible point of the line (D1 and D2 parts in the circuit illustrated in Figure 64).

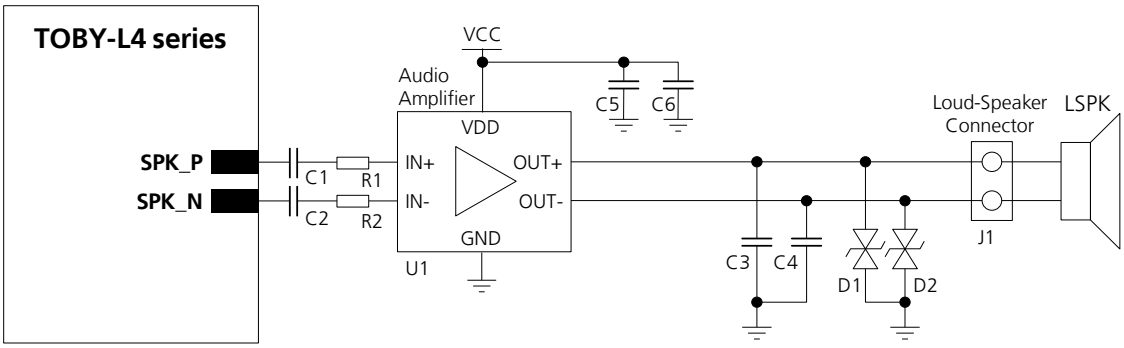

Figure 64: Application circuit connecting the analog audio interface to a high-power loudspeaker

Reference	Description	Part Number – Manufacturer
C1, C2	47 nF Capacitor Ceramic X7R 0402 10% 16V	GRM155R71C473KA01 – Murata
C3, C4	27 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H270JA01 – Murata
C5	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C6	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA88 – Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
J1	Speaker Connector	Various Manufacturers
LSPK	8 Ω Loud-Speaker	Various Manufacturers
MIC	2.2 kΩ Electret Microphone	Various Manufacturers
R1, R2	0 Ω Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
U1	Filter-less Mono 2.8 W Class-D Audio Amplifier	SSM2305CPZ – Analog Devices

Table 48: Example of components for connecting the analog audio interface to a high-power loudspeaker

Guidelines for connecting one external analog audio device input

Figure 65 and Table 49 describe application circuits connecting the downlink path of the analog audio interface of TOBY-L4 series modules to analog audio input of generic external analog audio devices:

- One differential analog audio input is connected to an analog audio downlink path of the module
- One single-ended analog audio input is connected to an analog audio downlink path of the module

Guidelines for the connection to a differential analog audio input:

- The **SPK_P** / **SPK_N** balanced output of the module must be connected to the differential input of the external audio device by means of series capacitors for DC blocking (e.g. 10 µF) to decouple the bias present at the module output, as illustrated in the left side of Figure 65.

Guidelines for the connection to a single-ended analog audio input:

- A suitable differential to single-ended circuit must be inserted from the **SPK_P** / **SPK_N** balanced output of the module to the single-ended input of the external audio device, as illustrated in the Figure 65 right side: 10 µF series capacitors are provided to decouple the bias present at the module output, and a voltage divider is provided to properly adapt the signal level from module output to external audio device input.

Additional guidelines for any connection:

- Audio devices with differential analog I/O are preferable, as they are more immune to external disturbances.
- The DC-block series capacitor acts as a high-pass filter for audio signals, with a cut-off frequency depending on both the values of capacitor and on the input impedance of the device. For example: for differential input impedance of 600 Ω , the two 10 µF capacitors will set the -3 dB cut-off frequency to 53 Hz, while for single-ended connection to a 600 Ω external device, the cut-off frequency with just the single 10 µF capacitor will be 103 Hz. In both cases. the high-pass filter has a low enough cut-off for the correct frequency response.
- Use a suitable power-on sequence to avoid audio bump due to charging of the capacitor: the final audio stage should be always enabled as the last one.
- The signal levels can be adapted by setting the internal gains, but additional circuitry must be inserted if **SPK_P** / **SPK_N** output level of the module is too high for the audio device input, as the voltage dividers present in the circuits illustrated in Figure 65 right side to properly adapt the signal level.

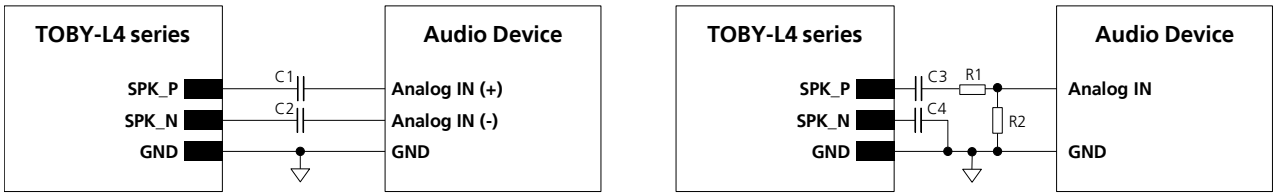

Figure 65: Application circuits to connect the module to audio devices with suitable differential or single-ended input

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	10 µF Capacitor X5R 0603 5% 6.3 V	GRM188R60J106M – Murata
R1	0 Ω Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
R2	Not populated	

Table 49: Example of components for connecting audio devices with suitable analog differential or single-ended input

2.8.1.3 Guidelines for analog audio layout design

Accurate design of the analog audio circuit is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 217 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise from audio lines due to both **VCC** burst noise coupling and RF detection.

General guidelines for the uplink path (microphone), which is commonly the most sensitive, are the following:

- Avoid coupling of any noisy signal to microphone lines: it is strongly recommended to route microphone lines away from the module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between the microphone and speaker / receiver lines.
- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of microphone and speaker parts in order to avoid echo interference between the uplink path and downlink path.
- Keep ground separation from microphone lines to other noisy signals. Use an intermediate ground layer or vias wall for coplanar signals.
- For an external audio device providing differential microphone input, route the microphone signal lines as a differential pair embedded in ground to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF very close to the active microphone. The preferred microphone should be designed for GSM applications which typically have an internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device.

General guidelines for the downlink path (speaker / receiver) are the following:

- The physical width of the audio output lines on the application board must be wide enough to minimize series resistance since the lines are connected to low impedance speaker transducers.
- Avoid coupling of any noisy signal to speaker lines: it is recommended to route speaker lines away from the module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between speaker / receiver and microphone lines.
- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of speaker and microphone parts in order to avoid echo interference between the downlink path and uplink path.
- For external audio device providing differential speaker / receiver output, route the speaker signal lines as a differential pair embedded in ground up to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place the RF bypass capacitor close to the speaker.

☞ The ESD sensitivity rating of analog audio interface pins is 1 kV (HBM, according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the analog audio pins functionality is not used, they can be left unconnected on the application board.

2.8.2 Digital audio interface

☞ The second digital audio interface (I2S1) will be supported by future firmware versions.

2.8.2.1 Guidelines for digital audio circuit design

The I²S digital audio interfaces can be connected to an external digital audio device for voice applications.

Any external digital audio device compliant with the configuration of the digital audio interface of the TOBY-L4 series cellular module can be used, given that the external digital audio device must provide:

- The opposite role: slave or master role, as TOBY-L4 series modules may act as master or slave
- The same mode and frame format: PCM / short synch mode or Normal I²S / long synch mode with
  - data in 2's complement notation, linear
  - MSB transmitted first
  - data word length = 16-bit (16 clock cycles)
  - frame length = synch signal period:
    - 17-bit or 18-bit in PCM / short alignment mode (16 + 1 or 16 + 2 clock cycles, with the Word Alignment / Synchronization signal set high for 1 clock cycle or 2 clock cycles)
    - 32-bit in Normal I²S mode / long alignment mode (16 x 2 clock cycles)
- The same sample rate, i.e. synch signal frequency, <I2S_sample_rate> parameter:
  - 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- The same serial clock frequency:
  - 17 x <I2S_sample_rate> or 18 x <I2S_sample_rate> in PCM / short alignment mode, or
  - 16 x 2 x <I2S_sample_rate> in Normal I²S mode / long alignment mode
- Compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V digital audio interface of the module to the external 3.0 V (or similar) digital audio device by means of appropriate unidirectional voltage translators (e.g. TI SN74AVC4T774 or SN74AVC2T245, providing a partial power down feature so that the digital audio device 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply), using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side.

An appropriate specific application circuit must be implemented and configured according to the particular external digital audio device or audio codec used and according to the application requirements.

Examples of manufacturers offering compatible audio codec parts are the following:

- Maxim Integrated (as the MAX9860, MAX9867, MAX9880A audio codecs)
- Texas Instruments / National Semiconductor
- Cirrus Logic / Wolfson Microelectronics
- Nuvoton Technology
- Asahi Kasei Microdevices
- Realtek Semiconductor

Figure 66 and Table 50 describe application circuits for the digital audio interfaces, considering these scenarios:

- 1.8 V digital audio device with slave role connected to a digital audio interface of the module set as master
- 1.8 V digital audio device with master role connected to a digital audio interface of the module set as slave
- 3.0 V digital audio device with slave role connected to a digital audio interface of the module set as master
- 3.0 V digital audio device with master role connected to a digital audio interface of the module set as slave

The same circuits can be implemented for both the I2S0 and the I2S1 digital audio interfaces of the module.

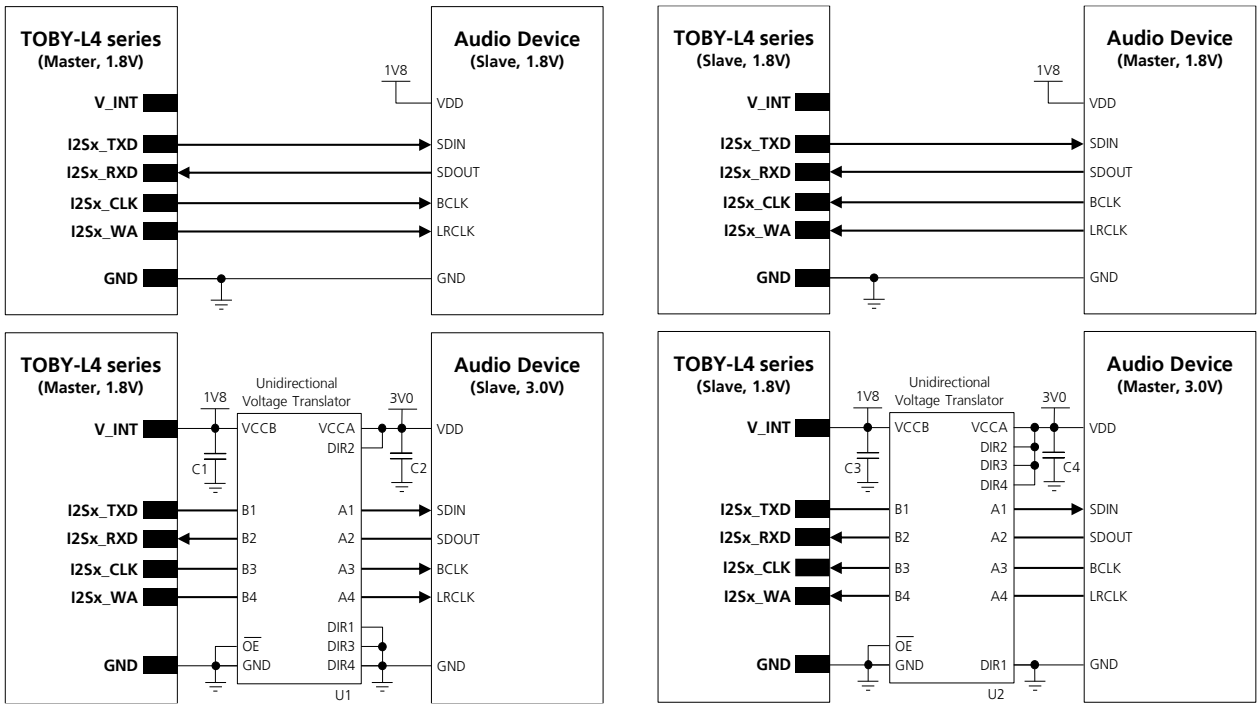

Figure 66: I²S interface application circuit with an external audio codec to provide voice capability

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774[20] - Texas Instruments

Table 50: Example of components for an audio voice codec application circuit

Do not apply voltage to any I²S pin before the switch-on of the I²S supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.

The ESD sensitivity rating of the I²S interface pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

If the I²S digital audio pins are not used, they can be left unconnected on the application board.

2.8.2.2 Guidelines for digital audio layout design

I²S interface and clock output lines require the same considerations regarding electromagnetic interference as any other high speed digital interface. Keep the traces short and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

[20] Voltage translator providing partial power down feature so that the external 3 V supply can be also ramped up before **V_INT** 1.8 V supply

2.9 ADC interfaces

☞ The ADC pins are not supported by the "50" product version.

2.9.1.1 Guidelines for ADC circuit design

TOBY-L4 series modules include Analog to Digital Converter inputs (**ADC1**, **ADC2**), which can be handled by means of the dedicated uCPU API.

The ADC pins can be connected to external circuits for general purpose voltage measurements.

The voltage value at the ADC input must be within the range reported in the TOBY-L4 series Data Sheet [1].

If an external voltage divider is implemented to increase the measurement voltage range, check the input resistance of the ADC inputs reported in the TOBY-L4 series Data Sheet [1]: if the Thévenin's equivalent of the external circuit has a significant value as compared to the input resistance of the ADC inputs, this should be taken into account and corrected to properly associate the ADC response to the voltage source value, implementing an appropriate ADC calibration procedure.

☞ The ESD sensitivity rating of ADC interface pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the ADC pins are not used, they can be left unconnected on the application board.

2.9.1.2 Guidelines for ADC layout design

The Analog to Digital Converters (**ADC1**, **ADC2**) are high impedance analog inputs. The conversion accuracy will be degraded if noise is injected. Low-pass filter may be used to improve noise rejection; typically L-C tuned for RF rejection gives better results.

2.10 General Purpose Input/Output

2.10.1.1 Guidelines for GPIO circuit design

A typical usage of TOBY-L4 series modules' GPIOs can be the following:

- Wi-Fi enable function provided by **GPIO1** (see Figure 58 in section 2.6.5)[21]
- GNSS supply enable function provided by **GPIO2** (see Figure 54, Figure 56 in section 2.6.4)[21]
- GNSS Tx data ready function provided by **GPIO3** (see Figure 54, Figure 56 in section 2.6.4)[21]
- GNSS RTC sharing function provided by **GPIO4** (see Figure 54, Figure 56 in section 2.6.4)[21]
- SIM card detection provided by the **GPIO5** (see Figure 39 / Table 30 in section 2.5)

Other configurations of the TOBY-L4 series modules' GPIOs are possible, as illustrated in section 1.13.

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series with the GPIO of TOBY-L4 series modules.

☞ Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a clean module boot. If the external signals connected to the module cannot be tri-stated or set low, insert a multi-channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

☞ The ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

2.10.1.2 Guidelines for general purpose input/output layout design

The general purpose inputs / outputs pins are generally not critical for layout.

[21] Not supported by "50" product version

2.11 Reserved pins (RSVD)

TOBY-L4 series modules have pins reserved for future use, marked as **RSVD**. All the **RSVD** pins are to be left unconnected on the application board except the following **RSVD** pins as illustrated in Figure 67:

- the **RSVD** pin number **6** that must be externally connected to ground

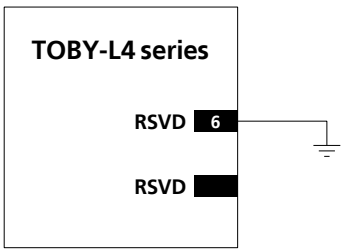

Figure 67: Application circuit for the reserved pins (RSVD)

2.12 Module placement

An optimized placement allows a minimum RF line's length and a closer path from the DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce electromagnetic interference that affects the module, analog parts and RF circuits' performance. Implement suitable countermeasures to avoid any possible electromagnetic compatibility issues.

Make sure that the module, RF and analog parts / circuits, and high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by electromagnetic interference, or employ countermeasures to avoid any possible electromagnetic compatibility issue.

Provide enough clearance between the module and any external part.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the TOBY-L4 series modules: avoid placing temperature sensitive devices close to the module.

2.13 Module footprint and paste mask

Figure 68 and Table 51 describe the suggested footprint (i.e. copper mask) and the paste mask (i.e. stencil) layout for TOBY-L4 series modules, to be implemented on the application PCB.

The proposed land pattern layout (i.e. the footprint, the application board top-layer copper mask) reflects the modules' pads layout, with the pads on the application board designed as the LGA pads of the module.

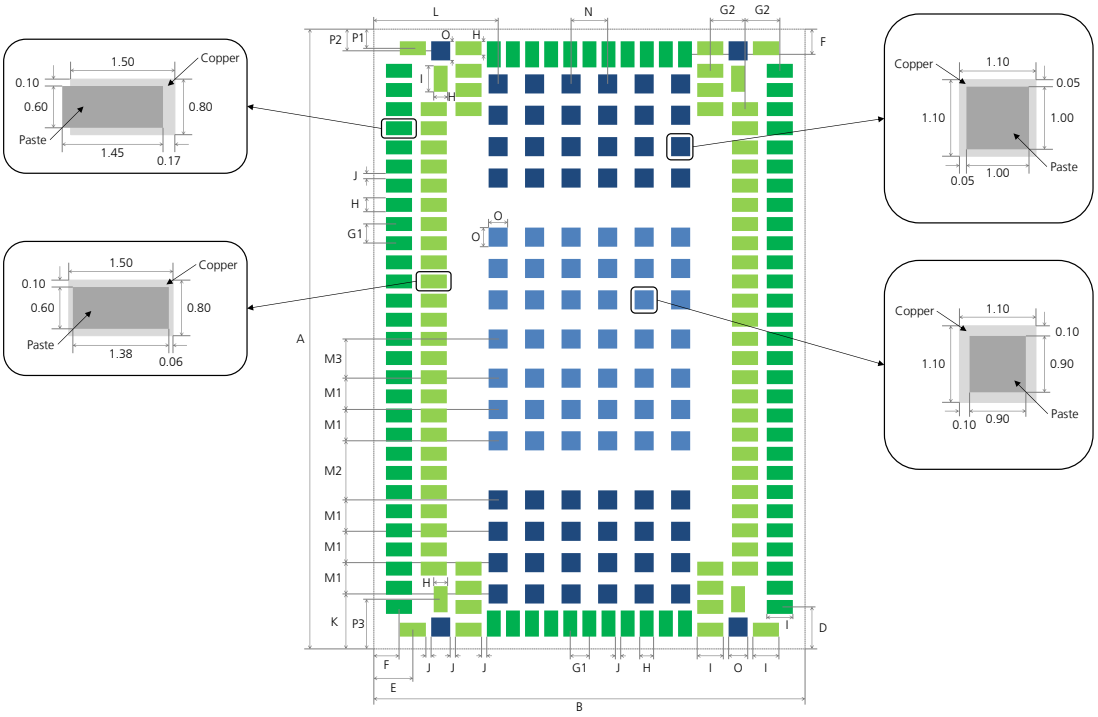

Figure 68: Suggested footprint and stencil design for TOBY-L4 series modules, to be implemented on application PCB (top view)

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
A	35.6 mm	G1	1.10 mm	K	3.15 mm	N	2.10 mm
B	24.8 mm	G2	2.00 mm	L	7.15 mm	O	1.10 mm
D	2.40 mm	H	0.80 mm	M1	1.80 mm	P1	1.10 mm
E	2.25 mm	I	1.50 mm	M2	3.40 mm	P2	1.25 mm
F	1.45 mm	J	0.30 mm	M3	2.25 mm	P3	2.85 mm

Table 51: Suggested footprint design dimensions for TOBY-L4 series modules, to be implemented on application PCB

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, implementing the solder mask opening 50 µm larger per side than the corresponding copper pad.

The suggested paste mask (i.e. stencil) layout to mount TOBY-L4 series modules on the application PCB is also illustrated in Figure 68. Different stencil apertures layout for any specific pad is recommended:

- Green marked pads: Paste layout enlarged on the lateral side and reduced on other sides (see Figure 68)
- Light-Green marked pads: Paste layout reduced circumferentially to Copper layout (see Figure 68)
- Blue marked pads: Paste layout reduced circumferentially 0.05 mm to Copper layout (see Figure 68)
- Light-Blue marked pads: Paste layout reduced circumferentially 0.1 mm to Copper layout (see Figure 68)

The recommended solder paste thickness is 150 µm, according to application production process requirements.

☞ These are recommendations only and not specifications. The exact mask geometries, distances and stencil thicknesses must be adapted to the specific production processes (e.g. soldering) of the customer.

2.14 Thermal guidelines

☞ Modules' temperature range and thermal parameters are specified in the TOBY-L4 series Data Sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected mode), because when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution for WCDMA, taken from operation on a live network, described in the GSMA TS.09 Battery Life Measurement and Current Consumption Technique [10]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power, the TOBY-L4 series modules generate thermal power that may exceed 4 W in the worst case condition: this is an indicative value since the exact generated power strictly depends on operating conditions such as the actual antenna return loss, the number of allocated TX resource blocks, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the actual Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

☞ The actual Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the actual Module-to-Ambient thermal resistance, will decrease the temperature of the modules' internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with a complete thermal via stacked down to the main ground layer.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application device.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Further hardware techniques that may be considered to improve the heat dissipation in the application:

- Provide a heat sink component on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads of the TOBY-L4 series LGA modules and dissipated over the backside of the application board.
- Force ventilation air-flow within the mechanical enclosure.

Beside the reduction of the Module-to-Ambient thermal resistance implemented with the correct application hardware design, the increase of module temperature can be moderated by suitable application software implementation:

- Enable power saving configuration by means of the AT+UPSV command or the uCPU API.
- Enable module connected mode for a given time period and then disable it for a time period long enough to properly mitigate temperature increase.

2.15 Design-in checklist

This section provides a design-in checklist.

2.15.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at the **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting both the highest peak and the highest averaged current consumption values in connected mode, as specified in the TOBY-L4 series Data Sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for the maximum available current from **V_INT** supply.
- ☑ Check that the voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the following pins of the TOBY-L4 series modules: **V_INT**, **PWR_ON** and **RESET_N** for diagnostic purposes.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, as the modules' signal names follow the ITU-T V.24 Recommendation [5].
- ☑ Provide accessible test points directly connected to all the UART pins of the TOBY-L4 series modules (**TXD**, **RXD**) for diagnostic purposes.
- ☑ Provide accessible test points directly connected to all the UART3 pins of the TOBY-L4 series modules (**TXD3**, **RXD3**) for Linux console access.
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ Provide accessible test points directly connected to the USB 2.0 interface pins of the TOBY-L4 series modules (**VUSB_DET**, **USB_D+** and **USB_D–**) for diagnostic and FW update purposes.
- ☑ Consider providing appropriate low value series damping resistors on SDIO lines to avoid reflections.
- ☑ Add a suitable pull-up resistor (e.g. 4.7 kΩ) to **V_INT** or another suitable 1.8 V supply on each DDC (I^2C) interface line, if the interface is used.
- ☑ Check the digital audio interface specifications to connect a suitable external audio device.
- ☑ Capacitance and series resistance must be limited on master clock output line and each I^2S interface line
- ☑ Consider passive filtering parts on each used analog audio line.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide suitable precautions for EMC / ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of TOBY-L4 series modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins can be left unconnected except the **RSVD** pin number **6** of TOBY-L4 series modules, which must be connected to GND.

2.15.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT1** and the **ANT2** ports (antenna RF interfaces).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (primarily analog audio input/output signals, SIM signals, high-speed digital lines such as the USB, SDIO, RGMII, eMMC, SPI and other data lines).
- ☑ Optimize placement for minimum length of the RF line.
- ☑ Check the footprint and paste mask designed for TOBY-L4 series modules as illustrated in section 2.13.
- ☑ **VCC** line should be as wide and as short as possible.
- ☑ Route **VCC** supply line away from RF lines / parts and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with the application board solid ground layer.
- ☑ Use as many vias as possible to connect the ground planes on a multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along the RF and high speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ USB 2.0 and USB 3.0 data line traces must meet characteristic impedance requirements as per USB 2.0 specification [3] and USB 3.0 specification [4], and should not be routed close to any RF line / part.
- ☑ Keep the SDIO traces short, avoid stubs, avoid coupling with any RF line / part and consider low value series damping resistors to avoid reflections and other losses in signal integrity.
- ☑ Ensure appropriate RF precautions for the Wi-Fi and Cellular technologies coexistence .
- ☑ Ensure appropriate RF precautions for the GNSS and Cellular technologies coexistence.
- ☑ Route analog audio signals away from noisy sources (primarily RF interface, **VCC**, switching supplies).
- ☑ The audio outputs lines on the application board must be wide enough to minimize series resistance.

2.15.3 Antenna checklist

- ☑ Antenna termination should provide a 50 Ω characteristic impedance with VSWR at least less than 3:1 (recommended 2:1) on operating bands in the deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement.
- ☑ Ensure high and similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antennas.
- ☑ Ensure high isolation between the primary (**ANT1**) and the secondary (**ANT2**) antennas.
- ☑ Ensure a low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antennas: the 3D antenna radiation patterns should have radiation lobes in different directions.
- ☑ Ensure high isolation between the cellular antennas and any other antenna or transmitter.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information about the TOBY-L4 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the TOBY-L4 series Data Sheet [1] and the u-blox Package Information Guide [16].

3.2 Handling

The TOBY-L4 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ **Ensure ESD precautions are implemented during handling of the module.**

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of TOBY-L4 series modules (as Human Body Model according to JESD22-A114F) is specified in the TOBY-L4 series Data Sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the TOBY-L4 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,…).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such an exposed antenna area is touched in a non-ESD protected work area, implement suitable ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

"No Clean" soldering paste is strongly recommended for TOBY-L4 series modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	+217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.13.

☞ The quality of the solder joints on the connectors ("half vias") should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended for TOBY-L4 series modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Refer to the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes" guide, published in 2001.

Reflow profiles are to be selected according to the following recommendations.

⚠ **Failure to observe these recommendations can result in severe damage to the device!**

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s — If the temperature rise is too rapid in the preheat phase, it may cause excessive slumping.
- Time: 60 – 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 °C - 200 °C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 - 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors, such as the choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

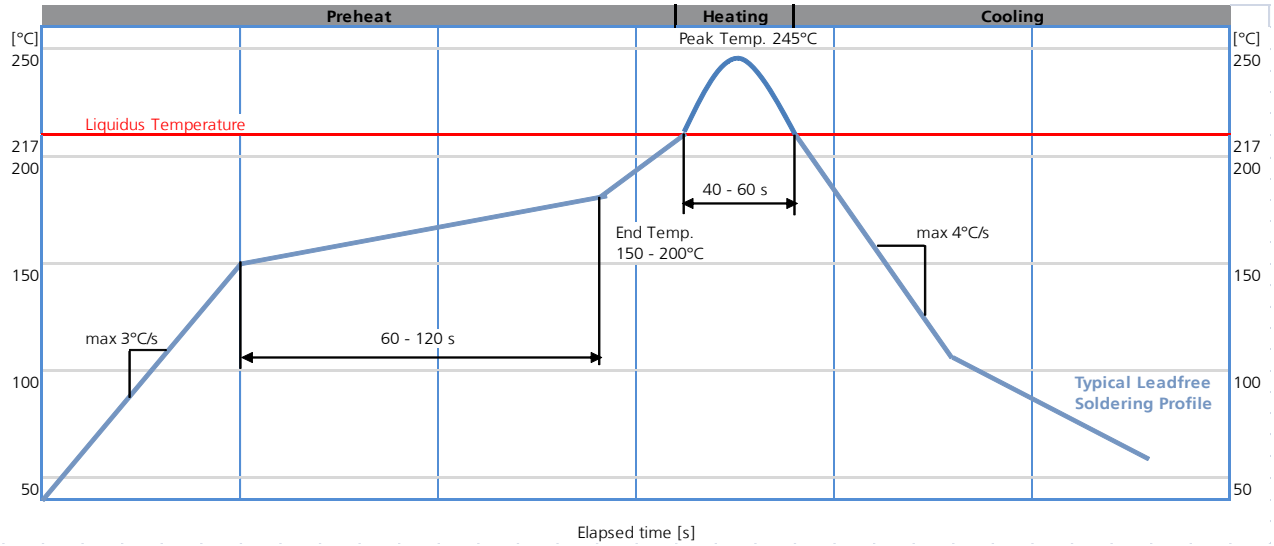

Figure 69: Recommended soldering profile

The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the TOBY-L4 series modules, inspect the modules optically to verify that the module is properly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a module populated on it.

3.3.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. TOBY-L4 series LGA modules must not be soldered with a wave soldering process.

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, and therefore care is required in applying the coating.

☞ Conformal coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the cellular modules caused by any ultrasonic processes.

4 Approvals

☞ For the complete list and specific details regarding the certification schemes approvals, see the TOBY-L4 series Data Sheet [1], or contact the u-blox office or sales representative nearest you.

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called "certification schemes" that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, such as:
    - CE (Conformité Européenne) marking for the European Union
    - FCC (Federal Communications Commission) approval for the United States
- Industry certification
  - Telecom industry specific approval verifying the interoperability between devices and networks:
    - GCF (Global Certification Forum), a partnership between mainly European device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator specific approval required by some mobile network operator, such as:
    - AT&T network operator in the United States

Even using a module already approved under all major certification schemes, the application device integrating the module must be approved under all the certification schemes required by the specific application device to be deployed into the market. The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device integrating the module is intended to be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device is intended to operate.

☞ Check the appropriate applicability of the TOBY-L4 series module's approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module's approval can significantly reduce the cost and time-to-market of the application device certification.

☞ The certification of the application device that integrates a TOBY-L4 series module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

TOBY-L4 series modules are certified according to all the supported capabilities, functions and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to the 3GPP TS 51.010-2 [11], 3GPP TS 34.121-2 [12], 3GPP TS 36.521-2 [14] and 3GPP TS 36.523-2 [15] documents, is a statement of the implemented and supported capabilities, functions and options of a device.

☞ The PICS document of the application device integrating TOBY-L4 series modules must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device.

4.2 US Federal Communications Commission notice

United States Federal Communications Commission (FCC) IDs:

- u-blox TOBY-L4006 cellular modules: XPY1EHQ37NN

4.2.1 Safety warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed

4.2.2 Declaration of conformity

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC procedures and as authorized in the module certification filing.

The gain of the system antenna(s) used for the TOBY-L4006 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value specified in the FCC Grant for mobile and fixed or mobile operating configurations:

- **10.2 dBi in the 700 MHz band, i.e. LTE FDD-12 band**
- **10.2 dBi in the 750 MHz band, i.e. LTE FDD-13 band**
- **4.0 dBi in the 850 MHz band, i.e. GSM 850, UMTS FDD-5 or LTE FDD-5 band**
- **5.5 dBi in the 1700 MHz band, i.e. UMTS FDD-4 or LTE FDD-4 band**
- **2.7 dBi in the 1900 MHz band, i.e. GSM 1900, UMTS FDD-2 or LTE FDD-2 band**

4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the TOBY-L4006 modules are authorized to use the FCC Grants of the TOBY-L4006 modules for their own final products according to the conditions referenced in the certificates.

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPY1EHQ37NN" resp.

IMPORTANT: Manufacturers of portable applications incorporating the TOBY-L4006 modules are required to have their final product certified and apply for their own FCC Grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Additional Note: as per 47CFR15.105 this equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- **Reorient or relocate the receiving antenna**
- **Increase the separation between the equipment and receiver**
- **Connect the equipment into an outlet on a circuit different from that to which the receiver is connected**
- **Consultant the dealer or an experienced radio/TV technician for help**

4.3 Innovation, Science and Economic Development Canada notice

ISED Canada (formerly known as IC - Industry Canada) Certification Numbers:

- u-blox TOBY-L4006 cellular modules: 8595A-1EHQ37NN

4.3.1 Declaration of Conformity

This device complies with the ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for the TOBY-L4006 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed not exceed the value specified in the ISED Canada Certificate Grant for mobile and fixed or mobile operating configurations:

- **7.1 dBi in the 700 MHz band, i.e. LTE FDD-12 band**
- **7.0 dBi in the 750 MHz band, i.e. LTE FDD-13 band**
- **0.7 dBi in the 850 MHz band, i.e. GSM 850, UMTS FDD-5 or LTE FDD-5 band**
- **5.5 dBi in the 1700 MHz band, i.e. UMTS FDD-4 or LTE FDD-4 band**
- **2.7 dBi in the 1900 MHz band, i.e. GSM 1900, UMTS FDD-2 or LTE FDD-2 band**

4.3.2 Modifications

The ISED Canada requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the TOBY-L4006 modules are authorized to use the ISED Canada Certificates of the TOBY-L4006 modules for their own final products according to the conditions referenced in the certificates.

The ISED Canada Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains IC: 8595A-1EHQ37NN" resp.

Innovation, Science and Economic Development Canada (ISED) Notices

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B) and RSS-210.

Operation is subject to the following two conditions:

- **this device may not cause interference**
- **this device must accept any interference, including interference that may cause undesired operation of the device**

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Cellular Module is below the Innovation, Science and Economic Development Canada (ISED) radio frequency exposure limits. The u-blox Cellular Module should be used in such a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the ISED RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Innovation, Science and Economic Development's REL (Radio Equipment List) can be found at the following web address:

http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng

Additional Canadian information on RF exposure also can be found at the following web address: http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: Manufacturers of portable applications incorporating the TOBY-L4006 modules are required to have their final product certified and apply for their own Innovation, Science and Economic Development Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Avis d'Innovation, Sciences et Développement économique Canada (ISDE)

Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3(B) / NMB-3(B) et CNR-210.

Son fonctionnement est soumis aux deux conditions suivantes :

- **cet appareil ne doit pas causer d'interférence**
- **cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement**

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Innovation, Sciences et Développement économique Canada (ISDE). Utilisez l'appareil de sans fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur:

http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: http://www.ic.gc.ca/eic/site/smt-gst.nsf/fra/sf08792.html

IMPORTANT: les fabricants d'applications portables contenant les modules TOBY-L4006 doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat ISDE Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.4 European Conformance CE mark

TOBY-L4906 modules have been evaluated against the essential requirements of the Radio Equipment Directive 2014/53/EU.

In order to satisfy the essential requirements of the 2014/53/EU RED, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 3.2):
  - EN 301 511
  - EN 301 908-1
  - EN 301 908-2
  - EN 301 908-13
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-52
- Health and Safety (Article 3.1a)
  - EN 60950-1
  - IEC 62368-1 and EN 62368-1

Radiofrequency radiation exposure information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for the TOBY-L4906 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the following values for mobile and fixed or mobile operating configurations:

- **2.9 dBi in the 900 MHz band, i.e. GSM 900 or UMTS FDD-8 band**
- **8.8 dBi in the 1800 MHz band, i.e. GSM 1800 or LTE FDD-3 band**
- **12.7 dBi in the 1900 MHz band, i.e. LTE TDD-39 band**
- **12.3 dBi in the 2100 MHz band, i.e. UMTS FDD-1 or LTE FDD-1 band**
- **13.0 dBi in the 2300 MHz band, i.e. LTE TDD-40 band**
- **13.0 dBi in the 2500 MHz band, i.e. LTE TDD-41 band**

The conformity assessment procedure for the modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed.

Thus, the following marking is included in the product:

CE

4.5 Chinese CCC and SRRC certifications

TOBY-L4906 modules have the CCC (China Compulsory Certification) and the SRRC (State Radio Regulation of China) grants.

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically in the production line. Stringent quality control process has been implemented in the production line. The defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment (ATE) in the production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. Figure 70 illustrates the typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests:

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of the reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

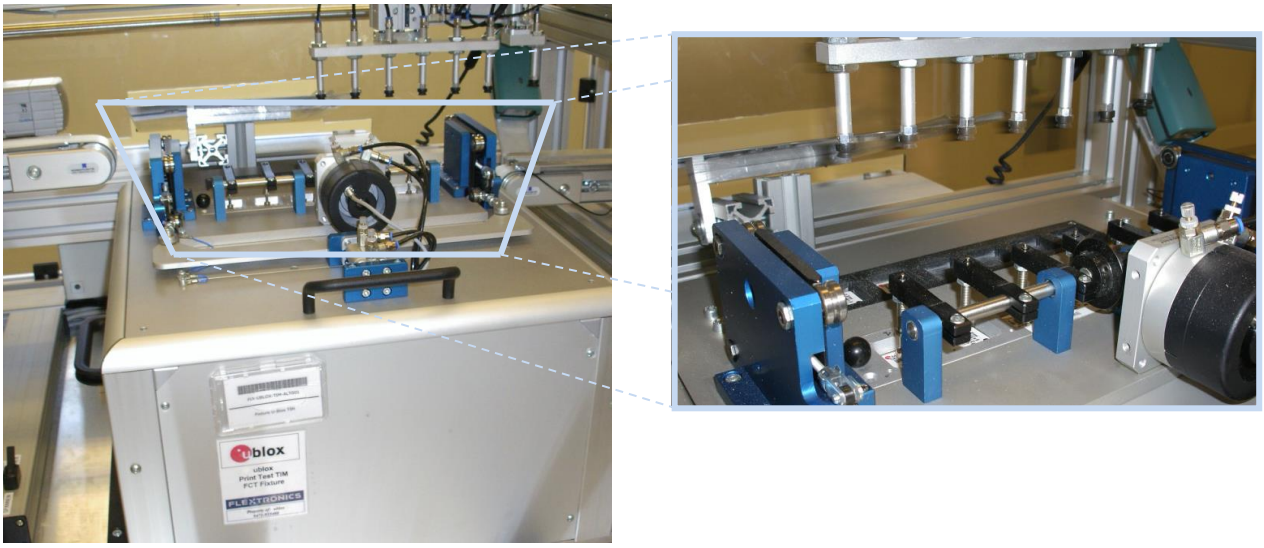

Figure 70: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturers

Because of the testing performed by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling processes did not damage the module components
  - All module pins are well soldered on the device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communications with the external host controller can be established
  - The interfaces between the module and external devices are working
  - Overall RF performance test of the device including the antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

In addition, module AT commands can be used to perform functional tests on digital interfaces (communication with host controller, check SIM interface, GPIOs, etc.), on audio interfaces (audio loop for test purposes can be enabled as described in the u-blox AT Commands Manual [2]), and to perform RF performance tests (see the following section 5.2.2 for details).

5.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test is typically performed to compare the signal quality with a "Golden Device" in a location with excellent network coverage and known signal quality. This test should be performed after data connection has been established. AT+CSQ is the typical AT command used to check signal quality in term of RSSI. See the u-blox AT Commands Manual [2] for details of the AT command.

☞ These kinds of test may be useful as a "go/no go" test but not for RF performance measurements.

This test is suitable to check the functionality of communication with the host controller or SIM card as well as the power supply. It is also a means to verify if the components are well soldered at the antenna interface.

5.2.2 RF functional tests

The overall RF functional test of the OEM device integrating the cellular module, including the antenna(s), can be performed in the OEM production line with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator with the assistance of the AT+UTEST command over the AT command user interface.

The AT+UTEST command provides a simple interface to set the module to Rx or Tx test modes ignoring the LTE/3G/2G signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported modulation schemes and bands
- receiving mode in a specified channel to returns the measured power level in all supported bands

☞ See the u-blox AT Commands Manual [2] for the AT+UTEST command syntax description.

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces on which RF performance depends.

To avoid module damage during the transmitter test, a suitable antenna according to module specifications or a 50 Ω termination must be connected to the ANT1 port.

To avoid module damage during receiver, test the maximum power level received at the ANT1 and ANT2 ports which must meet the module specifications.

The AT+UTEST command sets the module to emit RF power ignoring LTE/3G/2G signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purposes in controlled environments by qualified users and must not be used during normal module operation. Follow the instructions suggested in the u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 71 illustrates a typical test setup for such an RF functional test.

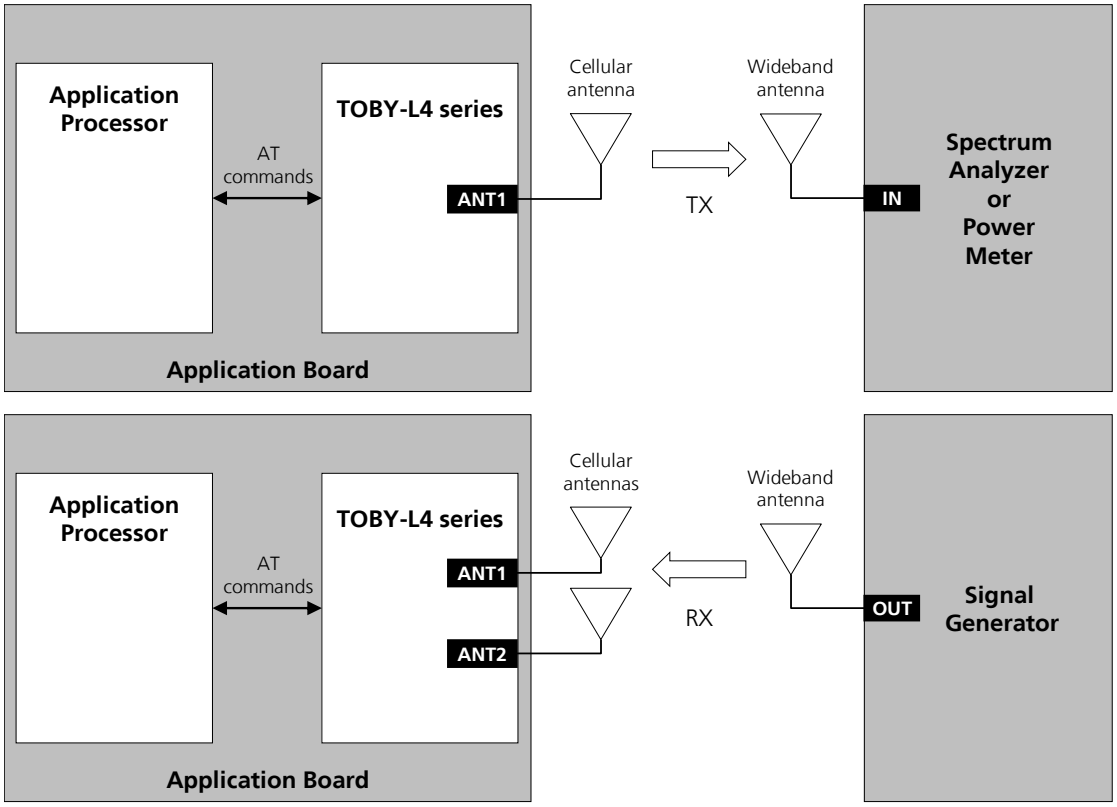

Figure 71: Setup with spectrum analyzer or power meter and signal generator for radiated measurements

Appendix

A Migration between TOBY-L2 and TOBY-L4

A.1 Overview

TOBY-L2 and TOBY-L4 series cellular modules have the same TOBY form factor (35.6 x 24.8 mm LGA), with a different number of pins: as illustrated in Figure 72, TOBY-L2 modules have 152 pins, while TOBY-L4 modules have the same 152 pins of TOBY-L2 modules plus 96 additional pins, reaching a total number of 248 pins.

Figure 72 shows that all the functions provided by the 152 pins of TOBY-L2 modules are also available on the same pins of TOBY-L4 modules, which provide additional functions (RGMII and UART3 interfaces) on RSVD pins of TOBY-L2 modules, intended to be left unconnected on a board designed for TOBY-L2 modules.

This means that TOBY-L2 and TOBY-L4 series modules can be alternatively mounted on a single application board using exactly the same copper mask, solder mask and paste mask: TOBY-L4 series modules can be mounted on any design appropriately implemented for TOBY-L2 modules, given that any additional interface provided by TOBY-L4 modules will result not connected.

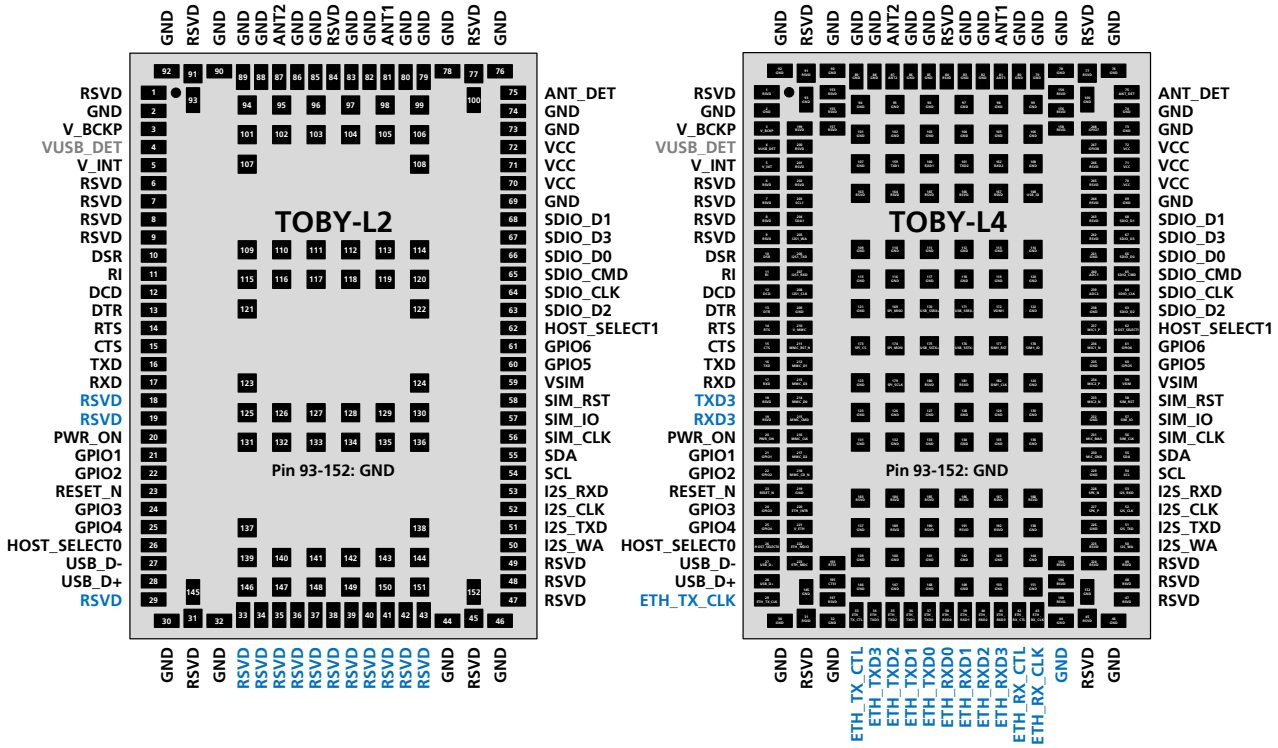

Figure 72: TOBY-L2 and TOBY-L4 series modules pad layout and pin assignment

TOBY modules are also form-factor compatible with the u-blox LISA, SARA and LARA cellular module families: although TOBY modules, LISA modules (33.2 x 22.4 mm, 76-pin LCC), SARA modules (26.0 x 16.0 mm, 96-pin LGA) and LARA modules (26.0 x 24.0 mm, 100-pin LGA) each have different form factors, the footprints for the TOBY, LISA, SARA and LARA modules have been developed to ensure layout compatibility.

With the u-blox "nested design" solution, any TOBY, LISA, SARA or LARA module can be alternatively mounted on the same space of a single "nested" application board as described in the Nested Design Application Note [19].

Figure 73 summarizes the LTE, 3G and 2G operating frequency bands of TOBY-L2 and TOBY-L4 series modules.

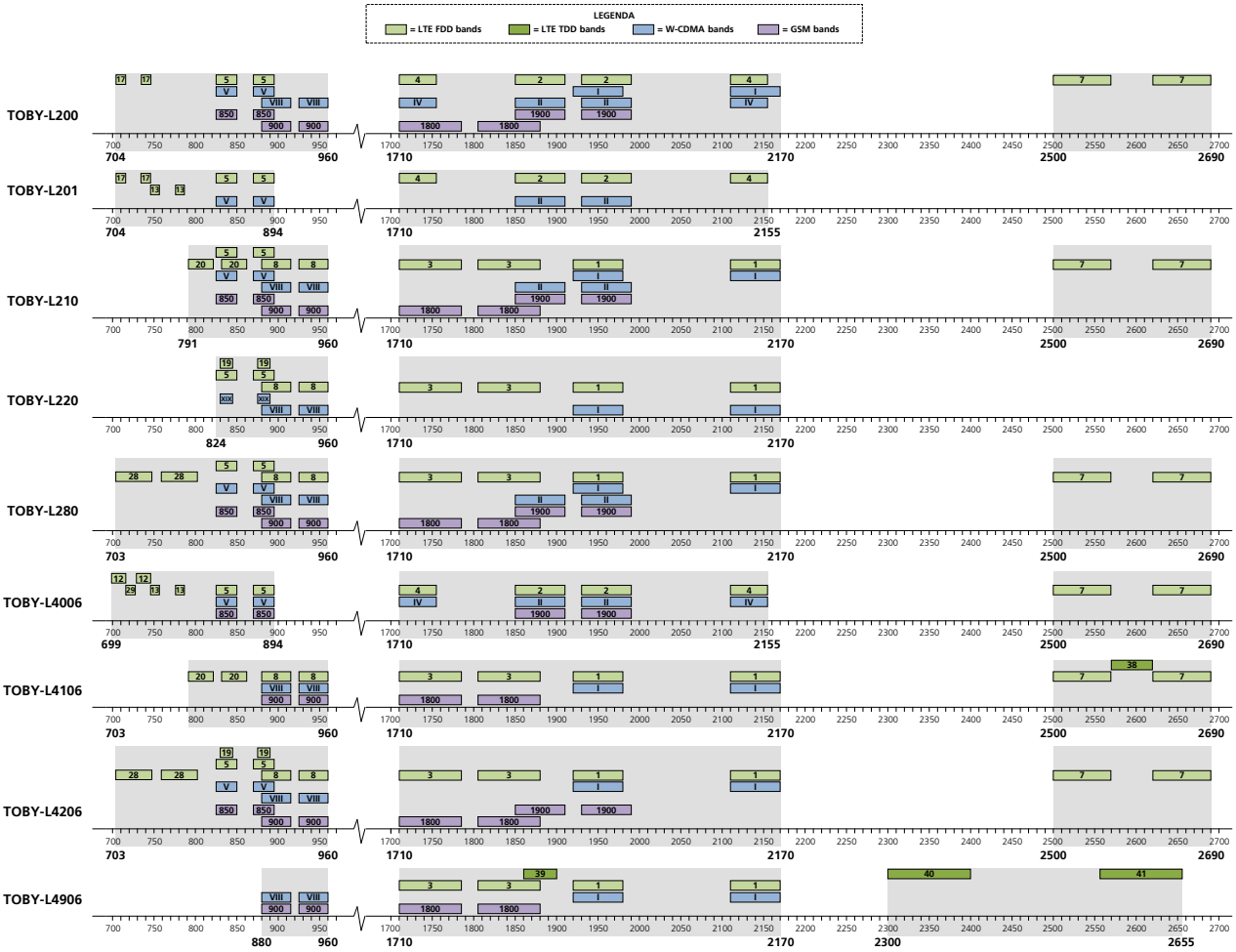

Figure 73: Summary of TOBY-L2 and TOBY-L4 series modules LTE, 3G and 2G operating frequency bands

A.2 Pin-out comparison between TOBY-L2 and TOBY-L4

	TOBY-L2		TOBY-L4		
Pin No	Pin Name	Description	Pin Name	Description	Remarks for migration
1	RSVD	Reserved	RSVD	Reserved	
2	GND	Ground	GND	Ground	
3	V_BCKP	RTC Back-up Supply	V_BCKP	RTC Back-up Supply	
4	VUSB_DET	Not supported	VUSB_DET	VBUS USB supply (5 V) detection	5 V must be applied at VUSB_DET of TOBY-L4 to enable USB device. The pin must be left unconnected on TOBY-L2, as it is not supported.
5	V_INT	1.8 V Interfaces Supply Output	V_INT	1.8 V Interfaces Supply Output	
6	RSVD	Reserved This pin must be connected to GND	RSVD	Reserved This pin must be connected to GND	
7-9	RSVD	Reserved	RSVD	Reserved	
10	DSR	UART DSR Output[22] / GPIO[23]	DSR	GPIO[24] / EINT[24]	
11	RI	UART RI Output[22] / GPIO[23]	RI	UART0 RI Output / GPIO / EINT[24]	
12	DCD	UART DCD Output[22] / GPIO[23]	DCD	GPIO[24] / EINT[24]	
13	DTR	UART DTR Input[22] / GPIO[23]	DTR	GPIO[24] / EINT[24]	
14	RTS	UART RTS Input[22]	RTS	UART0 RTS Input[24]	
15	CTS	UART CTS Output[22]	CTS	UART0 CTS Output[24]	
16	TXD	UART Data Input[22]	TXD	UART0 Data Input[24]	
17	RXD	UART Data Output[22]	RXD	UART0 Data Output[24]	
18	RSVD	Reserved	TXD3	UART3 Data Input[24]	RSVD → UART3
19	RSVD	Reserved	RXD3	UART3 Data Output[24]	RSVD → UART3
20	PWR_ON	Power-on Input Internal 50k pull-up to VCC Switch-on, Switch-off	PWR_ON	Power-on Input Internal 35k pull-up to 1.3 V Switch-on, Switch-off	Internal pull-up slightly different No functional difference
21	GPIO1	GPIO[23]	GPIO1	GPIO	
22	GPIO2	GPIO[23]	GPIO2	GPIO	
23	RESET_N	Reset signal Input Internal 50k pull-up to VCC Reset, Switch-on, Switch-off	RESET_N	Reset signal Input Internal 100k pull-up to V_INT Reset	Internal pull-up slightly different. Function slightly different.
24	GPIO3	GPIO[23]	GPIO3	GPIO	
25	GPIO4	GPIO[23]	GPIO4	GPIO	
26	HOST_SELECT0	Not supported	HOST_SELECT0	GPIO[24] / EINT[24]	Not supported → GPIO / EINT
27	USB_D-	USB Data I/O (D-)	USB_D-	USB Data I/O (D-)	
28	USB_D+	USB Data I/O (D+)	USB_D+	USB Data I/O (D+)	
29	RSVD	Reserved	ETH_TX_CLK	Ethernet Transmission Clock[24]	RSVD → RGMII
30	GND	Ground	GND	Ground	
31	RSVD	Reserved	RSVD	Reserved	
32	GND	Ground	GND	Ground	
33	RSVD	Reserved	ETH_TX_CTL	Ethernet Transmit Control[24]	RSVD → RGMII
34	RSVD	Reserved	ETH_TXD3	Ethernet Transmit Data [3][24]	RSVD → RGMII
35	RSVD	Reserved	ETH_TXD2	Ethernet Transmit Data [2][24]	RSVD → RGMII
36	RSVD	Reserved	ETH_TXD1	Ethernet Transmit Data [1][24]	RSVD → RGMII
37	RSVD	Reserved	ETH_TXD0	Ethernet Transmit Data [0][24]	RSVD → RGMII
38	RSVD	Reserved	ETH_RXD0	Ethernet Receive Data [0][24]	RSVD → RGMII
39	RSVD	Reserved	ETH_RXD1	Ethernet Receive Data [1][24]	RSVD → RGMII
40	RSVD	Reserved	ETH_RXD2	Ethernet Receive Data [2][24]	RSVD → RGMII
41	RSVD	Reserved	ETH_RXD3	Ethernet Receive Data [3][24]	RSVD → RGMII
42	RSVD	Reserved	ETH_RX_CTL	Ethernet Receive Control[24]	RSVD → RGMII
43	RSVD	Reserved	ETH_RX_CLK	Ethernet Receive Clock[24]	RSVD → RGMII
44	GND	Ground	GND	Ground	
45	RSVD	Reserved	RSVD	Reserved	
46	GND	Ground	GND	Ground	

[22] Not supported by "00" product versions
[23] Not supported by "00", "01", "60" product versions
[24] Not supported by "50" product versions

	TOBY-L2		TOBY-L4		
Pin No	**Pin Name**	**Description**	**Pin Name**	**Description**	**Remarks for migration**
47-49	RSVD	Reserved	RSVD	Reserved	
50	I2S_WA	I²S Word Alignment[22] / GPIO[23]	I2S_WA	I²S Word Alignment	I2S / GPIO → I2S
51	I2S_TXD	I²S Data Output[22] / GPIO[23]	I2S_TXD	I²S Data Output	I2S / GPIO → I2S
52	I2S_CLK	I²S Clock[22] / GPIO[23]	I2S_CLK	I²S Clock	I2S / GPIO → I2S
53	I2S_RXD	I²S Data Input[22] / GPIO[23]	I2S_RXD	I²S Data Input	I2S / GPIO → I2S
54	SCL	I²C Clock Output[25]	SCL	I²C Clock Output[26]	
55	SDA	I²C Data I/O[25]	SDA	I²C Data I/O[26]	
56	SIM_CLK	SIM Clock Output	SIM_CLK	SIM Clock Output	
57	SIM_IO	SIM Data I/O	SIM_IO	SIM Data I/O	
58	SIM_RST	SIM Reset Output	SIM_RST	SIM Reset Output	
59	VSIM	SIM Supply Output	VSIM	SIM Supply Output	
60	GPIO5	GPIO[25]	GPIO5	GPIO	
61	GPIO6	GPIO[25]	GPIO6	GPIO	
62	HOST_SELECT1	Not supported	HOST_SELECT1	GPIO[26] / EINT[26]	Not supported → GPIO / EINT
63	SDIO_D2	SDIO serial data [2][25]	SDIO_D2	SDIO serial data [2][26]	
64	SDIO_CLK	SDIO serial clock[25]	SDIO_CLK	SDIO serial clock[26]	
65	SDIO_CMD	SDIO command[25]	SDIO_CMD	SDIO command[26]	
66	SDIO_D0	SDIO serial data [0][25]	SDIO_D0	SDIO serial data [0][26]	
67	SDIO_D3	SDIO serial data [3][25]	SDIO_D3	SDIO serial data [3][26]	
68	SDIO_D1	SDIO serial data [1][25]	SDIO_D1	SDIO serial data [1][26]	
69	GND	Ground	GND	Ground	
70-72	VCC	Module Supply Input 3.40 V – 4.35 V normal range 3.20 V – 4.35 V extended range	VCC	Module Supply Input 3.40 V – 4.40 V normal range 3.00 V – 4.50 V extended range	Larger operating ranges on TOBY-L4
73-74	GND	Ground	GND	Ground	
75	ANT_DET	Antenna Detection Input[25]	ANT_DET	Antenna Detection Input	
76	GND	Ground	GND	Ground	
77	RSVD	Reserved	RSVD	Reserved	
78-80	GND	Ground	GND	Ground	
81	ANT1	RF Antenna Input/Output Up to six LTE bands Up to five 3G bands Up to four 2G bands	ANT1	RF Antenna Input/Output Up to seven LTE bands Up to three 3G bands Up to four 2G bands	No RF functional difference Different operating bands (Figure 73)
82-83	GND	Ground	GND	Ground	
84	RSVD	Reserved	RSVD	Reserved	
85-86	GND	Ground	GND	Ground	
87	ANT2	RF Antenna Input	ANT2	RF Antenna Input	No RF functional difference Different operating bands (Figure 73)
88-90	GND	Ground	GND	Ground	
91	RSVD	Reserved	RSVD	Reserved	
92-152	GND	Ground	GND	Ground	
152-248		Pins not available		Additional functions	Not available → Additional functions

Table 52: TOBY-L2 and TOBY-L4 series modules pin assignment with remarks for migration

☞ For further details regarding the characteristics, capabilities, usage or settings applicable for each interface of the cellular modules, see the TOBY-L4 series Data Sheet [1], the TOBY-L2 series Data Sheet [17], the TOBY-L2 / MPCI-L2 series System Integration Manual [18], and the u-blox AT Commands Manual [2].

[25] Not supported by "00", "01", "60" product versions
[26] Not supported by "50" product versions

B Glossary

3GPP	3rd Generation Partnership Project
8-PSK	8 Phase-Shift Keying modulation
16QAM	16-state Quadrature Amplitude Modulation
64QAM	64-state Quadrature Amplitude Modulation
ACM	Abstract Control Model
ADC	Analog to Digital Converter
AP	Application Processor
API	Application Program Interface
ASIC	Application-Specific Integrated Circuit
AT	AT Command Interpreter Software Subsystem, or attention
BAW	Bulk Acoustic Wave
CA	Carrier Aggregation
CSFB	Circuit Switched Fall-Back
DC	Direct Current
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DTE	Data Terminal Equipment
EDGE	Enhanced Data rates for GSM Evolution
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
eMMC	Embedded Multi-Media Card
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
E-UTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplex
FEM	Front End Module
FOAT	Firmware Over AT commands
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware
GMSK	Gaussian Minimum-Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
HBM	Human Body Model
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	HyperText Transfer Protocol
HW	Hardware
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit interface
I^2S	Inter IC Sound interface
LDO	Low-Dropout

LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low Power Double Data Rate synchronous dynamic RAM memory
LTE	Long Term Evolution
M2M	Machine-to-Machine
MIMO	Multi-Input Multi-Output
N/A	Not Applicable
N.A.	Not Available
OEM	Original Equipment Manufacturer device: an application device integrating a u-blox cellular module
OTA	Over The Air
PA	Power Amplifier
PCM	Pulse Code Modulation
PCN	Product Change Notification / Information Note / Sample Delivery Note
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PWM	Pulse Width Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RSE	Radiated Spurious Emission
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input Output
SDN / PCN / IN	Sample Delivery Note / Product Change Notification / Information Note
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
SRF	Self Resonant Frequency
SSL	Secure Socket Layer
TBD	To Be Defined
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TIS	Total Isotropic Sensitivity
TP	Test-Point
TRP	Total Radiated Power
UART	Universal Asynchronous Receiver-Transmitter
uCPU	u-blox universal Central Processing Unit
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
VoLTE	Voice over LTE
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WLAN	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WWAN	Wireless Wide Area Network (GSM / UMTS / LTE cellular radio technology)

Related documents

[1] u-blox TOBY-L4 series Data Sheet, Docu No UBX-16009856

[2] u-blox AT Commands Manual, Docu No UBX-13002752

[3] Universal Serial Bus Rev. 2.0 specification, http://www.usb.org/developers/docs/usb20_docs/

[4] Universal Serial Bus Rev. 3.0 specification, http://www.usb.org/developers/docs/documents_archive/

[5] ITU-T Recommendation V.24 - 02-2000 - List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE), http://www.itu.int/rec/T-REC-V.24-200002-I/en

[6] I^2C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP Semiconductors, http://www.nxp.com/documents/user_manual/UM10204.pdf

[7] Reduced Gigabit Media-Independent Interface (RGMII) Version 1.3, www.hp.com/rnd/pdfs/RGMIIv1_3.pdf

[8] Reduced Media-Independent Interface (RMII) Specification, Rev. 1.2

[9] JESD84-B451 - Embedded Multimedia Card (eMMC), Electrical Standard 4.51

[10] GSM Association TS.09 - Battery Life Measurement and Current Consumption Technique https://www.gsma.com/newsroom/wp-content/uploads//TS.09_v10.0.pdf

[11] 3GPP TS 51.010-2 - Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS)

[12] 3GPP TS 34.121-2 - Technical Specification Group Radio Access Network; User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 2: Implementation Conformance Statement (ICS)

[13] 3GPP TS 36.521-1 - Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing

[14] 3GPP TS 36.521-2 - Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)

[15] 3GPP TS 36.523-2 - Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)

[16] u-blox Package Information Guide, Docu No UBX-14001652

[17] u-blox TOBY-L2 series Data Sheet, Docu No UBX-13004573

[18] u-blox TOBY-L2 / MPCI-L2 series System Integration Manual, Docu No UBX- 13004618

[19] u-blox Nested Design Application Note, Docu No UBX-16007243

Some of the above documents can be downloaded from the u-blox web-site (http://www.u-blox.com/).

Revision history

Revision	Date	Name	Status / Comments
R01	03-Mar-2017	sses	Initial release
R02	02-Aug-2017	sses	Added document applicability to "50" product versions. Updated FW features supported by "00" product versions. Updated 3G maximum data rate. Clarified Rx diversity support. Updated Power-on and Power-off sections. Updated USB, UART, I2C, GPIOs supported functions / features. Updated support of SIM interfaces and digital audio interfaces. Corrected some typo in migration between TOBY-L2 and TOBY-L4. Minor other corrections.
R03	03-Jan-2018	sses	Added USB capabilities. Added data rate supported by UART, SPI and I2C interfaces. Added SDIO capabilities and application circuit. Updated recommended Ethernet PHY chips. Added analog audio use-cases and digital audio interfaces capabilities. Added GPIOs capabilities. Clarified application circuits with SIM interfaces. Minor other corrections.
R04	08-Feb-2018	sses	Updated TOBY-4006-50A / TOBY-4106-50A product status. Added FCC, ISED, CE, CCC and SRRC sections including related approvals info. Updated minimum limit for VCC normal operating range.

Contact

For complete contact information visit us at http://www.u-blox.com/

u-blox Offices

North, Central and South America

u-blox America, Inc.
Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:
Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

Technical Support:
Phone: +1 703 483 3185
E-mail: support_us@u-blox.com

Headquarters Europe, Middle East, Africa

u-blox AG
Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.
Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office Australia:
Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support: support_ap@u-blox.com

Regional Office China (Beijing):
Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Chongqing):
Phone: +86 23 6815 1588
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shanghai):
Phone: +86 21 6090 4832
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shenzhen):
Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office India:
Phone: +91 80 4050 9200
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

Regional Office Japan (Osaka):
Phone: +81 6 6941 3660
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Japan (Tokyo):
Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:
Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:
Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com