CELLULAR

SARA-R4 series

LTE Cat M1 modules

System Integration Manual

Abstract

This document describes the features and the system integration of SARA-R4 series cellular modules.

These modules are a complete, cost efficient and performance optimized LTE Cat M1 solution in the compact SARA form factor.

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Document Information		
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Document status explanation	
Objective Specification	Document contains target values. Revised and supplementary data will be published later.
Advance Information	Document contains data based on early testing. Revised and supplementary data will be published later.
Early Production Information	Document contains data from product verification. Revised and supplementary data may be published later.
Production Information	Document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
SARA-R404M	SARA-R404M-00B-00	K0.0.00.00.05.01	UBX-17003782

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **AT Commands Manual**: This document provides the description of the AT commands supported by the u-blox cellular modules.
- **System Integration Manual**: This document provides the description of u-blox cellular modules' system from the hardware and the software point of view, it provides hardware design guidelines for the optimal integration of the cellular modules in the application device and it provides information on how to set up production and final product tests on application devices integrating the cellular modules.
- **Application Note**: These documents provide guidelines and information on specific hardware and/or software topics on u-blox cellular modules. See Related documents for a list of Application Notes related to your Cellular Module.

How to use this Manual

The SARA-R4 series System Integration Manual provides the necessary information to successfully design and configure the u-blox cellular modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox Cellular Integration:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com/

Technical Support

Worldwide Web

Our website (http://www.u-blox.com/) is a rich pool of information. Product information, technical documents can be accessed 24h a day.

By E-mail

Contact the closest Technical Support office by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support, have the following information ready:

- Module type (SARA-R404M) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

The SARA-R4 series comprises LTE Cat M1 modules supporting single band data transmission in the small SARA LGA form-factor (26.0 x 16.0 mm), that allows an easy integration in compact designs and a seamless drop-in migration from u-blox cellular module families.

SARA-R4 series modules are form-factor compatible with u-blox LISA, LARA and TOBY cellular module families and are pin-to-pin compatible with u-blox SARA-N, SARA-G and SARA-U cellular module families. This facilitates migration from the u-blox NB-IoT, GSM/GPRS, CDMA, UMTS/HSPA and other LTE modules, maximizes customers investments, simplifies logistics, and enables very short time-to-market.

The modules are ideal for LPWA applications with low to medium data throughput rates, as well as devices that require long battery lifetimes, such as connected health, smart metering, smart cities and wearables.

SARA-R4 series includes the following modules:

- SARA-R404M, designed primarily to operate in North America on the Verizon network.

LTE Cat M1 supports vehicular handover capability and delivers the technology necessary to enable the use of the modules in applications such as vehicle, asset and people tracking where mobility is a pre-requisite. Other applications where the module is well suited include and are not limited to: smart home, security systems, industrial monitoring and control.

SARA-R4 series modules support data communication with a throughput of 375 kb/s.

Table 1 summarizes the main features and interfaces of SARA-R4 series modules.

Module	LTE		Interfaces					Audio		Features								Grade		
	LTE FDD category	Bands	UART	USB 2.0	SDIO	DDC (I^2C)	GPIOs	Analog audio	Digital audio	Network indication	Antenna supervisor	Embedded TCP/UDP, FTP	Embedded SSL	Embedded HTTP	FOAT	FOTA	Dual stack IPv4/IPv6	Standard	Professional	Automotive
SARA-R404M	M1	13	•	•	F	F	•		F	•	•	•	•	•	•	F	•			

F = supported by future product versions

Table 1: SARA-R4 series main features summary

Table 2 reports a summary of cellular radio access technologies characteristics and features of the modules.

Item	SARA-R404M
Protocol stack release	3GPP Release 13 Frequency Division Duplex (FDD) Half-Duplex
Operating band	Band 13 (Upper 700 MHz)
Power class	Power Class 3 (23 dBm)
Data rate	375 kb/s DL/UL

Table 2: SARA-R4 series characteristics summary

1.2 Architecture

Figure 1 summarizes the internal architecture of SARA-R4 series modules.

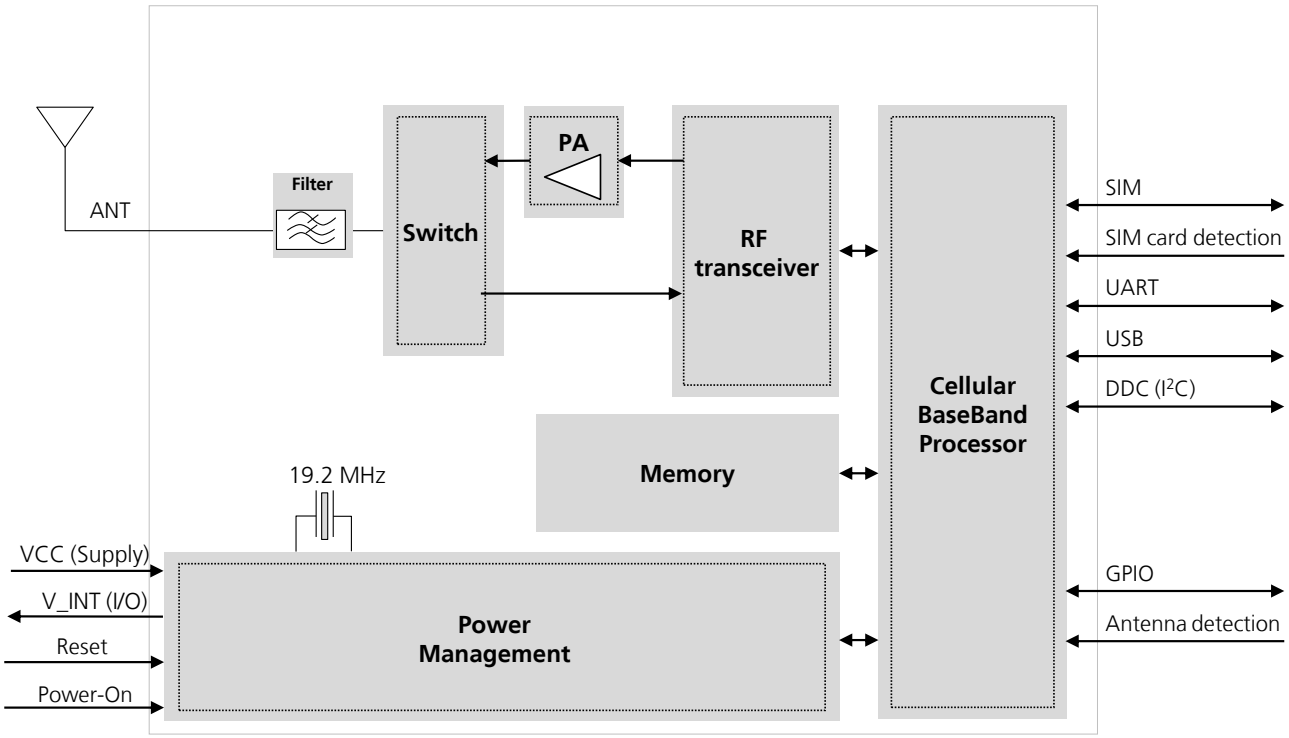

Figure 1: SARA-R4 series modules simplified block diagram

1.3 Pin-out

Table 3 lists the pin-out of the SARA-R4 series modules, with pins grouped by function.

Function	Pin Name	Pin No	I/O	Description	Remarks
Power	**VCC**	51, 52, 53	I	Module supply input	**VCC** supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description / requirements. See section 2.2.1 for external circuit design-in.
	GND	1, 3, 5, 14, 20-22, 30, 32, 43, 50, 54, 55, 57-61, 63-96	N/A	Ground	**GND** pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_INT	4	O	Generic digital interfaces supply output	**V_INT** = 1.8 V (typical) generated by internal DC/DC regulator when the module is switched on. Test-Point for diagnostic access is recommended. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
System	**PWR_ON**	15	I	Power-on input	Internal 200 kΩ pull-up resistor. See section 1.6.1 for functional description. See section 2.3.1 for external circuit design-in.
	RESET_N	18	I	External reset input	Internal pull-up resistor to **V_INT**. Test-Point for diagnostic access is recommended. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.
Antenna	**ANT**	56	I/O	Primary antenna	Main Tx / Rx antenna interface. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7 for functional description / requirements. See section 2.4 for external circuit design-in.
	ANT_DET	62	I	Antenna detection	ADC for antenna presence detection function See section 1.7.2 for functional description. See section 2.4.2 for external circuit design-in.
SIM	**VSIM**	41	O	SIM supply output	**VSIM** = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	39	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM Internal 4.7 kΩ pull-up to **VSIM**. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	38	O	SIM clock	3.25 MHz clock output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	40	O	SIM reset	Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
UART	**RXD**	13	O	UART data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, for AT commands, data communication, FOAT and diagnostic. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	TXD	12	I	UART data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, for AT commands, data communication, FOAT and diagnostic. Internal active pull-up to **V_INT**. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	11	O	UART clear to send output	1.8 V output, Circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	10	I	UART ready to send input	1.8 V input, Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to **V_INT**. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	6	O	UART data set ready output	1.8 V, Circuit 107 in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	7	O	UART ring indicator output	1.8 V, Circuit 125 in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	I	UART data terminal ready input	1.8 V, Circuit 108/2 in ITU-T V.24. Internal active pull-up to **V_INT**. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DCD	8	O	UART data carrier detect output	1.8 V, Circuit 109 in ITU-T V.24. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
USB	**VUSB_DET**	17	I	USB detect input	VBUS (5 V typical) USB supply generated by the host must be connected to this input pin to enable the USB interface. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	USB_D-	28	I/O	USB Data Line D-	USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance (Z_0) 30 Ω nominal common mode impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [4] are part of the USB pin driver and need not be provided externally. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	USB_D+	29	I/O	USB Data Line D+	USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance (Z_0) 30 Ω nominal common mode impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [4] are part of the USB pin driver and need not be provided externally. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
DDC	**SCL**	27	O	I^2C bus clock line	1.8 V open drain, for communication with I2C-slave devices. External pull-up are not required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	SDA	26	I/O	I^2C bus data line	1.8 V open drain, for communication with I2C-slave devices. External pull-up are not required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
GPIO	**GPIO1**	16	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO2	23	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO3	24	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO4	25	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	SIM_DET	42	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
Reserved	**RSVD**	2, 31, 33-37, 44-49	N/A	Reserved pin	Leave unconnected. See sections 1.11 and 2.8

Table 3: SARA-R4 series module pin definition, grouped by function

1.4 Operating modes

SARA-R4 series modules have several operating modes. The operating modes are defined in Table 4 and described in detail in Table 5, providing general guidelines for operation.

General Status	Operating Mode	Definition
Power-down	**Not-Powered Mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-Off Mode	**VCC** supply within operating range and module is switched off.
Normal Operation	**Idle-Mode**	Module processor core runs with 32 kHz reference internally generated.
	Active-Mode	Module processor core runs with 19.2 MHz reference generated by the internal oscillator.
	Connected-Mode	RF Tx/Rx data connection enabled and processor core runs with 19.2 MHz reference.

Table 4: SARA-R4 series modules operating modes definition

Mode	Description	Transition between operating modes
Not-Powered	Module is switched off. Application interfaces are not accessible.	When **VCC** supply is removed, the modules enter not-powered mode. When in not-powered mode, the module can enter power-off mode applying **VCC** supply (see 1.6.1).
Power-Off	Module is switched off: normal shutdown by an appropriate power-off event (see 1.6.2). Application interfaces are not accessible.	When the modules are switched off by an appropriate switch-off event (see 1.6.2), the modules enter power-off mode from active-mode. When in power-off mode, the modules can be switched on by **PWR_ON**. When in power-off mode, the modules enter not-powered mode by removing **VCC** supply.
Idle	Module is switched on with application interfaces temporarily disabled or suspended: the module is temporarily not ready to communicate with an external device by means of the application interfaces as configured to reduce the current consumption. The module enters the low power idle-mode whenever possible if power saving is enabled by AT+UPSV command (see u-blox SARA-R404M AT Commands Manual [1]) reducing current consumption (see 1.5.1.3). The **CTS** output line indicates when the UART interface is disabled/enabled due to the module idle/active-mode transitions according to the power saving and HW flow control settings (see 1.9.1.2). Power saving configuration is not enabled by default; it can be enabled by AT+UPSV (see the u-blox SARA-R404M AT Commands Manual [1]).	The modules automatically switch from the active-mode to low power idle-mode whenever possible if power saving is enabled (see sections 1.5.1.30 and u-blox SARA-R404M AT Commands Manual [1], AT+UPSV command). The modules wake up from low power idle-mode to active-mode in the following events: • Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (see 1.5.1.3) • Automatic periodic enable of the UART interface to receive / send data, with AT+UPSV=1 • Data received over UART, according to HW flow control (AT&K) and power saving (AT+UPSV) settings • **RTS** input set ON by the host DTE, with HW flow control disabled and AT+UPSV=2 • **DTR** input set ON by the host DTE, with AT+UPSV=3 • USB detection, applying 5 V (typ.) to **VUSB_DET** input (see 1.9.2) • The connected USB host forces a remote wakeup of the module as USB device (see 0)
Active	Module is switched on with application interfaces enabled or not suspended: the module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by AT+UPSV (see 0u-blox SARA-R404M AT Commands Manual [1]).	When the modules are switched on by an appropriate power-on event (see 1.6.1), the modules enter active-mode from not-powered or power-off mode. If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from active to idle-mode whenever possible and the module wakes up from idle to active-mode in the events listed above (see idle-mode to active-mode transition description above). When a RF Tx/Rx data connection is initiated or when RF Tx/Rx activity is required due to a connection previously initiated, the module switches from active to connected-mode.

Mode	Description	Transition between operating modes
Connected	RF Tx/Rx data connection is in progress. The module is prepared to accept data signals from an external device unless power saving configuration is enabled by AT+UPSV (see 0u-blox SARA-R404M AT Commands Manual [1]).	When a data connection is initiated, the module enters connected-mode from active-mode. Connected-mode is suspended if Tx/Rx data is not in progress, due to connected discontinuous reception and fast dormancy capabilities of the module and according to the network environment settings and scenario. In such cases the module automatically switches from connected to active mode and then, if power saving configuration is enabled by the AT+UPSV command, the module automatically switches to idle-mode whenever possible. Vice-versa, the module wakes up from idle to active mode and then connected mode if RF Tx/Rx activity is necessary. When a data connection is terminated, the module returns to the active-mode.

Table 5: SARA-R4 series modules operating modes description

Figure 2 describes the transition between the different operating modes.

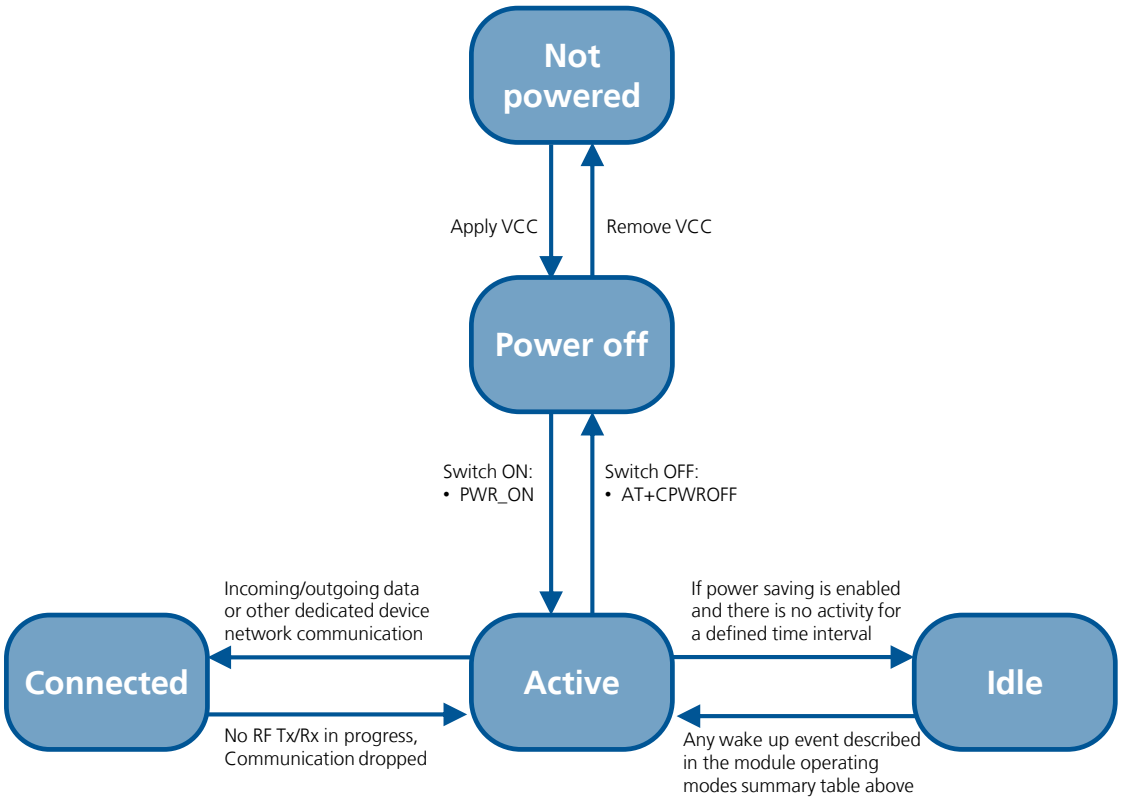

Figure 2: SARA-R4 series modules operating modes transitions

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

During operation, the current drawn by the SARA-R4 series modules through the **VCC** pins can vary by several orders of magnitude, depending on the operating mode and state (as described in sections 1.5.1.2, 1.5.1.3 and 1.5.1.4).

It is important that the supply source is able to support the average current consumption occurring during a LTE transmission at maximum RF power level.

1.5.1.1 VCC supply requirements

Table 6 summarizes the requirements for the **VCC** modules supply. See section 2.2.1 for suggestions to properly design a **VCC** supply circuit compliant with the requirements listed in Table 6.

The supply circuit affects the RF compliance of the device integrating SARA-R4 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the requirements summarized in the Table 6 are fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.20 V min. / 4.40 V max	RF performance is guaranteed when **VCC** voltage is inside the normal operating range limits. RF performance may be affected when **VCC** voltage is outside the normal operating range limits, though the module is still fully functional until the **VCC** voltage is inside the extended operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.00 V min. / 4.30 V max	**VCC** voltage must be above the extended operating range minimum limit to switch-on the module. The module may switch-off when the **VCC** voltage drops below the extended operating range minimum limit. Operation above **VCC** extended operating range is not recommended and may affect device reliability.
VCC average current	Support with adequate margin the highest averaged **VCC** current consumption value in connected-mode conditions specified in SARA-R4 Data Sheet [1]	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Section 1.5.1.2 describes current consumption profiles in LTE connected-mode.
VCC voltage ripple during LTE Tx	Noise in the supply pins has to be minimized	High supply voltage ripple values during LTE RF transmissions in connected-mode directly affect the RF compliance with the applicable certification schemes.

Table 6: Summary of VCC modules supply requirements

1.5.1.2 VCC current consumption in connected-mode

During an LTE connection, the SARA-R4 module transmits and receives in half duplex mode. The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. Figure 3 shows an example of the module current consumption profile versus time in LTE connected-mode. Detailed current consumption values can be found in SARA-R4 series Data Sheet [1].

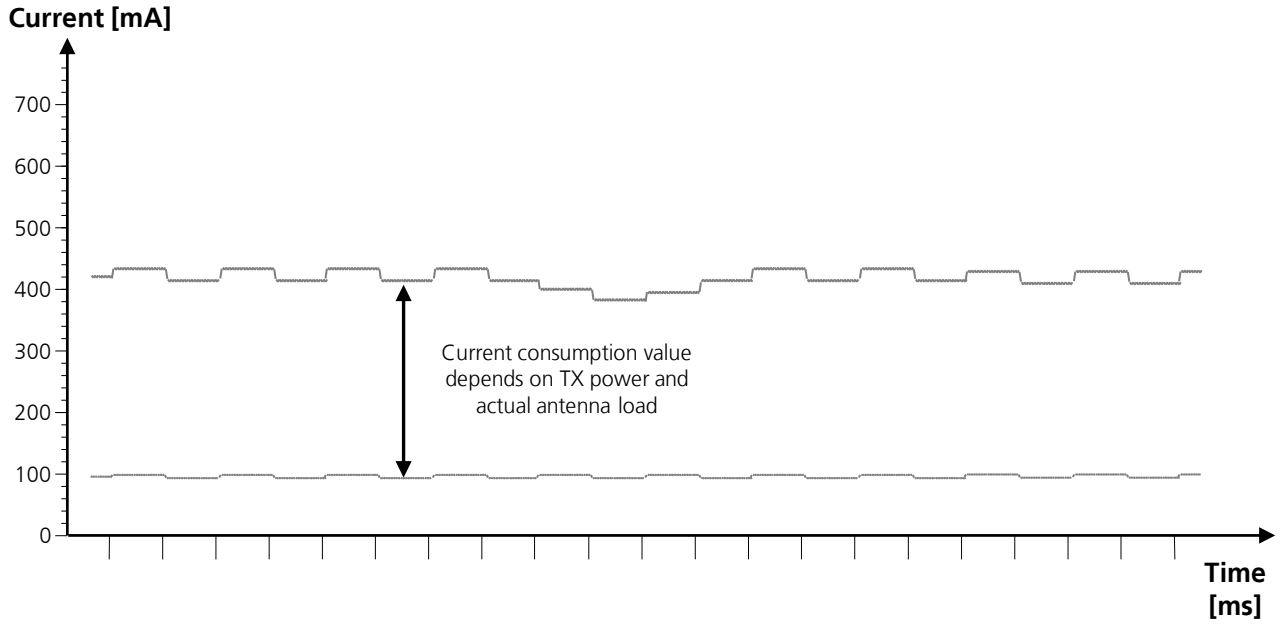

Figure 3: VCC current consumption profile versus time during a LTE data connection

1.5.1.3 VCC current consumption in cyclic idle/active mode (power saving enabled)

The power saving configuration is by default disabled, but it can be enabled using the AT+UPSV command (see the u-blox SARA-R404M AT Commands Manual [1]). When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption.

During low power idle-mode, the module processor runs with internal 32 kHz reference clock frequency.

When the power saving configuration is enabled and the module is registered or attached to a network, the module automatically enters the low power idle-mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the LTE system requirements. When the module monitors the paging channel, it wakes up to the active-mode, to enable the reception of paging block. In between, the module switches to low power idle-mode. This is known as discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 19.2 MHz used in active-mode.

The time period between two paging block receptions is defined by the network. This is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell.

1.5.1.4 VCC current consumption in fixed active-mode (power saving disabled)

When power saving is disabled, the module does not automatically enter the low power idle-mode whenever possible: the module remains in active-mode. Power saving configuration is by default disabled. It can also be disabled using the AT+UPSV command (see u-blox SARA-R404M AT Commands Manual [1] for detail usage).

The module processor core is activated during idle-mode, and the 19.2 MHz reference clock frequency is used. It would draw more current during the paging period than that in the power saving mode.

1.5.2 Generic digital interfaces supply output (V_INT)

The **V_INT** output pin of the SARA-R4 series modules is generated by the module internal power management circuitry. The typical operating voltage is 1.8 V, whereas the current capability is specified in the SARA-R4 series Data Sheet [1]. The **V_INT** voltage domain can be used in place of an external discrete regulator as a reference voltage rail for external components.

1.6 System function interfaces

1.6.1 Module power-on

When the SARA-R4 series modules are in the not-powered mode (i.e. the **VCC** module supply is not applied), they can be switched on as follows:

- Rising edge on the **VCC** input pins to a valid voltage level and then the **PWR_ON** input pin is held low for a valid time. After the module power on event, the **PWR_ON** pin can be released.

When the SARA-R4 series modules are in the power-off mode (i.e. switched off with a valid **VCC** supply applied), they can be switched on as follows:

- Low pulse on the **PWR_ON** pin for a valid time period

The **PWR_ON** input pin is equipped with an internal active pull-up resistor. Detailed electrical characteristics with voltages and timings are described in SARA-R4 series Data Sheet [1].

Figure 4 shows the module switch-on sequence from the not-powered mode, describing the following phases:

- The external power supply is applied to the **VCC** module pins
- The **PWR_ON** pin is held low for a valid time
- All the generic digital pins of the module are tri-stated until the switch-on of their supply source (**V_INT**).
- The internal reset signal is held low: the baseband core and all the digital pins are held in the reset state.
- When the internal reset signal is released, any digital pin is set in a proper sequence from the reset state to the default operational configured state. The duration of this pins' configuration phase differs within generic digital interfaces and the USB interface due to host / device enumeration timings (see section 1.9.2).
- The module is fully ready to operate after all interfaces are configured.

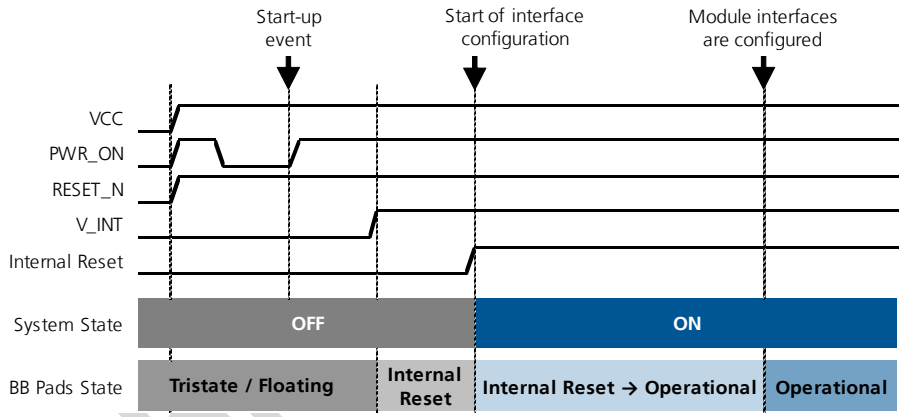

Figure 4: SARA-R4 series switch-on sequence description

The Internal Reset signal is not available on a module pin, but the host application can monitor the **V_INT** pin to sense the start of the SARA-R4 series module switch-on sequence.

Before the switch-on of the generic digital interface supply source (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the module.

Before the SARA-R4 series module is fully ready to operate, the host application processor should not send any AT command over the AT communication interfaces (USB, UART) of the module.

1.6.2 Module power-off

SARA-R4 series can be properly switched off by:

- AT+CPWROFF command (see u-blox SARA-R404M AT Commands Manual [1]). The current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.
- Low pulse on the **PWR_ON** pin for a valid time period (see SARA-R4 series Data Sheet [1]).

An abrupt under-voltage shutdown occurs on SARA-R4 series modules when the **VCC** module supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform the proper network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during SARA-R4 series modules normal operations.

An abrupt hardware shutdown occurs on SARA-R4 series modules when a low level is applied on **RESET_N** pin. In this case, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

☞ It is highly recommended to avoid an abrupt hardware shutdown of the module by forcing a low level on the **RESET_N** input pin during module normal operation: the **RESET_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not reply to a specific AT command after a time period longer than the one defined in the u-blox SARA-R404M AT Commands Manual [1].

An over-temperature or an under-temperature shutdown occurs on SARA-R4 series modules when the temperature measured within the cellular module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details see section 1.12.9 and u-blox SARA-R404M AT Commands Manual [1], +USTS AT command.

Figure 5 describes the SARA-R4 series modules switch-off sequence started SARA-R4 by means of the AT+CPWROFF command, allowing storage of current parameter settings in the module's non-volatile memory and a proper network detach, with the following phases:

- When the +CPWROFF AT command is sent, the module starts the switch-off routine.
- The module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch on event does not occur (e.g. applying a proper low level to the **PWR_ON** input pin), and enters not-powered mode if the supply is removed from the **VCC** pins.

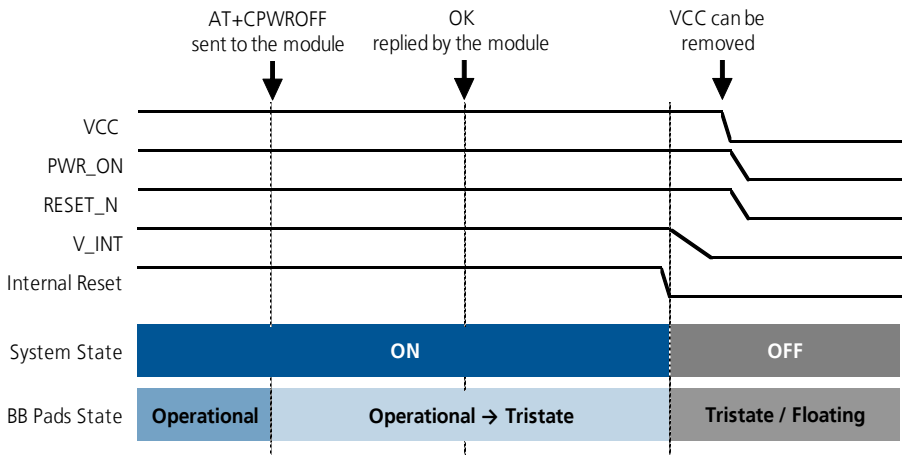

Figure 5: SARA-R4 series switch-off sequence by means of AT+CPWROFF command

The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the end of the switch-off sequence.

The duration of each phase in the SARA-R4 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

Figure 6 describes the SARA-R4 series modules switch-off sequence started by means of the **PWR_ON** input pin, allowing storage of current parameter settings in the module's non-volatile memory and a proper network detach, with the following phases:

- A low pulse with appropriate time duration (see SARA-R4 series Data Sheet [1]) is applied at the **PWR_ON** input pin.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in power-off mode as long as a switch on event does not occur (e.g. applying a proper low level to the **PWR_ON** input), and enters not-powered mode if the supply is removed from the **VCC** pins.

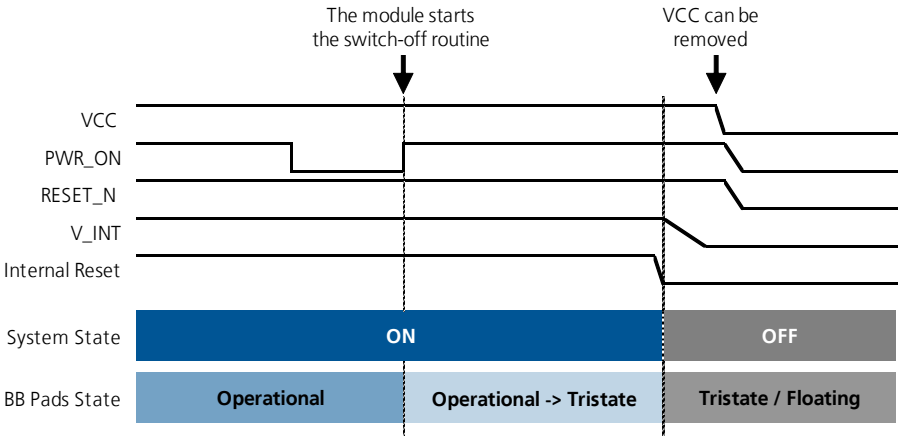

Figure 6: SARA-R4 series switch-off sequence by means of PWR_ON pin

☞ The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the end of the switch-off sequence.

☞ The duration of each phase in the SARA-R4 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

SARA-R4 series modules can be properly reset (rebooted) by:

- AT+CFUN command (see u-blox SARA-R404M AT Commands Manual [1]).

In the case listed above an "internal" or "software" reset of the module is executed: the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

An abrupt hardware shutdown occurs on SARA-R4 series modules when a low level is applied on **RESET_N** input pin. In this case, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed. Then, the module remains in power-off mode as long as a switch on event does not occur applying a proper low level to the **PWR_ON** input.

☞ It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET_N** input during modules normal operation: the **RESET_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the u-blox SARA-R404M AT Commands Manual [1].

The **RESET_N** input pin is equipped with an internal pull-up to the **V_INT** supply. For more electrical characteristics details see SARA-R4 series Data Sheet [1].

1.7 Antenna interface

1.7.1 Antenna RF interface (ANT)

SARA-R4 series modules provide an RF interface for connecting the external antenna. The **ANT** pin represents the primary RF input/output for transmission and reception of LTE RF signals.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the primary Tx / Rx antenna through a 50 Ω transmission line to allow proper RF transmission and reception.

1.7.1.1 Antenna RF interfaces requirements

Table 7 summarizes the requirements for the antenna RF interface. See section 2.4.1 for suggestions to properly design antennas circuits compliant with these requirements.

The antenna circuits affect the RF compliance of the device integrating SARA-R4 series modules with applicable required certification schemes (for more details see section 4). Compliance is guaranteed if the antenna RF interface requirements summarized in Table 7 are fulfilled.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** port.
Frequency Range	See the SARA-R4 series Data Sheet [1]	The required frequency range of the antenna connected to **ANT** port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum Gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT** port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info see sections 4.2.2 and/or 0.
Input Power	> 24 dBm (> 0.25 W)	The antenna connected to the **ANT** port must support with adequate margin the maximum power transmitted by the modules.

Table 7: Summary of Tx/Rx antenna RF interface requirements

1.7.2 Antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the u-blox SARA-R404M AT Commands Manual [1] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics see the SARA-R4 series Data Sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.2 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM interface

SARA-R4 series modules provide high-speed SIM/ME interface including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported. Activation and deactivation with automatic voltage switch from 1.8 V to 3 V are implemented, according to ISO-IEC 7816-3 specifications. The **VSIM** supply output provides internal short circuit protection to limit start-up current and protect the SIM to short circuits.

The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM card or chip.

1.8.2 SIM detection interface (SIM_DET)

The **SIM_DET** pin is configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin is configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **SIM_DET** input pin is recognized as SIM card not present
- High logic level at **SIM_DET** input pin is recognized as SIM card present

For more details see the u-blox SARA-R404M AT Commands Manual [1]).

1.9 Data communication interfaces

SARA-R4 series modules provide the following serial communication interface:

- UART interface: Universal Asynchronous Receiver/Transmitter serial interface available for the communication with a host application processor (AT commands, data communication, FW update by means of FOAT) and for diagnostic. (see section 1.9.1)
- USB interface: Universal Serial Bus 2.0 compliant interface available for the communication with a host application processor (AT commands, data communication, FW update by means of the FOAT feature), for FW update by means of the u-blox EasyFlash tool and for diagnostic. (see section 1.9.2)
- DDC interface: I^2C bus compatible interface available for the communication with u-blox GNSS positioning chips or modules and with external I^2C devices (see section 1.9.3)

1.9.1 UART interface

1.9.1.1 UART features

The UART interface is a 9-wire 1.8 V unbalanced asynchronous serial interface available on all the SARA-R4 series modules, supporting:

- AT command mode[1]
- Data mode and Online command mode1
- Multiplexer protocol functionality
- FW upgrades by means of the FOAT feature (see 1.12.8)
- Trace log capture (diagnostic purpose)

UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation [5], with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state (for detailed electrical characteristics see SARA-R4 series Data Sheet [1]), providing:

- data lines (**RXD** as output, **TXD** as input),
- hardware flow control lines (**CTS** as output, **RTS** as input),
- modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output).

SARA-R4 series modules are designed to operate as cellular modems, i.e. as the data circuit-terminating equipment (DCE) according to the ITU-T V.24 Recommendation [5]. A host application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ UART signal names of the cellular modules conform to the ITU-T V.24 Recommendation [5]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

SARA-R4 series modules' UART interface is by default configured in AT command mode: the module waits for AT command instructions and interprets all the characters received as commands to execute. All the functionalities supported by SARA-R4 series modules can be in general set and configured by AT commands:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7], 3GPP TS 27.010 [8]
- u-blox AT commands (for the complete list and syntax see the u-blox SARA-R404M AT Commands Manual [1])

[1] For the definition of the interface data mode, command mode and online command mode see the u-blox SARA-R404M AT Commands Manual [1]

Flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see u-blox SARA-R404M AT Commands Manual [1], &K, \Q AT commands): hardware flow control (over the **RTS** / **CTS** lines), software flow control (XON/XOFF), or none flow control.

☞ Hardware flow control is enabled by default. The autobauding is not supported

The following baud rates can be configured by AT command (see u-blox SARA-R404M AT Commands Manual [1]):

- 115200 b/s, default value

The following frame formats can be configured by AT command (see u-blox SARA-R404M AT Commands Manual [1]):

- 8N1 (8 data bits, No parity, 1 stop bit), default frame configuration with fixed baud rate, see Figure 7

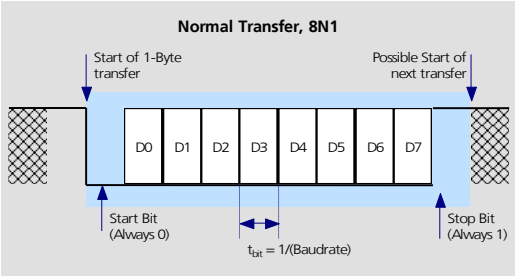

Figure 7: Description of UART 8N1 frame format (8 data bits, no parity, 1 stop bit)

	2
	2
	•

1.9.1.2 UART signals behavior

At the module switch-on, before the UART interface initialization (as described in the power-on sequence reported in Figure 4), each pin is first tri-stated and then is set to its relative internal reset state[4]. At the end of the boot sequence, the UART interface is initialized, the module is by default in active-mode, and the UART interface is enabled as AT commands interface.

The configuration and the behavior of the UART signals after the boot sequence are described below. See section 1.4 for definition and description of module operating modes referred to in this section.

RXD signal behavior

The module data output line (**RXD**) is set by default to the OFF state (high level) at UART initialization. The module holds **RXD** in the OFF state until the module transmits some data.

[2] For the definition of the interface data mode, command mode and online command mode see the u-blox SARA-R404M AT Commands Manual [1]
[3] Not supported by "02" product versions
[4] See the pin description table in the SARA-R4 series Data Sheet [1]

TXD signal behavior

The module data input line (**TXD**) is set by default to the OFF state (high level) at UART initialization. The **TXD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TXD** input.

CTS signal behavior

The module hardware flow control output (**CTS** line) is set to the ON state (low level) at UART initialization.

If the hardware flow control is enabled, as it is by default, the **CTS** line indicates when the UART interface is enabled (data can be received): the module drives the **CTS** line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE over the UART.

☞ If hardware flow control is enabled, then when the **CTS** line is OFF it does not necessarily mean that the module is in low power idle-mode, but only that the UART is not enabled, as the module could be forced to stay in active-mode for other activities, e.g. related to the network or related to other interfaces.

The **CTS** hardware flow control setting can be changed by AT commands (for more details, see the u-blox SARA-R404M AT Commands Manual [1], AT&K, AT\Q AT commands).

☞ When the power saving configuration is enabled by AT+UPSV command and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in low power idle-mode will not be a valid communication character.

RTS signal behavior

The hardware flow control input (**RTS** line) is set by default to the OFF state (high level) at UART initialization. The module then holds the **RTS** line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **RTS** input.

If the HW flow control is enabled, as it is by default, the module monitors the **RTS** line to detect permission from the DTE to send data to the DTE itself. If the **RTS** line is set to the OFF state, any on-going data transmission from the module is interrupted until the **RTS** line changes to the ON state.

The module behavior according to the **RTS** hardware flow control status can be configured by AT commands (for more details, see the u-blox SARA-R404M AT Commands Manual [1], AT&K, AT\Q, AT+IFC AT commands).

If AT+UPSV=2 is set and HW flow control is disabled, the module monitors the **RTS** line to manage the power saving configuration (for more details, see u-blox SARA-R404M AT Commands Manual [1], AT+UPSV):

- When an OFF-to-ON transition occurs on the **RTS** input, the UART is enabled and the module is forced to active-mode. After ~20 ms, the switch is completed and data can be received without loss. The module cannot enter low power idle-mode and the UART is enabled as long as the **RTS** is in the ON state
- If the **RTS** input line is set to the OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters low power idle-mode whenever possible

1.9.2 USB interface

1.9.2.1 USB features

SARA-R4 series modules include a High-Speed USB 2.0 compliant interface with 480 Mb/s maximum data rate, representing the main interface for transferring high speed data with a host application processor, supporting:

- AT command mode[6]
- Data mode and Online command mode6
- FW upgrades by means of the FOAT feature (see 1.12.8 and u-blox SARA-R404M AT Commands Manual [1])

[5] See the u-blox SARA-R404M AT Commands Manual [1] for the definition of the interface data mode, command mode and online command mode.

[6] For the definition of the interface data mode, command mode and online command mode see the u-blox SARA-R404M AT Commands Manual [1]

- FW upgrades by means of the u-blox EasyFlash tool
- Trace log capture (diagnostic purpose)

The module itself acts as a USB device and can be connected to a USB host such as a Personal Computer or an embedded application microprocessor equipped with compatible drivers.

The **USB_D+/USB_D-** lines carry USB serial bus data and signaling according to the Universal Serial Bus Revision 2.0 specification [4], while the **VUSB_DET** input pin senses the VBUS USB supply presence (nominally 5 V at the source) to detect the host connection and enable the interface.

The USB interface of the module is enabled only if a valid voltage is detected by the **VUSB_DET** input (see the SARA-R4 series Data Sheet [1]). Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs few microamperes.

The USB interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7]
- u-blox AT commands (for the complete list and syntax see u-blox SARA-R404M AT Commands Manual [1])

The USB interface of SARA-R4 series modules can provide the following USB functions:

- AT commands and data communication
- Diagnostic log

The USB profile of SARA-R4 series modules identifies itself by the following VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor according to the USB 2.0 specifications [4].

- VID = 0x05C6
- PID = 0x90B2

1.9.2.2 USB in Windows

USB drivers are provided for Windows operating system platforms and should be properly installed / enabled by following the step-by-step instructions available in the EVK-R2xx User Guide [2] or in the Windows Embedded OS USB Driver Installation Application Note [3].

USB drivers are available for the following operating system platforms:

- Windows 7
- Windows 8
- Windows 8.1
- Windows 10
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Compact 2013

The module firmware can be upgraded over the USB interface by means of the FOAT feature or using the u-blox EasyFlash tool.

1.9.2.3 USB in Linux/Android

It is not required to install a specific driver for each Linux-based or Android-based operating system (OS) to use the module USB interface, which is compatible with standard Linux/Android USB kernel drivers.

1.9.3 DDC (I^2C) interface

☞ The I^2C interface is not supported by "00" product version.

1.10 General Purpose Input/Output

SARA-R4 series modules include six pins (**GPIO1**-**GPIO5**, **SIM_DET**) which can be configured as General Purpose Input/Output or to provide custom functions via u-blox AT commands (for more details see the u-blox SARA-R404M AT Commands Manual [1], +UGPIOC, +UGPIOR, +UGPIOW AT commands), as summarized in Table 8.

Function	Description	Default GPIO	Configurable GPIOs
Network status indication	Network status: registered home network, registered roaming, data transmission, no service	--	GPIO1-GPIO4
SIM card detection[7]	External SIM card physical presence detection	GPIO5	--
General purpose input	Input to sense high or low digital level	--	GPIO1-GPIO5
General purpose output	Output to set the high or the low digital level	--	GPIO1-GPIO5
Pin disabled	Tri-state with an internal active pull-down enabled	GPIO1-GPIO5	GPIO1-GPIO5

Table 8: SARA-R4 series GPIO custom functions configuration

1.11 Reserved pins (RSVD)

SARA-R4 series modules have pins reserved for future use, marked as **RSVD**: they can all be left unconnected on the application board.

1.12 System features

1.12.1 Network indication

GPIOs can be configured by the AT command to indicate network status (for further details see section 1.10 and the u-blox SARA-R404M AT Commands Manual [1]):

- No service (no network coverage or not registered)
- Registered to the home network
- Registered to the visitor network (roaming)
- Data call enabled (RF data transmission / reception)

1.12.2 Antenna supervisor

The antenna detection function provided by the **ANT_DET** pin is based on an ADC measurement as optional feature that can be implemented if the application requires it. The antenna supervisor is forced by the +UANTR AT command (see the u-blox SARA-R404M AT Commands Manual [1] for more details).

The requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 1.7.2 for detailed antenna detection interface functional description and see section 2.4.2 for detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.12.3 Dual stack IPv4/IPv6

SARA-R4 series support both Internet Protocol version 4 and Internet Protocol version 6 in parallel.

For more details about dual stack IPv4/IPv6 see the u-blox SARA-R404M AT Commands Manual [1].

[7] Not supported by "00" product version

1.12.4 TCP/IP and UDP/IP

SARA-R4 series modules provide embedded TCP/IP and UDP/IP protocol stack: a PDP context can be configured established and handled via the data connection management packet switched data commands.

SARA-R4 series modules provide Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via serial interfaces (USB, UART). In Direct Link mode, data sent to the serial interface from an external application processor is forwarded to the network and vice-versa.

For more details about embedded TCP/IP and UDP/IP functionalities see the u-blox SARA-R404M AT Commands Manual [1].

1.12.5 FTP

SARA-R4 series provide embedded File Transfer Protocol (FTP) services. Files are read and stored in the local file system of the module.

FTP files can also be transferred using FTP Direct Link:

- **FTP download**: data coming from the FTP server is forwarded to the host processor via USB / UART serial interfaces (for FTP without Direct Link mode the data is always stored in the module's Flash File System)
- **FTP upload**: data coming from the host processor via USB / UART serial interface is forwarded to the FTP server (for FTP without Direct Link mode the data is read from the module's Flash File System)

When Direct Link is used for a FTP file transfer, only the file content pass through USB / UART serial interface, whereas all the FTP commands handling is managed internally by the FTP application.

For more details about embedded FTP functionalities see u-blox SARA-R404M AT Commands Manual [1].

1.12.6 HTTP

SARA-R4 series modules provide the embedded Hyper-Text Transfer Protocol (HTTP) services via AT commands for sending requests to a remote HTTP server, receiving the server response and transparently storing it in the module's Flash File System (FFS).

For more details about embedded HTTP functionalities see the u-blox SARA-R404M AT Commands Manual [1].

1.12.7 SSL SARA-R4 series modules support the Secure Sockets Layer (SSL) with certificate key sizes up to 4096 bits to provide security over the FTP and HTTP protocols.

The SSL support provides different connection security aspects:

- Server authentication: use of the server certificate verification against a specific trusted certificate or a trusted certificates list
- Client authentication: use of the client certificate and the corresponding private key
- Data security and integrity: data encryption and Hash Message Authentication Code (HMAC) generation

The security aspects used during a connection depend on the SSL configuration and features supported.

For a complete list of supported configurations and settings see the u-blox SARA-R404M AT Commands Manual [1].

1.12.8 Firmware update Over AT (FOAT)

This feature allows upgrading the module firmware over USB interface, using AT commands.

- The +FWINSTALL AT command triggers a reboot followed by the upgrade procedure at specified a baud rate
- A special boot loader on the module performs firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader

detects a fault at the next wake-up, and restarts the firmware download from the Xmodem-1k handshake. After completing the upgrade, the module is reset again and wakes-up in normal boot

For more details about Firmware update Over AT procedure see the the u-blox SARA-R404M AT Commands Manual [1], +UFWUPD AT command.

1.12.9 Power saving

The power saving configuration is by default disabled, but it can be enabled using the AT+UPSV command (for the complete description of the AT+UPSV command, see the u-blox SARA-R404M AT Commands Manual [1]).

When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption (see section 1.5.1.3 and SARA-R4 series Data Sheet [1]).For the definition and the description of SARA-R4 series modules operating modes, including the events forcing transitions between the different operating modes, see the section 1.4.

2 Design-in

2.1 Overview

For an optimal integration of SARA-R4 series modules in the final application board follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the relative interface, however a number of points require high attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT** and **ANT_DET** pins.
   Antenna circuit directly affects the RF compliance of the device integrating a SARA-R4 series module with applicable certification schemes. Follow the suggestions provided in the relative section 2.4 for schematic and layout design.
2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a SARA-R4 series module with applicable required certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in the relative section 2.2.1 for schematic and layout design.
3. USB interface: **USB_D+**, **USB_D-** and **VUSB_DET** pins.
   Accurate design is required to guarantee USB 2.0 high-speed interface functionality. Carefully follow the suggestions provided in the relative section 2.6.2 for schematic and layout design.
4. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins.
   Accurate design is required to guarantee SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in the relative section 2.5 for schematic and layout design.
5. System functions: **RESET_N** , **PWR_ON** pins.
   Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in the relative section 2.3 for schematic and layout design.
6. Other digital interfaces: UART, I^2C, GPIOs and Reserved pins.
   Accurate design is required to guarantee proper functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6.1, 2.6.2, 2.6.3, 2.7 and 2.8 for schematic and layout design.
7. Other supplies: **V_INT** generic digital interfaces supply.
   Accurate design is required to guarantee proper functionality. Follow the suggestions provided in the corresponding section 2.2.2 for schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins have to be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-R4 series modules must be sourced through the **VCC** pins with a proper DC power supply that should meet the following prerequisites to comply with the modules' **VCC** requirements summarized in Table 6.

The proper DC power supply can be selected according to the application requirements (see Figure 8) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

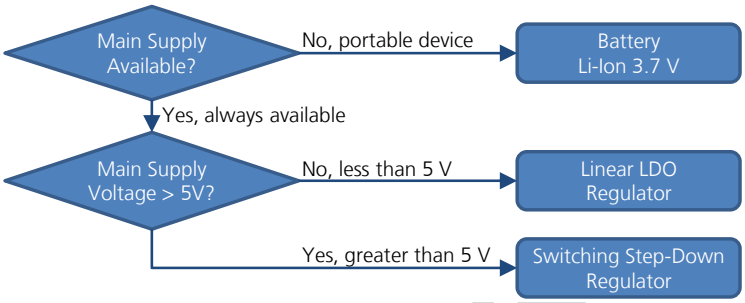

Figure 8: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of SARA-R4 series. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See section 2.2.1.2 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See section 2.2.1.3 for specific design-in.

If SARA-R4 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.5, 2.2.1.7 and 2.2.1.8 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit which is not included in the modules. The charger circuit has to be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements: a DC/DC switching charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is

the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a proper charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.7 and 2.2.1.8 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected taking into account the maximum current specified in SARA-R4 series Data Sheet [1] during connected-mode, considering that primary cells might have weak power capability. See section 2.2.1.5 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The selected regulator or battery must be able to support with adequate margin the highest averaged current consumption value specified in the SARA-R4 series Data Sheet [1].

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 6.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occuring during transmissions at the maximum power, as specified in the SARA-R4 series Data Sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications it is recommended to select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile and therefore negatively impact the LTEmodulation spectrum performance.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected-mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the idle/active-modes to connected-mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 9 and Table 9 show an example of a high reliability power supply circuit, where the module **VCC** input is supplied by a step-down switching regulator capable of delivering maximum current with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

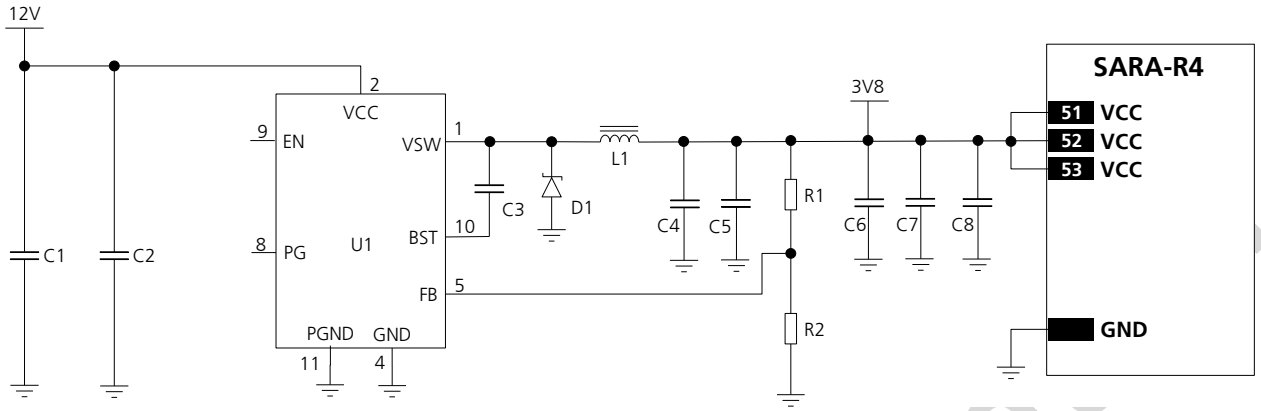

Figure 9: Example of high reliability VCC supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X7R 50 V	Generic manufacturer
C2	10 nF Capacitor Ceramic X7R 16 V	Generic manufacturer
C3	22 nF Capacitor Ceramic X7R 16 V	Generic manufacturer
C4	22 µF Capacitor Ceramic X5R 25 V	Generic manufacturer
C5	22 µF Capacitor Ceramic X5R 25 V	Generic manufacturer
C6	68 pF Capacitor Ceramic C0G 0402 5% 50 V	Generic manufacturer
C7	10 nF Capacitor Ceramic X7R 16 V	Generic manufacturer
C8	100 nF Capacitor Ceramic X7R 16 V	Generic manufacturer
D1	Schottky Diode 30 V 2 A	MBR230LSFT1G - ON Semiconductor
L1	4.7 µH Inductor 20% 2 A	SLF7045T-4R7M2R0-PF - TDK
R1	470 kΩ Resistor 0.1 W	Generic manufacturer
R2	150 kΩ Resistor 0.1 W	Generic manufacturer
U1	Step-Down Regulator 1 A 1 MHz	TS30041 - Semtech

Table 9: Components for high reliability VCC supply application circuit using a step-down regulator

2.2.1.3 Guidelines for VCC supply circuit design using a Low Drop-Out linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low. The linear regulators provide high efficiency when transforming a 5 VDC supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during a transmission at the maximum Tx power, as specified in SARA-R4 series Data Sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 10 and the components listed in Table 10 show an example of a power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the required current, with proper power handling capability.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V for the **VCC**, as in the circuits described in Figure 10 and Table 10). This reduces the power on the linear regulator and improves the thermal design of the circuit.

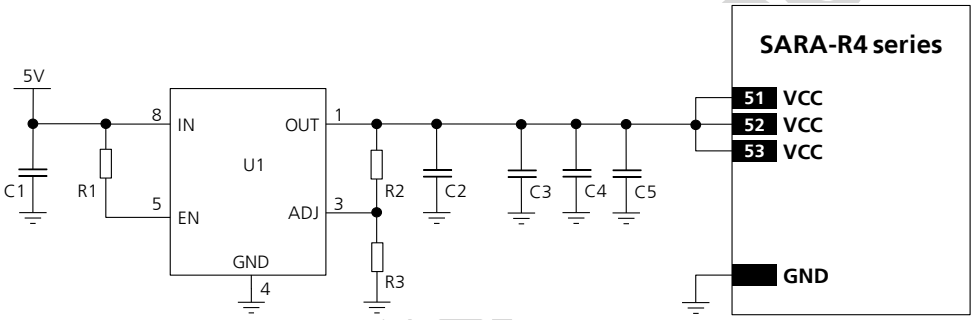

Figure 10: Example of high reliability VCC supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1	1 µF Capacitor Ceramic X5R 6.3 V	Generic manufacturer
C2	4.7 µF Capacitor Ceramic X5R 6.3 V	Generic manufacturer
C3	68 pF Capacitor Ceramic C0G 50 V	Generic manufacturer
C4	10 nF Capacitor Ceramic X7R 16 V	Generic manufacturer
C5	100 nF Capacitor Ceramic X7R 16 V	Generic manufacturer
R1	47 kΩ Resistor 0.1 W	Generic manufacturer
R2	41 kΩ Resistor 0.1 W	Generic manufacturer
R3	10 kΩ Resistor 0.1 W	Generic manufacturer
U1	LDO Linear Regulator 1.0 A	AP7361 – Diodes Incorporated

Table 10: Components for high reliability VCC supply application circuit using an LDO linear regulator

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current occurring during a transmission at maximum Tx power, as specified in SARA-R4 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 6 during transmit bursts.

2.2.1.5 Guidelines for VCC supply circuit design using a primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current consumption occurring during a transmission at maximum Tx power, as specified in SARA-R4 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the max DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 6 during transmit bursts.

2.2.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the power supply lines (connected to the modules' **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated to **VCC** supply. Several pins are designated for **GND** connection. It is recommended to properly connect all of them to supply the module to minimize series resistance losses.

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 68 pF capacitor with Self-Resonant Frequency in the 800/900 MHz range (e.g. Murata GRM1555C1H680J)
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 100 nF capacitor (e.g. Murata GRM155R61C104K) to filter digital logic noise from clocks and data sources

A suitable series ferrite bead can be properly placed on the **VCC** line for additional noise filtering if required by the specific application according to the whole application board design.

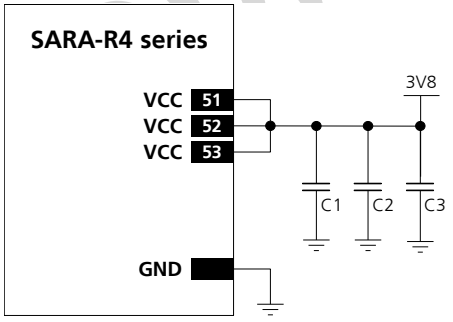

Figure 11: Suggested schematic for the VCC bypass capacitors to reduce ripple / noise on supply voltage profile

Reference	Description	Part Number - Manufacturer
C1	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata

Table 11: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the bypass capacitors described in Figure 11 / Table 11 if the application device integrates an internal antenna.

2.2.1.7 Guidelines for external battery charging circuit

SARA-R4 series modules do not have an on-board charging circuit. Figure 12 provides an example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the Battery Charger IC that, from a USB power source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor
- **Constant voltage**: when the battery voltage reaches the regulated output voltage, the Battery Charger IC starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor or when the charging timer reaches the factory set value

Using a battery pack with an internal NTC resistor, the Battery Charger IC can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The Battery Charger IC, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see the following section 2.2.1.8 for specific design-in).

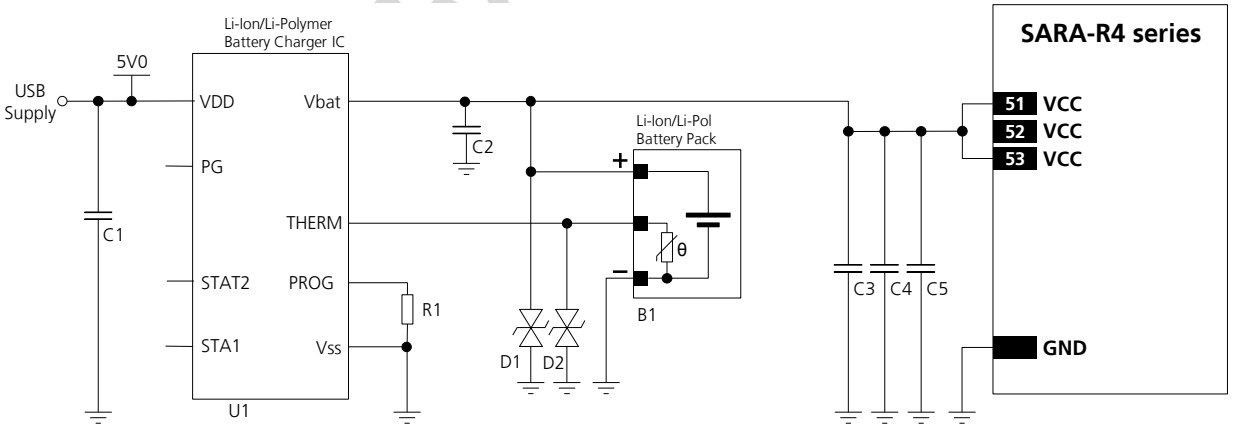

Figure 12: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Generic manufacturer
C1, C2	1 µF Capacitor Ceramic X7R 16 V	Generic manufacturer
C3	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1	10 kΩ Resistor 0.1 W	Generic manufacturer
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC	MCP73833 - Microchip

Table 12: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit

2.2.1.8 Guidelines for external battery charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 13 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system: the power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- High efficiency internal step down converter, compliant with the performances specified in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

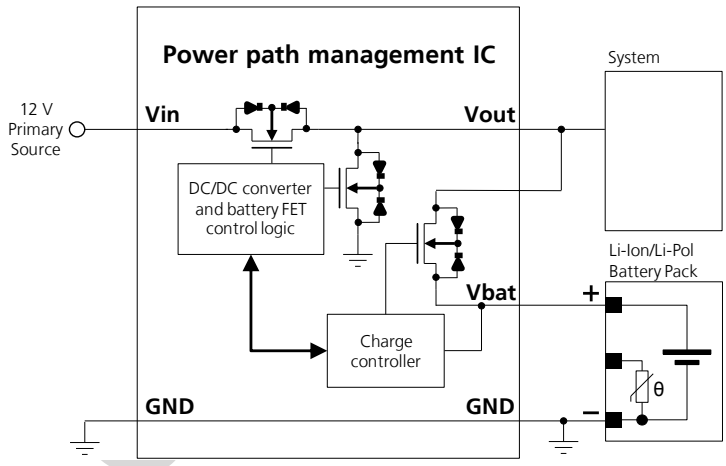

Figure 13: Charger / regulator with integrated power path management circuit block diagram

Figure 14 and the components listed in Table 13 provide an application circuit example where the MPS MP2617 switching charger / regulator with integrated power path management function provides the supply to the cellular module while concurrently and autonomously charging a suitable Li-Ion (or Li-Polymer) battery with proper pulse and DC discharge current capabilities and proper DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617 IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617 IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor

Using a battery pack with an internal NTC resistor, the MP2617 can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: proper resistors or capacitors have to be accordingly connected to the related pins of the IC.

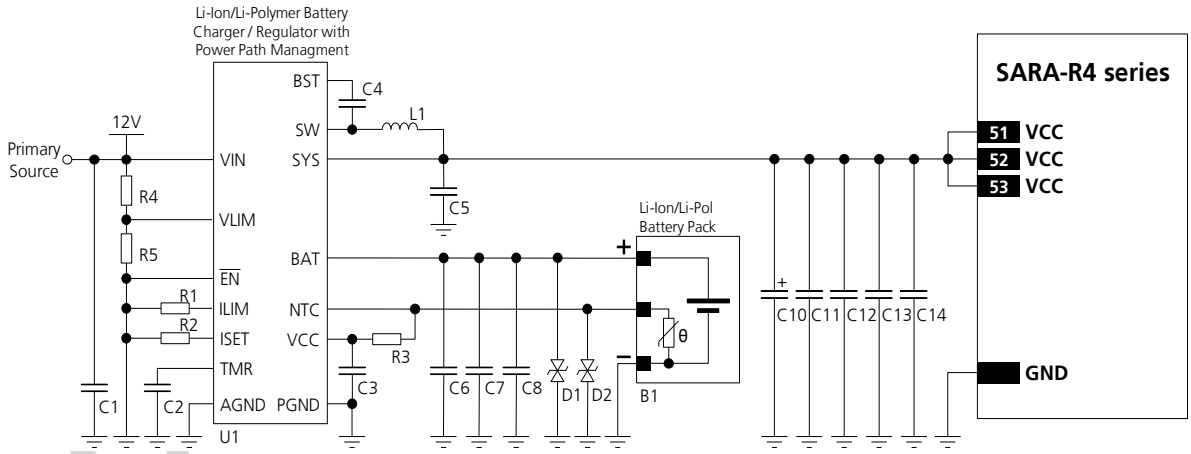

Figure 14: Li-Ion (or Li-Polymer) battery charging and power path management application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC	Various manufacturer
C1, C5, C6	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C7, C13	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C8, C14	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C10	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C12	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R3, R5	10 kΩ Resistor 0402 5% 1/16 W	RC0402JR-0710KL - Yageo Phycomp
R2	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
R4	22 kΩ Resistor 0402 5% 1/16 W	RC0402JR-0722KL - Yageo Phycomp
L1	1.2 µH Inductor 6 A 21 mΩ 20%	7447745012 - Wurth
U1	Li-Ion/Li-Polymer Battery DC/DC Charger / Regulator with integrated Power Path Management function	MP2617 - Monolithic Power Systems (MPS)

Table 13: Suggested components for Li-Ion (or Li-Polymer) battery charging and power path management application circuit

2.2.1.9 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source
- **VCC** connection must be as wide as possible and as short as possible
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing
- Coupling between **VCC** and digital lines, especially USB, must be avoided.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.6 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and module tank capacitor
- The bypass capacitors in the pF range described in Figure 11 and Table 11 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF noise rejection in the band centered on the Self-Resonant Frequency of the pF capacitors. This is highly recommended if the application device integrates an internal antenna
- Since **VCC** input provide the supply to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-R4 series modules in the worst case
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection functionality may be compromised)

2.2.1.10 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source
- It is recommended to implement one layer of the application board as ground plane as wide as possible
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board. Use as many vias as possible to connect the ground planes
- Provide a dense line of vias at the edges of each ground area, in particular along RF and high speed lines
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs
- Good grounding of **GND** pads also ensures thermal heat sink. This is critical during connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating.

2.2.2 Generic digital interfaces supply output (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

SARA-R4 series provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on (as described in sections 1.6.1, 1.6.2)
- Supply voltage translators to connect 1.8 V module generic digital interfaces to 3.0 V devices (e.g. see 2.6.1)
- Enable external voltage regulators providing supply for external devices,

☞ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply (see the SARA-R4 series Data Sheet [1]) as this can cause malfunctions in internal circuitry.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible test point directly connected to the **V_INT** pin.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

SARA-R4 series **PWR_ON** input is equipped with an internal active pull-up resistor; an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 15 and Table 14.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as described in Figure 15.A compatible push-pull output of an application processor can also be used. In any case, take care to set the proper level in all the possible scenarios to avoid an inappropriate module switch on or switch off.

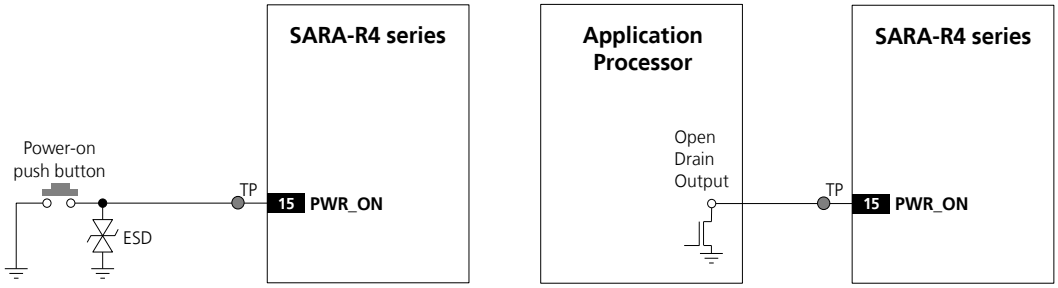

Figure 15: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 14: Example ESD protection component for the PWR_ON application circuit

☞ It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of an accessible test point directly connected to the **PWR_ON** pin.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout since it is the sensitive input available to switch on and switch off the SARA-R4 series modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

SARA-R4 series **RESET_N** is equipped with an internal pull-up; an external pull-up resistor is not required.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to accessible point on the line connected to this pin, as described in Figure 16 and Table 15.

An open drain output is suitable to drive the **RESET_N** input from an application processor, as described in Figure 16. A compatible push-pull output of an application processor can also be used. In any case, take care to set the proper level in all the possible scenarios to avoid an inappropriate module switch off.

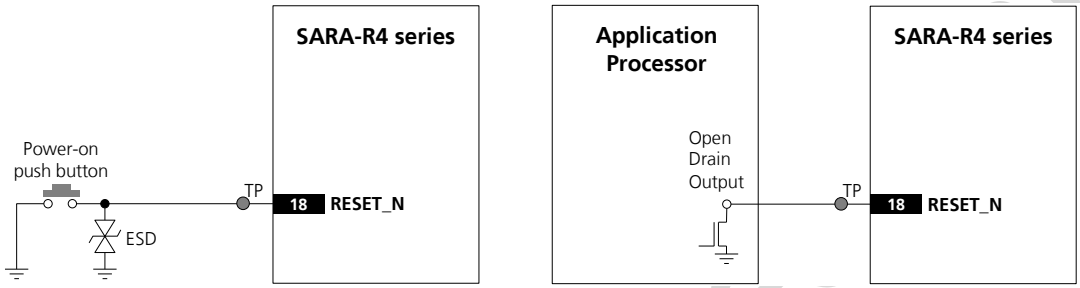

Figure 16: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 15: Example of ESD protection component for the RESET_N application circuits

☞ If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of an accessible test point directly connected to the **RESET_N** pin.

2.3.2.2 Guidelines for RESET_N layout design

The **RESET_N** circuit require careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** pin as short as possible.

2.4 Antenna interface

SARA-R4 series modules provide an RF interface for connecting the external antenna: the **ANT** pin represents the RF input/output for RF signals transmission and reception.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the physical antenna through a 50 Ω transmission line to allow proper transmission / reception of RF signals.

2.4.1 Antenna RF interface (ANT)

2.4.1.1 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antenna from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating SARA-R4 series modules with all the applicable required certification schemes depends on antenna's radiating performance.

LTE antennas are typically available in the types of linear monopole or PCB antennas such as patches or ceramic SMT elements.

- External antennas (e.g. linear monopole)
  - External antennas basically do not imply physical restriction to the design of the PCB where the SARA-R4 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides proper PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. patch-like antennas):
  - Internal integrated antennas imply physical restriction to the design of the PCB:

    Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered.

    As numerical example, the physical restriction to the PCB design can be considered as following:

    Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
  - Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
  - It is recommended to select a custom antenna designed by an antennas' manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry
  - Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to

consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application

In both of cases, selecting external or internal antennas, these recommendations should be observed:

- Select an antenna providing optimal return loss (or V.S.W.R.) figure over all the operating frequencies.
- Select an antenna providing optimal efficiency figure over all the operating frequencies.
- Select an antenna providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States, as reported in the section 4.2.2).

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for ANT pin RF connection design

Proper transition between **ANT** pad and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** pad:

- On a multilayer board, the whole layer stack below the RF connection should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** pad, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 17
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 17

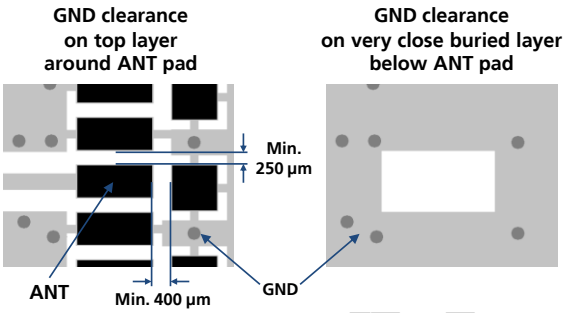

Figure 17: GND keep-out area on top layer around ANT pad and on very close buried layer below ANT pad

Guidelines for RF transmission line design

Any RF transmission line, such as the ones from the **ANT** pad up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 18 and Figure 19 provide two examples of proper 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

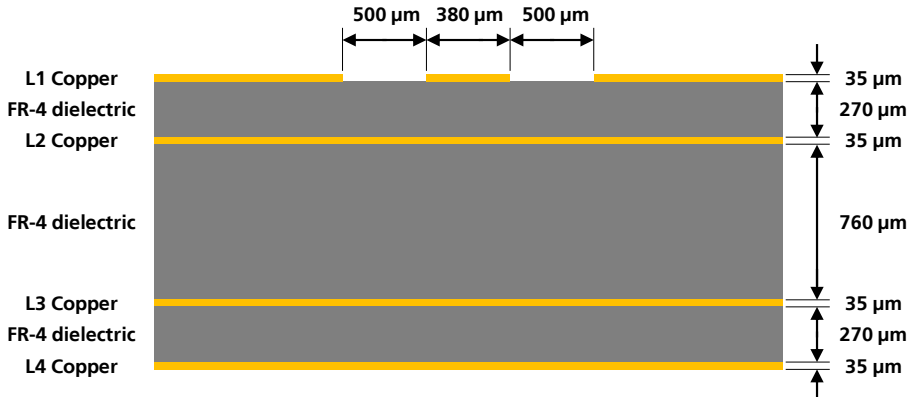

Figure 18: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

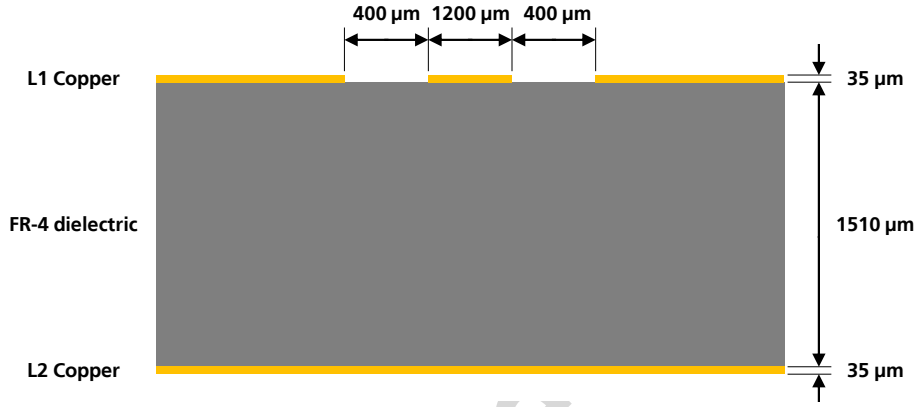

Figure 19: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent (www.agilent.com) or TXLine from Applied Wave Research (www.mwoffice.com), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 18 and Figure 19)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 18, 1510 µm in Figure 19)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 18 and Figure 19)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 18, 400 µm in Figure 19)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission lines design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB,
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission lines, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground,
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND,
- Add GND stitching vias around transmission lines, as described in Figure 20,
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer, as described in Figure 20,
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB),
- Avoid stubs on the transmission lines,
- Avoid signal routing in parallel to transmission lines or crossing the transmission lines on buried metal layer,
- Do not route microstrip lines below discrete component or other mechanics placed on top layer

An example of proper RF circuit design is reported in Figure 20. In this case, the **ANT** pin is directly connected to SMA connectors by means of proper 50 Ω transmission lines, designed with proper layout.

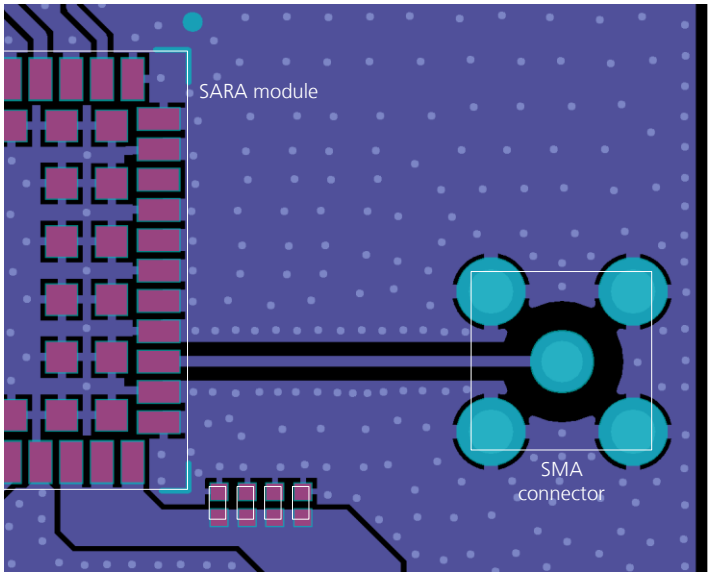

Figure 20: Example of circuit and layout for antenna RF circuits on application board

Guidelines for RF termination design

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination, to match the characteristic impedance of the **ANT** port.

However, real antennas do not have perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antennas mismatch, the RF termination must provide optimal return loss (or V.S.W.R.) figure over all the operating frequencies, as summarized in Table 7.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use suitable a 50 Ω connector providing proper PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts, as shown in Figure 20
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under the RF connector and close to buried vias, to remove stray capacitance and thus keep the RF line 50 Ω, e.g. the active pad of UFL connector needs to have a GND keep-out (i.e. clearance, a void area) at least on first inner layer to reduce parasitic capacitance to ground.

If an integrated antenna is used, the RF terminations are represented by the integrated antenna. The following guidelines should be followed:

- Use an antenna designed by an antenna manufacturer, providing the best possible return loss (or V.S.W.R.).
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. As numerical example,

  Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna matching relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place the antenna within closed metal case.
- Do not place the antenna in close vicinity to end user since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce EMC issues.
- Take care of interaction between co-located RF systems since the LTE transmitted power may interact or disturb the performance of companion systems.

Examples of antennas

Table 16 lists some examples of possible internal on-board surface-mount antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PA.711.A	Warrior II	GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.06.A	Havok	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm

Table 16: Examples of internal surface-mount antennas

Table 17 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part Number	Product Name	Description
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB Antenna with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Taoglas	FXUB66.07.0150C	Maximus	GSM / WCDMA / LTE PCB Antenna with cable and U.FL 698..960 MHz, 1390..1435 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz, 3400..3600 MHz, 4800..6000 MHz 120.2 x 50.4 mm
Taoglas	FXUB70.A.07.C.001		GSM / WCDMA / LTE PCB MIMO Antenna with cables and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 182.2 x 21.2 mm
Ethertronics	5001537	Prestta	GSM / WCDMA / LTE PCB Antenna with cable 704..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 80.0 x 18.0 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB Antenna with cable and U.FL 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm

Table 17: Examples of internal antennas with cable and connector

Table 18 lists some examples of possible external antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE adhesive-mount antenna with cable and SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm
Taoglas	TG.30.8112		GSM / WCDMA / LTE swivel dipole antenna with SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm
Taoglas	MA241.BI.001	Genesis	GSM / WCDMA / LTE MIMO 2in1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2170 MHz, 2400..2700 MHz 205.8 x 58 x 12.4 mm
Laird Tech.	TRA6927M3PW-001		GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount antenna with cable and N-type(F) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Laird Tech.	CMD69273-30NM		GSM / WCDMA / LTE ceiling-mount MIMO antenna with cables & N-type(M) 698..960 MHz, 1710..2700 MHz 43.5 x Ø 218.7 mm
Pulse Electronics	WA700/2700SMA		GSM / WCDMA / LTE clip-mount MIMO antenna with cables and SMA(M) 698..960 MHz,1710..2700 MHz 149 x 127 x 5.1 mm

Table 18: Examples of external antennas

2.4.2 Antenna detection interface (ANT_DET)

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 21 and Table 19 describe the recommended schematic / components for the antenna detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antenna's assembly to achieve primary and secondary antenna detection functionality.

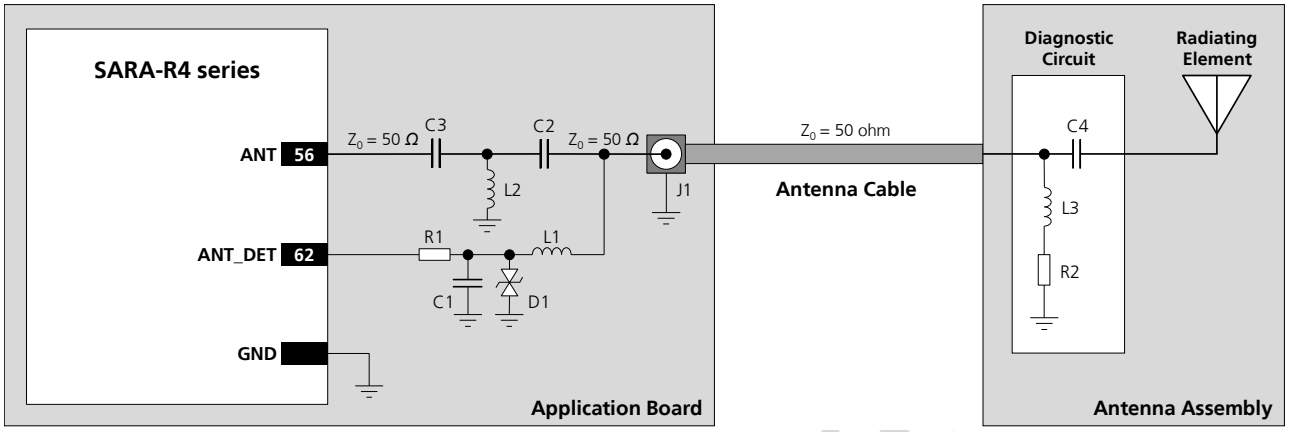

Figure 21: Suggested schematic for antenna detection circuit on application board and diagnostic circuit on antenna assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2,	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1,	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 19: Suggested components for antenna detection circuit on application board and diagnostic circuit on antennas assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 21 and Table 19 are here explained:

- When antenna detection is forced by the +UANTR AT command, the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Resistor on the **ANT_DET** path (R1) is needed for accurate measurements through the +UANTR AT command. It also acts as an ESD protection.
- Additional components (C1 and D1 in Figure 21) are needed at the **ANT_DET** pin as ESD protection.

- Additional high pass filter (C3 and L2 in Figure 21) is provided at the **ANT** pin as ESD immunity improvement for SARA-U260, SARA-U270 and SARA-U280 modules (a series 0 Ω jumper can be mounted for SARA-G340 and SARA-G350 modules instead of the high pass filter, as no further precaution to ESD immunity test is needed).
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 21, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see u-blox SARA-R404M AT Commands Manual [1]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 20.

2.4.2.2 Guidelines for ANT_DET layout design

The recommended layout for the antenna detection circuit to be provided on the application board to achieve the antenna detection functionality, implementing the recommended schematic described in Figure 21 and Table 19, is explained here:

- The ANT pin have to be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT** pins (C2, C3) has to be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin has to be connected to the 50 Ω transmission line by means of a sense line.

- Choke inductor in series at the **ANT_DET** pin (L1) has to be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT_DET** line have to be placed as ESD protection.

2.5 SIM interface

2.5.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE/3G/2G network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 6 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as:

- Case Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case Pin 5 = UICC Contact C4 = AUX1 (Aux.contact) → It must be left not connected
- Case Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to **GND**
- Case Pin 2 = UICC Contact C6 = VPP (Progr. supply) → It can be left not connected
- Case Pin 3 = UICC Contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case Pin 4 = UICC Contact C8 = AUX2 (Aux. contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder has to be connected to the SIM card interface of SARA-R4 series modules as described in Figure 22, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the SIM requirements (27.7 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

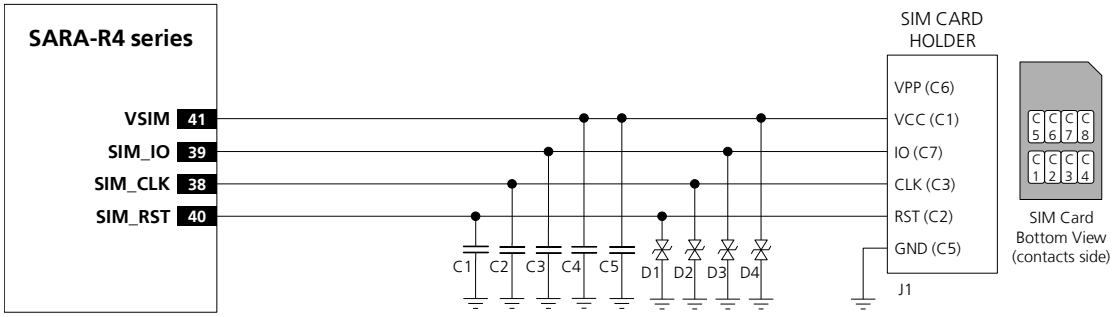

Figure 22: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder, 6 p, without card presence switch	Various manufacturers, as C707 10M006 136 2 - Amphenol

Table 20: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

Guidelines for single SIM chip connection

A solderable SIM chip (M2M UICC Form Factor) has to be connected the SIM card interface of SARA-R4 series modules as described in Figure 23.

Follow these guidelines to connect the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM lines.
- Limit capacitance and series resistance on each SIM signal to match the SIM requirements (27.7 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

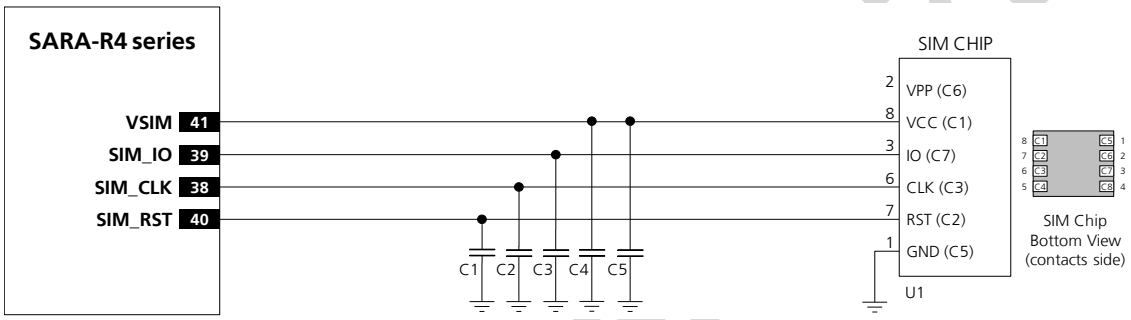

Figure 23: Application circuits for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 21: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** may be critical if the SIM card is placed far away from the SARA-R4 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE receiver channels whose carrier frequency is coincidental with harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 22 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 UART interface

2.6.1.1 Guidelines for UART circuit design

Providing the full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators can be used to provide full RS-232 (9 lines) functionality: e.g. using the Texas Instruments SN74AVC8T245PW for the translation from 1.8 V to 3.3 V, and the Maxim MAX3237E for the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V Application Processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART interface of the module (DCE) should be connected to a 1.8 V DTE, as described in Figure 24.

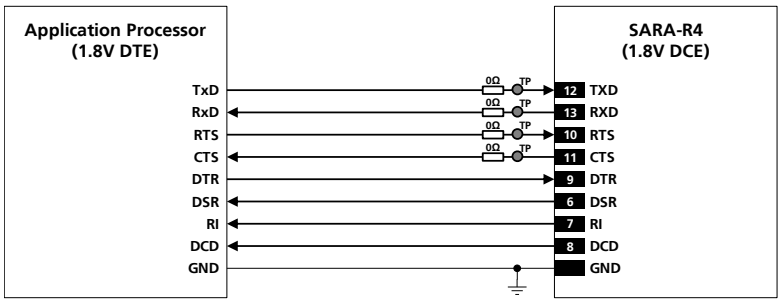

Figure 24: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 25.

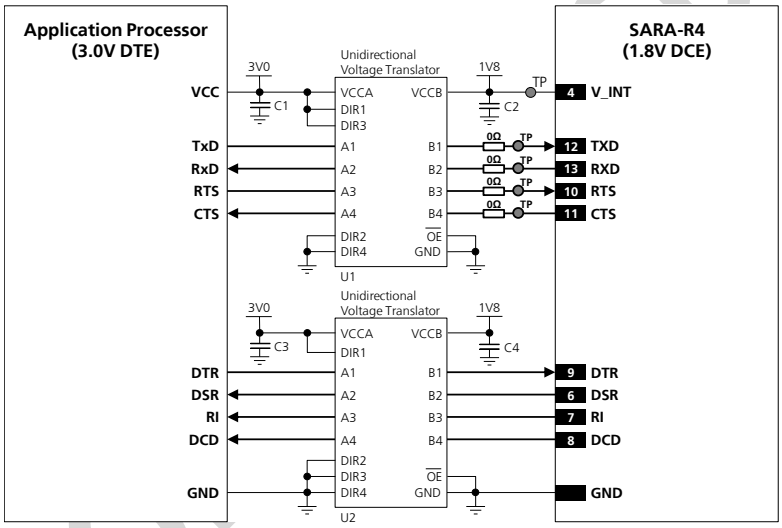

Figure 25: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774[8] - Texas Instruments

Table 22: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

[8] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing the TXD, RXD, RTS, CTS and DTR lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD** and **RI** lines is not required, or the lines are not available:

- Leave **DSR**, **DCD** and **RI** lines of the module floating, with a test-point on **DCD**

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

Figure 26 describes the circuit that should be implemented as if a 1.8 V Application Processor (DTE) is used, given that the DTE will behave properly regardless **DSR** input setting.

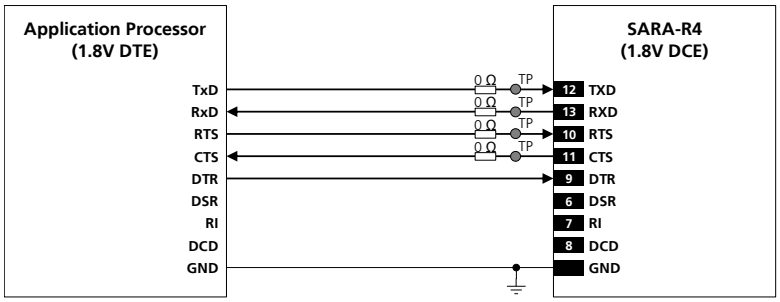

Figure 26: UART interface application circuit with partial V.24 link (6-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 27, given that the DTE will behave properly regardless **DSR** input setting.

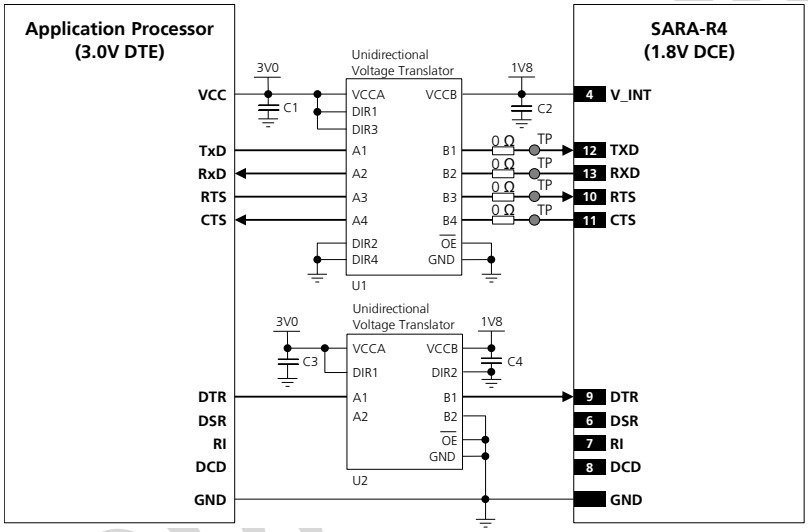

Figure 27: UART interface application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774[9] - Texas Instruments
U2	Unidirectional Voltage Translator	SN74AVC2T2459 - Texas Instruments

Table 23: Component for UART application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

[9] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing the TXD, RXD, RTS and CTS lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required in, or the lines are not available:

- Connect the module **DTR** input to GND using a 0 Ω series resistor, since it may be useful to set **DTR** active if not specifically handled (see u-blox SARA-R404M AT Commands Manual [1], &D, S0, +CSGT, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating, with a test-point on **DCD**

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor is used, the circuit should be implemented as described in Figure 28.

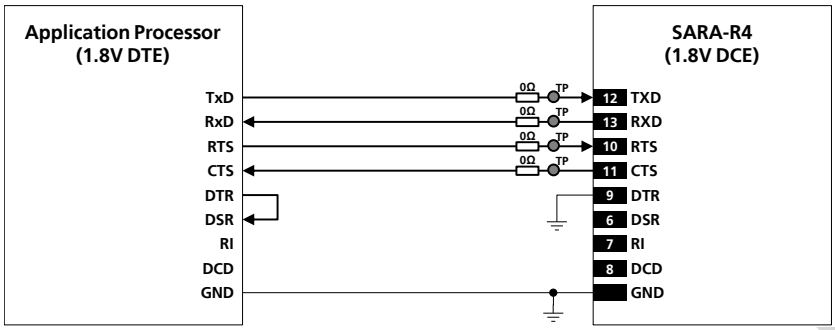

Figure 28: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 29.

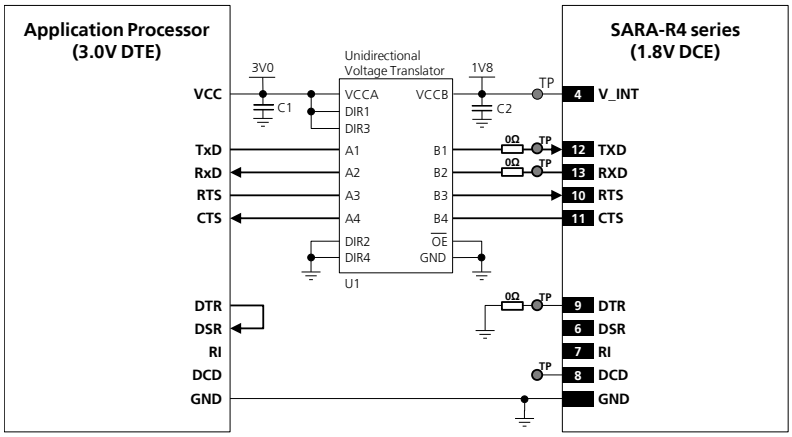

Figure 29: UART interface application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774[10] - Texas Instruments

Table 24: Component for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

[10] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing the TXD and RXD lines only (not using the complete V24 link)

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available, then:

- Connect the module **RTS** input line to GND or to the **CTS** output line of the module: since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, which is the default setting)
- Connect the module **DTR** input line to GND using a 0 Ω series resistor, because it is useful to set **DTR** active if not specifically handled (see u-blox SARA-R404M AT Commands Manual [1], &D, S0, +CSGT, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating, with a test-point on **DCD**

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor (DTE) is used, the circuit that should be implemented as described in Figure 30

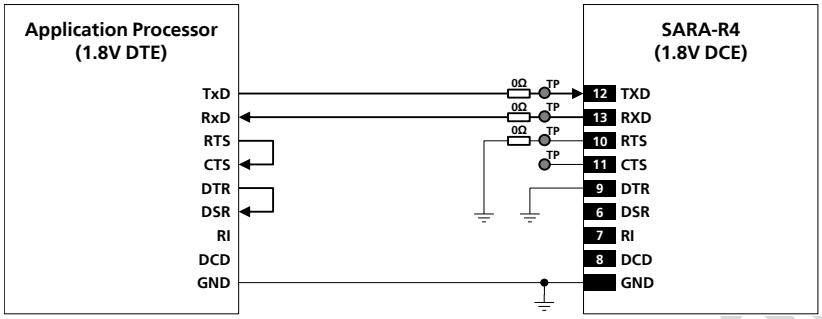

Figure 30: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 31.

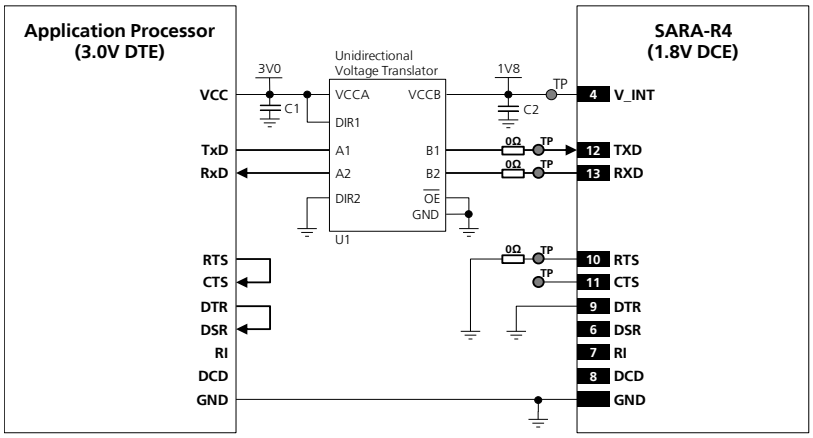

Figure 31: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245[11] - Texas Instruments

Table 25: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

[11] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V Application Processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values. Make sure that any DTE signal connected to the module is tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the Application Processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

☞ If power saving is enabled, the application circuit with the **TXD** and **RXD** lines only is not recommended. During command mode the DTE must send to the module a wake-up character or a dummy "AT" before each command line, but during data mode the wake-up character or the dummy "AT" would affect the data communication.

☞ Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

☞ If the UART interface pins are not used, they can be left unconnected on the application board, but it is recommended providing accessible test points directly connected to the **TXD**, **RXD**, **DTR** and **DCD** pins for diagnostic purpose, in particular providing a 0 Ω series jumper on each line to detach each UART pin of the module from the DTE application processor.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

2.6.2.1 Guidelines for USB circuit design

The **USB_D+** and **USB_D-** lines carry the USB serial data and signaling. The lines are used in single ended mode for full speed signaling handshake, as well as in differential mode for high speed signaling and data transfer.

USB pull-up or pull-down resistors and external series resistors on **USB_D+** and **USB_D-** lines as required by the USB 2.0 specification [4] are part of the module USB pins driver and do not need to be externally provided.

The USB interface of the module is enabled only if a valid voltage is detected by the **VUSB_DET** input (see the SARA-R4 series Data Sheet [1]). Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs few microamperes.

Routing the USB pins to a connector, they will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to accessible point on the line connected to this pin, as described in Figure 32 and Table 26.

The USB pins of the modules can be directly connected to the USB host application processor without additional ESD protections if they are not externally accessible or according to EMC/ESD requirements.

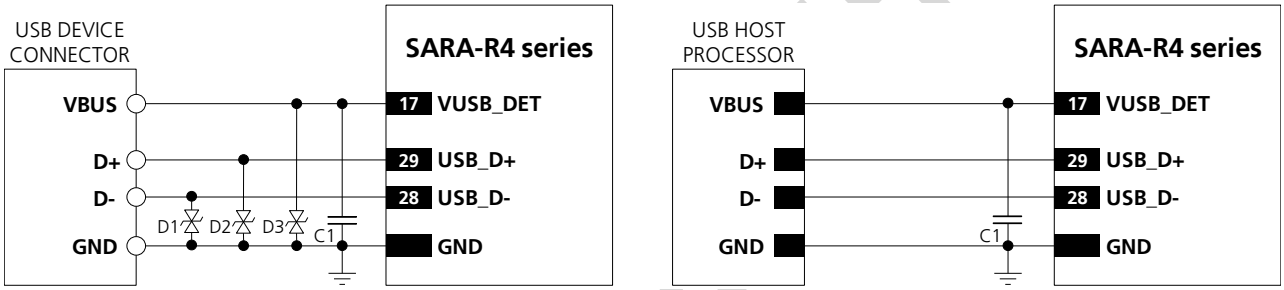

Figure 32: USB Interface application circuits

Reference	Description	Part Number - Manufacturer
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics

Table 26: Component for USB application circuits

☞ If the USB interface pins are not used, they can be left unconnected on the application board, but it is recommended providing accessible test points directly connected to **VUSB_DET**, **USB_D+**, **USB_D-** pins.

2.6.2.2 Guidelines for USB layout design

The **USB_D+** / **USB_D-** lines require accurate layout design to achieve reliable signaling at the high speed data rate (up to 480 Mb/s) supported by the USB serial interface.

The characteristic impedance of the **USB_D+** / **USB_D-** lines is specified by the Universal Serial Bus Revision 2.0 specification [4]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route **USB_D+** / **USB_D-** lines as a differential pair
- Route **USB_D+** / **USB_D-** lines as short as possible
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω
- Consider design rules for **USB_D+** / **USB_D-** similar to RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area

Figure 33 and Figure 34 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

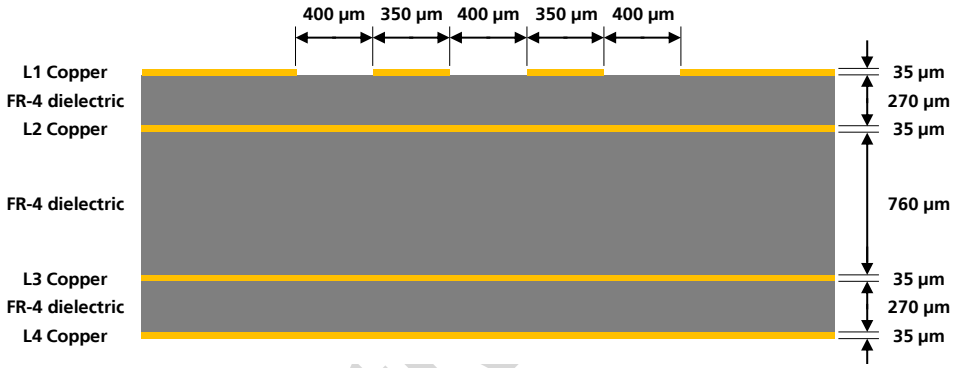

Figure 33: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

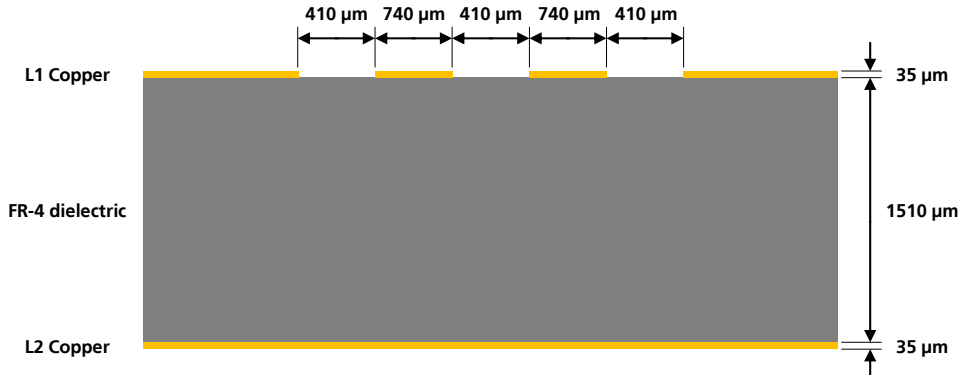

Figure 34: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.6.3 DDC (I²C) interface

2.6.3.1 Guidelines for DDC (I²C) circuit design

Communication with u-blox GNSS receivers over DDC (I²C) is not supported by "00" product versions.

2.7 General Purpose Input/Output

2.7.1.1 Guidelines for GPIO circuit design

A typical usage of SARA-R4 series modules' GPIOs can be the following:

- Network indication provided over **GPIO1** pin (see Figure 35 / Table 27 below)

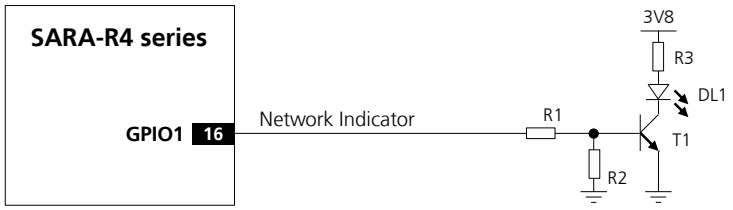

Figure 35: Application circuit for network indication provided over GPIO1

Reference	Description	Part Number - Manufacturer
R1	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	820 Ω Resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED Red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 27: Components for network indication application circuit

Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of SARA-R4 series modules.

Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a proper module boot. If the external signals connected to the module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

If the GPIO pins are not used, they can be left unconnected on the application board.

2.7.1.2 Guidelines for general purpose input/output layout design

The general purpose inputs / outputs pins are generally not critical for layout.

2.8 Reserved pins (RSVD)

SARA-R4 series modules have pins reserved for future use, marked as **RSVD**. All the **RSVD** pins are to be left unconnected.

2.9 Module placement

An optimized placement allows a minimum RF line's length and closer path from DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce Electro-Magnetic Interference that affects the module, analog parts and RF circuits' performance. Implement proper countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Make sure that the module, RF and analog parts / circuits, and high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by Electro-Magnetic Interference, or employ countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Provide enough clearance between the module and any external part.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the SARA-R4 series modules: avoid placing temperature sensitive devices close to the module.

2.10 Module footprint and paste mask

Figure 36 and Table 28 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, implementing the solder mask opening 50 µm larger per side than the corresponding copper pad.

The recommended solder paste thickness is 150 µm, according to application production process requirements.

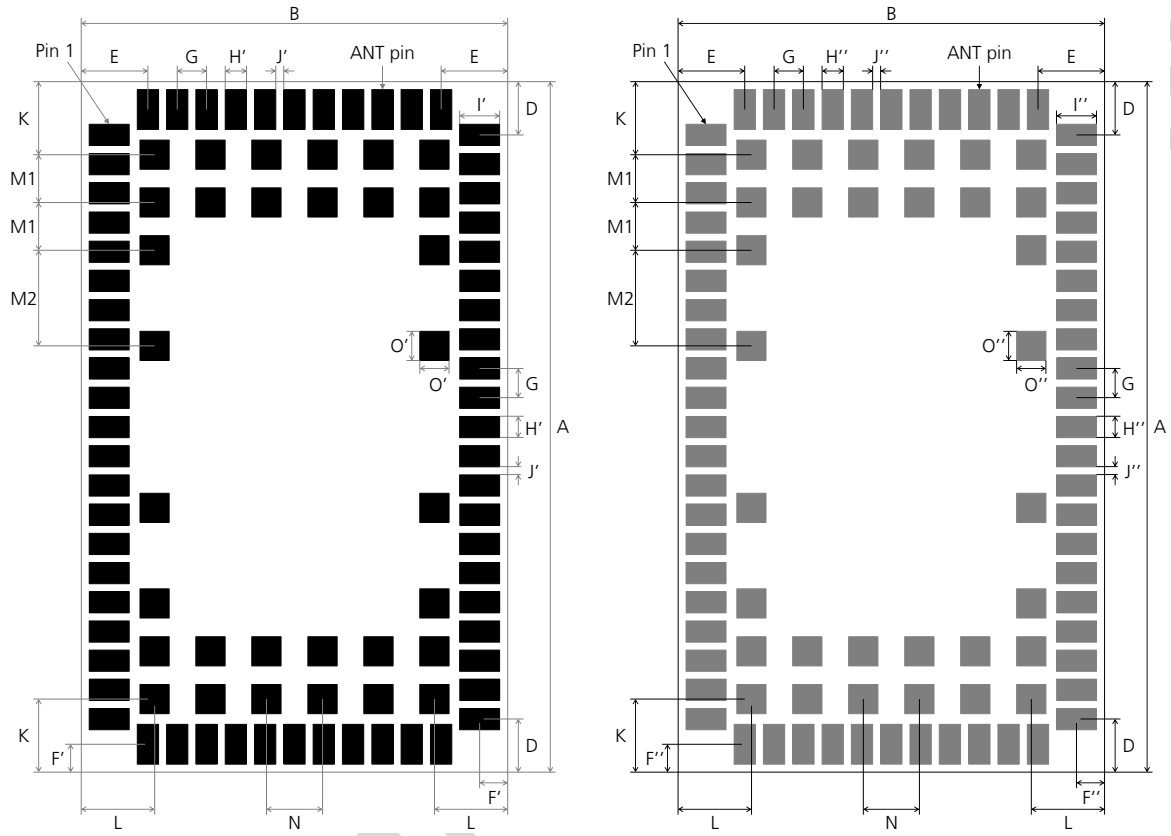

Figure 36: SARA-R4 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	G	1.10 mm	K	2.75 mm
B	16.0 mm	H'	0.80 mm	L	2.75 mm
C	3.00 mm	H''	0.75 mm	M1	1.80 mm
D	2.00 mm	I'	1.50 mm	M2	3.60 mm
E	2.50 mm	I''	1.55 mm	N	2.10 mm
F'	1.05 mm	J'	0.30 mm	O'	1.10 mm
F''	1.00 mm	J''	0.35 mm	O''	1.05 mm

Table 28: SARA-R4 series modules suggested footprint and paste mask dimensions

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.11 Thermal guidelines

☞ The module operating temperature range is specified in SARA-R4 series Data Sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected-mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution for WCDMA, taken from operation on a live network, described in the GSMA TS.09 Battery Life Measurement and Current Consumption Technique [12]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power the SARA-R4 series modules generate thermal power that may exceed 2 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the actual antenna return loss, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

☞ The Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the Module-to-Ambient thermal resistance, will decrease the temperature of the modules' internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with complete thermal via stacked down to main ground layer.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application device.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Further hardware techniques that may be considered to improve the heat dissipation in the application:

- Force ventilation air-flow within mechanical enclosure.
- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads of the SARA-R4 series LGA modules and dissipated over the backside of the application board.

For example, the Module-to-Ambient thermal resistance ($R_{th,M-A}$) is strongly reduced with forced air ventilation and a heat-sink installed on the back of the application board, decreasing the module temperature variation.

Beside the reduction of the Module-to-Ambient thermal resistance implemented by proper application hardware design, the increase of module temperature can be moderated by proper application software implementation:

- Enable power saving configuration using the AT+UPSV command
- Enable module connected-mode for a given time period and then disable it for a time period enough long to properly mitigate temperature increase.

2.12 Schematic for SARA-R4 series module integration

2.12.1 Schematic for SARA-R4 series modules

Figure 37 is an example of a schematic diagram where a SARA-R4 series cellular module "02" product version is integrated into an application board, using all the available interfaces and functions of the module.

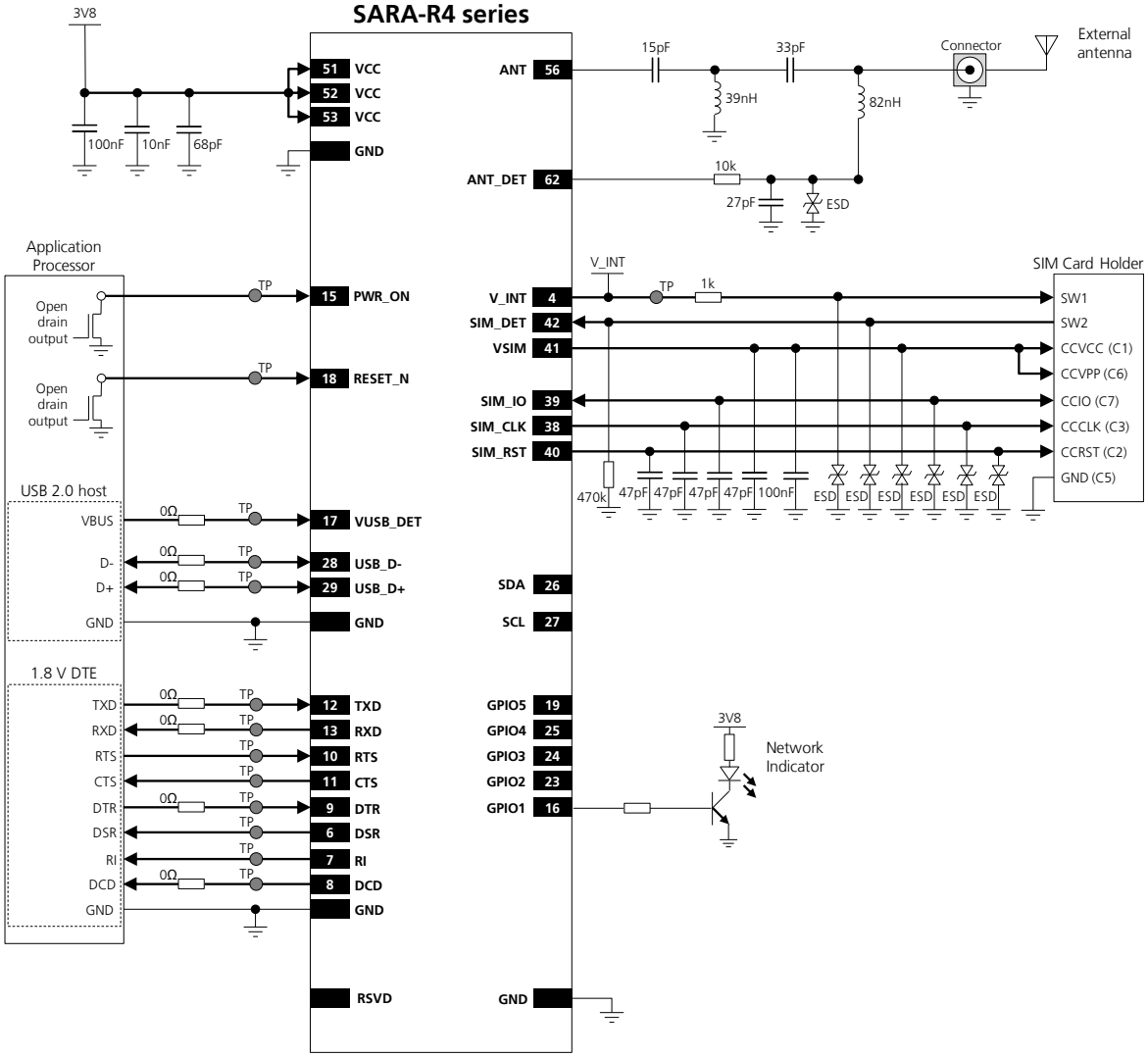

Figure 37: Example of schematic diagram to integrate a SARA-R4 module using all available interfaces

2.13 Design-in checklist

This section provides a design-in checklist.

2.13.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting the highest averaged current consumption values in connected-mode, as specified in the SARA-R4 series Data Sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the following pins of the SARA-R4 series modules: **V_INT**, **PWR_ON** and **RESET_N** for diagnostic purpose.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, as the modules' signal names follow the ITU-T V.24 Recommendation [5].
- ☑ Provide accessible test points directly connected to all the UART pins of the SARA-R4 series modules (**TXD**, **RXD**, **DTR**, **DCD**) for diagnostic purpose, in particular providing a 0 Ω series jumper on each line to detach each UART pin of the module from the DTE application processor.
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ If the USB is not used, provide accessible test points directly connected to the USB interface (**VUSB_DET**, **USB_D+** and **USB_D-** pins).
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide proper precautions for EMC / ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of SARA-R4 series modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins can be left unconnected.

2.13.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** port (antenna RF interface).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (SIM signals, high-speed digital lines such as USB, and other data lines).
- ☑ Optimize placement for minimum length of RF line.
- ☑ Check the footprint and paste mask designed for SARA-R4 series module as illustrated in section 2.10.
- ☑ **VCC** line should be wide and as short as possible.
- ☑ Route **VCC** supply line away from RF line / part and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with application board solid ground layer.
- ☑ Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.

2.13.3 Antenna checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement, as reported in sections 4.2.2 and/or 0 for products marked with the FCC and/or IC.
- ☑ Ensure high isolation between the cellular antenna and any other antennas or transmitters present on the end device.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to SARA-R4 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the SARA-R4 series Data Sheet [1] and the u-blox Package Information Guide [23].

3.2 Handling

The SARA-R4 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ **Ensure ESD precautions are implemented during handling of the module.**

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of SARA-R4 series modules (as Human Body Model according to JESD22-A114F) is specified in the SARA-R4 series Data Sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the SARA-R4 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,…).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

"No Clean" soldering paste is strongly recommended for SARA-R4 series modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.10.

☞ The quality of the solder joints on the connectors ("half vias") should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended for SARA-R4 series modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes", published 2001.

Reflow profiles are to be selected according to the following recommendations.

⚠ **Failure to observe these recommendations can result in severe damage to the device!**

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200 °C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of 217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217 °C liquidus temperature: 40 - 60 s
- Peak reflow temperature: 245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

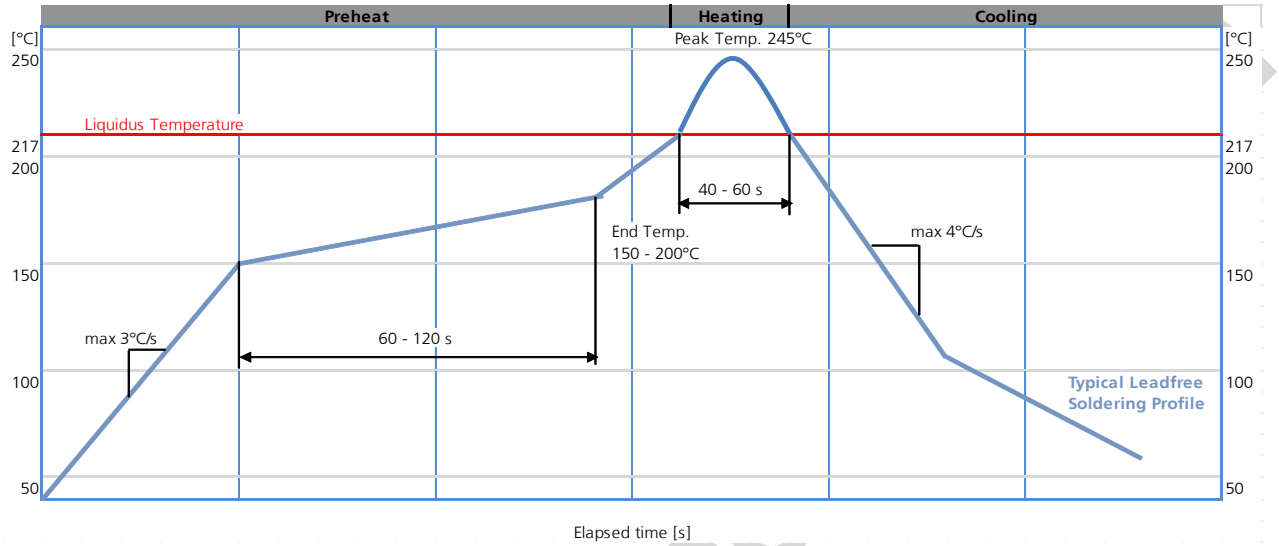

Figure 38: Recommended soldering profile

The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the SARA-R4 series modules, inspect the modules optically to verify that the module is properly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a module populated on it.

3.3.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with the modules.

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in the production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the cellular modules caused by any Ultrasonic Processes.

4 Approvals

☞ For the complete list and specific details regarding the certification schemes approvals, see SARA-R4 series Data Sheet [1], or please contact the u-blox office or sales representative nearest you.

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called "certification schemes" that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, such as:
    - CE (Conformité Européenne) marking for European Union
    - FCC (Federal Communications Commission) approval for United States
- Industry certification
  - Telecom industry specific approval verifying the interoperability between devices and networks:
    - GCF (Global Certification Forum), partnership between European device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator specific approval required by some mobile network operator, such as:
    - AT&T network operator in United States
    - Verizon Wireless network operator in United States

Even if SARA-R4 series modules are approved under all major certification schemes, the application device that integrates SARA-R4 series modules must be approved under all the certification schemes required by the specific application device to be deployed in the market.

The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device that integrates SARA-R4 series modules must be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device must operate.

☞ Check the appropriate applicability of the SARA-R4 series module's approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module's approval can significantly reduce the cost and time to market of the application device certification.

☞ The certification of the application device that integrates a SARA-R4 series module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

SARA-R4 series modules are certified according to all capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to the 3GPP TS 51.010-2 [17], 3GPP TS 34.121-2 [18], 3GPP TS 36.521-2 [20] and 3GPP TS 36.523-2 [21], is a statement of the implemented and supported capabilities and options of a device.

☞ The PICS document of the application device integrating SARA-R4 series modules must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device. For more details regarding the AT commands settings that affect the PICS, see the u-blox SARA-R404M AT Commands Manual [1].

☞ Check the specific settings required for mobile network operators approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.

4.2 US Federal Communications Commission notice

United States Federal Communications Commission (FCC) IDs:

- u-blox SARA-R404M cellular modules: XPY2AGQN1NNN

4.2.1 Safety warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, hygroscopic materials, or materials containing asbestos are employed

4.2.2 Declaration of Conformity

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for the SARA-R4 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value specified in the FCC Grant for mobile and fixed or mobile operating configurations:

- **SARA-R404 modules:**
  - **13 dBi in 750 MHz, i.e. LTE FDD-13 band**

4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the SARA-R4 series modules are authorized to use the FCC Grants of the SARA-R4 series modules for their own final products according to the conditions referenced in the certificates.

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPY2AGQN1NNN "

IMPORTANT: Manufacturers of portable applications incorporating the SARA-R4 series modules are required to have their final product certified and apply for their own FCC Grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Additional Note: as per 47CFR15.105 this equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- **Reorient or relocate the receiving antenna**
- **Increase the separation between the equipment and receiver**
- **Connect the equipment into an outlet on a circuit different from that to which the receiver is connected**
- **Consultant the dealer or an experienced radio/TV technician for help**

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically in production line. Stringent quality control process has been implemented in the production line. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment (ATE) in production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. Figure 39 illustrates typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

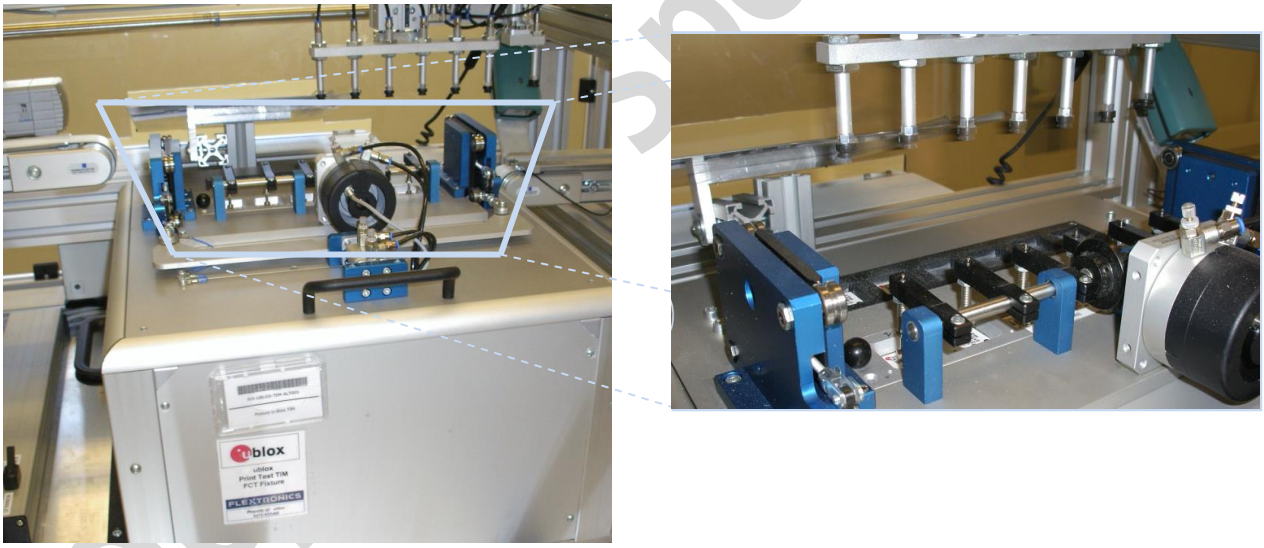

Figure 39: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

In addition, module AT commands can be used to perform functional tests on digital interfaces (communication with host controller, check SIM interface, GPIOs, etc.) or to perform RF performance tests (see the following section 5.2.2 for details).

5.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test is typically to compare the signal quality with a "Golden Device" in a location with excellent network coverage and known signal quality. This test should be performed after data connection has been established.

☞ These kinds of test may be useful as a "go/no go" test but not for RF performance measurements.

This test is suitable to check the functionality of communication with host controller, SIM card as well as power supply. It is also a means to verify if components at antenna interface are well soldered.

5.2.2 RF functional tests

The overall RF functional test of the device including the antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator with the assistance of AT+UTEST command over AT command user interface.

The AT+UTEST command provides a simple interface to set the module to Rx or Tx test modes ignoring the LTE signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported modulation schemes and bands
- receiving mode in a specified channel to returns the measured power level in all supported bands

☞ See the u-blox SARA-R404M AT Commands Manual [1] and the End user test Application Note [22], for the AT+UTEST command syntax description and detail guide of usage.

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces from which depends the RF performance.

To avoid module damage during transmitter test, a proper antenna according to module specifications or a 50 Ω termination must be connected to the ANT port.

To avoid module damage during receiver test, the maximum power level received at the ANT port must meet module specifications.

The AT+UTEST command sets the module to emit RF power ignoring LTE signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purpose in controlled environments by qualified user and must not be used during the normal module operation. Follow instructions suggested in u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 40 illustrates a typical test setup for such RF functional test.

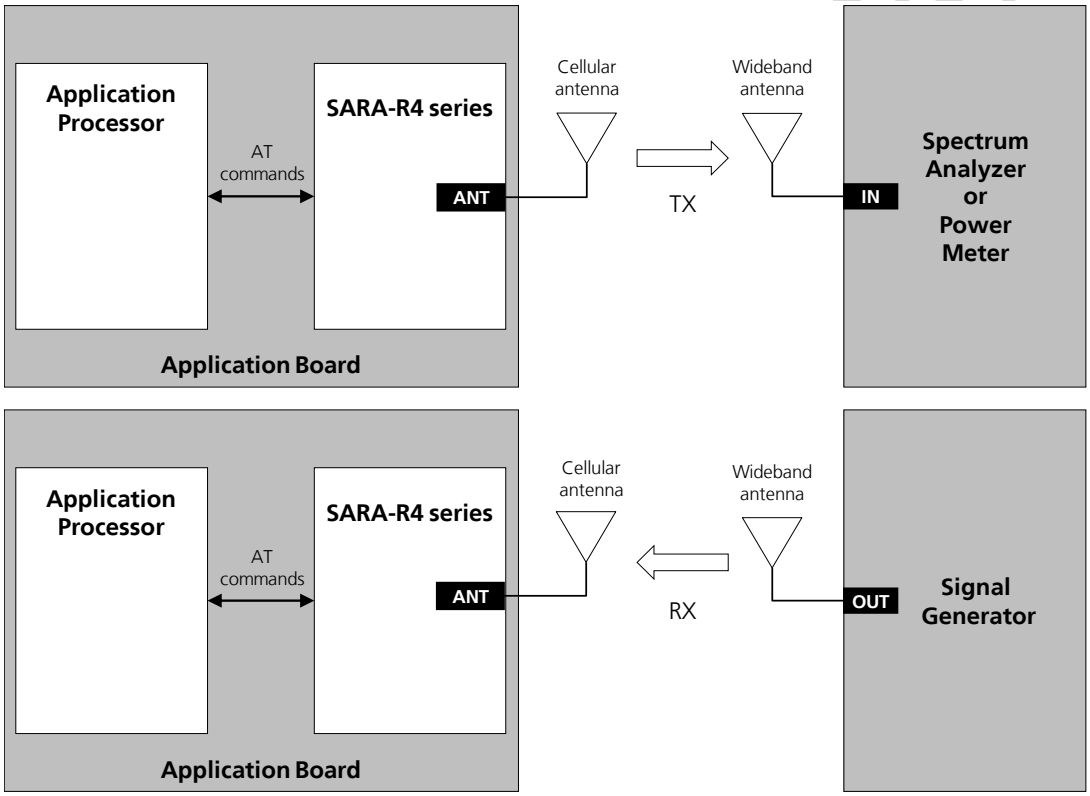

Figure 40: Setup with spectrum analyzer or power meter and signal generator for radiated measurements

Appendix

A Migration between SARA-R4 and SARA-G3

A.1 Overview

SARA-G3 and SARA-R4 series cellular modules have exactly the same SARA form factor (26.0 x 16.0 mm LGA) with exactly the same 96-pin layout as described in Figure 41, so that the modules can be alternatively mounted on a single application board using exactly the same copper mask, solder mask and paste mask.

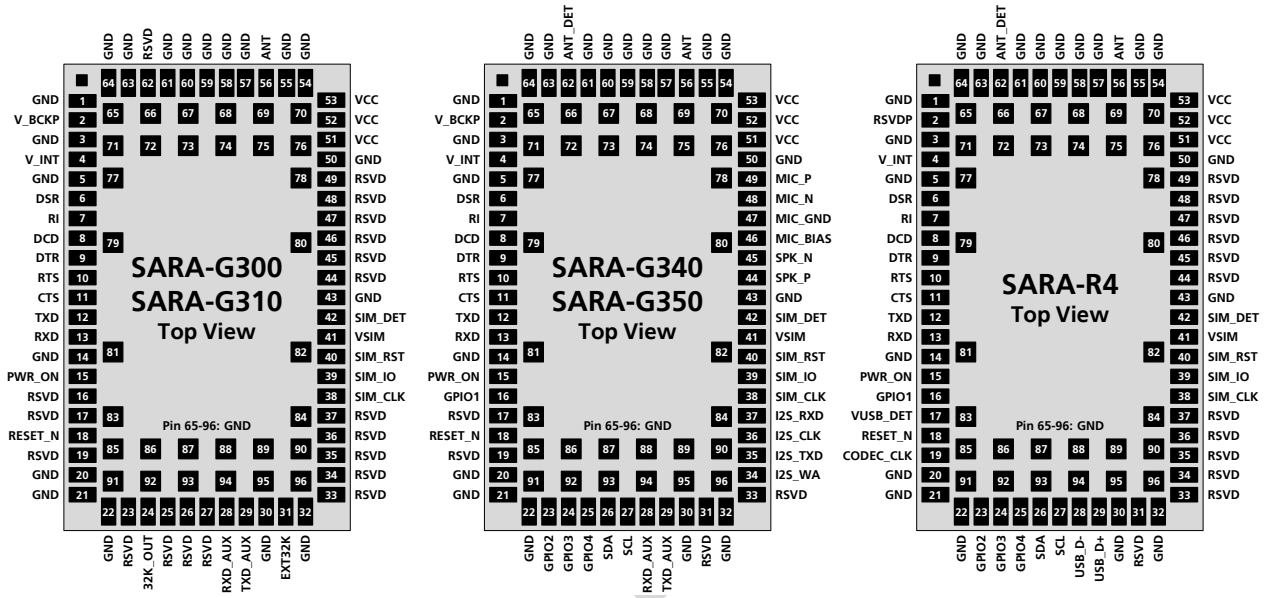

Figure 41: SARA-R4 and SARA-R4 seriesSARA-G3 series modules pad layout and pin assignment

SARA modules are also form-factor compatible with the u-blox LISA, LARA and TOBY cellular module families: although each has a different form factor, the footprints for the TOBY, LISA, SARA and LARA modules have been developed to ensure layout compatibility.

With the u-blox "nested design" solution, any TOBY, LISA, SARA or LARA module can be alternatively mounted on the same space of a single "nested" application board as described in Figure 42. Guidelines in order to implement a nested application board, description of the u-blox reference nested design and comparison between TOBY, LISA, SARA and LARA modules are provided in the Nested Design Application Note [26].

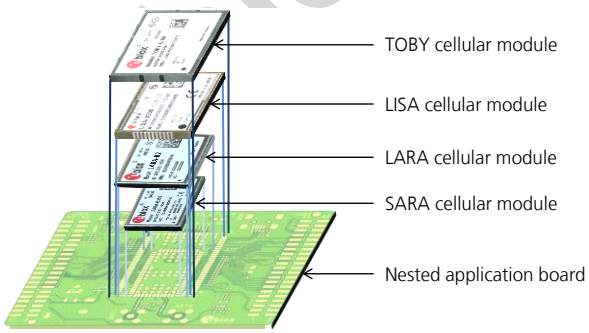

Figure 42: TOBY, LISA, SARA, LARA modules' layout compatibility: all modules are accommodated on the same nested footprint

Figure 28 summarizes the interfaces provided by TOBY-L2 and SARA-R4 series modules.

Modules	Power			Antenna			System				SIM		Serial					Audio			Other				
	Module supply input	RTC supply I/O	1.8 V supply Output	Antenna RF I/O	Rx diversity input	Antenna detection	Power-on input	Reset input	32 kHz input	32 kHz output	1.8 V / 3.0 V SIM	SIM detection	1.8 V UART	1.8 V UART AUX	1.8 V SPI	USB 2.0	1.8 V DDC	Analog audio I/O	1.8 V digital audio	13/26 MHz output	1.8 V GPIOs	Network indication	GNSS supply enable	GNSS Tx data ready	GNSS RTC sharing
SARA-G300/G310 series	•	•	•	•			•	•	•	•	•	•	•	•											
SARA-G340/G350 series	•	•	•	•		•	•	•			•	•	•	•			•	•	•		•	•	•	•	•
SARA-R4 series	•		•	•		•	•	•			•	F	•			•	F				•	•	F	F	F

F = supported by future product versions

Table 30: Summary of SARA-R4 and SARA-G3 series modules interfaces

A.2 Pin-out comparison between SARA-R4 and SARA-G3

	SARA-G3		SARA-R4		
Pin No	**Pin Name**	**Description**	**Pin Name**	**Description**	**Remarks for migration**
1	GND	Ground	GND	Ground	
2	V_BCKP	RTC Supply I/O Output characteristics: 2.3 V typ, 2 mA max Input op. range: 1.0 V – 2.4 V	RSVD	Reserved	RTC supply not available on SARA-R4 series modules
3	GND	Ground	GND	Ground	
4	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 50 mA max	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 300 mA max	No functional difference
5	GND	Ground	GND	Ground	
6	DSR	UART DSR Output 1.8 V, Driver strength: 6 mA	DSR	UART DSR Output 1.8 V	No functional difference
7	RI	UART RI Output 1.8 V, Driver strength: 6 mA	RI	UART RI Output 1.8 V	No functional difference
8	DCD	UART DCD Output 1.8 V, Driver strength: 6 mA	DCD	UART DCD Output 1.8 V	No functional difference
9	DTR	UART DTR Input 1.8 V, Internal pull-up: ~33k	DTR	UART DTR Input 1.8 V	No functional difference
10	RTS	UART RTS Input 1.8 V, Internal pull-up:~58 k	RTS	UART RTS Input 1.8 V	No functional difference
11	CTS	UART CTS Output 1.8 V, Driver strength: 6 mA	CTS	UART CTS Output 1.8 V	No functional difference
12	TXD	UART Data Input 1.8 V, Internal pull-up:~18 k	TXD	UART Data Input 1.8 V	No functional difference
13	RXD	UART Data Output 1.8 V, Driver strength: 6 mA	RXD	UART Data Output 1.8 V	No functional difference
14	GND	Ground	GND	Ground	
15	PWR_ON	Power-on Input No internal pull-up L-level: -0.10 V – 0.65 V H-level: 2.00 V – 4.50 V ON L-level time: 5 ms min OFF L-level pulse time: Not Available	PWR_ON	Power-on Input 200 k internal pull-up L-level: -0.3 V – 0.35*V_INT V H-level: 0.65*V_INT V – V_INT+0.3 V ON L-level pulse time: 85 ms min OFF L-level pulse time: 1018 ms min	On SARA-R4 series, the module is powered on applying a low pulse on the PWR_ON pin. PWR_ON pin can be used to power off SARA-R4 series modules
16	GPIO1 / RSVD	1.8 V GPIO / Reserved Default: Pin disabled Driver strength: 6 mA Internal pull-down: ~35 k	GPIO1	1.8 V GPIO Default: Pin disabled	No functional difference
17	RSVD	Reserved	VUSB_DET	USB Detect Input 5 V, Supply detection	USB detection instead of Reserved available on SARA-R4 series
18	RESET_N	Reset signal Internal diode & pull-up L-level: -0.30 V – 0.30 V H-level: 2.00 V – 4.70 V Reset L-level pulse time: 50 ms min (SARA-G350/G340) 3 s min (SARA-G300/G310)	RESET_N	Reset signal 37.4 k internal pull-up L-level: -0.30 V – 0.35*V_INT V H-level: 0.65*V_INT V – V_INT+0.3 V Reset L-level pulse time: 7900 ms min	On SARA-R4 series, a low level on the RESET_N line triggers an abrupt hardware shutdown of the module
19	RSVD	Reserved	GPIO5	1.8 V GPIO	GPIO available instead of Reserved on SARA-R4 series
20-22	GND	Ground	GND	Ground	
23	GPIO2 / RSVD	1.8 V GPIO / Reserved Default: GNSS supply enable Driver strength: 6 mA Internal pull-down: ~35 k	GPIO2	1.8 V GPIO	No functional difference
24	GPIO3 / 32K_OUT	1.8 V GPIO / 32 kHz Output Default: GNSS data ready Driver strength: 5 mA Inner pull-down: ~67 k	GPIO3	1.8 V GPIO	No functional difference

	SARA-G3		SARA-R4		
Pin No	**Pin Name**	**Description**	**Pin Name**	**Description**	**Remarks for migration**
25	GPIO4 / RSVD	1.8 V GPIO / Reserved Default: GNSS RTC sharing Driver strength: 6 mA Internal pull-down: ~35 k	GPIO4	1.8 V GPIO	No functional difference
26	SDA / RSVD	I²C Data I/O / Reserved 1.8 V, open drain Driver strength: 3 mA	SDA	I²S Data I/O 1.8 V, open drain	No functional difference
27	SCL / RSVD	I²C Clock Output / Reserved 1.8 V, open drain Driver strength: 3 mA	SCL	I²C Clock Output 1.8 V, open drain	No functional difference
28	RXD_AUX	Aux UART Data Out 1.8 V, Driver strength: 5 mA	USB_D-	USB Data I/O (D-) High-Speed USB 2.0	USB instead of Auxiliary UART on SARA-R4 series
29	TXD_AUX	Aux UART Data In 1.8 V, Internal pull-up:~18 k	USB_D+	USB Data I/O (D+) High-Speed USB 2.0	USB instead of Auxiliary UART on SARA-R4 series
30	GND	Ground	GND	Ground	
31	RSVD / EXT32K	Reserved / 32 kHz Input	RSVD	Reserved	No functional difference
32	GND	Ground	GND	Ground	
33	RSVD	Reserved	RSVD	Reserved	No functional difference
34	I2S_WA / RSVD	I²S Word Alignment / Reserved 1.8 V, Driver strength: 6 mA	RSVD	Reserved	Reserved on SARA-R4 series modules
35	I2S_TXD / RSVD	I²S Data Output / Reserved 1.8 V, Driver strength: 5 mA	RSVD	Reserved	Reserved on SARA-R4 series modules
36	I2S_CLK / RSVD	I²S Clock / Reserved 1.8 V, Driver strength: 5 mA	RSVD	Reserved	Reserved on SARA-R4 series modules
37	I2S_RXD / RSVD	I²S Data Input / Reserved 1.8 V, Internal pull-down:~18 k	RSVD	Reserved	Reserved on SARA-R4 series modules
38	SIM_CLK	SIM Clock Output	SIM_CLK	SIM Clock Output	No functional difference
39	SIM_IO	SIM Data I/O	SIM_IO	SIM Data I/O	No functional difference
40	SIM_RST	SIM Reset Output	SIM_RST	SIM Reset Output	No functional difference
41	VSIM	SIM Supply Output	VSIM	SIM Supply Output	No functional difference
42	SIM_DET	SIM Detection Input 1.8 V, Internal pull-down:~18 k	SIM_DET	SIM Detection Input 1.8 V	No functional difference
43	GND	Ground	GND	Ground	
44	SPK_P / RSVD	Analog Audio Out (+) / Reserved	RSVD	Reserved	Reserved on SARA-R4 series modules
45	SPK_N / RSVD	Analog Audio Out (-) / Reserved	RSVD	Reserved	Reserved on SARA-R4 series modules
46	MIC_BIAS / RSVD	Microphone Supply Out / Reserved	RSVD	Reserved	Reserved on SARA-R4 series modules
47	MIC_GND / RSVD	Microphone Ground / Reserved	RSVD	Reserved	Reserved on SARA-R4 series modules
48	MIC_N / RSVD	Analog Audio In (-) / Reserved	RSVD	Reserved	Reserved on SARA-R4 series modules
49	MIC_P / RSVD	Analog Audio In (+) / Reserved	RSVD	Reserved	Reserved on SARA-R4 series modules
50	GND	Ground	GND	Ground	
51-53	VCC	Module Supply Input Normal op. range: 3.35 V – 4.5 V Extended op. range: 3.00 V – 4.5 V	VCC	Module Supply Input Normal op. range: 3.2 V – 4.2 V Extended op. range: 3.0 V – 4.3 V	No functional difference
54-55	GND	Ground	GND	Ground	
56	ANT	RF Antenna I/O ESD immunity (IEC 61000-4-2): ±4 kV contact / ±8 kV air ESD	ANT	RF Antenna I/O	No functional difference
57-61	GND	Ground	GND	Ground	
62	ANT_DET / RSVD	Antenna Detection Input / Reserved	ANT_DET	Antenna Detection Input	No functional difference
63-96	GND	Ground	GND	Ground	

Table 31: SARA-R4 and SARA-G4 series modules pin assignment with remarks for migration

For further details regarding the characteristics, capabilities, usage or settings applicable for each interface of the cellular modules, see the SARA-R4 series Data Sheet [1], the SARA-G3 series Data Sheet [24], the SARA-G3 / SARA-U2 series System Integration Manual [25], the u-blox SARA-R404M AT Commands Manual [1] and the Nested Design Application Note [26].

A.3 Schematic for SARA-R4 and SARA-G3 integration

Figure 43 shows an example of schematic diagram where a SARA-R3 or a SARA-G3 series module can be integrated into the same application board, using all the available interfaces and functions of the modules. The different mounting options for the external parts are highlighted in different colors as described in the legend, according to the interfaces supported by the relative modules.

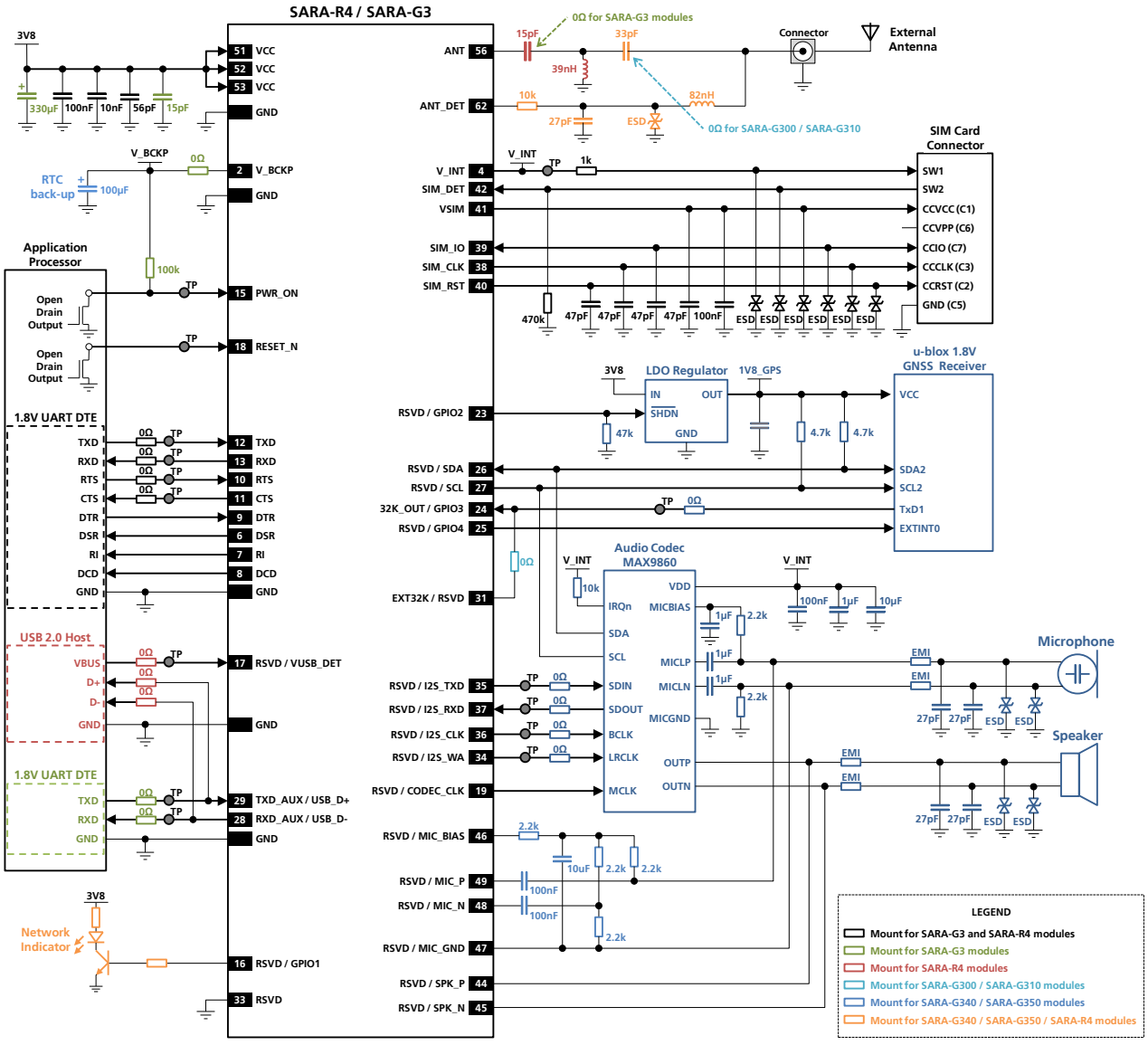

Figure 43: Example of complete schematic diagram to integrate SARA-R4 modules and SARA-G3 modules on the same application board, using all the available interfaces / functions of the modules

B Glossary

3GPP	3rd Generation Partnership Project
8-PSK	8 Phase-Shift Keying modulation
16QAM	16-state Quadrature Amplitude Modulation
64QAM	64-state Quadrature Amplitude Modulation
ACM	Abstract Control Model
ADC	Analog to Digital Converter
AP	Application Processor
ASIC	Application-Specific Integrated Circuit
AT	AT Command Interpreter Software Subsystem, or attention
BAW	Bulk Acoustic Wave
CSFB	Circuit Switched Fall-Back
DC	Direct Current
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DTE	Data Terminal Equipment
ECM	Ethernet networking Control Model
EDGE	Enhanced Data rates for GSM Evolution
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
E-UTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplex
FEM	Front End Module
FOAT	Firmware Over AT commands
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
HBM	Human Body Model
HSIC	High Speed Inter Chip
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	HyperText Transfer Protocol
HW	Hardware
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit interface
I^2S	Inter IC Sound interface
IP	Internet Protocol
LDO	Low-Dropout
LGA	Land Grid Array

LNA	Low Noise Amplifier
LPDDR	Low Power Double Data Rate synchronous dynamic RAM memory
LTE	Long Term Evolution
M2M	Machine-to-Machine
MBIM	Mobile Broadband Interface Model
MIMO	Multi-Input Multi-Output
N/A	Not Applicable
N.A.	Not Available
NCM	Network Control Model
OEM	Original Equipment Manufacturer device: an application device integrating a u-blox cellular module
OTA	Over The Air
PA	Power Amplifier
PCM	Pulse Code Modulation
PCN / IN	Product Change Notification / Information Note
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PWM	Pulse Width Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMII	Reduced Media Independent Interface
RNDIS	Remote Network Driver Interface Specification
RSE	Radiated Spurious Emission
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input Output
SIM	Subscriber Identification Module
SMS	Short Message Service
SRF	Self Resonant Frequency
SSL	Secure Socket Layer
TBD	To Be Defined
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TIS	Total Isotropic Sensitivity
TP	Test-Point
TRP	Total Radiated Power
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VoLTE	Voice over LTE
VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WLAN	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WWAN	Wireless Wide Area Network (GSM / UMTS / LTE cellular radio technology)

Related documents

[1] u-blox SARA-R404M AT Commands Manual, Docu No UBX-17003787

[2] u-blox EVK-R2xx User Guide, Docu No UBX-16016088

[3] u-blox Windows Embedded OS USB Driver Installation Application Note, Docu No UBX-14003263

[4] Universal Serial Bus Revision 2.0 specification, http://www.usb.org/developers/docs/usb20_docs/

[5] ITU-T Recommendation V.24 - 02-2000 - List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE), http://www.itu.int/rec/T-REC-V.24-200002-I/en

[6] 3GPP TS 27.007 - AT command set for User Equipment (UE)

[7] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

[8] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol

[9] u-blox Mux Implementation Application Note, Docu No UBX-13001887

[10] I^2C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP Semiconductors, http://www.nxp.com/documents/user_manual/UM10204.pdf

[11] u-blox GNSS Implementation Application Note, Docu No UBX-13001849

[12] GSM Association TS.09 - Battery Life Measurement and Current Consumption Technique http://www.gsma.com/newsroom/wp-content/uploads//TS.09_v8.0.pdf

[13] CENELEC EN 61000-4-2 (2001): "Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test".

[14] ETSI EN 301 489-1 V1.8.1: "Electromagnetic compatibility and Radio spectrum Matters (ERM); EMC standard for radio equipment and services; Part 1: Common technical requirements"

[15] ETSI EN 301 489-7 V1.3.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); EMC standard for radio equipment and services; Part 7: Specific conditions for mobile and portable radio and ancillary equipment of digital cellular radio telecommunications systems"

[16] ETSI EN 301 489-24 V1.4.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); EMC standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment"

[17] 3GPP TS 51.010-2 - Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS)

[18] 3GPP TS 34.121-2 - Technical Specification Group Radio Access Network; User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 2: Implementation Conformance Statement (ICS)

[19] 3GPP TS 36.521-1 - Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing

[20] 3GPP TS 36.521-2 - Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)

[21] 3GPP TS 36.523-2 - Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)

[22] u-blox End user test Application Note, Docu No UBX-13001922

[23] u-blox Package Information Guide, Docu No UBX-14001652

[24] u-blox SARA-G3 series Data Sheet, Docu No UBX-13000993

[25] u-blox SARA-G3 / SARA-U2 series System Integration Manual, Docu No UBX- 13000995

[26] u-blox Nested Design Application Note, Docu No UBX-16007243

Some of the above documents can be downloaded from u-blox web-site (http://www.u-blox.com/).

Revision history

Revision	Date	Name	Status / Comments
R01	31-Jan-2017	sfal	Initial release for SARA-R4 series modules

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