WIRELESS

LISA-U series

3.75G HSPA / HSPA+ Wireless Modules

System Integration Manual

locate, communicate, accelerate

Abstract

This document describes the features and the system integration of LISA-U1 series HSPA and LISA-U2 series HSPA+ wireless modules.

These modules are complete and cost efficient 3.75G solutions offering up to six-band HSDPA/HSUPA and quad-band GSM/EGPRS voice and/or data transmission technology in a compact form factor.

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Document Information	
Title	LISA-U series
Subtitle	3.75G HSPA / HSPA+ Wireless Modules
Document type	System Integration Manual
Document number	3G.G2-HW-10002-A2
Document status	Preliminary

Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
LISA-U100	LISA-U100-00S-00	10.72	3G.G2-SW-11000
	LISA-U100-01S-00	11.40	n.a.
LISA-U110	LISA-U110-00S-00	10.72	3G.G2-SW-11000
	LISA-U110-01S-00	11.40	n.a.
LISA-U120	LISA-U120-00S-00	10.72	3G.G2-SW-11000
	LISA-U120-01S-00	11.40	n.a.
LISA-U130	LISA-U130-00S-00	10.72	3G.G2-SW-11000
	LISA-U130-01S-00	11.40	n.a.
	LISA-U130-01A-00	11.40	n.a.
LISA-U200	LISA-U200-00S-00	21.21	n.a.
	LISA-U200-01S-00	TBD	n.a.
LISA-U230	LISA-U230-01S-00	TBD	n.a.
	LISA-U230-01A-00	TBD	n.a.

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

AT Commands Manual: This document provides the description of the supported AT commands by the LISA-U series modules to verify all implemented functionalities.

System Integration Manual: This Manual provides hardware design instructions and information on how to set up production and final product tests.

Application Note: document provides general design instructions and information that applies to all u-blox Wireless modules. See Section Related documents for a list of Application Notes related to your Wireless Module.

How to use this Manual

The LISA-U series System Integration Manual provides the necessary information to successfully design in and configure these u-blox wireless modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox Wireless Integration, please:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com
- Read the questions and answers on our FAQ database on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

Contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support please have the following information ready:

- Module type (e.g. LISA-U100) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

LISA-U series wireless modules integrate full-feature 3G UMTS/HSxPA and 2G GSM/GPRS/EDGE protocol stack with Assisted GPS support. These SMT modules come in the compact LISA form factor, featuring Leadless Chip Carrier (LCC) packaging technology.

3G UMTS/HSDPA/HSUPA Characteristics	**2G GSM/GPRS/EDGE Characteristics**
Class A User Equipment[1]	Class B Mobile Station[2]
UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) • 3GPP Release 6 High Speed Packet Access (HSPA) for LISA-U1 series • 3GPP Release 7 Evolved High Speed Packet Access (HSPA+) for LISA-U2 series • Rx Diversity for LISA-U230	GSM EDGE Radio Access (GERA) • 3GPP Release 6 for LISA-U1 series • 3GPP Release 7 for LISA-U2 series • Rx Diversity for LISA-U230
2-band support for LISA-U100, LISA-U120: • Band II (1900 MHz), Band V (850 MHz) 2-band support for LISA-U110, LISA-U130: • Band I (2100 MHz), Band VIII (900 MHz) 4-band support for LISA-U200-00: • Band I (2100 MHz), Band II (1900 MHz), Band V (850 MHz), Band VI (800 MHz) 6-band support for LISA-U200-01, LISA-U230: • Band I (2100 MHz), Band II (1900 MHz), Band IV (1700 MHz), Band V (850 MHz), Band VI (800 MHz), Band VIII (900 MHz)	4-band support • GSM 850 MHz, E-GSM 900 MHz, DCS 1800 MHz, PCS 1900 MHz
WCDMA/HSDPA/HSUPA Power Class • Power Class 3 (24 dBm) for WCDMA/HSDPA/HSUPA mode	GSM/GPRS Power Class • Power Class 4 (33 dBm) for GSM/E-GSM bands • Power Class 1 (30 dBm) for DCS/PCS bands EDGE Power Class • Power Class E2 (27 dBm) for GSM/E-GSM bands • Power Class E2 (26 dBm) for DCS/PCS bands
PS (Packet Switched) Data Rate • HSUPA category 6, up to 5.76 Mb/s UL • HSDPA category 8 up to 7.2 Mb/s DL for LISA-U1 series, LISA-U200 • HSDPA category 14 up to 21.1 Mb/s DL for LISA-U230 • WCDMA PS data up to 384 kb/s DL/UL	PS (Packet Switched) Data Rate • GPRS multislot class 33[4], coding scheme CS1-CS4, up to 107 kb/s DL, 85.6 kb/s UL for LISA-U2 series • GPRS multislot class 12[4], coding scheme CS1-CS4, up to 85.6 kb/s DL/UL for LISA-U1 for LISA-U1 series • EDGE multislot class 33[3], coding scheme MCS1-MCS9, up to 296 kb/s DL, 236.8 kb/s UL for LISA-U2 • EDGE multislot class 12[4], coding scheme MCS1-MCS9, up to 236.8 kb/s DL/UL for LISA-U1
CS (Circuit Switched) Data Rate • WCDMA CS data up to 64 kb/s DL/UL	CS (Circuit Switched) Data Rate • GSM CS data up to 9.6 kb/s DL/UL supported in transparent/non transparent mode

Table 1: LISA-U series UMTS/HSDPA/HSUPA and GSM/GPRS/EDGE characteristics

Operation modes I to III are supported on GSM/GPRS network, with user-defined preferred service selectable from GSM to GPRS. Paging messages for GSM calls can be optionally monitored during GPRS data transfer in not-coordinating NOM II-III.

[1] Device can work simultaneously in Packet Switch and Circuit Switch mode: voice calls are possible while the data connection is active without any interruption in service.
[2] Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for example during data transmission an incoming call occurs, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.
[3] GPRS/EDGE multislot class 33 implies a maximum of 5 slots in DL (reception) and 4 slots in UL (transmission) with 6 slots in total.
[4] GPRS/EDGE multislot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.

Direct Link mode is supported for TCP / UDP sockets except for LISA-U1xx-00 module versions.

Regarding 3G transmit and receive data rate capability, LISA-U series modules implement 3G High-Speed Uplink Packet Access (HSUPA) category 6, LISA-U1 series and LISA-U200 modules implement 3G High Speed Downlink Packet Access (HSDPA) category 8, while LISA-U230 modules implement the 3G HSDPA category 14. HSUPA and HSDPA categories determine the maximum speed at which data can be respectively transmitted and received: higher categories allowing faster data transfer rates as indicated in Table 1.

The 3G network automatically performs adaptive coding and modulation using a choice of forward error correction code rate and choice of modulation type, to achieve the highest possible data rate and data transmission robustness according to the quality of the radio channel.

Regarding 2G transmit and receive data rate capability, LISA-U1 series modules implement GPRS/EGPRS class 12, while LISA-U2 series modules implement GPRS/EGPRS class 33. GPRS and EGPRS classes determine the maximum number of timeslots available for upload and download and thus the speed at which data can be transmitted and received: higher classes typically allowing faster data transfer rates as indicated in Table 1.

The 2G network automatically configures the number of timeslots used for reception or transmission (voice calls take precedence over GPRS/EGPRS traffic) and channel encoding (from Coding Scheme 1 up to Modulation and Coding Scheme 9), performing link adaptation to achieve the highest possible data rate.

A summary of interfaces and features provided by LISA-U series modules is described in the Table 2. Note that LISA-U130-01 and LISA-U230-01 are available in standard and automotive quality grade versions.

Module	**Technology**		**Bands**		**Interface**					**Audio**	
	HSUPA [Mb/s]	HSDPA [Mb/s]	UMTS/HSPA bands [MHz]	GSM/GPRS/EDGE quad-band	UART	SPI (5 wire)	USB	DDC for u-blox GPS	GPIO	Analog Audio	Digital Audio
LISA-U100-00	5.76	7.2	850/1900	•	1	1	1	1	5		
LISA-U100-01	5.76	7.2	850/1900	•	1	1	1	1	5		
LISA-U110-00	5.76	7.2	900/2100	•	1	1	1	1	5		
LISA-U110-01	5.76	7.2	900/2100	•	1	1	1	1	5		
LISA-U120-00	5.76	7.2	850/1900	•	1	1	1	1	5	1	1
LISA-U120-01	5.76	7.2	850/1900	•	1	1	1	1	5	1	1
LISA-U130-00	5.76	7.2	900/2100	•	1	1	1	1	5	1	1
LISA-U130-01	5.76	7.2	900/2100	•	1	1	1	1	5	1	1
LISA-U200-00	5.76	7.2	800/850/ 1900/2100	•	1	1	1	1	9		
LISA-U200-01	5.76	7.2	800/850/900/ 1700/1900/2100	•	1	1	1	1	14		2
LISA-U230-01	5.76	21.1	800/850/900/ 1700/1900/2100	•	1	1	1	1	14		2

Module	**Functions**											
	Network indication	Antenna Supervisor	Jamming detection	Embedded TCP/UDP stack	HTTP, SSL	GPS via Modem	Embedded AssistNow	FW update over AT (FOAT)	In-band modem	Rx diversity	CellLocate	SIM Access Profile (SAP)
LISA-U100-00	•	•		•		•	•					
LISA-U100-01	•	•	•	•	•	•	•	•			•	
LISA-U110-00	•	•		•		•	•					
LISA-U110-01	•	•	•	•	•	•	•	•			•	
LISA-U120-00	•	•		•		•	•					
LISA-U120-01	•	•	•	•	•	•	•	•			•	
LISA-U130-00	•	•		•		•	•					
LISA-U130-01	•	•	•	•	•	•	•	•	•		•	
LISA-U200-00	•	•	•	•	•			•				
LISA-U200-01	•	•	•	•	•	•	•	•	•		•	•
LISA-U230-01	•	•	•	•	•	•	•	•	•	•	•	•

Table 2: LISA-U series features summary

1.2 Architecture

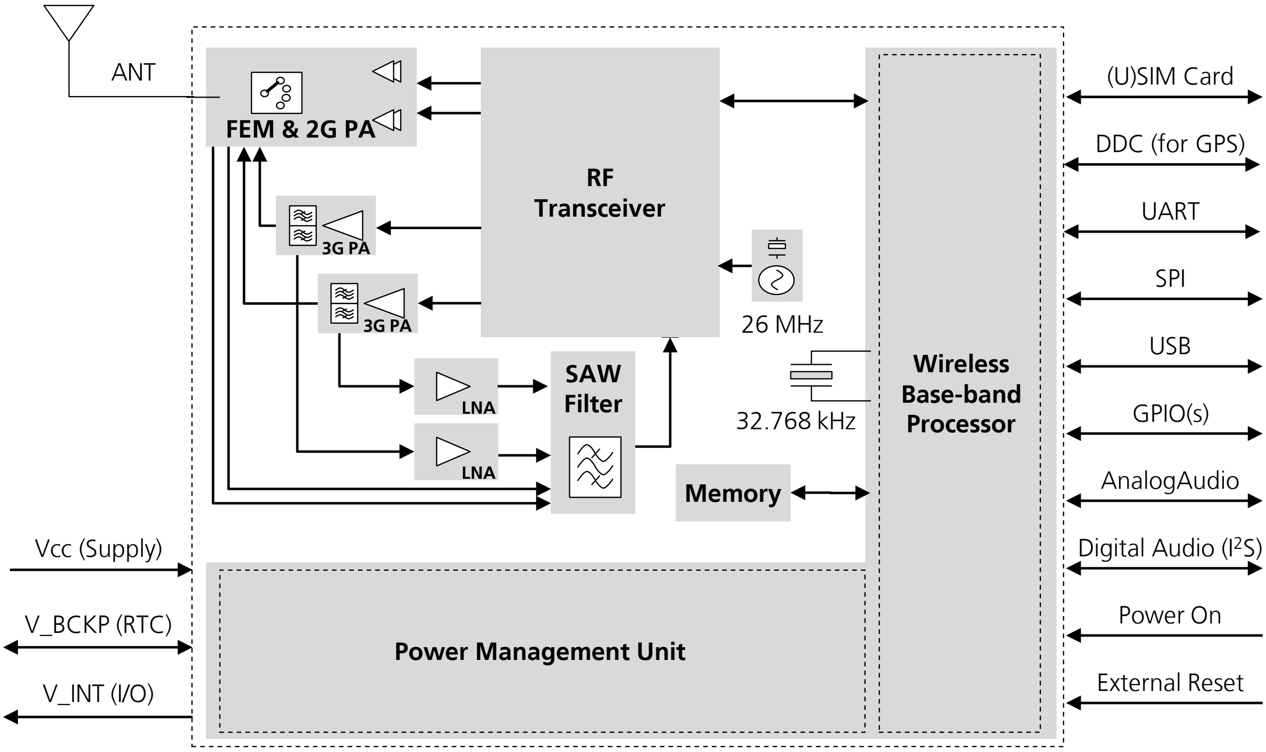

Figure 1: LISA-U1 series block diagram (for available options refer to the product features summary in Table 2)

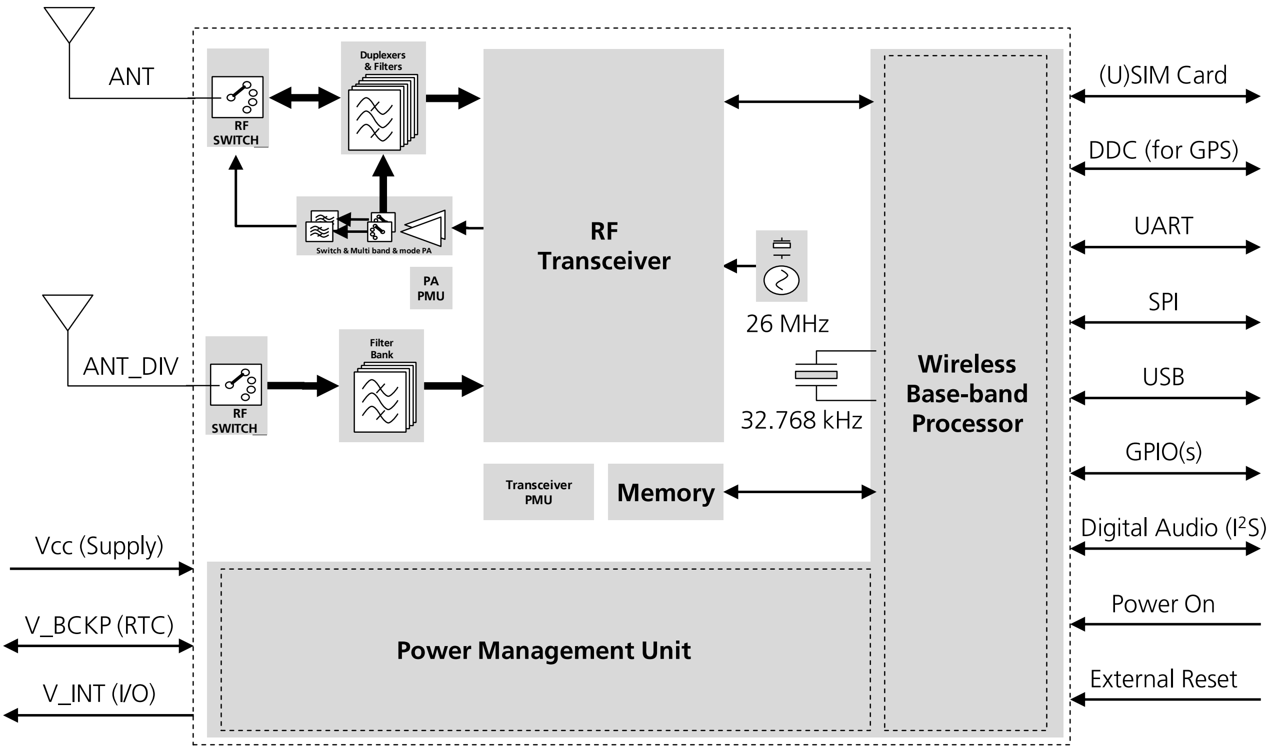

Figure 2: LISA-U2 series block diagram (for available options refer to the product features summary in Table 2)

1.2.1 Functional blocks

LISA-U series modules consist of the following internal functional blocks: RF section, Baseband and Power Management Unit section.

LISA-U1 series RF section

A shielding box includes the RF high-power signal circuitry, namely:

- Front-End Module (FEM) with integrated quad-band 2G Power Amplifier and antenna switch multiplexer
- Two single-band 3G HSPA/WCDMA Power Amplifier modules with integrated duplexers

The RF antenna pad (**ANT**) is directly connected to the FEM, which dispatches the RF signals according to the active mode. For time-duplex 2G operation, the incoming signal at the active Receiver (RX) slot is applied to integrated SAW filters for out-of-band rejection and then sent to the appropriate receiver port of the RF transceiver. During the allocated Transmitter (TX) slots, the low level signal coming from the RF transceiver is enhanced by the 2G power amplifier module and then directed to the antenna through the FEM. The 3G transmitter and receiver are instead active at the same time due to frequency-domain duplex operation. The switch integrated in the FEM connects the antenna port to the passive duplexer which separates the TX and RX signal paths. The duplexer itself provides front-end RF filtering for RX band selection while combining the amplified TX signal coming from the fixed gain linear power amplifier.

In the same shielding box that includes the RF high-power signal circuitry there are all the low-level analog RF components, namely:

- Dual-band HSPA/WCDMA and quad-band EDGE/GPRS/GSM transceiver
- Voltage Controlled Temperature Compensated 26 MHz Crystal Oscillator (VC-TCXO)
- Low Noise Amplifier (LNA) and SAW RF filters for 2G and 3G receivers

While operating in 3G mode, the RF transceiver performs direct up-conversion and down-conversion of the baseband I/Q signals, with the RF voltage controlled gain amplifier being used to set the uplink TX power. In the downlink path, the external LNA enhances the RX sensitivity while discrete inter-stage SAW filters additionally improve the rejection of out-of-band blockers. An internal programmable gain amplifier optimizes the signal levels before delivering to the analog I/Q to baseband for further digital processing.

For 2G operations, a constant gain direct conversion receiver with integrated LNAs and highly linear RF quadrature demodulator are used to provide the same I/Q signals to baseband as well. In transmission mode, the up-conversion is implemented by means of a digital sigma-delta transmitter or polar modulator depending on the modulation to be transmitted.

In all the modes, a fractional-N sigma-delta RF synthesizer and an on-chip 3.296-4.340 GHz voltage controlled oscillator are used to generate the local oscillator signal.

The frequency reference to RF oscillators is provided by the 26 MHz VC-TCXO. The same signal is buffered to the baseband as a master reference for clock generation circuits while operating in active mode.

LISA-U2 series RF section

A shielding box contains the RF high-power signal circuitry, including:

- Multimode Single Chain Power Amplifier Module used for 3G HSPA/WCDMA and 2G EDGE/GSM operations
- Power Management Unit with integrated DC/DC converter for the Power Amplifier Module

The RF antenna pad (**ANT**) is directly connected to the main antenna switch, which dispatches the RF signals according to the active mode. For time-duplex 2G operation, the incoming signal at the active Receiver (RX) slot is applied by the main antenna switch to the duplexer SAW filter bank for out-of-band rejection and then sent to the appropriate receiver port of the RF transceiver. During the allocated Transmitter (TX) slots, the low level signal coming from the RF transceiver is enhanced by the power amplifier and then directed to the antenna pad through the main antenna switch. The 3G transmitter and receiver are active at the same time due to frequency-domain duplex operation. The switch integrated in the main antenna switch connects the antenna port to the duplexer SAW filter bank which separates the TX and RX signal paths. The duplexer itself provides front-end RF filtering for RX band selection while combining the amplified TX signal coming from the power amplifier.

A separated shielding box contains all the other analog RF components, including:

- Main Antenna Switch
- Duplexer SAW filter bank
- Antenna Switch for diversity receiver
- SAW filter bank for diversity receiver
- Six-band HSPA/WCDMA and quad-band EDGE/GPRS/GSM transceiver
- Power Management Unit with integrated DC/DC converter for the Power Amplifier Module
- Voltage Controlled Temperature Compensated 26 MHz Crystal Oscillator (VC-TCXO)

While operating in 3G mode, the RF transceiver performs direct up-conversion and down-conversion of the baseband I/Q signals, with the RF voltage controlled gain amplifier being used to set the uplink TX power. In the downlink path, the integrated LNA enhances the RX sensitivity while discrete inter-stage SAW filters additionally improve the rejection of out-of-band blockers. An internal programmable gain amplifier optimizes the signal levels before delivering to the analog I/Q to baseband for further digital processing.

For 2G operations, a constant gain direct conversion receiver with integrated LNAs and highly linear RF quadrature demodulator are used to provide the same I/Q signals to the baseband as well. In transmission mode, the up-conversion is implemented by means of a digital sigma-delta transmitter or polar modulator depending on the modulation to be transmitted.

The RF antenna pad for the diversity receiver (**ANT_DIV**) available on LISA-U230 modules is directly connected to the antenna switch for the diversity receiver, which dispatches the incoming RF signals to the dedicated SAW filter bank for out-of-band rejection and then to the diversity receiver port of the RF transceiver.

In all the modes, a fractional-N sigma-delta RF synthesizer and an on-chip 3.296-4.340 GHz voltage controlled oscillator are used to generate the local oscillator signal.

The frequency reference to RF oscillators is provided by the 26 MHz VC-TCXO. The same signal is buffered to the baseband as a master reference for clock generation circuits while operating in active mode.

LISA-U series modulation techniques

Modulation techniques related to radio technologies supported by LISA-U series modules, are listed as follows:

- GSM → GSMK
- GPRS → GMSK
- EDGE → GMSK / 8-PSK
- WCDMA → QPSK
- HSDPA → QPSK / 16-QAM
- HSUPA → QPSK / 16-QAM

LISA-U series Baseband and Power Management Unit section

Another shielding box of LISA-U series modules includes all the digital circuitry and the power supplies, basically the following functional blocks:

- Wireless baseband processor, a mixed signal ASIC which integrates:
  - Microprocessor for controller functions, 2G & 3G upper layer software
  - DSP core for 2G Layer 1 and audio processing
  - 3G coprocessor and HW accelerator for 3G Layer 1 control software and routines
  - Dedicated HW for interfaces management
- Memory system in a Multi-Chip Package (MCP) integrating two devices:
  - NOR flash non-volatile memory
  - DDR SRAM volatile memory
- Power Management Unit (PMU), used to derive all the system supply voltages from the module supply VCC

- 32.768 kHz crystal, connected to the Real Time Clock (RTC) oscillator to provide the clock reference in idle or power-off mode

1.2.2 Hardware differences between LISA-U series modules

Main hardware differences between the LISA-U series modules are summarized in Table 3.

Characteristic	LISA-U1 series	LISA-U2 series
3G bands	LISA-U100, LISA-U120: • Band II (1900 MHz), Band V (850 MHz) LISA-U110, LISA-U130: • Band I (2100 MHz), Band VIII (900 MHz)	LISA-U200-00: • Band I (2100 MHz), Band II (1900 MHz), Band V (850 MHz), Band VI (800 MHz) LISA-U200-01, LISA-U230: • Band I (2100 MHz), Band II (1900 MHz), Band IV (1700 MHz), Band V (850 MHz), Band VI (800 MHz), Band VIII (900 MHz)
HSDPA data rate	LISA-U1 series: • HSDPA category 8, up to 7.2 Mb/s DL	LISA-U200: • HSDPA category 8, up to 7.2 Mb/s DL LISA-U230: • HSDPA category 14, up to 21.1 Mb/s DL
EDGE/GPRS data rate	EDGE multislot class 12, MCS1-MCS9, up to 236.8 kb/s DL/UL GPRS multislot class 12, CS1-CS4, up to 85.6 kb/s DL/UL	EDGE multislot class 33, MCS1-MCS9, up to 296 kb/s DL, 236.8 kb/s UL GPRS multislot class 33, CS1-CS4, up to 107 kb/s DL, 85.6 kb/s UL
Rx diversity	LISA-U1 series: • Not supported	LISA-U200: • Not supported LISA-U230: • Supported: **ANT_DIV** RF input for Rx diversity
Analog audio	LISA-U100, LISA-U110: • Not supported LISA-U120, LISA-U130: • One differential input, one differential output	LISA-U2 series: • Not supported
Digital audio	LISA-U100, LISA-U110: • Not supported LISA-U120, LISA-U130: • One 4-wire digital audio interface	LISA-U200-00: • Not supported LISA-U200-01, LISA-U230: • Two 4-wire digital audio interfaces • **CODEC_CLK** clock output for external codec
GPIO	5 GPIOs	Up to 14 GPIOs
VCC operating range	**VCC** normal operating range: 3.4 V – 4.2 V **VCC** extended operating range: 3.1 V – 4.2 V	**VCC** normal operating range: 3.3 V – 4.4 V **VCC** extended operating range: 3.1 V – 4.5 V
V_BCKP operating range	**V_BCKP** output: 2.3 V typ. **V_BCKP** input: 1.0 V – 2.5 V	**V_BCKP** output: 1.8 V typ. **V_BCKP** input: 1.0 V – 1.9 V
Exposed GND area	One signals keep-out area on the top layer of the application board, due to one exposed GND area on the bottom layer of the module (see Figure 61)	Two signals keep-out areas on the top layer of the application board, due to two exposed GND areas on the bottom layer of the module (see Figure 62)

Table 3: Main hardware differences between LISA-U series modules

For additional details and minor hardware differences between the LISA-U series modules, refer to section A.3.

1.3 Pin-out

Table 4 lists the pin-out of the LISA-U series modules, with pins grouped by function.

Function	Pin	Module	No	I/O	Description	Remarks
Power	**VCC**	All	61, 62, 63	I	Module supply input	Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided has to be always above the minimum limit of the operating range. Consider that there are large current spikes in connected mode, when a GSM call is enabled. **VCC** pins are internally connected, but all the available pads must be connected to the external supply in order to minimize power loss due to series resistance. See section 1.5.2
	GND	All	1, 3, 6, 7, 8, 17, 25, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 75, 76	N/A	Ground	**GND** pins are internally connected but a good (low impedance) external ground connection can improve RF performance: all **GND** pins must be externally connected to ground.
	V_BCKP	All	2	I/O	Real Time Clock supply input/output	**V_BCKP** = 2.3 V (typical) on LISA-U1 series **V_BCKP** = 1.8 V (typical) on LISA-U2 series generated by the module when **VCC** supply voltage is within valid operating range. See section 1.5.4
	V_INT	All	4	O	Digital Interfaces supply output	**V_INT** = 1.8V (typical) generated by the module when it is switched-on and the **RESET_N** (external reset input pin) is not forced to the low level. See section 1.5.5
	VSIM	All	50	O	SIM supply output	**VSIM** = 1.80 V typical or 2.90 V typical generated by the module according to the SIM card type. See section 1.8
RF	**ANT**	All	68	I/O	RF input/output for main Tx/Rx antenna	50 Ω nominal impedance. See section 1.7, section 2.4 and section 2.2.1.1
	ANT_DIV	LISA-U230	74	I	RF input for Rx diversity antenna	50 Ω nominal impedance See section 1.7, section 2.4 and section 2.2.1.1
SIM	**SIM_IO**	All	48	I/O	SIM data	Internal 4.7 kΩ pull-up to **VSIM**. Must meet SIM specifications. See section 1.8
	SIM_CLK	All	47	O	SIM clock	Must meet SIM specifications. See section 1.8
	SIM_RST	All	49	O	SIM reset	Must meet SIM specifications. See section 1.8
SPI	**SPI_MISO**	All	57	O	SPI Data Line Output	Module Output: module runs as an SPI slave. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. See section 1.9.4
	SPI_MOSI	All	56	I	SPI Data Line Input	Module Input: module runs as an SPI slave. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. Internal active pull-up to **V_INT** (1.8 V) enabled. See section 1.9.4

Function	Pin	Module	No	I/O	Description	Remarks
	SPI_SCLK	All	55	I	SPI Serial Clock Input	Module Input: module runs as an SPI slave. Idle low (CPOL=0). Internal active pull-down to **GND** enabled. See section 1.9.4
	SPI_SRDY	All	58	O	SPI Slave Ready Output	Module Output: module runs as an SPI slave. Idle low. See section 1.9.4
	SPI_MRDY	All	59	I	SPI Master Ready Input	Module Input: module runs as an SPI slave. Idle low. Internal active pull- down to **GND** enabled. See section 1.9.4
DDC	**SCL**	All	45	O	I^2C bus clock line	**Fixed open drain. External pull-up required.** See section 1.10
	SDA	All	46	I/O	I^2C bus data line	**Fixed open drain. External pull-up required.** See section 1.10
UART	**RxD**	All	16	O	UART data output	Circuit 104 (RxD) in ITU-T V.24. Provide access to the pin for FW update and debugging if the USB interface is connected to the application processor. See section 1.9.2
	TxD	All	15	I	UART data input	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to **V_INT** (1.8 V) enabled. Provide access to the pin for FW update and debugging if the USB interface is connected to the application processor. See section 1.9.2
	CTS	All	14	O	UART clear to send output	Circuit 106 (CTS) in ITU-T V.24. Provide access to the pin for debugging if the USB interface is connected to the application processor. See section 1.9.2
	RTS	All	13	I	UART ready to send input	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to **V_INT** (1.8 V) enabled. Provide access to the pin for debugging if the USB interface is connected to the application processor. See section 1.9.2
	DSR	All	9	O	UART data set ready output	Circuit 107 (DSR) in ITU-T V.24. See section 1.9.2
	RI	All	10	O	UART ring indicator output	Circuit 125 (RI) in ITU-T V.24. See section 1.9.2
	DTR	All	12	I	UART data terminal ready input	Circuit 108/2 (DTR) in ITU-T V.24. Internal active pull-up to **V_INT** (1.8 V) enabled. See section 1.9.2
	DCD	All	11	O	UART data carrier detect output	Circuit 109 (DCD) in ITU-T V.24. See section 1.9.2
GPIO	**GPIO1**	All	20	I/O	GPIO	See section 1.12
	GPIO2	All	21	I/O	GPIO	See section 1.12
	GPIO3	All	23	I/O	GPIO	See section 1.12
	GPIO4	All	24	I/O	GPIO	See section 1.12
	GPIO5	All	51	I/O	GPIO	See section 1.12
	GPIO6	LISA-U2	39	I/O	GPIO	See section 1.12
	GPIO7	LISA-U2	40	I/O	GPIO	See section 1.12
	GPIO8	LISA-U2	53	I/O	GPIO	See section 1.12
	GPIO9	LISA-U2	54	I/O	GPIO	See section 1.12
	GPIO10	LISA-U200-01 LISA-U230	55	I/O	GPIO	See section 1.12

Function	Pin	Module	No	I/O	Description	Remarks
	GPIO11	LISA-U200-01 LISA-U230	56	I/O	GPIO	See section 1.12
	GPIO12	LISA-U200-01 LISA-U230	57	I/O	GPIO	See section 1.12
	GPIO13	LISA-U200-01 LISA-U230	58	I/O	GPIO	See section 1.12
	GPIO14	LISA-U200-01 LISA-U230	59	I/O	GPIO	See section 1.12
USB	**VUSB_DET**	All	18	I	USB detect input	Input for VBUS (5 V typical) USB supply sense to enable USB interface. Provide access to the pin for FW update and debugging if the USB interface is not connected to the application processor. See section 1.9.3
	USB_D-	All	26	I/O	USB Data Line D-	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [8] are part of the USB pad driver and need not be provided externally. Provide access to the pin for FW update and debugging if the USB interface is not connected to the application processor. See section 1.9.3
	USB_D+	All	27	I/O	USB Data Line D+	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [8] are part of the USB pad driver and need not be provided externally. Provide access to the pin for FW update and debugging if the USB interface is not connected to the application processor. See section 1.9.3
System	**PWR_ON**	All	19	I	Power-on input	**PWR_ON** pin has high input impedance. Do not keep floating in noisy environment: external pull-up required. See section 1.6.1
	RESET_N	All	22	I	External reset input	Internal 10 kΩ pull-up to **V_BCKP**. See section 1.6.3
Analog Audio	**MIC_N**	LISA-U120 LISA-U130	39	I	Differential analog audio input (negative)	Differential analog input shared for all analog path modes: handset, headset, hands-free mode. Internal DC blocking capacitor. See section 1.11.1
	MIC_P	LISA-U120 LISA-U130	40	I	Differential analog audio input (positive)	Differential analog input shared for all analog path modes: handset, headset, hands-free mode. Internal DC blocking capacitor. See section 1.11.1
	SPK_P	LISA-U120 LISA-U130	53	O	Differential analog audio output (positive)	Differential analog audio output shared for all analog path modes: earpiece, headset and loudspeaker mode. See section 1.11.1
	SPK_N	LISA-U120 LISA-U130	54	O	Differential analog audio output (negative)	Differential analog audio output shared for all analog path modes: earpiece, headset and loudspeaker mode. See section 1.11.1
Digital Audio	**I2S_CLK**	LISA-U120 LISA-U130 LISA-U200-01 LISA-U230	43	I/O	First I²S clock	Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.

Function	Pin	Module	No	I/O	Description	Remarks
	I2S_RXD	LISA-U120 LISA-U130 LISA-U200-01 LISA-U230	44	I	First I^{2}S receive data	Internal active pull-down to GND enabled. Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.
	I2S_TXD	LISA-U120 LISA-U130 LISA-U200-01 LISA-U230	42	O	First I^{2}S transmit data	Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.
	I2S_WA	LISA-U120 LISA-U130 LISA-U200-01 LISA-U230	41	I/O	First I^{2}S word alignment	Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.
	I2S1_CLK	LISA-U200-01, LISA-U230	53	I/O	Second I^{2}S clock	Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.
	I2S1_RXD	LISA-U200-01 LISA-U230	39	I	Second I^{2}S receive data	Internal active pull-down to GND enabled. Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.
	I2S1_TXD	LISA-U200-01 LISA-U230	40	O	Second I^{2}S transmit data	Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.
	I2S1_WA	LISA-U200-01 LISA-U230	54	I/O	Second I^{2}S word alignment	Check device specifications to ensure compatibility to module supported modes. See section 1.11.2.
	CODEC_CLK	LISA-U200-01 LISA-U230	52	O	Clock output	Digital clock output for external audio codec See section 1.11.2.
Reserved	**RSVD**	All	5	N/A	RESERVED pin	This pin must be connected to ground See section 1.13
	RSVD	LISA-U1 LISA-U200-00	52	N/A	RESERVED pin	Pad disabled See section 1.13
	RSVD	LISA-U1 LISA-U200	74	N/A	RESERVED pin	Do not connect See section 1.13
	RSVD	LISA-U100 LISA-U110 LISA-U200-00	43	N/A	RESERVED pin	Pad disabled See section 1.13
	RSVD	LISA-U100 LISA-U110 LISA-U200-00	44	N/A	RESERVED pin	Pad disabled See section 1.13
	RSVD	LISA-U100 LISA-U110 LISA-U200-00	42	N/A	RESERVED pin	Pad disabled See section 1.13
	RSVD	LISA-U100 LISA-U110 LISA-U200-00	41	N/A	RESERVED pin	Pad disabled See section 1.13
	RSVD	LISA-U100 LISA-U110	39	N/A	RESERVED pin	Do not connect See section 1.13
	RSVD	LISA-U100 LISA-U110	40	N/A	RESERVED pin	Do not connect See section 1.13
	RSVD	LISA-U100 LISA-U110	53	N/A	RESERVED pin	Do not connect See section 1.13
	RSVD	LISA-U100 LISA-U110	54	N/A	RESERVED pin	Do not connect See section 1.13

Table 4: LISA-U series modules pin definition, grouped by function

1.4 Operating modes

LISA-U series modules have several operating modes. Table 5 summarizes the various operating modes and provides general guidelines for operation.

Operating Mode	Description	Features / Remarks	Transition condition
General Status: Power-down			
Not-Powered Mode	**VCC** supply not present or below operating range. Microprocessor switched off (not operating). RTC only operates if supplied through **V_BCKP** pin.	Module is switched off. Application interfaces are not accessible. Internal RTC timer operates only if a valid voltage is applied to **V_BCKP** pin.	Module cannot be switched on by a low level on the **PWR_ON** input, by a rising edge on the **RESET_N** input, or by a preset RTC alarm. Module can be switched on applying **VCC** supply.
Power-Off Mode	**VCC** supply within operating range. Microprocessor switched off (not operating). Only RTC runs.	Module is switched off: normal shutdown by AT+CPWROFF command (refer to u-blox AT Commands Manual [3]), or by **PWR_ON** held low for more than 1 s (LISA-U2xx-01 only). Application interfaces are not accessible. Only the internal RTC timer in operation.	Module can be switched on by a low level on the **PWR_ON** input, by a rising edge on the **RESET_N** input, or by a preset RTC alarm.
General Status: Normal Operation			
Idle-Mode	Microprocessor runs with 32 kHz as reference oscillator. Module does not accept data signals from an external device.	If power saving is enabled, the module automatically enters idle-mode whenever possible. Application interfaces are disabled. If hardware flow control is enabled, the **CTS** line to ON state indicates that the module is in active mode and the UART interface is enabled: the line is driven in the OFF state when the module is not prepared to accept data by the UART interface. If hardware flow control is disabled, the **CTS** line is fixed to ON state. Module by default is not set to automatically enter idle-mode whenever possible, unless power saving configuration is enabled by appropriate AT command (refer to u-blox AT Commands Manual [3], AT+UPSV).	Module enters automatically idle-mode when power saving is enabled and there is no activity for the defined time interval: • Module registered with the network and power saving enabled. Periodically wakes up to active mode to monitor the paging channel for the paging block reception according to network indication • Module not registered with the network and power saving is enabled. Periodically wakes up to monitor external activity Module wakes up from idle-mode to active-mode in the following events: • Incoming voice or data call • RTC alarm occurs • Data received on UART interface (refer to 1.9.2) • **RTS** input line set to the ON state by the DTE if the AT+UPSV=2 command is sent to the module (refer to 1.9.2) • USB detection, applying 5 V (typ.) to the **VUSB_DET** pin • The connected USB host forces a remote wakeup of the module as USB device (refer to 1.9.3) • The connected SPI master indicates to the module that it is ready for transmission or reception, by the SPI/IPC **SPI_MRDY** input signal (refer to 1.9.4)

Operating Mode	Description	Features / Remarks	Transition condition
Active-Mode	Microprocessor runs with 26 MHz as reference oscillator. The module is prepared to accept data signals from an external device.	Module is switched on and is fully active. The application interfaces are enabled, unless power saving configuration is enabled by the AT+UPSV command (refer to sections 1.9.2.3, 1.9.3.2, 1.9.4.2 and u-blox AT Commands Manual [3]). Power saving is not enabled by default: it can be enabled by the AT+UPSV command (see u-blox AT Commands Manual [3]).	If power saving is enabled, the module automatically enters idle-mode and application interfaces are disabled whenever possible (refer to sections 1.9.2.3, 1.9.3.2, 1.9.4.2 and u-blox AT Commands Manual [3], AT+UPSV).
Connected-Mode	Voice or data call enabled. Microprocessor runs with 26 MHz as reference oscillator. The module is prepared to accept data signals from an external device.	The module is switched on and a voice call or a data call (2G/3G) is in progress. Module is fully active. The application interfaces are enabled, unless power saving configuration is enabled by the AT+UPSV command (see section 1.9.2.3, 1.9.3.2, 1.9.4.2 and the u-blox AT Commands Manual [3]).	When call terminates, the module returns to the active operating mode.

Table 5: Module operating modes summary

Transition between the different modes is described in Figure 3.

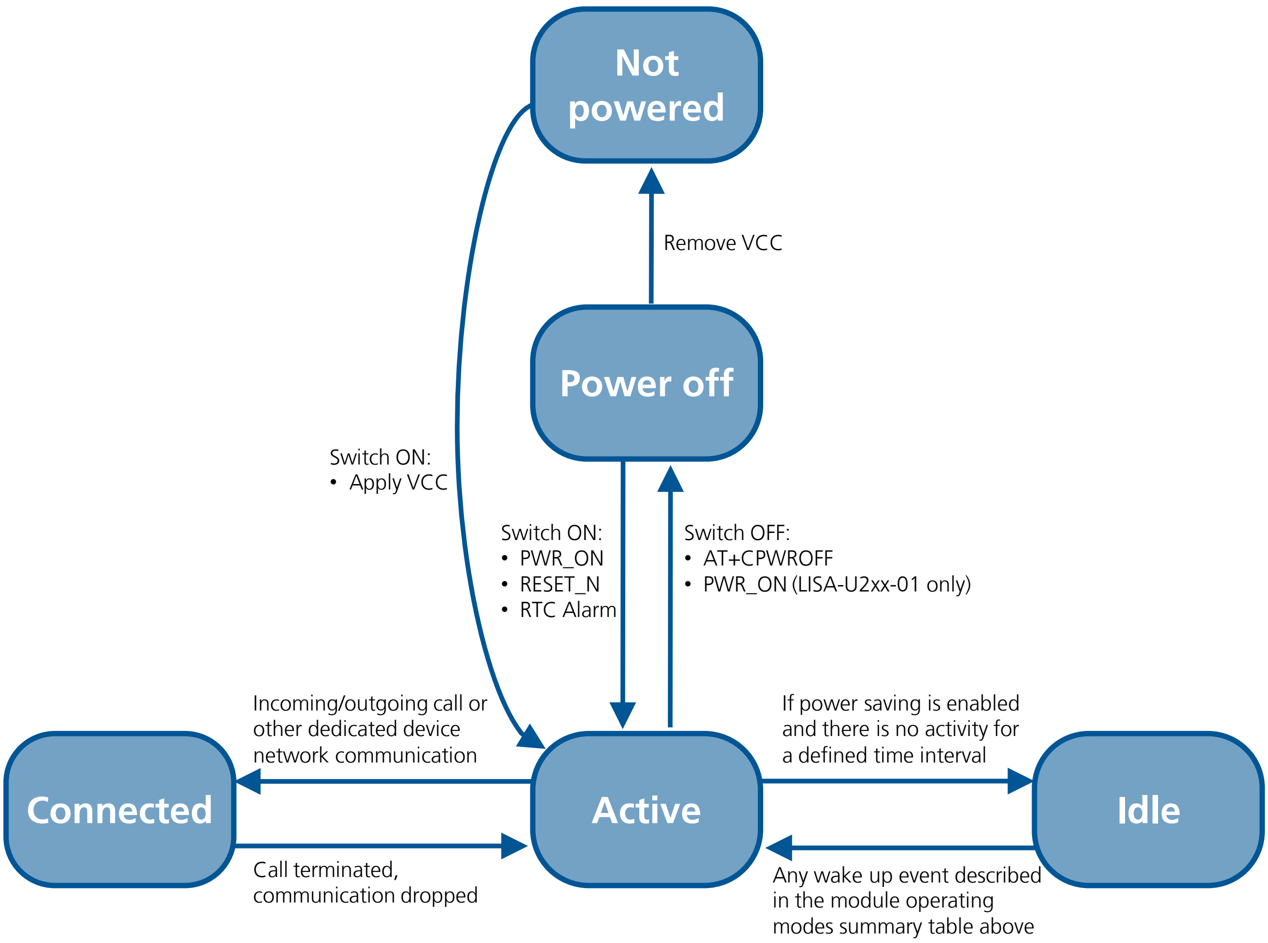

Figure 3: Operating modes transition

1.5 Power management

1.5.1 Power supply circuit overview

LISA-U series modules feature a power management concept optimized for the most efficient use of supplied power. This is achieved by hardware design utilizing a power efficient circuit topology (Figure 4), and by power management software controlling the module's power saving mode.

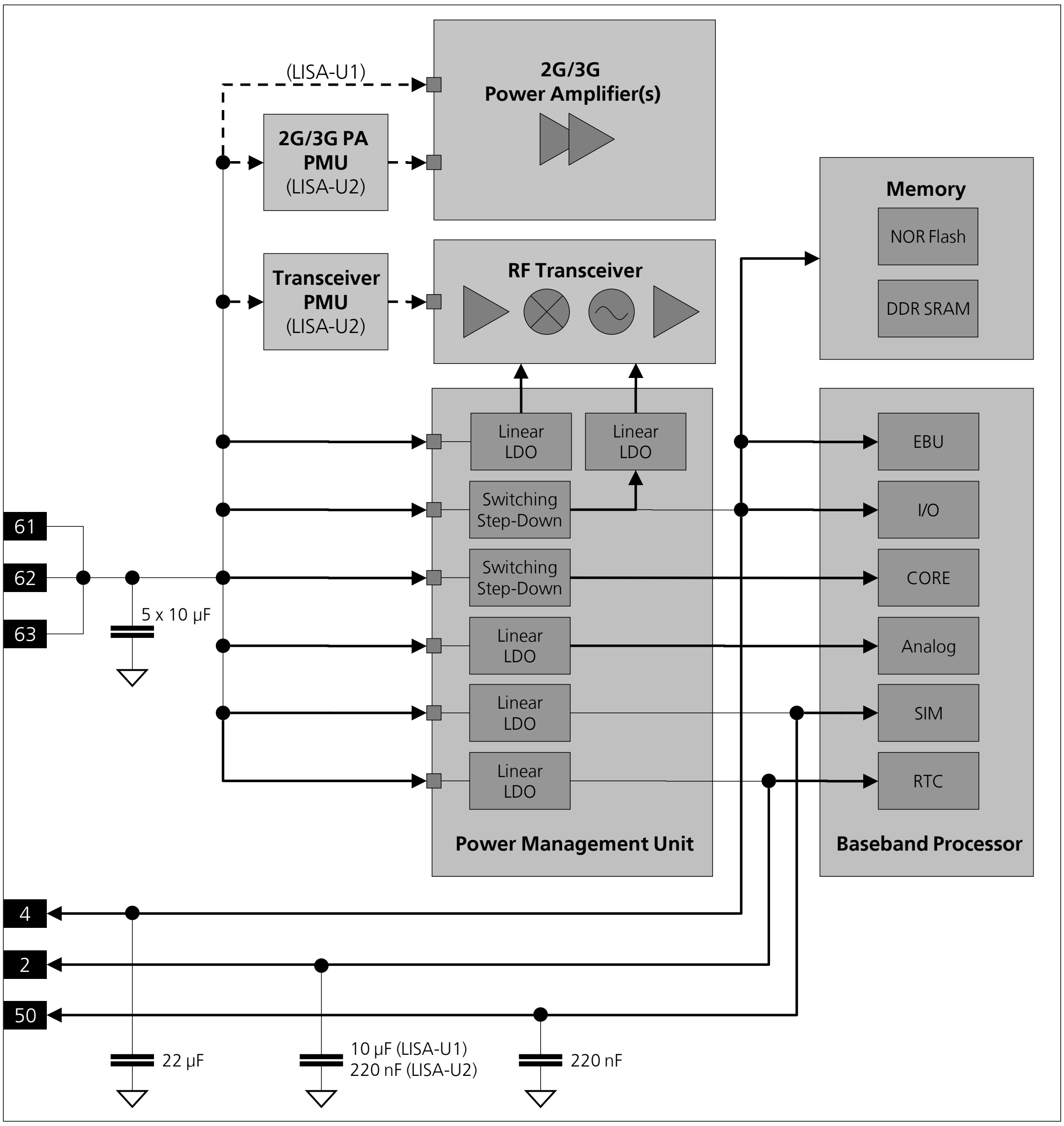

Figure 4: LISA-U series power management simplified block diagram

Pins with supply function are reported in Table 6, Table 11 and Table 14.

LISA-U series modules must be supplied via the **VCC** pins. There is only one main power supply input, available on the three **VCC** pins that must be all connected to the external power supply

The **VCC** pins are directly connected to the RF power amplifiers and to the integrated Power Management Unit (PMU) within the module: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators.

V_BCKP is the Real Time Clock (RTC) supply. When the **VCC** voltage is within the valid operating range, the internal PMU supplies the Real Time Clock and the same supply voltage will be available to the **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (for example, during not powered mode), the Real Time Clock can be externally supplied via the **V_BCKP** pin (see section 1.5.4).

When a 1.8 V or a 3 V SIM card type is connected, LISA-U series modules automatically supply the SIM card via the **VSIM** pin. Activation and deactivation of the SIM interface with automatic voltage switch from 1.8 to 3 V is implemented, in accordance to the ISO-IEC 7816-3 specifications.

The same voltage domain used internally to supply the digital interfaces is also available on the **V_INT** pin, to allow more economical and efficient integration of the LISA-U series modules in the final application.

The integrated Power Management Unit also provides the control state machine for system start up and system reset control.

1.5.2 Module supply (VCC)

The LISA-U series modules must be supplied through the **VCC** pins by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some orders of magnitude, especially due to surging consumption profile of the GSM system (described in the section 1.5.3). It is important that the system power supply circuit is able to support peak power (refer to LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2] for the detailed specifications).

Name	Description	Remarks
VCC	Module power supply input	**VCC** pins are internally connected, but all the available pads must be connected to the external supply in order to minimize the power loss due to series resistance. Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided must always be above the minimum limit of the operating range. Consider that during a GSM call there are large current spikes in connected mode.
GND	Ground	**GND** pins are internally connected but a good (low impedance) external ground can improve RF performance: all available pads must be connected to ground.

Table 6: Module supply pins

☞ **VCC** pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level can be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.

The voltage provided to the **VCC** pins must be within the normal operating range limits as specified in the LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]. Complete functionality of the module is only guaranteed within the specified minimum and maximum **VCC** voltage normal operating range.

☞ The module cannot be switched on if the **VCC** voltage value is below the specified normal operating range minimum limit. Ensure that the input voltage at **VCC** pins is above the minimum limit of the normal operating range for more than 3 s after the start of the module switch-on sequence.

When LISA-U series modules are in operation, the voltage provided to **VCC** pins can go outside the normal operating range limits but must be within the extended operating range limits specified in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]. Occasional deviations from the ETSI specifications may occur when the input voltage at **VCC** pins is outside the normal operating range and is within the extended operating range.

☞ LISA-U series modules switch off when **VCC** voltage value drops below the specified extended operating range minimum limit: ensure that the input voltage at **VCC** pins never drops below the minimum limit of the extended operating range when the module is switched on, not even during a GSM transmit burst, where the current consumption can rise up to maximum peaks of 2.5 A in case of a mismatched antenna load.

⚠ **Operation above the normal operating range maximum limit is not recommended and extended exposure beyond it may affect device reliability.**

⚠ **Stress beyond the VCC absolute maximum ratings can cause permanent damage to the module: if necessary, voltage spikes beyond VCC absolute maximum ratings must be restricted to values within the specified limits by using appropriate protection.**

☞ When designing the power supply for the application, pay specific attention to power losses and transients. The DC power supply must be able to provide a voltage profile to the **VCC** pins with the following characteristics:

- Voltage drop during transmit slots must be lower than 400 mV
- No undershoot or overshoot at the start and at the end of transmit slots
- Voltage ripple during transmit slots must be minimized:

  lower than 70 mVpp if $f_{ripple} \leq 200$ kHz

  lower than 10 mVpp if 200 kHz $< f_{ripple} \leq 400$ kHz

  lower than 2 mVpp if $f_{ripple} > 400$ kHz

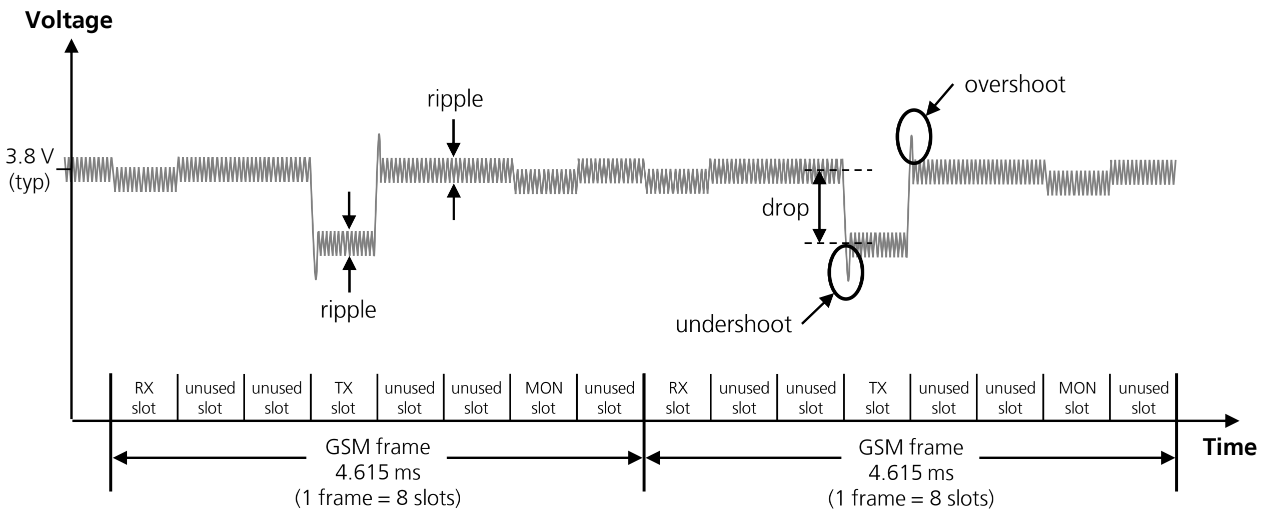

Figure 5: Description of the VCC voltage profile versus time during a GSM call

☞ Any degradation in power supply performance (due to losses, noise or transients) will directly affect the RF performance of the module since the single external DC power source indirectly supplies all the digital and analog interfaces, and also directly supplies the RF power amplifier (PA).

☞ The voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms. This **VCC** slope allows a proper switch on of the module when the voltage rises to the **VCC** normal operating range from a voltage of less than 2.25 V. If the external supply circuit cannot raise the **VCC** voltage from 2.5 V to 3.2 V within 1 ms **RESET_N** should be kept low during **VCC** rising edge, so that the module will switch on releasing the **RESET_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal operating range.

1.5.2.1 VCC application circuits

LISA-U series modules must be supplied through the **VCC** pins by one (and only one) proper DC power supply that must be one of the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

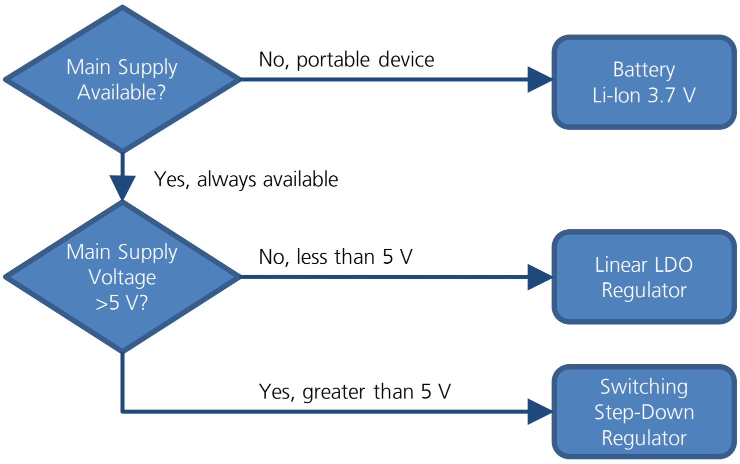

Figure 6: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the LISA-U series modules operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator will diminish the benefit of voltage step-down and no true advantage will be gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they will dissipate a considerable amount of energy in thermal power.

If LISA-U series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided.

The use of primary (not rechargeable) battery is uncommon, since the most cells available are seldom capable of delivering the burst peak current for a GSM call due to high internal resistance.

Keep in mind that the use of batteries requires the implementation of a suitable charger circuit (not included in LISA-U series modules). The charger circuit should be designed in order to prevent over-voltage on **VCC** beyond the upper limit of the absolute maximum rating.

The following sections highlight some design aspects for each of the supplies listed above.

Switching regulator

The characteristics of the switching regulator connected to **VCC** pins should meet the following requirements:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering 2.5 A current pulses with 1/8 duty cycle to the **VCC** pins
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile
- **High switching frequency:** for best performance and for smaller applications select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile and therefore negatively impact GSM modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple on **VCC**, but adds extra voltage drop due to resistive losses on series inductors
- **PWM mode operation**: select preferably regulators with Pulse Width Modulation (PWM) mode. While in active mode Pulse Frequency Modulation (PFM) mode and PFM/PWM mode transitions must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators able to switch between low ripple PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition occurs when the module changes status from idle/active mode to connected mode (where current consumption increases to a value greater than 100 mA): it is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 60 mA)
- **Output voltage slope**: the use of the soft start function provided by some voltage regulator must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module

Figure 7 and the components listed in Table 7 show an example of a high reliability power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering 2.5 A current pulses with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz. The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V supply to the typical 3.8 V value of the **VCC** supply.

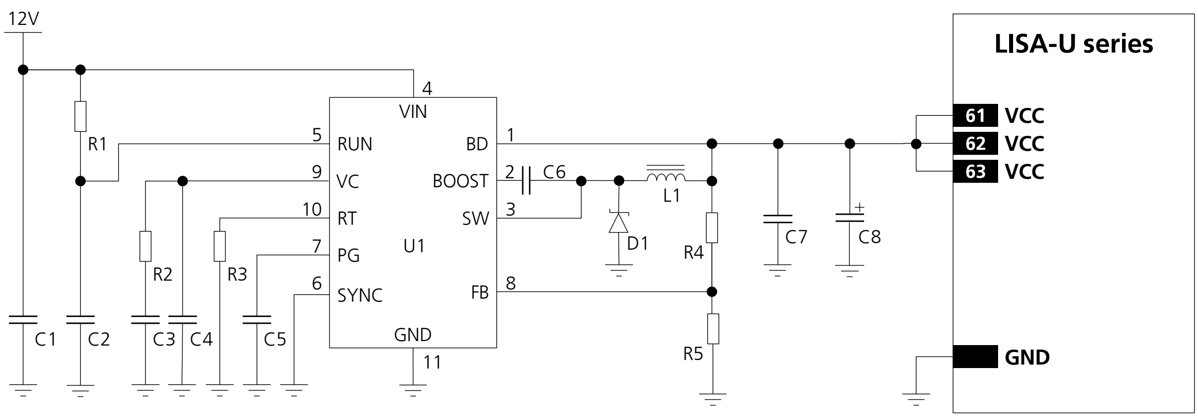

Figure 7: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 kΩ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	22 kΩ Resistor 0402 5% 0.1 W	2322-705-87223-L - Yageo
R4	390 kΩ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 kΩ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 7: Suggested components for the VCC voltage supply application circuit using a step-down regulator

Low Drop-Out (LDO) linear regulator

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following requirements:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pins and of delivering 2.5 A current pulses with 1/8 duty cycle
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator)
- **Output voltage slope**: the use of the soft start function provided by some voltage regulators must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module

Figure 8 and the components listed in Table 8 show an example of a power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering 2.5 A current pulses, with proper power handling capability. The use of a linear regulator is suggested when the difference from the available supply rail and the VCC value is low: linear regulators provide high efficiency when transforming a 5 V supply to the 3.8 V typical value of the VCC supply.

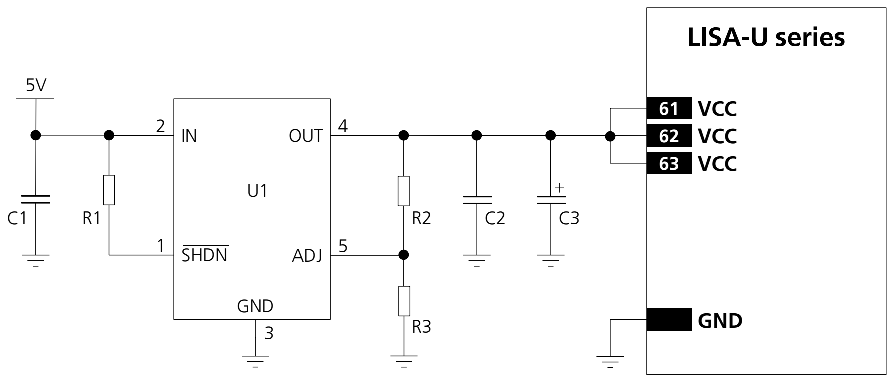

Figure 8: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C3	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 8: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

Rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following requirements:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its output circuit must be capable of delivering 2.5 A current pulses with 1/8 duty-cycle to the **VCC** pins and must be capable of delivering a DC current greater than the module maximum average current consumption to **VCC** pins. The maximum pulse discharge current and the maximum DC discharge current are not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts

Primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following requirements:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its output circuit must be capable of delivering 2.5 A current pulses with 1/8 duty-cycle to the **VCC** pins and must be capable of delivering a DC current greater than the module maximum average current consumption at the **VCC** pins. The maximum pulse and the maximum DC discharge current is not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts

Additional recommendations for the VCC supply application circuits

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible in order to minimize power losses.

Three pins are allocated for **VCC** supply. Another twenty pins are designated for **GND** connection. Even if all the **VCC** pins and all the **GND** pins are internally connected within the module, it is recommended to properly connect all of them to supply the module in order to minimize series resistance losses.

To avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a GSM call (when current consumption on the **VCC** supply can rise up to as much as 2.5 A in the worst case), place a capacitor with large capacitance (more than 100 µF) and low ESR near the **VCC** pins, for example:

- 330 µF capacitance, 45 mΩ ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

The use of very large capacitors (i.e. greater then 1000 µF) on the **VCC** line and the use of the soft start function provided by some voltage regulators must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch on of the module.

To reduce voltage ripple and noise, place the following near the **VCC** pins:

- 100 nF capacitor (e.g Murata GRM155R61A104K) to filter digital logic noise from clocks and data sources
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 10 pF capacitor (e.g. Murata GRM1555C1E100J) to filter EMI in the 1800 / 1900 / 2100 MHz bands
- 39 pF capacitor (e.g. Murata GRM1555C1E390J) to filter EMI in the 850 / 900 MHz bands

☞ Figure 9 shows the complete configuration but the mounting of each single component depends on the application design.

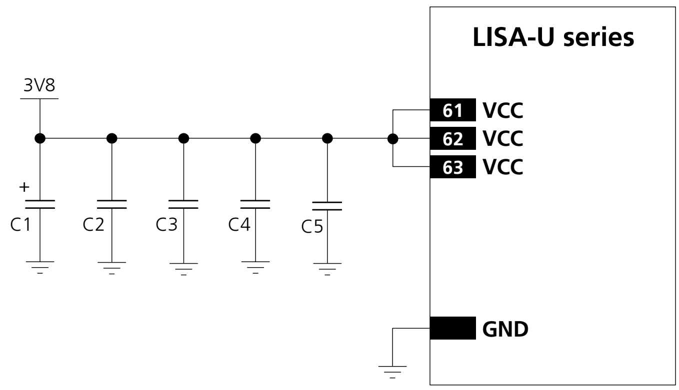

Figure 9: Suggested schematic design to reduce voltage ripple and noise and to avoid undershoot/ overshoot on voltage drops

Reference	Description	Part Number - Manufacturer
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	39 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E390JA01 - Murata
C5	10 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E100JA01 - Murata

Table 9: Suggested components to reduce voltage ripple and noise and to avoid undershoot/ overshoot on voltage drops

External battery charging application circuit

LISA-U series modules don't have an on-board charging circuit. An example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell, is provided in Figure 10.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the **VCC** supply input of LISA-U series module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA)
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Alternatively the L6924U, providing input voltage range up to 12 V, can charge from an AC wall adapter. When a current-limited adapter is used, it can operate in quasi-pulse mode, reducing power dissipation.

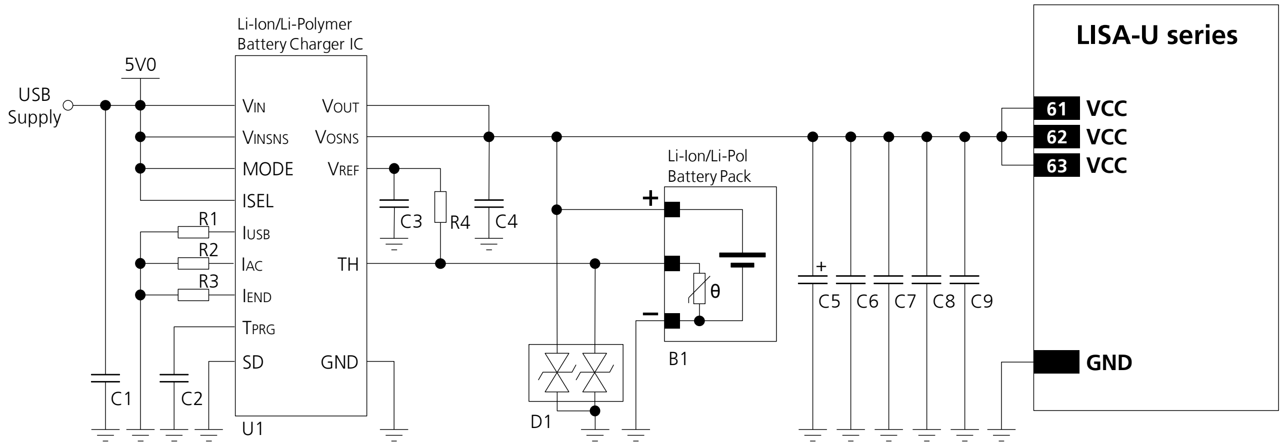

Figure 10: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 ΩNTC	Various manufacturer
C1, C4	1 µF Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	39 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E390JA01 - Murata
C9	10 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E100JA01 - Murata
D1	Low Capacitance ESD Protection	USB0002RP or USB0002DP - AVX
R1, R2	24 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0724KL - Yageo Phycomp
R3	3.3 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K3L - Yageo Phycomp
R4	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC for USB port and AC Adapter	L6924U - STMicroelectronics

Table 10: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit

1.5.3 Current consumption profiles

During operation, the current drawn by the LISA-U series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the high peak of current consumption during GSM transmitting bursts at maximum power level in 2G connected mode, to continuous high current drawn in UMTS connected mode, to the low current consumption during power saving in idle-mode.

1.5.3.1 2G connected mode

When a GSM call is established, the **VCC** consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. If the module is transmitting in GSM talk mode in the GSM 850 or in the E-GSM 900 band and at the maximum RF power control level (approximately 2 W or 33 dBm in the allocated transmit slot/burst) the current consumption can reach up to 2500 mA (with a highly unmatched antenna) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access). If the module is in GSM connected mode in the DCS 1800 or in the PCS 1900 band, the current consumption figures are lower than the one in the GSM 850 or in the E-GSM 900 band, due to 3GPP transmitter output power specifications (refer to refer to LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]).

During a GSM call, current consumption is in the order of 60-130 mA in receiving or in monitor bursts and is about 10-40 mA in the inactive unused bursts (low current period). The more relevant contribution to determine the average current consumption is set by the transmitted power in the transmit slot.

An example of current consumption profile of the data module in GSM talk mode is shown in Figure 11.

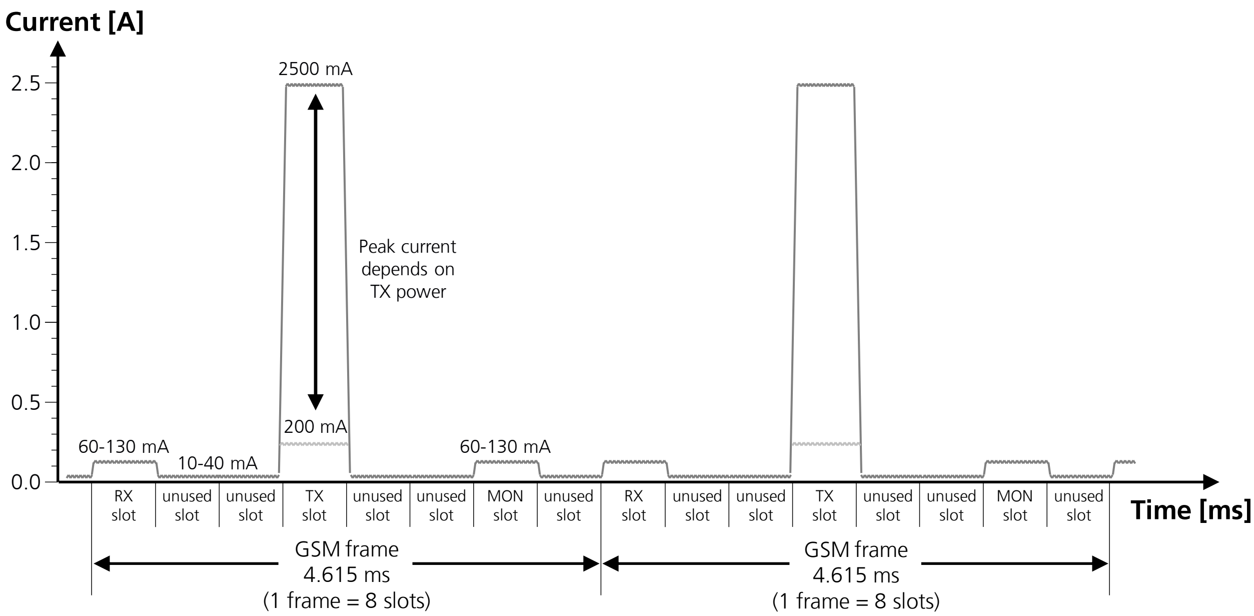

Figure 11: VCC current consumption profile versus time during a GSM call (1 TX slot, 1 RX slot), with VCC=3.8 V

When a GPRS connection is established there is a different VCC current consumption profile also determined by the transmitting and receiving bursts. In contrast to a GSM call, during a GPRS connection more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions, which set the peak current consumption, but following the GPRS specifications the maximum transmitted RF power is reduced if more than one slot is used to transmit, so the maximum peak of current consumption is not as high as can be in case of a GSM call.

If the module transmits in GPRS class 12 or class 33 connected mode in the GSM 850 or in the E-GSM 900 band at the maximum power control level, the current consumption can reach up to 1600 mA (with unmatched antenna). This happens for 2.307 ms (width of the 4 transmit slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/2 duty cycle, according to GSM TDMA. If the module is in GPRS connected mode in the DCS 1800 or in the PCS 1900 band, the current consumption figures are lower than in the GSM 850 or in the E-GSM 900 band, due to 3GPP transmitter output power specifications (refer to LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]).

Figure 12 reports the current consumption profiles in GPRS class 12 connected mode, in the GSM 850 or in the E-GSM 900 band, with 4 slots used to transmit and 1 slot used to receive.

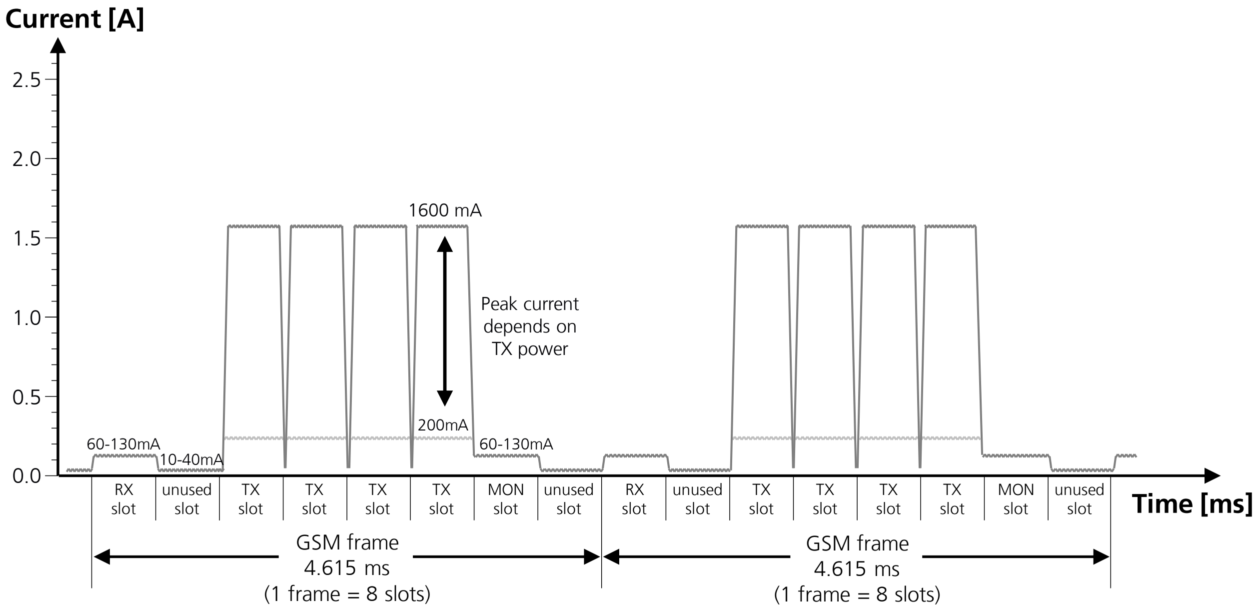

Figure 12: VCC current consumption profile versus time during a GPRS/EDGE connection (4TX slots, 1 RX slot), with VCC=3.8 V

In case of EDGE connections the VCC current consumption profile is very similar to the GPRS current profile, so the image shown in Figure 12, representing the current consumption profile in GPRS class 12 connected mode, is valid for the EDGE class 12 connected mode as well.

LISA-U2 series modules support GPRS and EDGE class 33: up to 4 slots can be used to transmit, as in the class 12 mode, and up to 2 slots can be used to receive in the same frame since up to 6 slots can be used in total. So, the VCC current consumption figures in GPRS and EDGE class 33 connected modes are similar to the current profile in GPRS and EDGE class 12 connected modes, since the same number of transmit slots are used.

1.5.3.2 3G connected mode

During a 3G connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation with the Wideband Code Division Multiple Access (WCDMA). The current consumption depends again on output RF power, which is always regulated by network commands. These power control commands are logically divided into a slot of 666 µs, thus the rate of power change can reach a maximum rate of 1.5 kHz. There are no high current peaks as in the 2G connection, since transmission and reception are continuously enabled due to FDD WCDMA implemented in the 3G that differs from the TDMA implemented in the 2G case. In the worst scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the current drawn by the module at the VCC pins is in the order of continuous 500-800 mA (refer to LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2] for detailed values). Even at lowest output RF power (approximately 0.01 µW or -50 dBm), the current still remains in the order of 200 mA due to module baseband processing and transceiver activity.

An example of current consumption profile of the data module in UMTS/HSxPA continuous transmission mode is shown in Figure 13.

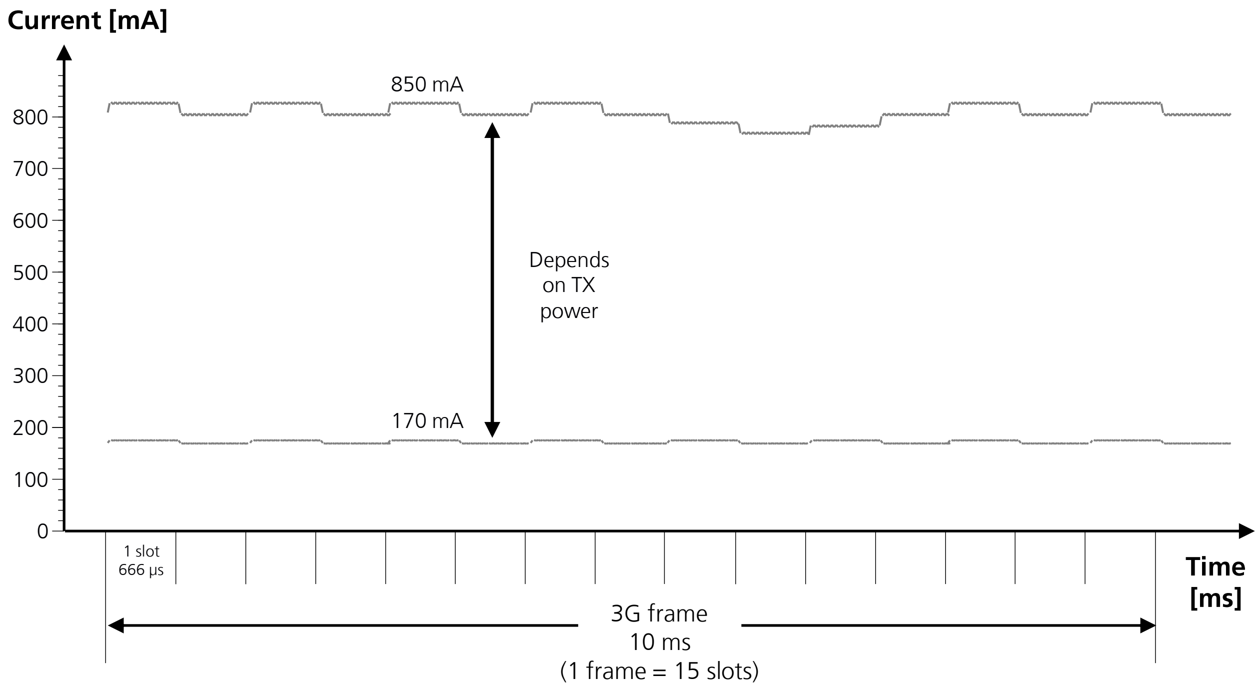

Figure 13: VCC current consumption profile versus time during a UMTS/HSPA connection, with VCC=3.8 V

When a packet data connection is established, the actual current profile depends on the amount of transmitted packets; there might be some periods of inactivity between allocated slots where current consumption drops about 100 mA. Alternatively, at higher data rates the transmitted power is likely to increase due to the higher quality signal required by the network to cope with enhanced data speed.

1.5.3.3 2G and 3G cyclic idle/active mode (power saving enabled)

The power saving configuration is by default disabled, but it can be enabled using the appropriate AT command (refer to u-blox AT Commands Manual [3], AT+UPSV command). When power saving is enabled, the module automatically enters idle-mode whenever possible.

When power saving is enabled, the module is registered or attached to a network and a voice or data call is not enabled, the module automatically enters idle-mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to GSM system requirements. When the module monitors the paging channel, it wakes up to active mode, to enable the reception of paging block. In between, the module switches to idle-mode. This is known as GSM discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 26 MHz used in active-mode.

The time period between two paging block receptions is defined by the network (2G or 3G). This is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell.

In case of 2G network, the time interval between two paging block receptions can be from 470.76 ms (DRX = 2, i.e. width of 2 GSM multiframes = 2 x 51 GSM frames = 2 x 51 x 4.615 ms) up to 2118.42 ms (DRX = 9, i.e. width of 9 GSM multiframes = 9 x 51 frames = 9 x 51 x 4.615 ms).

In case of 3G network, the principle is similar but time interval changes from 640 ms (DRX = 6, i.e. the width of 2^6 x 3G frames = 64 x 10 ms = 640 ms) up to 5120 ms (DRX = 9, i.e. width of 2^9 x 3G frames = 512 x 10 ms = 5120 ms).

An example of a module current consumption profile is shown in Figure 14: the module is registered with the network (2G or 3G), automatically enters idle-mode and periodically wakes up to active mode to monitor the paging channel for paging block reception.

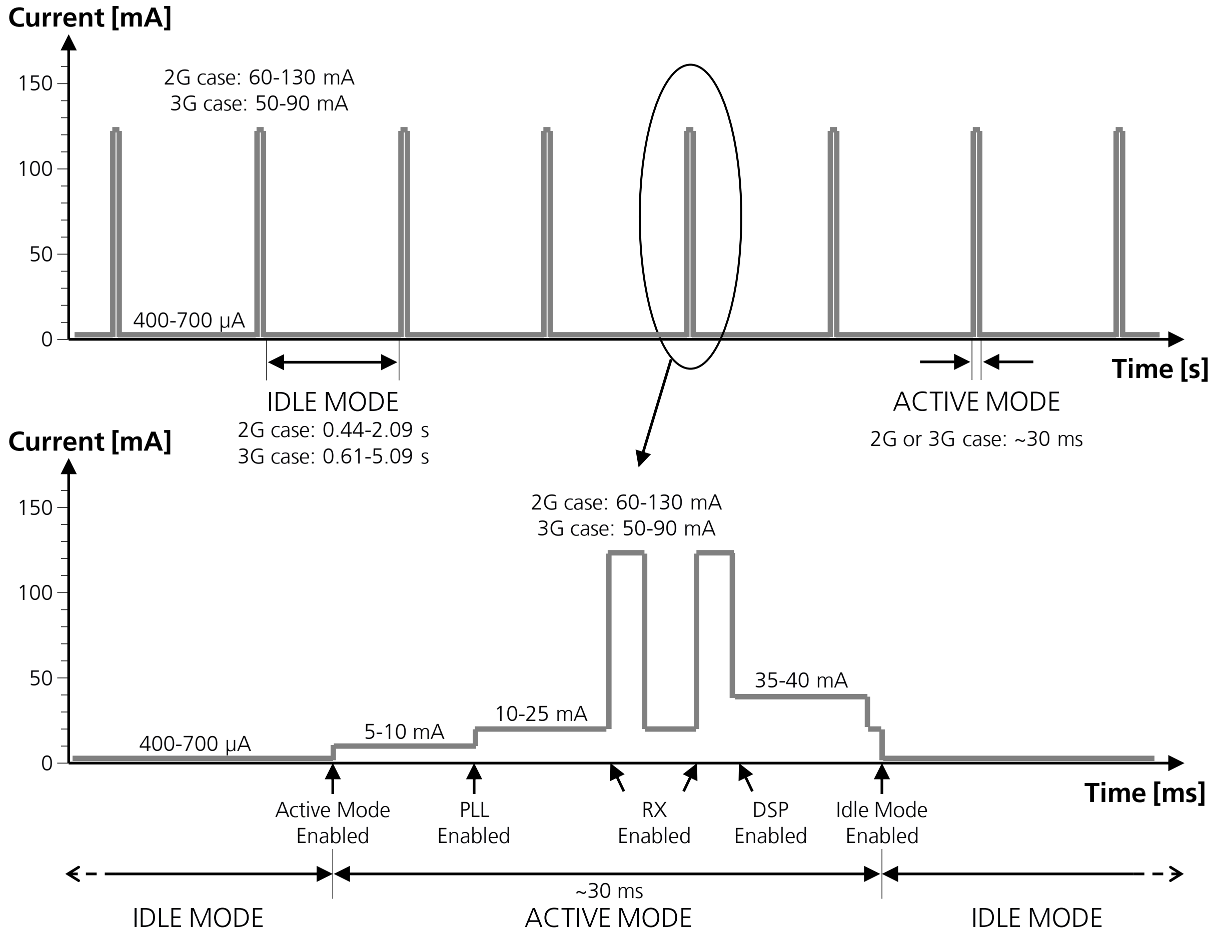

Figure 14: Description of VCC current consumption profile versus time when the module is registered with 2G or 3G networks: the module is in idle-mode and periodically wakes up to active mode to monitor the paging channel for paging block reception

1.5.3.4 2G and 3G fixed active mode (power saving disabled)

Power saving configuration is by default disabled, or it can be disabled using the appropriate AT command (refer to u-blox AT Commands Manual [3], AT+UPSV command). When power saving is disabled, the module doesn't automatically enter idle-mode whenever possible: the module remains in active mode.

The module processor core is activated during active-mode, and the 26 MHz reference clock frequency is used.

An example of the current consumption profile of the data module when power saving is disabled is shown in Figure 15: the module is registered with the network, active-mode is maintained, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception.

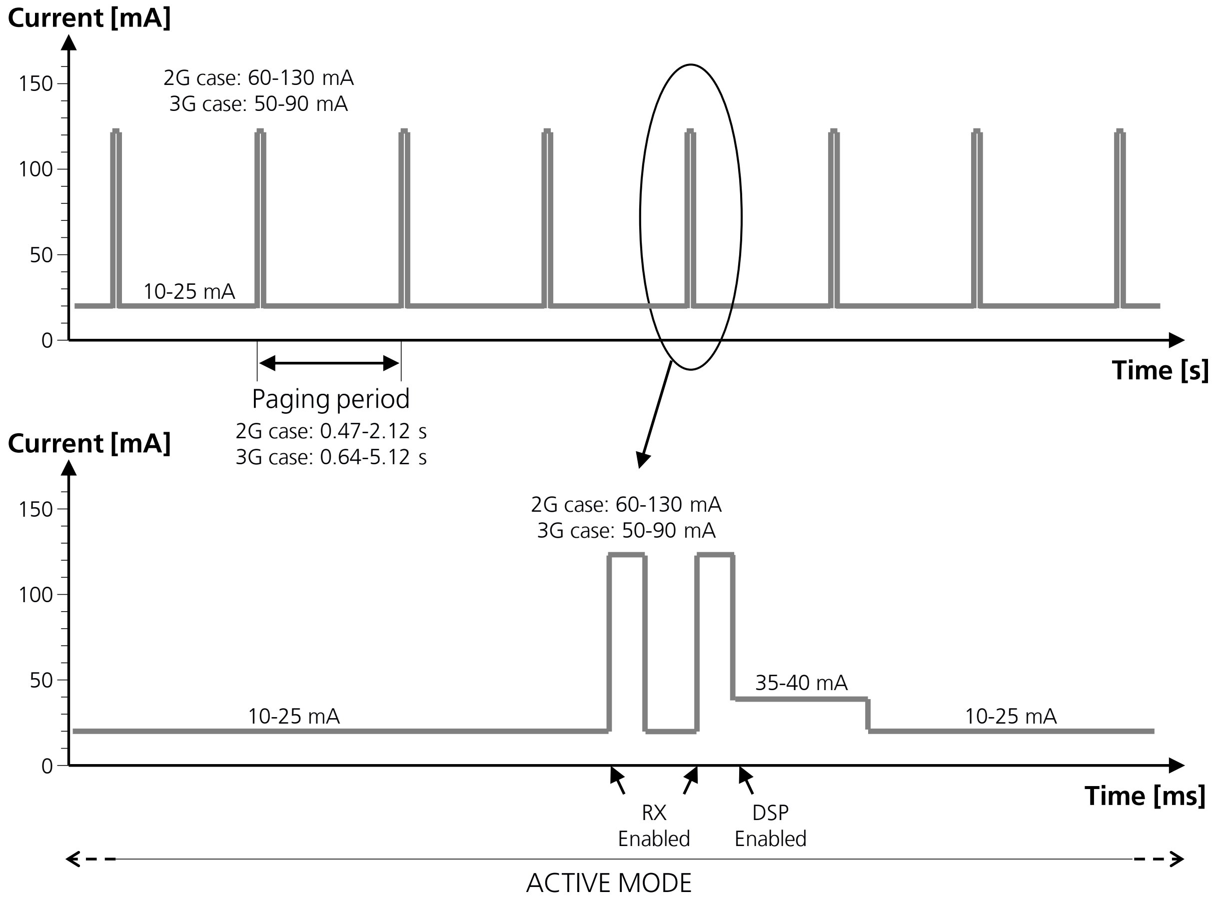

Figure 15: Description of the VCC current consumption profile versus time when power saving is disabled: the active-mode is always held, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception

1.5.4 RTC Supply (V_BCKP)

The **V_BCKP** pin connects the supply for the Real Time Clock (RTC) and Power-On / Reset internal logic. This supply domain is internally generated by a linear regulator integrated in the Power Management Unit. The output of this linear regulator is always enabled when the main voltage supply provided to the module through **VCC** is within the valid operating range, with the module switched-off or powered-on.

Name	Description	Remarks
V_BCKP	Real Time Clock supply	**V_BCKP** output voltage = 2.3 V (typical) on LISA-U1 series **V_BCKP** output voltage = 1.8 V (typical) on LISA-U2 series Generated by the module to supply Real Time Clock when VCC supply voltage is within valid operating range.

Table 11: Real Time Clock supply pin

☞ The **V_BCKP** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.

The RTC provides the time reference (date and time) of the module, also in power-off mode, when the **V_BCKP** voltage is within its valid range (specified in the Input characteristics of Supply/Power pins table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]). The RTC timing is normally used to set the wake-up interval during idle-mode periods between network paging, but is able to provide programmable alarm functions by means of the internal 32.768 kHz clock.

The RTC can be supplied from an external back-up battery through the **V_BCKP**, when the main voltage supply is not provided to the module through **VCC**. This lets the time reference (date and time) run until the **V_BCKP** voltage is within its valid range, even when the main supply is not provided to the module.

The RTC oscillator doesn't necessarily stop operation (i.e. the RTC counting doesn't necessarily stop) when **V_BCKP** voltage value drops below the specified operating range minimum limit (1.00 V): the RTC value read after a system restart could be not reliable as explained in the following Table 12.

V_BCKP voltage value	RTC value reliability	Notes
1.00 V < **V_BCKP** < 1.90 V (LISA-U2 series) 1.00 V < **V_BCKP** < 2.50 V (LISA-U1 series)	RTC oscillator doesn't stop operation RTC value read after a restart of the system is reliable	**V_BCKP** within operating range
0.05 V < **V_BCKP** < 1.00 V	RTC oscillator doesn't necessarily stop operation RTC value read after a restart of the system is not reliable	**V_BCKP** below operating range
0.00 V < **V_BCKP** < 0.05 V	RTC oscillator stops operation RTC value read after a restart of the system is reliable	**V_BCKP** below operating range

Table 12: RTC value reliability as function of V_BCKP voltage value

Consider that the module cannot switch on if a valid voltage is not present on **VCC** even when the RTC is supplied through **V_BCKP** (meaning that **VCC** is mandatory to switch-on the module).

The RTC has very low power consumption, but is highly temperature dependent. For example at 25°C, with the **V_BCKP** voltage equal to the typical output value, the power consumption is approximately 2 µA (refer to the Input characteristics of Supply/Power pins table in the LISA-U1 series Data Sheet [1] and in the LISA-U2 series Data Sheet [2] for the detailed specification), whereas at 70°C and an equal voltage the power consumption increases to 5-10 µA.

☞ The internal regulator for **V_BCKP** is optimized for low leakage current and very light loads. It is not recommended to use **V_BCKP** to supply external loads.

If **V_BCKP** is left unconnected and the module main voltage supply is removed from **VCC**, the RTC is supplied from the bypass capacitor mounted inside the module. However, this capacitor is not able to provide a long buffering time: within few milliseconds the voltage on **V_BCKP** will go below the valid range (1 V min). This has no impact on wireless connectivity, as all the functionalities of the module do not rely on date and time setting.

☞ Leave **V_BCKP** unconnected if the RTC is not required when the **VCC** supply is removed. The date and time will not be updated when **VCC** is disconnected. If **VCC** is always supplied, then the internal regulator is supplied from the main supply and there is no need for an external component on **V_BCKP**.

If RTC is required to run for a time interval of T [s] at 25°C when **VCC** supply is removed, place a capacitor with a nominal capacitance of C [µF] at the **V_BCKP** pin. Choose the capacitor using the following formula:

C [µF] = (Current_Consumption [µA] x T [s]) / Voltage_Drop [V]

= 1.92 x T [s] for LISA-U1 series

= 2.50 x T [s] for LISA-U2 series

For example, a 100 µF capacitor (such as the Murata GRM43SR60J107M) can be placed at **V_BCKP** to provide a long buffering time. This capacitor will hold **V_BCKP** voltage within its valid range for around 50 s at 25°C, after the **VCC** supply is removed. If a very long buffering time is required, a 70 mF super-capacitor (e.g. Seiko

Instruments XH414H-IV01E) can be placed at **V_BCKP**, with a 4.7 kΩ series resistor to hold the **V_BCKP** voltage within its valid range for approximately 10 hours at 25°C, after the **VCC** supply is removed. The purpose of the series resistor is to limit the capacitor charging current due to the large capacitor specifications, and also to let a fast rise time of the voltage value at the **V_BCKP** pin after **VCC** supply has been provided. These capacitors will allow the time reference to run during battery disconnection.

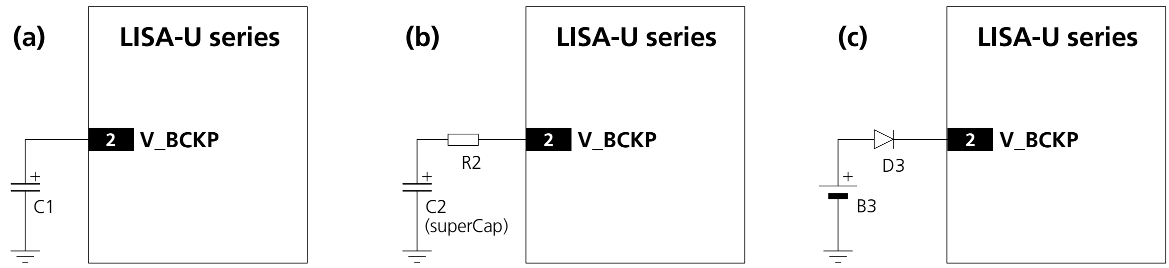

Figure 16: Real time clock supply (V_BCKP) application circuits: (a) using a 100 µF capacitor to let the RTC run for ~50 s after VCC removal; (b) using a 70 mF capacitor to let RTC run for ~10 hours after VCC removal; (c) using a non-rechargeable battery

Reference	Description	Part Number - Manufacturer
C1	100 µF Tantalum Capacitor	GRM43SR60J107M - Murata
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C2	70 mF Capacitor	XH414H-IV01E - Seiko Instruments

Table 13: Example of components for V_BCKP buffering

If longer buffering time is required to allow the time reference to run during a disconnection of the **VCC** supply, then an external battery can be connected to **V_BCKP** pin. The battery should be able to provide a proper nominal voltage and must never exceed the maximum operating voltage for **V_BCKP** (specified in the Input characteristics of Supply/Power pins table in LISA-U1 series Data Sheet [1] and in LISA-U2 series Data Sheet [2]). The connection of the battery to **V_BCKP** should be done with a suitable series resistor for a rechargeable battery, or with an appropriate series diode for a non-rechargeable battery. The purpose of the series resistor is to limit the battery charging current due to the battery specifications, and also to allow a fast rise time of the voltage value at the **V_BCKP** pin after the **VCC** supply has been provided. The purpose of the series diode is to avoid a current flow from the module **V_BCKP** pin to the non-rechargeable battery.

Combining a LISA-U series wireless module with a u-blox GPS receiver, the **VCC** supply of the GPS receiver is controlled by the wireless module by means of the GPS supply enable function provided by the GPIO2 of the wireless module. In this case the **V_BCKP** supply output of the LISA-U series wireless module can be connected to the **V_BCKP** backup supply input pin of the GPS receiver to provide the supply for the GPS real time clock and backup RAM when the **VCC** supply of the wireless module is within its operating range and the **VCC** supply of the GPS receiver is disabled. This enables the u-blox GPS receiver to recover from a power breakdown with either a Hotstart or a Warmstart (depending on the duration of the GPS **VCC** outage) and to maintain the configuration settings saved in the backup RAM. Refer to section 1.10 for more details regarding the application circuit with a u-blox GPS receiver.

1.5.5 Interface supply (V_INT)

The same voltage domain used internally to supply the digital interfaces is also available on the **V_INT** pin. The internal regulator that generates the **V_INT** supply is a switching step down converter that is directly supplied from **VCC**. The voltage regulator output is set to 1.8 V (typical) when the module is switched on and is disabled when the module is switched off or when the **RESET_N** pin is forced the low level. The switching regulator operates in Pulse Width Modulation (PWM) for high output current mode but automatically switches to Pulse

Frequency Modulation (PFM) at low output loads for greater efficiency, e.g. when the module is in idle-mode between paging periods.

Name	Description	Remarks
V_INT	Digital Interfaces supply output	**V_INT** = 1.8V (typical) generated by the module when it is switched-on and the **RESET_N** (external reset input pin) is not forced to the low level. **V_INT** is the internal supply for digital interfaces. The user may draw limited current from this supply rail.

Table 14: Interface supply pin

The **V_INT** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.

Since it supplies internal digital circuits (see Figure 4), **V_INT** is not suited to directly supply any sensitive analog circuit: the voltage ripple can range from 15 mVpp during active mode (PWM), to 70 mVpp in idle-mode (PFM).

V_INT can be used to supply external digital circuits operating at the same voltage level as the digital interface pins, i.e. 1.8 V (typical). It is not recommended to supply analog circuitry without adequate filtering for digital noise.

Don't apply loads which might exceed the limit for maximum available current from **V_INT** supply, as this can cause malfunctions in internal circuitry supplies to the same domain. The detailed electrical characteristics are described in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

V_INT can only be used as an output; don't connect any external regulator on **V_INT**. If not used, this pin should be left unconnected.

The **V_INT** digital interfaces supply output is mainly used to:

- Pull-up DDC (I^2C) interface signals (see section 1.10.2 for more details)
- Pull-up SIM detection signal (see section 1.8 for more details)
- Supply voltage translators to connect digital interfaces of the module to a 3.0 V device (see section 1.9.2.4)
- Indicate when the module is switched on and the **RESET_N** (external reset input) is not forced low

1.6 System functions

1.6.1 Module power-on

The power-on sequence of LISA-U series modules is initiated in one of these ways:

- Rising edge on the **VCC** pin to a valid voltage as module supply (i.e. applying module supply)
- Low level on the **PWR_ON** pin (i.e. forcing to the low level the pin normally high by external pull-up)
- Rising edge on the **RESET_N** pin (i.e. releasing from low level the pin, normally high by internal pull-up)
- RTC alarm (i.e. pre-programmed scheduled time by AT+CALA command)

Name	Description	Remarks
PWR_ON	Power-on input	**PWR_ON** pin has high input impedance. Do not keep floating in noisy environment: external pull-up required.

Table 15: Power-on pin

☞ The **PWR_ON** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.

1.6.1.1 Rising edge on VCC

When a supply is connected to **VCC** pins, the module supply supervision circuit controls the subsequent activation of the power up state machines: the module is switched on when the voltage rises up to the **VCC** normal operating range minimum limit starting from a voltage value lower than 2.25 V (refer to LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2] for the **VCC** normal operating range minimum limit).

☞ The voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to switch on the module.

1.6.1.2 Low level on PWR_ON

The module power-on sequence starts when a low level is forced on the **PWR_ON** input for at least 5 ms.

The electrical characteristics of the **PWR_ON** input pin are slightly different between LISA-U1 series and LISA-U2 series modules, and are different from the other digital I/O interfaces: the pin provides different input voltage thresholds and is tolerant of voltages up to the module supply level. The detailed electrical characteristics are described in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

☞ The **PWR_ON** pin has high input impedance and is weakly pulled to the high level on the module. Avoid keeping it floating in a noisy environment. To hold the high logic level stable, the **PWR_ON** pin must be connected to a pull-up resistor (e.g. 100 kΩ) biased by the **V_BCKP** supply pin of the module.

Following are some typical examples of application circuits to turn the module on using the **PWR_ON** input pin.

The simplest way to turn on the module is to use a push button that shorts the **PWR_ON** input to ground: in this case the **V_BCKP** supply pin can be used to bias the pull-up resistor.

If **PWR_ON** input is connected to an external device (e.g. application processor), it is suggested to use an open drain output on the external device with an external pull-up resistor (e.g. 100 kΩ) biased by the **V_BCKP** supply pin of the module.

A push-pull output of an application processor can also be used: in this case the pull-up can be used to pull the **PWR_ON** level high when the application processor is switched off. If the high-level voltage of the push-pull output pin of the application processor is greater than the maximum input voltage operating range of the **V_BCKP** pin (refer to the **V_BCKP** Input characteristics of Supply/Power pins table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]), the **V_BCKP** supply cannot be used to bias the pull-up resistor: the supply rail of the application processor or the **VCC** supply could be used, but this will increase the **V_BCKP** (RTC supply) current consumption when the module is in not-powered mode (**VCC** supply not present). Using a push-pull output of the external device, take care to fix the proper level in all the possible scenarios to avoid an inappropriate switch-on of the module.

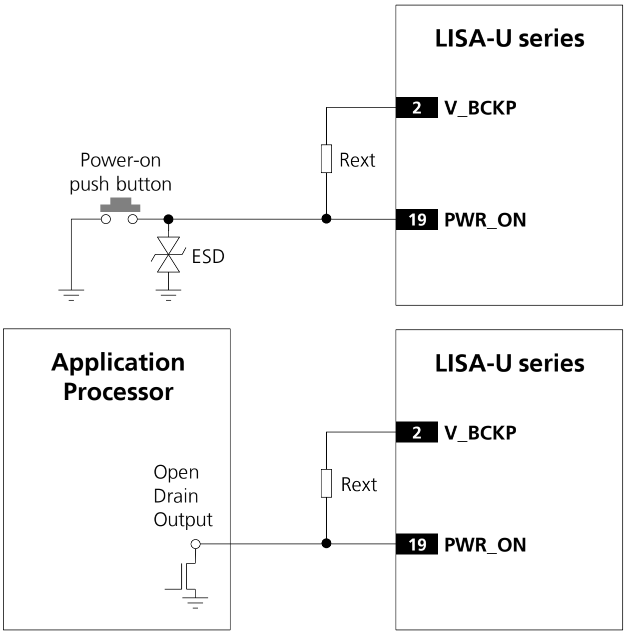

Figure 17: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
Rext	100 kΩ Resistor 0402 5% 0.1 W	External pull-up resistor
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 16: Example of pull-up resistor and ESD protection for the PWR_ON application circuits

1.6.1.3 Rising edge on RESET_N

LISA-U series modules can be switched on by means of the **RESET_N** input pin: the **RESET_N** signal must be forced low for at least 50 ms and then released to generate a rising edge that starts the module power-on sequence.

RESET_N input pin can also be used to perform an "external" or "hardware" reset of the module, as described in the section 1.6.3.

Electrical characteristics of the LISA-U series **RESET_N** input are slightly different from the other digital I/O interfaces: the pin provides different input voltage thresholds. Detailed electrical characteristics are described in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

RESET_N is pulled high to **V_BCKP** by an integrated pull-up resistor also when the module is in power-off mode. Therefore an external pull-up is not required on the application board.

The simplest way to switch on the module by means of the **RESET_N** input pin is to use a push button that shorts the **RESET_N** pin to ground: the module will be switched on at the release of the push button, since the **RESET_N** will be forced to the high level by the integrated pull-up resistor, generating a rising edge.

If **RESET_N** is connected to an external device (e.g. an application processor on an application board) an open drain output can be directly connected without any external pull-up. A push-pull output can be used too: in this case make sure that the high level voltage of the push-pull circuit is below the maximum voltage operating range of the **RESET_N** pin (specified in the **RESET_N** pin characteristics table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]). To avoid unwanted power-on or reset of the module make sure to fix the proper level at the **RESET_N** input pin in all possible scenarios.

Some typical examples of application circuits using the **RESET_N** input pin are described in the section 1.6.3.

1.6.1.4 Real Time Clock (RTC) alarm

If a voltage within the operating range is maintained at the **VCC** pin, the module can be switched on by the RTC alarm when the RTC system reaches a pre-programmed scheduled time (refer to the u-blox AT Commands Manual [3], AT+CALA command). The RTC system will then initiate the boot sequence by instructing the Power Management Unit to turn on power. Also included in this setup is an interrupt signal from the RTC block to indicate to the baseband processor that an RTC event has occurred.

1.6.1.5 Additional considerations

The module is switched on when the **VCC** voltage rises up to the normal operating range (i.e. applying module supply): the first time that the module is used, it is switched on in this way. Then, LISA-U series modules can be switched off by means of the AT+CPWROFF command. When the module is in power-off mode, i.e. the AT+CPWROFF command has been sent and a voltage value within the normal operating range limits is still provided to the **VCC** pin, the digital input-output pads of the baseband chipset (i.e. all the digital pins of the module) are locked in tri-state (i.e. floating). The power down tri-state function isolates the module pins from its environment, when no proper operation of the outputs can be guaranteed.

The module can be switched on from power-off mode by forcing a proper start-up event (i.e. **PWR_ON** low, **RESET_N** release or RTC alarm). After the detection of a start-up event, all the digital pins of the module are held in tri-state until all the internal LDO voltage regulators are turned on in a defined power-on sequence. Then, as described in Figure 18, the baseband core is still held in reset state for a time interval: the internal reset signal (which is not available on a module pin) is still low and any signal from the module digital interfaces is held in reset state. The reset state of all the digital pins is reported in the pin description table of LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]. When the internal signal is released, the configuration of the module interfaces starts: during this phase any digital pin is set in a proper sequence from the reset state to the default operational configuration. Finally, the module is fully ready to operate when all interfaces are configured.

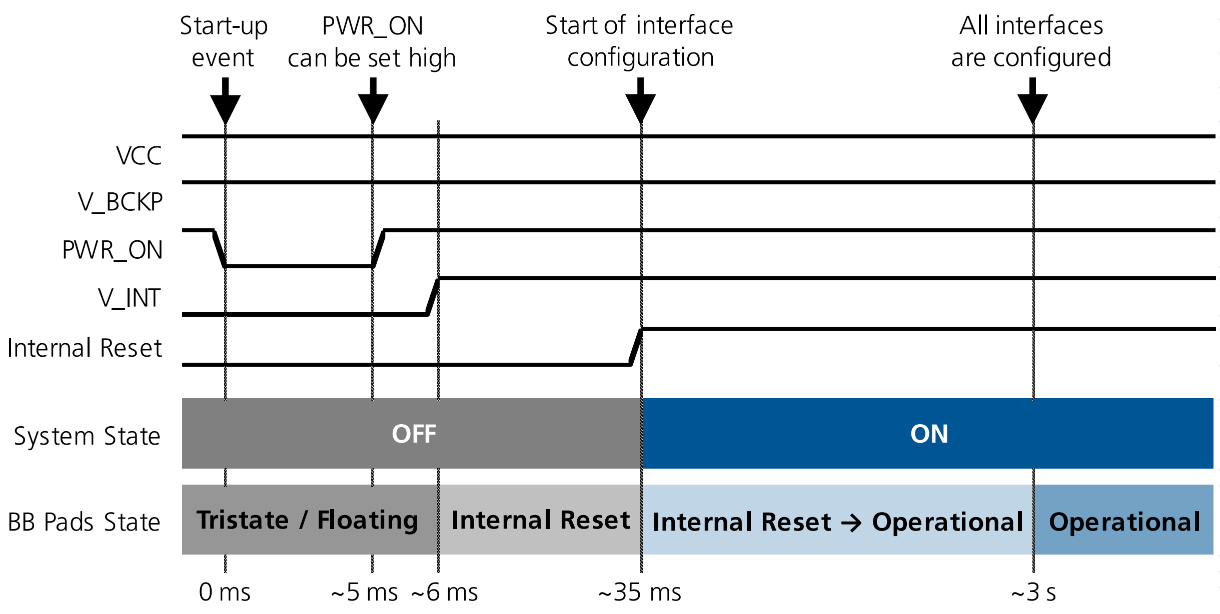

Figure 18: LISA-U series power-on sequence description

☞ The Internal Reset signal is not available on a module pin.

☞ Any external signal connected to the UART interface, SPI/IPC interface, I²S interfaces and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and let a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode, when external reset is forced low and during power on sequence.

1.6.2 Module power-off

The correct way to switch off LISA-U series modules is by means of +CPWROFF AT command (more details in u-blox AT Commands Manual [3]): in this way the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

LISA-U2xx-01 modules can also be properly switched off by means of the **PWR_ON** input pin: the **PWR_ON** signal must be held to the low logic level for more than 1 s to start the module power-off sequence. In this way, current parameter settings are saved in LISA-U2xx-01 module's non-volatile memory and a correct network detach is performed: the same sequence is performed as by the +CPWROFF AT command.

An under-voltage shutdown occurs on LISA-U series modules when the **VCC** supply is removed, but in this case the current parameter settings are not saved in the module's non-volatile memory and a proper network detach cannot be performed.

The power-off sequence by means of +CPWROFF AT command is described in Figure 19. When the +CPWROFF AT command is sent, the module starts the switch-off routine replying OK on the AT interface. At the end of the switch-off routine, all digital pins are locked in tri-state by the module and all the internal LDO voltage regulators except the RTC supply (**V_BCKP**) are turned off in a defined power-off sequence. The module remains in power-off mode as long as a switch on event doesn't occur (i.e. applying a low level on the **PWR_ON** pin, or releasing from low level the **RESET_N** pin, or by a pre-programmed RTC alarm), and enters not-powered mode if the supply is removed from the **VCC** pin.

Current parameter settings are stored to the module's non-volatile memory and a network detach is performed before the OK reply from AT+CPWROFF command on all LISA-U series modules except LISA-U1xx-00 versions. Storage of parameters and network detach are performed before the end of the switch-off routine, but not necessary before the OK reply from AT+CPWROFF command on LISA-U1xx-00 versions.

Since the time to perform a network detach depends on the network settings, the duration of the switch off routine phases can differ from the typical values reported in Figure 19.

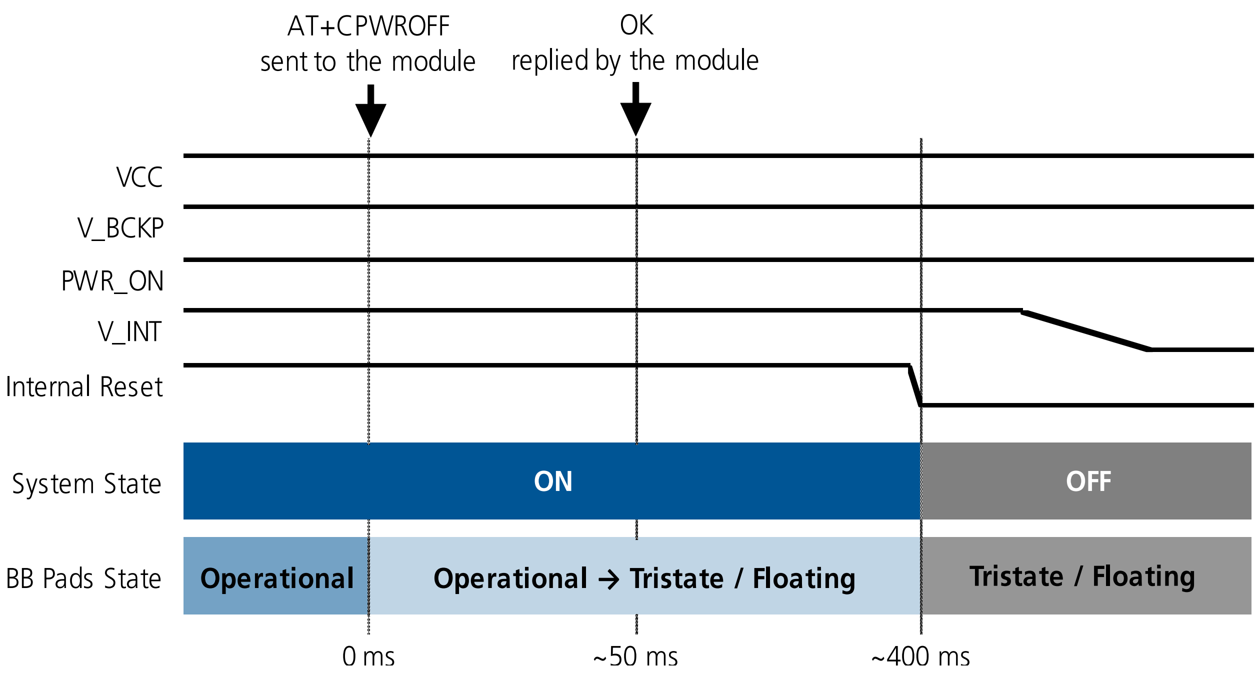

Figure 19: LISA-U series Power-off sequence description

☞ The Internal Reset signal is not available on a module pin.

☞ Tristated pins are always subject to floating caused by noise: to prevent unwanted effects, fix them with proper pull-up or pull down resistors to stable voltage rails to fix their level when the module is in Power down state.

☞ Any external signal connected to the UART interface, SPI/IPC interface, I^2S interfaces and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode, when external reset is forced low and during power-on sequence.

1.6.3 Module reset

LISA-U series modules reset can be performed in one of 2 ways:

- Forcing a low level on the **RESET_N** input pin, causing an "external" or "hardware" reset
- Via AT command, causing an "internal" or "software" reset

RESET_N input pin: force low for at least 50 ms; either an "external" or "hardware" reset is performed. This causes an asynchronous reset of the entire module, including the integrated Power Management Unit, except for the RTC internal block: the **V_INT** interfaces supply is switched off and all the digital pins are tri-stated, but the **V_BCKP** supply and the RTC block are enabled. Forcing an "external" or "hardware" reset, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

AT+CFUN command (more details in u-blox AT Commands Manual [3]): in this case an "internal" or "software" reset is performed, causing an asynchronous reset of the baseband processor, excluding the integrated Power Management Unit and the RTC internal block: the **V_INT** interfaces supply is enabled and each digital pin is set in its internal reset state (reported in the pin description table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]), the **V_BCKP** supply and the RTC block are enabled. Forcing an "internal" or "software" reset, the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

When **RESET_N** is released from the low level, the module automatically starts its power-on sequence from the reset state. The same procedure is followed for the module reset via AT command after having performed the network detach and the parameter saving in non-volatile memory.

☞ The internal reset state of all digital pins is reported in the pin description table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

Name	Description	Remarks
RESET_N	External reset input	Internal 10 kΩ pull-up to **V_BCKP**

Table 17: Reset pin

☞ The **RESET_N** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.

☞ For more details about **RESET_N** circuit precautions for ESD immunity please refer to chapter 2.5.3.

The electrical characteristics of **RESET_N** are different from the other digital I/O interfaces. The detailed electrical characteristics are described in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

RESET_N is pulled high by an integrated 10 kΩ pull-up resistor to **V_BCKP**. Therefore an external pull-up is not required on the application board.

Following are some typical examples of application circuits using the **RESET_N** input pin.

The simplest way to reset the module is to use a push button that shorts the **RESET_N** pin to ground.

If **RESET_N** is connected to an external device (e.g. an application processor on an application board) an open drain output can be directly connected without any external pull-up. A push-pull output can be used too: in this case make sure that the high level voltage of the push-pull circuit is below the maximum voltage operating range of the **RESET_N** pin (specified in the **RESET_N** pin characteristics table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]). To avoid unwanted reset of the module make sure to fix the proper level at the **RESET_N** input pin in all possible scenarios.

As ESD immunity test precaution, a 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JA01) and a series ferrite bead (e.g. Murata BLM15HD182SN1) must be added on the **RESET_N** line pin of LISA-U1 series modules and an additional 220 nF bypass capacitor (e.g. Murata GRM155R60J224KE01) must be added as close as possible to the **RESET_N** pin of LISA-U2 series modules to avoid a module reset caused by an electrostatic discharge applied to the application board (for more details, refer to chapter 2.5.3).

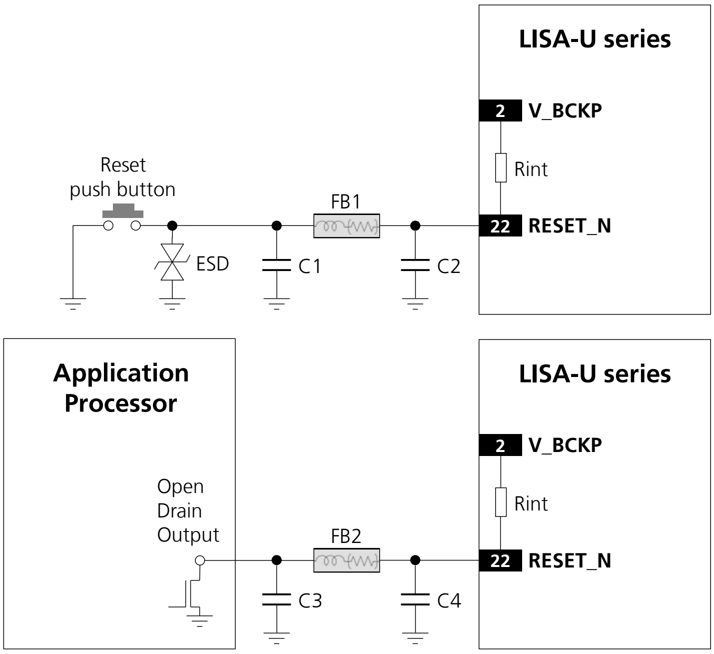

Figure 20: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection.	CT0402S14AHSG - EPCOS
C1, C3	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C2, C4	220 nF Capacitor Ceramic X5R 0402 10% 6.3 V	GRM155R60J224KE01 - Murata
FB1, FB2	Chip Ferrite Bead for Noise/EMI Suppression	BLM15HD182SN1 - Murata
Rint	10 kΩ Resistor 0402 5% 0.1 W	Internal pull-up resistor

Table 18: Example of ESD protection components for the RESET_N application circuit

☞ Any external signal connected to the UART interface, SPI/IPC interface, I^{2}S interfaces and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode, when external reset is forced low and during power-on sequence.

1.7 RF connection

The **ANT** pin, provided by all LISA-U series modules, represents the main RF input/output used to transmit and receive the 2G and 3G RF signal: the main antenna must be connected to this pad. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the 2G and 3G operating bands.

The **ANT_DIV** pin, provided by LISA-U230 modules, represents the RF input for the integrated diversity receiver: the antenna for the Rx diversity should be connected to this pad. The **ANT_DIV** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna for the Rx diversity through a 50 Ω transmission line to allow reception of radio frequency (RF) signals in the 2G and 3G operating bands.

Name	Module	Description	Remarks
ANT	All	RF input/output for main Tx/Rx antenna	Zo = 50 Ω nominal characteristic impedance.
ANT_DIV	LISA-U230	RF input for Rx diversity antenna	Zo = 50 Ω nominal characteristic impedance.

Table 19: Antenna pins

☞ ESD immunity rating of the **ANT** port of LISA-U1 series modules is 500 V (according to IEC 61000-4-2). ESD immunity rating of the **ANT** port of LISA-U200-00 modules is 1000 V (according to IEC 61000-4-2). Higher protection level could be required if the line is externally accessible on the application board (for further details see section 2.5.3).

Choose an antenna with optimal radiating characteristics for the best electrical performance and overall module functionality. An internal antenna, integrated on the application board, or an external antenna, connected to the application board through a proper 50 Ω connector, can be used. See section 2.4 and section 2.2.1.1 for further details regarding antenna guidelines.

⚠ **The recommendations of the antenna producer for correct installation and deployment (PCB layout and matching circuitry) must be followed.**

If an external antenna is used, the PCB-to-RF-cable transition must be implemented using either a suitable 50 Ω connector, or an RF-signal solder pad (including GND) that is optimized for 50 Ω characteristic impedance.

If antenna supervisor functionality is required, the main antenna connected to the **ANT** pin should have a built in DC diagnostic resistor to ground to get proper detection functionality (See section 2.4.3).

☞ If the Rx diversity is not implemented, **ANT_DIV** pin can be left unconnected on the application board.

1.8 (U)SIM interface

High-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM types are supported: activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The SIM driver supports the PPS

(Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM Card.

Name	Description	Remarks
VSIM	SIM supply	1.80 V typical or 2.90 V typical Automatically generated by the module
SIM_CLK	SIM clock	3.25 MHz clock frequency
SIM_IO	SIM data	Open drain, internal 4.7 kΩ pull-up resistor to **VSIM**
SIM_RST	SIM reset	

Table 20: SIM Interface pins

☞ A low capacitance (i.e. less than 10 pF) ESD protection (e.g. Infineon ESD8V0L2B-03L or AVX USB0002RP) must be placed near the SIM card holder on each line (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST**). The SIM interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F): higher protection level is required if the lines are connected to an SIM card connector, since they are externally accessible on the application board.

☞ For more details about the general precautions for ESD immunity about SIM interface pins please refer to chapter 2.5.3.

Figure 21 shows an application circuit connecting the LISA-U series module and the SIM card placed in a SIM card holder, using the SIM detection function provided by **GPIO5** pin.

Note that, as defined by ETSI TS 102 221 or ISO/IEC 7816, SIM card contacts assignment is as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact for USB interface and other uses) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It must be connected to **VSIM**
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact for USB interface and other uses) → It must be left not connected

A SIM card can have 6 contacts (C1 = VCC, C2 = RST, C3 = CLK, C5 = GND, C6 = VPP, C7 = I/O) or 8 contacts (providing also the auxiliary contacts C4 = AUX1 and C8 = AUX2). The contacts number depends if additional features, that are not supported by the (U)SIM card interface of the LISA-U series modules, are provided by the SIM card (contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses).

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins for the mechanical card presence detection are provided.

Figure 21 shows an application circuit connecting a LISA-U series module and a SIM card placed in a SIM card holder with 6+2 pins (as the CCM03-3013LFT R102 connector, produced by C&K Components, which provides 2 pins for the mechanical card presence detection), using the SIM detection function provided by the **GPIO5** of LISA-U series module. This configuration allows the module to detect if a SIM card is present in the connector. The SW1 and SW2 pins of the SIM card holder are connected to a normally-open mechanical switch integrated in the SIM connector. The following cases are available

- SIM card not present: the **GPIO5** signal is forced low by the pull-down resistor connected to ground (i.e. the switch integrated in the SIM connector is open)
- SIM card present: the **GPIO5** signal is forced high by the pull-up resistor connected to **V_INT** (i.e. the switch integrated in the SIM connector is closed)

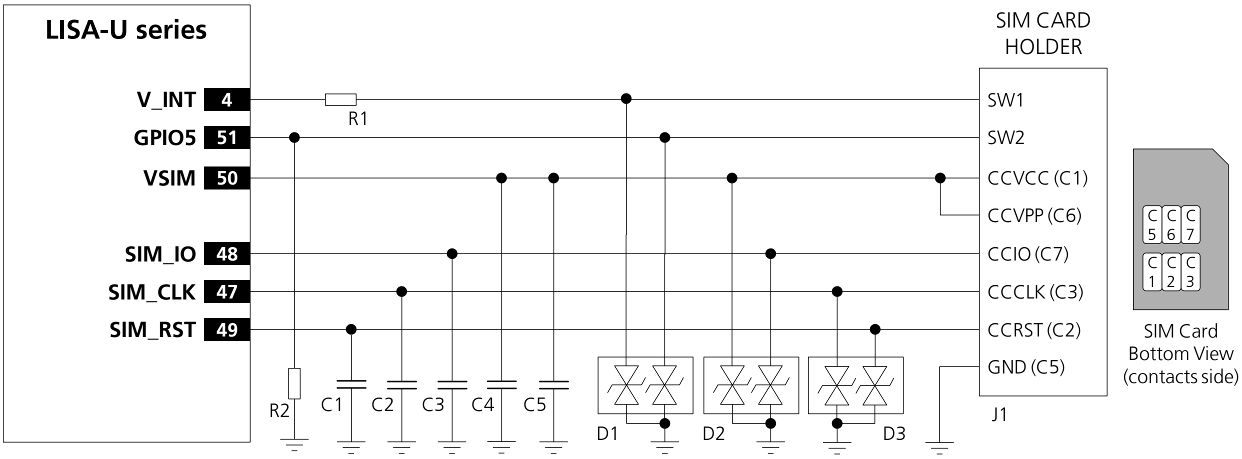

Figure 21: SIM interface application circuit

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	33 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3	Low capacitance ESD protection	USB0002RP or USB0002DP - AVX
R1	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM Card Holder	Various Manufacturers, CCM03-3013LFT R102 - C&K Components

Table 21: Example of components for SIM card connection

When connecting the module to an SIM connector, perform the following steps on the application board:

- Bypass digital noise via a 100 nF capacitor (e.g. Murata GRM155R71C104K) on the SIM supply (**VSIM**)
- To prevent RF coupling in case the module RF antenna is placed closer than 10 - 30 cm from the SIM card holder, connect a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) at each SIM signal (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) to ground near the SIM connector
- Mount very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Infineon ESD8V0L2B-03L or AVX USB0002) near the SIM card connector
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines): always route the connections to keep them as short as possible

1.8.1 (U)SIM functionality

The following SIM services are supported:

- Abbreviated Dialing Numbers (ADN)
- Fixed Dialing Numbers (FDN)
- Last Dialed Numbers (LDN)
- Service Dialing Numbers (SDN)

USIM Application Toolkit (USAT) R99 is supported.

1.9 Serial communication

LISA-U series modules provide the following serial communication interfaces where AT command interface and Packet-Switched / Circuit-Switched Data communication are concurrently available:

- One asynchronous serial interface (UART) that provides complete RS-232 functionality conforming to ITU-T V.24 Recommendation [4], with limited data rate. The UART interface can be used for firmware upgrade
- One Inter Processor Communication (IPC) interface that includes a synchronous SPI-compatible interface, with maximum data rate of 26 Mb/s
- One high-speed USB 2.0 compliant interface, with maximum data rate of 480 Mb/s. The single USB interface implements several logical devices. Each device is a USB communications device class (or USB CDC), that is a composite Universal Serial Bus device class. The USB interface can be used for firmware upgrade

The LISA-U series modules are designed to operate as an HSPA wireless modem, which represents the data circuit-terminating equipment (DCE) as described by the ITU-T V.24 Recommendation [4]. A customer application processor connected to the module through one of the interfaces represents the data terminal equipment (DTE).

All the interfaces listed above are controlled and operated with:

- AT commands according to 3GPP TS 27.007 [5]
- AT commands according to 3GPP TS 27.005 [6]
- AT commands according to 3GPP TS 27.010 [7]
- u-blox AT commands

☞ For the complete list of supported AT commands and their syntax refer to the u-blox AT Commands Manual [3].

The following serial communication interfaces can be used for firmware upgrade:

- The UART interface, using the **RxD** and **TxD** lines only
- The USB interface, using all the lines provided (**VUSB_DET**, **USB_D+** and **USB_D-**)

☞ To directly enable PC (or similar) connection to the module for firmware upgrade, provide direct access on the application board to the **VUSB_DET**, **USB_D+** and **USB_D-** lines of the module (or to the **RxD** and **TxD** lines). Also provide access to the **PWR_ON** or the **RESET_N** pins, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade (see Firmware Update Application Note [17]).

The following sub-chapters describe the serial interfaces configuration and provide a detailed description of each interface for the application circuits.

1.9.1 Serial interfaces configuration

UART, USB and SPI/IPC serial interfaces are available as AT command interface and for Packet-Switched / Circuit-Switched Data communication. The serial interfaces are configured as described in Table 22 (for information about further settings, please refer to the u-blox AT Commands Manual [3]).

Interface	AT Settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1 – 5: AT commands /data connection • Channel 6: GPS tunneling All LISA-U2 series modules versions except LISA-U200-00 provide an additional channel: • Channel 7: SIM Access Profile dedicated port
	AT+IPR=115200	Baud rate: 115200 b/s
	AT+ICF=3,1	Frame format: 8 bits, no parity, 1 stop bit
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
USB interface	Enabled	6 CDCs are available, configured as described in the following list: • USB1: AT commands / data connection • USB2: AT commands / data connection • USB3: AT commands / data connection • USB4: GPS tunneling dedicated port • USB5: 2G and BB trace dedicated port • USB6: 3G trace dedicated port All LISA-U2 series modules versions except LISA-U200-00 provide an additional CDC: • USB7: SIM Access Profile dedicated port
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
SPI interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1 – 5: AT commands /data connection • Channel 6: GPS tunneling All LISA-U2 series modules versions except LISA-U200-00 provide an additional channel: • Channel 7: SIM Access Profile dedicated port
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise

Table 22: Default serial interfaces configuration

1.9.2 Asynchronous serial interface (UART)

The UART interface is a 9-wire unbalanced asynchronous serial interface that provides AT commands interface, PSD and CSD data communication, firmware upgrade.

UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation (more details available in ITU Recommendation [4]), with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state. Two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC8T245PW) could be used to provide full RS-232 (9 lines) compatible signal levels. The Texas Instruments chip provides the translation from 1.8 V to 3.3 V, while the Maxim chip provides the necessary RS-232 compatible signal towards the external connector. If a UART interface with only 5 lines is needed, the Maxim 13234E voltage level translator can be used. This chip translates the voltage levels from 1.8 V (module side) to the RS-232 standard. For detailed electrical characteristics refer to LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

The LISA-U series modules are designed to operate as an HSPA wireless modem, which represents the data circuit-terminating equipment (DCE) as described by the ITU-T V.24 Recommendation [4]. A customer application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ The signal names of the LISA-U series modules UART interface conform to the ITU-T V.24 Recommendation [4].

UART interfaces include the following lines:

Name	Description	Remarks
DSR	Data set ready	Module output Circuit 107 (Data set ready) in ITU-T V.24
RI	Ring Indicator	Module output Circuit 125 (Calling indicator) in ITU-T V.24
DCD	Data carrier detect	Module output Circuit 109 (Data channel received line signal detector) in ITU-T V.24
DTR	Data terminal ready	Module input Circuit 108/2 (Data terminal ready) in ITU-T V.24 Internal active pull-up to **V_INT** (1.8 V) enabled.
RTS	Ready to send	Module hardware flow control input Circuit 105 (Request to send) in ITU-T V.24 Internal active pull-up to **V_INT** (1.8 V) enabled.
CTS	Clear to send	Module hardware flow control output Circuit 106 (Ready for sending) in ITU-T V.24
TxD	Transmitted data	Module data input Circuit 103 (Transmitted data) in ITU-T V.24 Internal active pull-up to **V_INT** (1.8 V) enabled.
RxD	Received data	Module data output Circuit 104 (Received data) in ITU-T V.24
GND	Ground	

Table 23: UART interface signals

☞ The UART interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins, close to accessible points.

1.9.2.1 UART features

All flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see u-blox AT Commands Manual [3], &K, +IFC, \Q AT commands): hardware flow control (RTS/CTS), software flow control (XON/XOFF), or none flow control.

☞ Hardware flow control is enabled by default.

The following baud rates can be configured using AT commands:

- 1200 b/s
- 2400 b/s

- 4800 b/s
- 9600 b/s
- 19200 b/s
- 38400 b/s
- 57600 b/s
- 115200 b/s
- 230400 b/s
- 460800 b/s

The default baud rate is 115200 b/s. Autobauding is not supported.

The frame format can be:

- 8N1 (8 data bits, No parity, 1 stop bit)
- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 8N2 (8 data bits, No parity, 2 stop bits)
- 7E1 (7 data bits, even parity, 1 stop bit)
- 7O1 (7 data bits, odd parity, 1 stop bit)

The default frame configuration with fixed baud rate is 8N1, described in the Figure 22.

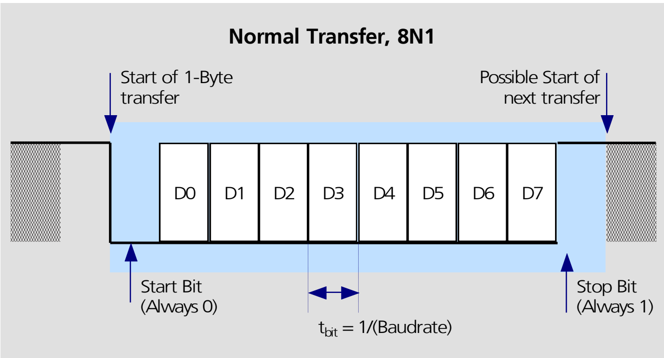

Figure 22: UART default frame format (8N1) description

1.9.2.2 UART signal behavior (AT commands interface case)

See Table 5 for a description of operating modes and states referred to in this section.

At the switch on of the module, before the initialization of the UART interface, as described in the power-on sequence reported in the Figure 18, each pin is first tri-stated and then is set to its relative internal reset state that is reported in the pin description table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]. At the end of the boot sequence, the UART interface is initialized, the module is by default in active mode and the UART interface is enabled. The configuration and the behavior of the UART signals after the boot sequence are described below.

☞ For a complete description of data and command mode please refer to u-blox AT Commands Manual [3].

RxD signal behavior

The module data output line (**RxD**) is set by default to OFF state (high level) at UART initialization. The module holds **RxD** in OFF state until no data is transmitted by the module.

TxD signal behavior

The module data input line (**TxD**) is set by default to OFF state (high level) at UART initialization. The **TxD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TxD** input.

CTS signal behavior

The module hardware flow control output (**CTS** line) is set to the ON state (low level) at UART initialization.

If the hardware flow control is enabled (for more details please refer to u-blox AT Commands Manual [3], AT&K, AT\Q, AT+IFC AT command) the **CTS** line indicates when the UART interface is enabled (data can be sent and received): the module drives the **CTS** line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE (refer to chapter 1.9.2.3 for the complete description).

If the hardware flow control is not enabled, the **CTS** line is always held in the ON state after UART initialization.

☞ In case of hardware flow control enabled, when **CTS** line is ON the UART is enabled and the module is in active mode. Instead, **CTS** line to OFF doesn't necessary mean that the module is in idle-mode, but only that the UART is not enabled (the module could be forced to stay in active-mode for instance by USB).

☞ When the power saving configuration is enabled and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in idle-mode won't be a valid communication character (refer to chapter 1.9.2.3 for the complete description).

☞ When the MUX protocol is active on UART interface, the **CTS** line state is mapped to FCon / FCoff MUX command for flow control issues outside the power saving configuration while the physical **CTS** line is still used as a power state indicator. For more details please refer to Mux Implementation Application Note [15].

RTS signal behavior

The hardware flow control input (**RTS** line) is set by default to the OFF state (high level) at UART initialization. The **RTS** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **RTS** input.

If the HW flow control is enabled (for more details please refer to u-blox AT Commands Manual [3] AT&K, AT\Q, AT+IFC command description) the **RTS** line is monitored by the module to detect permission from the DTE to send data to the DTE itself. If the **RTS** line is set to OFF state, any on-going data transmission from the module is immediately interrupted or any subsequent transmission forbidden until the **RTS** line changes to ON state.

☞ The DTE must be able to still accept a certain number of characters after the **RTS** line has been set to OFF state: the module guarantees the transmission interruption within 2 characters from **RTS** state change.

If AT+UPSV=2 is set and HW flow control is disabled, the **RTS** line is monitored by the module to manage the power saving configuration:

- When an OFF-to-ON transition occurs on the **RTS** input line, the UART is enabled and the module is forced to active-mode; after 20 ms from the transition the switch is completed and data can be received without loss. The module can't enter idle-mode and the UART is keep enabled as long as the **RTS** input line is held in the ON state

- If **RTS** is set to OFF state by the DTE, the module automatically enters idle-mode whenever possible as in the AT+UPSV=1 configuration (cyclic idle/active mode), but UART is disabled (held in low power mode)

For more details please refer to chapter 1.9.2.3 and u-blox AT Commands Manual [3], AT+UPSV command.

DSR signal behavior

If AT&S0 is set, the **DSR** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&S1 is set, the **DSR** module output line is set by default to OFF state (high level) at UART initialization. The **DSR** line is then set to the OFF state when the module is in command mode or in online command mode and is set to the ON state when the module is in data mode.

☞ The above behavior is valid for both Packet-Switched and Circuit-Switched Data transfer.

DTR signal behavior

The **DTR** module input line is set by default to OFF state (high level) at UART initialization. The **DTR** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **DTR** input. Module behavior according to **DTR** status depends on the AT command configuration (see u-blox AT Commands Manual [3], &D AT command).

DCD signal behavior

If AT&C0 is set, the **DCD** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&C1 is set, the **DCD** module output line is set by default to OFF state (high level) at UART initialization. The **DCD** line is then set by the module in accordance with the carrier detect status: ON if the carrier is detected, OFF otherwise. In case of voice call **DCD** is set to ON state when the call is established. For a data call there are the following scenarios:

- **GPRS data communication**: Before activating the PPP protocol (data mode) a dial-up application must provide the ATD*99***<context_number># to the module: with this command the module switches from command mode to data mode and can accept PPP packets. The module sets the **DCD** line to the ON state, then answers with a CONNECT to confirm the ATD*99 command. Please note that the **DCD** ON is not related to the context activation but with the data mode
- **CSD data call**: To establish a data call the DTE can send the ATD<number> command to the module which sets an outgoing data call to a remote modem (or another data module). Data can be transparent (non reliable) or non transparent (with the reliable RLP protocol). When the remote DCE accepts the data call, the module **DCD** line is set to ON and the CONNECT <communication baudrate> string is returned by the module. At this stage the DTE can send characters through the serial line to the data module which sends them through the network to the remote DCE attached to a remote DTE

☞ In case of a voice call **DCD** is set to ON state on all the serial communication interfaces supporting the AT command interface. (including MUX virtual channels, if active).

☞ **DCD** is set to ON during the execution of a command requiring input data from the DTE (all the commands where a prompt is issued; see AT commands +CMGS, +CMGW, +USOWR, +USODL, +UDWNFILE in u-blox AT Commands Manual [3]). The **DCD** line is set to ON state as soon as the switch to binary/text input mode is completed and the prompt is issued; **DCD** line is set to OFF as soon as the input mode is interrupted or completed.

DCD line is kept to ON state even during the online command state to indicate that the data call is still established even if suspended, while if the module enters command mode **DSR** line is set to OFF state. For more details refer to DSR signal behavior description.

In case of scenarios for which the **DCD** line setting is requested for different reasons (e.g. SMS texting during online command state), the **DCD** line changes to guarantee the correct behavior for all the scenarios. For instance, in case of SMS texting in online command state, if the data call is released, the **DCD** line will be kept to ON till the SMS command execution is completed (even if the data call release would request the **DCD** setting to OFF).

RI signal behavior

The **RI** module output line is set by default to the OFF state (high level) at UART initialization. Then, during an incoming call, the **RI** line is switched from OFF state to ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 23), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

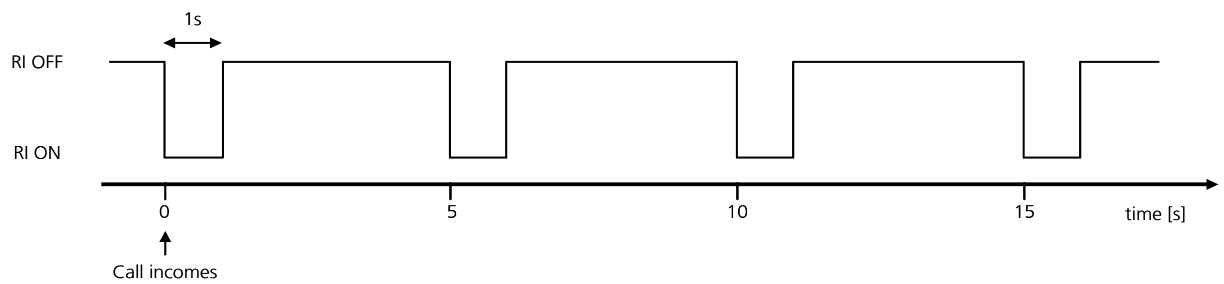

Figure 23: RI behavior during an incoming call

The **RI** line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 24), if the feature is enabled by the proper AT command (please refer to u-blox AT Commands Manual [3], AT+CNMI command).

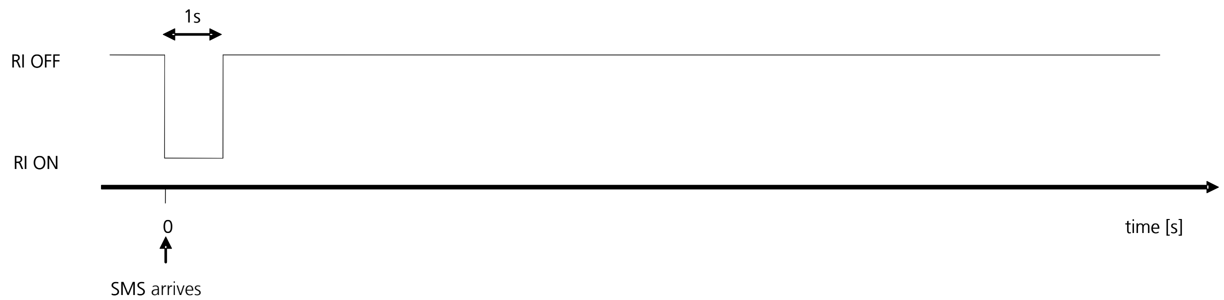

Figure 24: RI behavior at SMS arrival

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.
In case of SMS arrival, if several events occur coincidently or in quick succession each event triggers the **RI** line independently, although the line will not be deactivated between each event. As a result, the **RI** line may stay to ON for more than 1 s.

If an incoming call is answered within less than 1 s (with ATA or if autoanswering is set to ATS0=1) than the **RI** line will be set to OFF earlier.

As a result:

RI line monitoring can't be used by the DTE to determine the number of received SMSes.

☞ In case of multiple events (incoming call plus SMS received), the **RI** line can't be used to discriminate the two events, but the DTE must rely on the subsequent URCs and interrogate the DCE with the proper commands.

1.9.2.3 UART and power-saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description please refer to u-blox AT Commands Manual [3], AT+UPSV command). When power saving is enabled, the module automatically enters idle-mode whenever possible, otherwise the active-mode is maintained by the module. The AT+UPSV command sets the module power saving configuration, but also configures the UART behavior in relation to the power saving configuration. The conditions for the module entering idle-mode also depend on the UART power saving configuration.

The different power saving configurations that can be set by the AT+UPSV command are described in the following subchapters and are summarized in Table 24. For more details on the command description please refer to u-blox AT commands Manual [3].

AT+UPSV	HW flow control	RTS line	Communication during idle-mode and wake up
0	Enabled (AT&K3)	ON	Data sent by the DTE will be correctly received by the module.
0	Enabled (AT&K3)	OFF	Data sent by the module will be buffered by the module and will be correctly received by the DTE when it will be ready to receive data (i.e. **RTS** line will be ON).
0	Disabled (AT&K0)	ON	Data sent by the DTE will be correctly received by the module.
0	Disabled (AT&K0)	OFF	Data sent by the module will be correctly received by the DTE if it is ready to receive data, otherwise data will be lost.
1	Enabled (AT&K3)	ON	Data sent by the DTE will be buffered by the DTE and will be correctly received by the module when active-mode is entered.
1	Enabled (AT&K3)	OFF	Data sent by the module will be buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
1	Disabled (AT&K0)	ON	If the module is in idle-mode, when a low-to-high transition occurs on the **TxD** input line, the module switches from idle-mode to active-mode after 20 ms: this is the "wake up time" of the module. As a consequence, the first character sent when the module is in idle-mode (i.e. the wake up character) won't be a valid communication character because it can't be recognized, and the recognition of the subsequent characters is guaranteed only after the complete wake-up (i.e. after 20 ms).
1	Disabled (AT&K0)	OFF	Data sent by the module will be correctly received by the DTE if it is ready to receive data, otherwise data will be lost.
2	Enabled (AT&K3)	ON	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Enabled (AT&K3)	OFF	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	The module is forced in active-mode and it can't enter idle-mode until **RTS** line is set to OFF state. When a high-to-low (i.e. OFF-to-ON) transition occurs on the **RTS** input line, the module switches from idle-mode to active-mode after 20 ms: this is the "wake up time" of the module.
2	Disabled (AT&K0)	OFF	When a low-to-high transition occurs on the **TxD** input line, the UART is re-enabled and if the module was in idle-mode it switches from idle-mode to active-mode after 20 ms: this is the "wake up time" of the module. As a consequence, the first character sent when the module is in idle-mode (i.e. the wake up character) won't be a valid communication character because it can't be recognized, and the recognition of the subsequent characters is guaranteed only after the complete wake-up (i.e. after 20 ms).

Table 24: UART and power-saving summary

AT+UPSV=0: power saving disabled, fixed active-mode

The module doesn't enter idle-mode and the UART interface is enabled (data can be sent and received): the **CTS** line is always held in the ON state after UART initialization. This is the default configuration.

AT+UPSV=1: power saving enabled, cyclic idle/active mode

The module automatically enters idle-mode whenever possible, if a voice or data call (2G or 3G) is not enabled, and periodically wakes up from idle-mode to active-mode to monitor the paging channel of the current base station (paging block reception), according to 2G or 3G discontinuous reception (DRX) specification.

The time period between two paging receptions is defined by the current base station (i.e. by the network):

- If the module is registered with a 2G network, the paging reception period can vary from ~0.47 s (DRX = 2, i.e. 2 x 51 2G-frames) up to ~2.12 s (DRX = 9, i.e. 9 x 51 2G-frames)
- If the module is registered with a 3G network, the paging reception period can vary from 0.64 s (DRX = 6, i.e. 2^6 3G-frames) up to 5.12 s (DRX = 9, i.e. 2^9 3G-frames).

The UART interface is automatically disabled whenever possible, if data has not been received or sent by the UART for the timeout configured by the +UPSV AT command, and is periodically enabled to receive or send data. When the module is in idle-mode, the UART interface is always disabled. When the module is in active-mode or connected-mode, the UART interface is automatically disabled to reduce the consumed power, if data has not been received or sent by the UART for the configured timeout.

The time period of the UART enable/disable cycle is configured differently when the module is registered with a 2G network compared to when the module is registered with a 3G network:

- 2G: the UART is enabled synchronously to paging receptions, but not necessarily at every paging reception (to reduce the consumed power): the UART interface is enabled for 20 ms concurrently to a paging reception, and then, as data has not been received or sent, the UART is disabled until the first paging reception that occurs after a timeout of 2.0 s, and therefore the interface is enabled again
- 3G: the UART is enabled asynchronously to paging receptions: the UART interface is enabled for 20 ms, and then, as data has not been received or sent, the UART is disabled for 2.5 s, and afterwards the interface is enabled again
- Not registered: when the module is not registered with a network, the UART interface is enabled for 20 ms, and then, if data has not been received or sent, the UART is disabled for 2.5 s, and afterwards the interface is enabled again

When UART interface is disabled, data transmitted by the DTE will be lost if hardware flow control is disabled. If hardware flow control is enabled, data will be buffered by the DTE and will be correctly received by the module when UART interface is enabled again.

When UART interface is enabled, data can be received. When a character is received, it forces the UART interface to stay enabled for a longer time and it forces the module to stay in the active-mode for a longer time.

The active-mode duration depends by:

- Network parameters, related to the time interval for the paging block reception (minimum of ~11 ms)
- Duration of UART enable time in absence of data reception (20 ms)
- Time period from the last data received at the serial port during the active-mode: the module doesn't enter idle-mode until a timeout expires. This timeout is configured by the second parameter of the +UPSV AT command, from 40 2G-frames (i.e. 40 x 4.615 ms = 184 ms) up to 65000 2G-frames (i.e. 65000 x 4.615 ms = 300 s). Default value is 2000 2G-frames (i.e. 2000 x 4.615 ms = 9.2 s)

  Every subsequent character received during the active-mode, resets and restarts the timer; hence the active-mode duration can be extended indefinitely.

The hardware flow-control output (**CTS** line) indicates when the UART interface is enabled (data can be sent and received), if HW flow control is enabled, as illustrated in Figure 25.

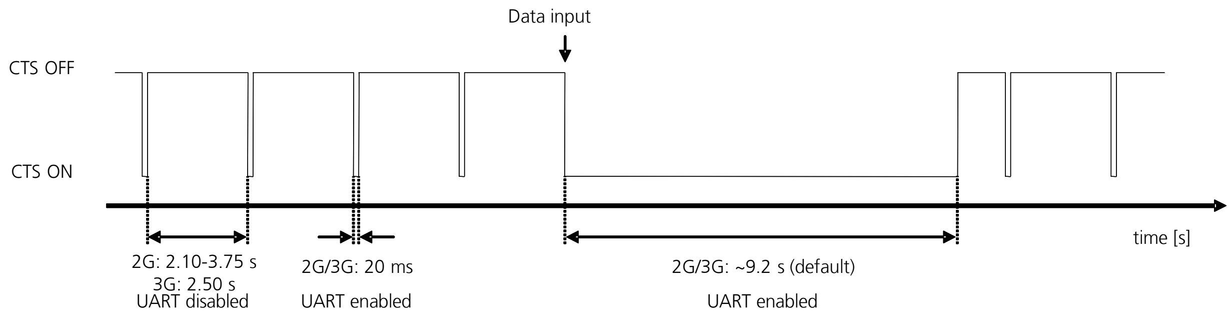

Figure 25: CTS behavior with power saving enabled (AT+UPSV=1) and HW flow control enabled: the CTS output line indicates when the UART interface of the module is enabled (CTS = ON = low level) or disabled (CTS = OFF = high level)

AT+UPSV=2: power saving enabled and controlled by the RTS line

If the **RTS** line is set to OFF by the DTE the module is allowed to enter idle-mode as for UPSV=1 case. Instead, the UART is disabled as long as **RTS** line is set to OFF.

If the **RTS** line is set to ON by the DTE the module is not allowed to enter idle-mode and the UART is kept enabled until the **RTS** line is set to OFF.

When an OFF-to-ON transition occurs on the **RTS** input line, the UART is re-enabled and the module switches from idle-mode to active-mode in 20 ms. This configuration can only be enabled with the module HW flow control disabled.

☞ Since HW flow control is disabled, the **CTS** line is always set to ON by the module.

☞ When the **RTS** line is set to OFF by the DTE, the timeout to enter idle-mode from the last data received at the serial port during the active-mode is the one previously set with the AT+UPSV=1 configuration or it is the default value.

☞ If the module must transmit some data (e.g. URC), the UART is temporarily enabled even if the **RTS** line is set to OFF; UART wake-up in case of **RTS** line set to OFF is also possible via data reception (as described in the following).

☞ If the USB is connected and active, the module is forced to stay in active-mode, therefore +UPSV=1 and +UPSV=2 modes are overruled, but in any case they have effect on the UART behavior (they configure UART power saving mode, when it is enabled/disabled).

Wake up from idle-mode to active-mode via data reception

If data is transmitted by the DTE during the module idle-mode, it will be lost (not correctly received by the module) in the following cases:

- +UPSV=1 with hardware flow control disabled
- +UPSV=2 with hardware flow control disabled and RTS line set to OFF

When the module is in idle-mode, the **TxD** input line of the module is always configured to wake up the module from idle-mode to active-mode via data reception: when a low-to-high transition occurs on the **TxD** input line, it causes the wake-up of the system. The module switches from idle-mode to active-mode within 20 ms from the first data reception: this is the "wake up time" of the module. As a consequence, the first character sent when the module is in idle-mode (i.e. the wake up character) won't be a valid communication character because it can't be recognized, and the recognition of the subsequent characters is guaranteed only after the complete wake-up (i.e. after 20 ms).

Figure 26 and Figure 27 show an example of common scenarios and timing constraints:

- HW flow control set in the DCE, and no HW flow control set in the DTE, needed to see the **CTS** line changing on DCE

- Power saving configuration is active and the timeout from last data received to idle-mode start is set to 2000 frames (AT+UPSV=1,2000)

Figure 26 shows the case where DCE is in idle-mode and a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE will return to idle-mode when the timeout from last data received expires. (2000 frames without data reception).

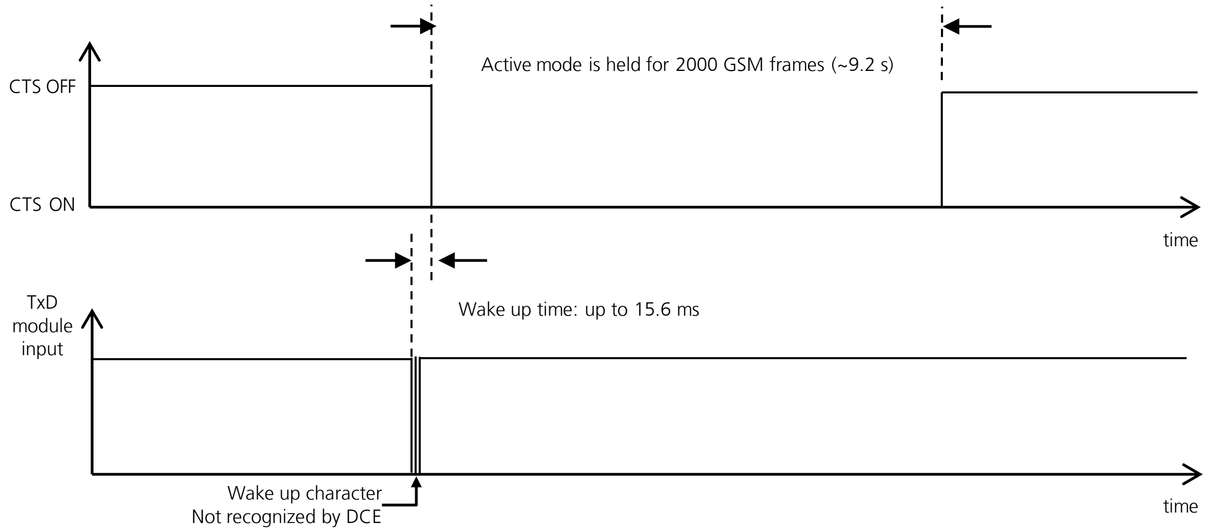

Figure 26: Wake-up via data reception without further communication

Figure 27 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake up character wakes-up the DCE. The other characters must be sent after the "wake up time" of 20 ms. If this condition is satisfied, the characters are recognized by the DCE. The DCE is allowed to re-enter idle-mode after 2000 GSM frames from the latest data reception.

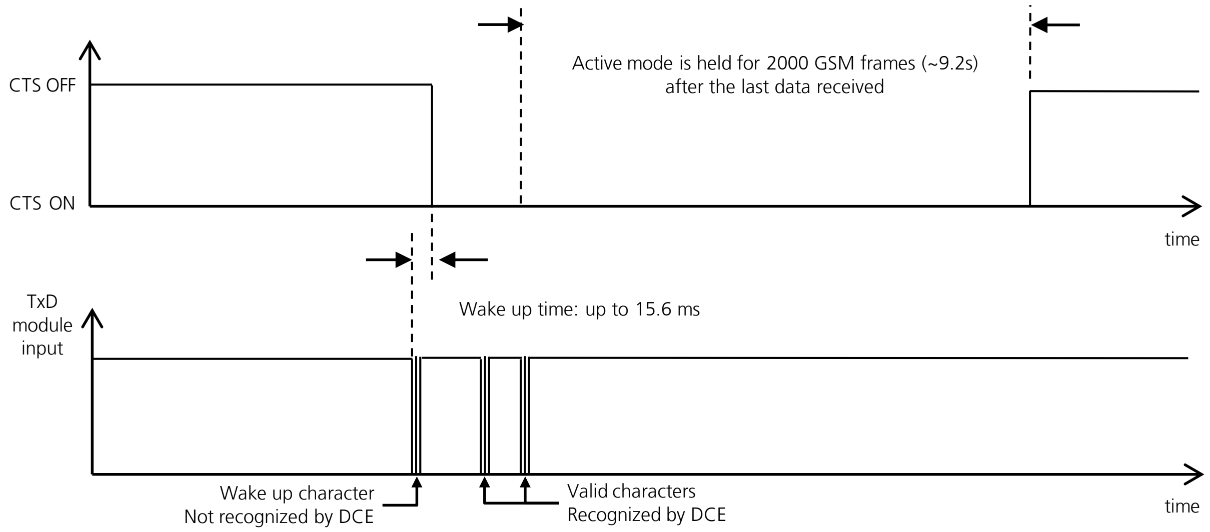

Figure 27: Wake-up via data reception with further communication

☞ LISA-U2 series modules don't wake-up from idle-mode to active-mode via data reception by **TxD** input line, if HW flow control is enabled.

☞ The "wake-up via data reception" feature can't be disabled.

☞ The "wake-up via data reception" feature can be used in both +UPSV=1 and +UPSV=2 case (when **RTS** line is set to OFF).

☞ In command mode, if HW flow control is not implemented by the DTE, the DTE must always send a dummy "AT" to the module before each command line: the first character will not be ignored if the module is in active-mode (i.e. the module will reply "OK"), or it will represent the wake up character if the module is in idle-mode (i.e. the module won't reply).

☞ No dummy "AT" is required from the DTE during connected-mode since the module continues to be in active-mode and doesn't need to be woken-up. Furthermore in data mode a dummy "AT" would affect the data communication.

1.9.2.4 UART application circuits

Providing the full RS-232 functionality (using the complete V.24 link)

For complete RS-232 functionality conforming to ITU Recommendation [4] in DTE/DCE serial communication, the complete UART interface of the module (DCE) must be connected to a 1.8V DTE as described in Figure 28.

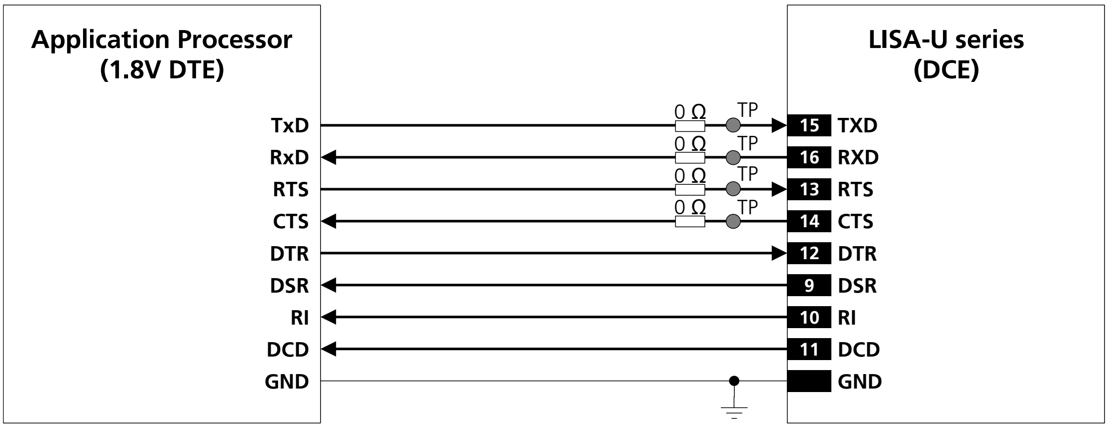

Figure 28: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor is used, appropriate voltage translators must be utilized, as described in Figure 29.

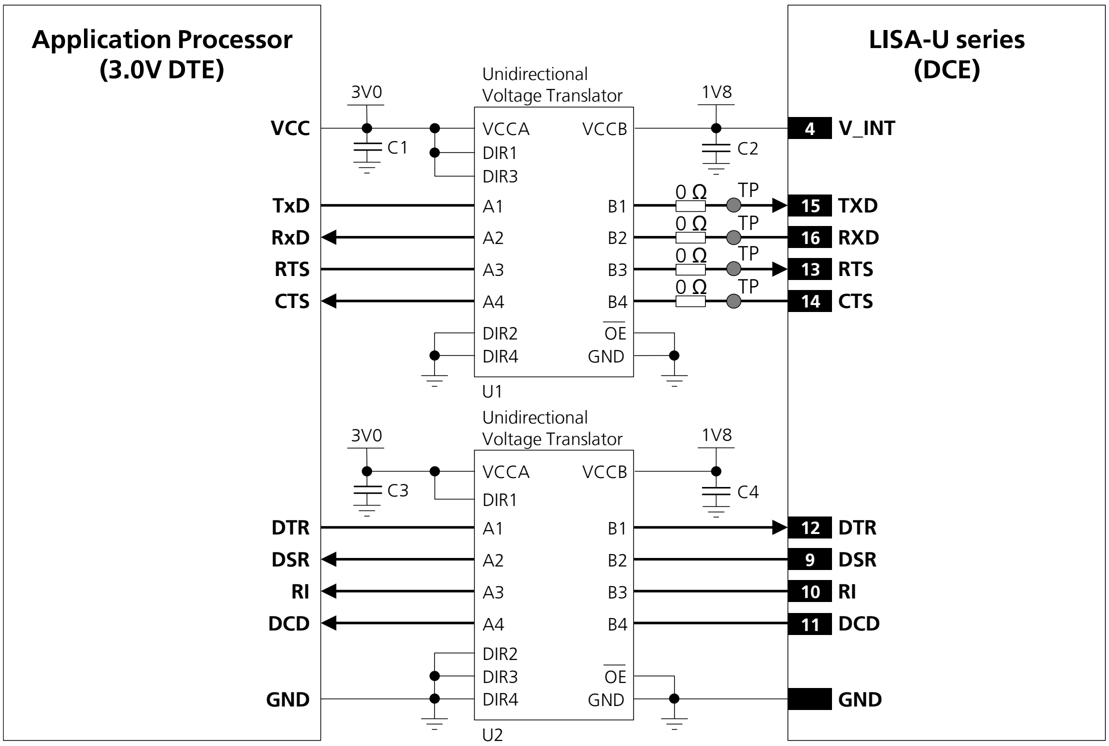

Figure 29: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments

Table 25: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Providing the TxD, RxD, RTS and CTS lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available, the circuit with a 1.8 V Application Processor should be implemented as described in Figure 30:

- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level)
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

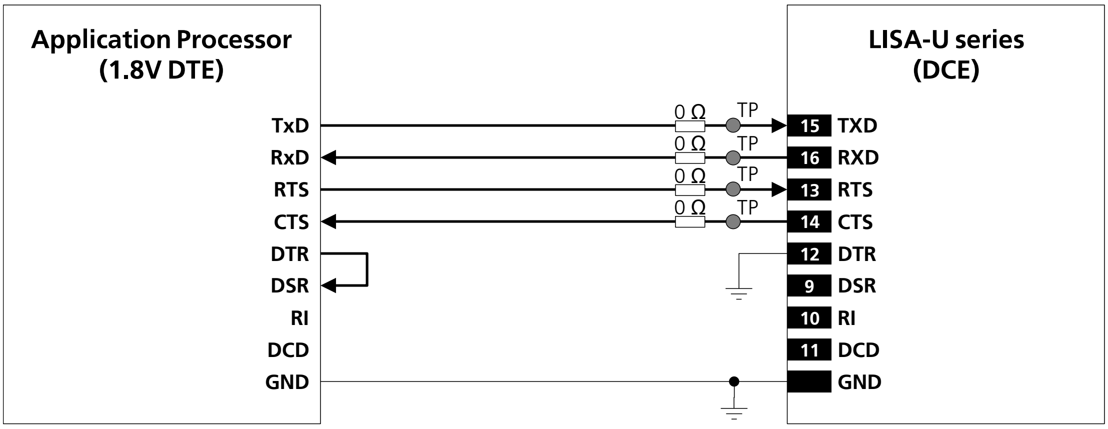

Figure 30: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor is used, proper voltage translator must be utilized, as described in Figure 31.

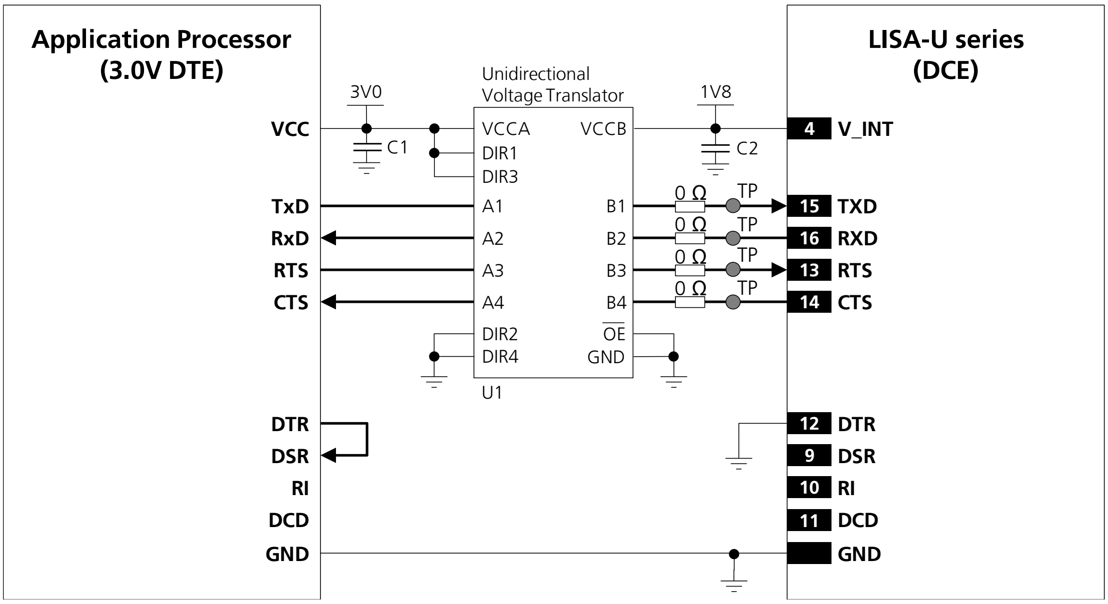

Figure 31: UART interface application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments

Table 26: Component for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

If only **TxD**, **RxD**, **RTS** and **CTS** lines are provided, as implemented in Figure 30 and in Figure 31, the procedure to enable power saving depends on the HW flow-control status. If HW flow-control is enabled (AT&K3, that is the default setting) power saving will be activated by AT+UPSV=1. Through this configuration, when the module is in idle-mode, data transmitted by the DTE will be buffered by the DTE and will be correctly received by the module when active-mode is entered.

If the HW flow-control is disabled (AT&K0), the power saving can be enabled by AT+UPSV=2. The module is in idle-mode until a high-to-low (i.e. OFF-to-ON) transition on the **RTS** input line will switch the module from idle-mode to active-mode in 20 ms. The module will be forced in active-mode if the **RTS** input line is held in the ON state.

Providing the TxD and RxD lines only (not using the complete V24 link)

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available, the circuit with a 1.8 V Application Processor should be implemented as described in Figure 32:

- Connect the module **CTS** output line to the module **RTS** input line, since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, that is the default setting), and **CTS** is active (low electrical level) when the module is in active mode, the UART interface is enabled and the HW flow-control is enabled
- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level)
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

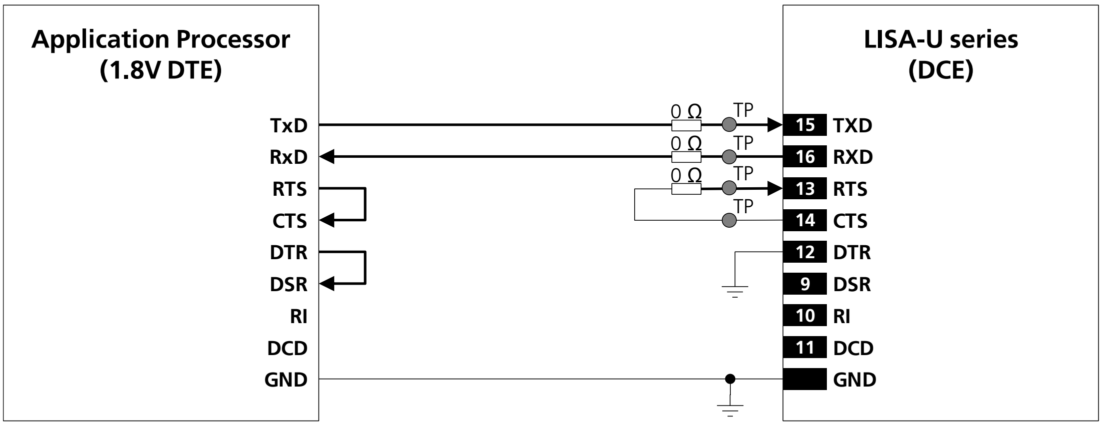

Figure 32: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor is used, proper voltage translator must be utilized, as described in Figure 33.

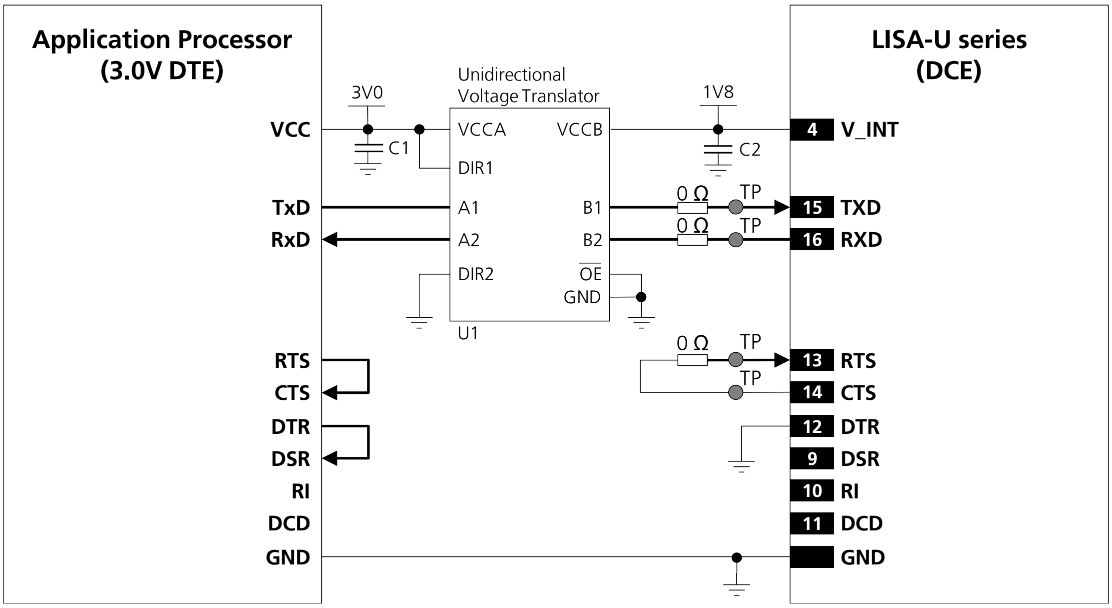

Figure 33: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 27: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

If only **TxD** and **RxD** lines are provided, as described in Figure 32 and in Figure 33, and HW flow-control is disabled (AT&K0), the power saving will be enabled by AT+UPSV=1. The module enters active-mode 20 ms after a low-to-high transition on the **TxD** input line, and the recognition of the subsequent characters is guaranteed until the module is in active-mode.

☞ Data delivered by the DTE can be lost using this configuration and the following settings:

- HW flow-control enabled in the module (AT&K3, that is the default setting)
- Module power saving enabled by AT+UPSV=1
- HW flow-control disabled in the DTE

In this case the first character sent when the module is in idle-mode will be a wake-up character and won't be a valid communication character (refer to chapter 1.9.1.3 for the complete description).

☞ If power saving is enabled the application circuit with the **TxD** and **RxD** lines only is not recommended. During command mode the DTE must send to the module a wake-up character or a dummy "AT" before each command line (refer to chapter 1.9.1.3 for the complete description), but during data mode the wake-up character or the dummy "AT" would affect the data communication.

Additional considerations

☞ If the module USB interface is connected to the application processor, it is highly recommended to provide direct access to **RxD**, **TxD**, **CTS** and **RTS** lines of the module for execution of firmware upgrade over UART and for debug purpose: testpoints can be added on the lines to accommodate the access and a 0 Ω series resistor must be mounted on each line to detach the module pin from any other connected device. Otherwise, if the USB interface is not connected to the application processor, it is highly recommended to provide direct access to **VUSB_DET**, **USB_D+**, **USB_D-** lines for execution of firmware upgrade over USB and for debug purpose. In both cases, provide as well access to **RESET_N** pin, or to the **PWR_ON** pin, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade (see Firmware Update Application Note [17]).

☞ If the UART interface is not used, all the UART interface pins can be left unconnected, but it is highly recommended to provide direct access to the **RxD**, **TxD**, **CTS** and **RTS** lines for execution of firmware upgrade and for debug purpose.

☞ Any external signal connected to the UART interface must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode, when external reset is forced low and during power-on sequence.

1.9.3 USB interface

LISA-U series modules provide a high-speed USB interface at 480 Mb/s compliant with the Universal Serial Bus Revision 2.0 specification [8]. It acts as a USB device and can be connected to any USB host such as a PC or other Application Processor.

The USB-device shall look for all upper-SW-layers like any other serial device. This means that LISA-U series modules emulate all serial control logical lines.

☞ If the logical DTR line isn't enabled by the USB host, the LISA-U1xx-00 modules don't answer to AT commands by the USB interface.

Name	Description	Remarks
VUSB_DET	USB detect input	Apply 5 V typical to enable USB
USB_D+	USB Data Line D+	90 Ω nominal differential impedance. Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [8] are part of the USB pad driver and need not be provided externally.
USB_D-	USB Data Line D-	90 Ω nominal differential impedance. Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [8] are part of the USB pad driver and need not be provided externally.

Table 28: USB pins

☞ The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

1.9.3.1 USB features

LISA-U series modules simultaneously support 6 USB CDC (Communications Device Class) that assure multiple functionalities to the USB physical interface. The 6 available CDCs are configured as described in the following list:

- USB1: AT commands / data connection
- USB2: AT commands / data connection
- USB3: AT commands / data connection
- USB4: GPS tunneling dedicated port
- USB5: 2G and BB trace dedicated port
- USB6: 3G trace dedicated port

All LISA-U2 series modules versions except LISA-U200-00 provide an additional USB CDC:

- USB7: SIM Access Profile dedicated port

The user can concurrently use AT command interface on one CDC and Packet-Switched / Circuit-Switched Data communication on another CDC.

All LISA-U2 series modules versions except LISA-U200-00 support audio over USB capabilities: Audio Device Class is implemented to provide an audio streaming interface, which transfers audio data over isochronous pipes.

USB drivers for Windows XP, Windows Vista, Windows 7, Windows CE 6, Windows EC 7 and Windows Mobile 6.5 are available.

LISA-U1 / LISA-U2 series modules are compatible with standard Linux/Android USB kernel drivers.

LISA-U series module identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor.

VID and PID of LISA-U series modules are the following:

- VID = 0x1546
- PID = 0x1101 for LISA-U1 series
- PID = 0x1102 for LISA-U2 series

If the USB interface of LISA-U series module is connected to the host before the module switch on, or if the module is reset with the USB interface connected to the host, the VID and PID are automatically updated runtime, after the USB detection. First, VID and PID are the following:

- VID = 0x058B
- PID = 0x0041

Then, after a time period (~5 s), VID and PID are updated to the following:

- VID = 0x1546
- PID = 0x1101 for LISA-U1 series
- PID = 0x1102 for LISA-U2 series

1.9.3.2 USB and power saving

If power saving is enabled by AT command (AT+UPSV=1 or AT+UPSV=2), the LISA-U series module automatically enters the USB suspended state when the device has observed no bus traffic for a specified period (refer to the Universal Serial Bus Revision 2.0 specification [8]). In suspended state, the module maintains any internal status as USB device, including its address and configuration. In addition, the module enters the suspended state when the hub port it is attached to is disabled: this is referred to as USB selective suspend. The module exits suspend mode when there is bus activity.

LISA-U series module is capable of USB remote wake-up signaling: i.e. may request the host to exit suspend mode or selective suspend by using electrical signaling to indicate remote wake-up. This notifies the host that it should resume from its suspended mode, if necessary, and service the external event that triggered the suspended USB device to signal the host. Remote wake-up is accomplished using electrical signaling described in the Universal Serial Bus Revision 2.0 specification [8].

When the USB enters suspended state, the average **VCC** module current consumption of LISA-U series module is ~400 µA higher then when the USB is not attached to a USB host.

If power saving is disabled by AT+UPSV=0 and the LISA-U series module is attached to a USB host as USB device, is configured and is not suspended, the average **VCC** module current consumption in fixed active mode is increased to ~40 mA.

1.9.3.3 USB application circuit

Since the module acts as a USB device, the USB supply (5.0 V typ.) must be provided to **VUSB_DET** by the connected USB host. The USB interface is enabled only when a valid voltage as USB supply is detected by the **VUSB_DET** input. Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs few microamperes.

The **USB_D+** and **USB_D-** lines carry the USB serial data and signaling. The lines are used in single ended mode for relatively low speed signaling handshake, as well as in differential mode for fast signaling and data transfer.

USB pull-up or pull-down resistors on pins **USB_D+** and **USB_D-** as required by the Universal Serial Bus Revision 2.0 specification [8] are part of the USB pad driver and do not need to be externally provided.

External series resistors on pins **USB_D+** and **USB_D-** as required by the Universal Serial Bus Revision 2.0 specification [8] are also integrated: characteristic impedance of **USB_D+** and **USB_D-** lines is specified by the USB standard. The most important parameter is the differential characteristic impedance applicable for odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential: signal integrity may be degraded if the PCB layout is not optimal, especially when the USB signaling lines are very long.

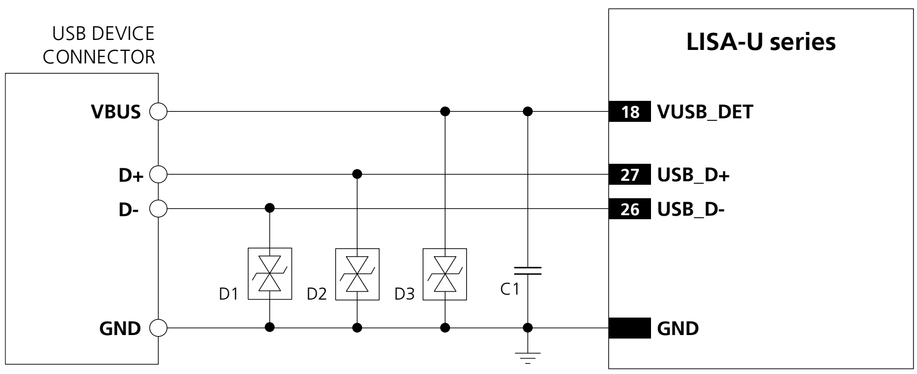

Figure 34: USB Interface application circuit

Reference	Description	Part Number - Manufacturer
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata

Table 29: Component for USB application circuit

☞ If the USB interface is not connected to the application processor, it is highly recommended to provide direct access to the **VUSB_DET**, **USB_D+**, **USB_D-** lines for execution of firmware upgrade over USB and for debug purpose: testpoints can be added on the lines to accommodate the access. Otherwise, if the USB interface is connected to the application processor, it is highly recommended to provide direct access to the **RxD**, **TxD**, **CTS** and **RTS** lines for execution of firmware upgrade over UART and for debug purpose. In both cases, provide as well access to **RESET_N** pin, or to the **PWR_ON** pin, or enable the

DC supply connected to the **VCC** pin to start the module firmware upgrade (see Firmware Update Application Note [17]).

☞ If the USB interface is not used, the **USB_D+**, **USB_D-** and **VUSB_DET** pins can be left unconnected, but it is highly recommended to provide direct access to the lines for execution of firmware upgrade and for debug purpose.

1.9.4 SPI interface

SPI is a master-slave protocol: the module runs as an SPI slave, i.e. it accepts AT commands on its SPI interface without specific configuration. The SPI-compatible synchronous serial interface cannot be used for FW upgrade.

The standard 3-wire SPI interface includes two signals to transmit and receive data (**SPI_MOSI** and **SPI_MISO**) and a clock signal (**SPI_SCLK**).

LISA-U series modules provide two handshake signals (**SPI_MRDY** and **SPI_SRDY**), added to the standard 3-wire SPI interface, implementing the 5-wire Inter Processor Communication (IPC) interface.

The purpose of the IPC interface is to achieve high speed communication (up to 26 Mb/s) between two processors following the same IPC specifications: the module baseband processor and an external processor. High speed communication is possible only if both sides follow the same Inter Processor Communication (IPC) specifications.

Name	Description	Remarks
SPI_MISO	SPI Data Line. Master Input, Slave Output	Module Output. Idle high. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). MSB is shifted first.
SPI_MOSI	SPI Data Line. Master Output, Slave Input	Module Input. Idle high. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). MSB is shifted first. Internal active pull-up to V_INT (1.8 V) enabled.
SPI_SCLK	SPI Serial Clock. Master Output, Slave Input	Module Input. Idle low (CPOL=0). Up to 26 MHz supported. Internal active pull-down to GND enabled.
SPI_MRDY	SPI Master Ready to transfer data control line. Master Output, Slave Input	Module Input. Idle low. Internal active pull-down to GND enabled.
SPI_SRDY	SPI Slave Ready to transfer data control line. Master Input, Slave Output	Module Output. Idle low.

Table 30: SPI interface signals

☞ The SPI interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting a low capacitance (i.e. less than 10 pF) ESD protection (e.g. AVX USB0002 varistor array) on the lines connected to these pins, close to accessible points.

1.9.4.1 IPC communication protocol overview

The module runs as an SPI slave, i.e. it accepts AT commands on its SPI interface without specific configuration. The SPI-device shall look for all upper-SW-layers like any other serial device. This means that LISA-U series modules emulate all serial logical lines: the transmission and the reception of the data are similar to an asynchronous device.

Two additional signals (**SPI_MRDY** and **SPI_SRDY**) are added to the SPI lines to communicate the state of readiness of the two processors: they are used as handshake signals to implement the data flow.

The function of the **SPI_MRDY** and **SPI_SRDY** signals is twofold:

- For transmitting data the signal indicates to the data receiver that data is available to be transmitted
- For receiving data the signal indicates to the transmitter that the receiver is ready to receive data

Due to this setup it is possible to use the control signals as interrupt lines waking up the receiving part when data is available for transfer. When the handshaking has taken place, the transfer occurs just as if it were a standard SPI interface without chip select functionality (i.e. one master - one slave setup).

SPI_MRDY is used by the application processor (i.e. the master) to indicate to the module baseband processor (i.e. the slave) that it is ready to transmit or receive (IPC master ready signal), and can also be used by the application processor to wake up the module baseband processor if it is in idle-mode.

SPI_SRDY line is used by the module baseband processor (i.e. the slave) to indicate to the application processor (i.e. the master) that it is ready to transmit or receive (IPC slave ready signal), and can also be used by the module baseband processor to wake up the application processor if it is in hibernation.

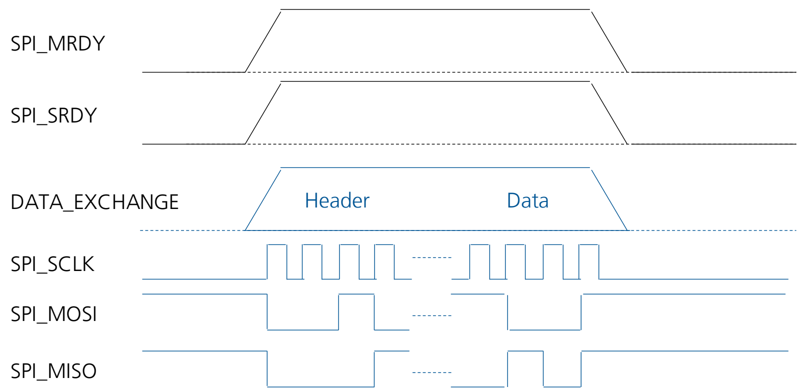

Figure 35: IPC Data Flow: SPI_MRDY and SPI_SRDY line usage combined with the SPI protocol

For the correct implementation of the SPI protocol, the frame size is known by both sides before a packet transfer of each packet. The frame is composed by a header with fixed size (always 4 bytes) and a payload with variable length (must be a multiple of 4 bytes).

The same amount of data is exchanged in both directions simultaneously. Both sides set their readiness lines (**SPI_MRDY** / **SPI_SRDY**) independently when they are ready to transfer data. For the correct transmission of the data the other side must wait for the activating interrupt to allow the transfer of the other side.

The master starts the clock shortly after **SPI_MRDY** and **SPI_SRDY** are set to active. The number of clock periods sent by the master is exactly that one of the frame-size to be transferred. The **SPI_SRDY** line will be set low after the master sets the clock line to idle state. The **SPI_MRDY** line is also set inactive after the clock line is set idle, but in case of a big transfer containing multiple packets, the **SPI_MRDY** line stays active.

1.9.4.2 IPC communication and power saving

If power saving is enabled by AT command (AT+UPSV=1 or AT+UPSV=2), the LISA-U series module automatically enters idle-mode when the master indicates that it is not ready to transmit or receive by the **SPI_MRDY** signal, or when the LISA-U series module itself doesn't transfer data.

1.9.4.3 IPC communication examples

In the following, three IPC communication scenarios are described:

- Slave initiated data transfer, with a sleeping master
- Master initiated data transfer, with a sleeping slave
- Slave ended data transfer

Slave initiated transfer with a sleeping master

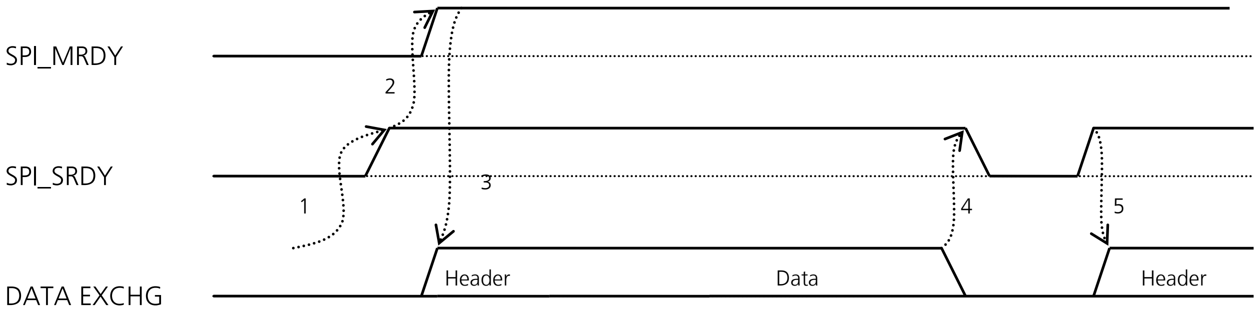

Figure 36: Data transfer initiated by LISA-U series module (slave), with a sleeping application processor (master)

When the master is sleeping (idle-mode), the following actions happen:

1. The slave indicates the master that is ready to send data by activating **SPI_SRDY**
2. When the master becomes ready to send, it signalizes this by activating **SPI_MRDY**
3. The master activates the clock and the two processors exchange the communication header and data
4. If the data has been exchanged, the slave deactivates **SPI_SRDY** to process the received information. The master does not need to de-assert **SPI_MRDY** as it controls the **SPI_SCLK**
5. After the preparation, the slave activates again **SPI_SRDY** and wait for **SPI_SCLK** activation. When the clock is active, all the data is transferred without intervention. If there is more data to transfer (flag set in any of the headers), the process will repeat from step 3

Master initiated transfer with a sleeping slave

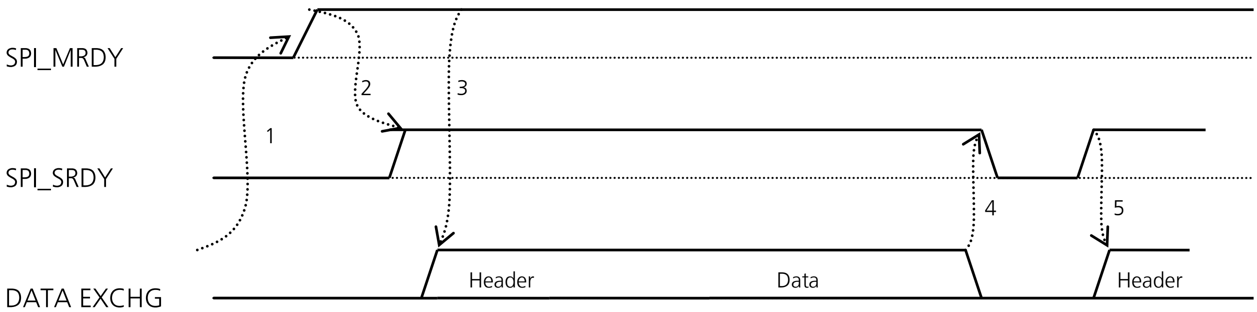

Figure 37: Data transfer initiated by application processor (master) with a sleeping LISA-U series module (slave)

When the slave is sleeping (idle-mode), the following actions happen:

1. The Master wakes the slave by setting the **SPI_MRDY** line active
2. As soon as the slave is awake, it signals it by activating **SPI_SRDY**
3. The master activates the clock and the two processors exchange the communication header and data

4. If the data has been exchanged, the slave deactivates **SPI_SRDY** to process the received information. The master does not need to de-assert **SPI_MRDY** as it controls the **SPI_SCLK**
5. After the preparation, the slave activates again **SPI_SRDY** and wait for **SPI_SCLK** activation. When the clock is active, all data is transferred without intervention. If there is more data to transfer (flag set in any of the headers), the process will repeat from step 3

Slave ended transfer

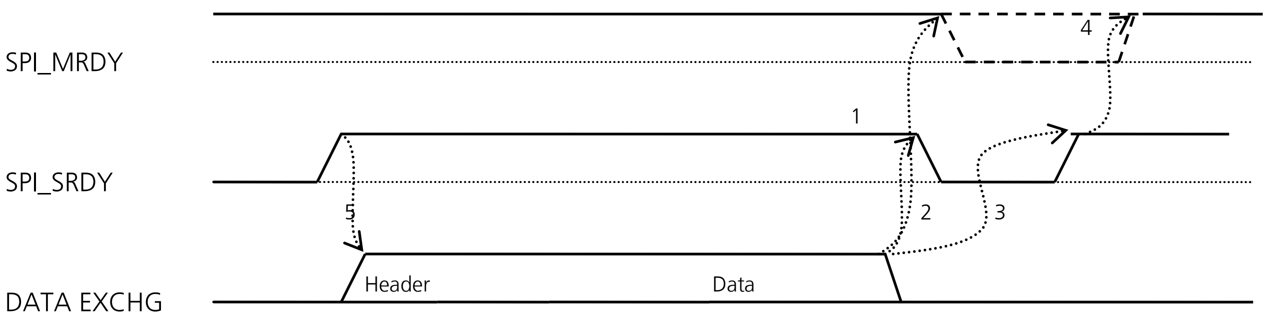

Figure 38: Data transfer terminated and then restarted by LISA-U series module (slave)

Starting from the state where data transfer is ongoing, the following actions will happen:

1. In case of the last transfer, the master will lower its **SPI_MRDY** line. After the data-transfer is finished the line must be low. If the slave has already set its **SPI_SRDY** line, the master must raise its line to initiate the next transfer (slave-waking-procedure)
2. If the data has been exchanged, the slave will deactivate **SPI_SRDY** to process the received information. This is the normal behavior
3. The slave will indicate the master that is ready to send data by activating **SPI_SRDY**
4. When the master is ready to send, it will signalize this by activating **SPI_MRDY**. This is optional, when **SPI_MRDY** is low before
5. The slave indicates immediately after a transfer termination that it is ready to start transmission again. In this case the slave will raise **SPI_SRDY** again. The **SPI_MRDY** line can be either high or low: the master has only to ensure that the **SPI_SRDY** change will be detected correctly via interrupt

☞ For more details regarding IPC communication protocol please refer to SPI Application Note [18].

1.9.4.4 IPC application circuit

SPI_MOSI is the data line input for the module since it runs as SPI slave: it must be connected to the data line output (MOSI) of the application processor that runs as an SPI master.

SPI_MISO is the data line output for the module since it runs as SPI slave: it must be connected to the data line input (MISO) of the application processor that runs as an SPI master.

SPI_SCLK is the clock input for the module since it runs as SPI slave: it must be connected to the clock line output (SCLK) of the application processor that runs as an SPI master.

SPI_MRDY is an input for the module able to detect an external interrupt which comes from the application processor.

SPI_SRDY is an output for the module, and the application processor should be able to detect an external interrupt which comes from the module on its connected pin.

Signal integrity of the high speed data lines may be degraded if the PCB layout is not optimal, especially when the SPI lines are very long: keep routing short and minimize parasitic capacitance to preserve signal integrity.

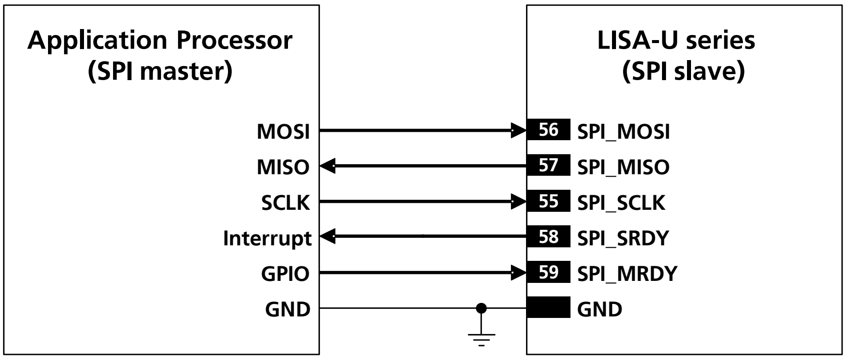

Figure 39: IPC Interface application circuit

☞ If direct access to the USB or the UART interfaces of the module is not provided, it is recommended to provide direct access to the **SPI_MOSI**, **SPI_MISO**, **SPI_SCLK**, **SPI_MRDY**, **SPI_SRDY** lines of the module for debug purpose: testpoints can be added on the lines to accommodate the access and a 0 Ω series resistor must be mounted on each line to detach the module pin from any other connected device.

☞ If the SPI/IPC interface is not used, the **SPI_MOSI**, **SPI_MISO**, **SPI_SCLK**, **SPI_MRDY**, **SPI_SRDY** pins can be left unconnected.

☞ Any external signal connected to the SPI / IPC interface must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode, when external reset is forced low and during power-on sequence.

1.9.5 MUX Protocol (3GPP 27.010)

LISA-U series modules have a software layer with MUX functionality, 3GPP TS 27.010 Multiplexer Protocol [7], available either on the UART or on the SPI physical link. The USB interface doesn't support the multiplexer protocol.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use AT command interface on one MUX channel and Packet-Switched / Circuit-Switched Data communication on another MUX channel. The multiplexer protocol can be used on one serial interface (UART or SPI) at a time. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GPS, AT commands in general. This permits, for example, SMS to be transferred to the DTE when a data connection is in progress.

The following virtual channels are defined:

- Channel 0: control channel
- Channel 1 – 5: AT commands /data connection
- Channel 6: GPS tunneling

All LISA-U2 series modules versions except LISA-U200-00 provide an additional channel:

- Channel 7: SIM Access Profile dedicated port

For more details please refer to GSM Mux implementation Application Note [15].

1.10 DDC (I²C) interface

1.10.1 Overview

An I²C compatible Display Data Channel (DDC) interface for communication with u-blox GPS receivers is available on LISA-U series modules. The communication between a u-blox wireless module and a u-blox GPS receiver is only provided by this DDC (I²C) interface.

Name	Description	Remarks
SCL	I²C bus clock line	Open drain. External pull-up required.
SDA	I²C bus data line	Open drain. External pull-up required.

Table 31: DDC pins

☞ The DDC (I²C) interface pins ESD sensitivity rating is 1 kV (HBM according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins, close to accessible points.

u-blox has implemented special features in LISA-U series wireless modules to ease the design effort required for the integration of a u-blox wireless module with a u blox GPS receiver.

Combining a u-blox wireless module with a u-blox GPS receiver allows designers to have full access to the GPS receiver directly via the wireless module: it relays control messages to the GPS receiver via a dedicated DDC (I²C) interface. A 2nd interface connected to the GPS receiver is not necessary: AT commands via the UART serial interface of the wireless module allows a fully control of the GPS receiver from any host processor.

LISA-U series modules feature embedded GPS aiding that is a set of specific features developed by u-blox to enhance GPS performance, decreasing Time To First Fix (TTFF), thus allowing to calculate the position in a shorter time with higher accuracy.

The DDC (I²C) interface of all LISA-U2 series modules versions except LISA-U200-00 can be used to communicate with u-blox GPS receivers and at the same time to control an external audio codec: the LISA-U2 series module acts as an I²C master which can communicate to two I²C slaves as allowed by the I²C bus specifications. Refer to section 1.11.2 for an application circuit with an external audio codec.

☞ LISA-U200-00 modules versions don't support an I²C compatible Display Data Channel (DDC) interface for communication with u-blox GPS receivers and don't feature embedded GPS aiding.

☞ For more details regarding the handling of the DDC (I²C) interface and the GPS aiding features please refer to u-blox AT Commands Manual [3] (AT+UGPS, AT+UGPRF, AT+UGPIOC commands) and GPS Implementation Application Note [16].

1.10.2 DDC application circuit

The DDC (I²C) interface of LISA-U series modules is used to connect the wireless module to a u-blox GPS receiver: the communication with the u-blox GPS receiver by DDC (I²C) interface is enabled by the AT+UGPS command (for more details refer to u-blox AT Commands Manual [3]). The **SDA** and **SCL** lines must be connected to the DDC (I²C) interface pins of the u-blox GPS receiver (i.e. the SDA2 and SCL2 pins of the u-blox GPS receiver) on the application board to allow the communication between the wireless module and the u-blox GPS receiver.

To be compliant to the I²C bus specifications, the module bus interface pads are open drain output and pull up resistors must be used. Since the pull-up resistors are not mounted on the module, they must be mounted externally. Resistor values must conform to the I²C bus specifications [9]. If a LISA-U series module is connected by the DDC (I²C) bus to a u-blox GPS receiver (only one device can be connected on the DDC bus), use a pull-up resistor of 4.7 kΩ. Pull-ups must be connected to a supply voltage of 1.8 V (typical), since this is the voltage domain of the DDC pins. **V_INT** digital interfaces supply output can be used to provide 1.8 V for the pull-ups (for detailed electrical characteristics see LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]).

DDC Slave-mode operation is not supported, the module can act as master only.

Two lines, serial data (**SDA**) and serial clock (**SCL**), carry information on the bus. **SCL** is used to synchronize data transfers, and **SDA** is the data line. Since both lines are open drain outputs, the DDC devices can only drive them low or leave them open. The pull-up resistor pulls the line up to the supply rail if no DDC device is pulling it down to GND. If the pull-ups are missing, **SCL** and **SDA** lines are undefined and the DDC bus will not work.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus will increase the capacitance. If the bus capacitance is increased, use pull-up resistors with nominal resistance value lower than 4.7 kΩ, to match the I²C bus specifications [9].regarding rise and fall times of the signals.

☞ Capacitance and series resistance must be limited on the bus to match the I²C specifications (1.0 µs is the maximum allowed rise time on the **SCL** and **SDA** lines): route connections as short as possible.

☞ If the pins are not used as DDC bus interface, they can be left unconnected.

LISA-U series modules support these GPS aiding types:

- Local aiding
- AssistNow Online
- AssistNow Offline
- AssistNow Autonomous

The embedded GPS aiding features can be used only if the DDC (I²C) interface of the wireless module is connected to the u-blox GPS receivers.

The GPIO pins can handle:

- GPS receiver power-on/off ("GPS supply enable" function provided by **GPIO2**)
- The wake up from idle-mode when the GPS receiver is ready to send data ("GPS data ready" function provided by **GPIO3**)
- The RTC synchronization signal to the GPS receiver ("GPS RTC sharing" function provided by **GPIO4**)

☞ LISA-U1xx-00 modules versions don't support the following further features related to GPS functionality:
  - LISA-U1xx-00 modules versions don't enter idle-mode when the DDC (I²C) interface is enabled by the AT+UGPS command, even if power saving is enabled by the AT+UPSV command
  - LISA-U1xx-00 modules versions don't support "GPS data ready" and "GPS RTC sharing" functions
  - LISA-U1xx-00 modules versions don't support AssistNow Autonomous GPS aiding

The **GPIO2** is by default configured to provide the "GPS supply enable" function (parameter <gpio_mode> of AT+UGPIOC command set to 3 by default), to enable or disable the supply of the u-blox GPS receiver connected to the wireless module by the AT+UGPS command. The pin is set as

- Output / High, to switch on the u-blox GPS receiver, if the parameter <mode> of AT+UGPS command is set to 1
- Output / Low, to switch off the u-blox GPS receiver, if the parameter <mode> of AT+UGPS command is set to 0 (default setting)

The pin must be connected to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GPS receiver on the application board.

The “GPS supply enable” function improves the power consumption of the GPS receiver. When the GPS functionality is not required, the GPS receiver can be completely switched off by the wireless module that is controlled by the application processor with AT commands.

The **GPIO3** is by default configured to provide the “GPS data ready” function (parameter <gpio_mode> of AT+UGPIOC command set to 4 by default), to sense when the u-blox GPS receiver connected to the wireless module is ready to send data by the DDC (I^2C) interface. The pin will be set as

- Input, to sense the line status, waking up the wireless module from idle-mode when the u-blox GPS receiver is ready to send data by the DDC (I^2C) interface, if the parameter <mode> of +UGPS AT command is set to 1 and the parameter <GPS_IO_configuration> of +UGPRF AT command is set to 16
- Tri-state with an internal active pull-down enabled, otherwise (default setting)

The pin that provides the “GPS data ready” function must be connected to the data ready output of the u-blox GPS receiver (i.e. the pin TxD1 of the u-blox GPS receiver) on the application board.

The “GPS data ready” function provides an improvement in the power consumption of the wireless module. When power saving is enabled in the wireless module by the AT+UPSV command and the GPS receiver doesn’t send data by the DDC (I^2C) interface, the module automatically enters idle-mode whenever possible. With the “GPS data ready” function the GPS receiver can indicate to the wireless module that it is ready to send data by the DDC (I^2C) interface: the GPS receiver can wake up the wireless module if it is in idle-mode, so that data sent by the GPS receiver will not be lost by the wireless module even if power saving is enabled.

The **GPIO4** is by default configured to provide the “GPS RTC sharing” function (parameter <gpio_mode> of +UGPIOC AT command set to 5), to provide an RTC (Real Time Clock) synchronization signal at the power up of the u-blox GPS receiver connected to the wireless module. The pin will be set as

- Output, to provide an RTC synchronization signal to the u-blox GPS receiver for RTC sharing if the parameter <mode> of AT+UGPS command is set to 1 and the parameter <GPS_IO_configuration> of +UGPRF AT command is set to 32
- Output / Low, otherwise (default setting)

The pin that provides the “GPS RTC sharing” function must be connected to the RTC synchronization signal of the u-blox GPS receiver (i.e. the pin EXTINT0 of the u-blox GPS receiver) on the application board.

The “GPS RTC sharing” function provides improved GPS receiver performance, decreasing the Time To First Fix (TTFF), and thus allowing to calculate the position in a shorter time with higher accuracy. When GPS local aiding is enabled, the wireless module automatically uploads data such as position, time, ephemeris, almanac, health and ionospheric parameter from the GPS receiver into its local memory, and restores this to the GPS receiver at the next power up of the GPS receiver.

The application circuit for connecting a LISA-U series wireless module to a u-blox 1.8 V GPS receiver is illustrated in Figure 40.

SDA and **SCL** pins of the LISA-U series wireless module are directly connected to the relative pins of the u-blox 1.8 V GPS receiver, with appropriate pull-up resistors.

GPIO3 and **GPIO4** pins are directly connected respectively to the **TxD1** and **EXTINT0** pins of the u-blox 1.8 V GPS receiver to provide “GPS data ready” and “GPS RTC sharing” functions.

A pull-down resistor is mounted on the **GPIO2** line to avoid a switch on of the GPS module when the LISA-U series module is in the internal reset state.

The **V_BCKP** supply output of the LISA-U series wireless module is connected to the **V_BCKP** backup supply input pin of the GPS receiver to provide the supply for the GPS real time clock and backup RAM when the **VCC** supply of the wireless module is within its operating range and the **VCC** supply of the GPS receiver is disabled. This enables the u-blox GPS receiver to recover from a power breakdown with either a Hotstart or a Warmstart (depending on the duration of the GPS **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

☞ "GPS data ready" and "GPS RTC sharing" functions are not supported by all u-blox GPS receivers HW or ROM/FW versions. Refer to the GPS Implementation Application Note [16] or to the Hardware Integration Manual of the u-blox GPS receivers for the supported features.

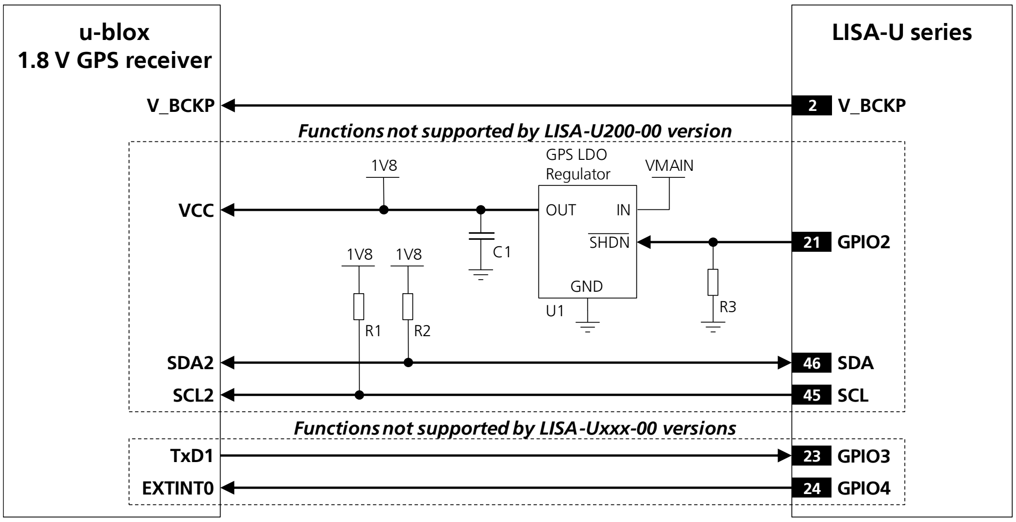

Figure 40: DDC Application circuit for u-blox 1.8 V GPS receiver

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1	Voltage Regulator for GPS Receiver	See GPS Receiver Hardware Integration Manual

Table 32: Components for DDC application circuit for u-blox 1.8 V GPS receiver

The application circuit for the connection of a LISA-U series wireless module to a u-blox 3.0 V GPS receiver is illustrated in Figure 41.

If a u-blox 3 V GPS receiver is used, the **SDA**, **SCL**, **GPIO3** and **GPIO4** pins of the LISA-U series wireless module cannot be directly connected to the u-blox 3 V GPS receiver: a proper I^2C-bus Bidirectional Voltage Translator must be used for the **SDA** and **SCL** signals, and a general purpose Voltage Translator must be used for the **GPIO3** and **GPIO4** signals. The **V_BCKP** supply output of the wireless module can be directly connected to the **V_BCKP** backup supply input pin of the GPS receiver as in the application circuit for a u-blox 1.8 V GPS receiver.

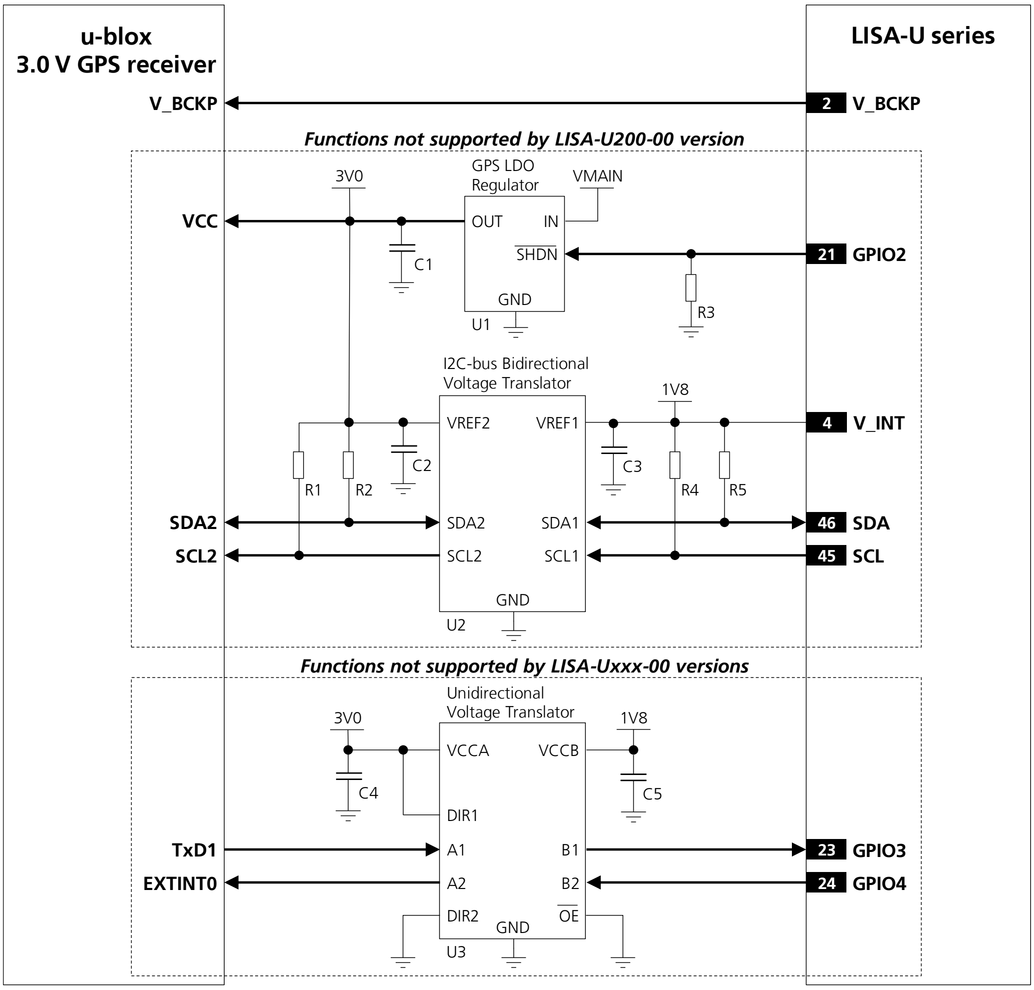

Figure 41: DDC Application circuit for u-blox 3.0 V GPS receiver

Reference	Description	Part Number - Manufacturer
R1, R2, R4, R5	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3, C4, C5	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1	Voltage Regulator for GPS Receiver	See GPS Receiver Hardware Integration Manual
U2	I2C-bus Bidirectional Voltage Translator	PCA9306DCURG4 - Texas Instruments
U3	Generic Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 33: Components for DDC application circuit for u-blox 3.0 V GPS receiver

1.11 Audio Interface

LISA-U120 and LISA-U130 modules provide analog and digital input/output audio interfaces:

- Differential analog audio input (**MIC_P**, **MIC_N**) and differential analog audio output (**SPK_P**, **SPK_N**)
- 4-wire I²S digital audio interface (**I2S_CLK**, **I2S_RXD**, **I2S_TXD** and **I2S_WA**)

All LISA-U2 series modules versions except LISA-U200-00 provide two digital input/output audio interfaces:

- First 4-wire I²S digital audio interface (**I2S_CLK**, **I2S_RXD**, **I2S_TXD** and **I2S_WA**)
- Second 4-wire I²S digital audio interface (**I2S1_CLK**, **I2S1_RXD**, **I2S1_TXD** and **I2S1_WA**)

Audio signal routing can be controlled by the dedicated AT command +USPM (refer to u-blox AT Commands Manual [3]). This command allows setting the audio path mode, composed by the uplink audio path and the downlink audio path.

Each uplink path mode defines the physical input (i.e. the analog or the digital audio input) and the set of parameters to process the uplink audio signal (uplink gains, uplink digital filters, echo canceller parameters). For example the "Headset microphone" uplink path uses the differential analog audio input with the default parameters for the headset profile.

Each downlink path mode defines the physical output (i.e. the analog or the digital audio output) and the set of parameters to process the downlink audio signal (downlink gains, downlink digital filters and sidetone). For example the "Mono headset" downlink path uses the differential analog audio output with the default parameters for the headset profile.

The set of parameters to process the uplink or the downlink audio signal can be changed with dedicated AT commands for each uplink or downlink path and then stored in two profiles in the non volatile memory (refer to u-blox AT Commands Manual [3] for Audio parameters tuning commands).

1.11.1 Analog Audio interface

☞ LISA-U100, LISA-U110 and LISA-U2 series modules versions don't support analog audio interface.

1.11.1.1 Uplink path (differential analog audio input)

The pins related to the differential analog audio input are:

- **MIC_P / MIC_N**: Differential analog audio signal inputs (positive/negative). These two pins are provided with internal series 100 nF capacitors for DC blocking that connect the module pads to the differential input of a Low Noise Amplifier. The LNA output is internally connected to the digital processing system by an integrated sigma-delta analog-to-digital converter

The analog audio input is selected when the parameter <main_uplink> in AT+USPM command is set to "Headset microphone", "Handset microphone" or "Hands-free microphone": the uplink analog path profiles use the same physical input but have different sets of audio parameters (for more details please refer to u-blox AT Commands Manual [3], AT+USPM, AT+UMGC, AT+UUBF, AT+UHFP commands).

There is no microphone supply pin available on the module: an external low noise LDO voltage regulator should be added to provide a proper supply for a microphone.

Detailed electrical characteristics of the differential analog audio input can be found in the LISA-U1 series Data Sheet [1].

1.11.1.2 Downlink path (differential analog audio output)

The pins related to the differential analog audio output are:

- **SPK_P / SPK_N**: Differential analog audio signal output (positive/negative). These two pins are internally directly connected to the differential output of a low power audio amplifier, for which the input is internally connected to the digital processing system by to an integrated digital-to-analog converter

The analog audio output is selected when the parameter <main_downlink> in AT+USPM command is set to "Normal earpiece", "Mono headset" or "Loudspeaker": the downlink analog path profiles use the same physical output but have different sets of audio parameters (for more details please refer to u-blox AT Commands Manual [3], AT+USPM, AT+USGC, AT+UDBF, AT+USTN commands).

The differential analog audio output can be directly connected to a headset earpiece or handset earpiece but is not able to drive an 8 Ω speaker.

Detailed electrical characteristics of the differential audio output can be found in LISA-U1 series Data Sheet [1].

⚠ **Warning: excessive sound pressure from headphones can cause hearing loss.**

Table 34 lists the signals related to analog audio functions.

Name	Module	Description	Remarks
MIC_P	LISA-U120 LISA-U130	Differential analog audio input (Positive)	Shared for all uplink analog path modes: handset, headset, hands-free mode. Internal DC blocking capacitor.
MIC_N	LISA-U120 LISA-U130	Differential analog audio input (Negative)	Shared for all uplink analog path modes: handset, headset, hands-free mode. Internal DC blocking capacitor.
SPK_P	LISA-U120 LISA-U130	Differential analog audio output (Positive)	Shared for all uplink analog path modes: earpiece, headset, loudspeaker mode.
SPK_N	LISA-U120 LISA-U130	Differential analog audio output (Negative)	Shared for all uplink analog path modes: earpiece, headset, loudspeaker mode.

Table 34: Analog audio interface pins

☞ The audio pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins, close to accessible points.

☞ All corresponding differential audio lines must be routed in pairs, be embedded in GND (have the ground lines as close as possible to the audio lines), and maintain distance from noisy lines such as **VCC** and from components such as switching regulators.

☞ If the audio pins are not used, they can be left unconnected on the application board.

1.11.1.3 Headset mode

Headset mode is the default audio operating mode of the LISA-U120 and LISA-U130 modules. The headset profile is configured when the uplink audio path is set to "Headset microphone" and the downlink audio path is set to "Mono headset" (refer to u-blox AT Commands Manual [3]: AT+USPM command: <main_uplink>, <main_downlink> parameters):

- Headset microphone must be connected to the module differential input **MIC_P / MIC_N**
- Headset receiver must be connected to the module differential output **SPK_P / SPK_N**

Figure 42 shows an example of an application circuit connecting a headset (with a 2.2 kΩ electret microphone and a 32 Ω receiver) to the LISA-U120 and LISA-U130 modules, with an external low noise LDO voltage regulator to provide a proper supply for the microphone.

☞ Mount an 82 nH series inductor (e.g. Murata LQG15HS82NJ02) on each microphone line, and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) on all audio lines to minimize RF coupling and TDMA noise.

☞ The physical width of the audio outputs lines on the application board must be wide enough to minimize series resistance.

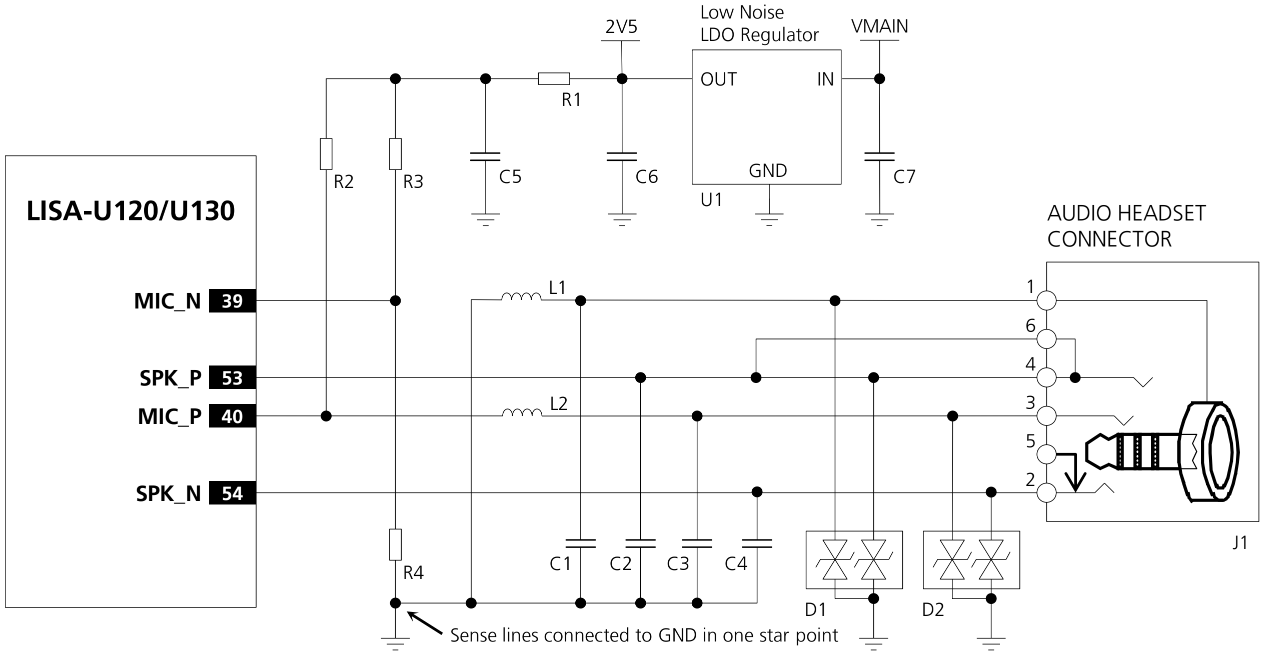

Figure 42: Headset mode application circuit

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JA01 – Murata
C5, C6, C7	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
L1, L2	82 nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
J1	Audio Headset 2.5 mm Jack Connector	SJ1-42535TS-SMT – CUI, Inc.
R1, R2, R3, R4	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
U1	Low Noise LDO Linear Regulator 2.5 V 300 mA	LT1962EMS8-2.5#PBF- Linear Technology

Table 35: Example of components for headset jack connection

1.11.1.4 Handset mode

The handset profile is configured when the uplink audio path is set to "Handset microphone" and the downlink audio path is set to "Normal earpiece" (refer to u-blox AT commands manual [3]: AT+USPM command: <main_uplink>, <main_downlink> parameters):

- Handset microphone must be connected to the module differential input **MIC_P / MIC_N**
- Handset receiver must be connected to the module differential output **SPK_P / SPK_N**

Figure 43 shows an example of an application circuit connecting a handset (with a 2.2 kΩ electret microphone and a 32 Ω receiver) to the LISA-U120 and LISA-U130 modules, with an external low noise LDO voltage regulator to provide a proper supply for the microphone.

☞ Mount an 82 nH series inductor (e.g. Murata LQG15HS82NJ02) on each microphone line and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) on all audio lines to minimize RF coupling and TDMA noise.

☞ The physical width of the audio outputs lines on the application board must be wide enough to minimize series resistance.

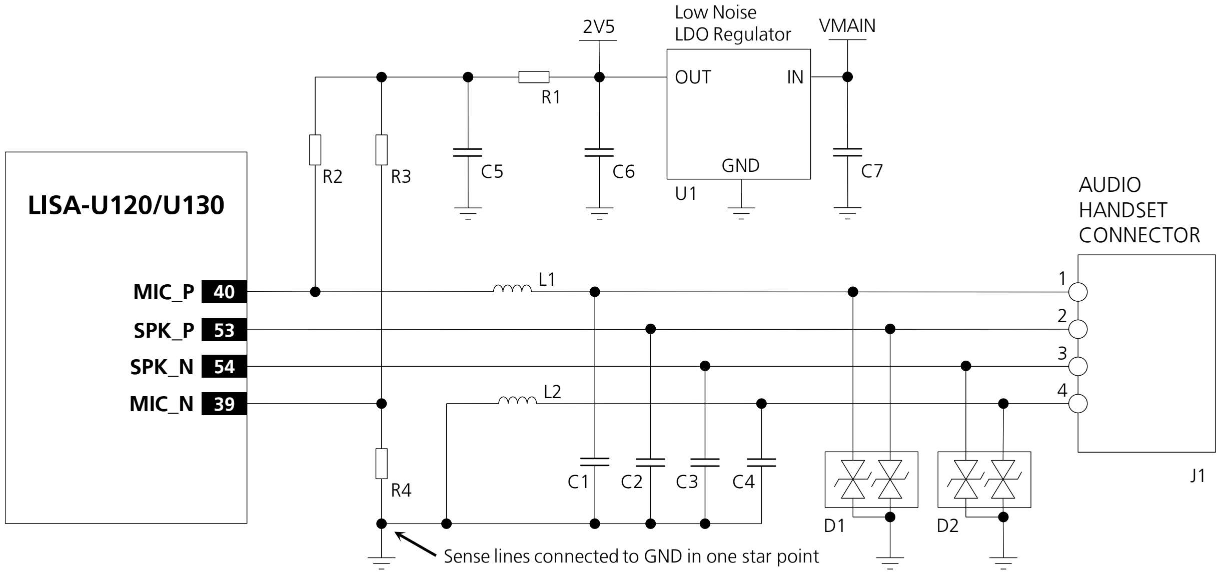

Figure 43: Handset mode application circuit

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JA01 – Murata
C5, C6, C7	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
L1, L2	82nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
J1	Audio Handset Jack Connector, 4Ckt (4P4C)	52018-4416 – Molex
R1, R2, R3, R4	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
U1	Low Noise LDO Linear Regulator 2.5 V 300 mA	LT1962EMS8-2.5#PBF- Linear Technology

Table 36: Example of components for handset connection

1.11.1.5 Hands-free mode

The hands-free profile is configured when the uplink audio path is set to "Hands-free microphone" and the downlink audio path is set to "Loudspeaker" (refer to u-blox AT commands manual [3]: AT+USPM command: <main_uplink>, <main_downlink> parameters):

- Hands-free microphone signal must be connected to the module differential input **MIC_P / MIC_N**
- High power loudspeaker must be connected to the output of an external audio amplifier, for which the input must be connected to the module differential output **SPK_P / SPK_N**

The module differential analog audio output is not able to drive an 8 Ω speaker: an external audio amplifier must be provided on the application board to amplify the low power audio signal provided by the module differential output **SPK_P / SPK_N**.

Hands-free functionality is implemented using appropriate digital signal processing algorithms for voice-band handling (echo canceller and automatic gain control), managed via software (refer to u-blox AT commands manual [3], AT+UHFP command).

Figure 43 shows an example of an application circuit connecting a 2.2 kΩ electret microphone and an 8 Ω speaker to the LISA-U120 and LISA-U130 modules, with an external low noise LDO voltage regulator to provide a proper supply for the microphone and with an external audio amplifier to amplify the low power audio signal provided by the module differential output.

☞ Mount an 82 nH series inductor (e.g. Murata LQG15HS82NJ02) on each microphone line and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) on all audio lines to minimize RF coupling and TDMA noise.

☞ The physical width of the audio outputs lines on the application board must be wide enough to minimize series resistance.

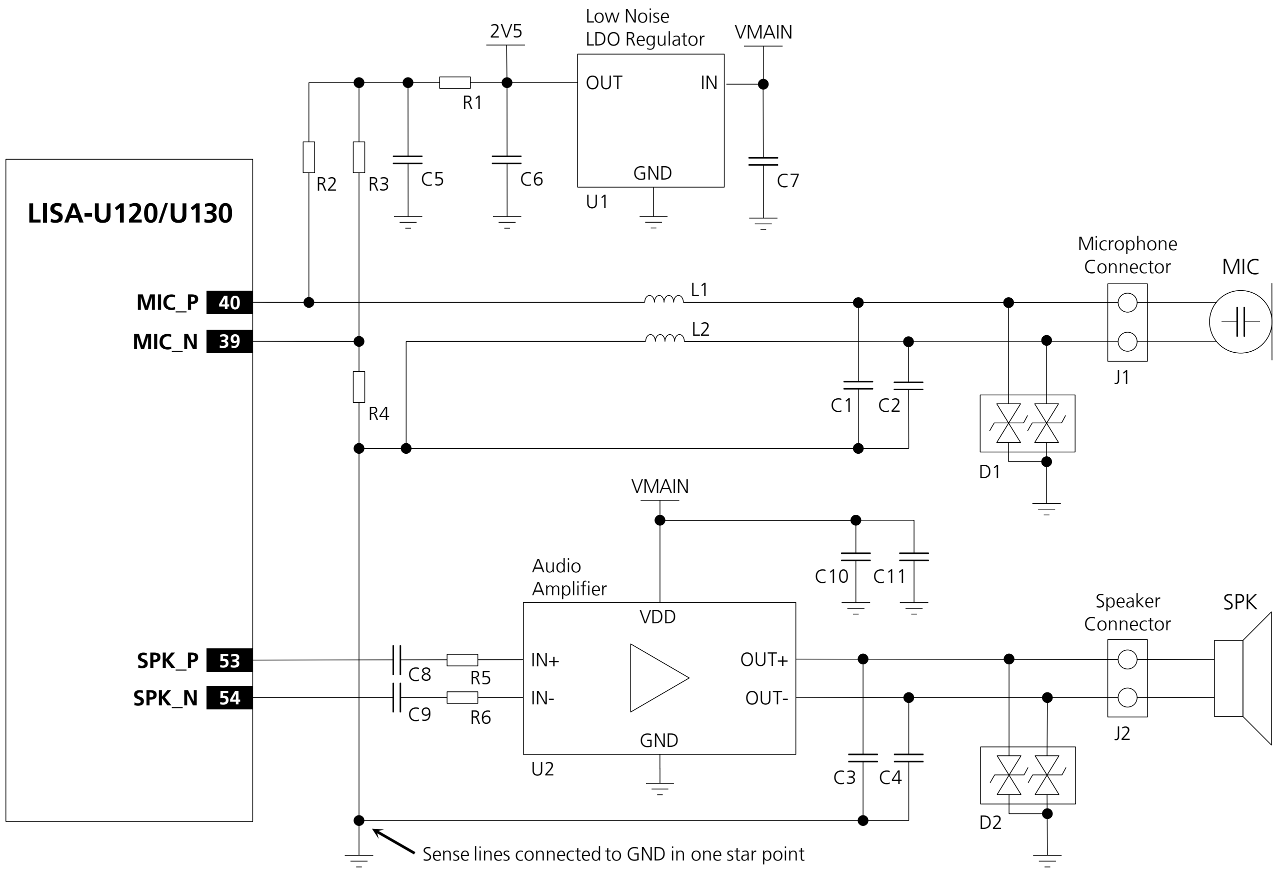

Figure 44: Hands-free mode application circuit

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 – Murata
C5, C6, C7, C10	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C8, C9	47 nF Capacitor Ceramic X7R 0402 10% 16V	GRM155R71C473KA01 – Murata
C11	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
J1	Microphone Connector	
J2	Speaker Connector	
L1, L2	82nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
MIC	2.2 kΩ Electret Microphone	

Reference	Description	Part Number – Manufacturer
R1, R2, R3, R4	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
R5, R6	0 Ω Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
SPK	8 Ω Loudspeaker	
U1	Low Noise LDO Linear Regulator 2.5 V 300 mA	LT1962EMS8-2.5#PBF- Linear Technology
U2	Filter-less Mono 2.8 W Class-D Audio Amplifier	SSM2305CPZ – Analog Devices

Table 37: Example of components for hands-free connection

1.11.1.6 Connection to an external analog audio device

The differential analog audio input / output can be used to connect the module to an external analog audio device. Audio devices with a differential analog input / output are preferable, as they are more immune to external disturbances.

If the external analog audio device is provided with a differential analog audio input, the **SPK_P** / **SPK_N** balanced output of the module must be connected to the differential input of the external audio device through a DC-block 10 µF series capacitor (e.g. Murata GRM188R60J106M) to decouple the bias present at the module output (see **SPK_P** / **SPK_N** common mode output voltage in the LISA-U1 series Data Sheet [1]). Use a suitable power-on sequence to avoid audio bump due to charging of the capacitor: the final audio stage should be always enabled as last one.

If the external analog audio device is provided with a single ended analog audio input, a proper differential to single ended circuit must be inserted from the **SPK_P** / **SPK_N** balanced output of the module to the single ended input of the external audio device. A simple application circuit is described in Figure 45: 10 µF series capacitors (e.g. Murata GRM188R60J106M) are provided to decouple the bias present at the module output, and a voltage divider is provided to properly adapt the signal level from the module output to the external audio device input.

The DC-block series capacitor acts as high-pass filter for audio signals, with cut-off frequency depending on both the values of capacitor and on the input impedance of the external audio device. For example: in case of differential input impedance of 600 Ω , the two 10 µF capacitors will set the -3 dB cut-off frequency to 53 Hz, while for single ended connection to 600 Ω external device, the cut-off frequency with just the single 10 µF capacitor will be 103 Hz. In both cases the high-pass filter has a low enough cut-off to not impact the audio signal frequency response.

The signal levels can be adapted by setting gain using AT commands, but additional circuitry must be inserted if the **SPK_P** / **SPK_N** output level of the module is too high for the input of the audio device.

If the external analog audio device is provided with a differential analog audio output, the **MIC_P** / **MIC_N** balanced input of the module must be connected directly to the differential output of the external audio device. Series capacitors are not needed since **MIC_P** / **MIC_N** pins are provided with internal 100 nF capacitors for DC blocking (see LISA-U1 series Data Sheet [1]).

If the external analog audio device is provided with a single ended analog audio output, a proper single ended to differential circuit has to be inserted from the single ended output of the external audio device to the **MIC_P** / **MIC_N** balanced input of the module. A simple application circuit is described in Figure 45: a voltage divider is provided to properly adapt the signal level from the external audio device output to the module input.

The signal levels can be adapted by setting gain using AT commands, but additional circuitry must be inserted if the output level of the audio device is too high for **MIC_P** / **MIC_N**. Please refer to Figure 45 for the application circuits.

☞ To enable the audio path corresponding to the differential analog audio input / output, please refer to u-blox AT Commands Manual [3]: AT+USPM command.

☞ To tune audio levels for the external device please refer to u-blox AT Commands Manual [3] (AT+USGC, AT+UMGC commands).

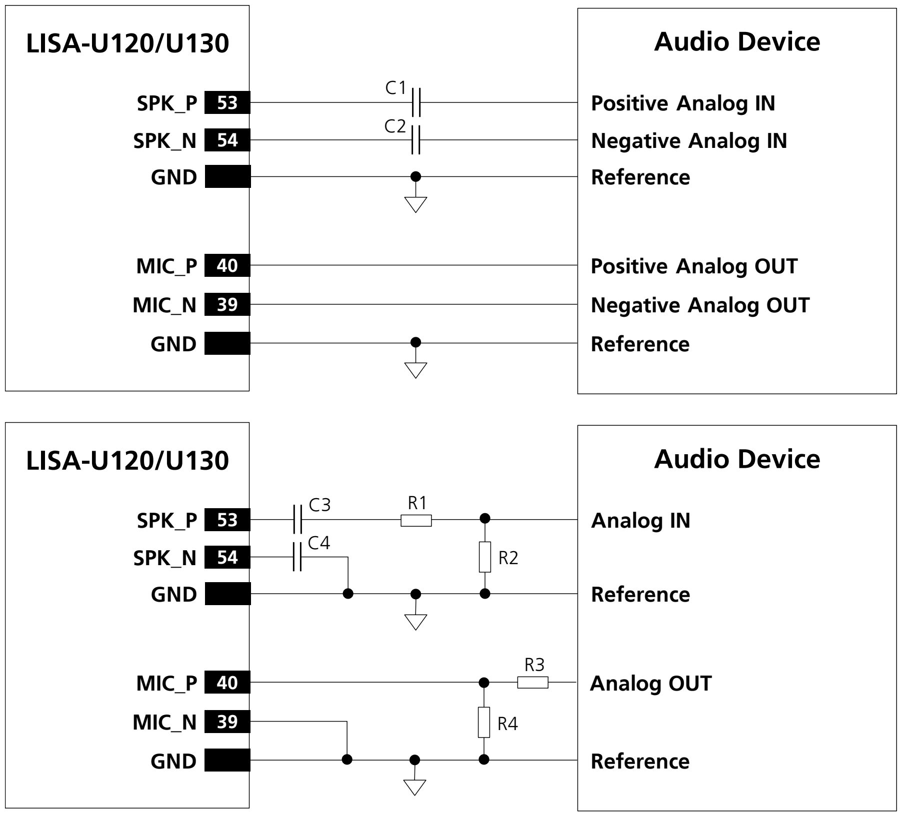

Figure 45: Application circuits to connect the module to audio devices with proper differential or single-ended input/output

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	10 µF Capacitor X5R 0603 5% 6.3 V	GRM188R60J106M – Murata
R1, R3	0 Ω Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
R2, R4	Not populated	

Table 38: Connection to an analog audio device

1.11.2 Digital Audio interface

☞ LISA-U100, LISA-U110 and LISA-U200-00 modules versions don't support digital audio interface.

LISA-U120 and LISA-U130 modules provide one bidirectional 4-wire I^2S digital audio interface, while all LISA-U2 series modules versions except LISA-U200-00 provide two bidirectional 4-wire I^2S digital audio interfaces for connecting to remote digital audio devices.

LISA-U series modules can act as an I^2S master or I^2S slave. In master mode the word alignment and clock signals of the I^2S digital audio interface are generated by the module. In slave mode these signal must be generated by the remote device.

Table 39 lists the signals related to digital audio functions.

Name	Module	Description	Remarks
I2S_TXD	LISA-U120-0x LISA-U130-0x LISA-U2xx-01	I²S transmit data	Module output
I2S_RXD	LISA-U120-0x LISA-U130-0x LISA-U2xx-01	I²S receive data	Module input
I2S_CLK	LISA-U120-00 LISA-U130-00	I²S clock	Module output in master mode
	LISA-U120-01 LISA-U130-01 LISA-U2xx-01	I²S clock	Module output in master mode Module input in slave mode
I2S_WA	LISA-U120-00 LISA-U130-00	I²S word alignment	Module output in master mode
	LISA-U120-01 LISA-U130-01 LISA-U2xx-01	I²S word alignment	Module output in master mode Module input in slave mode
I2S1_TXD	LISA-U2xx-01	Second I²S transmit data	Module output
I2S1_RXD	LISA-U2xx-01	Second I²S receive data	Module input
I2S1_CLK	LISA-U2xx-01	Second I²S clock	Module output in master mode Module input in slave mode
I2S1_WA	LISA-U2xx-01	Second I²S word alignment	Module output in master mode Module input in slave mode
CODEC_CLK	LISA-U2xx-01	Digital clock output	Digital clock output for external audio codec Configurable to 26 MHz or 13 MHz

Table 39: Digital audio interface pins

☞ The I²S interfaces and **CODEC_CLK** pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to the I²S interfaces pins, close to accessible points, and a low capacitance (i.e. less than 10 pF) ESD protection (e.g. AVX USB0002) on the line connected to **CODEC_CLK** pin, close to accessible point.

The I²S interface can be set to two modes, by the <I2S_mode> parameter of the AT+UI2S command:

- PCM mode
- Normal I²S mode

The I²S interface can be set to two configurations, by the <I2S_Master_Slave> parameter of AT+UI2S:

- Master mode
- Slave mode

☞ LISA-U120-00 and LISA-U130-00 modules versions don't support I²S slave mode: module acts as master only.

The sample rate of transmitted/received words can be set, by the <I2S_sample_rate> parameter of AT+UI2S, to:

- 8 kHz
- 11.025 kHz
- 12 kHz
- 16 kHz
- 22.05 kHz
- 24 kHz

- 32 kHz
- 44.1 kHz
- 48 kHz

☞ The sample rate of transmitted and received words of LISA-U120-00 and LISA-U130-00 modules cannot be configured: the sample rate is fixed at 8 kHz only.

The <main_uplink> and <main_downlink> parameters of the AT+USPM command must be properly configured to select the I^{2}S digital audio interfaces paths (for more details please refer to u-blox AT Commands Manual [3]):

- <main_uplink> has to be properly set to select:
  - the first I^{2}S interface (using **I2S_RXD** module input)
  - the second I^{2}S interface (using **I2S1_RXD** module input)
- <main_downlink> has to be properly set to select:
  - the first I^{2}S interface (using **I2S_TXD** module output)
  - the second I^{2}S interface (using **I2S1_TXD** module output)

Parameters of digital path can be configured and saved as the normal analog paths, using appropriate path parameter as described in the u-blox AT Commands Manual [3], +USGC, +UMGC, +USTN AT command. Analog gain parameters of microphone and speakers are not used when digital path is selected.

The I^{2}S receive data input and the I^{2}S transmit data output signals are respectively connected in parallel to the analog microphone input and speaker output signals, so resources available for analog path can be shared:

- Digital filters and digital gains are available in both uplink and downlink direction. They can be properly configured by the AT commands
- Ringer tone and service tone are mixed on the TX path when active (downlink)
- The HF algorithm acts on I^{2}S path

☞ Refer to the u-blox AT Commands Manual [3]: AT+UI2S command for possible settings of I^{2}S interface.

1.11.2.1 I^{2}S interface - PCM mode

Main features of the I^{2}S interface in PCM mode:

- I^{2}S runs in PCM - short alignment mode (configurable by AT commands)
- I^{2}S word alignment signal can be configured to 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz
- I^{2}S word alignment toggles high for 1 or 2 CLK cycles of synchronization (configurable), then toggles low for 16 CLK cycles of sample width. Frame length can be 1 + 16 = 17 bits or 2 + 16 = 18 bits
- I^{2}S clock frequency depends on frame length and <sample_rate>. Can be 17 x <sample_rate> or 18 x <sample_rate>
- I^{2}S transmit and I^{2}S receive data are 16 bit words long with the same sampling rate as I^{2}S word alignment, mono. Data is in 2's complement notation. MSB is transmitted first
- When I^{2}S word alignment toggles high, the first synchronization bit is always low. Second synchronization bit (present only in case of 2 bit long I^{2}S word alignment configuration) is MSB of the transmitted word (MSB is transmitted twice in this case)
- I^{2}S transmit data changes on I^{2}S clock rising edge, I^{2}S receive data changes on I^{2}S clock falling edge

1.11.2.2 I^{2}S interface - Normal I^{2}S mode

Normal I^{2}S supports:

- 16 bits word
- Mono interface
- Configurable sample rate: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz

Main features of I^{2}S interface in normal I^{2}S mode:

- I^{2}S word alignment signal always runs at <sample_rate> and synchronizes 2 channels (timeslots on word alignment high, word alignment low)
- I^{2}S transmit data is composed of 16 bit words, dual mono (the words are written on both channels). Data are in 2's complement notation. MSB is transmitted first. The bits are written on I^{2}S clock rising or falling edge (configurable)
- I^{2}S receive data is read as 16 bit words, mono (words are read only on the timeslot with WA high). Data is read in 2's complement notation. MSB is read first. The bits are read on the I^{2}S clock edge opposite to I^{2}S transmit data writing edge (configurable)
- I^{2}S clock frequency is 16 bits x 2 channels x <sample_rate>

The modes are configurable through a specific AT command (refer to the related chapter in u-blox AT Commands Manual [3], +UI2S AT command) and the following parameters can be set:

- MSB can be 1 bit delayed or non-delayed on I^{2}S word alignment edge
- I^{2}S transmit data can change on rising or falling edge of I^{2}S clock signal (rising edge in this example)
- I^{2}S receive data are read on the opposite front of I^{2}S clock signal

1.11.2.3 I^{2}S interface application circuits

LISA-U series I^{2}S digital audio interfaces can be connected to an external digital audio device for voice applications. The external digital audio device must be properly configured according to the wireless module configuration, with opposite role (i.e. master vs. slave), same mode (i.e. PCM mode or Normal I^{2}S mode), same sample rate and same voltage level.

Figure 46 shows an application circuit with a generic digital audio device.

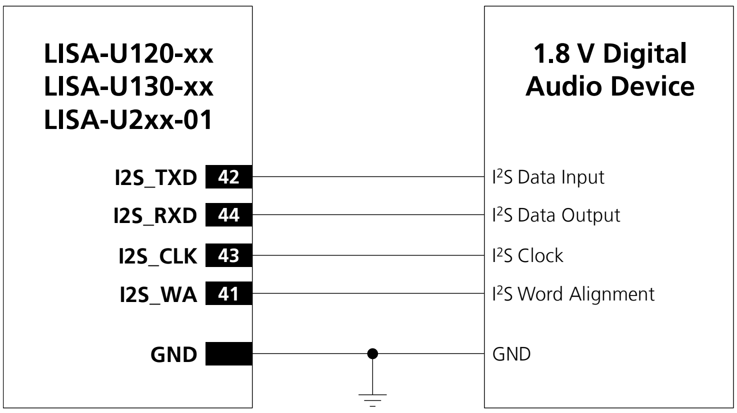

Figure 46: I^{2}S interface application circuit with a generic digital audio device

Figure 47 shows an application circuit for I^{2}S digital audio interfaces of LISA-U2xx-01 modules, providing voice capability using an external audio voice codec. DAC and ADC integrated in the external audio codec respectively converts an incoming digital data stream to analog audio output through a mono amplifier and converts the microphone input signal to the digital bit stream over the digital audio interface.

An I²S digital audio interface of the LISA-U2xx-01 modules (that acts as an I²S master) is connected to the digital audio interface of the external audio codec (that acts as an I²S slave). The first I²S interface can be used as well as the second I²S interface of the wireless module.

The **CODEC_CLK** digital output clock of the wireless module is connected to the clock input of the external audio codec to provide clock reference.

Signal integrity of the high speed lines may be degraded if the PCB layout is not optimal, especially when the **CODEC_CLK** clock line or also the I²S digital audio interface lines are very long: keep routing short and minimize parasitic capacitance to preserve signal integrity.

The external audio codec is controlled by the wireless module using the DDC (I²C) interface: this interface can be used to communicate with u-blox GPS receivers and at the same time to control an external audio codec on all LISA-U2 series modules versions except LISA-U200-00.

The **V_INT** supply output of the wireless module provides the supply to the external audio codec, defining a proper voltage level for the digital interfaces.

An external audio codec can be connected to the I²S digital audio interface of LISA-U120 or LISA-U130 modules as shown in the application circuit described in Figure 47. In this case the application processor should properly control the audio codec by I²C interface and should properly provide clock reference to the audio codec.

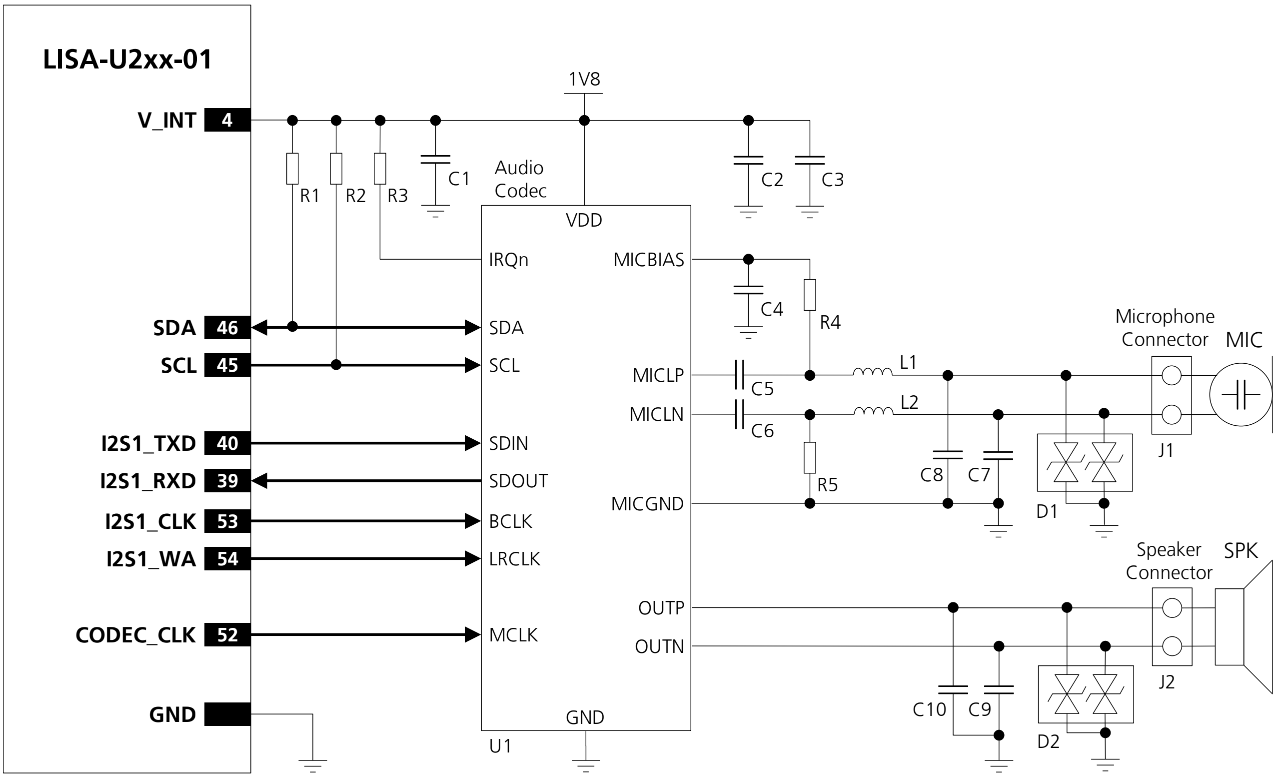

Figure 47: I²S interface application circuit with an external audio codec to provide voice capability

Reference	Description	Part Number – Manufacturer
C1	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
C2, C4, C5, C6	1 µF Capacitor Ceramic X5R 0402 10% 6.3 V	GRM155R60J105KE19 – Murata
C3	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C7, C8, C9, C10	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
J1	Microphone Connector	Various manufacturers
J2	Speaker Connector	Various manufacturers

Reference	Description	Part Number – Manufacturer
L1, L2	82nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
MIC	2.2 kΩ Electret Microphone	Various manufacturers
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R4, R5	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
SPK	32 Ω Speaker	Various manufacturers
U1	16-Bit Mono Audio Voice Codec	MAX9860ETG+ - Maxim

Table 40: Example of components for audio voice codec application circuit

☞ If the I^2S digital audio pins are not used, they can be left unconnected on the application board.

☞ Any external signal connected to the digital audio interfaces must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during power down mode, when external reset is forced low and during power-on sequence.

1.11.3 Voiceband processing system

The voiceband processing on the LISA-U series modules is implemented in the DSP core inside the baseband chipset. The analog audio front-end of the chipset is connected to the digital system through 16 bit ADC converters in the uplink path, and through 16 bit DAC converters in the downlink path. External digital audio devices can be interfaced directly to the DSP digital processing part via the I^2S digital interface. The analog amplifiers are skipped in this case.

Available audio signal processing algorithms are:

- Speech encoding (uplink) and decoding (downlink).The following speech codecs are supported in firmware on the DSP for speech encoding and decoding:

  GERAN GMSK codecs
  - GSM HR (GSM Half Rate)
  - GSM FR (GSM Full Rate)
  - GSM EFR (GSM Enhanced Full Rate)
  - HR AMR (GSM Half Rate Adaptive Multi Rate - Narrow Band)
  - FR AMR (GSM Full Rate Adaptive Multi Rate - Narrow Band)
  - FR AMR-WB (GSM Full Rate Adaptive Multi Rate - Wide Band)

  UTRAN codecs:
  - UMTS AMR2 (UMTS Adaptive Multi Rate version 2 – Narrow Band)
  - UMTS AMR-WB (UMTS Adaptive Multi Rate – Wide Band)
- Mandatory sub-functions:
  - Discontinuous transmission, DTX (GSM 46.031, 46.041, 46.081 and 46.093 standards)
  - Voice activity detection, VAD (GSM 46.032, 46.042, 46.082 and 46.094 standards)
  - Background noise calculation (GSM 46.012, 46.022, 46.062 and 46.092 standards)
- Function configurable via specific AT commands (refer to the u-blox AT Commands Manual [3])
  - Signal routing: +USPM command

- Analog amplification, Digital amplification: +USGC, +CLVL, +CRSL, +CMUT command
- Digital filtering: +UUBF, +UDBF commands
- Hands-free algorithms (echo cancellation, Noise suppression, Automatic Gain control) +UHFP command
- Sidetone generation (feedback of uplink speech signal to downlink path): +USTN command
- Playing/mixing of alert tones:
  Service tones: Tone generator with 3 sinus tones +UPAR command

  User generated tones: Tone generator with a single sinus tone +UTGN command

  PCM audio files (for prompting): The storage format of PCM audio files is 8 kHz sample rate, signed 16 bits, little endian, mono

With exception of the speech encoder/decoder, this audio processing can be controlled by AT commands.

This processing is implemented within the different blocks of the voiceband processing system:

- Sample-based Voice-band Processing (single sample processed at 16 kHz for Wide Band AMR codec or 8 kHz for all other speech codecs)
- Frame-based Voice-band Processing (frames of 320 samples for Wide Band AMR codec or 160 samples for all other speech codecs are processed every 20 ms)

These blocks are connected by buffers (circular buffer and voiceband sample buffer) and sample rate converters (for 8 / 16 to 47.6 kHz conversion).

Voiceband audio processing implemented in the DSP core of LISA-U series modules is summarized in Figure 48.

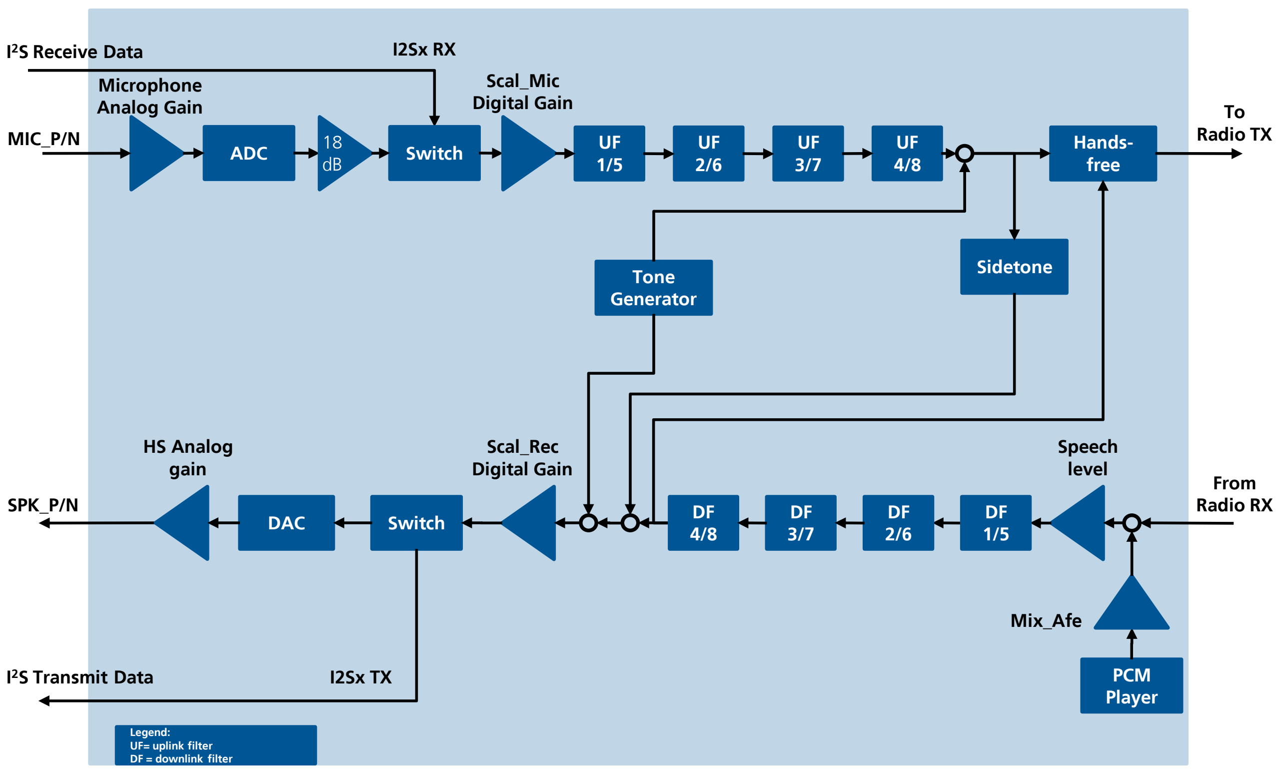

Figure 48: Voiceband processing system block diagram

1.12 General Purpose Input/Output (GPIO)

LISA-U1 series modules provide 5 pins (**GPIO1**-**GPIO5**), while LISA-U2 series modules provide up to 14 pins (**GPIO1-14**) which can be configured as general purpose input or output, or can be configured to provide special functions via u-blox AT commands (for further details refer to u-blox AT Commands Manual [3], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF, +USPM).

The following functions are available in the LISA-U series modules:

- **GSM Tx burst indication**:

  GPIO1 pin can be configured by AT+UGPIOC to indicate when a GSM Tx burst/slot occurs, setting the parameter <gpio_mode> of AT+UGPIOC command to 9.

  No GPIO pin is by default configured to provide the "GSM Tx burst indication" function.

  The pin configured to provide the "GSM Tx burst indication" function is set as
  - Output / High, since ~10 µs before the start of first Tx slot, until ~5 µs after the end of last Tx slot
  - Output / Low, otherwise

  The pin configured to provide the "GSM Tx burst indication" function can be connected on the application board to an input pin of an application processor to indicate when a GSM Tx burst/slot occurs.

- **GPS supply enable**:

  The **GPIO2** is by default configured by AT+UGPIOC command to enable or disable the supply of the u-blox GPS receiver connected to the wireless module.

  The **GPIO1**, **GPIO3**, **GPIO4** or **GPIO5** pins can be configured to provide the "GPS supply enable" function, alternatively to the default **GPIO2** pin, setting the parameter <gpio_mode> of AT+UGPIOC command to 3. The "GPS supply enable" mode can be provided only on one pin per time: it is not possible to simultaneously set the same mode on another pin.

  The pin configured to provide the "GPS supply enable" function is set as
  - Output / High, to switch on the u-blox GPS receiver, if the parameter <mode> of AT+UGPS command is set to 1
  - Output / Low, to switch off the u-blox GPS receiver, if the parameter <mode> of AT+UGPS command is set to 0 (default setting)

  The pin configured to provide the "GPS supply enable" function must be connected to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GPS receiver on the application board.

☞ LISA-U200-00 modules version don't support "GPS supply enable" function.

- **GPS data ready**:

  Only the **GPIO3** pin provides the "GPS data ready" function, to sense when a u-blox GPS receiver connected to the wireless module is ready to send data via the DDC (I^2C) interface, setting the parameter <gpio_mode> of AT+UGPIOC command to 4.

  The pin configured to provide the "GPS data ready" function will be set as
  - Input, to sense the line status, waking up the wireless module from idle-mode when the u-blox GPS receiver is ready to send data via the DDC (I^2C) interface; this is possible if the parameter <mode> of AT+UGPS command is set to 1 and the parameter <GPS_IO_configuration> of AT+UGPRF command is set to 16
  - Tri-state with an internal active pull-down enabled, otherwise (default setting)

  The pin that provides the "GPS data ready" function must be connected to the data ready output of the u-blox GPS receiver (i.e. the pin TxD1 of the u-blox GPS receiver) on the application board.

☞ LISA-U1xx-00 and LISA-U200-00 modules versions don’t support “GPS data ready” function.

- **GPS RTC sharing**:

  Only the **GPIO4** pin provides the “GPS RTC sharing” function, to provide an RTC (Real Time Clock) synchronization signal to the u-blox GPS receiver connected to the wireless module, setting the parameter <gpio_mode> of AT+UGPIOC command to 5.

  The pin configured to provide the “GPS RTC sharing” function will be set as
  - Output, to provide an RTC (Real Time Clock) synchronization signal to the u-blox GPS receiver if the parameter <mode> of AT+UGPS command is set to 1 and the parameter <GPS_IO_configuration> of AT+UGPRF command is set to 32
  - Output / Low, otherwise (default setting)

  The pin that provides the “GPS RTC sharing” function must be connected to the RTC synchronization input of the u-blox GPS receiver (i.e. the pin EXTINT0 of the u-blox GPS receiver) on the application board.

☞ LISA-U1xx-00 and LISA-U200-00 modules versions don’t support “GPS RTC sharing” function.

- **SIM card detection**:

  The **GPIO5** pin is by default configured by AT+UGPIOC command to detect SIM card presence.

  Only the **GPIO5** pin can be configured to provide the “SIM card detection” function, setting the parameter <gpio_mode> of AT+UGPIOC command to 7 (default setting).

  The pin configured to provide the “SIM card detection” function is set as
  - Input with an internal active pull-down enabled, to sense SIM card presence

  The pin must be connected on the application board to SW2 pin of the SIM card holder, which must provide 2 pins for the mechanical card presence detection, with a 470 kΩ pull-down resistor. SW1 pin of the SIM card holder must be connected to **V_INT** pin of the module, by a 1 kΩ pull-up resistor. Refer to Figure 49 and section 1.8 for the detailed application circuit. The **GPIO5** signal will be pulled low by the pull-down when a SIM card is not inserted in the holder, and will be pulled high by the pull-up when a SIM card is present.

- **Network status indication**:

  GPIO1, **GPIO2**, **GPIO3**, **GPIO4** or **GPIO5** can be configured to indicate network status (i.e. no service, registered home 2G network, registered home 3G network, registered visitor 2G network, registered visitor 3G network, voice or data 2G/3G call enabled), setting the parameter <gpio_mode> of AT+UGPIOC command to 2.

  No GPIO pin is by default configured to provide the “Network status indication” function.

  The “Network status indication” mode can be provided only on one pin per time: it is not possible to simultaneously set the same mode on another pin.

  The pin configured to provide the “Network status indication” function is set as
  - Continuous Output / Low, if no service (no network coverage or not registered)
  - Cyclic Output / High for 100 ms, Output / Low for 2 s, if registered home 2G network
  - Cyclic Output / High for 50 ms, Output / Low for 50 ms, Output / High for 50 ms, Output / Low for 2 s, if registered home 3G network
  - Cyclic Output / High for 100 ms, Output / Low for 100 ms, Output / High for 100 ms, Output / Low for 2 s, if registered visitor 2G network (roaming)
  - Cyclic Output / High for 50 ms, Output / Low for 50 ms, Output / High for 50 ms, Output / Low for 100 ms, if registered visitor 3G network (roaming)
  - Continuous Output / High, if voice or data 2G/3G call enabled

The pin configured to provide the "Network status indication" function can be connected on the application board to an input pin of an application processor or can drive a LED by a transistor with integrated resistors to indicate network status.

- **Module status indication**:

  The **GPIO13** and **GPIO1** pins can be configured to indicate module status (power-off mode, i.e. module switched off, versus idle, active or connected mode, i.e. module switched on), properly setting the parameter <gpio_mode> of AT+UGPIOC command to 10.

  No GPIO pin is by default configured to provide the "Module status indication".

  The pin configured to provide the "Module status indication" function is set as
  - Output / High, when the module is switched on (any operating mode during module normal operation: idle, active or connected mode)
  - Output / Low, when the module is switched off (power off mode)

  The "Module status indication" mode can be provided only on one pin at a time: it is not possible to simultaneously set the same mode on another pin.

☞ LISA-U1 series modules and LISA-U200-00 modules versions don't support "Module status indication".

- **Module operating mode indication**:

  The **GPIO14** and **GPIO5** pins can be configured to indicate module operating mode (idle-mode versus active or connected mode), properly setting the parameter <gpio_mode> of AT+UGPIOC command to 11.

  No GPIO pin is by default configured to provide the "Module operating mode indication".

  The pin configured to provide the "Module operating mode indication" function is set as
  - Output / High, when the module is in active or connected mode
  - Output / Low, when the module is in idle-mode (that can be reached if power saving is enabled by +UPSV AT command: for further details refer to u-blox AT Commands Manual [3])

  The "Module operating mode indication" mode can be provided only on one pin at a time: it is not possible to simultaneously set the same mode on another pin.

☞ LISA-U1 series modules and LISA-U200-00 versions don't support "Module operating mode indication".

- **I²S digital audio interface**:

  The **GPIO6**, **GPIO7**, **GPIO8**, **GPIO9** pins are by default configured as the second I²S digital audio interface (**I2S1_RXD**, **I2S1_TXD**, **I2S1_CLK**, **I2S1_WA** respectively).

  Only these pins can be configured as the second I²S digital audio interface, correctly setting the parameter <gpio_mode> of AT+UGPIOC command to 12 (default setting).

☞ LISA-U1 series modules and LISA-U200-00 versions don't support the second I²S digital audio interface over GPIOs.

- **SPI serial interface**:

  GPIO10, **GPIO11**, **GPIO12**, **GPIO13** and **GPIO14** pins are by default configured as the SPI / IPC serial interface (**SPI_SCLK**, **SPI_MOSI**, **SPI_MISO**, **SPI_SRDY** and **SPI_MRDY** respectively).

  Only these pins can be configured as the SPI / IPC serial interface, correctly setting the parameter <gpio_mode> of AT+UGPIOC command to 13 (default setting).

☞ LISA-U1 series modules and LISA-U200-00 versions don't support SPI / IPC serial interface over GPIOs: the SPI / IPC pins provide the SPI / IPC function only and cannot be configured as GPIO.

- **General purpose input**:

  All the GPIOs can be configured as input to sense high or low digital level through AT+UGPIOR command, setting the parameter <gpio_mode> of AT+UGPIOC command to 1.

  The "General purpose input" mode can be provided on more than one pin at a time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

  No GPIO pin is by default configured as "General purpose input".

  The pin configured to provide the "General purpose input" function is set as
  - Input, to sense high or low digital level by AT+UGPIOR command.

  The pin can be connected on the application board to an output pin of an application processor to sense the digital signal level.

- **General purpose output**:

  All the GPIOs can be configured as output to set the high or the low digital level through AT+UGPIOW command, setting the parameter <gpio_mode> of +UGPIOC AT command to 0.

  The "General purpose output" mode can be provided on more than one pin per time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

  No GPIO pin is by default configured as "General purpose output".

  The pin configured to provide the "General purpose output" function is set as
  - Output / Low, if the parameter <gpio_out_val> of AT+UGPIOW command is set to 0
  - Output / High, if the parameter <gpio_out_val> of AT+UGPIOW command is set to 1

  The pin can be connected on the application board to an input pin of an application processor to provide a digital signal.

- **Pad disabled**:

  All the GPIOs can be configured in tri-state with an internal active pull-down enabled, as a not used pin, setting the parameter <gpio_mode> of +UGPIOC AT command to 255.

  The "Pad disabled" mode can be provided on more than one pin per time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

  The pin configured to provide the "Pad disabled" function is set as
  - Tri-state with an internal active pull-down enabled

The configurations of all the GPIO pins of LISA-U series modules are described in Table 41.

Pin	Module	Name	Description	Remarks
20	LISA-U1xx-xx	**GPIO1**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the AT+UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • GSM Tx Burst Indication
	LISA-U200-00	**GPIO1**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the AT+UGPIOC command as • Output • Input • Network Status Indication • GSM Tx Burst Indication

Pin	Module	Name	Description	Remarks
	LISA-U2xx-01	**GPIO1**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the AT+UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • GSM Tx Burst Indication • Module Status Indication
21	LISA-U1xx-xx LISA-U2xx-01	**GPIO2**	GPIO	By default, the pin is configured to provide GPS Supply Enable function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • Pad disabled
	LISA-U200-00	**GPIO2**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication
23	LISA-U1xx-00	**GPIO3**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable
	LISA-U200-00	**GPIO3**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication
	LISA-U1xx-01 LISA-U2xx-01	**GPIO3**	GPIO	By default, the pin is configured to provide GPS Data Ready function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • Pad disabled
24	LISA-U1xx-00	**GPIO4**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable
	LISA-U200-00	**GPIO4**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication
	LISA-U1xx-01 LISA-U2xx-01	**GPIO4**	GPIO	By default, the pin is configured to provide GPS RTC sharing function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • Pad disabled

Pin	Module	Name	Description	Remarks
51	LISA-U1xx-xx	**GPIO5**	GPIO	By default, the pin is configured to provide SIM card detection function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • Pad disabled
	LISA-U200-00	**GPIO5**	GPIO	By default, the pin is configured to provide SIM card detection function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • Pad disabled
	LISA-U2xx-01	**GPIO5**	GPIO	By default, the pin is configured to provide SIM card detection function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • Module Operating Mode Indication • Pad disabled
39	LISA-U200-00	**GPIO6**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input
	LISA-U2xx-01	**I2S1_RXD / GPIO6**	2^{nd} I^2S receive data / GPIO	By default, the pin is configured as 2^{nd} I^2S receive data input. Can be alternatively configured by the +UGPIOC, +USPM commands as • Output • Input • Pad disabled
40	LISA-U200-00	**GPIO7**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input
	LISA-U2xx-01	**I2S1_TXD / GPIO7**	2^{nd} I^2S transmit data / GPIO	By default, the pin is configured as 2^{nd} I^2S transmit data output. Can be alternatively configured by the +UGPIOC, +USPM commands as • Output • Input • Pad disabled
53	LISA-U200-00	**GPIO8**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input
	LISA-U2xx-01	**I2S1_CLK / GPIO8**	2^{nd} I^2S clock / GPIO	By default, the pin is configured as 2^{nd} I^2S clock input/output. Can be alternatively configured by the +UGPIOC, +USPM commands as • Output • Input • Pad disabled
54	LISA-U200-00	**GPIO9**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the +UGPIOC command as • Output • Input
	LISA-U2xx-01	**I2S1_WA / GPIO9**	2^{nd} I^2S word alignment / GPIO	By default, the pin is configured as 2^{nd} I^2S word alignment input/output. Can be alternatively configured by the +UGPIOC, +USPM commands as • Output • Input • Pad disabled

Pin	Module	Name	Description	Remarks
55	LISA-U2xx-01	**SPI_SCLK / GPIO10**	SPI Serial Clock / GPIO	By default, the pin is configured as SPI Serial Clock Input: • Idle low (CPOL=0) • Internal active pull-down to GND enabled Can be alternatively configured by the +UGPIOC command as • Output • Input • Pad disabled
56	LISA-U2xx-01	**SPI_MOSI / GPIO11**	SPI Data Line / GPIO	By default, the pin is configured as SPI Data Line Input: • Shift data on rising clock edge (CPHA=1) • Latch data on falling clock edge (CPHA=1) • Idle high • Internal active pull-up to V_INT enabled Can be alternatively configured by the +UGPIOC command as • Output • Input • Pad disabled
57	LISA-U2xx-01	**SPI_MISO / GPIO12**	SPI Data Line Output / GPIO	By default, the pin is configured as SPI Data Line Output: • Shift data on rising clock edge (CPHA=1) • Latch data on falling clock edge (CPHA=1) • Idle high Can be alternatively configured by the +UGPIOC command as • Output • Input • Pad disabled
58	LISA-U2xx-01	**SPI_SRDY / GPIO13**	SPI Slave Ready / GPIO	By default, the pin is configured as SPI Slave Ready Output: • Idle low Can be alternatively configured by the +UGPIOC command as • Output • Input • Module Status Indication Pad disabled
59	LISA-U2xx-01	**SPI_MRDY / GPIO14**	SPI Master Ready / GPIO	By default, the pin is configured as SPI Master Ready Input: • Idle low • Internal active pull-down to GND enabled Can be alternatively configured by the +UGPIOC command as • Output • Input • Module Operating Mode Indication • Pad disabled

Table 41: GPIO pins

☞ The GPIO pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins, close to accessible points.

An application circuit for a typical GPIOs usage is described in Figure 49:

- Network indication function provided by the **GPIO1** pin
- GPS supply enable function provided by the **GPIO2** pin (function not supported by LISA-U200-00)
- GPS data ready function provided by the **GPIO3** pin (function not supported by LISA-Uxxx-00)
- GPS RTC sharing function provided by the **GPIO4** pin (function not supported by LISA-Uxxx-00)
- SIM card detection function provided by the **GPIO5** pin

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

☞ Any external signal connected to GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the module cannot be tri-stated, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode, when external reset is forced low and during power-on sequence.

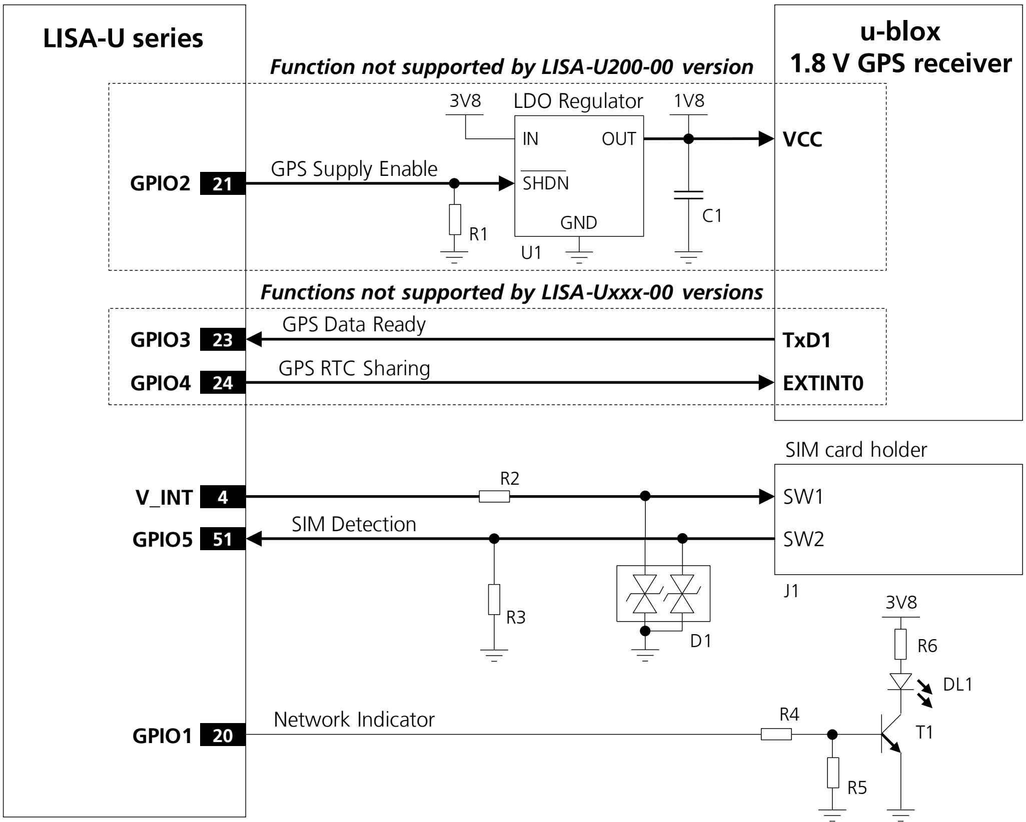

Figure 49: GPIO application circuit

Reference	Description	Part Number - Manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	Voltage Regulator for GPS Receiver	See GPS Module Hardware Integration Manual
R2	1 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	470 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
D1	ESD Transient Voltage Suppressor	USB0002RP or USB0002DP - AVX
J1	SIM Card Holder	CCM03-3013LFT R102 - C&K Components (or equivalent)
R4	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R5	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R6	820 Ω Resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED Red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 42: Components for GPIO application circuit

An application circuit for the module status indication function, provided by LISA-U2xx-01 **GPIO13** and **GPIO1** pins to indicate module status (power-off mode, i.e. module switched off, versus idle, active or connected mode, i.e. module switched on), is described in Figure 50.

The logic level of the pin configured to provide module status indication, that is set high when the module is switched on and low when the module is switched off, is inverted by a transistor biased by the **V_BCKP** supply, which is generated by the module when a valid **VCC** is applied.

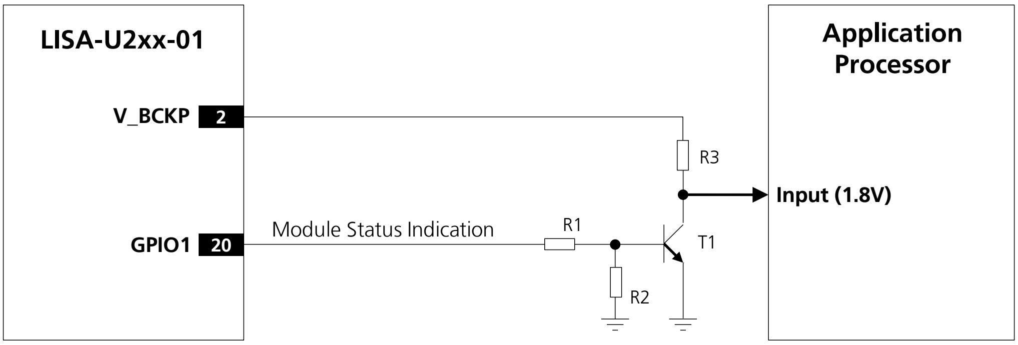

Figure 50: Module status indication application circuit

Reference	Description	Part Number - Manufacturer
R1, R3	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	100 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
T1	NPN BJT Transistor	BC847 - Infineon

Table 43: Components for module status indication application circuit

1.13 Reserved pins (RSVD)

LISA-U series modules have pins reserved for future use. All the **RSVD** pins, except pin number 5, can be left unconnected on the application board. The application circuit is illustrated in Figure 51.

☞ Pin 5 (**RSVD**) must be connected to GND.

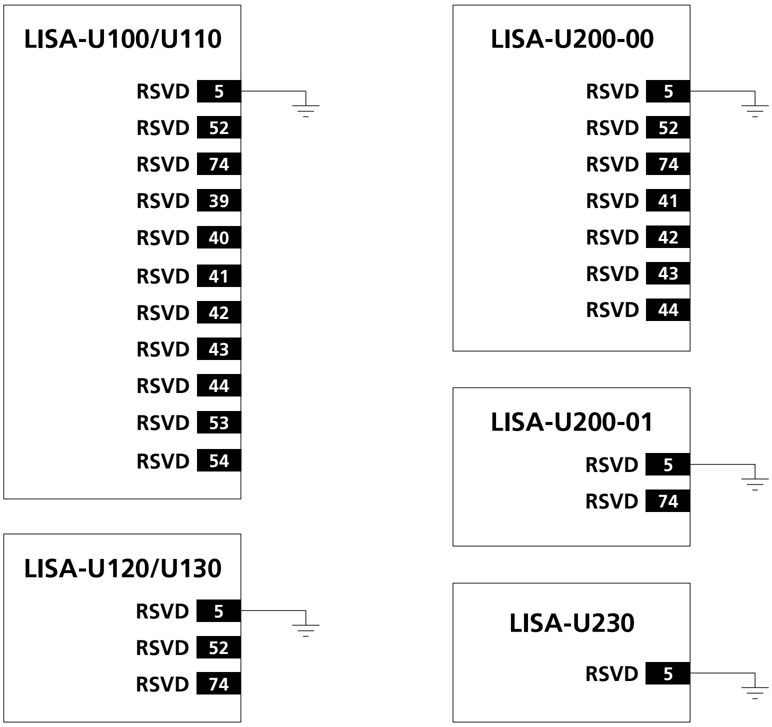

Figure 51: Application circuit for the reserved pins (RSVD)

1.14 Schematic for LISA-U series module integration

Figure 52 is an example of a schematic diagram where a LISA-U1 series module is integrated into an application board, using all the interfaces of the module.

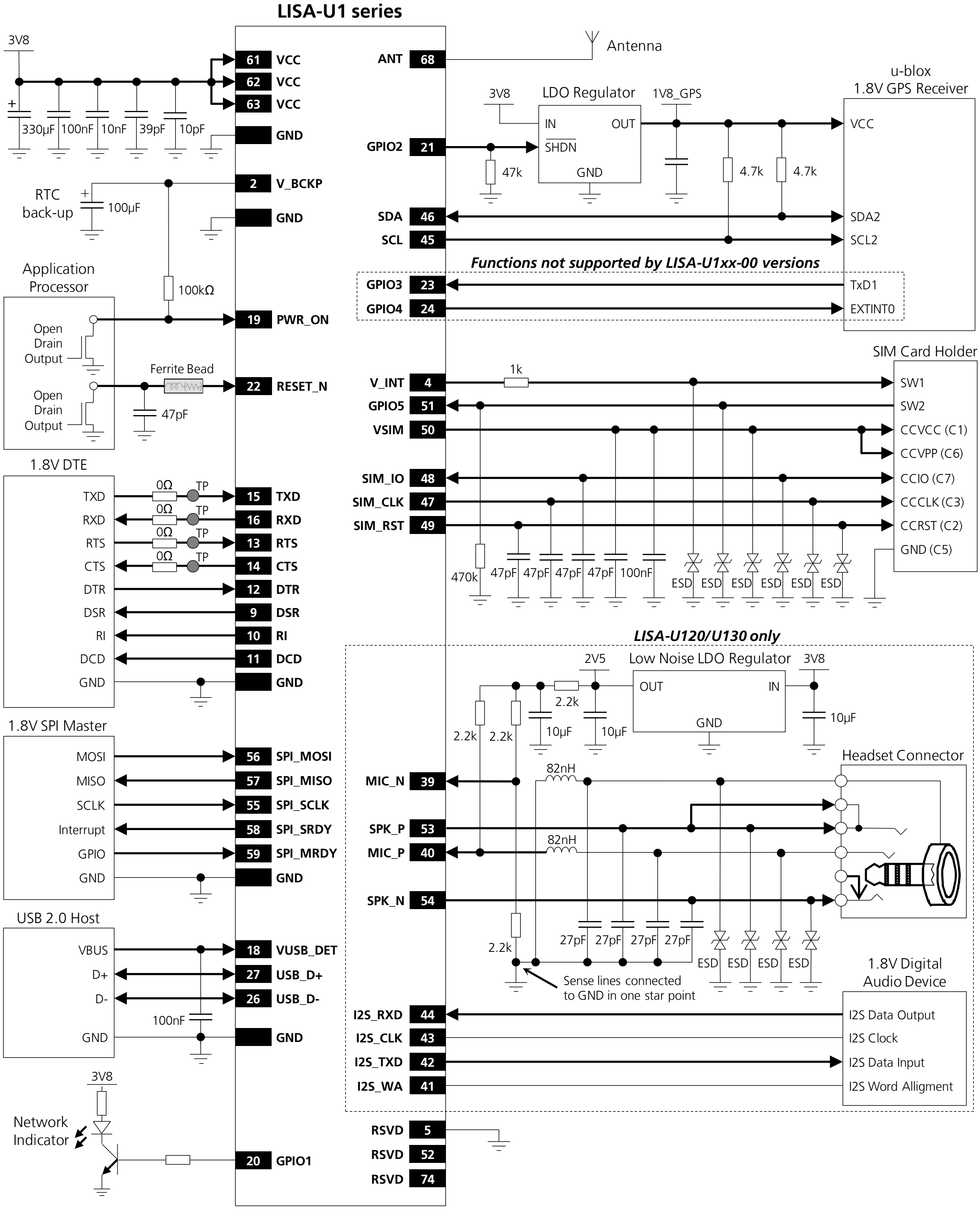

Figure 52: Example of schematic diagram to integrate LISA-U1 series modules in an application board, using all the interfaces

Figure 53 is an example of a schematic diagram where a LISA-U2 series module is integrated into an application board, using all the interfaces of the module.

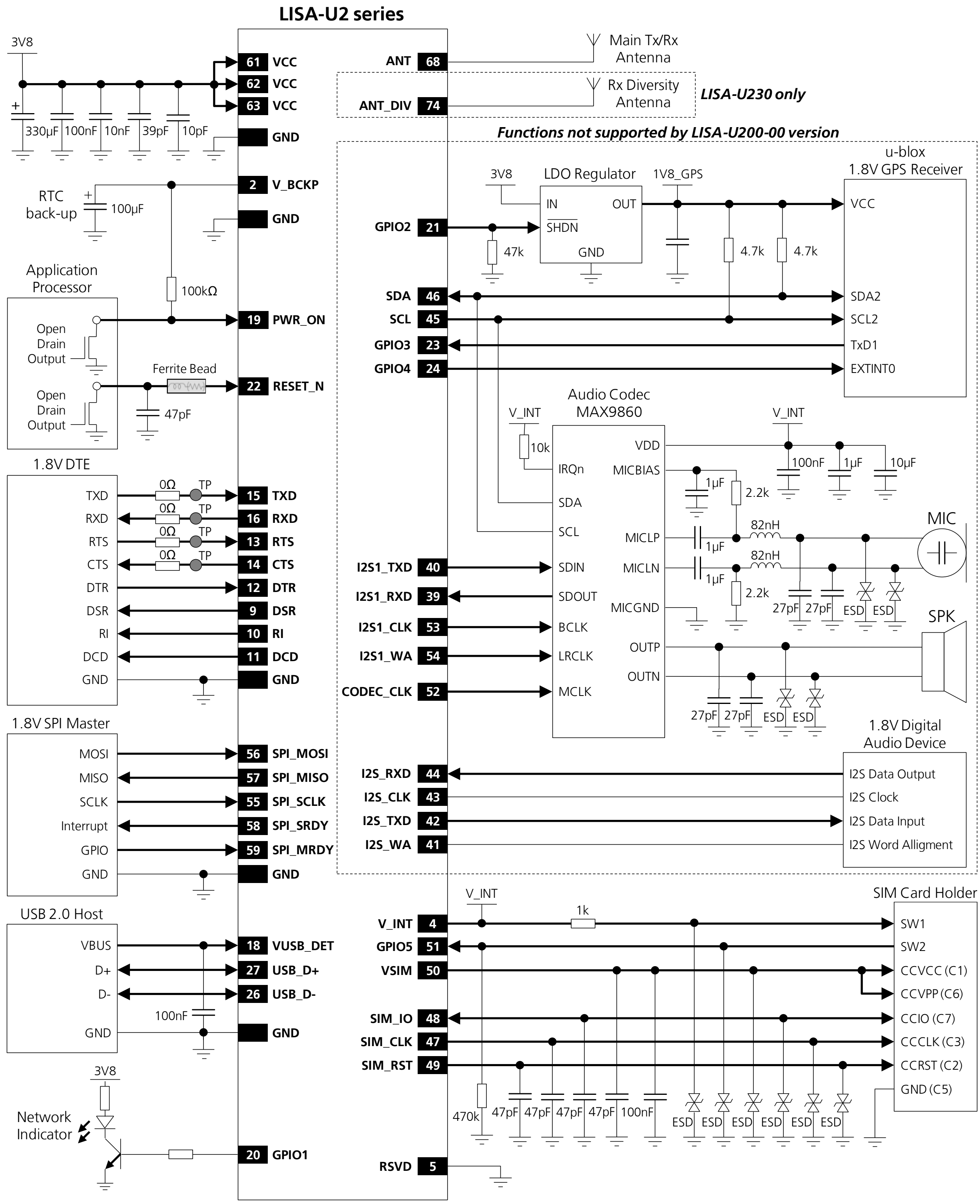

Figure 53: Example of schematic diagram to integrate LISA-U2 series modules in an application board, using all the interfaces

1.15 Approvals

LISA-U series modules have been or will be approved under the following schemes:

- [EU] R&TTE (Radio and Telecommunications Terminal Equipment Directive)
- [EU] CE (Conformité Européenne)
- [EU] GCF – CC (Global Certification Forum-Certification Criteria)
- [EU] GCF – FT (Global Certification Forum- Field Trials)
- [USA] FCC (Federal Communications Commission)
- [USA] PTCRB (PCS Type Certification Review Board)
- [Canada] IC (Industry Canada)
- [South Africa] ICASA (Independent Communications Authority of South Africa)
- [Australia] a-tick
- [Korea] KCC (Korean Communications Commission)
- [Japan] JATE (Japan Approvals Institute for Telecommunications Equipment)
- [Japan] TELEC (Telecom Engineering Center)
- [Taiwan] NCC (National Communications Commission)

LISA-U series modules will be approved by the following network operators:

- [USA] AT&T
- [Canada] Rogers
- [EU][AUS] Vodafone
- [AUS] Telstra
- [EU] Tmobile
- [Japan] NTTDoCoMo
- [EU] Orange

1.15.1 R&TTED and European Conformance CE mark

Products bearing the CE marking comply with the R&TTE Directive (99/5/EC), EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with these directives implies conformity to the following European Norms:

- Radio Frequency spectrum efficiency:
  - EN 301 511
  - EN 301 908-1
  - EN 301 908-2
- Electromagnetic Compatibility:
  - EN 301 489-1
  - EN 301 489-7
  - EN 301 489-24
- Safety
  - EN 60950-1: 2006
  - EN62311: 2008

Notified Body identification number for LISA-U100, LISA-U110, LISA-U120 and LISA-U130 is 0890.

Notified Body identification number for LISA-U200 is 0682.

1.15.2 IC

The IC Certification Numbers for the LISA-U series modules are:

- LISA-U100: 8595A-LISAU120
- LISA-U120: 8595A-LISAU120
- LISA-U200: 8595A-LISAU200

1.15.3 Federal communications commission notice

The FCC ID for the LISA-U series modules are

- LISA-U100: XPYLISAU120
- LISA-U120: XPYLISAU120
- LISA-U200: XPYLISAU200

1.15.3.1 Safety Warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed

1.15.3.2 Declaration of Conformity - United States only

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ **Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.**

⚠ **The gain of the system antenna(s) used for LISA-U200 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 3.45 dBi (850 MHz) and 2.74 dBi (1900 MHz) for mobile and fixed or mobile operating configurations.**

1.15.3.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ **Manufacturers of mobile or fixed devices incorporating the LISA-U series modules are authorized to use the FCC Grants and Industry Canada Certificates of the LISA-U series modules for their own final products according to the conditions referenced in the certificates.**

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

LISA-U100: "Contains FCC ID: XPYLISAU120" resp.
LISA-U120: "Contains FCC ID: XPYLISAU120" resp.
LISA-U200: "Contains FCC ID: XPYLISAU200" resp.

The IC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

LISA-U100: "Contains IC: 8595A-LISAU120" resp.
LISA-U120: "Contains IC: 8595A-LISAU120" resp.
LISA-U200: "Contains IC: 8595A-LISAU200" resp.

Canada, Industry Canada (IC) Notices

This Class B digital apparatus complies with Canadian ICES-003 and RSS-210.

Operation is subject to the following two conditions:

- **this device may not cause interference**
- **this device must accept any interference, including interference that may cause undesired operation of the device**

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Wireless Module is below the Industry Canada (IC) radio frequency exposure limits. The u-blox Wireless Module should be used in such a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address: http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng

Additional Canadian information on RF exposure also can be found at the following web address: http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: Manufacturers of portable applications incorporating the LISA-U series modules are required to have their final product certified and apply for their own FCC Grant and Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canada, avis d'Industrie Canada (IC)

Cet appareil numérique de classe B est conforme aux normes canadiennes ICES-003 et RSS-210.

Son fonctionnement est soumis aux deux conditions suivantes:

- **cet appareil ne doit pas causer d'interférence**
- **cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement**

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans fil u-blox Wireless Module est inférieure à la limite d'exposition aux fréquences radio d'Industrie Canada (IC). Utilisez l'appareil de sans fil u-blox Wireless Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur:

http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur : http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

⚠ **IMPORTANT: les fabricants d'applications portables contenant les modules LISA-U1 series doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat Industrie Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.**

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

1.15.4 a-tick AUS Certification

⚠ **The equipment may not function when mains power fail either on the packaging or with the equipment.**

☞ LISA-U2 series is not a-tick AUS certified.

2 Design-In

2.1 Design-in checklist

This section provides a design-in checklist.

2.1.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin above the minimum operating range limit.
- ☑ DC supply must be capable of providing 2.5 A current pulses, providing a voltage at **VCC** pin above the minimum operating range limit and with a maximum 400 mV voltage drop from the nominal value.
- ☑ **VCC** supply should be clean, with very low ripple/noise: suggested passive filtering parts can be inserted.
- ☑ **VCC** voltage must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module.
- ☑ Connect only one DC supply to **VCC**: different DC supply systems are mutually exclusive.
- ☑ Do not leave **PWR_ON** floating: add a pull-up resistor to **V_BCKP**.
- ☑ Don't apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested low capacitance ESD protection and passive filtering parts on each SIM signal.
- ☑ Check UART signals direction, since the signal names follow the ITU-T V.24 Recommendation [4].
- ☑ Provide appropriate access to USB interface and/or to UART **RxD**, **TxD** lines and access to **PWR_ON** and/or **RESET_N** lines on the application board in order to flash/upgrade the module firmware.
- ☑ Provide appropriate access to USB interface and/or to UART **RxD**, **TxD**, **CTS**, **RTS** lines for debugging.
- ☑ Capacitance and series resistance must be limited on each line of the SPI / IPC interface.
- ☑ Add a proper pull-up resistor to a proper supply on each DDC (I^2C) interface line, if the interface is used.
- ☑ Capacitance and series resistance must be limited on each line of the DDC interface.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Connect the pin number 5 (**RSVD**) to ground.
- ☑ Insert the suggested passive filtering parts on each used analog audio line.
- ☑ Check the digital audio interface specifications to connect a proper device.
- ☑ Capacitance and series resistance must be limited on **CODEC_CLK** line and each I^2S interface line.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ Any external signal connected to the UART interface, SPI/IPC interface, I^2S interfaces and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 s after the start-up event), to avoid latch-up of circuits and let a proper boot of the module.
- ☑ All unused pins can be left floating on the application board except the **PWR_ON** pin (must be connected to **V_BCKP** by a pull-up resistor) and the **RSVD** pin number 5 (must be connected to GND).

2.1.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** pad (main RF input/output) and to the **ANT_DIV** pad (RF input for Rx diversity).
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure no coupling occurs with other noisy or sensitive signals (primarily analog audio input/output signals, SIM signals).
- ☑ **VCC** line should be wide and short.
- ☑ Route **VCC** supply line away from sensitive analog signals.
- ☑ The high-power audio outputs lines on the application board must be wide enough to minimize series resistance.
- ☑ Ensure proper grounding.
- ☑ Consider "No-routing" areas for the Data Module footprint.
- ☑ Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.
- ☑ Design **USB_D+ / USB_D-** connection as 90 Ω differential pair.
- ☑ Keep routing short and minimize parasitic capacitance on the SPI lines to preserve signal integrity.
- ☑ Keep routing short and minimize parasitic capacitance on **CODEC_CLK** line to preserve signal integrity.

2.1.3 Antenna checklist

- ☑ Antenna should have 50 Ω impedance, V.S.W.R less than 3:1 (recommended 2:1)on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Follow the additional guidelines for products marked with the FCC logo (United States only) reported in chapter 2.2.1.1 and 1.15.3.2
- ☑ The antenna connected to the **ANT** pad should have built in DC resistor to ground to get proper antenna detection functionality.
- ☑ The antenna for the Rx diversity connected to the **ANT_DIV** pin should be carefully separated from the main Tx/Rx antenna connected to the **ANT** pin to ensure highly uncorrelated receive signals on each antenna. The distance between the two antennas should be greater than half a wavelength of the lowest used frequency (i.e. distance greater than ~20 cm, for 2G/3G low bands) to distinguish between different multipath channels, for proper spatial diversity implementation.

2.2 Design Guidelines for Layout

The following design guidelines must be met for optimal integration of LISA-U series modules on the final application board.

2.2.1 Layout guidelines per pin function

This section groups LISA-U series modules pins by signal function and provides a ranking of importance in layout design.

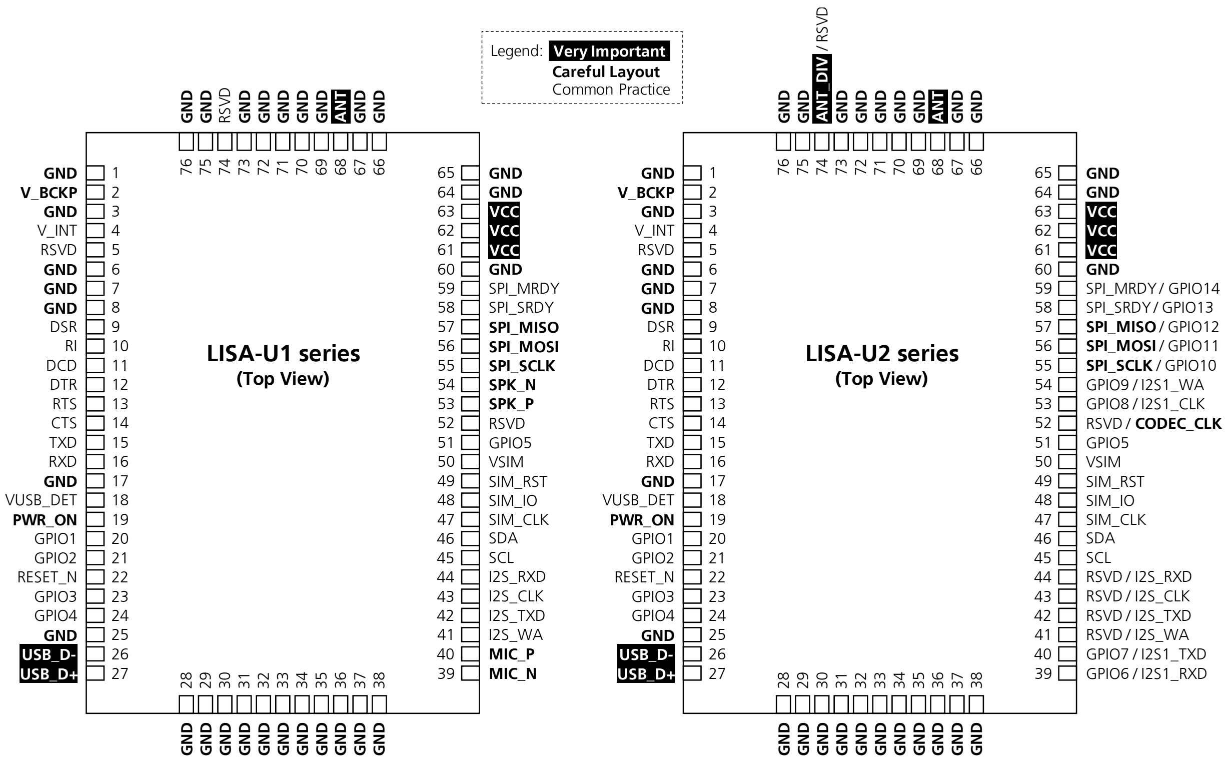

Figure 54: LISA-U1 and LISA-U2 series modules pin-out (top view) with ranked importance for layout design

Rank	Function	Pin(s)	Layout	Remarks
1st	**RF Antenna**			
	Main RF input/output	**ANT**	**Very Important**	Design for 50 Ω characteristic impedance. See section 2.2.1.1
	RF input for Rx diversity	**ANT_DIV**	**Very Important**	Design for 50 Ω characteristic impedance. See section 2.2.1.1
2nd	**Main DC Supply**	**VCC**	**Very Important**	**VCC** line should be wide and short. Route away from sensitive analog signals. See section 2.2.1.2
3rd	**USB Signals**	**USB_D+** **USB_D-**	**Very Important**	Route USB_D+ and USB_D- as differential lines: design for 90 Ω differential impedance. See section 2.2.1.3
4th	**Analog Audio**		**Careful Layout**	Avoid coupling with noisy signals. See section 2.2.1.4
	Audio Inputs	**MIC_P, MIC_N**		
	Audio Outputs	**SPK_P, SPK_N**		
5th	**Ground**	**GND**	**Careful Layout**	Provide proper grounding. See section 2.2.1.5
6th	**Sensitive Pin:**		**Careful Layout**	Avoid coupling with noisy signals. See section 2.2.1.6
	Backup Voltage	**V_BCKP**		
	Power-On	**PWR_ON**		
7th	**High-speed digital pins:**		**Careful Layout**	Avoid coupling with sensitive signals. See section 2.2.1.7
	SPI Signals	**SPI_SCLK, SPI_MISO, SPI_MOSI, SPI_SRDY, SPI_MRDY**		
	Clock Output	**CODEC_CLK**		
8th	**Digital pins and supplies:**		Common Practice	Follow common practice rules for digital pin routing. See section 2.2.1.8
	SIM Card Interface	VSIM, SIM_CLK, SIM_IO, SIM_RST		
	Digital Audio (If implemented)	I2S_CLK, I2S_RXD, I2S_TXD, I2S_WA I2S1_CLK, I2S1_RXD, I2S1_TXD, I2S1_WA		
	DDC	SCL, SDA		
	UART	TXD, RXD, CTS, RTS, DSR, RI, DCD, DTR		
	External Reset	RESET_N		
	General Purpose I/O	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5 GPIO6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO11, GPIO12, GPIO13, GPIO14		
	USB detection	VUSB_DET		
	Supply for Interfaces	V_INT		

Table 44: Pin list in order of decreasing importance for layout design

2.2.1.1 RF antenna connection

The **ANT** pin (main RF input/output) and the **ANT_DIV** pin (RF input for diversity receiver provided by LISA-U230 modules) are very critical in layout design. The PCB line must be designed to provide 50 Ω nominal characteristic impedance and minimum loss up to radiating element.

- Provide proper transition between the **ANT** pad and the **ANT_DIV** pad to application board PCB
- Increase GND keep-out (i.e. clearance) for **ANT** and **ANT_DIV** pads to at least 250 µm up to adjacent pads metal definition and up to 500 µm on the area below the module, as described in Figure 55

- Add GND keep-out (i.e. clearance) on buried metal layers below **ANT** and **ANT_DIV** pads and below any other pad of component present on the RF line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground (see Figure 55 for the description of the GND keep-out area below **ANT** and **ANT_DIV** pads)
- The transmission line up to antenna connector or pad may be a micro strip or a stripline. In any case must be designed to achieve 50 Ω characteristic impedance
- Microstrip lines are usually easier to implement and the reduced number of layer transitions up to antenna connector simplifies the design and diminishes reflection losses. However, the electromagnetic field extends to the free air interface above the stripline and may interact with other circuitry
- Buried striplines exhibit better shielding to external and internally generated interferences. They are therefore preferred for sensitive application. In case a stripline is implemented, carefully check that the via pad-stack does not couple with other signals on the crossed and adjacent layers
- Minimize the transmission line length; the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB
- The transmission line should not have abrupt change to thickness and spacing to GND, but must be uniform and routed as smoothly as possible
- The transmission line must be routed in a section of the PCB where minimal interference from noise sources can be expected
- Route RF transmission line far from other sensitive circuits as it is a source of electromagnetic interference
- Avoid coupling with **VCC** routing and analog audio lines
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer
- Add GND vias around transmission line
- Ensure no other signals are routed parallel to transmission line, or that other signals cross on adjacent metal layer
- If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for 50 Ω characteristic impedance calculation
- Don't route microstrip line below discrete component or other mechanics placed on top layer
- When terminating transmission line on antenna connector (or antenna pad) it is very important to strictly follow the connector manufacturer's recommended layout
- GND layer under RF connectors and close to buried vias should be cut out in order to remove stray capacitance and thus keep the RF line 50 Ω. In most cases the large active pad of the integrated antenna or antenna connector needs to have a GND keep-out (i.e. clearance) at least on first inner layer to reduce parasitic capacitance to ground. Note that the layout recommendation is not always available from connector manufacturer: e.g. the classical SMA Pin-Through-Hole needs to have GND cleared on all the layers around the central pin up to annular pads of the four GND posts. Check 50 Ω impedance of **ANT** and **ANT_DIV** lines
- Ensure no coupling occurs with other noisy or sensitive signals
- The antenna for the Rx diversity should be carefully separated from the main Tx/Rx antenna to ensure that uncorrelated signals are received at each antenna, because signal improvement is dependent on the cross correlation and relative signal strength levels between the two received signals. The distance between the two antennas should be greater than half a wavelength of the lowest used frequency (i.e. distance greater than ~20 cm, for 2G/3G low bands) to distinguish between different multipath channels, for proper spatial diversity implementation

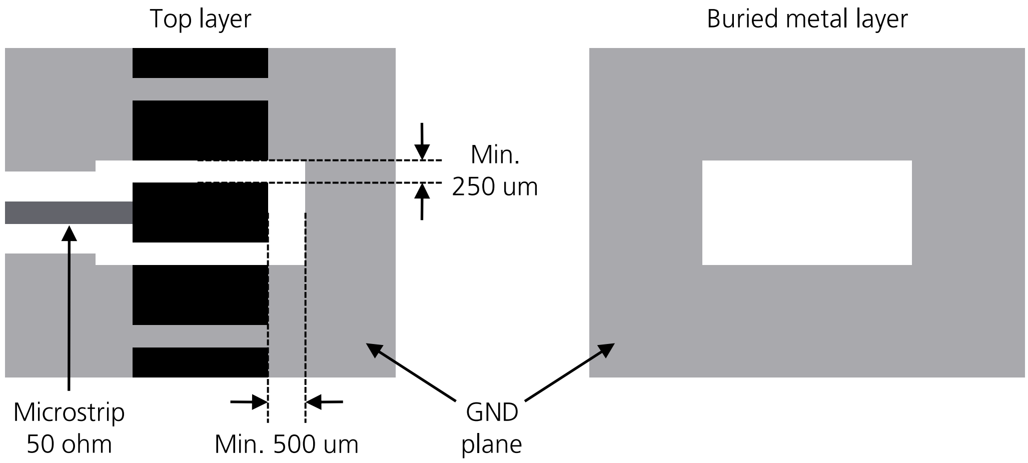

Figure 55: GND keep-out area on top layer around ANT and ANT_DIV pads and on buried layer below ANT and ANT_DIV pads

☞ Any RF transmission line on PCB should be designed for 50 Ω characteristic impedance.

☞ Ensure no coupling occurs with other noisy or sensitive signals.

Additional guidelines for products marked with the FCC logo - United States only

LISA-U series modules can only be used with a host antenna circuit trace layout according to these guidelines; a host system designer must follow the guidelines to keep the original Grant of LISA-U series modules.

☞ Strict compliance to the layout reference design already approved (described in the following guidelines) is required to ensure that only approved antenna shall be used in the host system.

☞ If in a host system there is any difference from the trace layout already approved, it requires a Class II permissive change or a new grant as appropriate as FCC defines.

Compliance of this device in all final host configurations is the responsibility of the Grantee.

The approved reference design for LISA-U series modules has a structure of 4 layers described in the following.

The Layer 1 (top layer, see Figure 56) provides a micro strip line to connect the **ANT** pin of the LISA-U series module to the antenna connector. The **ANT** pin of the LISA-U series module must be soldered on the designed pad which is connected to the antenna connector by a micro strip. The characteristics of the micro strip line (coplanar wave guide) are the following:

- Thickness = 0.035 mm
- Width = 0.26 mm
- Length = 7.85 mm
- Gap (signal to GND) = 0.5 mm

The micro strip line must be designed to achieve 50 Ω characteristic impedance: the dimensions of the micro strip line must be calculated in a host system according to PCB characteristics provided by PCB manufacturer.

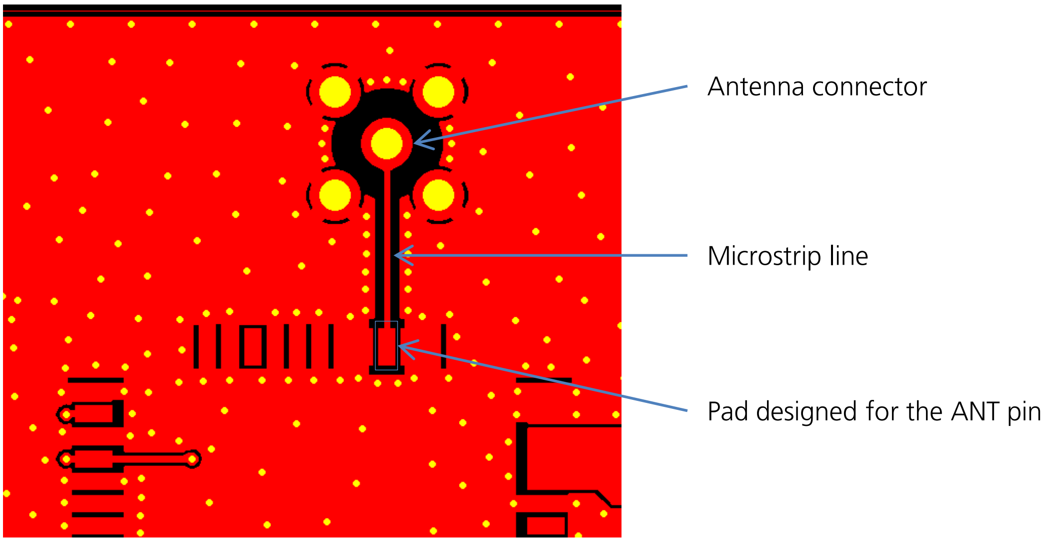

Figure 56: Layer 1 (top layer) of u-blox approved interface board for LISA-U series modules

The thickness of the dielectric (FR4 Prepreg 1080) from Layer 1 (top layer) to Layer 2 (inner layer) is 0.27 mm.
The Layer 2 (inner layer, described in Figure 57) provides a GND plane.
Layer 2 thickness is 0.035 mm.

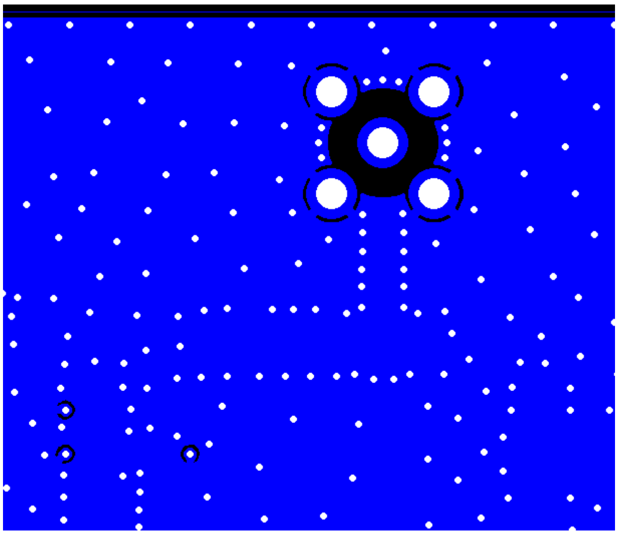

Figure 57: Layer 2 (inner layer) of u-blox approved interface board for LISA-U series modules

The dielectric thickness (FR4 Laminate 7628) from Layer 2 (inner layer) to Layer 3 (inner layer) is 0.76 mm.
The Layer 3 (inner layer, described in Figure 58) is designed for signals routing and GND plane.
Layer 3 thickness is 0.035 mm.

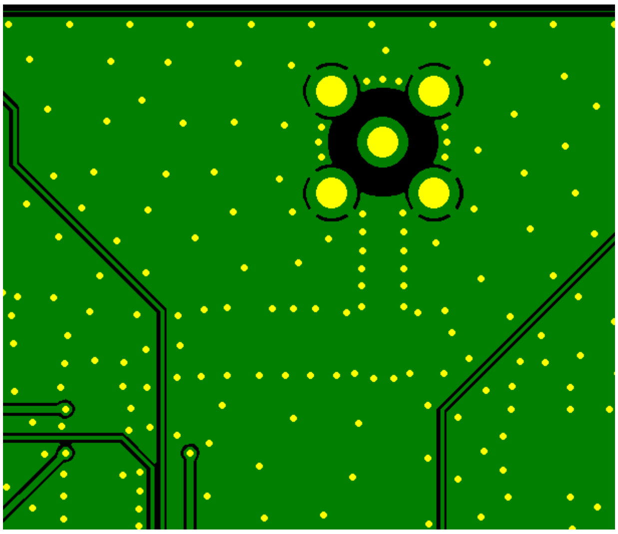

Figure 58: Layer 3 (inner layer) of u-blox approved interface board for LISA-U series modules

The dielectric thickness (FR4 Prepreg 1080) from Layer 3 (inner layer) to Layer 4 (bottom layer) is 0.27 mm.

The Layer 4 (bottom layer, described in Figure 59) is designed for signals routing, components placement and GND plane.

Layer 4 thickness is 0.035 mm.

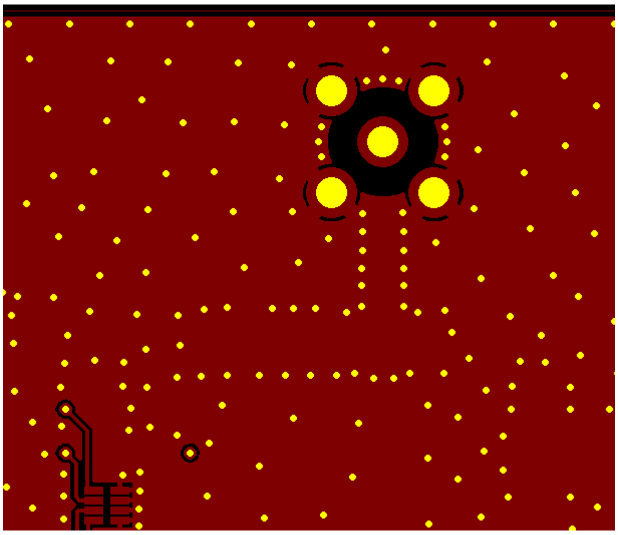

Figure 59: Layer 4 (bottom layer) of u-blox approved interface board for LISA-U series modules

☞ The antenna gain must not exceed the levels reported in the chapter 1.15.3.2 to preserve the original u-blox FCC ID.

☞ The antenna must be installed and operated with a minimum distance of 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Under the requirements of FCC Section 15.212(a)-iv, the module must contain a permanently attached antenna, or contain an unique antenna connector, and be marketed and operated only with specific antenna(s).

☞ In accordance with FCC Section 15.203, the antenna should use a unique coupling connector to the approved reference design for LISA-U series modules, to ensure that the design will not be deployed with antenna of different characteristic from the approved type.

The use of standard SMA type connector is not permitted, as its standard usage allows easy replacement of the attached antenna. However RP-SMA (Reverse-Polarized-SMA) connector type fulfills the minimum requirements to prevent exchangeability of antenna on the reference design.

2.2.1.2 Main DC supply connection

The DC supply of LISA-U series modules is very important for the overall performance and functionality of the integrated product. For detailed description, check the design guidelines in section 1.5.2. Some main characteristics are:

- **VCC** pins are internally connected, but it is recommended to use all the available pins in order to minimize the power loss due to series resistance
- **VCC** connection may carry a maximum burst current in the order of 2.5 A. Therefore, it is typically implemented as a wide PCB line with short routing from DC supply (DC-DC regulator, battery pack, etc)
- The module automatically initiates an emergency shutdown if supply voltage drops below hardware threshold. In addition, reduced supply voltage can set a worst case operation point for RF circuitry that may behave incorrectly. It follows that each voltage drop in the DC supply track will restrict the operating margin at the main DC source output. Therefore, the PCB connection must exhibit a minimum or zero voltage drop. Avoid any series component with Equivalent Series Resistance (ESR) greater than a few milliohms
- Given the large burst current, **VCC** line is a source of disturbance for other signals. Therefore route **VCC** through a PCB area separated from sensitive analog signals. Typically it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing
- The **VCC** supply current supply flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source
- A tank capacitor with low ESR is often used to smooth current spikes. This is most effective when placed as close as possible to **VCC**. From main DC source, first connect the capacitor and then **VCC**. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and LISA-U series module tank capacitor. Note that the capacitor voltage rating may be adequate to withstand the charger over-voltage if battery-pack is used
- **VCC** is directly connected to the RF power amplifiers. Add capacitor in the pF range from **VCC** to GND along the supply path
- Since **VCC** is directly connected to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the LISA-U series modules in the worst case
- The large current generates a magnetic field that is not well isolated by PCB ground layers and which may interact with other analog modules (e.g. VCO) even if placed on opposite side of PCB. In this case route **VCC** away from other sensitive functional units
- The typical GSM burst has a periodic nature of approx. 217 Hz, which lies in the audible audio range. Avoid coupling between **VCC** and audio lines (especially microphone inputs)
- If **VCC** is protected by transient voltage suppressor / reverse polarity protection diode to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the LISA-U series module, preferably closer to the DC source (otherwise functionality may be compromised)

☞ **VCC** line should be wide and short.

☞ Route away from sensitive analog signals.

2.2.1.3 USB signal

The LISA-U series modules include a high-speed USB 2.0 compliant interface with a maximum throughput of 480 Mb/s (see Section 1.9.3). Signals **USB_D+** / **USB_D-** carry the USB serial data and signaling. The lines are used in single ended mode for relatively low speed signaling handshake, as well as in differential mode for fast signaling and data transfer. Characteristic impedance of **USB_D+** / **USB_D-** lines is specified by USB standard. The most important parameter is the differential characteristic impedance applicable for odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential: signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

- Route **USB_D+** / **USB_D-** lines as a differential pair
- Ensure the differential characteristic impedance is as close as possible to 90 Ω
- Consider design rules for **USB_D+** / **USB_D-** similar to RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area

2.2.1.4 Analog audio (LISA-U120 / LISA-U130 only)

Accurate analog audio design is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 217 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise from audio lines due to both **VCC** burst noise coupling and RF detection.

Analog audio is separated in the two paths,

1. Audio Input (uplink path): **MIC_P** / **MIC_N**
2. Audio Outputs (downlink path): **SPK_P** / **SPK_N**

The most sensitive is the uplink path, since the analog input signals are in the microVolts range.

- Avoid coupling of any noisy signals to microphone input lines
- It is strongly recommended to route MIC signals away from battery and RF antenna lines. Try to skip fast switching digital lines as well
- Keep ground separation from other noisy signals. Use an intermediate GND layer or vias wall for coplanar signals
- **MIC_P** and **MIC_N** are sensed differentially within the module. Therefore they should be routed as a differential pair up to the audio signal source
- Cross other signals lines on adjacent layers with 90° crossing
- Place bypass capacitor for RF very close to active microphone. The preferred microphone should be designed for GSM applications which typically have internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device
- The bias for an external electret active microphone is not provided by the module. Verify that microphone is properly biased from an external low noise supply and verify that the supply noise is properly filtered

Output audio lines have two separated configurations.

- **SPK_P** / **SPK_N** are high level balanced output. They are DC coupled and must be used with a speaker connected in bridge configuration
- Route **SPK_P** / **SPK_N** as differential pair, to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise
- Consider enlarging PCB lines, to reduce series resistive losses, when the audio output is directly connected to low impedance speaker transducer
- Use twisted pair cables for balanced audio usage

- If DC decoupling is required, a large capacitor needs to be used, typically in the microFarad range, depending on the load impedance, in order to not increase the lower cut-off frequency of its High-Pass RC filter response

2.2.1.5 Module grounding

Good connection of the module with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer
- The shielding metal tabs are connected to GND, and are a fundamental part of electrical grounding and thermal heat-sink. Connect them to board solid ground layer, by soldering them on the baseboard using PCB plated through holes connected to **GND** net
- If the application board is a multilayer PCB, then it is required to connect together each GND area with complete via stack down to main board ground layer
- It is recommended to implement one layer of the application board as ground plane
- Good grounding of **GND** pads will also ensure thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating

2.2.1.6 Other sensitive pins

A few other pins on the LISA-U series modules requires careful layout.

- **RTC supply (V_BCKP):** avoid injecting noise on this voltage domain as it may affect the stability of sleep oscillator
- **Power-On (PWR_ON):** is the digital input to switch-on the LISA-U series modules. Ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request

2.2.1.7 High-speed digital pins

The following high speed digital pins require careful layout:

- **Serial Peripheral Interface (SPI)**: can be used for high speed data transfer (UMTS/HSPA) between the LISA-U series modules and the host processor, with a data rate up to 26 Mb/s (see Section 1.9.3). The high-speed data rate is carried by signals **SPI_SCLK**, **SPI_MISO** and **SPI_MOSI**, while **SPI_SRDY** and **SPI_MRDY** behave as handshake signals with relatively low activity
- **Digital Clock Output (CODEC_CLK)**: can be used to provide a 26 MHz or 13 MHz digital clock to an external audio codec

Follow these hints for high speed digital pins layout:

- High-speed signals become sources of digital noise, route away from RF and other sensitive analog signals

Keep routing short and minimize parasitic capacitance to preserve digital signal integrity

2.2.1.8 Digital pins and supplies

- **External Reset (RESET_N):** input for external reset, a logic low voltage will reset the module
- **SIM Card Interface (VSIM, SIM_CLK, SIM_IO, SIM_RST)**: the SIM layout may be critical if the SIM card is placed far away from the LISA-U series modules or in close proximity to the RF antenna. In the first case the long connection can cause the radiation of some harmonics of the digital data frequency. In the second case the same harmonics can be picked up and create self-interference that can reduce the sensitivity of GSM Receiver channels whose carrier frequency is coincidental with harmonic frequencies. The latter case, placing the RF bypass capacitors, suggested in Figure 21, near the SIM connector will mitigate the problem. In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection to protect module SIM pins near the SIM connector
- **Digital Audio (I2S_CLK**, **I2S_RX**, **I2S_TX**, **I2S_WA** and **I2S1_CLK**, **I2S1_RXD**, **I2S1_TXD**, **I2S1_WA)**: the I^2S interface requires the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **DDC (SCL, SDA)**: the DDC interface requires the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **UART (TXD, RXD, CTS, RTS, DSR, RI, DCD, DTR)**: the serial interface requires the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **General Purpose I/O (GPIOx)**: the general purpose input/output pins are generally not critical for layout
- **Reserved pins**: these pins are reserved for future use. Leave them unconnected on the baseboard
- **USB detection (VUSB_DET)**: this input will generate an interrupt to the baseband processor for USB detection. The USB supply (5.0 V typ.) must be provided to **VUSB_DET** by the connected USB host to enable the USB interface of the module
- **Interfaces Supply (V_INT)**: this supply output is generated by an integrated switching step down converter, used internally to supply the digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals

2.2.2 Footprint and paste mask

The following figure describes the footprint and provides recommendations for the paste mask for LISA-U series modules. These are recommendations only and not specifications. Note that the copper and solder masks have the same size and position.

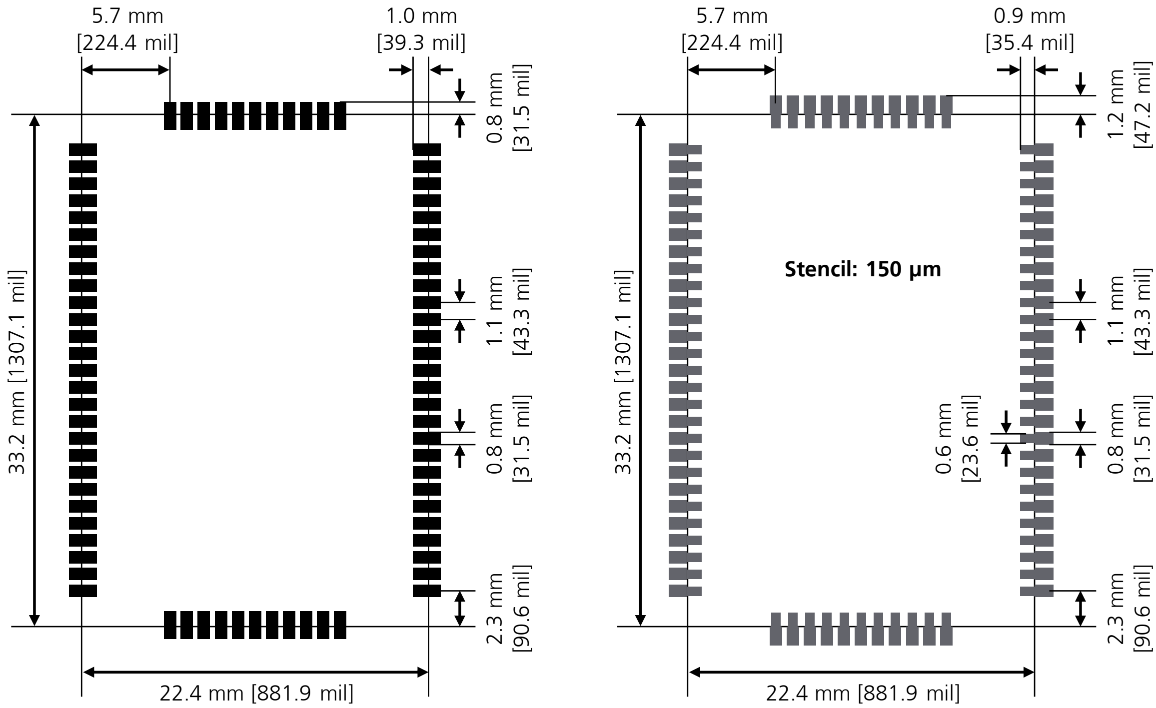

Figure 60: LISA-U series modules suggested footprint and paste mask

To improve the wetting of the half vias, reduce the amount of solder paste under the module and increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the copper mask. The solder paste should have a total thickness of 150 µm.

☞ The paste mask outline needs to be considered when defining the minimal distance to the next component.

☞ The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

The bottom layer of LISA-U1 series modules has one unprotected copper area for GND, shown in Figure 61.

The bottom layer of LISA-U2 series modules has two unprotected copper areas for GND, shown in Figure 62.

☞ Consider "No-routing" areas for the LISA-U series modules footprint as follows: signal keep-out area on the top layer of the application board, below LISA-U series modules, due to GND opening on module bottom layer (see Figure 61 and Figure 62).

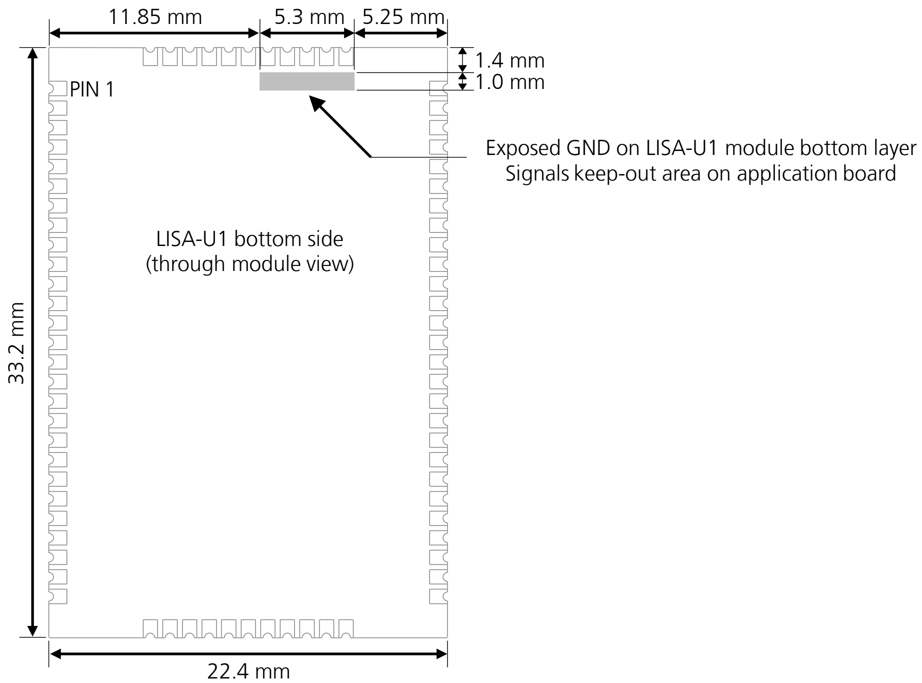

Figure 61: Signals keep-out area on the top layer of the application board, below LISA-U1 series modules

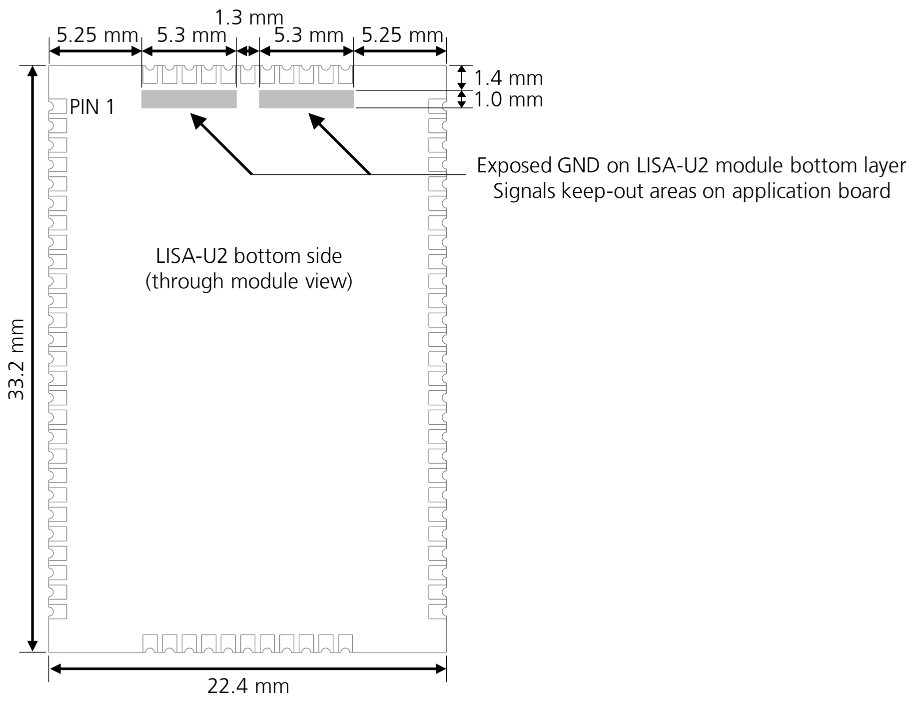

Figure 62: Signals keep-out areas on the top layer of the application board, below LISA-U2 series modules

2.2.3 Placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

Make sure that RF and analog circuits are clearly separated from any other digital circuits on the system board.

Provide enough clearance between the module and any external part due to solder and paste masks design.

Milled edges that are present at module PCB corners, away from module pins metallization, can slightly increase module dimensions from the width and the height described in the mechanical specifications sections of LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2]: provide enough clearance between module PCB corners and any other external part mounted on the application board.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the LISA-U series modules: avoid placing temperature sensitive devices (e.g. GPS receiver) close to the module.

2.3 Thermal aspects

☞ The operating temperature range is specified in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

The most critical condition concerning thermal performance is the uplink transmission at maximum power (data upload or voice call in connected mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks; however the application should be correctly designed to cope with it.

During transmission at maximum RF power the LISA-U series modules generate thermal power that can exceed 2 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the number of allocated TX slot and modulation (GMSK or 8PSK) or data rate (WCDMA), transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The Module-to-Ambient thermal resistance ($R_{th,M-A}$) of LISA-U series modules mounted on a 90 mm x 70 mm x 1.46 mm 4-Layers PCB with a high coverage of copper in still air conditions ranges between 9 and 12 °C/W. The spreading of $R_{th,M-A}$ depends on the operating condition (e.g. 2G or 3G mode, transmit band): the overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

With this setup, the increase of the module temperature[5] referred to idle state initial condition[6] is:

- around 7°C during a voice call at maximum power
- 19°C during GPRS data transfer with 4 TX slots
- 16°C during EDGE data transfer with 4 TX slots
- up to 25°C in UMTS connection at max TX power

☞ Case-to-Ambient thermal resistance value will be different for other mechanical deployments of the module, e.g. PCB with different size and characteristics, mechanical shells enclosure, or forced air flow.

The increase of thermal dissipation, i.e. reducing the thermal resistance, will decrease the operating temperature for internal circuitry of LISA-U series modules for a given operating ambient temperature. This improves the device long-term reliability for applications operating at high ambient temperature.

A few techniques may be used to reduce the thermal resistance in the application:

- Forced ventilation air-flow within mechanical enclosure
- Heat sink attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the wireless module
- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with complete via stack down to main ground layer

For example, after the installation of a robust aluminum heat-sink with forced air ventilation on the back of the same application board described above, the Module-to-Ambient thermal resistance is reduced to 1.5 ÷ 3.5 °C/W. The effect of lower $R_{th,M-A}$ can be seen from the module temperature which now becomes:

- around 1.5°C above the ambient temperature during a voice call at maximum power
- 3°C during GPRS data transfer with 4 TX slots
- 2.5°C during EDGE data transfer with 4 TX slots
- 5.5°C in UMTS connection at max TX power

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[5] Temperature is measured by internal sensor of wireless module

[6] Steady state thermal equilibrium is assumed. The module's temperature in idle state can be considered equal to ambient temperature

2.4 Antenna guidelines

Antenna characteristics are essential for good functionality of the module. Antenna radiating performance has direct impact on the reliability of connections over the Air Interface. A bad termination of the **ANT** pin (main RF input/output) and the **ANT_DIV** pin (RF input for diversity receiver provided by LISA-U230 modules) can result in poor performance of the module.

The following parameters should be checked:

Item	Recommendations
Impedance	50 Ω nominal characteristic impedance
Frequency Range	Depends on the LISA-U series module HW version and on the Mobile Network used. LISA-U100, LISA-U120: • 824..960 MHz (GSM 850, GSM 900, UMTS B5) • 1710..1990 MHz (GSM 1800, GSM 1900, UMTS B2) LISA-U110, LISA-U130: • 824..960 MHz (GSM 850, GSM 900, UMTS B8) • 1710..2170 MHz (GSM 1800, GSM 1900, UMTS B1) LISA-U200-00: • 824..960 MHz (GSM 850, GSM 900, UMTS B5, UMTS B6) • 1710..2170 MHz (GSM 1800, GSM 1900, UMTS B1, UMTS B2) LISA-U200-01, LISA-U230-01: • 824..960 MHz (GSM 850, GSM 900, UMTS B5, UMTS B6, UMTS B8) • 1710..2170 MHz (GSM 1800, GSM 1900, UMTS B1, UMTS B2, UMTS B4)
Input Power	>2 W peak
V.S.W.R	<2:1 recommended, <3:1 acceptable
Return Loss	S_{11}<-10 dB recommended, S_{11}<-6 dB acceptable

Table 45: General recommendation for GSM antenna

⚠ **The antenna gain shall remain below the levels reported in the chapter 1.15.3.2 to preserve the original u-blox FCC ID.**

Please note that some 2G and 3G bands are overlapping. This depends on worldwide band allocation for telephony services, where different bands are deployed for different geographical regions.

If the LISA-U110, LISA-U130 or LISA-U2 series modules are planned for use on the entire supported bands, then an antenna that supports the 824..960 MHz and the 1710..2170 MHz frequency range should be selected. If the LISA-U100 or LISA-U120 modules are planned for use with the entire range of supported bands, then an antenna that supports the 824..960 MHz and the 1710..1990 MHz frequency range should be selected. Otherwise, for fixed applications in specific geographical region, antenna requirements can be relaxed for non-deployed frequency bands. Refer to the operating RF frequency bands table in LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2] for the detailed uplink and downlink frequency ranges of each supported band.

LISA-U230 modules provide 2G and 3G dynamic receive diversity (Rx diversity) capability to improve the quality and reliability of the wireless link. This feature can be optionally used connecting a second antenna to the **ANT_DIV** pin, to receive an RF input signal that is processed by the module to increase the performance. All the antenna guidelines and recommendations reported are applicable also to the Rx diversity antenna design, even if the antenna for the Rx diversity is not used to transmit.

GSM antennas are typically available as:

- Linear monopole: typical for fixed applications. The antenna extends mostly as a linear element with a dimension comparable to lambda/4 of the lowest frequency of the operating band. Magnetic base may be available. Cable or direct RF connectors are common options. The integration normally requires the fulfillment of some minimum guidelines suggested by antenna manufacturer
- Patch-like antenna: better suited for integration in compact designs (e.g. mobile phone). These are mostly custom designs where the exact definition of the PCB and product mechanical design is fundamental for tuning of antenna characteristics

For integration observe these recommendations:

- Ensure 50 Ω antenna termination, minimize the V.S.W.R. or return loss, as this will optimize the electrical performance of the module. See section 2.4.1
- Select antenna with best radiating performance. See section 2.4.2
- If a cable is used to connect the antenna radiating element to application board, select a short cable with minimum insertion loss. The higher the additional insertion loss due to low quality or long cable, the lower the connectivity
- Follow the recommendations of the antenna manufacturer for correct installation and deployment
- Do not include antenna within closed metal case
- Do not place the main antenna in close vicinity to end user since the emitted radiation in human tissue is limited by S.A.R. regulatory requirements
- Do not use directivity antenna since the electromagnetic field radiation intensity is limited in some countries
- Take care of interaction between co-located RF systems since the GSM transmitted power may interact or disturb the performance of companion systems
- Place antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues that may arise
- The antenna for the Rx diversity should be carefully separated from the main Tx/Rx antenna to ensure uncorrelated signals received at each antenna, because signal improvement is dependent on the cross correlation and relative signal strength levels between the two received signals. The distance between the two antennas should be greater than half a wavelength of the lowest used frequency (i.e. distance greater than ~20 cm, for 2G/3G low bands) to distinguish between different multipath channels

2.4.1 Antenna termination

The LISA-U series modules are designed to work on a 50 Ω load. However, real antennas have no perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antenna mismatch, the following requirements should be met:

Measure the antenna termination with a network analyzer: connect the antenna through a coaxial cable to the measurement device, the $|S_{11}|$ indicates which portion of the power is delivered to antenna and which portion is reflected by the antenna back to the module output.

A good antenna should have an $|S_{11}|$ below -10 dB over the entire frequency band. Due to miniaturization, mechanical constraints and other design issues, this value will not be achieved. An $|S_{11}|$ value of about -6 dB - (in the worst case) - is acceptable.

Figure 63 shows an example of this measurement:

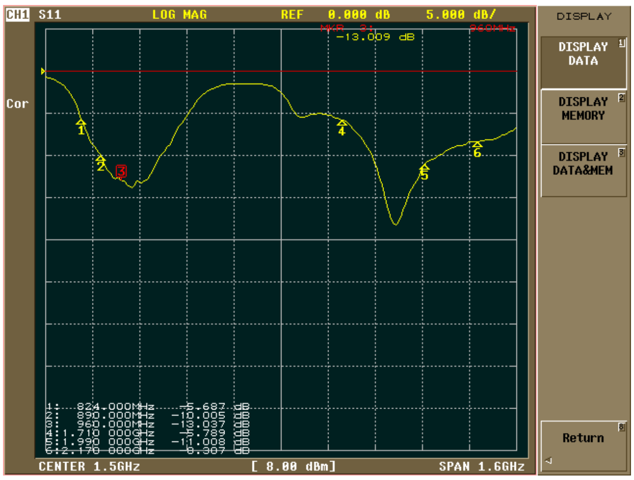


Figure 63: $|S_{11}|$ sample measurement of a penta-band antenna that covers in a small form factor the 4 GSM bands (850 MHz, 900 MHz, 1800 MHz and 1900 MHz) and the UMTS Band I

Figure 64 shows comparable measurements performed on a wideband antenna. The termination is better, but the size of the antenna is considerably larger.

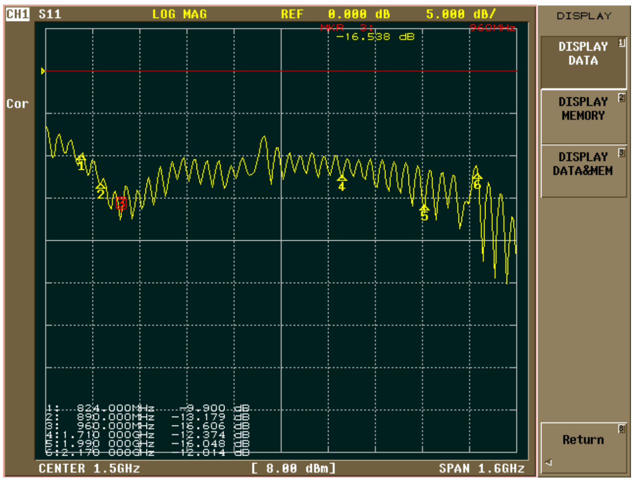


Figure 64: $|S_{11}|$ sample measurement of a wideband antenna

2.4.2 Antenna radiation

An indication of the antenna's radiated power can be approximated by measuring the $|S_{21}|$ from a target antenna to the measurement antenna, using a network analyzer with a wideband antenna. Measurements should be done at a fixed distance and orientation, and results compared to measurements performed on a known good antenna. Figure 65 through Figure 66 show measurement results. A wideband log periodic-like antenna was used, and the comparison was done with a half lambda dipole tuned at 900 MHz frequency. The measurements show both the $|S_{11}|$ and $|S_{21}|$ for the penta-band internal antenna and for the wideband antenna.

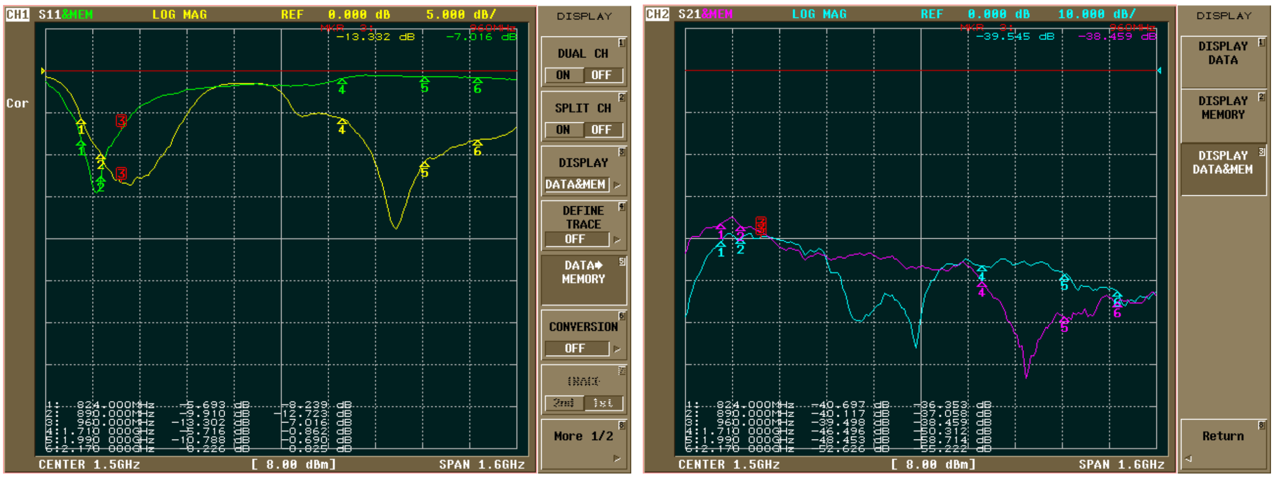


Figure 65: $|S_{11}|$ and $|S_{21}|$ comparison between a 900 MHz tuned half wavelength dipole (green/purple) and a penta-band internal antenna (yellow/cyan)

The half lambda dipole tuned at 900 MHz is known and has good radiation performance (both for gain and directivity). Then, by comparing the $|S_{21}|$ measurement with antenna under investigation for the frequency where the half dipole is tuned (e.g. marker 3 in Figure 65) it is possible to make a judgment on the antenna under test: if the performance is similar then the target antenna is good.

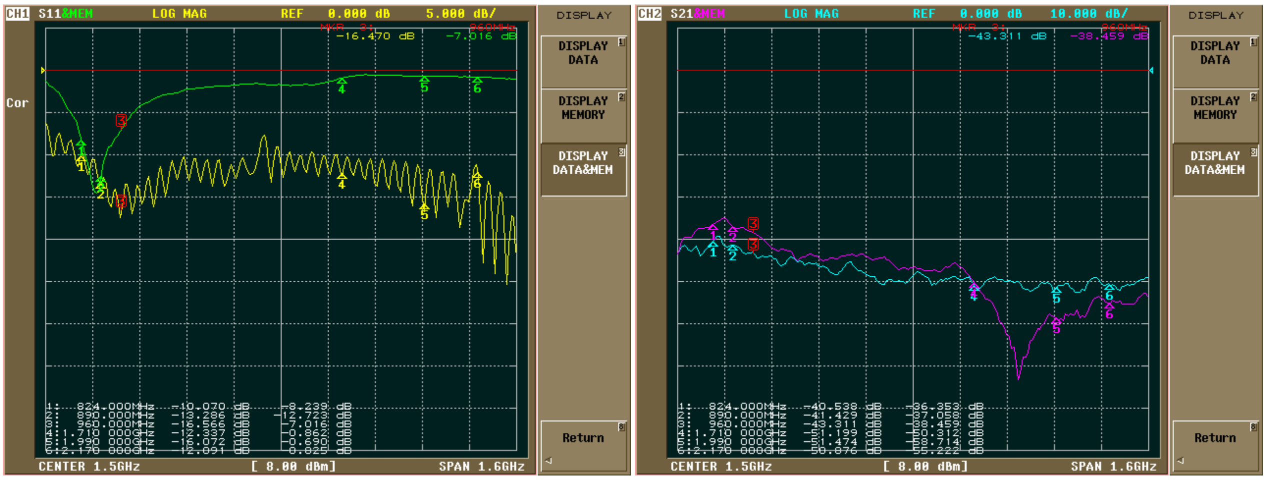


Figure 66: |S_{11}| and |S_{21}| comparison between a 900 MHz tuned half wavelength dipole (green/purple) and a wideband commercial antenna (yellow/cyan)

Instead if |S_{21}| values for the tuned dipole are much better than the antenna under evaluation (like for marker 1/2 area of Figure 66, where dipole is 5 dB better), then it can be argued that the radiation of the target antenna (the wideband dipole in this case) is considerably less.

The same procedure should be repeated on other bands with half wavelength dipole re-tuned to the band under investigation.

☞ For good antenna radiation performance, antenna dimensions should be comparable to a quarter of the wavelength. Different antenna types can be used for the module, many of them (e.g. patch antennas, monopole) are based on a resonating element that works in combination with a ground plane. The ground plane, ideally infinite, can be reduced down to a minimum size that must be similar to one quarter of the wavelength of the minimum frequency that has to be radiated (transmitted/received). Numerical sample: frequency = 1 GHz → wavelength = 30 cm → minimum ground plane (or antenna size) = 7.5 cm. Below this size, the antenna efficiency is reduced.

2.4.3 Antenna detection functionality

The internal antenna detect circuit is based on ADC measurement at **ANT**: the RF port is DC coupled to the ADC unit in the baseband chip which injects a DC current (10 µA for 128 µs) on **ANT** and measures the resulting DC voltage to evaluate the resistance from **ANT** pad to GND.

The antenna detection is forced by the +UANTR AT command: refer to the u-blox AT Commands Manual [3] for more details on how to access this feature.

To achieve antenna detection functionality, use an RF antenna with built-in resistor from **ANT** signal to GND, or implement an equivalent solution with a circuit between the antenna cable connection and the radiating element as shown in Figure 67.

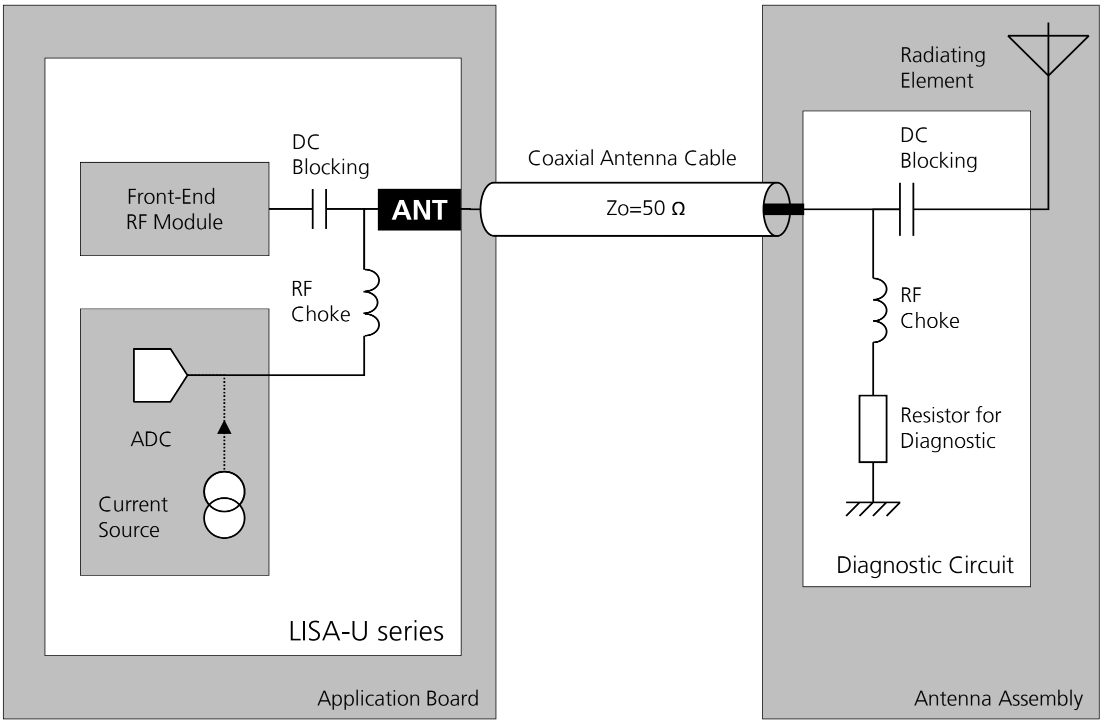


Figure 67: Antenna detection circuit and antenna with diagnostic resistor

Examples of components for the antenna detection diagnostic circuit are reported in the following table:

Description	Part Number - Manufacturer
DC Blocking Capacitor	Murata GRM1555C1H220JA01 or equivalent
RF Choke Inductor	Murata LQG15HS68NJ02, LQG15HH68NJ02 or equivalent (Self Resonance Frequency ~1GHz)
Resistor for Diagnostic	15 kΩ 5%, various Manufacturers

Table 46: Example of components for the antenna detection diagnostic circuit

Please note that the DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 67, the measured DC resistance will always be at the limits of the measurement range (respectively open or short), and there will be no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and to avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider a GSM antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from **ANT** connector to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected

- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see u-blox AT Commands Manual [3]) means that that the antenna is not connected or the RF cable is broken
- Reported values below the measurement range minimum limit (1 kΩ) will highlight a short to GND at antenna or along the RF cable
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method

2.5 ESD precautions

2.5.1 ESD immunity test overview

The immunity of the device (i.e. the application board where LISA-U series module is mounted) to the Electrostatic Discharge (ESD) must be certified in compliance to the testing standard CENELEC EN 61000-4-2 [10] and the radio equipment standards ETSI EN 301 489-1 [11], ETSI EN 301 489-7 [12], ETSI EN 301 489-24 [13], which requirements are summarized in Table 47.

The ESD immunity test is performed at the enclosure port, defined by ETSI EN 301 489-1 [11] as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of ESD immunity test to the whole device depends on the device classification as defined by ETSI EN 301 489-1 [11]. Applicability of ESD immunity test to the relative device ports or the relative interconnecting cables to auxiliary equipments, depends on device accessible interfaces and manufacturer requirements, as defined by ETSI EN 301 489-1 [11].

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in CENELEC EN 61000-4-2 [10].

☞ For the definition of integral antenna, removable antenna, antenna port, device classification refer to ETSI EN 301 489-1 [11].

☞ The contact and air discharges are defined in CENELEC EN 61000-4-2 [10].

Application	Category	Immunity Level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Contact Discharge	4 kV
	Air Discharge	8 kV

Table 47: Electromagnetic Compatibility ESD immunity requirements as defined by standards CENELEC EN 61000-4-2, ETSI EN 301 489-1 V1.8.1, ETSI EN 301 489-7 V1.3.1, ETSI EN 301 489-24 V1.4.1

2.5.2 ESD immunity test of LISA-U series reference design

Although electromagnetic compatibility (EMC) certification must be performed by the final application of the radio equipment under test (i.e. the application board where LISA-U series module is mounted), EMC certification (including ESD immunity) have been successfully performed on LISA-U1 series and LISA-U200-00 modules reference design according to CENELEC EN 61000-4-2 [10], ETSI EN 301 489-1 [11], ETSI EN 301 489-7 [12] and ETSI EN 301 489-24 [13] standards.

The EMC approved reference design consists of a LISA-U1 series or a LISA-U200-00 module soldered on a motherboard which provides an interface to power supply, SIM card, headset and communication port. An external antenna is connected to an SMA connector provided on the motherboard.

Since an external antenna is used, the antenna port can be separated from the enclosure port. The reference design is not enclosed in a box so the enclosure port is not indentified with physical surfaces. Therefore, some test cases cannot be applied. Only the antenna port is identified as accessible for direct ESD exposure.

The reference application implements all precautions described in the section 2.5.3. ESD immunity test results and applicability are reported in Table 48 according to test requirements CENELEC EN 61000-4-2 [10], ETSI EN 301 489-1 [11], ETSI EN 301 489-7 [12] and ETSI EN 301 489-24 [13].

Category	Application	Immunity Level
Contact Discharge to coupling planes (indirect contact discharge)	Enclosure	+2 kV / -2 kV
		+4 kV / -4 kV
Contact Discharges to conducted surfaces (direct contact discharge)	Enclosure port	Not Applicable[7]
Contact Discharges to conducted surfaces (direct contact discharge)	Antenna port (only antenna with completely insulating surface can be used)	Not Applicable[8]
Air Discharge at insulating surfaces	Enclosure port	Not Applicable[9]
Air Discharge at insulating surfaces	Antenna port (only antenna with completely insulating surface can be used)	+2 kV /
		+4 kV /
		+8 kV /

Table 48: Enclosure ESD immunity level (as defined by standards CENELEC EN 61000-4-2, ETSI EN 301 489-1 V1.8.1, ETSI EN 301 489-7 V1.3.1, ETSI EN 301 489-24 V1.4.1) of LISA-U1 series and LISA-U200-00 modules application reference design

[7] LISA-U1 series or LISA-U200-00 module mounted on application design:
Not Applicability: EUT with insulating enclosure surface, EUT without enclosure surface
Applicability: EUT with conductive enclosure surface

[8] LISA-U1 series or LISA-U200-00 module mounted on application design:
Not Applicability: Antenna with insulating surface
Applicability: Antenna with conductive surface

[9] LISA-U1 series or LISA-U200-00 module mounted on application design:
Applicability: EUT with insulating enclosure surface
Not Applicability: EUT with conductive enclosure surface, EUT without enclosure surface

2.5.3 ESD application circuits

The application circuits described in this section should be implemented, depending on the application board handling, to satisfy ESD immunity test requirements. These are defined in CENELEC EN 61000-4-2 [10], ETSI EN 301 489-1 [11] and ETSI EN 301 489-7 [12], and performed at the device enclosure in compliance to the category level defined in ETSI EN 301 489-1 [11]. The test requirements are summarized in Table 47.

Antenna interface

With LISA-U1 series modules, the **ANT** pin provides ESD immunity up to 500 V (contact and air discharge according to IEC 61000-4-2): higher protection level is required if the line is externally accessible on the device (i.e. the application board where LISA-U1 series module is mounted).

The following precautions are suggested to satisfy ESD immunity test requirements using LISA-U1 series modules:

- If the device implements an embedded antenna, the insulating enclosure of the device should provide protection to direct contact discharge up to +4 kV / -4 kV and protection to air discharge up to +8 kV / -8 kV to the antenna interface
- If the device implements an external antenna, the antenna and its connecting cable should provide a completely insulated enclosure able to provide protection to direct contact discharge up to +4 kV / -4 kV and protection to air discharge up to +8 kV / -8 kV to the whole antenna and cable surfaces

With the LISA-U200-00 module, the **ANT** pin provides ESD immunity up to 1000 V (contact and air discharge according to IEC 61000-4-2): higher protection level is required if the line is externally accessible on the device (i.e. the application board where LISA-U200-00 module is mounted).

The following precautions are suggested for satisfying ESD immunity test requirements using LISA-U200-00 modules:

- If the device implements an embedded antenna, the device insulating enclosure should provide protection to direct contact discharge up to +4 kV / -4 kV and protection to air discharge up to +8 kV / -8 kV to the antenna interface
- If the device implements an external antenna, the antenna and its connecting cable should provide a completely insulated enclosure able to provide protection to direct contact discharge up to +4 kV / -4 kV and protection to air discharge up to +8 kV / -8 kV to the whole antenna and cable surfaces
- If the device implements an external antenna and the antenna and its connecting cable don't provide a completely insulated enclosure able to provide protection to direct contact discharge up to +4 kV / -4 kV and protection to air discharge up to +8 kV / -8 kV to the whole antenna and cable surfaces, an external high pass filter, consisting of a series 15 pF capacitor (Murata GRM1555C1H150JA01) and a shunt 39 nH coil (Murata LQG15HN39NJ102) should be implemented at the antenna port as described in Figure 68

☞ Antenna detection functionality is not provided when implementing the high pass filter described in Figure 68 and Table 49, as ESD protection for the LISA-U200-00 antenna port.

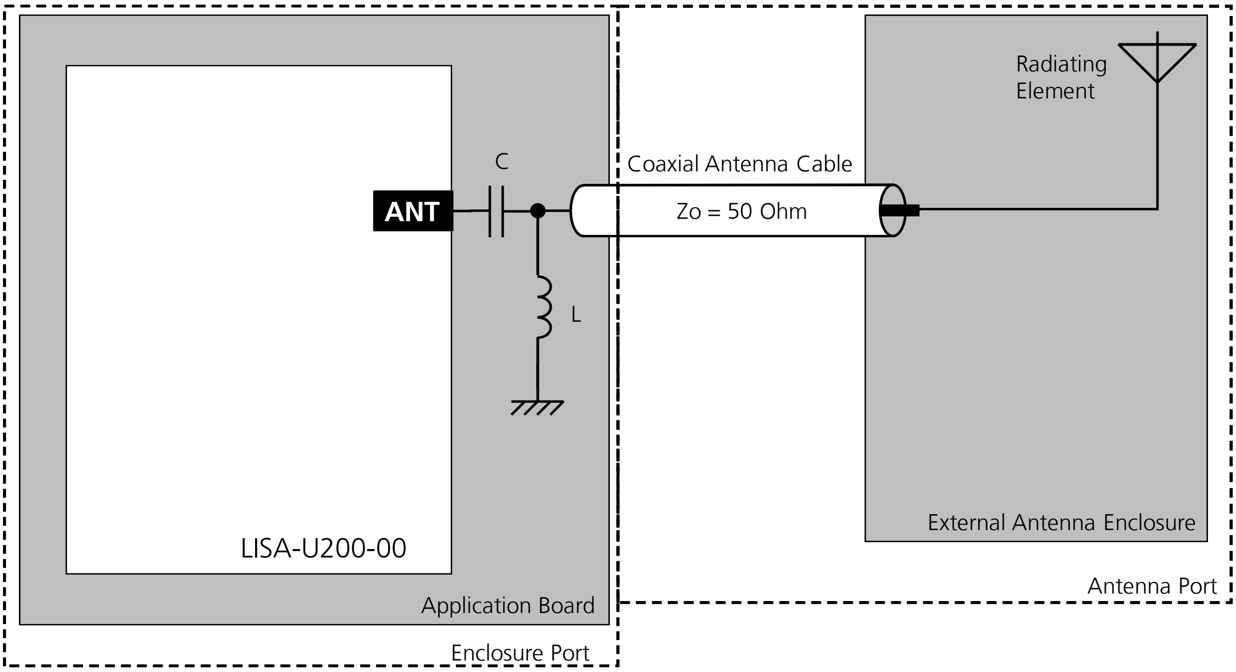


Figure 68: LISA-U200-00 antenna port ESD immunity protection application circuit

Reference	Description	Part Number - Manufacturer
C	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
L	39 nH Multilayer Chip Inductor L0G 0402 5%	LQG15HN39NJ102 - Murata

Table 49: Example of components for LISA-U200-00 antenna port ESD immunity protection application circuit

With LISA-U230 modules, the **ANT_DIV** pin provides ESD immunity up to +4 kV / -4 kV for direct Contact Discharge and up to +8 kV / -8 kV for Air Discharge: no further precaution to ESD immunity test is needed.

RESET_N pin

The following precautions are suggested for the **RESET_N** line of LISA-U series modules, depending on the application board handling, to satisfy ESD immunity test requirements:

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JA01) must be mounted on the line termination connected to the **RESET_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- A series ferrite bead (e.g. Murata BLM15HD182SN1) must be added on the line connected to the **RESET_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- An additional 220 nF bypass capacitor (e.g. Murata GRM155R60J224KE01) must be mounted as close as possible to the **RESET_N** pin of LISA-U2 series modules to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- It is recommended to keep the connection line to **RESET_N** as short as possible

Maximum ESD sensitivity rating of the **RESET_N** pin is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the **RESET_N** pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the **RESET_N** line, close to accessible point

For the **RESET_N** application circuit description refer to Figure 20 and Table 18 reported in section 1.6.3.

SIM interface

The following precautions are suggested for LISA-U series modules SIM interface (**VSIM**, **SIM_RST**, **SIM_IO**, **SIM_CLK** pins), depending on the application board handling, to satisfy ESD immunity test requirements:

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470J) must be mounted on the lines connected to **VSIM**, **SIM_RST**, **SIM_IO** and **SIM_CLK** pins to assure SIM interface functionality when an electrostatic discharge is applied to the application board enclosure
- It is suggested to use as short as possible connection lines at SIM pins

Maximum ESD sensitivity rating of SIM interface pins is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if SIM interface pins are externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Infineon ESD8V0L2B-03L or AVX USB0002) should be mounted on each SIM interface line, close to accessible points (i.e. close to the SIM card holder)

For the SIM interface application circuit description refer to Figure 21 and Table 21 reported in section 1.8.

Other pins and interfaces

All the module pins that are externally accessible on the device (i.e. the application board where LISA-U series module is mounted) should be included in the ESD immunity test since they are considered to be a port as defined in ETSI EN 301 489-1 [11]. Depending on applicability, to satisfy ESD immunity test requirements according to ESD category level, all the module pins that are externally accessible should be protected up to +4 kV / -4 kV for direct Contact Discharge and up to +8 kV / -8 kV for Air Discharge applied to the enclosure surface.

The maximum ESD sensitivity rating of all the other pins of the module is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the relative pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- **USB interface**: a very low capacitance (i.e. less or equal to 1 pF) ESD protection device (e.g. Tyco Electronics PESD0402-140 ESD protection device) should be mounted on the **USB_D+** and **USB_D-** lines, close to the accessible points (i.e. close to the USB connector)
- **SPI interface**: a low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Infineon ESD8V0L2B-03L or AVX USB0002) should be mounted on the **SPI_MISO**, **SPI_MOSI**, **SPI_SCLK**, **SPI_MRDY**, **SPI_SRDY** lines, close to accessible points
- **CODEC_CLK**: a low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Infineon ESD8V0L2B-03L or AVX USB0001) should be mounted on the **CODEC_CLK** line, close to accessible point
- **Other pins**: a general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the relative line, close to accessible point

3 Features description

3.1 Firmware (upgrade) Over AT (FOAT)

☞ Not supported by LISA-U1xx-00 modules.

3.1.1 Overview

This feature allows upgrading the module Firmware over UART and USB, using AT Commands.

- AT Command AT+UFWUPD triggers a reboot followed by the upgrade procedure at specified a baud rate (refer to u-blox AT Commands Manual [3] for more details)
- The Xmodem-1k protocol is used for downloading the new Firmware image via a terminal application
- A special boot loader on the module performs firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the firmware download from the Xmodem-1k handshake. After completing the upgrade, the module is reset again and wakes-up in normal boot

3.1.2 FOAT procedure

The application processor must proceed in the following way:

- Send the AT+UFWUPD command through the UART or over the USB interface, specifying the file type and the desired baud rate
- Reconfigure the serial communication at the selected baud rate, without flow control with the Xmodem-1k protocol
- Send the new FW image via Xmodem-1k

3.2 TCP/IP and UDP/IP

Via the AT commands it's possible to access the TCP/IP and UDP/IP functionalities over the Packet Switched data connection. For more details about AT commands see the u-blox AT Commands Manual [3].

Direct Link mode for TCP and UDP sockets is supported by all LISA-U series modules except LISA-U1xx-00 versions. Sockets can be set in Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via serial interface.

3.2.1 Multiple PDP contexts and sockets

Two PDP context types are defined:

- "external" PDP context: IP packets are built by the DTE, the MT's IP instance runs the IP relay function only
- "internal" PDP context: the PDP context (relying on the MT's TCP/IP stack) is configured, established and handled via the data connection management packet switched data commands described in u-blox AT commands manual [3]

Multiple PDP contexts are supported. The DTE can access these PDP contexts either alternatively through the physical serial port, or simultaneously through the virtual serial ports of the multiplexer (multiplexing mode MUX), with the following constraints:

- Using the MT's embedded TCP/IP stack, only 1 internal PDP context is supported. This IP instance supports up to 7 sockets

- Using only external PDP contexts, it is possible to have at most 3 IP instances (with 3 different IP addresses) simultaneously. If in addition the internal PDP context is used, at most 2 external PDP contexts can be activated

Secondary PDP contexts (PDP contexts sharing the IP address of a primary PDP context) are also supported. Traffic Flow Filters for such secondary contexts shall be specified according to 3GPP TS 23.060 [19].

At most 2 secondary PDP contexts can be activated, since the maximum number of PDP contexts, both normal and secondary, is always 3.

3.3 FTP and FTPS

☞ Not supported by LISA-U1xx-00 modules.

LISA-U series modules support the File Transfer Protocol and Secure File Transfer Protocol functionalities via AT commands. Files are read and stored in the local file system of the module. For more details about AT commands see u-blox AT Commands Manual [3].

3.4 HTTP and HTTPS

☞ Not supported by LISA-U1xx-00 modules.

HTTP and HTTPS clients are implemented in LISA-U series modules. HEAD, GET, POST, DELETE and PUT operations are available. The file size to be uploaded / downloaded depends on the free space available in the local file system (FFS) at the moment of the operation. Up to 4 client contexts can be simultaneously used.

For more details about AT commands see the u-blox AT Commands Manual [3].

3.5 AssistNow clients and GPS integration

☞ Not supported by LISA-U200-00 modules.

For customers using u-blox GPS receivers, LISA-U series wireless modules feature embedded AssistNow clients. AssistNow A-GPS provides better GPS performance and faster Time-To-First-Fix. The clients can be enabled and disabled with an AT command (see the u-blox AT Commands Manual [3]).

LISA-U series modules act as a stand-alone AssistNow client, making AssistNow available with no additional requirements for resources or software integration on an external host micro controller. Full access to u-blox GPS receivers is available via the LISA-U series, through a dedicated DDC (I^2C) interface, while the available GPIOs can handle the GPS device power-on/off. This means that GSM/WCDMA and GPS can be controlled through a single serial port from any host processor.

3.6 Jamming Detection

☞ Not supported by LISA-U1xx-00 modules.

In real network situations modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operators' choices, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carriers entitled to give access to the GSM/UMTS service.

The Jamming Detection Feature detects such "artificial" interference and reports the start and stop of such conditions to the client, which can react appropriately by e.g. switching off the radio transceiver in order to reduce power consumption and monitoring the environment at constant periods.

The feature consists of detecting, at radio resource level, an anomalous source of interference and signaling it to the client with an unsolicited indication when the detection is entered or released. The jamming condition occurs when:

- The module has lost synchronization with the serving cell and cannot select any other cell
- The band scan reveals at least n carriers with power level equal or higher than threshold
- On all such carriers, no synchronization is possible

The number of minimum disturbing carriers and the power level threshold can be configured by the client by using the AT+UCD command [3].

The jamming condition is cleared when any of the above mentioned statements does not hold.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command (for more details refer to the u-blox AT Commands Manual [3]).

3.7 In-Band modem

☞ Not supported by LISA-U100, LISA-U110, LISA-U120-00, LISA-U130-00, LISA-U200-00 modules versions.

LISA-U series modules implements the in-Band modem solution for eCall according to the 3GPP TS 26.267 specification [14].

According to the eCall (Pan-European automatic in-vehicle emergency call system) specification, an eCall must be generated automatically or manually following an car accident using GSM cellular service "112". When activated, the in-vehicle eCall system (IVS) creates an emergency call carrying both voice and data (e.g. vehicle GPS position) directly to the nearest 112 Public Safety Answering Point (PSAP) to quickly decide upon detaching rescue services to the known position.

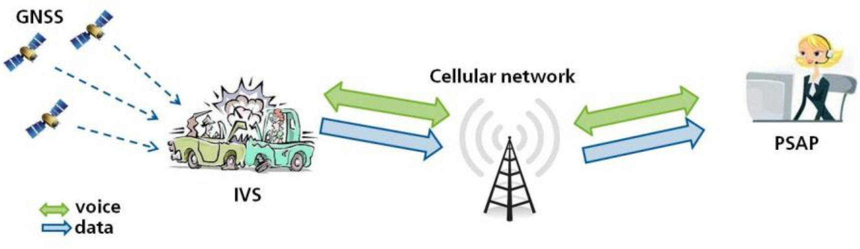


Figure 69: In-Band modem diagram flow

In-Band modem allows the fast and reliable transmission of vehicle Minimum Set of Data (MSD - 140 bytes) and the establishment of a voice emergency call using the same physical channel (voice channel) without any modifications of the existing cellular network architecture.

In-Band modem is a mandatory feature to meet the eCall requirements and to develop in vehicle devices fully supporting eCall.

3.8 Smart Temperature Management

Wireless modules – independent of the specific model –always have a well defined operating temperature range. This range should be respected to guarantee full device functionality and long life span.

Nevertheless there are environmental conditions that can affect operating temperature, e.g. if the device is located near a heating/cooling source, if there is/isn't air circulating, etc.

The module itself can also influence the environmental conditions; such as when it is transmitting at full power. In this case its temperature increases very quickly and can raise the temperature nearby.

The best solution is always to properly design the system where the module is integrated. Nevertheless an extra check/security mechanism embedded into the module is a good solution to prevent operation of the device outside of the specified range.

3.8.1 Smart Temperature Supervisor (STS)

The Smart Temperature Supervisor is activated and configured by a dedicated AT+USTS command. Please refer to u-blox AT Commands Manual [3] for more details.

The wireless module measures the internal temperature (Ti) and its value is compared with predefined thresholds to identify the actual working temperature range.

Temperature measurement is done inside the wireless module: the measured value could be different from the environmental temperature (Ta).

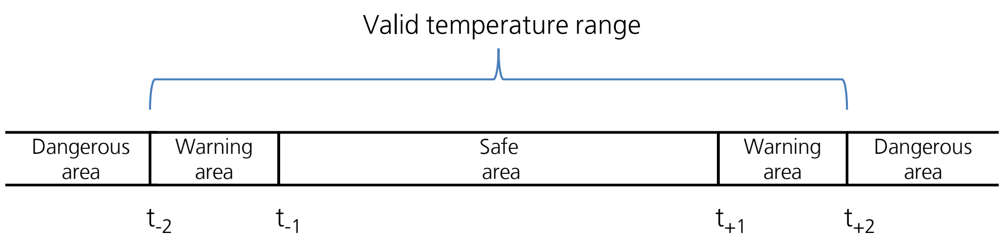


Figure 70: Temperature range and limits

The entire temperature range is divided into sub-regions by limits (see Figure 70) named t_{-2}, t_{-1}, t_{+1} and t_{+2}.

- Within the first limit, ($t_{-1} < Ti < t_{+1}$), the wireless module is in the normal working range, the Safe Area
- In the Warning Area, ($t_{-2} < Ti < t_{-1}$) or ($t_{+1} < Ti < t_{+2}$), the wireless module is still inside the valid temperature range, but the measured temperature approaches the limit (upper or lower). The module sends a warning to the user (through the active AT communication interface), which can take, if possible, the necessary actions to return to a safer temperature range or simply ignore the indication. The module is still in a valid and good working condition
- Outside the valid temperature range, ($Ti < t_{-2}$) or ($Ti > t_{+2}$), the device is working outside the specified range and represents a dangerous working condition. This condition is indicated and the device shuts down to avoid damage

For security reasons the shutdown is suspended in case an emergency call in progress. In this case the device will switch off at call termination.

The user can decide at anytime to enable/disable the Smart Temperature Supervisor feature. If the feature is disabled there is no embedded protection against disallowed temperature conditions.

Figure 71 shows the flow diagram implemented in LISA-U series modules for the Smart Temperature Supervisor.

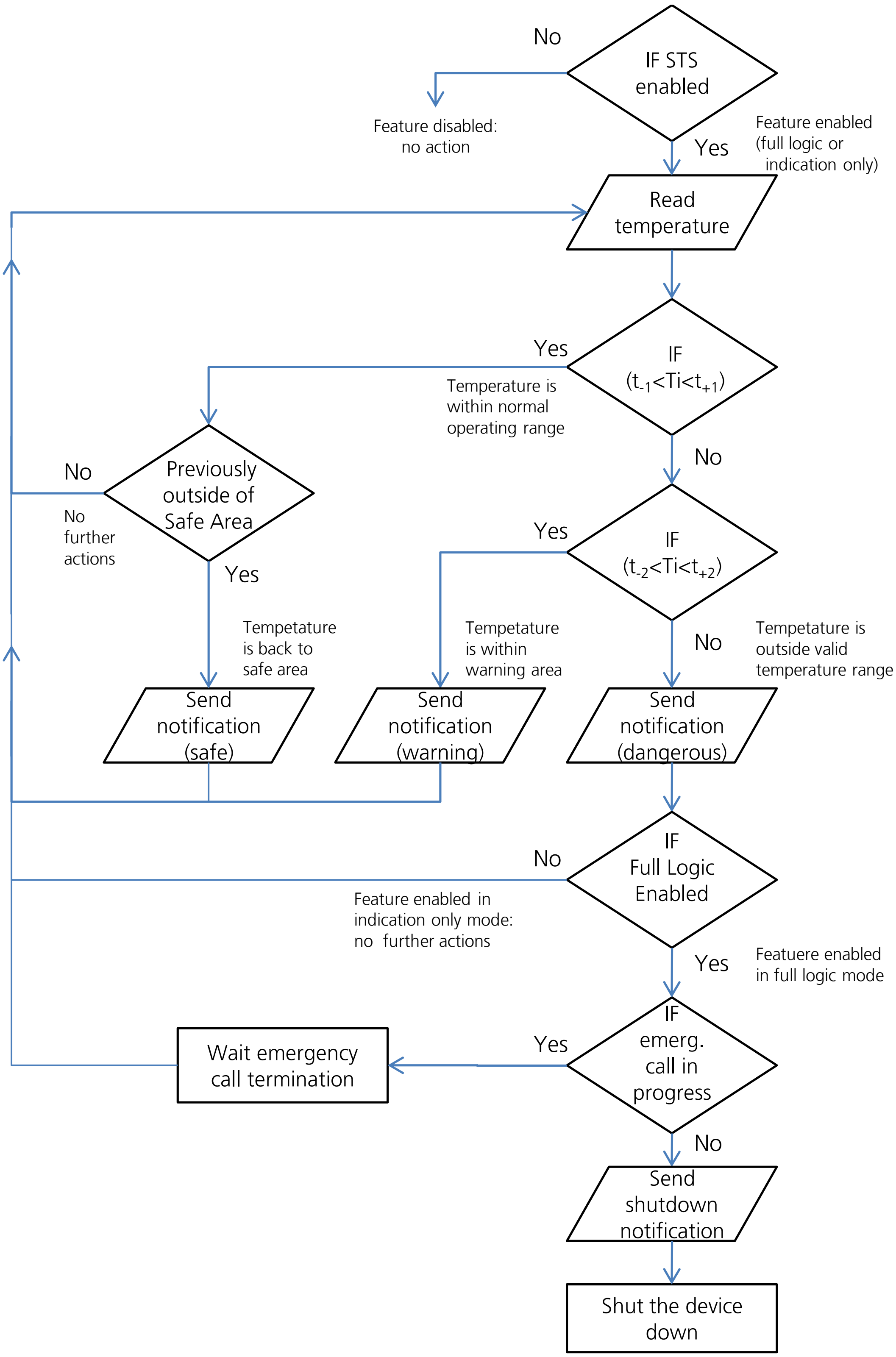


Figure 71: Smart Temperature Supervisor (STS) flow diagram

3.8.2 Threshold Definitions

When the application of wireless module operates at extreme temperatures with Smart Temperature Supervisor enabled, the user should note that outside the valid temperature range the device will automatically shut down as described above.

The input for the algorithm is always the temperature measured within the wireless module (Ti, internal). This value can be higher than the working ambient temperature (Ta, ambient), since (for example) during transmission at maximum power a significant fraction of DC input power is dissipated as heat This behavior is partially compensated by the definition of the upper shutdown threshold (t_{+2}) that is slightly higher than the declared environmental temperature limit.

The temperature thresholds are defined according the Table 50.

Symbol	Parameter	Temperature	Remarks
t_{-2}	Low temperature shutdown	–40 °C	Equal to the absolute minimum temperature rating for the wireless module (the lower limit of the extended temperature range)
t_{-1}	Low temperature warning	–30 °C	10°C above t_{-2}
t_{+1}	High temperature warning	+77 °C	20°C below t_{+2}. The higher warning area for upper range ensures that any countermeasures used to limit the thermal heating will become effective, even considering some thermal inertia of the complete assembly.
t_{+2}	High temperature shutdown	+97 °C	Equal to the internal temperature Ti measured in the worst case operating condition at typical supply voltage when the ambient temperature Ta in the reference setup (*) equals the absolute maximum temperature rating (upper limit of the extended temperature range)
(*)LISA-U series module mounted on a 90 mm x 70 mm x 1.46 mm 4-Layers PCB with a high coverage of copper within climatic chamber			

Table 50: Thresholds definition for Smart Temperature Supervisor on the LISA-U series modules

☞ The sensor measures board temperature inside the shields, which can differ from ambient temperature.

3.9 Hybrid positioning and CellLocate

☞ Not supported by LISA-U1xx-00 and LISA-U200-00 modules versions.

Although GPS is a widespread technology, its reliance on the visibility of extremely weak GPS satellite signals means that positioning is not always possible. Especially difficult environments for GPS are indoors, in enclosed or underground parking garages, as well as in urban canyons where GPS signals are blocked or jammed by multipath interference. The situation can be improved by augmenting GPS receiver data with cellular network information to provide positioning information even when GPS reception is degraded or absent. This additional information can benefit numerous applications.

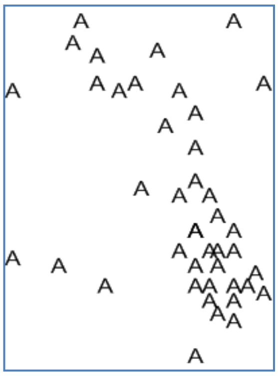
3.9.1 Positioning through cellular information: CellLocate

u-blox CellLocate enables the estimation of device position based on the parameters of the mobile network cells visible to the specific device. To estimate its position the u-blox Wireless module sends the CellLocate server the parameters of network cells visible to it using a UDP connection. In return the server provides the estimated position based on the CellLocate database. The u-blox Wireless module can either send the parameters of the visible home network cells only (normal scan) or the parameters of all surrounding cells of all mobile operators (deep scan).

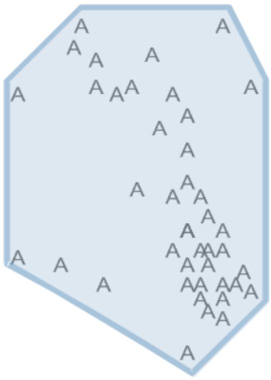
☞ Normal scan is only possible in 2G mode.

The CellLocate database is compiled from the position of devices which observed, in the past, a specific cell or set of cells (historical observations) as follows:

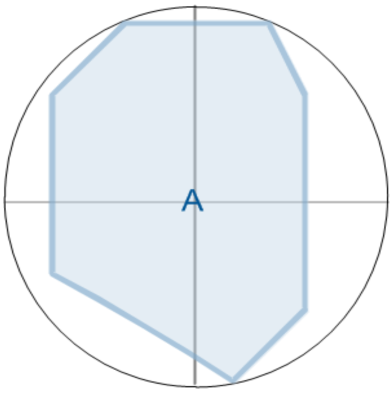
1. Several devices reported their position to the CellLocate server when observing a specific cell (the As in the picture represent the position of the devices which observed the same cell A)



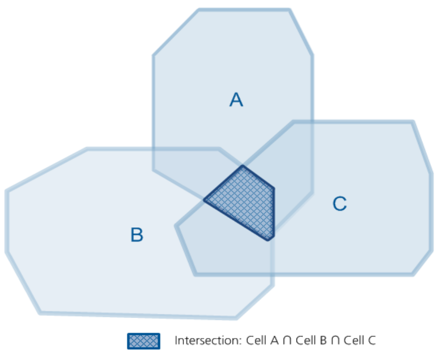
2. CellLocate server defines the area of Cell A visibility



3. If a new device reports the observation of Cell A CellLocate is able to provide the estimated position from the area of visibility



4. The visibility of multiple cells provides increased accuracy based on the intersection of areas of visibility.



CellLocate is implemented using a set of two AT commands that allow configuration of the CellLocate service (AT+ULOCCELL) and requesting position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy.

☞ The accuracy of the position estimated by CellLocate depends on the availability of historical observations in the specific area.

3.9.2 Hybrid positioning

With u-blox Hybrid positioning technology, u-blox wireless devices can be triggered to provide their current position using either a u-blox GPS receiver or the position estimated from CellLocate. The choice depends on which positioning method provides the best and fastest solution according to the user configuration, exploiting the benefit of having multiple and complementary positioning methods.

Hybrid positioning is implemented through a set of three AT commands that allow configuration of the GNSS receiver (AT+ULOCGNSS), configuration of the CellLocate service (AT+ULOCCELL), and requesting the position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy (if the position has been estimated by CellLocate), and additional parameters if the position has been computed by the GNSS receiver.

The configuration of mobile network cells does not remain static (e.g. new cells are continuously added or existing cells are reconfigured by the network operators). For this reason, when a Hybrid positioning method has been triggered and the GNSS receiver calculates the position, a database self-learning mechanism has been implemented so that these positions are sent to the server to update the database and maintain its accuracy.

The use of hybrid positioning requires a connection via the DDC (I^2C) bus between the LISA-U series wireless module and the u-blox GPS receiver (Refer to chapter 1.10).

Refer to GPS Implementation Application Note [16] for the complete description of the feature.

☞ u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate server u-blox is unable to track the SIM used or the specific device.

4 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

4.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the LISA-U1 series Data Sheet [1], the LISA-U2 series Data Sheet [2] and u-blox Package Information Guide [21].

The LISA-U series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ **Ensure ESD precautions are implemented during handling of the module.**

4.2 Soldering

4.2.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217°C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.2.2

☞ The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

4.2.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Reflow profiles are to be selected according to the following recommendations.

⚠ **Failure to observe these recommendations can result in severe damage to the device!**

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Please note that this preheat phase will not replace prior baking procedures.

• Temperature rise rate: max 3°C/s	If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.

- Time: 60 – 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200°C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of 217°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217°C liquidus temperature: 40 - 60 s
- Peak reflow temperature: 245°C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4°C / s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

⚠ **Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.**

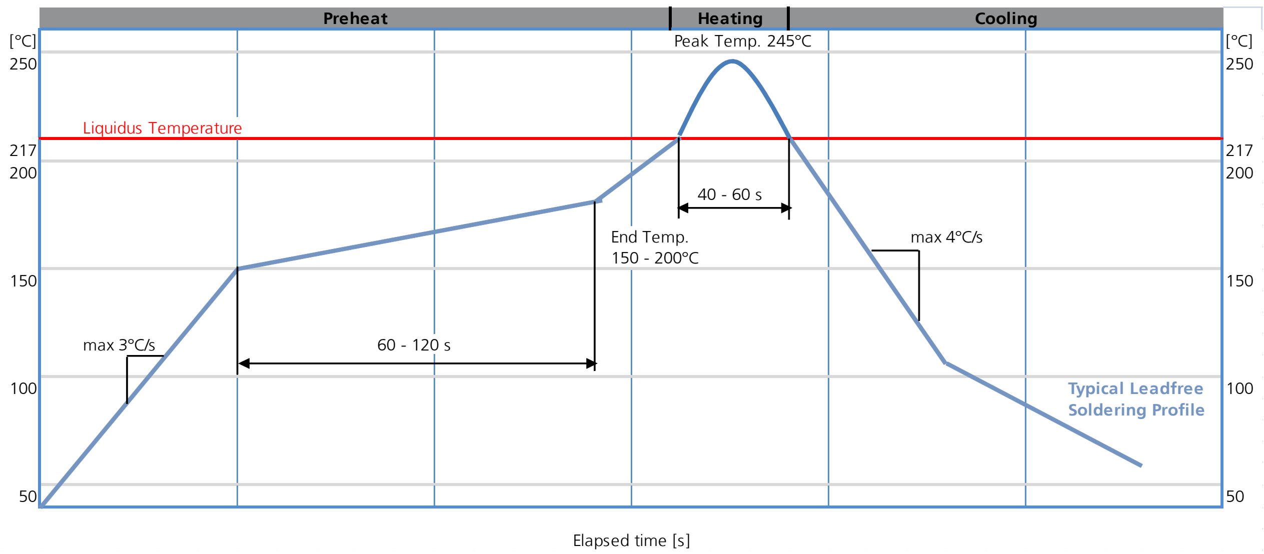


Figure 72: Recommended soldering profile

☞ LISA-U series modules must not be soldered with a damp heat process.

4.2.3 Optical inspection

After soldering the LISA-U series modules, inspect the modules optically to verify that he module is properly aligned and centered.

4.2.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

4.2.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a LISA-U series module populated on it. The reason for this is the risk of the module falling off due to high weight in relation to the adhesive properties of the solder.

4.2.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with LISA-U series modules.

4.2.7 Hand soldering

Hand soldering is not recommended.

4.2.8 Rework

The LISA-U series modules can be unsoldered from the baseboard using a hot air gun.

⚠ **Avoid overheating the module.**

After the module is removed, clean the pads before placing.

⚠ **Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.**

4.2.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the LISA-U series modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

4.2.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the LISA-U series modules before implementing this in the production.

☞ Casting will void the warranty.

4.2.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the LISA-U series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

4.2.12 Use of ultrasonic processes

LISA-U series modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the LISA-U series modules caused by any Ultrasonic Processes.

5 Product Testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (Serial interface communication, analog audio interface, real time clock, battery charger, temperature sensor, antenna detection, SIM card communication)
- Digital tests (GPIOs, digital interfaces)
- Measurement and calibration of RF characteristics in all supported bands (Receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels)
- Verification of RF characteristics after calibration (modulation accuracy, power levels and spectrum performance are checked to be within tolerances when calibration parameters are applied)

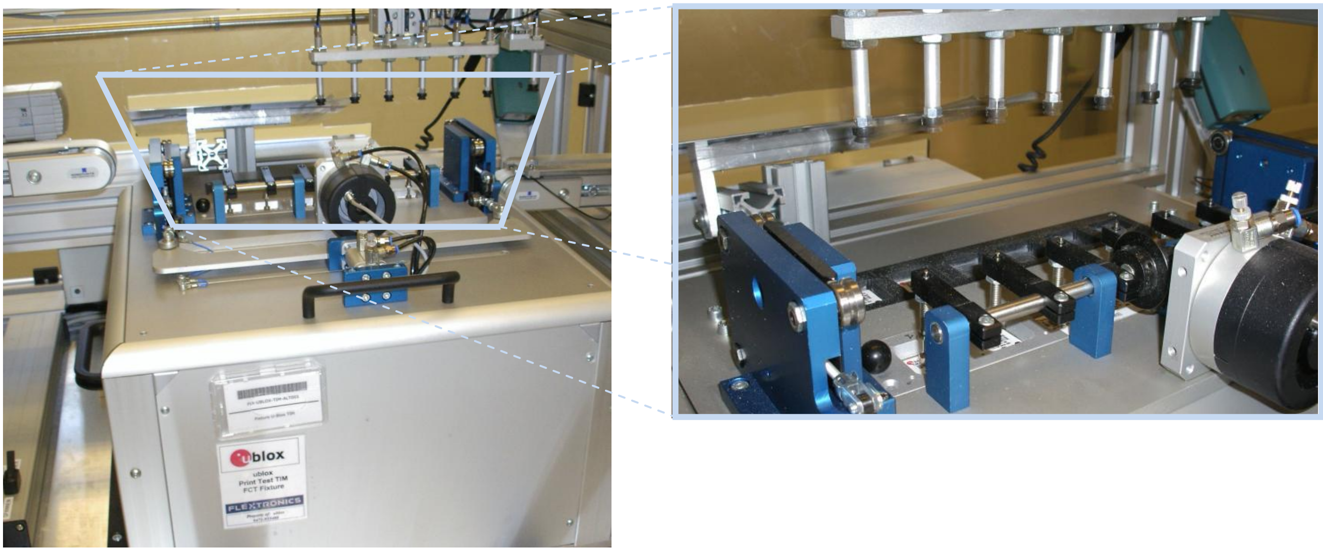


Figure 73: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer doesn’t need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damaged the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins

- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

Module AT commands are used to perform functional tests (communication with host controller, check SIM card interface, check communication between module and GPS, GPIOs, etc.) and to perform RF performance tests.

5.2.1 'Go/No go' tests for integrated devices

A 'Go/No go' test is to compare the signal quality with a "Golden Device" in a position with excellent 2G/3G network coverage and after having dialed a call (refer to u-blox AT Commands Manual [3], AT+CSQ command: <rssi>, <ber> parameters).

☞ These kinds of test may be useful as a 'go/no go' test but not for RF performance measurements.

This test is suitable to check the communication with host controller and SIM card, the audio and power supply functionality and verify if components at antenna interface are well soldered.

5.2.2 Functional tests providing RF operation

Overall RF performance test of the device including antenna can be performed with basic instruments such as a standard spectrum analyzer and signal generator using an AT interface and AT+UTEST command.

The AT+UTEST command gives a simple interface to set the module to Rx and Tx test modes ignoring 2G/3G signaling protocol. The command can set the module:

- In transmitting mode in a specified channel and power level in all supported modulation schemes (single slot GMSK, single slot 8PSK, WCDMA) and bands 2G, 3G
- In receiving mode in a specified channel to returns the measured power level in all supported bands 2G, 3G

☞ The AT+UTEST command used to perform these functional tests is available on all LISA-U series modules versions except LISA-U1xx-00.

☞ Refer to u-blox AT Commands Manual [3], for AT+UTEST command syntax description.

☞ Refer to End user test Application Note [20], for AT+UTEST command user guide, limitations and examples of use.

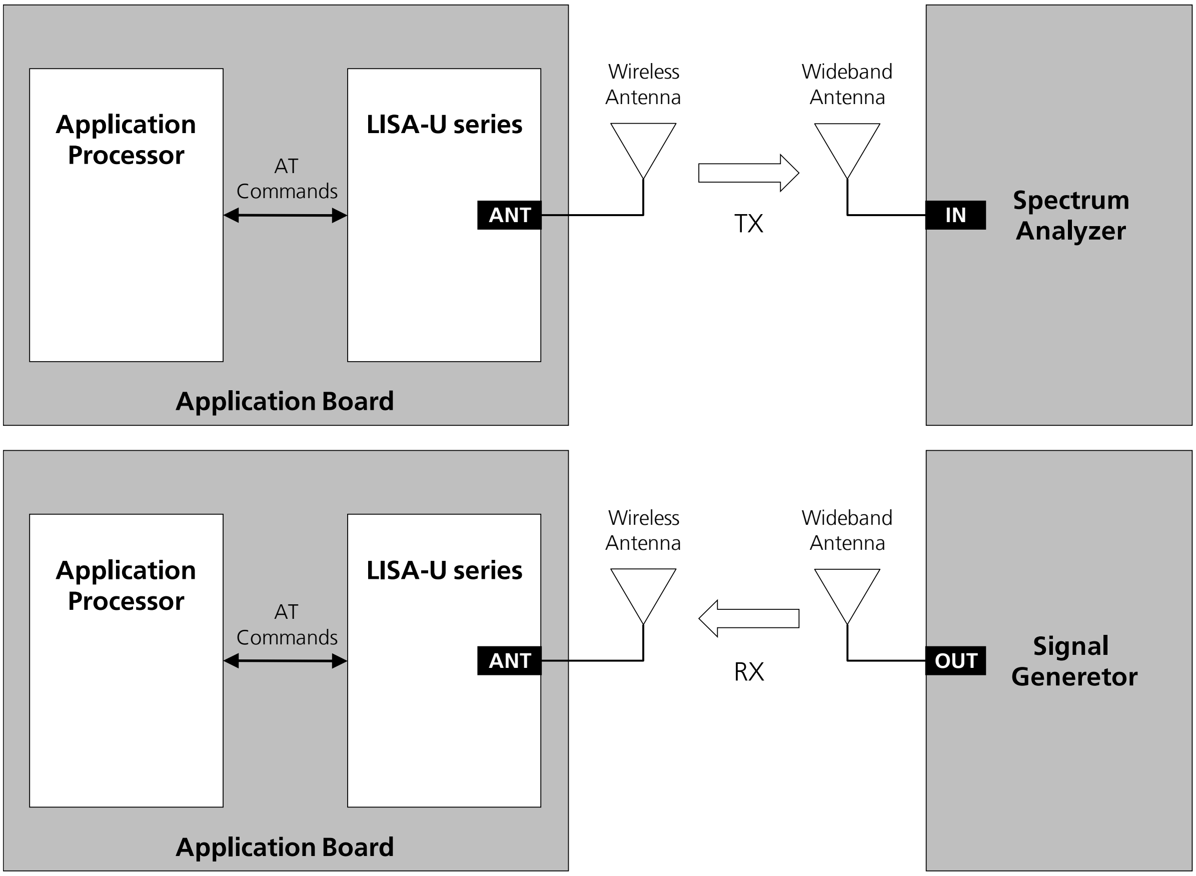


Figure 74: Setup with spectrum analyzer and signal generator for radiated measurement

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces from which depends the RF performance.

To avoid module damage during transmitter test, a proper antenna according to module specifications or a 50 Ω termination must be connected to ANT pin.

To avoid module damage during receiver test the maximum power level received at ANT pin must meet module specifications.

The AT+UTEST command sets the module to emit RF power ignoring 2G/3G signalling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purpose in controlled environments by qualified user and must not be used during the normal module operation. Follow instructions suggested in u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Example of production tests for OEM manufacturer:

1. Trigger TX GMSK burst at low Power Control Level (lower than 15) or a RX measure reporting to check:
   - If **ANT** pin is soldered
   - If **ANT** pin is in short circuit
   - If module was damaged during soldering process or during handling (ESD, mechanical shock…)
   - If antenna matching components on application board are soldered
   - If integrated antenna is correctly connected

To avoid module damage during transmitter test when good antenna termination is not guaranteed, use a low Power Control Level (i.e. PCL lower or equal to 15). u-blox assumes no responsibilities for module damaging caused by an inappropriate use of this feature.

2. Trigger TX GMSK burst at maximum PCL:
   - To check if the power supply is correctly assembled and is able to deliver the required current

3. Trigger TX GMSK and 8PSK burst and WCDMA signal:
   - To measure current consumption
   - To check if module components was damaged during soldering process or during handling (ESD, mechanical shock,…)

4. Trigger RX measurement:
   - To test receiver signal level. Assuming that there are no losses between **ANT** pin or **ANT_DIV** pin and input power source, be aware that the power level estimated by the module can vary approximately within 3GPP tolerances for the average value
   - To check if module was damaged during soldering process or during handling (ESD, mechanical shock…)

5. Trigger TX GMSK and 8PSK burst and WCDMA signal and RX measurement to check:
   - Overall RF performance of the device including antenna measuring TX and RX power levels

Appendix

A Migration to LISA-U2 series wireless modules

Migrating LISA-U1 series designs to LISA-U2 series modules is a fairly straightforward procedure. Nevertheless there are some points to be considered during the migration.

☞ Not all of the functionalities available with LISA-U1 series modules are supported by all LISA-U2 series modules versions. These include:

- Analog Audio Interfaces are not supported by all LISA-U2 series modules
- Digital Audio Interfaces are supported by all LISA-U2 series modules versions except LISA-U200-00
- Embedded AssistNow Software, GPS via Modem, Hybrid positioning and CellLocate functionalities are supported by all LISA-U2 series modules versions except LISA-U200-00
- In-Band modem is supported by all LISA-U2 series modules versions except LISA-U200-00

A.1 Checklist for migration

Have you chosen the optimal module?

☑ For HSDPA category 14, 6-band 3G, Digital Audio Interfaces support, select the LISA-U230-01 version.

☑ For HSDPA category 8, 6-band 3G, Digital Audio Interfaces support, select the LISA-U200-01 version.

☑ For HSDPA category 8, 4-band 3G support, select the LISA-U200-00 version.

Check LISA-U2 series Hardware Requirements

☑ Check the supported 3G bands for proper antenna circuit development, since LISA-U2 supports different 3G bands in comparison to LISA-U1 series wireless modules.

☑ Check audio requirements, since Analog Audio Interfaces are not supported by LISA-U2 series.

☑ Check audio requirements, since Digital Audio Interfaces are supported by all LISA-U2 series modules versions except LISA-U200-00.

☑ Check the **PWR_ON** input voltage thresholds, since they are slightly changed in comparison to LISA-U1 series modules. By the way, this is not relevant driving the **PWR_ON** input by an open drain or open collector driver as recommended.

☑ Check the **PWR_ON** behavior, since LISA-U2xx-01 can be switched off forcing **PWR_ON** pin to the low level for at least 1 s.

☑ Check the **RESET_N** input voltage thresholds, since they are slightly changed in comparison to LISA-U1 series modules. By the way, this is not relevant driving the **RESET_N** input by an open drain or open collector driver as recommended.

☑ Check the **V_BCKP** operating characteristics, since they are slightly changed in comparison to LISA-U1 series modules.

☑ Check board layout, since additional signals keep-out area must be implemented on the top layer of the application board, below LISA-U2 modules, due to GND opening on module bottom layer.

☑ Check section A.3 Hardware migration.

Check LISA-U2 series Software Requirements

- ☑ Not all of the functionalities available with LISA-U1 series modules are supported by all the LISA-U2 series modules versions. These include:
  - o Analog Audio Interfaces are not supported by all LISA-U2 series modules
  - o Digital Audio Interfaces are supported by all LISA-U2 series modules versions except LISA-U200-00
  - o Embedded AssistNow Software, GPS via Modem, Hybrid positioning and CellLocate functionalities are supported by all LISA-U2 series modules versions except LISA-U200-00
  - o In-band modem is supported by all LISA-U2 series modules versions except LISA-U200-00
- ☑ Check section A.2 Software migration.

A.2 Software migration

A.2.1 Software migration from LISA-U1 series to LISA-U2 series wireless modules

Software migration from LISA-U1 series to LISA-U2 series wireless modules is a straightforward procedure. Nevertheless there are some differences to be considered with firmware version. Like predecessors, LISA-U2 series wireless module supports AT commands according to 3GPP standards: TS 27.007 [5], TS 27.005 [6], TS 27.010 [7] and the u-blox AT command extension. Backward compatibility has been maintained as far as possible.

☞ For the complete list of supported AT commands and their syntax see u-blox AT Commands Manual [3].

A.3 Hardware migration

A.3.1 Hardware migration from LISA-U1 series to LISA-U2 series wireless modules

LISA-U2 series wireless modules have been designed with backward compatibility in mind but some minor differences were unavoidable. These minor differences will however not be relevant for the majority of the LISA-U1 series designs.

Clean and stable supply is required by LISA-U2 as by LISA-U1 series: low ripple and low voltage drop must be guaranteed at **VCC** pins. The voltage provided has to be within the normal operating range limits to allow module switch-on and has to be above the minimum limit of the extended operating range to avoid module switch-off. Consider that there are large current spikes in connected mode, when a GSM call is enabled.

LISA-U2 series provide wider **VCC** input voltage range compared to LISA-U1 series.

The **ANT** pin has 50 Ω nominal characteristic impedance and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the 2G and 3G operating bands. The recommendations of the antenna producer for correct installation and deployment (PCB layout and matching circuitry) must be followed.

The antenna and the whole RF circuit must provide optimal radiating characteristics on the entire supported bands: note that LISA-U2 supports different 3G bands in comparison to LISA-U1 series wireless modules.

LISA-U230 modules provide the RF antenna input for Rx diversity on the pin 74 (named **ANT_DIV**): it has an impedance of 50 Ω. The same pad is a reserved pin on LISA-U1 series and LISA-U200 modules.

Analog audio interfaces are not supported by LISA-U2 series modules, but a second 4-wire I^2S digital audio interface is provided instead of the 4 analog audio pins on all LISA-U2 series modules versions except LISA-U200-00. The same 4 pins can be configured as GPIO on all LISA-U2 series modules versions.

Digital audio interfaces are supported by all LISA-U2 series modules versions except LISA-U200-00: the relative pins are configured as pad disabled on LISA-U200-00 version.

PWR_ON and **RESET_N** input voltage thresholds are slightly changed in comparison to LISA-U1 series modules, but this is not relevant driving **PWR_ON** and **RESET_N** inputs by open drain / collector drivers as recommended.

LISA-U2xx-01 modules can be switched off forcing **PWR_ON** pin to the low level for at least 1 s.

V_BCKP operating characteristics are slightly changed in comparison to LISA-U1 series modules.

The 5 pins of the SPI / IPC Serial Interface can be configured as GPIOs on LISA-U2xx-01 modules.

LISA-U2 series wireless modules are SMT modules and come in the same compact form factor of LISA-U1 series, featuring Leadless Chip Carrier (LCC) packaging technology.

Additional signals keep-out area must be implemented on the top layer of the application board, below LISA-U2 modules, due to GND opening on module bottom layer.

Detailed pinout and layout comparisons between LISA-U1 series and LISA-U2 series modules, with remarks for migration, are provided in the subsections A.3.2 and A.3.3.

For more information regarding LISA-U1 and LISA-U2 series modules electrical characteristics refer to LISA-U1 series Data Sheet [1] and LISA-U2 series Data Sheet [2].

A.3.2 Pin-out comparison LISA-U1 series vs. LISA-U2 series

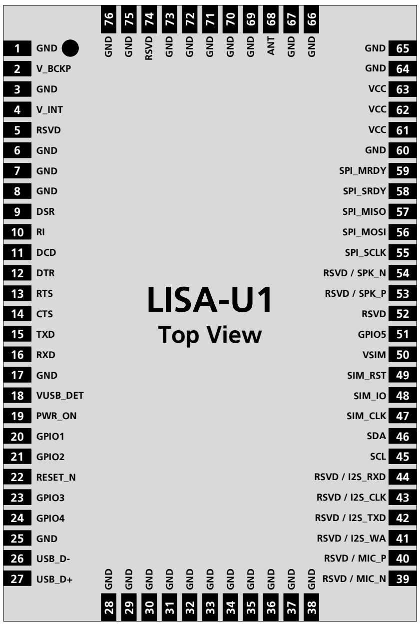


Figure 75: LISA-U1 series pin assignment

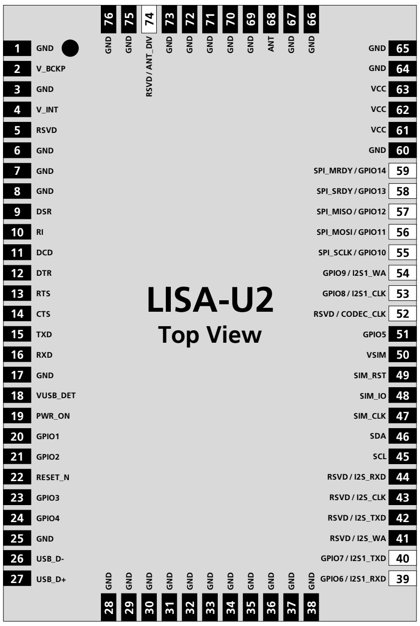


Figure 76: LISA-U2 series pin assignment (highlighted name/function changes)

No	LISA-U1 Name	Description	LISA-U2 Name	Description	Remarks for Migration
1	GND	Ground	GND	Ground	
2	V_BCKP	RTC supply input/output	V_BCKP	RTC supply input/output	V_BCKP operating characteristics difference: • LISA-U1: o V_BCKP output = 2.3V typ. o V_BCKP input = 1.0V min / 2.5V max • LISA-U2: o V_BCKP output = 1.8V typ. o V_BCKP input = 1.0V min / 1.9V max
3	GND	Ground	GND	Ground	
4	V_INT	Digital Interfaces supply output	V_INT	Digital Interfaces supply output	No difference: V_INT output = 1.8V typ.
5	RSVD	RESERVED pin	RSVD	RESERVED pin	No difference: This pin must be connected to GND
6	GND	Ground	GND	Ground	
7	GND	Ground	GND	Ground	
8	GND	Ground	GND	Ground	
9	DSR	UART data set ready output	DSR	UART data set ready output	No difference: Circuit 107 (DSR) in ITU-T V.24.
10	RI	UART ring indicator output	RI	UART ring indicator output	No difference: Circuit 125 (RI) in ITU-T V.24.
11	DCD	UART data carrier detect output	DCD	UART data carrier detect output	No difference: Circuit 109 (DCD) in ITU-T V.24.
12	DTR	UART data terminal ready input	DTR	UART data terminal ready input	No difference: Circuit 108/2 (DTR) in ITU-T V. 24.
13	RTS	UART ready to send input	RTS	UART ready to send input	No difference: Circuit 105 (RTS) in ITU-T V.24.
14	CTS	UART clear to send output	CTS	UART clear to send output	No difference: Circuit 106 (CTS) in ITU-T V.24.
15	TXD	UART transmitted data input	TXD	UART transmitted data input	No difference: Circuit 103 (TxD) in ITU-T V.24.
16	RXD	UART received data output	RXD	UART received data output	No difference: Circuit 104 (RxD) in ITU-T V.24.
17	GND	Ground	GND	Ground	
18	VUSB_DET	USB detect input	VUSB_DET	USB detect input	No difference: Input for VBUS (5V typical) USB supply sense.
19	PWR_ON	Power-on input	PWR_ON	Power-on input	Forcing PWR_ON to the low level for at least 5 ms causes a switch-on of LISA-U1 and LISA-U2. PWR_ON operating voltage difference: • LISA-U1: o L-level input = -0.30V min / 0.65V max o H-level input = 2.00 min / 4.20V max o External pull-up (e.g. to V_BCKP) required • LISA-U2: o L-level input = -0.30V min / 0.65V max o H-level input = 1.50V min / 4.40V max o External pull-up (e.g. to V_BCKP) required Additional feature provided by LISA-U2: LISA-U2xx-01 can be switched-off forcing PWR_ON pin to the low level for at least 1 s.
20	GPIO1	GPIO	GPIO1	GPIO	By default, the pin is configured as Pad disabled, and can be alternatively configured to provide the GSM Tx Burst Indication, Network Status Indication or as GPIO Additional features provided by LISA-U2xx-01: the pin can be alternatively configured to provide Module Status Indication

No	LISA-U1 Name	Description	LISA-U2 Name	Description	Remarks for Migration
21	GPIO2	GPIO	GPIO2	GPIO	No difference from LISA-U1xx-0x to LISA-U2xx-01: By default, the pin is configured to provide the GPS Supply Enable function, and can be alternatively configured as GPIO Different configuration on LISA-U200-00: By default, the pin is configured as Pad disabled, and can be alternatively configured as GPIO
22	RESET_N	External reset input	RESET_N	External reset input	Forcing RESET_N to the low level for at least 50 ms causes a hardware reset of LISA-U1 and LISA-U2. RESET_N operating voltage difference: • LISA-U1: o L-level input = -0.30V min / 0.65V max o H-level input = 1.69V min / 2.48V max o Internal 10kΩ pull-up to V_BCKP (2.3V typ) • LISA-U2: o L-level input = -0.30V min / 0.51V max o H-level input = 1.32V min / 2.01V max o Internal 10kΩ pull-up to V_BCKP (1.8V typ)
23	GPIO3	GPIO	GPIO3	GPIO	No difference from LISA-U1xx-00 to LISA-U2xx-00: By default, the pin is configured as Pad disabled, and can be alternatively configured as GPIO No difference from LISA-U1xx-01 to LISA-U2xx-01: By default, the pin is configured to provide the GPS Tx Data Ready function, and can be alternatively configured as GPIO.
24	GPIO4	GPIO	GPIO4	GPIO	No difference from LISA-U1xx-00 to LISA-U2xx-00: By default, the pin is configured as Pad disabled, and can be alternatively configured as GPIO No difference from LISA-U1xx-01 to LISA-U2xx-01: By default, the pin is configured to provide the GPS RTC sharing (time aiding) function, and can be alternatively configured as GPIO.
25	GND	Ground	GND	Ground	
26	USB_D-	USB Data Line D- input/output	USB_D-	USB Data Line D- input/output	No difference: 90 Ω nominal differential impedance. Pull-up/down & series resistors provided internally.
27	USB_D+	USB Data Line D+ input/output	USB_D+	USB Data Line D+ input/output	No difference: 90 Ω nominal differential impedance. Pull-up/down & series resistors provided internally.
28	GND	Ground	GND	Ground	
29	GND	Ground	GND	Ground	
30	GND	Ground	GND	Ground	
31	GND	Ground	GND	Ground	
32	GND	Ground	GND	Ground	
33	GND	Ground	GND	Ground	
34	GND	Ground	GND	Ground	
35	GND	Ground	GND	Ground	
36	GND	Ground	GND	Ground	
37	GND	Ground	GND	Ground	
38	GND	Ground	GND	Ground	
39	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	GPIO6	LISA-U200-00: GPIO	New feature provided by LISA-U2: By default, the pin is configured as Pad disabled, and can be alternatively configured as GPIO
	MIC_N	LISA-U120-0x, LISA-U130-0x: Differential analog audio input (neg.)	I2S1_RXD / GPIO6	LISA-U200-01, LISA-U230-01: 2^{nd} I^2S receive data input / GPIO	Different features provided by LISA-U2: By default, the pin is configured as receive data input of the second digital audio interface, and can be alternatively configured as GPIO

No	LISA-U1 Name	LISA-U1 Description	LISA-U2 Name	LISA-U2 Description	Remarks for Migration
40	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	GPIO7	LISA-U200-00: GPIO	New feature provided by LISA-U2: By default, the pin is configured as Pad disabled, and can be alternatively configured as GPIO
	MIC_P	LISA-U120-0x, LISA-U130-0x: Differential analog audio input (pos.)	I2S1_TXD / GPIO7	LISA-U200-01, LISA-U230-01: 2nd I^2S transmit data output / GPIO	Different features provided by LISA-U2: By default, the pin is configured as transmit data output of the second digital audio interface, and can be alternatively configured as GPIO
41	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	RSVD	LISA-U200-00: RESERVED pin	No difference: Pad disabled on LISA-U200-00.
	I2S_WA	LISA-U120-0x, LISA-U130-0x: I^2S word alignment	I2S_WA	LISA-U200-01, LISA-U230-01: 1st I^2S word alignment input/output	No difference: I^2S word alignment input/output
42	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	RSVD	LISA-U200-00: RESERVED pin	No difference: Pad disabled on LISA-U200-00.
	I2S_TXD	LISA-U120-0x, LISA-U130-0x: I^2S transmit data output	I2S_TXD	LISA-U200-01, LISA-U230-01: 1st I^2S transmit data output	No difference: I^2S transmit data output
43	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	RSVD	LISA-U200-00: RESERVED pin	No difference: Pad disabled on LISA-U200-00.
	I2S_CLK	LISA-U120-0x, LISA-U130-0x: I^2S clock	I2S_CLK	LISA-U200-01, LISA-U230-01: 1st I^2S clock input/output	No difference: I^2S clock input/output
44	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	RSVD	LISA-U200-00: RESERVED pin	No difference: Pad disabled on LISA-U200-00.
	I2S_RXD	LISA-U120-0x, LISA-U130-0x: I^2S receive data input	I2S_RXD	LISA-U200-01, LISA-U230-01: 1st I^2S receive data input	No difference: I^2S receive data input
45	SCL	I^2C bus clock line output	SCL	I^2C bus clock line output	No difference: Fixed open drain. External pull-up resistor (e.g. to V_INT) required
46	SDA	I^2C bus data line input/output	SDA	I^2C bus data line input/output	No difference: Fixed open drain. External pull-up resistor (e.g. to V_INT) required
47	SIM_CLK	SIM clock output	SIM_CLK	SIM clock output	No difference: 3.25 MHz clock frequency for SIM card
48	SIM_IO	SIM data input/output	SIM_IO	SIM data input/output	No difference: Internal 4.7 kΩ pull-up resistor to VSIM.
49	SIM_RST	SIM reset output	SIM_RST	SIM reset output	No difference: Reset output for SIM card
50	VSIM	SIM supply output	VSIM	SIM supply output	No difference: VSIM output = 1.80 V typ or 2.90 V typ
51	GPIO5	GPIO	GPIO5	GPIO	By default, the pin is configured to provide the SIM card presence detection function. Additional features provided by LISA-U2xx-01: The pin can be alternatively configured to provide Module Operating Mode Indication

	LISA-U1		LISA-U2		
No	**Name**	**Description**	**Name**	**Description**	**Remarks for Migration**
52	RSVD	RESERVED pin	RSVD	LISA-U200-00: RESERVED pin	No difference: Pad disabled on LISA-U200-00.
			CODEC_CLK	LISA-U200-01, LISA-U230-01: Clock output	New feature provided by LISA-U2: Digital clock output for external audio codec
53	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	GPIO8	LISA-U200-00: GPIO	New feature provided by LISA-U2: By default, the pin is configured as Pad disabled, and can be alternatively configured as GPIO
	SPK_P	LISA-U120-0x, LISA-U130-0x: Differential analog audio output (pos.)	I2S1_CLK / GPIO8	LISA-U200-01, LISA-U230-01: 2nd I²S clock input/output / GPIO	Different features provided by LISA-U2: By default, the pin is configured as clock input/output of the second digital audio interface, and can be alternatively configured as GPIO
54	RSVD	LISA-U100-0x, LISA-U110-0x: RESERVED pin	GPIO9	LISA-U200-00: GPIO	New feature provided by LISA-U2: By default, the pin is configured as Pad disabled, and can be alternatively configured as GPIO
	SPK_N	LISA-U120-0x, LISA-U130-0x: Differential analog audio output (neg.)	I2S1_WA / GPIO9	LISA-U200-01, LISA-U230-01: 2nd I²S word alignment input/output / GPIO	Different features provided by LISA-U2: By default, the pin is configured as word alignment input/output of the second digital audio interface, and can be alternatively configured as GPIO
55	SPI_SCLK	SPI Serial Clock Input	SPI_SCLK / GPIO10	SPI Serial Clock Input / GPIO	SPI / IPC Clock Input (CPOL=0, internal pull-down) by default on LISA-U1 and LISA-U2 Additional features provided by LISA-U2xx-01: The pin can be alternatively configured as GPIO
56	SPI_MOSI	SPI Data Line Input	SPI_MOSI / GPIO11	SPI Data Line Input / GPIO	SPI / IPC Data Line Input, (CPHA=1, internal pull-up) by default on LISA-U1 and LISA-U2. Additional features provided by LISA-U2xx-01: The pin can be alternatively configured as GPIO
57	SPI_MISO	SPI Data Line Output	SPI_MISO / GPIO12	SPI Data Line Output / GPIO	SPI / IPC Data Line Output (CPHA=1, idle high) by default on LISA-U1 and LISA-U2. Additional features provided by LISA-U2xx-01: The pin can be alternatively configured as GPIO
58	SPI_SRDY	SPI Slave Ready Output	SPI_SRDY / GPIO13	SPI Slave Ready Output / GPIO	SPI / IPC Slave Ready Output (idle low) by default on LISA-U1 and LISA-U2 Additional features provided by LISA-U2xx-01: The pin can be alternatively configured to provide Module Status Indication or as GPIO
59	SPI_MRDY	SPI Master Ready Input	SPI_MRDY / GPIO14	SPI Master Ready Input / GPIO	SPI / IPC Master Ready Input (Internal pull-down, Idle low) by default on LISA-U1 and LISA-U2. Additional features provided by LISA-U2xx-01: The pin can be alternatively configured to provide Module Operating Mode Indication or as GPIO
60	GND	Ground	GND	Ground	
61	VCC	Module supply input	VCC	Module supply input	VCC operating voltage difference: • LISA-U1: o VCC normal range = 3.4 V min / 4.2 V max o VCC extended range = 3.1 V min / 4.2 V max • LISA-U2: o VCC normal range = 3.3 V min / 4.4 V max o VCC extended range = 3.1 V min / 4.5 V max
62	VCC	Module supply input	VCC	Module supply input	VCC operating voltage difference: • LISA-U1: o VCC normal range = 3.4 V min / 4.2 V max o VCC extended range = 3.1 V min / 4.2 V max • LISA-U2: o VCC normal range = 3.3 V min / 4.4 V max o VCC extended range = 3.1 V min / 4.5 V max

	LISA-U1		LISA-U2		
No	**Name**	**Description**	**Name**	**Description**	**Remarks for Migration**
63	VCC	Module supply input	VCC	Module supply input	VCC operating voltage difference: • LISA-U1: o VCC normal range = 3.4 V min / 4.2 V max o VCC extended range = 3.1 V min / 4.2 V max • LISA-U2: o VCC normal range = 3.3 V min / 4.4 V max o VCC extended range = 3.1 V min / 4.5 V max
64	GND	Ground	GND	Ground	
65	GND	Ground	GND	Ground	
66	GND	Ground	GND	Ground	
67	GND	Ground	GND	Ground	
68	ANT	RF antenna	ANT	RF input/output for main Tx/Rx antenna	RF antenna input/output 50 Ω nominal impedance 3G band support difference: • LISA-U100/U120: o Band II (1900), Band V (850) • LISA-U110/U130: o Band I (2100), Band VIII (900) • LISA-U200: o Band I (2100), Band II (1900), Band V (850), Band VI (800) • LISA-U230: o Band I (2100), Band II (1900), Band IV (1700), Band V (850), Band VI (800), Band VIII (900)
69	GND	Ground	GND	Ground	
70	GND	Ground	GND	Ground	
71	GND	Ground	GND	Ground	
72	GND	Ground	GND	Ground	
73	GND	Ground	GND	Ground	
74	RSVD	RESERVED pin	RSVD	LISA-U200-0x: RESERVED pin	No difference: Leave unconnected.
			ANT_DIV	LISA-U230-01: RF input for Rx diversity antenna	New feature provided by LISA-U2: RF antenna input for Rx diversity 50 Ω nominal impedance
75	GND	Ground	GND	Ground	
76	GND	Ground	GND	Ground	

Table 51: Pinout comparison LISA-U1 series vs. LISA-U2 series

A.3.3 Layout comparison LISA-U1 series vs. LISA-U2 series

Additional signals keep-out area must be implemented on the top layer of the application board, below LISA-U2 modules, due to GND opening on module bottom layer, as described in Figure 77 and Figure 78.

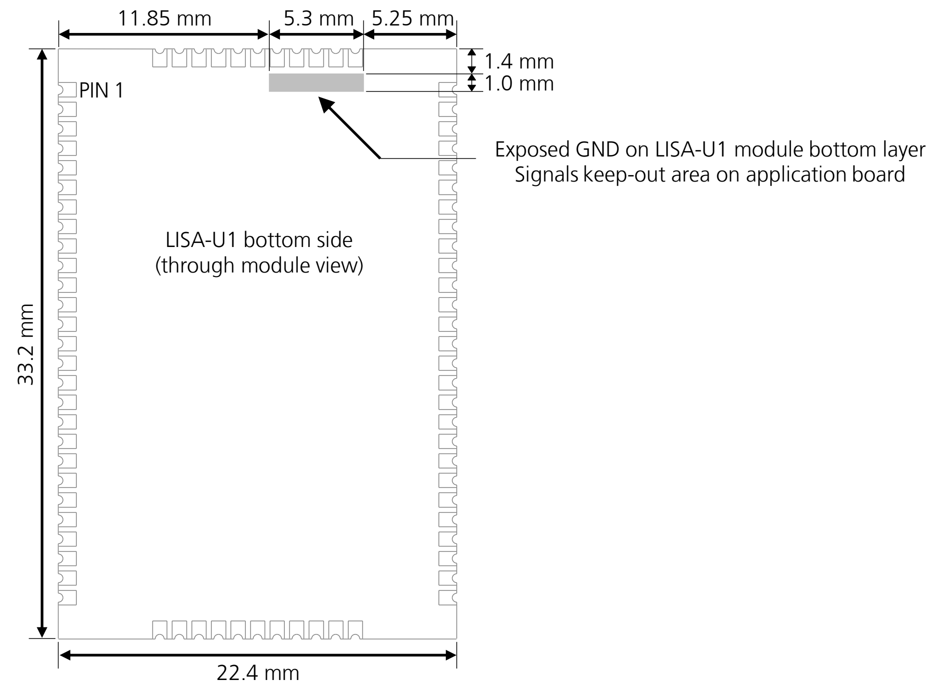


Figure 77: Signals keep-out area on the top layer of the application board, below LISA-U1 series modules

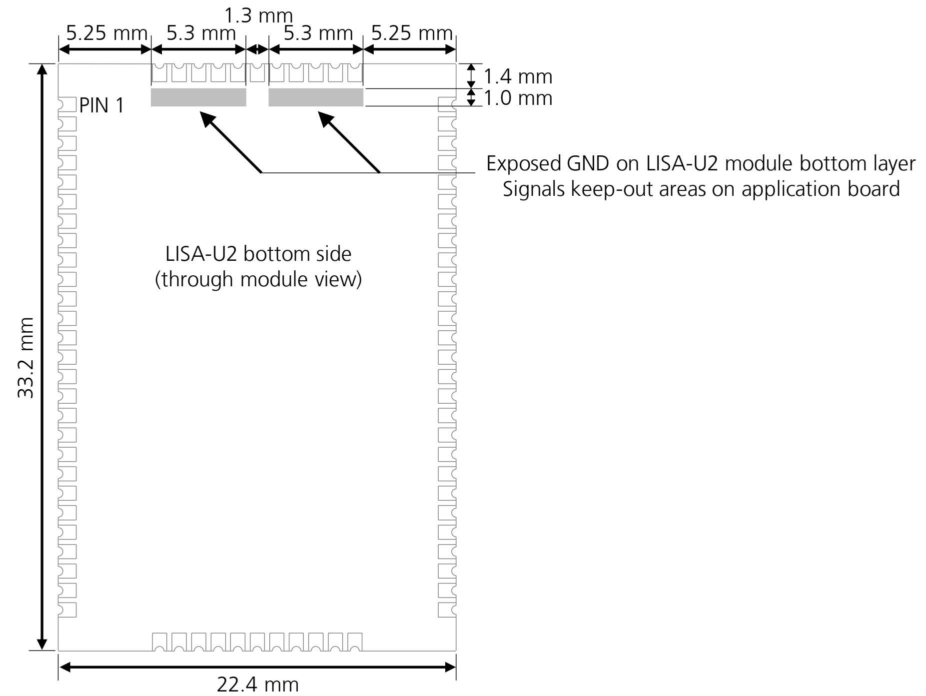


Figure 78: Signals keep-out areas on the top layer of the application board, below LISA-U2 series modules

B Glossary

ADC	Analog to Digital Converter
AP	Application Processor
AT	AT Command Interpreter Software Subsystem, or attention
CBCH	Cell Broadcast Channel
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DDC	Display Data Channel
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTM	Dual Transfer Mode
DTR	Data Terminal Ready
EBU	External Bus Interface Unit
EDGE	Enhanced Data rates for GSM Evolution
E-GPRS	Enhanced GPRS
FDD	Frequency Division Duplex
FEM	Front End Module
FOAT	Firmware Over AT commands
FTP	File Transfer Protocol
FTPS	FTP Secure
GND	Ground
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HF	Hands-free
HSDPA	High Speed Downlink Packet Access
HTTP	HyperText Transfer Protocol
HTTPS	Hypertext Transfer Protocol over Secure Socket Layer
HW	Hardware
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit
I^2S	Inter IC Sound
IP	Internet Protocol
IPC	Inter Processor Communication

LNA	Low Noise Amplifier
MCS	Modulation Coding Scheme
NOM	Network Operating Mode
PA	Power Amplifier
PBCCH	Packet Broadcast Control Channel
PCM	Pulse Code Modulation
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
RF	Radio Frequency
RI	Ring Indicator
RTC	Real Time Clock
RTS	Request To Send
RXD	RX Data
SAW	Surface Acoustic Wave
SIM	Subscriber Identification Module
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SPI	Serial Peripheral Interface
SRAM	Static RAM
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TXD	TX Data
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
UTRA	UMTS Terrestrial Radio Access
VC-TCXO	Voltage Controlled - Temperature Compensated Crystal Oscillator
WCDMA	Wideband CODE Division Multiple Access

Related documents

[1] u-blox LISA-U1 series Data Sheet, Docu No 3G.G1-HW-10001

[2] u-blox LISA-U2 series Data Sheet, Docu No 3G.G1-HW-11004

[3] u-blox AT Commands Manual, Docu No WLS-SW-11000

[4] ITU-T Recommendation V.24, 02-2000. List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en

[5] 3GPP TS 27.007 - AT command set for User Equipment (UE) (Release 1999)

[6] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)

[7] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)

[8] Universal Serial Bus Revision 2.0 specification, http://www.usb.org/developers/docs/

[9] I2C-Bus Specification Version 2.1 Philips Semiconductors (January 2000), http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf

[10] CENELEC EN 61000-4-2 (2001): "Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test".

[11] ETSI EN 301 489-1 V1.8.1: "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements"

[12] ETSI EN 301 489-7 V1.3.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 7: Specific conditions for mobile and portable radio and ancillary equipment of digital cellular radio telecommunications systems (GSM and DCS)"

[13] ETSI EN 301 489-24 V1.4.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment"

[14] 3GPP TS 26.267 - Technical Specification Group Services and System Aspects; eCall Data Transfer; In-band modem solution; General description (Release 9)

[15] GSM Mux Implementation Application Note, Docu No WLS-CS-11002

[16] GPS Implementation Application Note, Docu No GSM.G1-CS-09007

[17] Firmware Update Application Note, Docu No WLS-CS-11001

[18] SPI Interface application Note, Docu No 3G.G2-CS-11000

[19] 3GPP TS 23.060 - Technical Specification Group Services and System Aspects; General Packet Radio Service (GPRS); Service description

[20] End user test Application Note, Docu No TBD

[21] u-blox Package Information Guide, Docu. No GPS-X-11004

Some of the above documents can be downloaded from u-blox web-site (http://www.u-blox.com).

Revision history

Revision	Date	Name	Status / Comments
-	21/10/2010	sses	Initial Release
1	11/01/2011	sses	Thickness information added GPIO description improved
2	26/04/2011	lpah	Update to Advance Information status
3	07/07/2011	lpah	Update to Preliminary status
A	26/10/2011	sses	Changed status to Objective Specification Initial release for LISA-U series From LISA-U1xx-00 system integration manual, added description and integration of LISA-U1xx-01, LISA-U200-00, LISA-U2xx-01 Added notes regarding VCC normal and extended operating ranges Added RTC value reliability as function of V_BCKP voltage value Added recommendation regarding any external signal connected to the UART interface, SPI/IPC interface, I2S interfaces and GPIOs when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence: must be tri-stated to avoid latch-up of circuits and let a proper boot of the module.
A1	22/11/2011	sses	Update to Advance Information status Updated module behavior during power-off sequence. Added LISA-U200-00 ESD application circuit for antenna port. Added application circuit for the module status indication function.
A2	02/02/2012	sses	Update to Preliminary status Updated Federal Communications Commission notice Updated LISA-U2 features in module power off and GPIO sections

Contact

For complete contact information visit us at www.u-blox.com

u-blox Offices

North, Central and South America

u-blox America, Inc.

Phone: +1 (703) 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:

Phone: +1 (703) 483 3184
E-mail: info_us@u-blox.com

Technical Support:

Phone: +1 (703) 483 3185
E-mail: support_us@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG

Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support @u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.

Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office China:

Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office Japan:

Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:

Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:

Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com