LISA-U2 series

3.75G HSPA / HSPA+ Cellular Modules

System Integration Manual

Abstract

This document describes the features and the system integration of LISA-U2 series HSPA+ cellular modules. These modules are complete and cost efficient 3.75G solutions offering up to six-band HSDPA/HSUPA and quad-band GSM/EGPRS voice and/or data transmission technology in a compact form factor.

www.u-blox.com

UBX-13001118 - R25

Document Information

Title	**LISA-U2 series**
Subtitle	3.75G HSPA / HSPA+ Cellular Modules
Document type	System Integration Manual
Document number	UBX-13001118
Revision and date	R25 10-Apr-2019
Disclosure Restriction	

This document applies to the following products:

Product name	Type number	Modem version	Application version	PCN reference	Product status
LISA-U200	LISA-U200-01S-00	22.40		UBX-TN-12040	Obsolete
	LISA-U200-01S-01	22.40	A01.00		End of Life
	LISA-U200-01S-02	22.40	A01.02	UBX-17048820	End of Life
	LISA-U200-01S-03	22.40	A01.03	UBX-18055867	Mass Production
	LISA-U200-02S-01	22.90	A01.01	UBX-14005768	End of Life
	LISA-U200-02S-02	22.90	A01.03	UBX-17048820	End of Life
	LISA-U200-03S-00	23.41	A01.01	UBX-15020745	Obsolete
	LISA-U200-03S-01	23.41	A01.04	UBX-17048820	End of Life
	LISA-U200-03S-02	23.41	A01.05	UBX-18055867	Mass Production
	LISA-U200-52S-01	22.86	A01.01	UBX-14005768	Obsolete
	LISA-U200-52S-02	22.86	A01.03	UBX-17048820	End of Life
	LISA-U200-52S-03	22.86	A01.04	UBX-18055867	Mass Production
	LISA-U200-62S-01	22.90	A01.01	UBX-14005768	Obsolete
	LISA-U200-62S-02	22.90	A01.02	UBX-16017712	End of Life
	LISA-U200-62S-03	22.90	A01.03	UBX-17048820	End of Life
	LISA-U200-62S-04	22.90	A01.04	UBX-18055867	Mass Production
LISA-U200 FOTA	LISA-U200-83S-00	23.41	A01.01	UBX-15020745	End of Life
LISA-U201	LISA-U201-03S-00	23.41	A01.01	UBX-15020745	End of Life
	LISA-U201-03S-01	23.41	A01.04	UBX-17048820	Mass Production
	LISA-U201-03A-00	23.41	A01.01	UBX-16010501	End of Life
	LISA-U201-03A-01	23.41	A01.02	UBX-17010533	End of Life
	LISA-U201-03A-02	23.41	A01.04	UBX-17046899	Mass Production
LISA-U201 FOTA	LISA-U201-83S-00	23.41	A01.02	UBX-16004570	Obsolete
	LISA-U201-83S-01	23.41	A01.04	UBX-17048820	Mass Production
LISA-U230	LISA-U230-01S-01	22.40		UBX-TN-12040	Obsolete
	LISA-U230-01S-02	22.40	A01.02	UBX-17048820	End of Life
	LISA-U230-01S-03	22.40	A01.03	UBX-18055867	Mass Production
LISA-U260	LISA-U260-01S-02	22.61		UBX-TN-12061	Obsolete
	LISA-U260-01S-03	22.61	A01.05	UBX-17048820	End of Life
	LISA-U260-02S-02	22.90	A01.02	UBX-14042086	End of Life
	LISA-U260-02S-03	22.90	A01.04	UBX-17048820	End of Life

Product name	Type number	Modem version	Application version	PCN reference	Product status
LISA-U270	LISA-U270-01S-02	22.61	A01.02	UBX-14042086	Obsolete
	LISA-U270-02S-02	22.90	A01.02	UBX-14042086	End of Life
	LISA-U270-02S-03	22.90	A01.04	UBX-17048820	End of Life
	LISA-U270-62S-04	22.93	A01.02	UBX-14042086	Obsolete
	LISA-U270-62S-05	22.93	A01.04	UBX-15029938	Obsolete
	LISA-U270-62S-06	22.93	A01.05	UBX-16009934	Obsolete
	LISA-U270-62S-07	22.93	A01.07	UBX-17048820	End of Life
	LISA-U270-63S-00	22.93	A01.06	UBX-16010383	Obsolete
	LISA-U270-63S-01	22.93	A01.07	UBX-17048820	End of Life
	LISA-U270-63S-02	22.93	A01.08	UBX-18055867	Mass Production
	LISA-U270-68S-00	22.93	A01.03	UBX-15019240	Obsolete
	LISA-U270-68S-01	22.93	A01.07	UBX-17048820	End of Life

Contents

1 System description

1.1 Overview

LISA-U2 cellular modules integrate full-feature 3G UMTS/HSxPA and 2G GSM/GPRS/EDGE protocol stack with Assisted GPS support. These SMT modules come in the compact LISA form factor, featuring Leadless Chip Carrier (LCC) packaging technology.

3G UMTS/HSDPA/HSUPA Characteristics	2G GSM/GPRS/EDGE Characteristics
Class A User Equipment[1]	Class B Mobile Station[2]
UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) 3GPP Release 7 (HSPA+) Rx Diversity for LISA-U230	GSM EDGE Radio Access (GERA) 3GPP Release 7 Rx Diversity for LISA-U230
2-band support for LISA-U260: • Band II (1900 MHz), Band V (850 MHz) 2-band support for LISA-U270: • Band I (2100 MHz), Band VIII (900 MHz) 5-band support for LISA-U201: • Band I (2100 MHz), Band II (1900 MHz), Band V (850 MHz), Band VI (800 MHz), Band VIII (900 MHz) 6-band support for LISA-U200 and LISA-U230: • Band I (2100 MHz), Band II (1900 MHz), Band IV (1700 MHz), Band V (850 MHz), Band VI (800 MHz), Band VIII (900 MHz)	4-band support • GSM 850 MHz, E-GSM 900 MHz, DCS 1800 MHz, PCS 1900 MHz
WCDMA/HSDPA/HSUPA Power Class • Power Class 3 (24 dBm) for WCDMA/HSDPA/HSUPA mode	GSM/GPRS Power Class • Power Class 4 (33 dBm) for GSM/E-GSM bands • Power Class 1 (30 dBm) for DCS/PCS bands EDGE Power Class • Power Class E2 (27 dBm) for GSM/E-GSM bands • Power Class E2 (26 dBm) for DCS/PCS bands
PS (Packet Switched) Data Rate • HSUPA category 6, up to 5.76 Mbit/s UL • HSDPA category 8 up to 7.2 Mbit/s DL for LISA-U200, LISA-U201, LISA-U260 and LISA-U270 • HSDPA category 14 up to 21.1 Mbit/s DL for LISA-U230 • WCDMA PS data up to 384 kbit/s DL/UL	PS (Packet Switched) Data Rate • GPRS multislot class 12[3], coding scheme CS1-CS4, up to 85.6 kbit/s DL/UL • EDGE multislot class 12[3], coding scheme MCS1-MCS9, up to 236.8 kbit/s DL/UL
CS (Circuit Switched) Data Rate • WCDMA CS data up to 64 kbit/s DL/UL	CS (Circuit Switched) Data Rate • GSM CS data up to 9.6 kbit/s DL/UL supported in transparent/non transparent mode

Table 1: LISA-U2 series UMTS/HSDPA/HSUPA and GSM/GPRS/EDGE characteristics

Operation modes I to III are supported on GSM/GPRS networks, while allowing users to define their preferred service from GSM to GPRS. Paging messages for GSM calls may be monitored (optional) during GPRS data transfer in non-coordinating NOM II-III.

[1] Device can work simultaneously in Packet Switch and Circuit Switch mode: voice calls are possible while the data connection is active without any interruption in service.
[2] Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for example during data transmission an incoming call occurs, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.
[3] GPRS/EDGE multislot class 12 implies maximum of 4 slots in DL (reception), 4 slots in UL (transmission) with 5 slots in total

3G Transmission and Receiving: LISA-U2 modules implement 3G High-Speed Uplink Packet Access (HSUPA) category 6. LISA-U200, LISA-U201, LISA-U260 and LISA-U270 modules implement 3G High Speed Downlink Packet Access (HSDPA) category 8. LISA-U230 modules implement the 3G HSDPA category 14. The HSUPA and HSDPA categories determine the maximum speed at which data can be respectively transmitted and received. Higher categories allow faster data transfer rates, as indicated in Table 1.

The 3G network automatically performs adaptive coding and modulation using a choice of forward error correction code rate and choice of modulation type, to achieve the highest possible data rate and data transmission robustness according to the quality of the radio channel.

2G Transmission and Receiving: LISA-U2 series modules implement GPRS/EGPRS multislot class 12. GPRS and EGPRS multislot classes determine the maximum number of timeslots available for upload and download and thus the speed at which data can be transmitted and received. Higher classes typically allow faster data transfer rates, as indicated in Table 1.

The 2G network automatically configures the number of timeslots used for reception or transmission (voice calls take precedence over GPRS/EGPRS traffic) and channel encoding (from Coding Scheme 1 up to Modulation and Coding Scheme 9), performing link adaptation to achieve the highest possible data rate. Table 2 summarizes the interfaces and features provided by LISA-U2 modules.

Model	UMTS		Bands		Interfaces					Audio		Functions												Grade		
	HSUPA [Mbit/s]	HSDPA [Mbit/s]	UMTS/HSPA [MHz]	GSM/GPRS/EDGE quad-band	UART	SPI	USB	DDC (I²C)	GPIO	Analog audio	Digital audio	Network indication	Antenna detection	Jamming detection	Embedded TCP/UDP	Embedded FTP, HTTP	Embedded SSL/TLS	AssistNow software	CellLocate®	FOTA	FW update via serial	eCall / ERA-GLONASS	Rx diversity	GNSS via Modem	Standard	Professional	Automotive
LISA-U200	5.76	7.2	800/850/900 1700/1900/2100	•	1	1	1	1	14		2	•	•	•	•	•	•	•	•		•	•[4]		•		•	
LISA-U200 FOTA	5.76	7.2	800/850/900 1700/1900/2100	•	1	1	1	1	14		2	•	•	•	•	•	•	•	•	•	•	•		•		•	
LISA-U201	5.76	7.2	800/850/900 1900/2100	•	1	1	1	1	14		2	•	•	•	•	•	•	•	•		•	•		•		•	
LISA-U201 FOTA	5.76	7.2	800/850/900 1900/2100	•	1	1	1	1	14		2	•	•	•	•	•	•	•	•	•	•	•		•		•	
LISA-U230	5.76	21.1	800/850/900 1700/1900/2100	•	1	1	1	1	14		2	•	•	•	•	•	•	•	•		•		•	•		•	
LISA-U260	5.76	7.2	850/1900	•	1	1	1	1	14		2	•	•	•	•	•	•	•	•		•	•[4]		•		•	
LISA-U270	5.76	7.2	900/2100	•	1	1	1	1	14		2	•	•	•	•	•	•	•	•		•	•[4]		•		•	

LISA-U200-52S module product version is approved by SKT Korean network operator.
LISA-U200-62S module product version is approved by NTT DoCoMo Japanese network operator
LISA-U270-62S, LISA-U270-63S and LISA-U270-68S modules product versions are approved and locked for SoftBank Japanese network operator.

Table 2: LISA-U2 series summary of interfaces and features

[4] Not supported by the "01" product version

1.2 Architecture

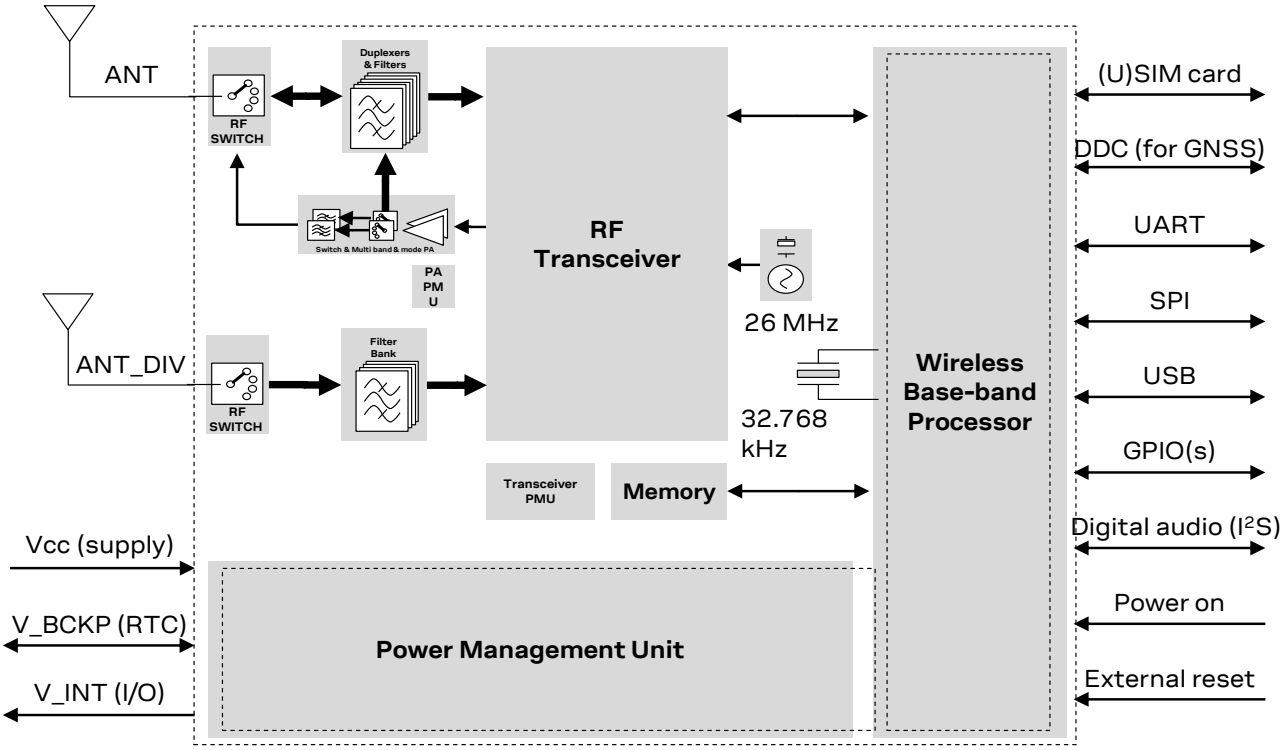


Figure 1: LISA-U2 series block diagram (for available options see Table 2)

1.2.1 Functional blocks

LISA-U2 modules consist of the following internal functional blocks: RF section, Baseband and Power Management Unit section.

LISA-U2 series RF section

A shielding box contains the RF high-power signal circuitry, including:

- Multimode Single Chain Power Amplifier Module used for 3G HSPA/WCDMA and 2G EDGE/GSM operations
- Power Management Unit with integrated DC/DC converter for the Power Amplifier Module

The RF antenna pad (**ANT**) is directly connected to the main antenna switch, which dispatches the RF signals according to the active mode. For time-duplex 2G operation, the incoming signal at the active receiver (RX) slot is applied by the main antenna switch to the duplexer SAW filter bank for out-of-band rejection and then sent to the appropriate receiver port of the RF transceiver. During the allocated Transmitter (TX) slots, the low level signal coming from the RF transceiver is enhanced by the power amplifier and then directed to the antenna pad through the main antenna switch. The 3G transmitter and receiver are active at the same time due to frequency-domain duplex operation. The switch integrated in the main antenna switch connects the antenna port to the duplexer SAW filter bank which separates the TX and RX signal paths. The duplexer itself provides front-end RF filtering for RX band selection while combining the amplified TX signal coming from the power amplifier.

A separated shielding box contains all the other analog RF components, including:

- Antenna switch and duplexer SAW filter bank for main paths
- Antenna switch and SAW filter bank for diversity receiver
- Up to six-band HSPA/WCDMA and quad-band EDGE/GPRS/GSM transceiver

- Power management unit with integrated DC/DC converter for the power amplifier module
- Voltage-controlled temperature compensated 26 MHz crystal oscillator (VC-TCXO)

While operating in 3G mode, the RF transceiver performs direct up-conversion and down-conversion of the baseband I/Q signals, with the RF voltage controlled gain amplifier being used to set the uplink TX power. In the downlink path, the integrated LNA enhances the RX sensitivity while discrete inter-stage SAW filters additionally improve the rejection of out-of-band blockers. An internal programmable gain amplifier optimizes the signal levels before delivering to the analog I/Q to baseband for further digital processing.

For 2G operations, a constant gain direct conversion receiver with integrated LNAs and highly linear RF quadrature demodulator are used to provide the same I/Q signals to the baseband as well. In transmission mode, the up-conversion is implemented by means of a digital sigma-delta transmitter or polar modulator depending on the modulation to be transmitted.

The RF antenna pad for the diversity receiver (**ANT_DIV**) available on LISA-U230 modules is directly connected to the antenna switch for the diversity receiver, which dispatches the incoming RF signals to the dedicated SAW filter bank for out-of-band rejection and then to the diversity receiver port of the RF transceiver.

In all the modes, a fractional-N sigma-delta RF synthesizer and an on-chip 3.296-4.340 GHz voltage-controlled oscillator are used to generate the local oscillator signal. The frequency reference to RF oscillators is provided by the 26 MHz VC-TCXO. The same signal is buffered to the baseband as a master reference for clock generation circuits while operating in active mode.

LISA-U2 series modulation techniques

Modulation techniques related to radio technologies supported by LISA-U2 modules, are listed as follows:

- GSM → GMSK
- GPRS → GMSK
- EDGE → GMSK / 8-PSK
- WCDMA → QPSK
- HSDPA → QPSK / 16-QAM
- HSUPA → QPSK / 16-QAM

LISA-U2 series Baseband and Power Management Unit section

Another shielding box of the LISA-U2 modules includes all the digital circuitry and the power supplies, basically the following functional blocks:

- Cellular baseband processor, a mixed signal ASIC which integrates:
  - Microprocessor for controller functions, 2G & 3G upper layer software
  - DSP core for 2G Layer 1 and audio processing
  - 3G coprocessor and HW accelerator for 3G layer 1 control software and routines
  - Dedicated HW for interfaces management
- Memory system in a Multi-Chip Package (MCP) integrating two devices:
  - NOR flash non-volatile memory
  - DDR SRAM volatile memory
- Power Management Unit (PMU), used to derive all the system supply voltages from the module supply VCC
- 32.768 kHz crystal, connected to the Real Time Clock (RTC) oscillator to provide the clock reference in idle or power-off modes

1.3 Pin-out

Table 3 details the pin-out of the LISA-U2 modules, with pins grouped by function.

Function	Pin	Module	No	I/O	Description	Remarks
Power	**VCC**	All	61, 62, 63	I	Module supply input	Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided must be always above the minimum limit of the operating range. Consider that there are large current spikes in connected mode, when a GSM call is enabled. **VCC** pins are internally connected, but all the available pads must be connected to the external supply in order to minimize power loss due to series resistance. See section 1.5.2
	GND	All	1, 3, 6, 7, 8, 17, 25, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 60, 64, 65, 66, 67, 69, 70, 71, 72, 73, 75, 76	N/A	Ground	**GND** pins are internally connected but a good (low impedance) external ground connection can improve RF performance: all **GND** pins must be externally connected to ground.
	V_BCKP	All	2	I/O	Real Time Clock supply input/output	**V_BCKP** = 1.8 V (typical) generated by the module when **VCC** supply voltage is within valid operating range. See section 1.5.4
	V_INT	All	4	O	Digital Interfaces supply output	**V_INT** = 1.8V (typical) generated by the module when it is switched-on and the **RESET_N** (external reset input pin) is not forced to the low level. See section 1.5.5
	VSIM	All	50	O	SIM supply output	**VSIM** = 1.80 V typical or 2.90 V typical generated by the module according to the SIM card type. See section 1.8
RF	**ANT**	All	68	I/O	RF input/output for main Tx/Rx antenna	50 Ω nominal impedance. See section 1.7, section 2.4 and section 2.2.1.1
	ANT_DIV	LISA-U230	74	I	RF input for Rx diversity antenna	50 Ω nominal impedance See section 1.7, section 2.4 and section 2.2.1.1
SIM	**SIM_IO**	All	48	I/O	SIM data	Internal 4.7 kΩ pull-up to **VSIM**. Must meet SIM specifications. See section 1.8
	SIM_CLK	All	47	O	SIM clock	Must meet SIM specifications. See section 1.8
	SIM_RST	All	49	O	SIM reset	Must meet SIM specifications. See section 1.8

Function	Pin	Module	No	I/O	Description	Remarks
SPI	**SPI_MISO**	All	57	O	SPI Data Line Output	Module Output: module runs as an SPI slave. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. See section 1.9.4
	SPI_MOSI	All	56	I	SPI Data Line Input	Module Input: module runs as an SPI slave. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). Idle high. Internal active pull-up to **V_INT** (1.8 V) enabled. See section 1.9.4
	SPI_SCLK	All	55	I	SPI Serial Clock Input	Module Input: module runs as an SPI slave. Idle low (CPOL=0). Internal active pull-down to **GND** enabled. See section 1.9.4
	SPI_SRDY	All	58	O	SPI Slave Ready Output	Module Output: module runs as an SPI slave. Idle low. See section 1.9.4
	SPI_MRDY	All	59	I	SPI Master Ready Input	Module Input: module runs as an SPI slave. Idle low. Internal active pull- down to **GND** enabled. See section 1.9.4
DDC	**SCL**	All	45	O	I^2C bus clock line	**Fixed open drain. External pull-up required.** See section 1.10
	SDA	All	46	I/O	I^2C bus data line	**Fixed open drain. External pull-up required.** See section 1.10
UART	**RxD**	All	16	O	UART data output	Circuit 104 (RxD) in ITU-T V.24. Provide access to the pin for FW update and debugging if the USB interface is connected to the application processor. See section 1.9.2
	TxD	All	15	I	UART data input	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to **V_INT** (1.8 V) enabled. Provide access to the pin for FW update and debugging if the USB interface is connected to the application processor. See section 1.9.2
	CTS	All	14	O	UART clear to send output	Circuit 106 (CTS) in ITU-T V.24. Provide access to the pin for debugging if the USB interface is connected to the application processor. See section 1.9.2
	RTS	All	13	I	UART ready to send input	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to **V_INT** (1.8 V) enabled. Provide access to the pin for debugging if the USB interface is connected to the application processor. See section 1.9.2
	DSR	All	9	O	UART data set ready output	Circuit 107 (DSR) in ITU-T V.24. See section 1.9.2
	RI	All	10	O	UART ring indicator output	Circuit 125 (RI) in ITU-T V.24. See section 1.9.2
	DTR	All	12	I	UART data terminal ready input	Circuit 108/2 (DTR) in ITU-T V.24. Internal active pull-up to **V_INT** (1.8 V) enabled. See section 1.9.2
	DCD	All	11	O	UART data carrier detect output	Circuit 109 (DCD) in ITU-T V.24. See section 1.9.2

Function	Pin	Module	No	I/O	Description	Remarks
GPIO	**GPIO1**	All	20	I/O	GPIO	See section 1.12
	GPIO2	All	21	I/O	GPIO	See section 1.12
	GPIO3	All	23	I/O	GPIO	See section 1.12
	GPIO4	All	24	I/O	GPIO	See section 1.12
	GPIO5	All	51	I/O	GPIO	See section 1.12
	GPIO6	All	39	I/O	GPIO	See section 1.12
	GPIO7	All	40	I/O	GPIO	See section 1.12
	GPIO8	All	53	I/O	GPIO	See section 1.12
	GPIO9	All	54	I/O	GPIO	See section 1.12
	GPIO10	All	55	I/O	GPIO	See section 1.12
	GPIO11	All	56	I/O	GPIO	See section 1.12
	GPIO12	All	57	I/O	GPIO	See section 1.12
	GPIO13	All	58	I/O	GPIO	See section 1.12
	GPIO14	All	59	I/O	GPIO	See section 1.12
USB	**VUSB_DET**	All	18	I	USB detect input	Input for VBUS (5 V typical) USB supply sense to enable USB interface. Provide access to the pin for FW update and debugging if the USB interface is not connected to the application processor. See section 1.9.3
	USB_D-	All	26	I/O	USB Data Line D-	90 Ω nominal differential impedance (Z_0) 30 Ω nominal common mode impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by USB 2.0 specifications [7] are part of the USB pad driver and need not be provided externally. Provide access to the pin for FW update and debugging if the USB interface is not connected to the application processor. See section 1.9.3
	USB_D+	All	27	I/O	USB Data Line D+	90 Ω nominal differential impedance (Z_0) 30 Ω nominal common mode impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [7] are part of the USB pad driver and need not be provided externally. Provide access to the pin for FW update and debugging if the USB interface is not connected to the application processor. See section 1.9.3
System	**PWR_ON**	All	19	I	Power-on input	**PWR_ON** pin has high input impedance. Do not keep floating in noisy environment: external pull-up required. See section 1.6.1
	RESET_N	All	22	I	External reset input	Internal 10 kΩ pull-up to **V_BCKP**. See section 1.6.3

Function	Pin	Module	No	I/O	Description	Remarks
Digital Audio	**I2S_CLK**	All	43	I/O	First I²S clock	Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	I2S_RXD	All	44	I	First I²S receive data	Internal active pull-down to GND enabled. Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	I2S_TXD	All	42	O	First I²S transmit data	Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	I2S_WA	All	41	I/O	First I²S word alignment	Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	I2S1_CLK	All	53	I/O	Second I²S clock	Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	I2S1_RXD	All	39	I	Second I²S receive data	Internal active pull-down to GND enabled. Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	I2S1_TXD	All	40	O	Second I²S transmit data	Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	I2S1_WA	All	54	I/O	Second I²S word alignment	Check device specifications to ensure compatibility with module supported modes. See section 1.11.
	CODEC_CLK	All	52	O	Clock output	Digital clock output for external audio codec See section 1.11.
Reserved	**RSVD**	All	5	N/A	RESERVED pin	This pin must be connected to ground See section 1.13
	RSVD	LISA-U200 LISA-U201 LISA-U260 LISA-U270	74	N/A	RESERVED pin	Do not connect See section 1.13

Table 3: LISA-U2 modules pin definition, grouped by function

1.4 Operating modes

LISA-U2 series modules have several operating modes. The operating modes are defined in Table 4 and described in details in Table 5, providing general guidelines for operation.

General Status	Operating Mode	Definition
Power-down	**Not-Powered Mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-Off Mode	**VCC** supply within operating range and module is switched off.
Normal Operation	**Idle mode**	Module processor core runs with 32 kHz as the reference oscillator.
	Active mode	Module processor core runs with 26 MHz as the reference oscillator.
	Connected mode	Voice or data call enabled and processor core runs with 26 MHz as the reference oscillator.

Table 4: Module operating modes definition

Operating Mode	Description	Transition between operating modes
Not-Powered	Module is switched off. Application interfaces are not accessible. Internal RTC timer operates only if a valid voltage is applied to **V_BCKP** pin.	When **VCC** supply is removed, the module enters not-powered mode. When in not-powered mode, the module cannot be switched on by a low pulse on **PWR_ON** input, by a rising edge on **RESET_N** input, or by a preset RTC alarm. When in not-powered mode, the module can be switched on by applying **VCC** supply (see 1.6.1) so that the module switches from not-powered to active mode.
Power-Off	Module is switched off: normal shutdown by an appropriate power-off event (see 1.6.2). Application interfaces are not accessible. Only the internal RTC timer in operation.	When the module is switched off by an appropriate power-off event (see 1.6.2), the module enters power-off mode from active mode. When in power-off mode, the module can be switched on by a low pulse on **PWR_ON** input, by a rising edge on **RESET_N** input, or by a preset RTC alarm (see 1.6.1): module switches from power-off to active mode. When **VCC** supply is removed, the module switches from power-off mode to not-powered mode.
Idle	Application interfaces are disabled: the module does not accept data signals from an external device connected to the module. The module automatically enters idle mode whenever possible if power saving is enabled by AT+UPSV (see u-blox AT Commands Manual [2]), reducing current consumption (see 1.5.3.3). If HW flow control is enabled (default setting) and AT+UPSV=1 or AT+UPSV=3 has been set, the UART **CTS** line indicates when the UART is enabled (see 1.9.2.2, 1.9.2.3). If HW flow control is disabled by AT&K0, the UART **CTS** line is fixed to ON state (see 1.9.2.2). Power saving configuration is not enabled by default: it can be enabled by AT+UPSV (see the u-blox AT Commands Manual [2]).	The module automatically switches from active mode to idle mode whenever possible if power saving is enabled (see 1.5.3.3, 1.9.2.3, 1.9.3.2, 1.9.4.2 and the u-blox AT Commands Manual [2], AT+UPSV). The module wakes up from idle mode to active mode for these events: Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (see 1.5.3.3, 1.9.2.3) Automatic periodic enable of the UART interface to receive and send data, if AT+UPSV=1 has been set (see 1.9.2.3) RTC alarm occurs (see the u-blox AT Commands Manual [2], AT+CALA) Data received on UART interface, if HW flow control has been disabled by AT&K0 and AT+UPSV=1 has been set (see 1.9.2.3) **RTS** input set ON by the DTE if HW flow control has been disabled by AT&K0 and AT+UPSV=2 has been set (see 1.9.2.3) **DTR** input set ON by DTE if AT+UPSV=3 has been set (see 1.9.2.3) USB detection, applying 5 V (typical) to **VUSB_DET** input (see 1.9.3) The connected USB host forces a remote wakeup of the module as a USB device (see 1.9.3) The connected SPI master indicates by the **SPI_MRDY** input signal that it is ready for transmission or reception (see 1.9.4) The connected u-blox GNSS receiver indicates by the **GPIO3** pin that it is ready to send data (see 1.10, 1.12)

Operating Mode	Description	Transition between operating modes
Active	The module is ready to accept data signals from an external device unless power saving configuration is enabled by AT+UPSV (see sections 1.9.2.3, 1.9.3.2, 1.9.4.2 and the u-blox AT Commands Manual [2]).	When the module is switched on by an appropriate power-on event (see 1.6.1), the module enters active mode from not-powered or power-off mode. If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from active to idle mode whenever possible and the module wakes up from idle to active mode in the events listed above (see the idle to active transition description). When a voice call or a data call is initiated, the module switches from active mode to connected mode.
Connected	A voice call or a data call is in progress. When a voice or a data call is enabled, the application interfaces are kept enabled and the module is prepared to accept data from an external device unless power saving configuration is enabled by AT+UPSV (see 1.9.2.3, 1.9.3.2, 1.9.4.2 and the u-blox AT Commands Manual [2]).	When a voice call or a data call is initiated, the module enters connected mode from active mode. If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from connected to idle mode whenever possible in case of PSD data call with internal context activation, and then it wakes up from idle to connected mode in the events listed above (see the idle to active transition description). When a voice call or a data call is terminated, the module returns to active mode.

Table 5: Module operating modes description

Figure 2 describes the transition between the different operating modes.

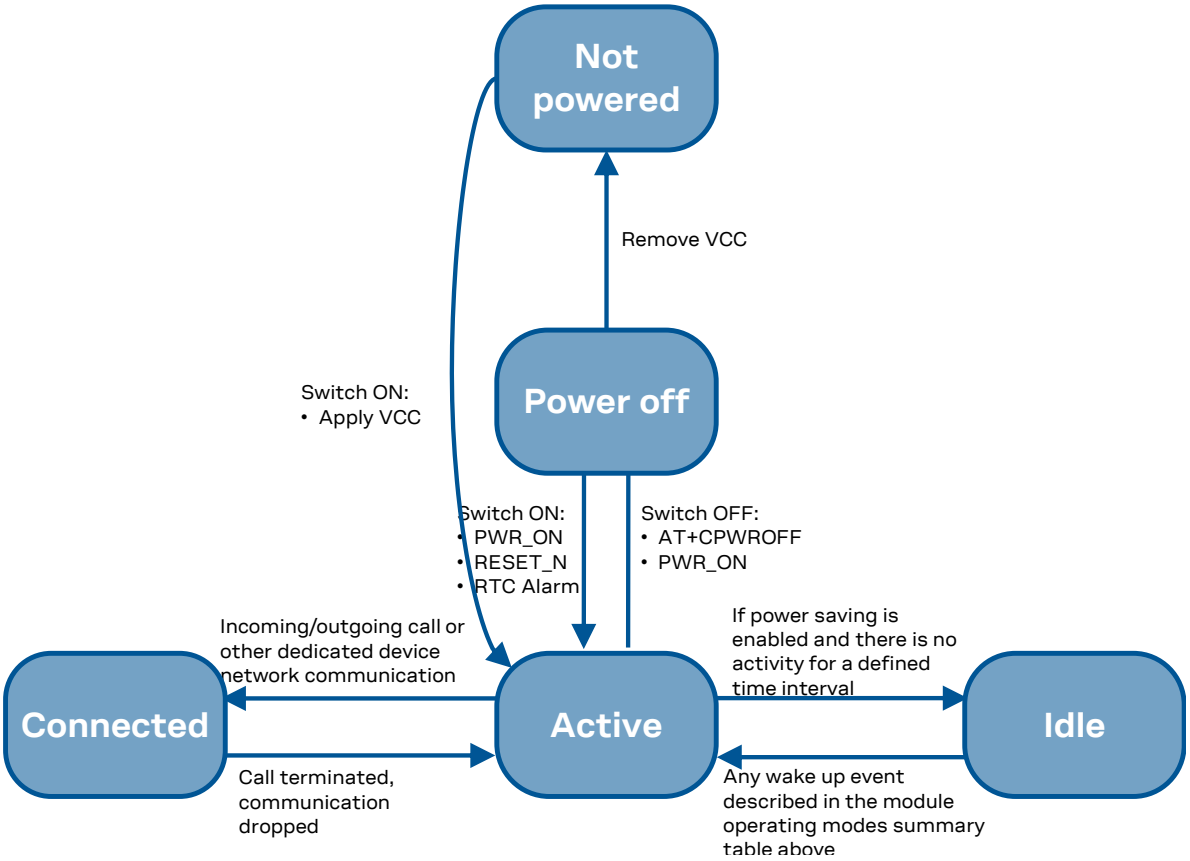


Figure 2: Operating modes transition

1.5 Power management

1.5.1 Power supply circuit overview

LISA-U2 series modules feature a power management concept optimized for the most efficient use of the supplied power. This is achieved by hardware design that uses a power efficient circuit topology (Figure 3), and by power management software that controls the module's power saving mode.

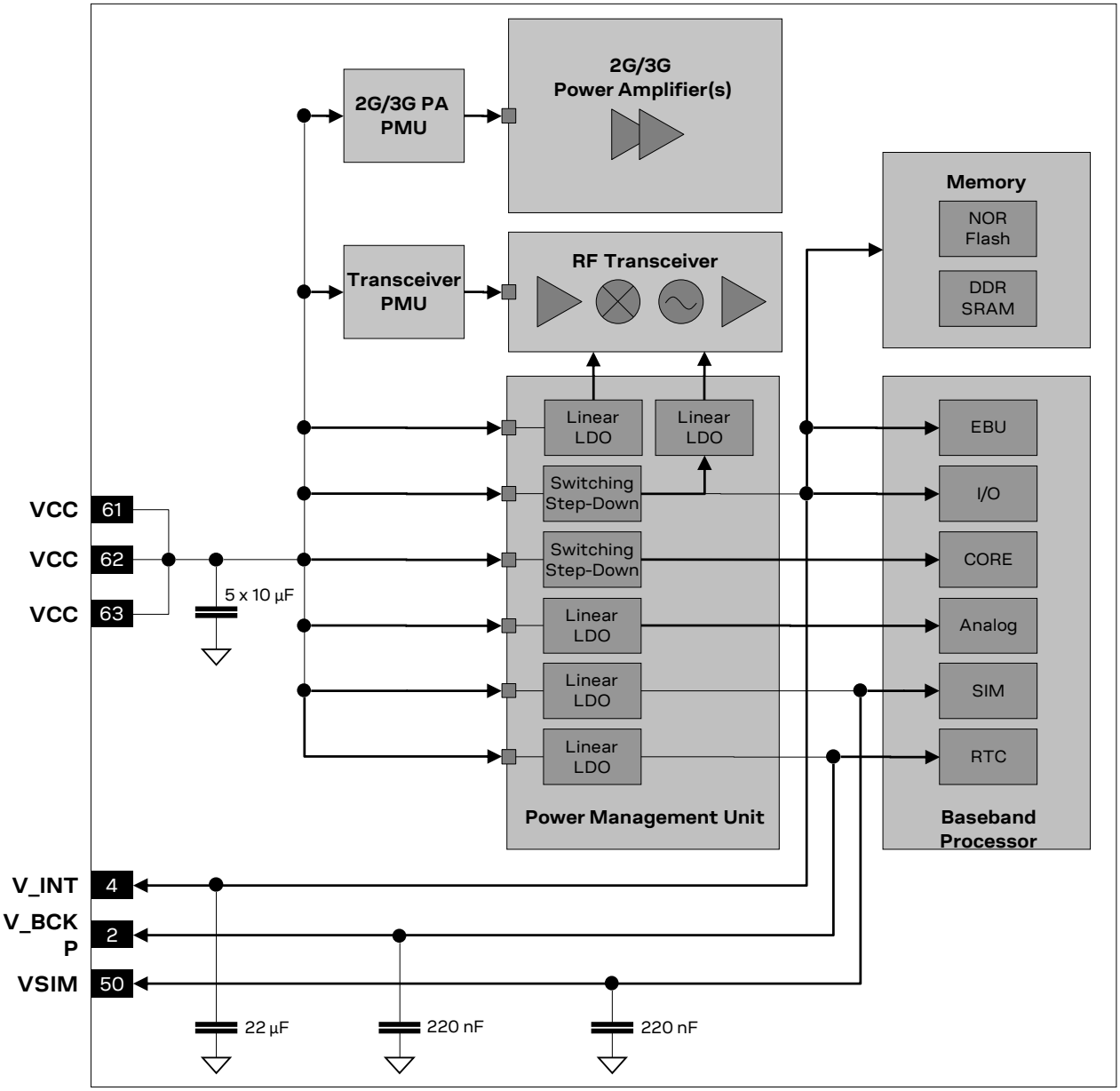


Figure 3: LISA-U2 series power management simplified block diagram

The pins with supply functions are listed in Table 6, Table 12 and Table 15.

LISA-U2 series modules must be supplied via the **VCC** pins. There is only one main power supply input, available on the three **VCC** pins that must be all connected to the external power supply.

The **VCC** pins are directly connected to the RF power amplifiers and to the integrated Power Management Unit (PMU) within the module: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators.

V_BCKP is the Real Time Clock (RTC) supply. When the **VCC** voltage is within the valid operating range, the internal PMU supplies the Real Time Clock and the same supply voltage will be available to the **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (for example, during not powered mode), the Real Time Clock can be externally supplied via the **V_BCKP** pin (see section 1.5.4).

When a 1.8 V or a 3 V SIM card type is connected, LISA-U2 series modules automatically supply the SIM card via the **VSIM** pin. Activation and deactivation of the SIM interface with automatic voltage switch from 1.8 to 3 V is implemented, in accordance with the ISO-IEC 7816-3 specifications.

The same voltage domain used internally to supply the digital interfaces is also available on the **V_INT** pin, to allow more economical and efficient integration of the LISA-U2 series modules in the final application.

The integrated Power Management Unit also provides the control state machine for system start-up and system reset control.

1.5.2 Module supply (VCC)

The LISA-U2 series modules must be supplied through the **VCC** pins by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some orders of magnitude, especially due to surging consumption profile of the GSM system (described in the section 1.5.3). It is important that the system power supply circuit is able to support peak power (see the LISA-U2 series Data Sheet [1] for the detailed specifications).

Name	Description	Remarks
VCC	Module power supply input	**VCC** pins are internally connected, but all the available pads must be connected to the external supply in order to minimize the power loss due to series resistance. Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided must always be above the minimum limit of the operating range. Consider that during a GSM call there are large current spikes in connected mode.
GND	Ground	**GND** pins are internally connected but a good (low impedance) external ground can improve RF performance: all available pads must be connected to ground.

Table 6: Module supply pins

☞ **VCC** pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels can be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible points.

The voltage provided to the **VCC** pins must be within the normal operating range limits as specified in the LISA-U2 series Data Sheet [1]. Complete functionality of the module is only guaranteed within the specified minimum and maximum **VCC** voltage normal operating range.

☞ The module cannot be switched on if the **VCC** voltage value is below the specified normal operating range minimum limit. Ensure that the input voltage at **VCC** pins is above the minimum limit of the normal operating range for more than 3 seconds after the start of the module switch-on sequence.

When LISA-U2 series modules are in operation, the voltage provided to **VCC** pins can exceed the normal operating range limits but must be within the extended operating range limits specified in the LISA-U2 series Data Sheet [1]. Occasional deviations from the ETSI specifications may occur when the input voltage at the **VCC** pins is outside the normal operating range and is within the extended operating range.

LISA-U2 series modules switch off when the **VCC** voltage value drops below the specified extended operating range minimum limit: ensure that the input voltage at the **VCC** pins never drops below the minimum limit of the extended operating range when the module is switched on, not even during a GSM transmit burst, where the current consumption can rise up to maximum peaks of 2.5 A in case of a mismatched antenna load.

Operation above the normal operating range maximum limit is not recommended and extended exposure beyond it may affect device reliability.

Stress beyond the VCC absolute maximum ratings can cause permanent damage to the module: if necessary, voltage spikes beyond the VCC absolute maximum ratings must be restricted to values within the specified limits by using appropriate protection.

When designing the power supply for the application, pay specific attention to power losses and transients. The DC power supply must be able to provide a voltage profile to the **VCC** pins with the following characteristics:

- Voltage drop during transmit slots must be lower than 400 mV
- No undershoot or overshoot at the start and at the end of transmit slots
- Voltage ripple during transmit slots must be minimized:
  less than 70 mVpp if $f_{ripple} \leq 200$ kHz
  less than 10 mVpp if 200 kHz < $f_{ripple} \leq 400$ kHz
  less than 2 mVpp if $f_{ripple} > 400$ kHz

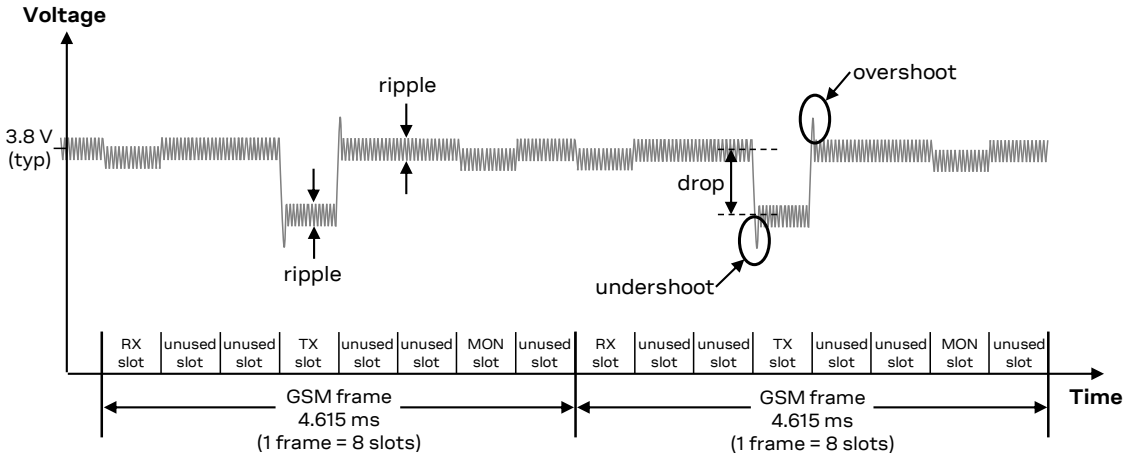


Figure 4: Description of the VCC voltage profile versus time during a GSM call

Any degradation in power supply performance (due to losses, noise or transients) will directly affect the RF performance of the module since the single external DC power source indirectly supplies all the digital and analog interfaces, and also directly supplies the RF power amplifier (PA).

The voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms. This **VCC** slope allows a proper switch-on of the module when the voltage rises to the **VCC** normal operating range from a voltage of less than 2.25 V. If the external supply circuit cannot raise the **VCC** voltage from 2.5 V to 3.2 V within 1 ms, the **RESET_N** pin should be kept low during **VCC** rising edge, so that the module will switch on releasing the **RESET_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal operating range.

1.5.2.1 VCC application circuits

LISA-U2 series modules must be supplied through the **VCC** pins by a clean DC power supply, which can be selected according to the application requirements (see Figure 5) between the different possible supply sources types, the most common ones of which are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

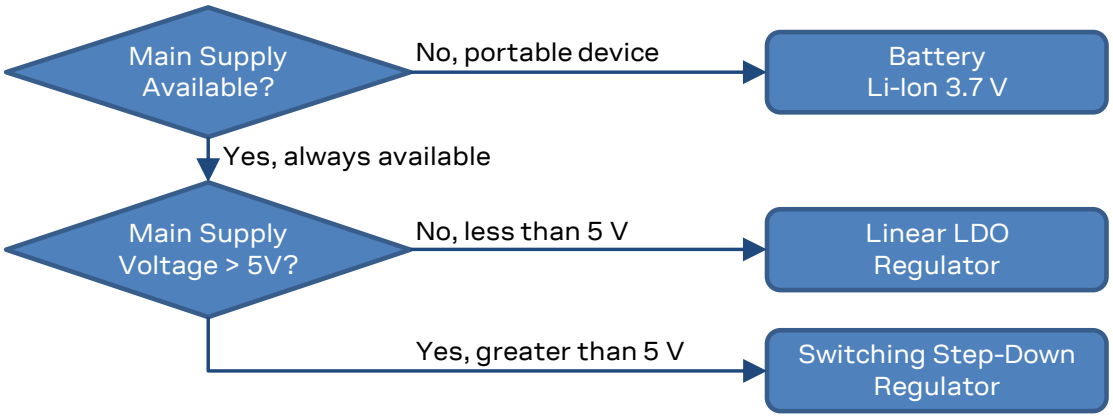


Figure 5: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the LISA-U2 series module's operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes the current drawn from the main supply source.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case, the typical 90% efficiency of the switching regulator will diminish the benefit of voltage step-down and no true advantage will be gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they will dissipate a considerable amount of energy in thermal power.

If LISA-U2 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided.

The use of a primary (not rechargeable) battery is uncommon, since most of the cells available are seldom capable of delivering the burst peak current for a GSM call due to high internal resistance.

Keep in mind that the use of batteries requires the implementation of a suitable charger circuit (not included in LISA-U2 series modules). The charger circuit should be designed in order to prevent over-voltage on **VCC** beyond the upper limit of the absolute maximum rating.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as being mutually exclusive.

The usage of a regulator or a battery not able to withstand the maximum **VCC** peak current consumption stated in the LISA-U2 series Data Sheet [1] is generally not recommended. However, if the selected regulator or battery is not able to withstand the maximum **VCC** peak current, it must be

able to withstand at least the maximum average current consumption value specified in the LISA-U2 series Data Sheet [1].

The additional energy required by the module during a GSM/GPRS Tx slot (when in the worst case the current consumption can rise up to 2.5 A, as described in section 1.5.3.1) can be provided by an appropriate bypass tank capacitor or supercapacitor with very large capacitance and very low ESR placed close to the module **VCC** pins. Depending on the actual capability of the selected regulator or battery, the required capacitance can be considerably larger than 1 mF and the required ESR can be in the range of a few tens of mΩ. Carefully evaluate the implementation of this solution since aging and temperature conditions significantly affect the actual capacitor characteristics.

The following sections highlight some design aspects for each of the supplies listed above.

Switching regulator

The characteristics of the switching regulator connected to **VCC** pins should meet the following requirements:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering 2.5 A current pulses with 1/8 duty cycle to the **VCC** pins.
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications, select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile and therefore negatively impact GSM modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple on **VCC**, but adds extra voltage drop due to resistive losses on series inductors.
- **PWM mode operation**: select preferably regulators with Pulse Width Modulation (PWM) mode. While in connected mode Pulse Frequency Modulation (PFM) mode and PFM/PWM mode transitions must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators able to switch between low ripple PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition occurs when the module changes status from idle/active mode to connected mode (where current consumption increases to a value greater than 100 mA): it is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 60 mA).
- **Output voltage slope**: the use of the soft start function provided by some voltage regulator must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module.

Figure 6 and the components listed in Table 7 show an example of a high reliability power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering 2.5 A current pulses with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz. The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V supply to the typical 3.8 V value of the **VCC** supply.

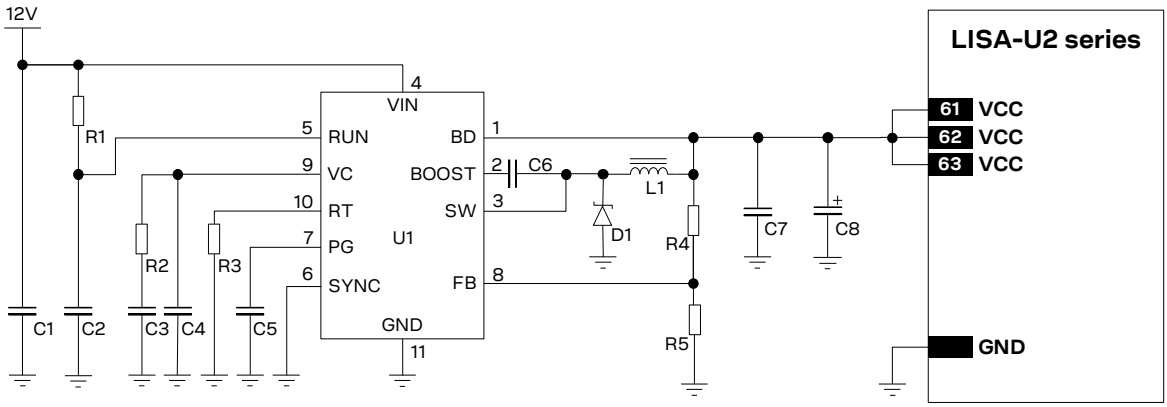


Figure 6: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 kΩ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	22 kΩ Resistor 0402 5% 0.1 W	2322-705-87223-L - Yageo
R4	390 kΩ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 kΩ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 7: Suggested components for the VCC voltage supply application circuit using a step-down regulator

Figure 7 and the components listed in Table 8 show an example of a low-cost power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable of delivering 2.5 A current pulses, transforming a 12 V supply input.

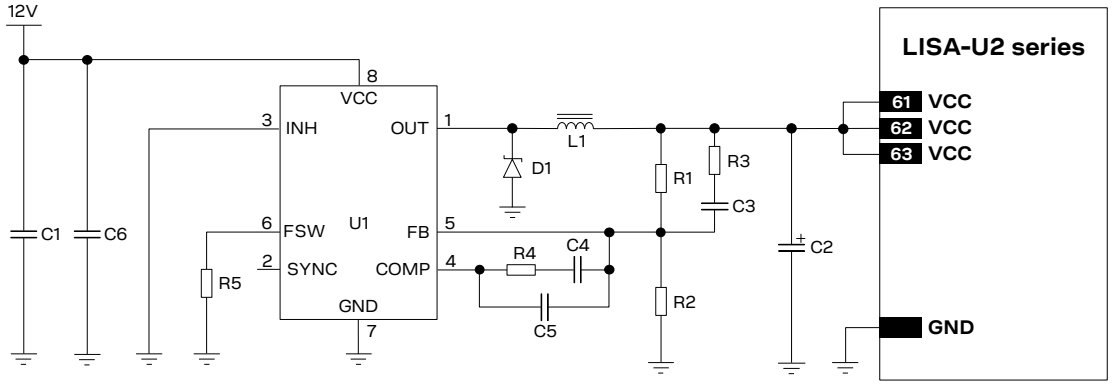


Figure 7: Suggested low cost solution for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 – Murata
C2	100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 – Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 – Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H560JA01 – Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 – Murata
D1	Schottky Diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ Resistor 0402 1% 0.063 W	RC0402FR-074K7L – Yageo
R2	910 Ω Resistor 0402 1% 0.063 W	RC0402FR-07910RL – Yageo
R3	82 Ω Resistor 0402 5% 0.063 W	RC0402JR-0782RL – Yageo
R4	8.2 kΩ Resistor 0402 5% 0.063 W	RC0402JR-078K2L – Yageo
R5	39 kΩ Resistor 0402 5% 0.063 W	RC0402JR-0739KL – Yageo
U1	Step-Down Regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 8: Suggested components for low cost solution VCC voltage supply application circuit using a step-down regulator

Low Drop-Out (LDO) linear regulator

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following requirements:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pins and of delivering 2.5 A current pulses with 1/8 duty cycle.
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).
- **Output voltage slope**: the use of the soft start function provided by some voltage regulators must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module.

Figure 8 and the components listed in Table 9 show an example of a power supply circuit where the **VCC** module supply is provided by an LDO linear regulator capable of delivering 2.5 A current pulses, with appropriate power handling capability. The use of a linear regulator is suggested when the difference from the available supply rail and the VCC value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module VCC normal operating range.

It is recommended to configure the LDO linear regulator so that it generates a voltage supply value slightly below the maximum limit of the module VCC normal operating range (e.g. ~4.1 V as in the circuit described in Figure 8 and Table 9). This reduces the power on the linear regulator and improves the thermal design of the supply circuit.

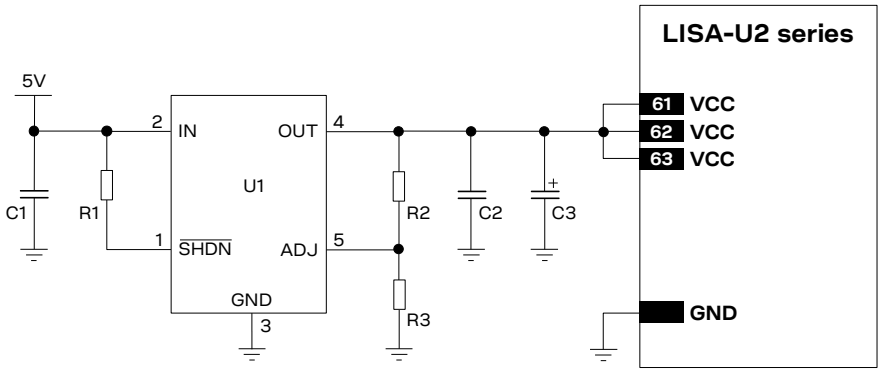


Figure 8: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C3	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	9.1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-079K1L - Yageo Phycomp
R3	3.9 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K9L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 9: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

Rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following requirements:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its output circuit must be capable of delivering 2.5 A current pulses with 1/8 duty-cycle to the **VCC** pins and must be capable of delivering a DC current greater than the module's maximum average current consumption to **VCC** pins. The maximum pulse discharge current and the maximum DC discharge current are not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts.

Primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following requirements:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its output circuit must be capable of delivering 2.5 A current pulses with 1/8 duty-cycle to the **VCC** pins and must be capable of delivering a DC current greater than the module maximum average current consumption at the **VCC** pins. The maximum pulse and the maximum DC discharge current is not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts.

Additional recommendations for the VCC supply application circuits

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible in order to minimize power losses.

It is recommended to properly connect all three **VCC** pins and all twenty **GND** pins of the module to the supply source to minimize series resistance losses.

To avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a GSM call (when current consumption on the **VCC** supply can rise up to as much as 2.5 A in the worst case), place a bypass capacitor with large capacitance (more than 100 µF) and low ESR near the **VCC** pins, for example:

- 330 µF capacitance, 45 mΩ ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

The use of very large capacitors (i.e. greater than 1000 µF) on the **VCC** line and the use of the soft start function provided by some voltage regulators must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module.

To reduce voltage ripple and noise, which should improve RF performance if the application device integrates an internal antenna, place the following series ferrite bead and bypass capacitors near the **VCC** pins of the module:

- Ferrite bead for GHz band noise (e.g. Murata BLM18EG221SN1) as close as possible to the **VCC** pins of the module, implementing the circuit described in Figure 9, to filter EMI in all the GSM / UMTS bands.

- 68 pF capacitor with Self-Resonant Frequency in the 800/900 MHz range (e.g. Murata GRM1555C1H680J) at the **VCC** line where it narrows close to the module (see Figure 9), to filter EMI in lower bands
- 15 pF capacitor with Self-Resonant Frequency in 1800/1900 MHz range (e.g. Murata GRM1555C1H150J)
  at the **VCC** line where it narrows close to the module (see Figure 9), to filter EMI in higher bands
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 100 nF capacitor (e.g. Murata GRM155R61A104K) to filter digital logic noise from clocks and data sources

☞ Figure 9 shows the complete configuration, but keep in mind that the mounting of each single component depends on the application design. It is highly recommended to provide the series ferrite bead and all the **VCC** bypass capacitors as described in Figure 9 and Table 10 if the application device integrates an internal antenna.

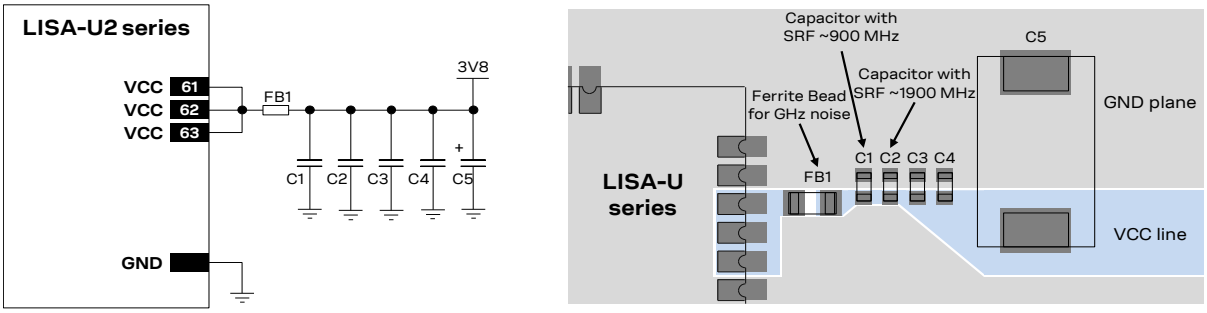


Figure 9: Suggested schematic and layout design for the VCC line; highly recommended when using an integrated antenna

Reference	Description	Part Number - Manufacturer
C1	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C2	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C3	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
FB1	Chip Ferrite Bead EMI Filter for GHz Band Noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 10: Suggested parts for VCC circuit close to module' pins; highly recommended when using an integrated antenna

External battery charging application circuit

LISA-U2 series modules do not have an on-board charging circuit. An example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell, is provided in Figure 10.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the **VCC** supply input of LISA-U2 series module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.

- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA).
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 seconds.

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Alternatively the L6924U, providing input voltage range up to 12 V, can charge from an AC wall adapter. When a current-limited adapter is used, it can operate in quasi-pulse mode, reducing power dissipation.

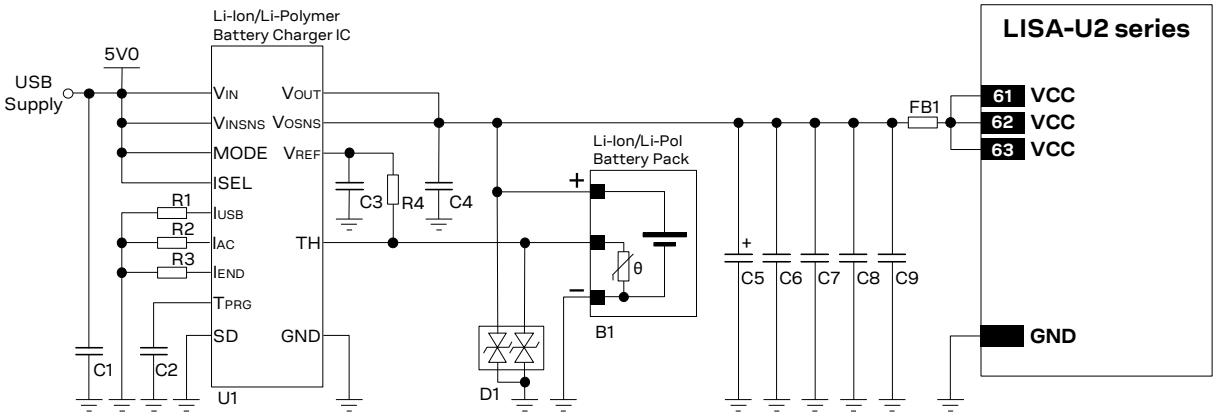


Figure 10: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Various manufacturer
C1, C4	1 µF Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C9	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
D1	Low Capacitance ESD Protection	USB0002RP or USB0002DP - AVX
FB1	Chip Ferrite Bead EMI Filter for GHz Band Noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata
R1, R2	24 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0724KL - Yageo Phycomp
R3	3.3 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K3L - Yageo Phycomp
R4	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC for USB port and AC Adapter	L6924U - STMicroelectronics

Table 11: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit

1.5.3 Current consumption profiles

During operation, the current drawn by the LISA-U2 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the high peak of current consumption during GSM transmitting bursts at maximum power level in 2G connected mode, to a continuous high current drawn in UMTS connected mode, to the low current consumption during power saving in idle mode.

1.5.3.1 2G connected mode

When a GSM call is established, the **VCC** consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. If the module is transmitting in GSM talk mode in the GSM 850 or in the E-GSM 900 band and at the maximum RF power control level (approximately 2 W or 33 dBm in the allocated transmit slot/burst) the current consumption can reach up to 2500 mA (with a highly unmatched antenna) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access). If the module is in GSM connected mode in the DCS 1800 or in the PCS 1900 band, the current consumption figures are lower than the one in the GSM 850 or in the E-GSM 900 band, due to 3GPP transmitter output power specifications (see the LISA-U2 series Data Sheet [1]).

During a GSM call, current consumption is in the order of 60-130 mA in receiving or in monitor bursts and is about 10-40 mA in the inactive unused bursts (low current period). The more relevant contribution to determine the average current consumption is set by the transmitted power in the transmit slot.

An example of the current consumption profile of the data module in GSM talk mode is shown in Figure 11.

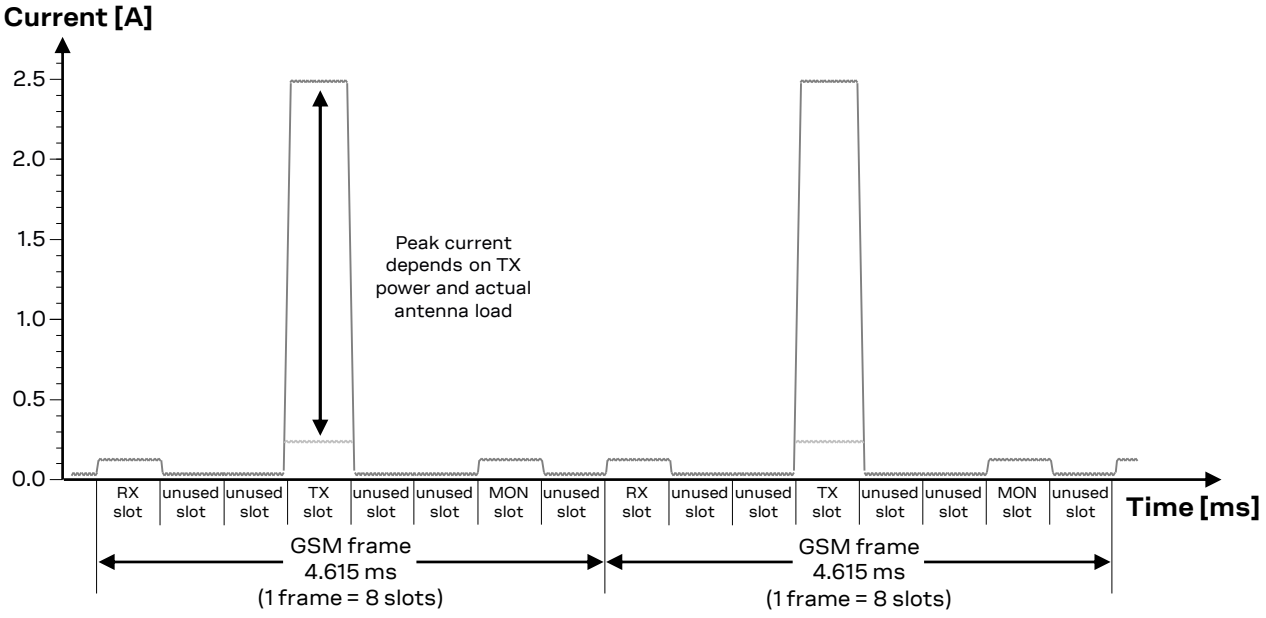


Figure 11: VCC current consumption profile versus time during a GSM call (1 TX slot, 1 RX slot)

When a GPRS connection is established, there is a different VCC current consumption profile also determined by the transmitting and receiving bursts. In contrast to a GSM call, during a GPRS connection more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions, which set the peak current consumption, but if following the GPRS specifications, the maximum transmitted RF power is reduced when more than one slot is used to transmit, so the maximum peak of current consumption is not as high as can be in the case of a GSM call.

If the module transmits in GPRS class 12 connected mode in the GSM 850 or in the E-GSM 900 band at the maximum power control level, the current consumption can reach up to 1600 mA (with unmatched antenna). This happens for 2.307 ms (width of the 4 transmit slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/2 duty cycle, according to GSM TDMA. If the module is in GPRS connected mode in the DCS 1800 or in the PCS 1900 band, the current consumption figures are lower than in the GSM 850 or in the E-GSM 900 band, due to 3GPP transmitter output power specifications (see the LISA-U2 series Data Sheet [1]).

Figure 12 reports the current consumption profiles in GPRS class 12 connected mode, in the GSM 850 or in the E-GSM 900 band, with 4 slots used to transmit and 1 slot used to receive.

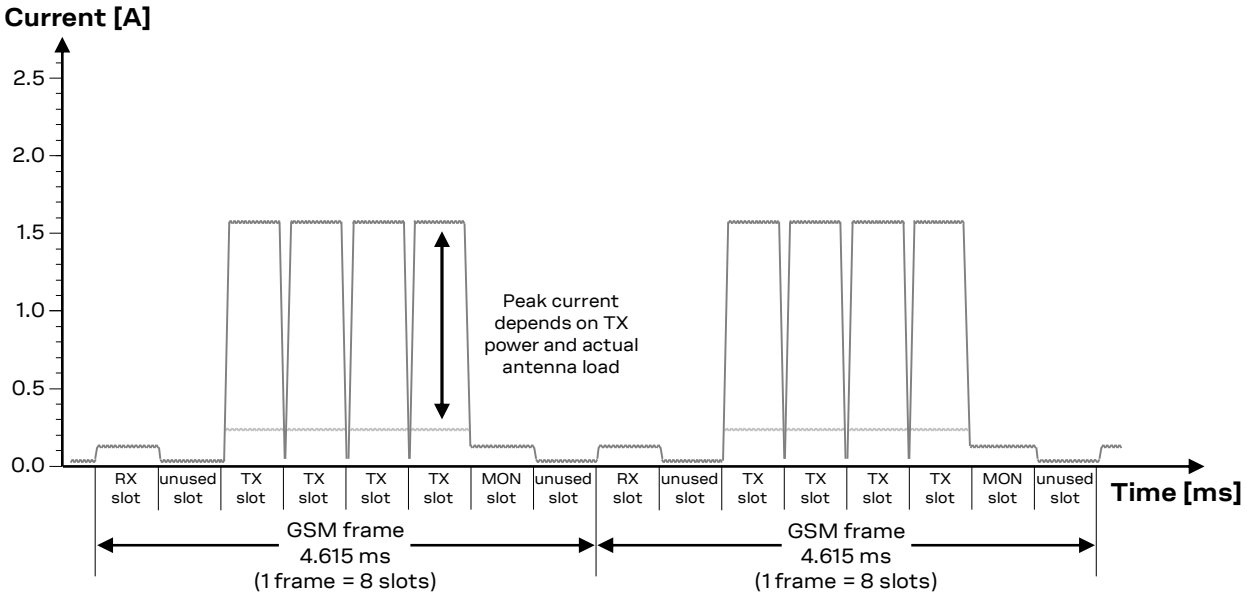


Figure 12: VCC current consumption profile versus time during a GPRS/EDGE connection (4TX slots, 1 RX slot)

In case of EDGE connections, the VCC current consumption profile is very similar to the GPRS current profile, so the image shown in Figure 12, representing the current consumption profile in GPRS class 12 connected mode, is valid for the EDGE class 12 connected mode as well.

1.5.3.2 3G connected mode

During a 3G connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation with the Wideband Code Division Multiple Access (WCDMA). The current consumption depends again on output RF power, which is always regulated by network commands. These power control commands are logically divided into a slot of 666 µs, thus the rate of power change can reach a maximum rate of 1.5 kHz. There are no high current peaks as in the 2G connection, since transmission and reception are continuously enabled due to FDD WCDMA implemented in the 3G that differs from the TDMA implemented in the 2G case. In the worst case scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the current drawn by the module at the VCC pins is in the order of continuous 500-800 mA (see LISA-U2 series Data Sheet [1] for detailed values). Even at lowest output RF power (approximately 0.01 µW or -50 dBm), the current still remains in the order of 200 mA due to module baseband processing and transceiver activity.

An example of current consumption profile of the data module in UMTS/HSxPA continuous transmission mode is shown in Figure 13.

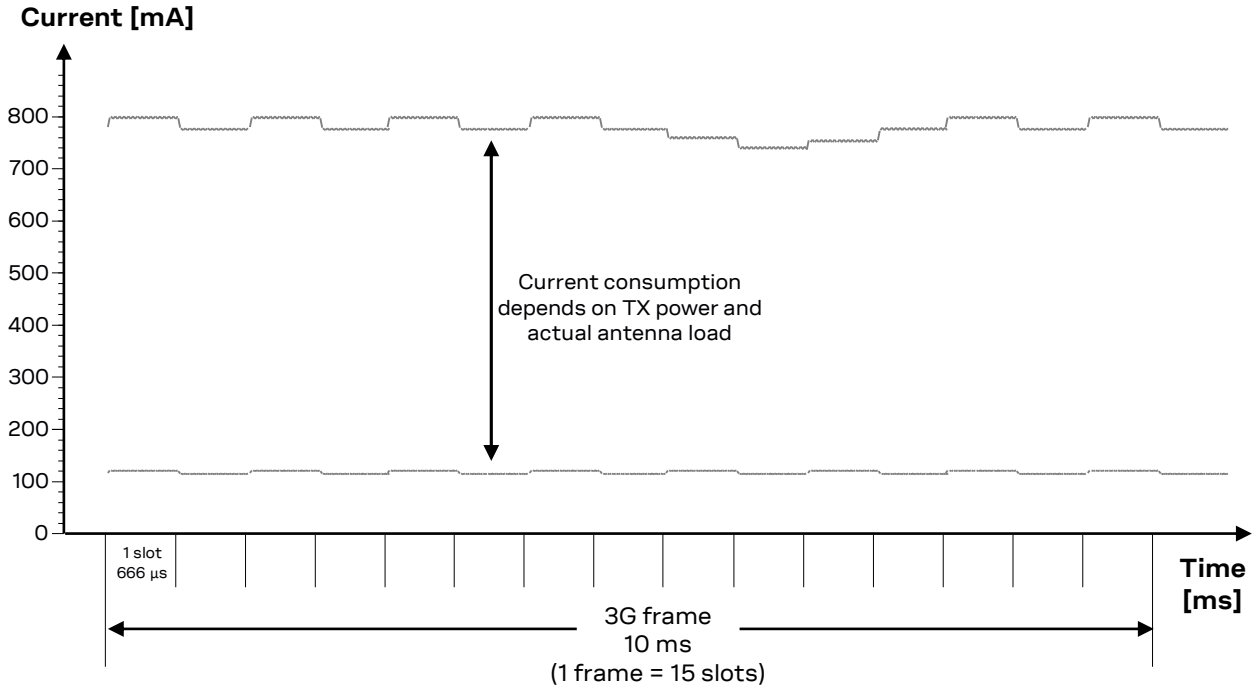


Figure 13: VCC current consumption profile versus time during a UMTS/HSPA connection

When a packet data connection is established, the actual current profile depends on the volume of transmitted packets; there might be some periods of inactivity between allocated slots where current consumption drops about 100 mA. Alternatively, at higher data rates the transmitted power is likely to increase due to the higher quality signal required by the network to cope with the enhanced data speed.

1.5.3.3 2G and 3G cyclic idle/active mode (power saving enabled)

The power saving configuration is disabled by default, but it can be enabled using the appropriate AT command (see the u-blox AT Commands Manual [2], AT+UPSV command). When power saving is enabled, the module automatically enters idle mode whenever possible.

When power saving is enabled, the module is registered or attached to a network and a voice or data call is not enabled, the module automatically enters idle mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance with GSM system requirements. When the module monitors the paging channel, it wakes up to active mode, to enable the reception of paging block. In between, the module switches to idle mode. This is known as GSM discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 26 MHz used in active mode.

The time period between two paging block receptions is defined by the network (2G or 3G). This is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell.

For a 2G network, the time interval between two paging block receptions can be from 470.76 ms (DRX = 2, i.e. width of 2 GSM multiframes = 2 x 51 GSM frames = 2 x 51 x 4.615 ms) up to 2118.42 ms (DRX = 9, i.e. width of 9 GSM multiframes = 9 x 51 frames = 9 x 51 x 4.615 ms).

For a 3G network, the principle is similar but time interval changes from 640 ms (DRX = 6, i.e. the width of 2^6 x 3G frames = 64 x 10 ms = 640 ms) up to 5120 ms (DRX = 9, i.e. width of 2^9 x 3G frames = 512 x 10 ms = 5120 ms).

An example of a module's current consumption profile is shown in Figure 14: the module is registered with the network (2G or 3G), automatically enters idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception.

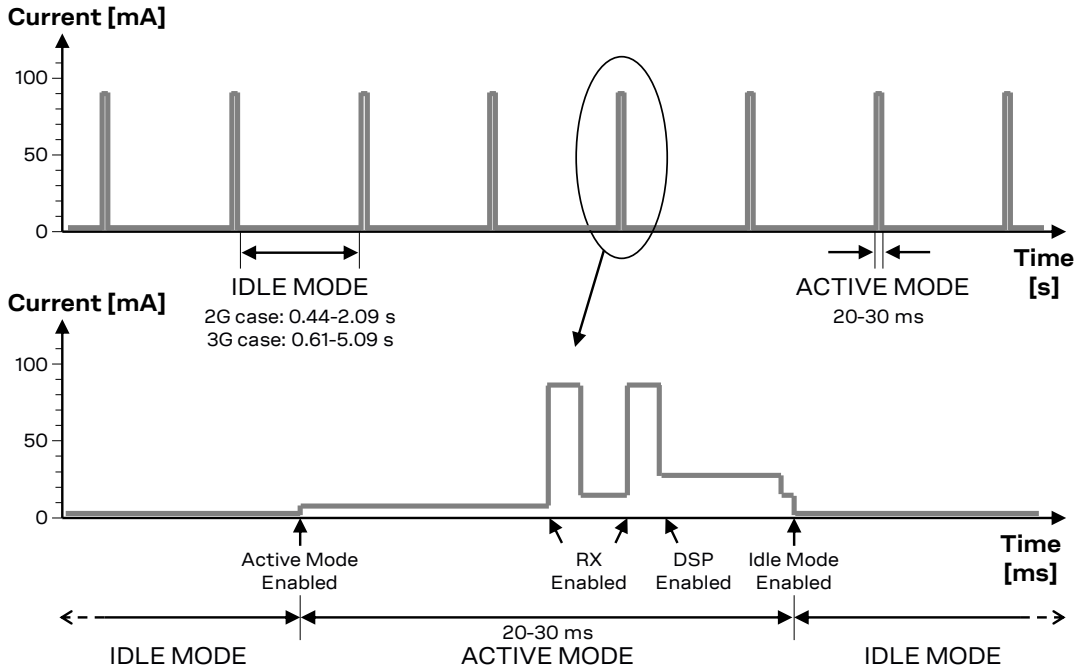


Figure 14: Description of VCC current consumption profile versus time when the module is registered with 2G or 3G networks: the module is in idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception

1.5.3.4 2G and 3G fixed active mode (power saving disabled)

Power saving configuration is disabled by default, or it can be disabled using the appropriate AT command (see the u-blox AT Commands Manual [2], AT+UPSV command). When power saving is disabled, the module does not automatically enter idle mode whenever possible: the module remains in active mode.

The module processor core is activated during active mode, and the 26 MHz reference clock frequency is used.

An example of the current consumption profile of the data module when power saving is disabled is shown in Figure 15: the module is registered with the network, active mode is maintained, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception.

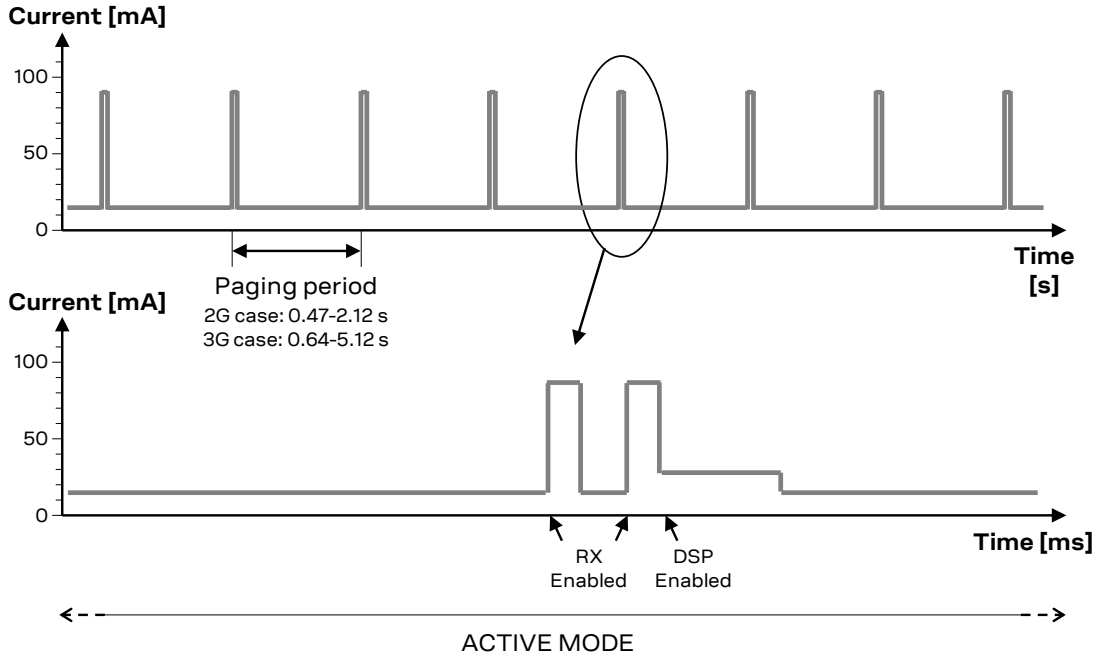


Figure 15: Description of the VCC current consumption profile versus time when power saving is disabled: the active mode is always held, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception

1.5.4 RTC Supply (V_BCKP)

The **V_BCKP** pin connects the supply for the Real Time Clock (RTC) and Power-On / Reset internal logic. This supply domain is internally generated by a linear regulator integrated in the Power Management Unit. The output of this linear regulator is always enabled when the main voltage supply provided to the module through **VCC** is within the valid operating range, with the module switched-off or powered-on.

V_BCKP supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

Name	Description	Remarks
V_BCKP	Real Time Clock supply	**V_BCKP** output voltage = 1.8 V (typical) Generated by the module to supply Real Time Clock when VCC supply voltage is within valid operating range.

Table 12: Real Time Clock supply pin

☞ The **V_BCKP** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the line is externally accessible on the application board. Higher protection levels can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.

The RTC provides the time reference (date and time) of the module, also in power-off mode, when the **V_BCKP** voltage is within its valid range (specified in the input characteristics of the supply/power pins table in the LISA-U2 series Data Sheet [1]). The RTC timing is normally used to set the wake-up interval during idle mode periods between network paging, but is able to provide programmable alarm functions by means of the internal 32.768 kHz clock.

The RTC can be supplied from an external back-up battery through the **V_BCKP**, when the main voltage supply is not provided to the module through **VCC**. This lets the time reference (date and time) run until the **V_BCKP** voltage is within its valid range, even when the main supply is not provided to the module.

The RTC oscillator does not necessarily stop operation (i.e. the RTC counting does not necessarily stop) when the **V_BCKP** voltage value drops below the specified operating range minimum limit (1 V): the RTC value read after a system restart might be not reliable, as explained in Table 13.

V_BCKP voltage value	RTC value reliability	Notes
1.00 V < **V_BCKP** < 1.90 V	RTC oscillator does not stop operation RTC value read after a restart of the system is reliable	**V_BCKP** within operating range
0.05 V < **V_BCKP** < 1.00 V	RTC oscillator does not necessarily stop operation RTC value read after a restart of the system is not reliable	**V_BCKP** below operating range
0.00 V < **V_BCKP** < 0.05 V	RTC oscillator stops operation RTC value read after a restart of the system is reliable	**V_BCKP** below operating range

Table 13: RTC value reliability as function of V_BCKP voltage value

Consider that the module cannot switch on if a valid voltage is not present on **VCC** even when the RTC is supplied through **V_BCKP** (meaning that **VCC** is mandatory to switch-on the module).

The RTC has very low power consumption, but is highly temperature dependent. For example at +25 °C, with the **V_BCKP** voltage equal to the typical output value, the power consumption is approximately 2 µA (see the input characteristics of supply/power pins table in the LISA-U2 series Data Sheet [1] for the detailed specification), whereas at +70 °C and an equal voltage, the power consumption increases to 5-10 µA.

☞ The internal regulator for **V_BCKP** is optimized for low leakage current and very light loads. It is not recommended to use **V_BCKP** to supply external loads.

If **V_BCKP** is left unconnected and the module main voltage supply is removed from **VCC**, the RTC is supplied from the bypass capacitor mounted inside the module. However, this capacitor is not able to provide a long buffering time: within a few milliseconds, the voltage on **V_BCKP** will drop below the valid range (1 V minimum). This has no impact on cellular connectivity, as none of the functionalities of the module rely on the date and time settings.

☞ Leave **V_BCKP** unconnected if the RTC is not required when the **VCC** supply is removed. The date and time will not be updated when **VCC** is disconnected. If **VCC** is always supplied, then the internal regulator is supplied from the main supply and there is no need for an external component on **V_BCKP**.

If RTC is required to run for a time interval of T [s] at +25 °C when **VCC** supply is removed, place a capacitor with a nominal capacitance of C [µF] at the **V_BCKP** pin. Choose the capacitor using the following formula:

C [µF] = (Current_Consumption [µA] x T [s]) / Voltage_Drop [V]

= 2.50 x T [s] for LISA-U2 series

For example, a 100 µF capacitor (such as the Murata GRM43SR60J107M) can be placed at **V_BCKP** to provide a long buffering time. This capacitor will hold **V_BCKP** voltage within its valid range for around 50 s at +25 °C, after the **VCC** supply is removed. If a very long buffering time is required, a 70 mF super-capacitor (e.g. Seiko Instruments XH414H-IV01E) can be placed at **V_BCKP**, with a 4.7 kΩ series resistor to hold the **V_BCKP** voltage within its valid range for approximately 10 hours at +25 °C, after the **VCC** supply is removed. The purpose of the series resistor is to limit the capacitor charging current due to the large capacitor specifications, and also to let a fast rise time of the voltage value at the **V_BCKP** pin after **VCC** supply has been provided. These capacitors will allow the time reference to run during battery disconnection.

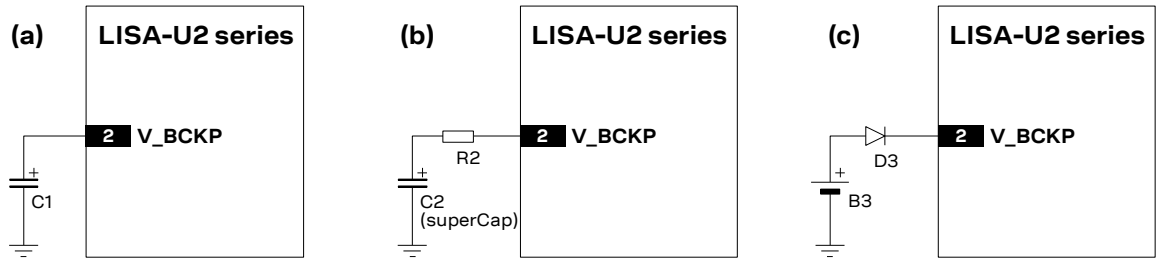


Figure 16: Real time clock supply (V_BCKP) application circuits: (a) using a 100 µF capacitor to let the RTC run for ~50 s after VCC removal; (b) using a 70 mF capacitor to let RTC run for ~10 hours after VCC removal; (c) using a non-rechargeable battery

Reference	Description	Part Number - Manufacturer
C1	100 µF Tantalum Capacitor	GRM43SR60J107M - Murata
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C2	70 mF Capacitor	XH414H-IV01E - Seiko Instruments

Table 14: Example of components for V_BCKP buffering

If longer buffering time is required to allow the time reference to run during a disconnection of the **VCC** supply, then an external battery can be connected to **V_BCKP** pin. The battery should be able to provide a proper nominal voltage and must never exceed the maximum operating voltage for **V_BCKP** (specified in the input characteristics of the supply/power pins table in the LISA-U2 series Data Sheet [1]). The connection of the battery to **V_BCKP** should be done with a suitable series resistor for a rechargeable battery, or with an appropriate series diode for a non-rechargeable battery. The purpose of the series resistor is to limit the battery charging current due to the battery specifications, and also to allow a fast rise time of the voltage value at the **V_BCKP** pin after the **VCC** supply has been provided. The purpose of the series diode is to avoid a current flow from the module **V_BCKP** pin to the non-rechargeable battery.

Combining a LISA-U2 series cellular module with a u-blox GNSS receiver, the **VCC** supply of the GNSS receiver is controlled by the cellular module by means of the “GNSS supply enable” function provided by the GPIO2 of the cellular module. In this case the **V_BCKP** supply output of the LISA-U2 series cellular module can be connected to the **V_BCKP** backup supply input pin of the GNSS receiver to provide the supply for the GNSS real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled. This enables the u-blox GNSS receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the GNSS **VCC** outage) and to maintain the configuration settings saved in the backup RAM. See the section 1.10 for more details regarding the application circuit with a u-blox GNSS receiver.

1.5.5 Interface supply (V_INT)

The same voltage domain used internally to supply the digital interfaces is also available on the **V_INT** pin. The internal regulator that generates the **V_INT** supply is a switching step down converter that is directly supplied from **VCC**. The voltage regulator output is set to 1.8 V (typical) when the module is switched on and is disabled when the module is switched off or when the **RESET_N** pin is forced the low level. The switching regulator operates in Pulse Width Modulation (PWM) for high output current mode but automatically switches to Pulse Frequency Modulation (PFM) at low output loads for greater efficiency, e.g. when the module is in idle mode between paging periods.

V_INT supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

Name	Description	Remarks
V_INT	Digital Interfaces supply output	**V_INT** = 1.8V (typical) generated by the module when it is switched-on and the **RESET_N** (external reset input pin) is not forced to the low level. **V_INT** is the internal supply for digital interfaces. The user may draw limited current from this supply rail.

Table 15: Interface supply pin

☞ The **V_INT** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the line is externally accessible on the application board. Higher protection levels can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to the accessible point.

Since it supplies internal digital circuits (see Figure 3), **V_INT** is not suited to directly supply any sensitive analog circuit: the voltage ripple can range from 15 mVpp during active mode (PWM), to 70 mVpp in idle mode (PFM).

☞ **V_INT** can be used to supply external digital circuits operating at the same voltage level as the digital interface pins, i.e. 1.8 V (typical). It is not recommended to supply analog circuitry without adequate filtering for digital noise.

☞ Do not apply loads which might exceed the limit for the maximum available current from the **V_INT** supply, as this can cause malfunctions in internal circuitry supplies to the same domain. The detailed electrical characteristics are described in the LISA-U2 series Data Sheet [1].

☞ **V_INT** can only be used as an output; do not connect any external regulator on **V_INT**. If not used, this pin should be left unconnected.

The **V_INT** digital interfaces supply output is mainly used to:

- Pull-up DDC (I^2C) interface signals (see section 1.10.2 for more details)
- Pull-up SIM detection signal (see section 1.8 for more details)
- Supply voltage translators to connect digital interfaces of the module to a 3.0 V device (see sections 1.9.2.4, 1.9.4.4 for more details)
- Supply a 1.8 V u-blox 6 or subsequent GNSS receiver (see section 1.10.2 for more details)
- Indicate when the module is switched on and the **RESET_N** external hardware reset input is not forced low (see sections 1.6.1.5, 1.6.2 and 1.6.3 for more details)

1.6 System functions

1.6.1 Module power-on

When the LISA-U2 series modules are in the not-powered mode (i.e. switched off with the **VCC** module supply not applied), they can be switched on by:

- Rising edge on the **VCC** pin to a valid voltage as the module supply (i.e. applying module supply)
- Alternately, the **RESET_N** pin can be held to the low level during the **VCC** rising edge, so that the module switches on, releasing the **RESET_N** pin when the **VCC** module supply voltage stabilizes at its correct nominal value within the normal operating range

The status of the **PWR_ON** input pin of LISA-U2 series modules while applying the **VCC** module supply is not relevant: during this phase, the **PWR_ON** pin can be set high or low by the external circuit.

When the LISA-U2 series modules are in the power-off mode (i.e. switched off by means of the AT+CPWROFF command, with valid **VCC** module supply applied), they can be switched on by:

- Low pulse on the **PWR_ON** pin (i.e. forcing the pin to the low level, normally high by external pull-up)
- Rising edge on the **RESET_N** pin (i.e. releasing the pin from low level, normally high by internal pull-up)
- RTC alarm (i.e. pre-programmed scheduled time by AT+CALA command)

Name	Description	Remarks
PWR_ON	Power-on input	**PWR_ON** pin has high input impedance. Do not keep floating in noisy environment: external pull-up required.

Table 16: Power-on pin

☞ The **PWR_ON** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the line is externally accessible on the application board. Higher protection levels can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to the accessible point.

1.6.1.1 Rising edge on VCC

Applying a proper supply to **VCC** pins, the module supply supervision circuit controls the subsequent activation of the power-up state machines: the module is switched on when the voltage rises up to the **VCC** normal operating range minimum limit starting from a voltage value lower than 2.25 V (see the LISA-U2 series Data Sheet [1] for the **VCC** normal operating range minimum limit).

☞ The voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to properly switch on the module. If the external supply circuit is not able to provide this **VCC** voltage slope, keep the **RESET_N** input low during the **VCC** rising edge, so that the module switches on, releasing the **RESET_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal operating range.

The status of the **PWR_ON** input pin during the **VCC** apply phase is not relevant: LISA-U2 modules switch on when a suitable rising edge on the **VCC** pin is applied, during this phase the **PWR_ON** pin can be set high or low by the external circuit.

1.6.1.2 Low pulse on PWR_ON

When the module is in power-off mode, i.e. it has been cleanly switched off as described in the section 1.6.2 (e.g. by the AT+CPWROFF command) and a voltage within the operating range is maintained at the **VCC** pins, the module can be switched on by means of the **PWR_ON** input pin: a falling edge must be provided on the **PWR_ON** pin, which must be then held low for an appropriate time period as specified in the LISA-U2 series Data Sheet [1].

The electrical characteristics of the **PWR_ON** input pin are different from the other digital I/O interfaces; the detailed electrical characteristics are described in the LISA-U2 series Data Sheet [1].

☞ The **PWR_ON** pin has high input impedance and is weakly pulled to the high level on the module. Avoid keeping it floating in a noisy environment. To hold the high logic level stable, the **PWR_ON** pin must be connected to a pull-up resistor (e.g. 100 kΩ) biased by the **V_BCKP** supply pin of the module.

Following are some typical examples of application circuits to turn the module on using the **PWR_ON** input pin.

Connecting the **PWR_ON** input to an external device (e.g. application processor), use an open drain output on the external device with an external pull-up resistor (e.g. 100 kΩ) biased by **V_BCKP** supply pin of the module.

A push-pull output of an application processor can also be used: in this case the pull-up can be used to pull the **PWR_ON** level high when the application processor is switched off. If the high-level voltage of the push-pull output pin of the application processor is greater than the maximum input voltage operating range of the **V_BCKP** pin (see the **V_BCKP** input characteristics of the supply/power pins table in the LISA-U2 series Data Sheet [1]), the **V_BCKP** supply cannot be used to bias the pull-up resistor: the supply rail of the application processor or the **VCC** supply could be used, but this will increase the **V_BCKP** (RTC supply) current consumption when the module is in not-powered mode (**VCC** supply not present). Using a push-pull output of the external device, take care to fix the proper level in all the possible scenarios to avoid an inappropriate switch-on of the module.

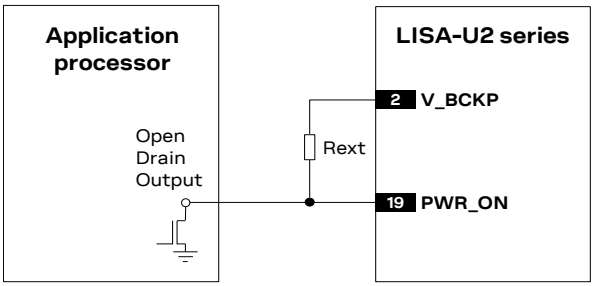


Figure 17: PWR_ON application circuits using an open drain output of an application processor

Reference	Description	Remarks
Rext	100 kΩ Resistor 0402 5% 0.1 W	External pull-up resistor

Table 17: Example of pull-up resistor for the PWR_ON application circuit

1.6.1.3 Rising edge on RESET_N

When the module is in power-off mode (i.e. switched off with **VCC** maintained), the module can be switched on by means of the **RESET_N** input pin alternatively to the **PWR_ON** input pin: the **RESET_N** signal must be forced low for at least 50 ms and then released to generate a rising edge that starts the module power-on sequence.

RESET_N input pin can also be used to perform an "external" or "hardware" reset of the module, as described in section 1.6.3.

Electrical characteristics of the LISA-U2 series **RESET_N** input are slightly different from the other digital I/O interfaces: the pin provides different input voltage thresholds. Detailed electrical characteristics are described in the LISA-U2 series Data Sheet [1].

RESET_N is pulled high to **V_BCKP** by an integrated pull-up resistor also when the module is in power-off mode. Therefore an external pull-up is not required on the application board.

The simplest way to switch on the module by means of the **RESET_N** input pin is to use a push button that shorts the **RESET_N** pin to ground: the module will be switched on at the release of the push button, since the **RESET_N** will be forced to the high level by the integrated pull-up resistor, generating a rising edge.

If **RESET_N** is connected to an external device (e.g. an application processor on an application board) an open drain output can be directly connected without any external pull-up. A push-pull output can be used too: in this case, make sure that the high level voltage of the push-pull circuit is below the maximum voltage operating range of the **RESET_N** pin (specified in the **RESET_N** pin characteristics table in the LISA-U2 series Data Sheet [1]). To avoid an unwanted power-on or reset of the module, make sure to fix the proper level at the **RESET_N** input pin in all possible scenarios.

Some typical examples of application circuits using the **RESET_N** input pin are described in section 1.6.3.

1.6.1.4 Real Time Clock (RTC) alarm

When the module is in power-off mode (i.e. switched off with **VCC** maintained), it can be switched on by means of a previously programmed RTC alarm (see the u-blox AT Commands Manual [2], AT+CALA command) alternatively to the **PWR_ON** and **RESET_N** pins: the RTC system will initiate the power-on sequence.

1.6.1.5 Additional considerations

The module is switched on when the **VCC** voltage rises up to the normal operating range (i.e. applying supply properly, as described in section 1.6.1.1): the module is commonly switched on in this way for the first time. Then, the module must be properly switched off as described in section 1.6.2, e.g. by the AT+CPWROFF command.

When the module is in power-off mode, i.e. it has been properly switched off as described in the section 1.6.2 (e.g. by the AT+CPWROFF command) and a voltage within the operating range is maintained at the **VCC** pins, the module can be switched on by a proper start-up event (i.e. by **PWR_ON** as described in Figure 18 and section 1.6.1.2, or by **RESET_N** as described in section 1.6.1.3, or by RTC alarm as described in section 1.6.1.4).

Figure 18 shows the modules power-on sequence from power-off mode, with the following phases:

- The external supply is still applied to the **VCC** inputs as it is assumed that the module has been previously switched off by means of the AT+CPWROFF command: the **V_BCKP** output is internally enabled as suitable VCC is present, the **RESET_N** is set to high logic level due to internal pull-up to **V_BCKP**, the **PWR_ON** is set to high logic level due to an external pull-up.
- The **PWR_ON** input pin is set low for a valid time period, representing the start-up event.
- All the generic digital pins of the modules are tri-stated until the switch-on of their supply source (**V_INT**): any external signal connected to the generic digital pins must be tri-stated or set low at least until the activation of the **V_INT** supply output to avoid latch-up of circuits and allow a complete boot of the module.
- The **V_INT** generic digital interfaces supply output is enabled by the integrated PMU.
- The internal reset signal is held low by the integrated power management unit: the baseband processor core and all the digital pins of the modules are held in reset state, which is reported for each pin of the module in the pin description table of the LISA-U2 series Data Sheet [1].
- When the internal reset signal is released by the integrated power management unit, the processor core starts to configure the digital pins of the modules to each default operational state.
- The duration of these pins' configuration phase differs within generic digital interfaces (3 s typical) and USB interface due to specific enumeration timings (5 s typical, see section 1.9.3.1). The host application processor should not send any AT command over the modules' AT interfaces (USB, UART) until the end of this interfaces' configuration phase to allow a complete boot of the module.
- After the interfaces' configuration phase, the application can start sending AT commands, and the following starting procedure is suggested to check the effective completion of the module internal boot sequence: send AT and wait for the response with a 30 second timeout, iterate it 4 times without resetting or removing the **VCC** supply of the module, and then run the application.

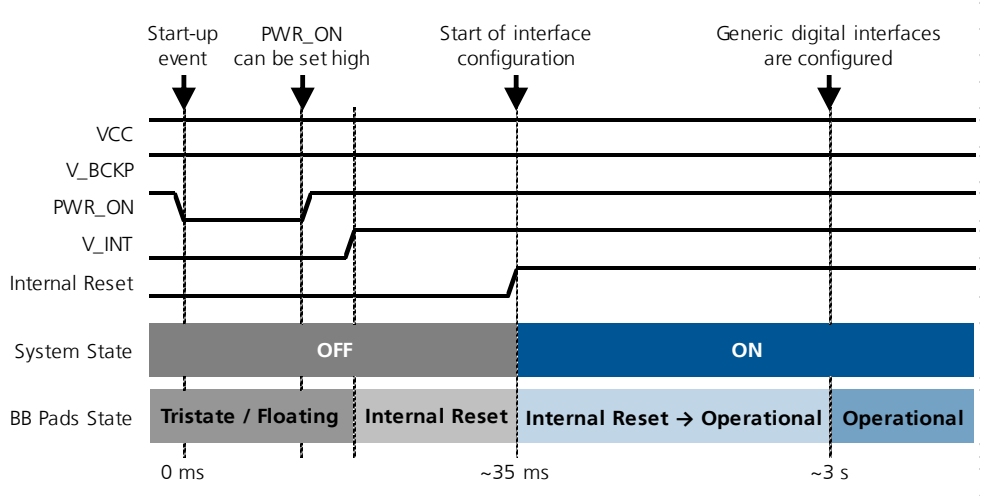


Figure 18: LISA-U2 series power-on sequence description

The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the start of the power-on sequence.

Any external signal connected to the UART interface, SPI/IPC interface, I^2S interfaces and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and let a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated, insert a multi-channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode, when the external reset is forced low, and during the power-on sequence.

1.6.2 Module power-off

The power-off sequence of LISA-U2 series modules can be correctly started, so that the current parameter settings are saved in the module's non-volatile memory and a clean network detach is performed, in one of these ways:

- AT+CPWROFF command (more details in the u-blox AT Commands Manual [2])
- Low pulse on the **PWR_ON** pin for at least 1 second

An over-temperature or an under-temperature shutdown occurs when the temperature measured within the cellular module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details, see the section 3.16 and the u-blox AT Commands Manual [2], +USTS AT command.

An abrupt under-voltage shutdown occurs on LISA-U2 modules when the **VCC** supply is removed, but in this case the current parameter settings are not saved in the module's non-volatile memory and a proper network detach cannot be performed.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply: the power-off sequence of the module must be properly started as described above (e.g. by means of the AT+CPWROFF command), and a clean **VCC** supply must be maintained at least until the end of the power-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

An abrupt hardware shutdown occurs on LISA-U2 series modules when a low level is applied to the **RESET_N** pin. In this case, the current parameter settings are not saved in the module's non-volatile memory and a clean network detach is not performed.

☞ It is highly recommended to avoid an abrupt hardware shutdown of the module by forcing a low level on the **RESET_N** input pin during module normal operation: the **RESET_N** line should be set low only if a reset or shutdown via AT commands fails or if the module does not reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [2].

Figure 19 describes the module's power-off sequence, properly started by sending the AT+CPWROFF command, allowing storage of current parameter settings in the module's non-volatile memory and a proper network detach:

- When the +CPWROFF AT command is sent, the module starts the switch-off routine.
- The module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**), except the RTC supply (**V_BCKP**).
- Then, the module remains in power-off mode as long as a switch-on event does not occur (e.g. applying a proper low level to the **PWR_ON** input, or applying a proper low level to the **RESET_N** input), and enters not-powered mode if the supply is removed from the **VCC** pins.

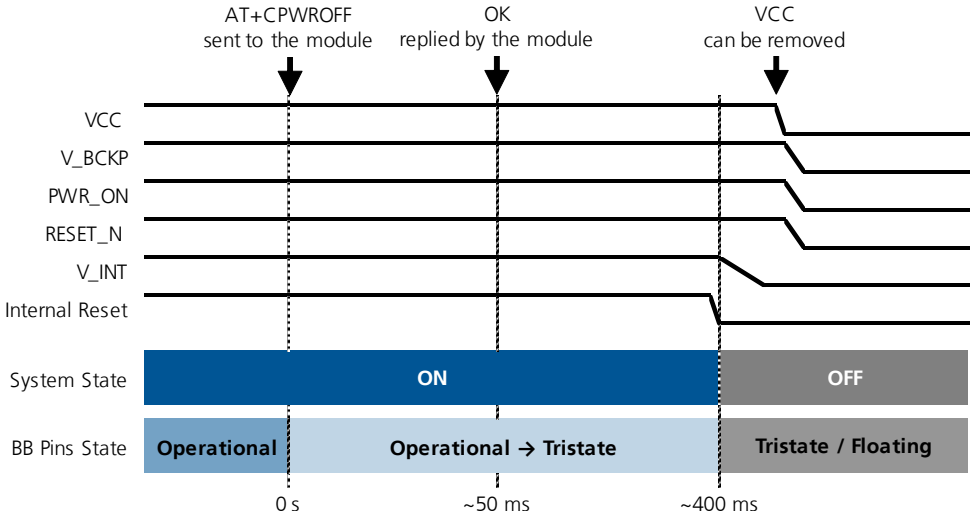


Figure 19: LISA-U2 series Power-off sequence description

☞ The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the end of the LISA-U2 series power-off sequence.

☞ The duration of each phase in the LISA-U2 series modules' switch-off routines can largely vary from the values reported in Figure 19 (e.g. from tens of milliseconds up to tens of seconds), depending on the application / network settings and the concurrent module activities.

☞ If the AT command +CPWROFF is issued to switch off the module over a multiplexer channel, the completion of the module power-off sequence could require additionally up to 2.5 seconds after the module OK reply. Therefore, if the Application Processor (AP) controls the **VCC** supply of the module, the AP should disable the multiplexer protocol and then issue the AT+CPWROFF command over the used AT interface, or otherwise the AP should issue the AT+CPWROFF command over a multiplexer channel and wait additionally 2.5 seconds after OK reception before removing the module **VCC** supply.

☞ Tri-stated pins are always subject to floating caused by noise: to prevent unwanted effects, fix them with suitable pull-up or pull down resistors to stable voltage rails to fix their level when the module is in power-down state.

☞ Any external signal connected to the UART, SPI/IPC, I^2S and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated, insert a multi-channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two circuit connections and set to high impedance during module power-down mode, when the external reset is forced low and during the power-on sequence.

1.6.3 Module reset

LISA-U2 series modules can be properly reset (rebooted) by:

- AT+CFUN command (see the u-blox AT Commands Manual [2] for more details).

This command causes an “internal” or “software” reset of the module, causing an asynchronous reset of the module baseband processor, excluding the integrated Power Management Unit and the RTC internal block. The **V_INT** interfaces supply is enabled and each digital pin is set to its internal reset state (detailed in the pin description table in the LISA-U2 series Data Sheet [1]), the **V_BCKP** supply and the RTC block are enabled.

Forcing an “internal” or “software” reset, the current parameter settings are saved in the module’s non-volatile memory and a clean network detach is performed: this is the proper way to reset the modules.

An abrupt hardware reset occurs on LISA-U2 series modules when a low level is applied on the **RESET_N** input pin for a specific time period. In this case, the current parameter settings are not saved in the module’s non-volatile memory and a clean network detach is not performed.

☞ It is highly recommended to avoid an abrupt “external” or “hardware” reset of the module by forcing a low level on the **RESET_N** input pin during the module normal operation: the **RESET_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [2].

When a low level is applied to the **RESET_N** input, it causes an “external” or “hardware” reset of the module, with an asynchronous abrupt reset of the entire module, including the integrated Power Management Unit, except for the RTC internal block. The **V_INT** interfaces supply is switched off and all the digital pins of the modules are tri-stated, but the **V_BCKP** supply and the RTC block are enabled.

Forcing an “external” or “hardware” reset, the current parameter settings are not saved in the module’s non-volatile memory and a clean network detach is not performed.

When **RESET_N** is released from the low level, the module automatically starts its power-on sequence from the reset state. The same procedure is followed for the module reset via AT command after having performed the network detach and the parameter saving in non-volatile memory.

Name	Description	Remarks
RESET_N	External reset input	Internal 10 kΩ pull-up to **V_BCKP**

Table 18: Reset pin

☞ The **RESET_N** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the line is externally accessible on the application board. Higher protection levels can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to the accessible point.

☞ For more details about **RESET_N** circuit precautions for ESD immunity, see section 2.5.3.

The electrical characteristics of **RESET_N** are different from the other digital I/O interfaces. The detailed electrical characteristics are described in the LISA-U2 series Data Sheet [1].

RESET_N is pulled high by an integrated 10 kΩ pull-up resistor to **V_BCKP**. Therefore an external pull-up is not required on the application board.

Following are some typical examples of application circuits using the **RESET_N** input pin.

The simplest way to reset the module is to use a push button that shorts the **RESET_N** pin to ground.

If **RESET_N** is connected to an external device (e.g. an application processor on an application board), an open drain output can be directly connected without any external pull-up. A push-pull output can be used too: in this case, make sure that the high level voltage of the push-pull circuit is below the maximum voltage operating range of the **RESET_N** pin (specified in the **RESET_N** pin characteristics table in the LISA-U2 series Data Sheet [1]). To avoid unwanted resets of the module, make sure to fix the proper level at the **RESET_N** input pin in all possible scenarios.

As ESD immunity test precaution, a 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JA01), a proper series chip ferrite bead noise/EMI suppression filter (e.g. Murata BLM15HD182SN1) and a 220 nF bypass capacitor (e.g. Murata GRM155R60J224KE01) must be added as close as possible to the **RESET_N** pin of LISA-U2 series modules to avoid a module reset caused by an electrostatic discharge applied to the application board (for more details, see section 2.5.3).

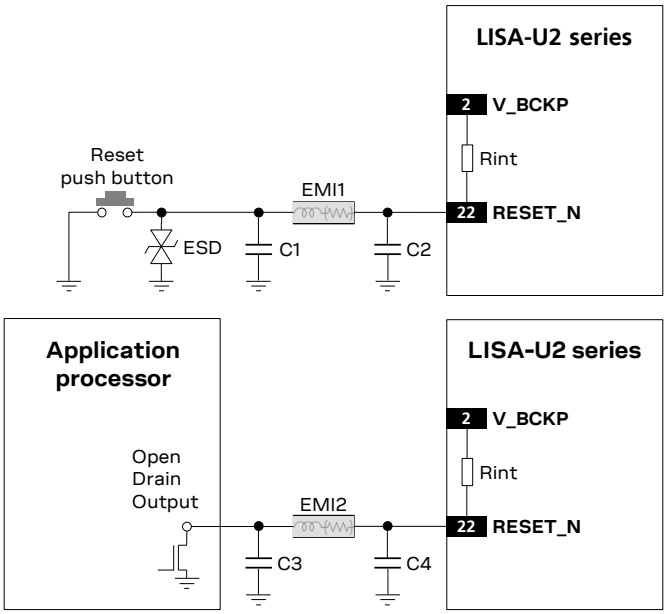


Figure 20: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection.	CT0402S14AHSG - EPCOS
C1, C3	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C2, C4	220 nF Capacitor Ceramic X5R 0402 10% 6.3 V	GRM155R60J224KE01 - Murata
EMI1, EMI2	Chip Ferrite Bead Noise/EMI Suppression Filter 1800 Ω at 100 MHz, 2700 Ω at 1 GHz	BLM15HD182SN1 - Murata
Rint	10 kΩ Resistor 0402 5% 0.1 W	Internal pull-up resistor

Table 19: Example of ESD protection components for the RESET_N application circuit

☞ Any external signal connected to the UART, SPI/IPC, I²S and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and allow a clean boot of the module. If the external signals connected to the cellular module cannot be tri-stated, insert a multi-channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power-down mode, when external reset is forced low and during the power-on sequence.

1.7 RF connection

The **ANT** pin, provided by all LISA-U2 modules, represents the main RF input/output used to transmit and receive the 2G and 3G RF signal: the main antenna must be connected to this pad. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the 2G and 3G operating bands.

The **ANT_DIV** pin, provided by LISA-U230 modules, represents the RF input for the integrated diversity receiver implemented for both 2G and 3G cases: the antenna for the Rx diversity must be connected to this pad. The **ANT_DIV** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna for the Rx diversity through a 50 Ω transmission line to allow reception of radio frequency (RF) signals, improving the cellular link quality and reliability on all 2G and 3G operating bands except the 2G DCS 1800.

Name	Module	Description	Remarks
ANT	All	RF input/output for main Tx/Rx antenna	Zo = 50 Ω nominal characteristic impedance.
ANT_DIV	LISA-U230	RF input for Rx diversity antenna	Zo = 50 Ω nominal characteristic impedance.

Table 20: Antenna pins

☞ The ESD immunity rating of the **ANT** port is 1000 V (according to IEC 61000-4-2). Higher protection level could be required if the line is externally accessible on the application board (for further details, see section 2.5.3).

Choose an antenna with optimal radiating characteristics for the best electrical performance and overall module functionality. An internal antenna, integrated on the application board, or an external antenna, connected to the application board through a suitable 50 Ω connector, can be used. See section 2.4 and section 2.2.1.1 for further details regarding antenna guidelines.

⚠ The recommendations of the antenna producer for correct installation and deployment (PCB layout and matching circuitry) must be followed.

If an external antenna is used, the PCB-to-RF-cable transition must be implemented using either a suitable 50 Ω connector, or an RF-signal solder pad (including GND) that is optimized for 50 Ω characteristic impedance.

If antenna supervisor functionality is required, the main antenna connected to the **ANT** pin should have a built-in DC diagnostic resistor to ground to achieve reliable detection functionality (see section 2.4.4).

☞ Connect the Rx diversity antenna to the **ANT_DIV** pin of LISA-U230 modules, unless the 2G and 3G Rx diversity feature is disabled by the AT command (see the u-blox AT Commands Manual [2], +URXDIV command). The same pin (74) is marked **RSVD** (reserved) on the other modules that do not implement Rx diversity: in this case the **RSVD** pin can be left unconnected.

1.8 (U)SIM interface

The high-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud rate selection, according to the values determined by the SIM card.

The **VSIM** supply output pin provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

Name	Description	Remarks
VSIM	SIM supply	1.80 V typical or 2.90 V typical Automatically generated by the module
SIM_CLK	SIM clock	3.25 MHz clock frequency
SIM_IO	SIM data	Open drain, internal 4.7 kΩ pull-up resistor to **VSIM**
SIM_RST	SIM reset	

Table 21: SIM interface pins

☞ A low capacitance (i.e. less than 10 pF) ESD protection (e.g. Infineon ESD8V0L2B-03L or AVX USB0002RP) must be placed near the SIM card holder on each line (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST**). The SIM interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F): higher protection level is required if the lines are connected to an SIM card connector, since they are externally accessible on the application board.

☞ For more details about ESD immunity precautions for SIM interface pins, see section 2.5.3.

The following SIM services are supported:

- Abbreviated Dialing Numbers (ADN)
- Fixed Dialing Numbers (FDN)
- Last Dialed Numbers (LDN)
- Service Dialing Numbers (SDN)

The SIM Application Toolkit and USIM Application Toolkit (USAT) are supported.

The **GPIO5** pin is configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin is configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if properly connected to the mechanical switch of a SIM card holder as described in section 1.8.1.4 and 1.8.1.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card not present
- High logic level at **GPIO5** input pin is recognized as SIM card present

The SIM card detection function provided by **GPIO5** pin is an optional feature that can be implemented / used or not according to the application requirements. An Unsolicited Result Code (URC) can be generated each time that there is a change of status (for more details, see the “simind” value of the <descr> parameter of +CIND and +CMER commands in the u-blox AT Commands Manual [2]).

All the LISA-U2 series modules provide the additional function “SIM card hot insertion/removal” on the **GPIO5** pin, which can be enabled using the AT+UDCONF=50 command.

For more details on SIM detection function, see section 1.12 as well as the u-blox AT Commands Manual [2], +UGPIOC, +UDCONF=50 commands.

1.8.1 (U)SIM application circuits

1.8.1.1 SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC) which contain the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the GSM network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221as follows:

- Contact C1 = VCC (Supply) → Must be connected to **VSIM**
- Contact C2 = RST (Reset) → Must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → Must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → Must be left not connected
- Contact C5 = GND (Ground) → Must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → Must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → Must be left not connected

A removable SIM card can have 6 contacts (C1 = VCC, C2 = RST, C3 = CLK, C5 = GND, C6 = VPP, C7 = I/O) or 8 contacts, providing also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses. Only 6 contacts are required and must be connected to the module SIM card interface as described above, since LISA-U2 modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Removable SIM cards are suitable for applications where SIM changing is required during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins corresponding to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided: select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without an integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contacts mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as follows:

- Package Pin 8 = UICC Contact C1 = VCC (Supply) → Must be connected to **VSIM**
- Package Pin 7 = UICC Contact C2 = RST (Reset) → Must be connected to **SIM_RST**
- Package Pin 6 = UICC Contact C3 = CLK (Clock) → Must be connected to **SIM_CLK**
- Package Pin 5 = UICC Contact C4 = AUX1 (Auxiliary contact) → Must be left not connected
- Package Pin 1 = UICC Contact C5 = GND (Ground) → Must be connected to **GND**
- Package Pin 2 = UICC Contact C6 = VPP (Programming supply) → It can be left not connected
- Package Pin 3 = UICC Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Package Pin 4 = UICC Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can also provide the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses, but only 6 contacts are required and need to be connected to the module SIM card interface as described above, since LISA-U2 modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

1.8.1.2 Single SIM card without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of LISA-U2 modules as described in Figure 21, where the optional SIM detection feature is not implemented (see the circuit described in Figure 23 if the SIM detection feature is required).

Follow these guidelines connecting the module to a SIM connector without the SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module
- Connect the UICC / SIM contact C5 (GND) to ground
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the corresponding pad of the SIM connector, to prevent digital noise
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H330J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each specific pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each specific pad of the SIM connector: the ESD sensitivity rating of the SIM interface pins is 1 kV (Human Body Model according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection levels can be required if the lines are externally accessible on the application device
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines)

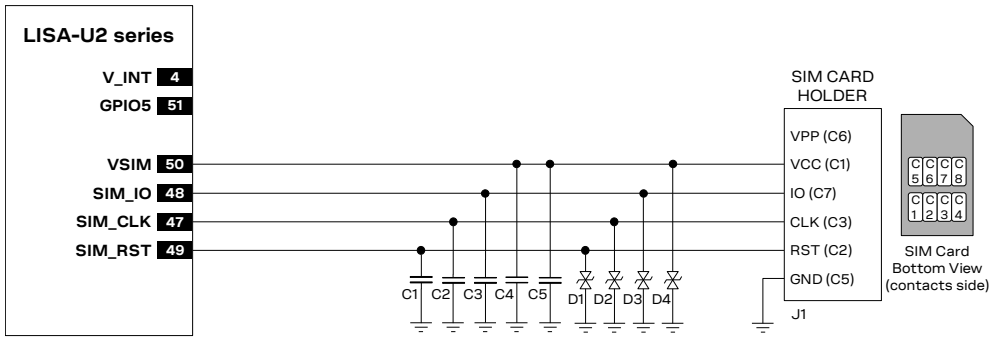


Figure 21: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	33 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol

Table 22: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

1.8.1.3 Single SIM chip

A solderable SIM chip (M2M UICC form factor) must be connected the SIM card interface of LISA-U2 modules as described in Figure 22 when the optional SIM detection feature is not implemented (see the circuit described in Figure 23 if the SIM detection feature is required).

Follow these guidelines connecting the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module
- Connect the UICC / SIM contact C5 (GND) to ground
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**) close to the specific pad of the SIM chip, to prevent digital noise
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H330J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines)

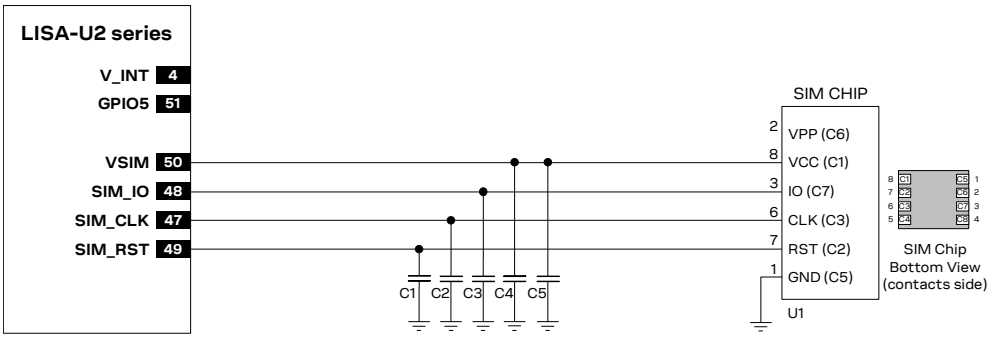


Figure 22: Application circuit for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	33 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 23: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

1.8.1.4 Single SIM card with detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of LISA-U2 modules as described in Figure 23 when the optional SIM card detection feature is implemented so that the module detects if a SIM card is present in the connector by means of the **GPIO5** signal. The SW1 and SW2 pins of the SIM card holder are connected to a normally-open mechanical switch integrated in the SIM connector. The following cases are available:

- SIM card not present: the **GPIO5** signal is forced low by the pull-down resistor connected to ground (i.e. the switch integrated in the SIM connector is open)
- SIM card present: the **GPIO5** signal is forced high by the pull-up resistor connected to **V_INT** (i.e. the switch integrated in the SIM connector is closed)

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module
- Connect the UICC / SIM contact C5 (GND) to ground
- Connect one pin of the mechanical switch integrated in the SIM connector (e.g. the SW2 pin as described in Figure 23) to the **GPIO5** input pin of the module
- Connect the other pin of the mechanical switch integrated in the SIM connector (e.g. the SW1 pin as described in Figure 23) to the **V_INT** 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 resistor in Figure 23
- Provide a weak (e.g. 470 kΩ) pull-down resistor at the SIM detection line, as the R2 resistor in Figure 23
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the specific pad of the SIM connector, to prevent digital noise
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H330J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each specific pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each specific pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (HBM as per JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection levels can be required if the lines are externally accessible on the application device
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines)

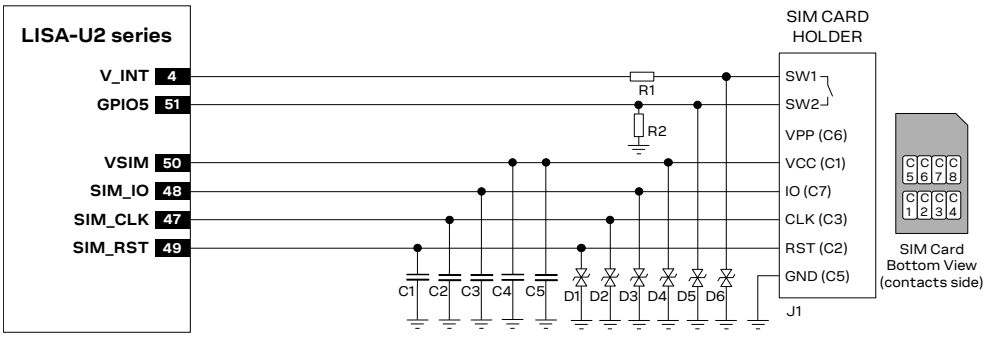


Figure 23: Application circuit for connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	33 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4, D5, D6	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM Card Holder 6 + 2 positions, with card presence switch	Various Manufacturers, CCM03-3013LFT R102 - C&K Components

Table 24: Example of components for connection to a single removable SIM card, with SIM detection implemented

1.8.1.5 Dual SIM card connection

Two SIM cards / chips can be connected to the module's SIM interface, as described in the circuit of Figure 24.

LISA-U2 modules do not support the usage of two SIMs at the same time, but two SIMs can be populated on an application board that provides a suitable switch to connect only the first SIM or only the second SIM per time to the SIM interface of the modules as described in Figure 24.

All LISA-U2 series modules support SIM hot insertion / removal on the **GPIO5** pin: if the feature is enabled using the specific AT commands, the switch from first SIM to the second SIM can be cleanly done when a Low logic level is present on the **GPIO5** pin ('SIM not inserted' = SIM interface not enabled), without the necessity of a module re-boot, so that the SIM interface will be re-enabled by the module to use the second SIM when a High logic level will be re-applied on the **GPIO5** pin. (For more details, see section 1.12 and the u-blox AT Commands Manual [2], +UGPIOC, +UDCONF=50 commands.)

In the application circuit represented in Figure 24, the application processor will drive the SIM switch using its own GPIO to properly select the SIM that is used by the module. Another GPIO may be used to handle the SIM hot insertion / removal function of LISA-U2 series modules, which can also be handled by other external circuits or by the cellular module GPIO according to the application requirements.

The dual SIM connection circuit described in Figure 24 can be implemented for SIM chips as well, providing proper connection between SIM switch and SIM chip as described in Figure 22.

If it is required to switch between more than two SIMs, a circuit similar to the one described in Figure 24 can be implemented: for example, in case of four SIM circuits, using a suitable 4-pole 4-throw switch (or, alternatively, four 1-pole 4-throw switches) instead of the suggested 4-pole 2-throw switch.

Follow these guidelines connecting the module to two SIM connectors:

- Use a suitable low-on resistance (i.e. few ohms) and low-on capacitance (i.e. few pF) 2-throw analog switch (e.g. Fairchild FSA2567) as SIM switch to ensure high-speed data transfer according to the SIM requirements.
- Connect the contacts C1 (VCC) of the two UICC / SIM to the **VSIM** pin of the module by means of a suitable 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C7 (I/O) of the two UICC / SIM to the **SIM_IO** pin of the module by means of a suitable 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C3 (CLK) of the two UICC / SIM to the **SIM_CLK** pin of the module by means of a suitable 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C2 (RST) of the two UICC / SIM to the **SIM_RST** pin of the module by means of a suitable 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C5 (GND) of the two UICC / SIM to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the two SIM connectors, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the two SIM connectors, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holders.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the two SIM connectors, according to the EMC/ESD requirements of the custom application.
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines).

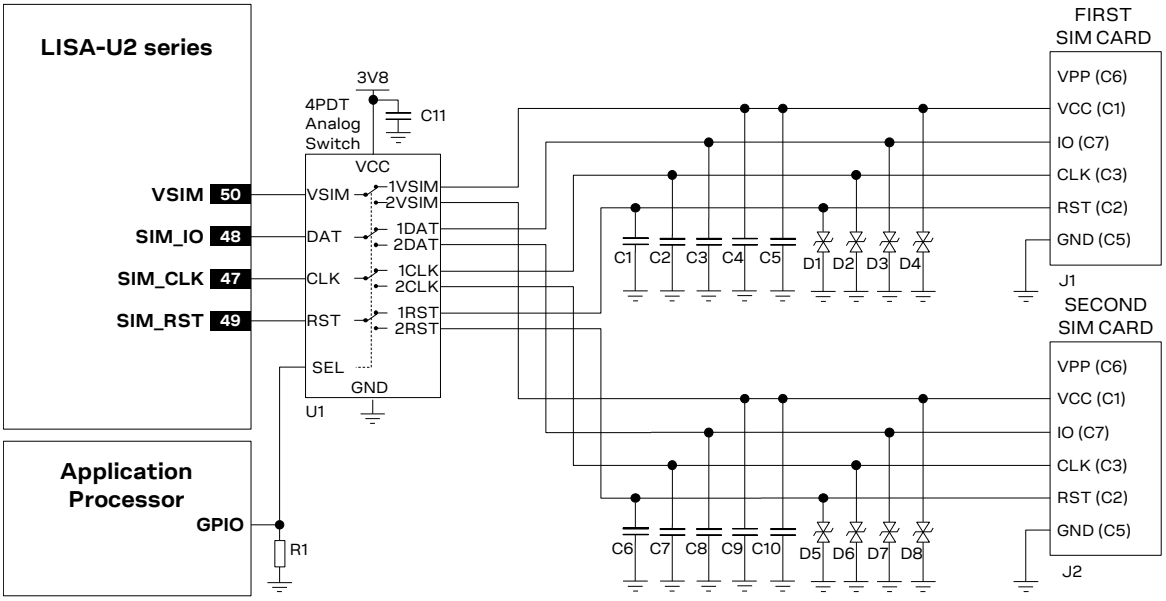


Figure 24: Application circuit for connection to two removable SIM cards, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1 – C4, C6 – C9	33 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5, C10, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D8	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL- Yageo Phycomp
J1, J2	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol
U1	4PDT Analog Switch, with Low On-Capacitance and Low On-Resistance	FSA2567 - Fairchild Semiconductor

Table 25: Example of components for connection to two removable SIM cards, with SIM detection implemented

1.9 Serial communication

LISA-U2 modules provide the following serial communication interfaces where the AT command interface and Packet-Switched / Circuit-Switched Data communication are concurrently available:

- One asynchronous serial interface (UART) that provides complete RS-232 functionality conforming to the ITU-T V.24 Recommendation [3], with a limited data rate
- One Inter Processor Communication (IPC) interface that includes a synchronous SPI-compatible interface, with a maximum data rate of 26 Mbit/s
- One high-speed USB 2.0 compliant interface, with a maximum data rate of 480 Mbit/s.

The LISA-U2 modules are designed to operate as an HSPA cellular modem, which represents a data circuit-terminating equipment (DCE) as described by the ITU-T V.24 Recommendation [3]. A customer application processor connected to the module through one of the interfaces represents the data terminal equipment (DTE).

All the interfaces listed above are controlled and operated with:

- AT commands according to 3GPP TS 27.007 [4]
- AT commands according to 3GPP TS 27.005 [5]
- AT commands according to 3GPP TS 27.010 [6]
- u-blox AT commands

☞ For the complete list of supported AT commands and their syntax, see the u-blox AT Commands Manual [2].

The module firmware can be upgraded over all the serial interfaces listed above by means of an AT command (for more details, see section 3.1 as well as the u-blox AT Commands Manual [2], +UFWUPD command).

The module firmware can be upgraded over the following serial interfaces using the u-blox EasyFlash tool:

- The UART interface (only the **RxD** and **TxD** lines are needed)
- The USB interface (all the provided lines **VUSB_DET**, **USB_D+** and **USB_D-** are needed)

☞ To directly enable PC (or similar) connection to the module for firmware upgrade using the u-blox EasyFlash tool, provide direct access on the application board to the **VUSB_DET**, **USB_D+** and **USB_D-** lines of the module (or to the **RxD** and **TxD** lines). Also provide access to the **PWR_ON** or the **RESET_N** pins, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade (see the Firmware Update Application Note [16]).

The following sub-sections describe the serial interfaces configuration and provide a detailed description of each interface for the application circuits.

1.9.1 Serial interfaces configuration

UART, USB and SPI/IPC serial interfaces are available through the AT command interface and for Packet-Switched / Circuit-Switched Data communication. The serial interfaces are configured as described in Table 26 (for information about further settings, see the u-blox AT Commands Manual [2]).

Interface	AT Settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1 – 5: AT commands / data connection • Channel 6: GNSS tunneling • Channel 7: SAP (SIM Access Profile)
	AT+IPR=0	One-shot autobauding enabled by default
	AT+ICF=0	One-shot frame format recognition enabled by default
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode[5]
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command mode and issues an OK result code[5]
	AT&C1	Circuit 109 changes in accordance with the carrier detect status; ON if the carrier is detected, OFF otherwise
USB interface	Enabled	6 CDCs are available, configured as described in the following list: • USB1: AT commands / data connection • USB2: AT commands / data connection • USB3: AT commands / data connection • USB4: GPS tunneling • USB5: Primary TraceLog • USB6: Secondary TraceLog • USB7: SAP (SIM Access Profile)
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode[5]
	AT&D1	Upon an ON-to-OFF transition of the DTR, the DCE enters online command mode and issues an OK result code[5]
	AT&C1	Circuit 109 changes in accordance with the carrier detect status; ON if the carrier is detected, OFF otherwise
SPI interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1 – 5: AT commands / data connection • Channel 6: GNSS tunneling • Channel 7: SAP (SIM Access Profile)
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode[5]
	AT&D1	Upon an ON-to-OFF transition of the DTR, the DCE enters online command mode and issues an OK result code[5]
	AT&C1	Circuit 109 changes in accordance with the carrier detect status; ON if the carrier is detected, OFF otherwise

Table 26: Default serial interfaces configuration

[5] Refer to the u-blox AT Commands Manual [2] for the definition of the interface data mode, command mode and online command mode.

1.9.2 Asynchronous serial interface (UART)

The UART interface is a 9-wire unbalanced asynchronous serial interface that provides AT commands interface, PSD and CSD data communication.

The module firmware can be upgraded over the UART interface using the u-blox EasyFlash tool or by means of an AT command (for more details, see section 3.1 and Firmware update application note [16]).

UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation (more details available in ITU Recommendation [3]), with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state. For detailed electrical characteristics see LISA-U2 series Data Sheet [1].

The LISA-U2 modules are designed to operate as an HSPA cellular modem, which represents the data circuit-terminating equipment (DCE) as described by the ITU-T V.24 Recommendation [3]. A customer application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ The signal names of the LISA-U2 modules UART interface conform to the ITU-T V.24 Recommendation [3].

UART interfaces include the following lines:

Name	Description	Remarks
DSR	Data set ready	Module output Circuit 107 (Data set ready) in ITU-T V.24
RI	Ring Indicator	Module output Circuit 125 (Calling indicator) in ITU-T V.24
DCD	Data carrier detect	Module output Circuit 109 (Data channel received line signal detector) in ITU-T V.24
DTR	Data terminal ready	Module input Circuit 108/2 (Data terminal ready) in ITU-T V.24 Internal active pull-up to **V_INT** (1.8 V) enabled.
RTS	Ready to send	Module hardware flow control input Circuit 105 (Request to send) in ITU-T V.24 Internal active pull-up to **V_INT** (1.8 V) enabled.
CTS	Clear to send	Module hardware flow control output Circuit 106 (Ready for sending) in ITU-T V.24
TxD	Transmitted data	Module data input Circuit 103 (Transmitted data) in ITU-T V.24 Internal active pull-up to **V_INT** (1.8 V) enabled.
RxD	Received data	Module data output Circuit 104 (Received data) in ITU-T V.24
GND	Ground	

Table 27: UART interface signals

☞ The UART interface pins' ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the lines are externally accessible on the application board. Higher protection levels can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins, close to the accessible points.

1.9.2.1 UART features

All flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see the u-blox AT Commands Manual [2], &K, +IFC, \Q AT commands): hardware flow control (RTS/CTS), software flow control (XON/XOFF), or none flow control.

☞ Hardware flow control is enabled by default.

One-shot autobauding is supported: the baud rate detection is performed once, at module start-up. Then the module works at the fixed baud rate (the detected one) and the baud rate can only be changed via the appropriate AT command (+IPR, for more details, see the u-blox AT Commands Manual [2]). In particular:

- If automatic baud rate detection is configured in the active memory profile, the baud rate is detected once at the module power-on
- The factory-programmed setting enables the automatic baud rate detection (<rate> value is 0)

Since autobauding is implemented as “one shot” autobauding, any setting of +IPR=0 should be avoided; the only exception is if the baud rate is fixed in the stored NVRAM profile. In this case, the module starts without autobauding and the host needs to reactivate it.

If the system starts in autobauding (i.e. the +IPR is 0), the first “at” sequence provided to the module detects the baud rate. For example the first command sent from the DTE at any rate can be: AT+CPIN="1234".Characters different than “AT” are ignored during the baud rate detection since the “at” or “AT” sequence triggers the hardware detection sequence. “At” or “aT” sequences are invalid: the two detection characters must be both lowercase or uppercase.

The module generates a response once autobauding detection is successful, the command is accepted and the command response is available. Therefore, even if the detection was previously successful, it is only possible to assume that the detection phase was successful after a response.

If the DTE does not receive any response after some time, it must retry (the timeout value should be adjustable inside the DTE application). In any case, use a very simple command as the first command, for which the execution time is short and almost constant (e.g. ATE). Note that the only way to recover from a detection failure is the detection reattempt, since the AT interface is only available after a successful detection.

☞ One-shot autobauding is enabled by factory programmed setting.

☞ The only way to recover from a detection failure is the detection reattempt, since the AT interface is only available after a successful detection.

The following baud rates can be configured by AT command:

- 1200 bit/s
- 2400 bit/s
- 4800 bit/s
- 9600 bit/s
- 19200 bit/s
- 38400 bit/s
- 57600 bit/s
- 115200 bit/s, default value when the one-shot autobauding is disabled
- 230400 bit/s
- 460800 bit/s
- 921600 bit/s

☞ 460800 bit/s and 921600 bit/s baud rates cannot be automatically detected by one-shot autobauding.

One-shot automatic frame recognition is supported and enabled in conjunction with the one-shot automatic baud rate detection only: when the one-shot autobauding is active, the one-shot automatic frame recognition is enabled overruling the frame format setting. The frame format recognition is performed once and then, after the successful recognition of the frame format, the automatic frame recognition is disabled, as the automatic baud rate detection.

☞ One-shot automatic frame recognition is enabled by default as the one-shot autobauding.

The following frame formats can be configured by AT command:

- 8N1 (8 data bits, no parity, 1 stop bit), default frame configuration with fixed baud rate
- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 8N2 (8 data bits, no parity, 2 stop bits)
- 7E1 (7 data bits, even parity, 1 stop bit)
- 7O1 (7 data bits, odd parity, 1 stop bit)

☞ The 8N2 frame format cannot be automatically detected by one-shot automatic frame recognition.

The 8N1 frame format, which is the default configuration with a fixed baud rate, is described in Figure 25.

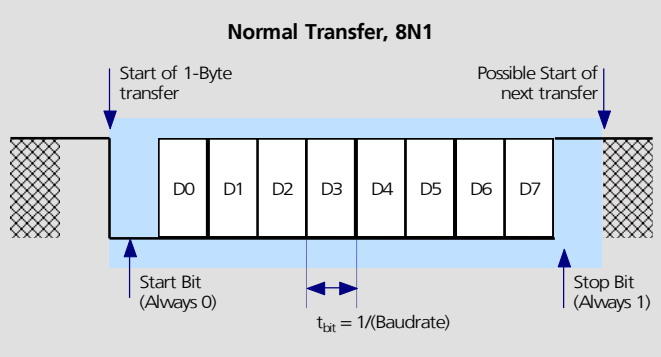


Figure 25: Description of the UART default frame format (8N1) with a fixed baud rate

1.9.2.2 UART signal behavior

See Table 5 for a description of operating modes and states referred to in this section.

At the switch-on of the module, before the initialization of the UART interface as described in the power-on sequence detailed in Figure 18, each pin is first tri-stated and then is set to its specific internal reset state that is reported in the pin description table in the LISA-U2 series Data Sheet [1]. At the end of the boot sequence, the UART interface is initialized, the module is by default in active mode and the UART interface is enabled. The configuration and the behavior of the UART signals after the boot sequence are described below.

☞ For a complete description of data and command mode, see the u-blox AT Commands Manual [2].

RxD signal behavior

The module data output line (**RxD**) is set by default to OFF state (high level) at UART initialization. The module holds **RxD** in OFF state until no data is transmitted by the module.

TxD signal behavior

The module data input line (**TxD**) is set by default to OFF state (high level) at UART initialization. The **TxD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TxD** input.

CTS signal behavior

The module hardware flow control output (**CTS** line) is set to the ON state (low level) at UART initialization.

If the hardware flow control is enabled, as it is by default, the **CTS** line indicates when the UART interface is enabled (data can be sent and received). The module drives the **CTS** line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE over the UART (see 1.9.2.3 for more details).

☞ If hardware flow control is enabled, then when the **CTS** line is OFF it does not necessarily mean that the module is in low-power idle mode, but only that the UART is not enabled, as the module could be forced to stay in active mode for other activities, e.g. related to the network or related to other interfaces.

☞ When the multiplexer protocol is active, the **CTS** line state is mapped to the FCon / FCoff MUX command for flow control issues outside the power saving configuration, while the physical **CTS** line is still used as a power state indicator. For more details, see the Mux Implementation Application Note [14].

The **CTS** hardware flow control setting can be configured by AT commands (for more details, see the u-blox AT Commands Manual [2], AT&K, AT\Q, AT+IFC, AT+UCTS AT command).

If the hardware flow control is not enabled, the **CTS** line after the UART initialization behaves as follows:

- on LISA-U2 modules "01", "x2", "63" and "68" product versions, the **CTS** line is always held in the ON state
- on LISA-U2 modules "03" product version onward, the **CTS** line is by default set in the ON state, but can be configured in the OFF state by the AT+UCTS command

☞ When the power saving configuration is enabled and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in the low-power idle mode will not be a valid communication character (see 1.9.2.3 for more details).

RTS signal behavior

The hardware flow control input (**RTS** line) is set by default to the OFF state (high level) at UART initialization. The **RTS** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **RTS** input.

If the HW flow control is enabled (for more details, see the u-blox AT Commands Manual [2] AT&K, AT\Q, AT+IFC command description) the **RTS** line is monitored by the module to detect permission from the DTE to send data to the DTE itself. If the **RTS** line is set to OFF state, any on-going data transmission from the module is immediately interrupted or any subsequent transmission forbidden until the **RTS** line changes to ON state.

☞ The DTE must be able to still accept a certain number of characters after the **RTS** line has been set to OFF state: the module guarantees the transmission interruption within 2 characters from **RTS** state change.

If AT+UPSV=2 is set and HW flow control is disabled, the **RTS** line is monitored by the module to manage the power saving configuration:

- When an OFF-to-ON transition occurs on the **RTS** input line, the UART is enabled and the module is forced to active mode: after 20 ms from the transition the switch is completed and data can be received without loss. The module cannot enter idle mode and the UART is kept enabled as long as the **RTS** input line is held in the ON state
- If **RTS** is set to OFF state by the DTE, the UART is immediately disabled (held in low-power mode) and the module automatically enters idle mode whenever possible

For more details on the power saving configuration controlled by the **RTS** input line see section 1.9.2.3 and the u-blox AT Commands Manual [2], AT+UPSV command.

DSR signal behavior

If AT&S0 is set, the **DSR** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&S1 is set, the **DSR** module output line is set by default to OFF state (high level) at UART initialization. The **DSR** line is then set to the OFF state when the module is in command mode or in online command mode and is set to the ON state when the module is in data mode (see the u-blox AT Commands Manual [2] for the definition of the interface data mode, command mode and online command mode).

☞ The above behavior is valid for both Packet-Switched and Circuit-Switched data transfers.

DTR signal behavior

The **DTR** module input line is set by default to OFF state (high level) at UART initialization. The **DTR** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **DTR** input. Module behavior according to **DTR** status depends on the AT command configuration (see the u-blox AT Commands Manual [2], &D AT command).

Except for “01” product version, if AT+UPSV=3 is set, the **DTR** line is monitored by the module to manage the power saving configuration:

- When an OFF-to-ON transition occurs on the **DTR** input line, the UART is enabled and the module is forced to active mode: after 20 ms from the transition, the switch is completed and data can be received without loss. The module cannot enter idle mode and the UART is keep enabled as long as the **DTR** input line is held in the ON state
- If **DTR** is set to OFF state by the DTE, the UART is immediately disabled (held in low-power mode) and the module automatically enters idle mode whenever possible

For more details on the power saving configuration controlled by the **DTR** input line, see section 1.9.2.3 and the u-blox AT Commands Manual [2], AT+UPSV command.

DCD signal behavior

If AT&C0 is set, the **DCD** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&C1 is set, the **DCD** module output line is set by default to OFF state (high level) at UART initialization. The **DCD** line is then set by the module in accordance with the carrier detect status: ON if the carrier is detected, OFF otherwise. For a voice call, **DCD** is set to ON state when the call is

established. For a data call there are the following scenarios (see the u-blox AT Commands Manual [2] for the definition of the interface data mode, command mode and online command mode):

- **PSD data call**: Before activating the PPP protocol (data mode) a dial-up application must provide the ATD*99***<context_number># to the module: with this command the module switches from command mode to data mode and can accept PPP packets. The module sets the **DCD** line to the ON state, then answers with a CONNECT to confirm the ATD*99 command. The **DCD** ON is not related to the context activation but with the data mode.
- **CSD data call**: To establish a data call, the DTE can send the ATD<number> command to the module which sets an outgoing data call to a remote modem (or another data module). Data can be transparent (non-reliable) or non-transparent (with the reliable RLP protocol). When the remote DCE accepts the data call, the module **DCD** line is set to ON and the CONNECT <communication baudrate> string is returned by the module. At this stage, the DTE can send characters through the serial line to the data module which sends them through the network to the remote DCE attached to a remote DTE.

☞ For a voice call, **DCD** is set to ON state on all the serial communication interfaces supporting the AT command interface (including MUX virtual channels, if active).

☞ **DCD** is set to ON during the execution of a command that requires input data from the DTE (all the commands where a prompt is issued; see AT commands +CMGS, +CMGW, +USOWR, +USODL, +UDWNFILE in the u-blox AT Commands Manual [2]). The **DCD** line is set to ON state as soon as the switch to binary/text input mode is completed and the prompt is issued; **DCD** line is set to OFF as soon as the input mode is interrupted or completed.

☞ **DCD** line is kept to ON state even during the online command mode to indicate that the data call is still established even if suspended, while if the module enters command mode, the **DSR** line is set to OFF state. For more details, see the **DSR** signal behavior description.

☞ For scenarios where the **DCD** line setting is requested for various reasons (e.g. SMS texting during online command mode), the **DCD** line changes to guarantee the correct behavior for all the scenarios. For instance, in case of SMS texting in online command mode, if the data call is released, the **DCD** line will be kept to ON until the SMS command execution is completed (even if the data call release would request the **DCD** setting to OFF).

RI signal behavior

The **RI** module output line is set by default to the OFF state (high level) at UART initialization. Then, during an incoming call, the **RI** line is switched from OFF state to ON state with a 4:1 duty cycle and a 5 second period (ON for 1 second, OFF for 4 seconds, see Figure 26), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

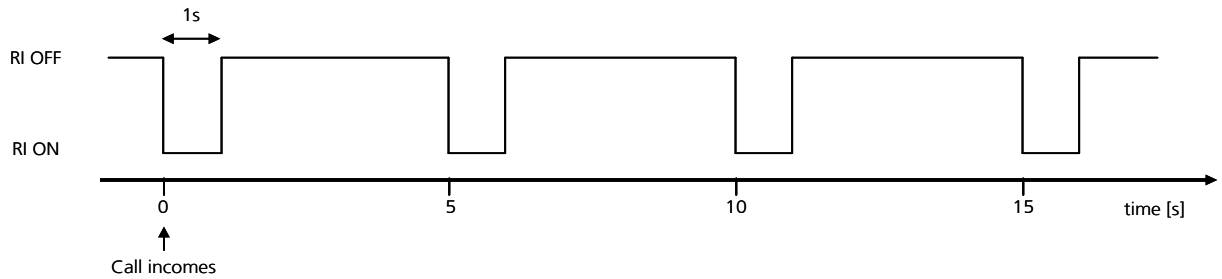


Figure 26: RI behavior during an incoming call

The **RI** line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 27), if the feature is enabled by the appropriate AT command (see the u-blox AT Commands Manual [2], AT+CNMI command).

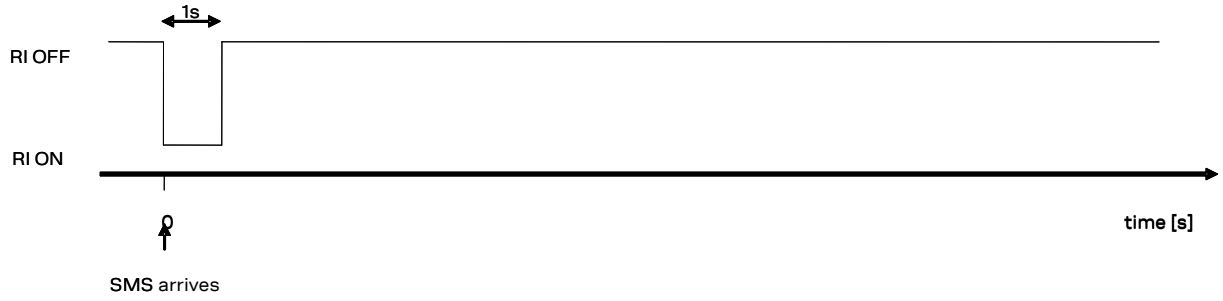


Figure 27: RI behavior at SMS arrival

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.
In case of SMS arrival, if several events occur coincidently or in quick succession each event triggers the **RI** line independently, although the line will not be deactivated between each event. As a result, the **RI** line may stay ON for more than 1 second.

If an incoming call is answered within less than 1 second (with ATA or if auto-answering is set to ATS0=1), then the **RI** line will be set to OFF earlier.

As a result:

- **RI** line monitoring cannot be used by the DTE to determine the number of received SMSs.
- In case of multiple events (incoming call plus SMS received), the **RI** line cannot be used to discriminate the two events, but the DTE must rely on the subsequent URCs and interrogate the DCE with the appropriate commands.

The **RI** line can additionally notify all the URCs and all the incoming data (PPP, Direct Link, sockets, FTP) on all LISA-U2 series modules except for the "01" product version, if the feature is enabled by the proper AT command (see the u-blox AT Commands Manual [2], AT+URING command): the **RI** line is asserted when one of the configured events occur and it remains asserted for 1 second unless another configured event will happen, with the same behavior described in Figure 27.

1.9.2.3 UART and power-saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description see the u-blox AT Commands Manual [2]). When power saving is enabled, the module automatically enters low-power idle mode whenever possible; otherwise the active mode is maintained by the module (see section 1.4 for the definition and description of module operating modes).

The AT+UPSV command configures both the module power saving and also the UART behavior in relation to the power saving. The conditions for the module entering idle mode also depend on the UART power saving configuration.

The AT+UPSV command can set these different power saving configurations:

- AT+UPSV=0, power saving disabled: module forced to active mode and UART interface enabled (default)
- AT+UPSV=1, power saving enabled: module cyclic active / idle mode and UART enabled / disabled
- AT+UPSV=2, power saving enabled and controlled by the UART **RTS** input line
- AT+UPSV=3, power saving enabled and controlled by the UART **DTR** input line

☞ The AT+UPSV=3 power saving configuration is not supported by the “01” product version.

The different power saving configurations that can be set by the +UPSV AT command are described in detail in the following subsections. The UART interface communication behaviors for the different power saving configurations, in relation to the HW flow control settings and **RTS** input line status, are summarized in Table 28. For more details on the +UPSV AT command description, see the u-blox AT commands Manual [2].

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle mode and wake-up
0	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE.
0	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when RTS is set to ON. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. RTS line will be ON).
0	Disabled (AT&K0)	ON or OFF	ON or OFF	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise the data is lost.
1	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when active mode is entered. Data sent by the module is correctly received by the DTE.
1	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE is buffered by the DTE and will be correctly received by the module when active mode is entered. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. RTS line will be ON).
1	Disabled (AT&K0)	ON or OFF	ON or OFF	The first character sent by the DTE is lost, but after ~20 ms the UART and the module are waked up: recognition of subsequent characters is guaranteed after the complete UART / module wake-up. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
2	Enabled (AT&K3)	ON or OFF	ON or OFF	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	ON or OFF	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
2	Disabled (AT&K0)	OFF	ON or OFF	Data sent by the DTE is lost by LISA-U2 modules. The first character sent by the DTE is lost by LISA-U2 modules, but after ~20 ms the UART and the module are waked up: recognition of subsequent characters is guaranteed after the complete UART / module wake-up. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
3	Enabled (AT&K3)	ON	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE.
3	Enabled (AT&K3)	ON	OFF	Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE.
3	Enabled (AT&K3)	OFF	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. RTS line will be ON).
3	Enabled (AT&K3)	OFF	OFF	Data sent by the DTE is lost by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. RTS line will be ON).

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle mode and wake-up
3	Disabled (AT&K0)	ON or OFF	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
3	Disabled (AT&K0)	ON or OFF	OFF	Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.

Table 28: UART and power-saving summary

AT+UPSV=0: power saving disabled, fixed active mode

The module does not enter idle mode and the UART interface is enabled (data can be sent and received): the **CTS** line is always held in the ON state after UART initialization. This is the default configuration.

AT+UPSV=1: power saving enabled, cyclic idle/active mode

When the DTE issues the AT+UPSV=1 command, the UART is immediately disabled.

Afterwards, the UART of LISA-U2 series modules is periodically enabled to receive or send data and, if data has not been received or sent over the UART, the interface is automatically disabled whenever possible according to the timeout configured by the second parameter of the +UPSV AT command.

The module automatically enters the low-power idle mode whenever possible but it wakes up to active mode according to the UART periodic wake-up so that the module cycles between the low-power idle mode and the active mode. Additionally, the module wakes up to active mode according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The UART is enabled, and the module does not enter low-power idle mode, in the following cases:

- During the periodic UART wake-up to receive or send data
- If the module needs to transmit some data over the UART (e.g. URC)
- If a character is sent by the DTE with HW flow control disabled, the first character sent causes the system wake-up due to the “wake-up via data reception” feature described in the following subsection, and the UART will be then kept enabled after the last data received according to the timeout set by the second parameter of the AT+UPSV=1 command

The module, outside an active call, periodically wakes up from idle mode to active mode to monitor the paging channel of the current base station (paging block reception), according to the 2G or 3G discontinuous reception (DRX) specifications.

The time period between two paging receptions is defined by the current base station (i.e. by the network):

- If the module is registered with a 2G network, the paging reception period can vary from ~0.47 s (DRX = 2, i.e. 2 x 51 2G-frames) up to ~2.12 s (DRX = 9, i.e. 9 x 51 2G-frames)
- If the module is registered with a 3G network, the paging reception period can vary from 0.64 s (DRX = 6, i.e. 2^6 3G-frames) up to 5.12 s (DRX = 9, i.e. 2^9 3G-frames)

The time period of the UART enable/disable cycle is configured differently when the module is registered with a 2G network compared to when the module is registered with a 3G network:

- 2G: the UART is enabled concurrently to a paging reception, and then, as data has not been received or sent, the UART is disabled until the first paging reception that occurs after a timeout of 2.0 s, and afterwards the interface is enabled again

- 3G: the UART is asynchronously enabled to paging receptions, as the UART is enabled for ~20 ms, and then, if data are not received or sent, the UART is disabled for 2.5 s, and afterwards the interface is enabled again
- Not registered: when a module is not registered with a network, the UART is enabled for ~20 ms, and then, if data has not been received or sent, the UART is disabled for 2.5 s and afterwards the interface is enabled again

The module active mode duration outside an active call depends on:

- Network parameters, related to the time interval for the paging block reception (minimum of ~11 ms)
- Duration of UART enable time in absence of data reception (~20 ms)
- The time period from the last data received at the serial port during the active mode: the module does not enter idle mode until a timeout expires. The second parameter of the +UPSV AT command configures this timeout, from 40 2G-frames (i.e. 40 x 4.615 ms = 184 ms) up to 65000 2G-frames (i.e. 65000 x 4.615 ms = 300 s). The default value is 2000 2G-frames (i.e. 2000 x 4.615 ms = 9.2 s)
- The active mode duration can be extended indefinitely since every subsequent character received during the active mode will reset and restart the timer.
- The timeout is ignored immediately after AT+UPSV=1 has been sent, so that the UART interface is disabled and the module may enter idle mode immediately after the AT+UPSV=1 has been sent

The hardware flow-control output (**CTS** line) indicates when the UART interface is enabled (data can be sent and received over the UART), if HW flow control is enabled, as illustrated in Figure 28.

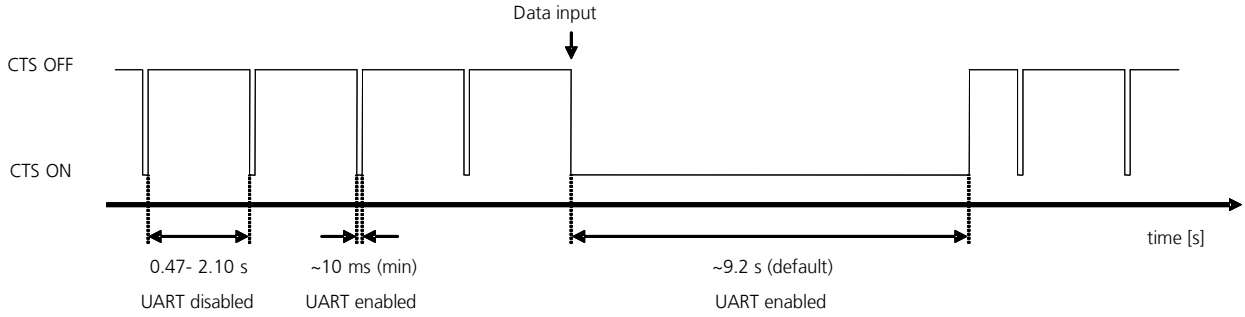


Figure 28: CTS behavior with power saving enabled (AT+UPSV=1) and HW flow control enabled: the CTS output line indicates when the UART interface of the module is enabled (CTS = ON = low level) or disabled (CTS = OFF = high level)

AT+UPSV=2: power saving enabled and controlled by the RTS line

This configuration can only be enabled with the module hardware flow control disabled by AT&K0 command.

The UART interface is immediately disabled after the DTE sets the **RTS** line to OFF.

Then the module automatically enters idle mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The UART is disabled as long as the **RTS** line is held to OFF, but the UART is enabled in case the module needs to transmit some data over the UART (e.g. URC).

When an OFF-to-ON transition occurs on the **RTS** input line, the UART is re-enabled and the module, if it was in idle mode, switches from idle to active mode after ~20 ms: this is the UART and module "wake-up time".

If the **RTS** line is set to ON by the DTE, the module is not allowed to enter the low-power idle mode and the UART is kept enabled.

AT+UPSV=3: power saving enabled and controlled by the DTR line

The AT+UPSV=3 configuration can be enabled regardless of the flow control setting on UART. In particular, the HW flow control can be enabled (AT&K3) or disabled (AT&K0) on UART during this configuration.

The UART interface is immediately disabled after the DTE sets the **DTR** line to OFF.

Then the module automatically enters idle mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The UART is disabled as long as the **DTR** line is set to OFF, but the UART is enabled in case the module needs to transmit some data over the UART (e.g. URC).

When an OFF-to-ON transition occurs on the **DTR** input line, the UART is re-enabled and the module, if it was in idle mode, switches from idle to active mode after 20 ms: this is the UART and module "wake-up time".

If the **DTR** line is set to ON by the DTE, the module is not allowed to enter idle mode and the UART is kept enabled until the **DTR** line is set to OFF.

When the AT+UPSV=3 configuration is enabled, the **DTR** input line can still be used by the DTE to control the module behavior according to AT&D command configuration (see u-blox AT Commands Manual [2]).

☞ The **CTS** output line indicates the UART power saving state as illustrated in Figure 28, if HW flow control is enabled with AT+UPSV=3.

☞ The AT+UPSV=3 power saving configuration is not supported by the "01" product version.

Wake-up via data reception

The UART wake-up via data reception consists of a special configuration of the module **TXD** input line that causes the system wake-up when a low-to-high transition occurs on the **TXD** input line. In particular, the UART is enabled and the module switches from the low-power idle mode to active mode within ~20 ms from the first character received: this is the system "wake-up time".

As a consequence, the first character sent by the DTE when the UART is disabled (i.e. the wake-up character) is not a valid communication character even if the wake-up via data reception configuration is active, because it cannot be recognized, and the recognition of the subsequent characters is guaranteed only after the complete system wake-up (i.e. after ~20 ms).

The UART wake-up via data reception configuration is active in the following case:

- the **TXD** input line is configured to wake up the system via data reception only if AT+UPSV=1 is set with hardware flow control disabled

The UART wake-up via data reception configuration is not active on the **TXD** input, and therefore all the data sent by the DTE is lost, if:

- AT+UPSV=2 is set with HW flow control disabled, and the **RTS** line is set OFF
- AT+UPSV=3 is set, regardless of the HW flow control setting, and the **DTR** line is set OFF

Figure 29 and Figure 30 show examples of common scenarios and timing constraints:

- AT+UPSV=1 power saving configuration is active and the timeout from last data received to idle mode start is set to 2000 frames (AT+UPSV=1,2000)
- Hardware flow control is disabled

Figure 29 shows the case where the module UART is disabled and only a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE module UART is disabled when the timeout from last data received expires (2000 frames without data reception, as the default case).

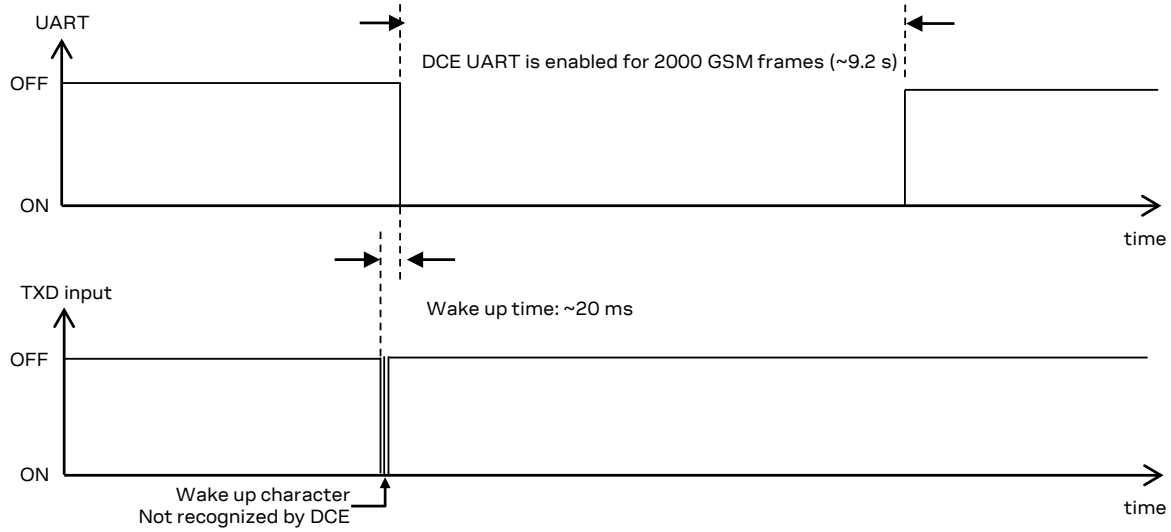


Figure 29: Wake-up via data reception without further communication

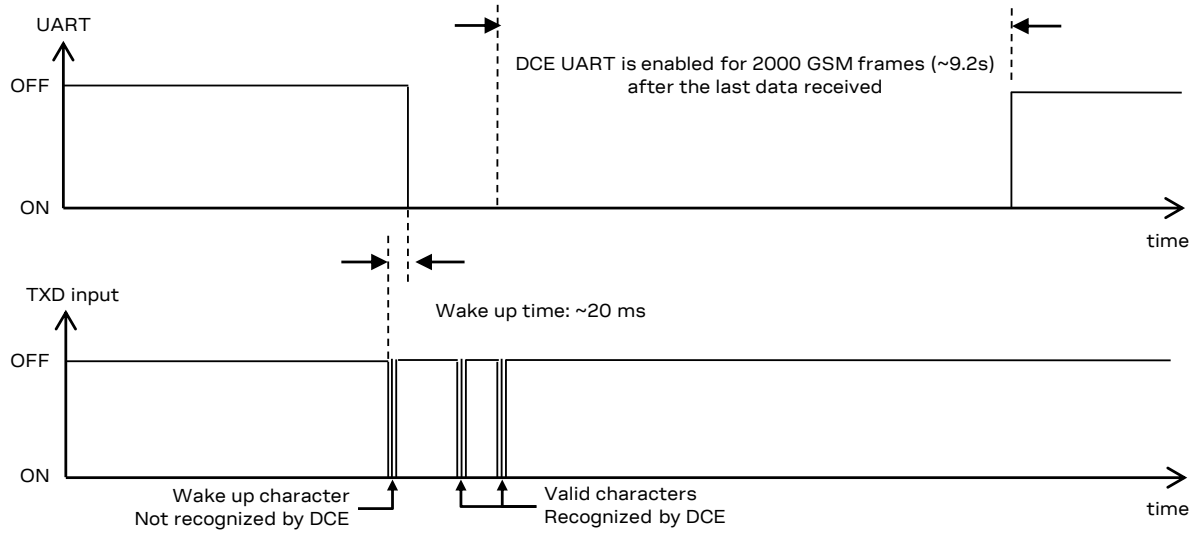


Figure 30: Wake-up via data reception with further communication

Figure 30 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake-up character wakes up the module UART. The other characters must be sent after the “wake up time” of ~20 ms. If this condition is satisfied, the module (DCE) recognizes characters. The module will disable the UART after 2000 GSM frames from the latest data reception.

- The “wake-up via data reception” feature cannot be disabled.
- In command mode[6], if autobauding is enabled and the DTE does not implement HW flow control, the DTE must always send a character to the module before the “AT” prefix set at the beginning of each command line: the first character is ignored if the module is in active mode, or it represents the wake-up character if the module is in idle mode.

[6] See the u-blox AT Commands Manual [2] for definitions of interface data mode, command mode and online command mode.

☞ In command mode[6], if autobauding is disabled, the DTE must always send a dummy “AT” before each command line: the first character is not ignored if the module is in active mode (i.e. the module replies “OK”), or it represents the wake-up character if the module is in low-power idle mode (i.e. the module does not reply).

☞ No wake-up character or dummy “AT” is required from the DTE during a voice or data call since the module UART interface continues to be enabled and does not need to be woken-up. Furthermore in data mode[6], a dummy “AT” would affect the data communications.

Additional considerations

The LISA-U2 series modules are forced to stay in active mode if the USB is connected and not suspended, and therefore the AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 settings are overruled, but they still have effect on the UART behavior: they configure the UART interface power saving, so that the UART is enabled / disabled according to the AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 settings.

To set the AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 configuration over the USB interface of LISA-U2 modules, the autobauding must be previously disabled on the UART by the +IPR AT command over the used AT interface (the USB), and this +IPR AT command configuration must be saved in the module’s non-volatile memory (see the u-blox AT Commands Manual [2]). Then, after the subsequent module re-boot, AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 can be issued over the used AT interface (the USB): all the AT profiles are updated accordingly.

1.9.2.4 UART application circuits

Providing the full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed to provide full RS-232 (9 lines) functionality, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chip provides the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to an RS-232 compatible signal level.

If a 1.8V application processor is used for complete RS-232 functionality conforming to the ITU Recommendation [3] in DTE/DCE serial communication, the complete UART interface of the module (DCE) must be connected to a 1.8 V DTE as described in Figure 31.

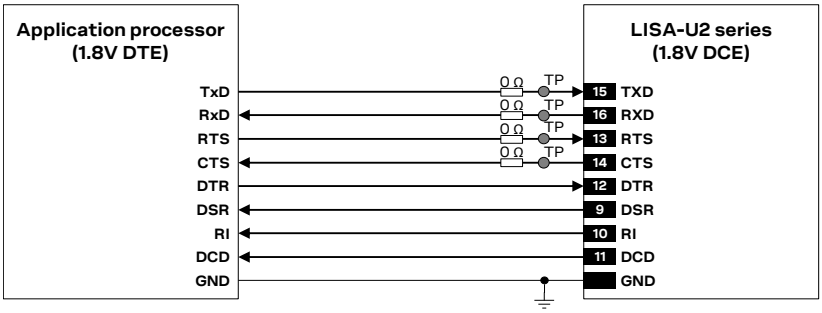


Figure 31: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output as a 1.8 V supply, as illustrated in Figure 32.

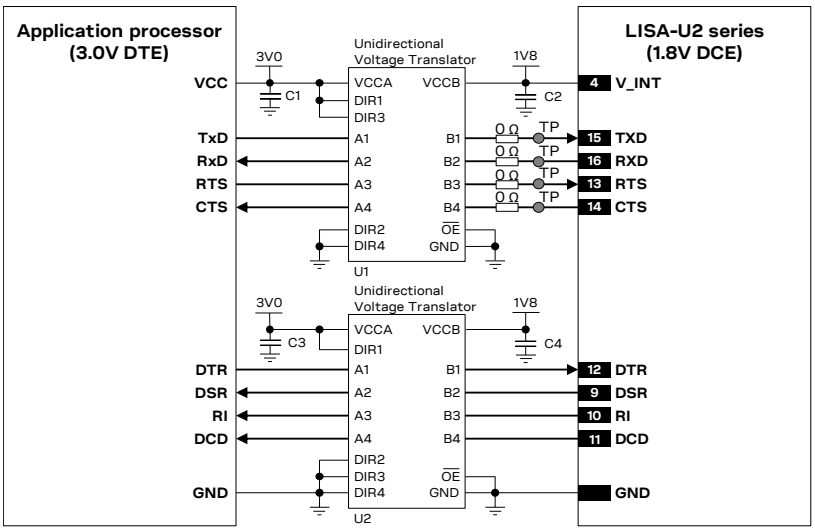


Figure 32: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 – Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774 – Texas Instruments

Table 29: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Providing the TxD, RxD, RTS, CTS and DTR lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD** and **RI** lines is not required, or the lines are not available:

- Leave the **DSR**, **DCD** and **RI** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chip provides the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to an RS-232 compatible signal level.

Figure 35 describes the circuit that should be implemented as if a 1.8 V application processor is used, given that the DTE will behave properly regardless of the **DSR** input setting.

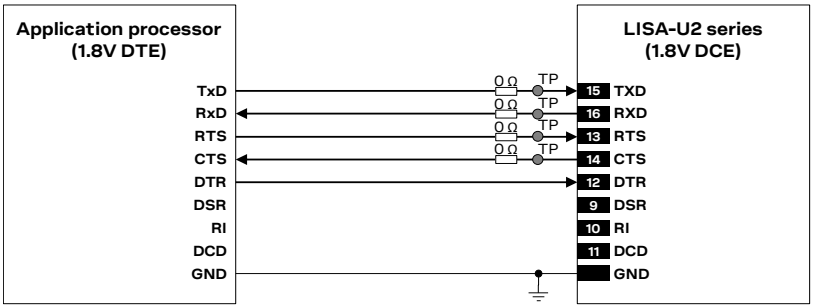


Figure 33: UART interface application circuit with partial V.24 link (6-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output pin as a 1.8 V supply, as described in Figure 34, given that the DTE will behave properly regardless of the **DSR** input setting.

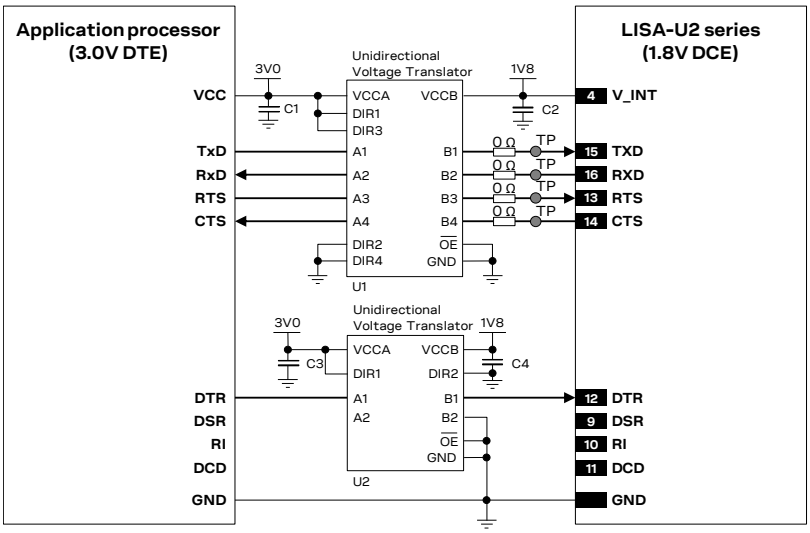


Figure 34: UART interface application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments
U2	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 30: Component for UART application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

If only the **TxD**, **RxD**, **RTS**, **CTS** and **DTR** lines are provided (as implemented in Figure 33 and in Figure 34) and if HW flow-control is enabled (AT&K3, default setting), the power saving can be activated as it can be done when the complete UART link is provided (9-wire, as implemented in Figure 31 and in Figure 32), i.e. in these ways:

- AT+UPSV=1: the module automatically enters the low-power idle mode whenever possible and the UART interface is periodically enabled, as described in section 1.9.2.3, reaching low current consumption.
  With this configuration, when the module is in idle mode, the data transmitted by the DTE will be buffered by the DTE and will be correctly received by the module when active mode is entered.
- AT+UPSV=3: the module automatically enters the low-power idle mode whenever possible and the UART interface is enabled by the **DTR** line, as described in section 1.9.2.3, reaching very low current consumption.
  With this configuration, not supported by the "01" product version, when the module is in idle mode, the UART is re-enabled 20 ms after **DTR** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active mode

If the HW flow-control is disabled (AT&K0), it is recommended to enable the power saving in one of these ways:

- AT+UPSV=2: the module automatically enters the low-power idle mode whenever possible and the UART interface is enabled by the **RTS** line, as described in section 1.9.2.3, reaching very low current consumption.
  With this configuration, when the module is in idle mode, the UART is re-enabled 20 ms after **RTS** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active mode.
- AT+UPSV=3: the module automatically enters the low-power idle mode whenever possible and the UART interface is enabled by the **DTR** line, as described in section 1.9.2.3, reaching very low current consumption.
  With this configuration, not supported by the "01" product version, when the module is in idle mode, the UART is re-enabled 20 ms after **DTR** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active mode.

Providing the TxD, RxD, RTS and CTS lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required, or the lines are not available:

- Connect the module **DTR** input line to GND, to robustly fix the logic level
- Leave the **DSR**, **DCD** and **RI** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, the Maxim 13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

Figure 35 describes the circuit that should be implemented as if a 1.8 V application processor is used.

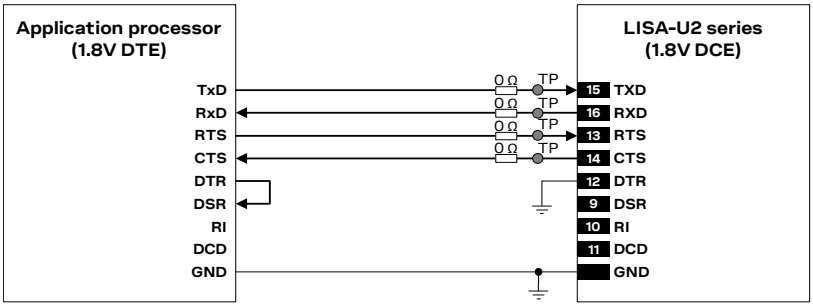


Figure 35: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output as a 1.8 V supply, as described in Figure 36.

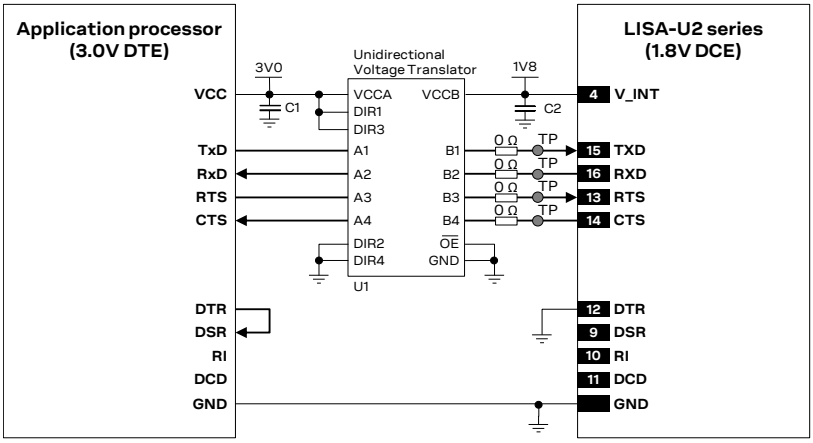


Figure 36: UART interface application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments

Table 31: Component for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

If only the **TxD**, **RxD**, **RTS** and **CTS** lines are provided, as implemented in Figure 35 and in Figure 36, and if HW flow-control is enabled (AT&K3, default setting), the power saving can be activated in this way:

- AT+UPSV=1: the module automatically enters the low-power idle mode whenever possible and the UART interface is periodically enabled, as described in section 1.9.2.3, reaching low current consumption.
  With this configuration, when the module is in idle mode, data transmitted by the DTE will be buffered by the DTE and will be correctly received by the module when active mode is entered.

If the HW flow-control is disabled (AT&K0), it is recommended to enable the power saving in this way:

- AT+UPSV=2: the module automatically enters the low-power idle mode whenever possible and the UART interface is enabled by the **RTS** line, as described in section 1.9.2.3, reaching very low current consumption.
  With this configuration, when the module is in idle mode, the UART is re-enabled 20 ms after **RTS** has been set ON, and the recognition of subsequent characters is guaranteed until the module is in active mode.

Providing the TxD and RxD lines only (not using the complete V24 link)

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available:

- Connect the module **RTS** input line to GND or to the **CTS** output line of the module: since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, that is the default setting), the pin can be connected using a 0 Ω series resistor to GND or to the active module **CTS** (low electrical level) when the module is in active mode, the UART interface is enabled and the HW flow-control is enabled.
- Connect the module **DTR** input line to GND, to robustly fix the logic level.
- Leave the **DSR**, **DCD** and **RI** lines of the module unconnected and floating.

If RS-232 compatible signal levels are needed, the Maxim 13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

Figure 37 describes the circuit that should be implemented as if a 1.8 V application processor is used.

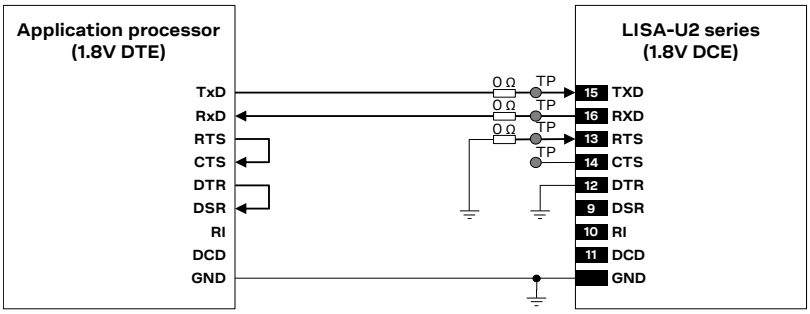


Figure 37: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V application processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output as a 1.8 V supply, as illustrated in Figure 38.

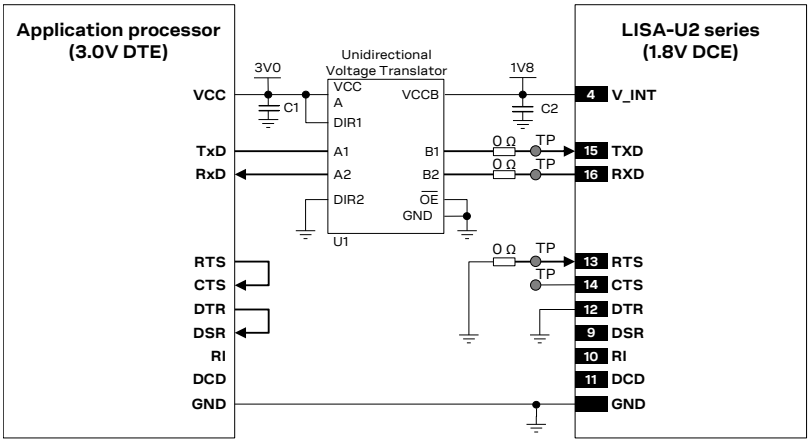


Figure 38: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 32: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

If only the **TxD** and **RxD** lines are provided, as described in Figure 37 or in Figure 38, and HW flow-control is disabled (AT&K0), the power saving must be enabled in this way:

- AT+UPSV=1: the module automatically enters the low-power idle mode whenever possible and the UART interface is periodically enabled, as described in section 1.9.2.3, reaching low current consumption.
  With this configuration, when the module is in idle mode, the UART is re-enabled 20 ms after the first data reception, and the recognition of subsequent characters is guaranteed until the module is in active mode.

☞ If only **TxD** and **RxD** lines are provided, data delivered by the DTE can be lost with these settings:

- HW flow-control enabled in the module (AT&K3, that is the default setting)
- Module power saving enabled by AT+UPSV=1
- HW flow-control disabled in the DTE

☞ In this case, the first character sent when the module is in idle mode will be a wake-up character and will not be a valid communication character (see section 1.9.2.3 for the complete description).

☞ If power saving is enabled, the application circuit with the **TxD** and **RxD** lines only is not recommended. During command mode, the DTE must send to the module a wake-up character or a dummy "AT" before each command line (see section 1.9.2.3 for the complete description), but during data mode, the wake-up character or the dummy "AT" would affect the data communications.

Additional considerations

If a 3.0 V application processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented, as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values and mind that any DTE signal connected to the module must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a clean boot of the module (see the remark below). Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the application processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

☞ If the module USB interface is connected to the application processor, it is highly recommended to provide direct access to the **RxD**, **TxD**, **CTS** and **RTS** lines of the module for execution of the firmware upgrade over UART using the u-blox EasyFlash tool and for debugging purposes: testpoints can be added on the lines to accommodate the access and a 0 Ω series resistor must be mounted on each line to detach the module pin from any other connected device. Otherwise, if the USB interface is not connected to the application processor, it is highly recommended to provide direct access to the **VUSB_DET**, **USB_D+**, **USB_D-** lines for execution of the firmware upgrade over USB and for debugging purposes. In both cases, provide as well access to the **RESET_N** pin, or to the **PWR_ON** pin, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade (see the Firmware Update Application Note [16]).

☞ If the UART interface is not used, all the UART interface pins can be left unconnected, but it is highly recommended to provide direct access to the **RxD**, **TxD**, **CTS** and **RTS** lines for execution of the firmware upgrade using the u-blox EasyFlash tool and for debugging purposes .

☞ Any external signal connected to the UART interface must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated, insert a multi-channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during the module's power-down mode, when external reset is forced low, and during the power-on sequence.

1.9.3 USB interface

LISA-U2 modules provide a high-speed USB interface at 480 Mbit/s compliant with the Universal Serial Bus Revision 2.0 specification [7]. It acts as a USB device and can be connected to any USB host such as a PC or other application processor.

The USB-device shall look for all upper SW layers like any other serial device. This means that the LISA-U2 modules emulate all serial control logical lines.

Name	Description	Remarks
VUSB_DET	USB detect input	Apply 5 V typical to enable USB
USB_D+	USB Data Line D+	90 Ω nominal differential characteristic impedance (Z_0) 30 Ω nominal common mode characteristic impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [7] are part of the USB pad driver and need not be provided externally.
USB_D-	USB Data Line D-	90 Ω nominal differential characteristic impedance (Z_0) 30 Ω nominal common mode characteristic impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [7] are part of the USB pad driver and need not be provided externally.

Table 33: USB pins

☞ The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the lines are externally accessible on the application board. Higher protection levels can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins, close to the accessible points.

1.9.3.1 USB features

LISA-U2 modules include a High-Speed USB 2.0 compliant interface with a maximum data rate of 480 Mbit/s between the module and a host processor.

The module itself acts as a USB device and can be connected to any USB host such as a personal computer or an embedded application microprocessor for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purposes.

The **USB_D+**/**USB_D-** lines carry the USB serial bus data and signaling, while the **VUSB_DET** input pin senses the VBUS USB supply presence (nominally +5 V at the source) to detect the host connection and enable the interface.

The USB interface of the module is enabled only if a valid voltage is detected by the **VUSB_DET** input (see the LISA–U2 series Data Sheet [1]). Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs only a few microamperes.

LISA-U2 series modules can provide the following functions over the USB interface:

- CDC-ACM for AT commands and data communication
- CDC-ACM for GNSS tunneling
- CDC-ACM for diagnostic
- CDC-ACM for SAP (SIM Access Profile)
- CDC-ECM for Ethernet-over-USB

☞ CDC-ECM for Ethernet-over-USB function is not supported by the "01", "x2", "63" and "68" versions.

Each USB profile of LISA-U2 module identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor according to the USB 2.0 specifications [7].

If the USB interface is connected to the host before the module switch-on, or if the module is reset with the USB interface connected to the host, the VID and PID are automatically updated at runtime, after the USB detection. At first, VID and PID are the following:

- VID = 0x058B
- PID = 0x0041

This VID and PID combination identifies a USB profile where no USB functions are available: AT commands must not be sent to the module over the USB profile identified by this VID and PID combination.

Then, after a time period (roughly 5 seconds, depending on the host / device enumeration timings), the VID and PID are updated to the following values, which are related to the LISA-U2 module default USB profile:

- VID = 0x1546
- PID = 0x1102

The default configuration of the USB interface provides 7 USB CDC-ACM modem COM ports:

- USB1: AT and data
- USB2: AT and data
- USB3: AT and data
- USB4: GNSS tunneling
- USB5: Primary Log (diagnostic purposes)
- USB6: Secondary Log (diagnostic purposes)
- USB7: SAP (SIM Access Profile)

The user can concurrently use the AT command interface on one CDC, and Packet-Switched / Circuit-Switched data communication on another CDC.

Figure 39 (left side) summarizes the USB end-points available with the default USB profile configuration.

The USB interface of the LISA-U2 series can be configured by the AT+UUSBCONF command (for more details, see the u-blox AT Commands Manual [2]) to select a different set of USB functions, available in a mutually exclusive way, and including 1 CDC-ECM for Ethernet-over-USB and 4 CDC-ACM modem COM ports enumerated as follows:

- USB1: AT and data
- USB2: GNSS tunneling
- USB3: Primary Log (diagnostic purpose)
- USB4: SAP (SIM Access Profile)

In the case of the USB profile with the set of functions described above, the VID and PID combination is the following:

- VID = 0x1546
- PID = 0x1104

Figure 39 (right side) summarizes the USB end-points available with this alternative USB profile configuration.

☞ The USB profile cannot be changed on the "01", "x2", "63" and "68" product versions of LISA-U2 series modules, as the AT+UUSBCONF command is not supported.

☞ The USB profile change, triggered by means of the AT+UUSBCONF command, is not performed at run-time. The settings are saved in the Non-Volatile Memory at the module power-off, triggered by means of the AT+CPWROFF command, and the new configuration will be effective at the subsequent module reboot.

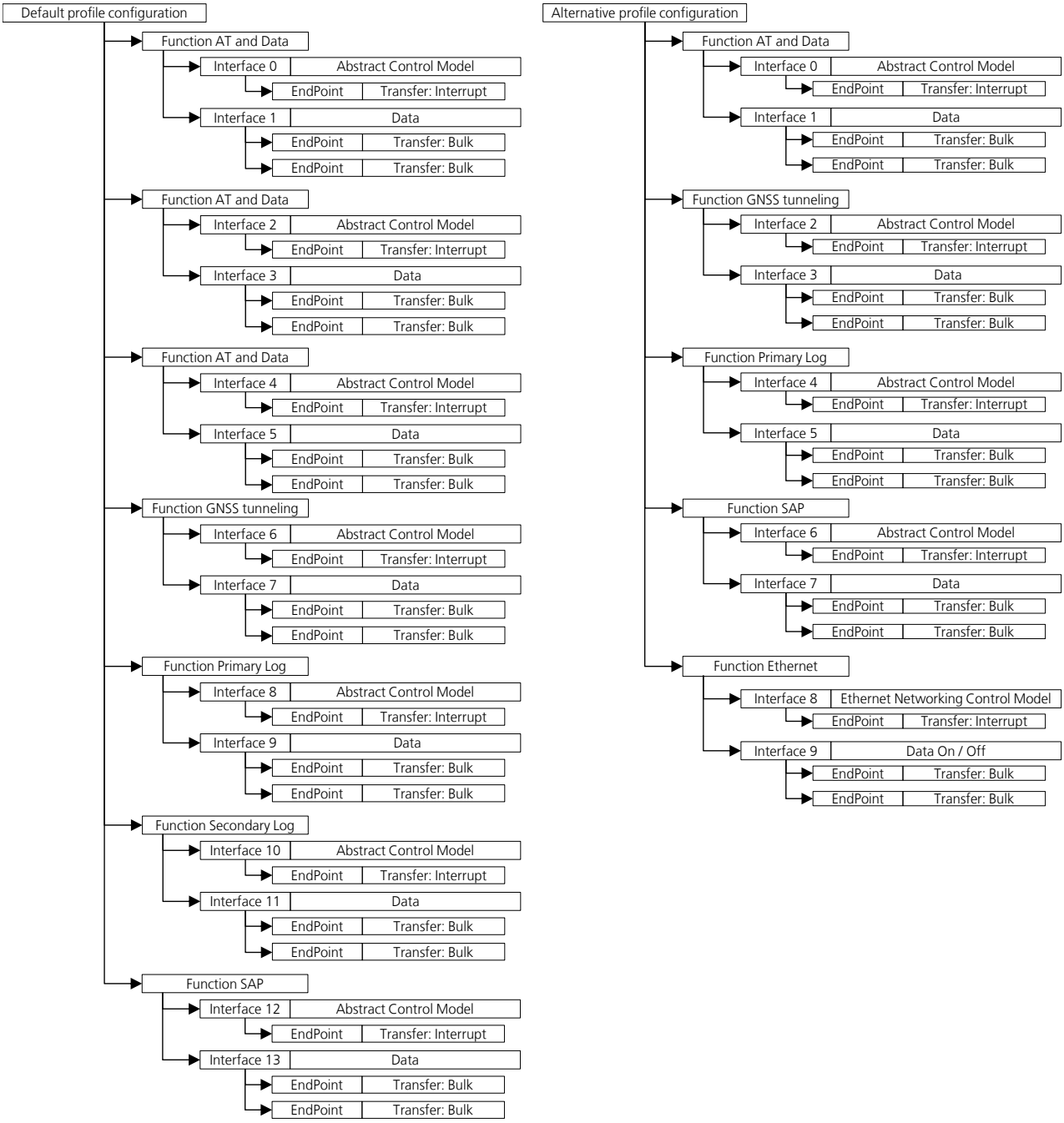


Figure 39: LISA-U2 series end-points summary for the default and alternative USB profile configuration

☞ For more details on the configuration of the USB interface of LISA-U2 modules, see the u-blox AT Commands Manual [2], +UUSBCONF AT command.

The module firmware can be upgraded over the USB interface using the u-blox EasyFlash tool or by means of an AT command (for more details, see section 3.12 and the Firmware update application note [16]).

The USB drivers are available for the following operating system platforms:

- Windows XP (WHQL, Thesycon v1.8, Thesycon v1.96)
- Windows Vista (WHQL, Thesycon v1.8, Thesycon v1.96)
- Windows 7 (WHQL, Thesycon v1.8, Thesycon v1.96)
- Windows 8
- Windows 8.1
- Windows 10
- Windows CE 5.0 (Thesycon v1.42, Thesycon v1.50)
- Windows Embedded CE 6.0 (Thesycon v1.42, Thesycon v1.50)
- Windows Embedded Compact 7 (Thesycon v1.50)
- Windows Embedded Automotive 7 (Thesycon v1.50)
- Windows Mobile 5 (Thesycon v1.42, Thesycon v1.50)
- Windows Mobile 6 (Thesycon v1.42, Thesycon v1.50)
- Windows Mobile 6.1 (Thesycon v1.50)
- Windows Mobile 6.5

LISA-U2 modules are compatible with standard Linux/Android USB kernel drivers.

1.9.3.2 USB and power saving

The modules automatically enter the USB suspended state when the device has observed no bus traffic for a specific time period according to the USB 2.0 specification [7]. In suspended state, the module maintains any USB internal status as a device. In addition, the module enters the suspended state when the hub port it is attached to is disabled. This is referred to as a USB selective suspend.

If the USB is suspended and a power saving configuration is enabled by the AT+UPSV command, the module automatically enters the low-power idle mode whenever possible, but it wakes up to active mode according to any required activity related to the network (e.g. the periodic paging reception described in section 1.5.3.3) or any other required activity related to the functions / interfaces of the module.

The USB exits suspend mode when there is bus activity. If the USB is connected and not suspended, the module is forced to stay in active mode, and so the AT+UPSV settings are overruled, but they still have effect on the power saving configuration of the other interfaces.

The modules are capable of USB remote wake-up signaling: i.e. it may request the host to exit suspend mode or selective suspend by using electrical signaling to indicate a remote wake-up, for example due to an incoming call, URCs, or data reception on a socket. The remote wake-up signaling notifies the host that it should resume from its suspended mode, if necessary, and service the external event. Remote wake-up is accomplished using electrical signaling described in the USB 2.0 specifications [7].

For the module current consumption description with power saving enabled and USB suspended, or with power saving disabled and USB not suspended, see the sections 1.5.3.3 and 1.5.3.4 and LISA-U2 series Data Sheet [1].

1.9.3.3 USB application circuit

Since the module acts as a USB device, the USB supply (5.0 V typ.) must be provided to **VUSB_DET** by the connected USB host. The USB interface is enabled only when a valid voltage as a USB supply is detected by the **VUSB_DET** input. Neither the USB interface nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs only a few microamperes.

The **USB_D+** and **USB_D-** lines carry the USB serial data and signaling. The lines are used in single-ended mode for relatively low speed signaling handshaking, as well as in differential mode for fast signaling and data transfer.

USB pull-up or pull-down resistors on pins **USB_D+** and **USB_D-** as required by the Universal Serial Bus Revision 2.0 specification [7] are part of the USB pad driver and do not need to be externally provided.

External series resistors on pins **USB_D+** and **USB_D-** as required by the Universal Serial Bus Revision 2.0 specification [7] are also integrated: characteristic impedance of the **USB_D+** and **USB_D-** lines is specified by the USB standard. The most important parameter is the differential characteristic impedance (Z_0) applicable for an odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential: signal integrity may be degraded if the PCB layout is not optimal, especially when the USB signaling lines are very long. The common mode characteristic impedance (Z_{CM}) of each USB data line should be as close as possible to 30 Ω.

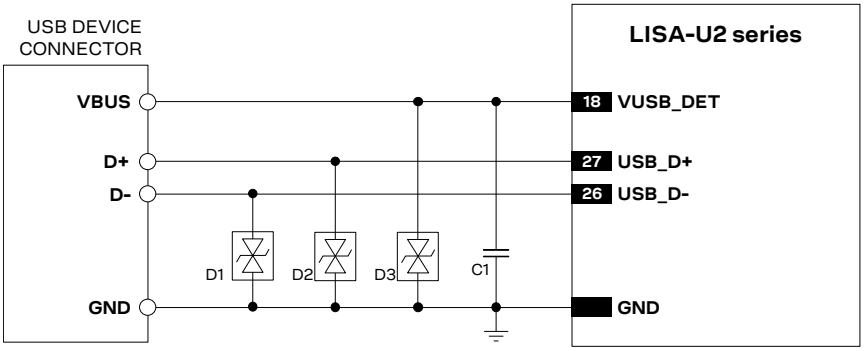


Figure 40: USB Interface application circuit

Reference	Description	Part Number - Manufacturer
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata

Table 34: Component for USB application circuit

☞ If the USB interface is not connected to the application processor, it is highly recommended to provide direct access to the **VUSB_DET**, **USB_D+**, **USB_D-** lines for execution of the firmware upgrade over USB using the u-blox EasyFlash tool and for debugging purposes: testpoints can be added on the lines to accommodate the access. Otherwise, if the USB interface is connected to the application processor, it is highly recommended to provide direct access to the **RxD**, **TxD**, **CTS** and **RTS** lines for execution of the firmware upgrade over UART and for debugging purposes. In both cases, provide as well access to **RESET_N** pin, or to the **PWR_ON** pin, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade (see the Firmware Update Application Note [16]).

☞ If the USB interface is not used, the **USB_D+**, **USB_D-** and **VUSB_DET** pins can be left unconnected, but it is highly recommended to provide direct access to the lines for FW upgrade and debugging purposes.

1.9.4 SPI interface

SPI is a master-slave protocol: the module runs as an SPI slave, i.e. it accepts AT commands on its SPI interface without any specific configuration. The SPI-compatible synchronous serial interface cannot be used for the FW upgrade.

The standard 3-wire SPI interface includes two signals to transmit and receive data (**SPI_MOSI** and **SPI_MISO**) and a clock signal (**SPI_SCLK**).

LISA-U2 modules provide two handshake signals (**SPI_MRDY** and **SPI_SRDY**), added to the standard 3-wire SPI interface, implementing the 5-wire Inter Processor Communication (IPC) interface.

The purpose of the IPC interface is to achieve high speed communication (up to 26 Mbit/s) between two processors following the same IPC specifications: the module baseband processor and an external processor. High speed communication is possible only if both sides follow the same Inter Processor Communication (IPC) specifications.

The module firmware can be upgraded over the SPI interface by means of an AT command (for more details, see section 3.1 and the Firmware Update application note [16]).

Name	Description	Remarks
SPI_MISO	SPI Data Line. Master Input, Slave Output	Module Output. Idle high. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). MSB is shifted first.
SPI_MOSI	SPI Data Line. Master Output, Slave Input	Module Input. Idle high. Shift data on rising clock edge (CPHA=1). Latch data on falling clock edge (CPHA=1). MSB is shifted first. Internal active pull-up to V_INT (1.8 V) enabled.
SPI_SCLK	SPI Serial Clock. Master Output, Slave Input	Module Input. Idle low (CPOL=0). Supported clock frequency: from 260 kHz up to 26 MHz. Internal active pull-down to GND enabled.
SPI_MRDY	SPI Master Ready to transfer data control line. Master Output, Slave Input	Module Input. Idle low. Internal active pull-down to GND enabled.
SPI_SRDY	SPI Slave Ready to transfer data control line. Master Input, Slave Output	Module Output. Idle low.

Table 35: SPI interface signals

☞ The SPI interface pins' ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the lines are externally accessible on the application board. Higher protection levels can be achieved by mounting a low capacitance (i.e. less than 10 pF) ESD protection (e.g. AVX USB0002 varistor array) on the lines connected to these pins, close to the accessible points.

1.9.4.1 IPC communication protocol overview

The module runs as an SPI slave, i.e. it accepts AT commands on its SPI interface without any specific configuration. The SPI device shall look for all upper SW layers like any other serial device. This means that LISA-U2 modules emulate all serial logical lines: the transmission and the reception of the data are similar to an asynchronous device.

Two additional signals (**SPI_MRDY** / **SPI_SRDY**) are added to the SPI lines to communicate the state of readiness of the two processors: they are used as handshake signals to implement the data flow.

The function of the **SPI_MRDY** and **SPI_SRDY** signals is two-fold:

- For transmitting data, the signal indicates to the data receiver that data is available to be transmitted
- For receiving data, the signal indicates to the transmitter that the receiver is ready to receive data

Due to this setup, it is possible to use the control signals as interrupt lines waking up the receiving part when data is available for transfer. When the handshaking has taken place, the transfer occurs just as if it were a standard SPI interface without chip select functionality (i.e. one master - one slave setup).

SPI_MRDY is used by the application processor (i.e. the master) to indicate to the module baseband processor (i.e. the slave) that it is ready to transmit or receive (IPC master ready signal), and can also be used by the application processor to wake up the module baseband processor if it is in idle mode.

SPI_SRDY line is used by the module baseband processor (i.e. the slave) to indicate to the application processor (i.e. the master) that it is ready to transmit or receive (IPC slave ready signal), and can also be used by the module baseband processor to wake up the application processor if it is in hibernation.

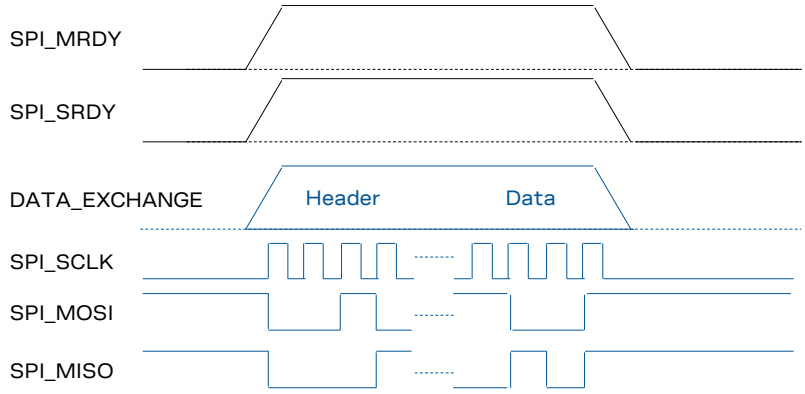


Figure 41: IPC Data Flow: SPI_MRDY and SPI_SRDY line usage combined with the SPI protocol

For the correct implementation of the SPI protocol, the frame size is known by both sides before a packet transfer of each packet. The frame is composed by a header with fixed size (always 4 bytes) and a payload with variable length (must be a multiple of 4 bytes).

The same amount of data is exchanged in both directions simultaneously. Both sides set their readiness lines (**SPI_MRDY** / **SPI_SRDY**) independently when they are ready to transfer data. For the correct transmission of the data, the other side must wait for the activating interrupt to allow the transfer of the other side.

The master starts the clock shortly after **SPI_MRDY** and **SPI_SRDY** are set to active. The number of clock periods sent by the master is exactly that one of the frame-size to be transferred. The **SPI_SRDY** line will be set low after the master sets the clock line to the idle state. The **SPI_MRDY** line is also set inactive after the clock line is set idle, but in case of a big transfer containing multiple packets, the **SPI_MRDY** line stays active.

1.9.4.2 IPC communication and power saving

If power saving is enabled by an AT command (AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3), the LISA-U2 module automatically enters idle mode whenever possible, if the master indicates that it is not ready to transmit or receive by the **SPI_MRDY** signal, or if the LISA-U2 series module itself does not transfer data.

1.9.4.3 IPC communication examples

In the following, three IPC communication scenarios are described:

- Slave-initiated data transfer, with a sleeping master
- Master-initiated data transfer, with a sleeping slave
- Slave-ended data transfer

Slave-initiated transfer with a sleeping master

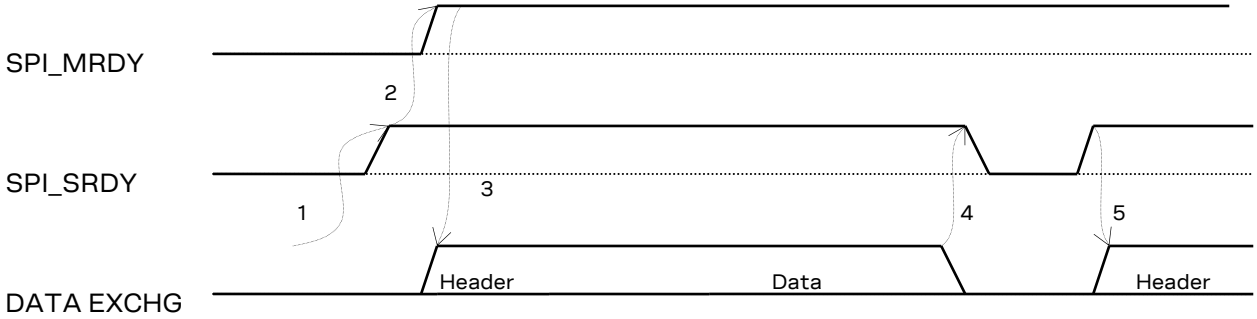


Figure 42: Data transfer initiated by the LISA-U2 module (slave), with a sleeping application processor (master)

When the master is sleeping (idle mode), the following actions happen:

1. The slave indicates to the master that is ready to send data by activating **SPI_SRDY**.
2. When the master becomes ready to send, it signalizes this by activating **SPI_MRDY**.
3. The master activates the clock and the two processors exchange the communication header and data.
4. If the data has been exchanged, the slave deactivates **SPI_SRDY** to process the received information. The master does not need to de-assert **SPI_MRDY** as it controls the **SPI_SCLK**.
5. After the preparation, the slave activates **SPI_SRDY** again and waits for **SPI_SCLK** activation. When the clock is active, all the data is transferred without intervention. If there is more data to transfer (flag set in any of the headers), the process will repeat from step 3.

Master-initiated transfer with a sleeping slave

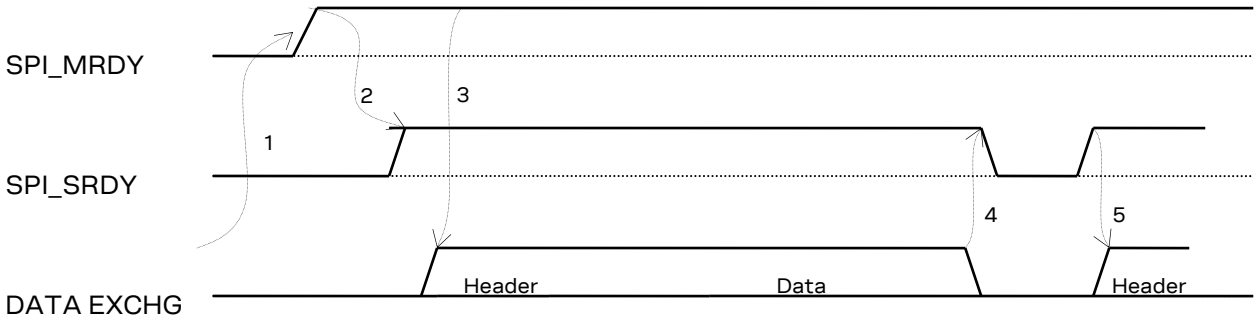


Figure 43: Data transfer initiated by the application processor (master) with a sleeping LISA-U2 module (slave)

When the slave is sleeping (idle mode), the following actions happen:

1. The master wakes the slave by setting the **SPI_MRDY** line active.
2. As soon as the slave is awake, it signals it by activating **SPI_SRDY**.
3. The master activates the clock and the two processors exchange the communication header and data.
4. If the data has been exchanged, the slave deactivates **SPI_SRDY** to process the received information. The master does not need to de-assert **SPI_MRDY** as it controls the **SPI_SCLK**.
5. After the preparation, the slave activates **SPI_SRDY** again and waits for **SPI_SCLK** activation. When the clock is active, all data is transferred without intervention. If there is more data to transfer (flag set in any of the headers), the process will repeat from step 3.

Slave ended transfer

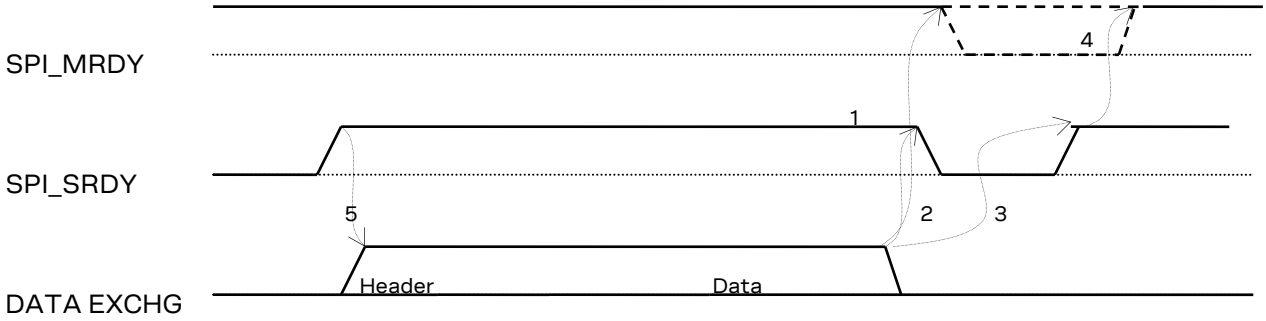


Figure 44: Data transfer terminated and then restarted by LISA-U2 module (slave)

Starting from the state where data transfer is ongoing, the following actions will happen:

1. In case of the last transfer, the master will lower its **SPI_MRDY** line. After the data transfer is finished, the line must be low. If the slave has already set its **SPI_SRDY** line, the master must raise its line to initiate the next transfer (slave-waking-procedure).
2. If the data has been exchanged, the slave will deactivate **SPI_SRDY** to process the received information. This is the normal behavior.
3. The slave will indicate the master that is ready to send data by activating **SPI_SRDY.**
4. When the master is ready to send, it will signalize this by activating **SPI_MRDY**. This is optional, when **SPI_MRDY** is low before.
5. The slave indicates immediately after a transfer termination that it is ready to start transmission again. In this case, the slave will raise **SPI_SRDY** again. The **SPI_MRDY** line can be either high or low: the master only needs to ensure that the **SPI_SRDY** change will be detected correctly via interrupt.

☞ For more details regarding IPC communication protocol, see the SPI Application Note [17].

1.9.4.4 IPC application circuits

SPI_MOSI is the data line input for the module since it runs as an SPI slave: it must be connected to the data line output (MOSI) of the application processor that runs as an SPI master.

SPI_MISO is the data line output for the module since it runs as an SPI slave: it must be connected to the data line input (MISO) of the application processor that runs as an SPI master.

SPI_SCLK is the clock input for the module since it runs as an SPI slave: it must be connected to the clock line output (SCLK) of the application processor that runs as an SPI master.

SPI_MRDY is an input for the module able to detect an external interrupt which comes from the SPI master: it must be connected to a GPIO of the application processor that runs as an SPI master.

SPI_SRDY is an output for the module that must be connected to a pin of the application processor that runs as an SPI master able to detect an external interrupt which comes from the module.

Signal integrity of the high speed data lines may be degraded if the PCB layout is not optimal, especially when the SPI lines are very long: keep routing short and minimize parasitic capacitance to preserve signal integrity. It is recommended to match the length of SPI signals.

If a 1.8 V application processor is used, the SPI master pins can be directly connected to the specific LISA-U2 SPI slave pins as described in Figure 45. It is recommended to tri-state the output pins of the SPI Master (i.e. set in high impedance mode) when the LISA-U2 module is in power-down mode, when the external reset is forced low, and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and allow a clean boot of the module.

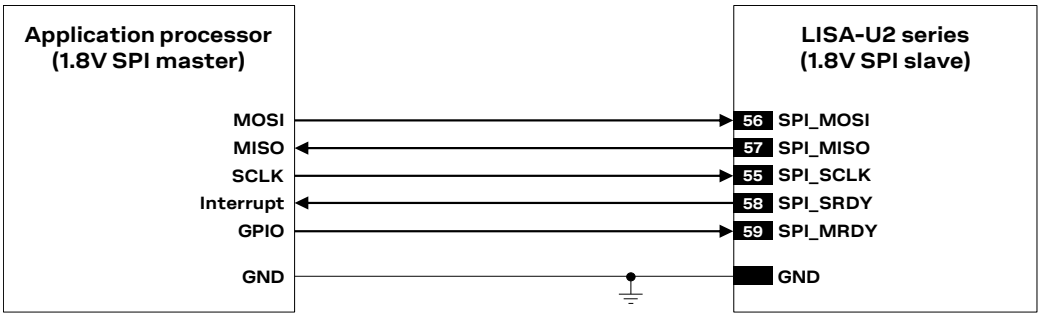


Figure 45: IPC / SPI Interface application circuit connecting LISA-U2 series 1.8V SPI slave to a 1.8V SPI master

If a 3.0 V SPI master application processor is used, implement a circuit with appropriate unidirectional voltage translators with tri-state (i.e. high impedance) mode controlled by the application processor, as illustrated in Figure 46.

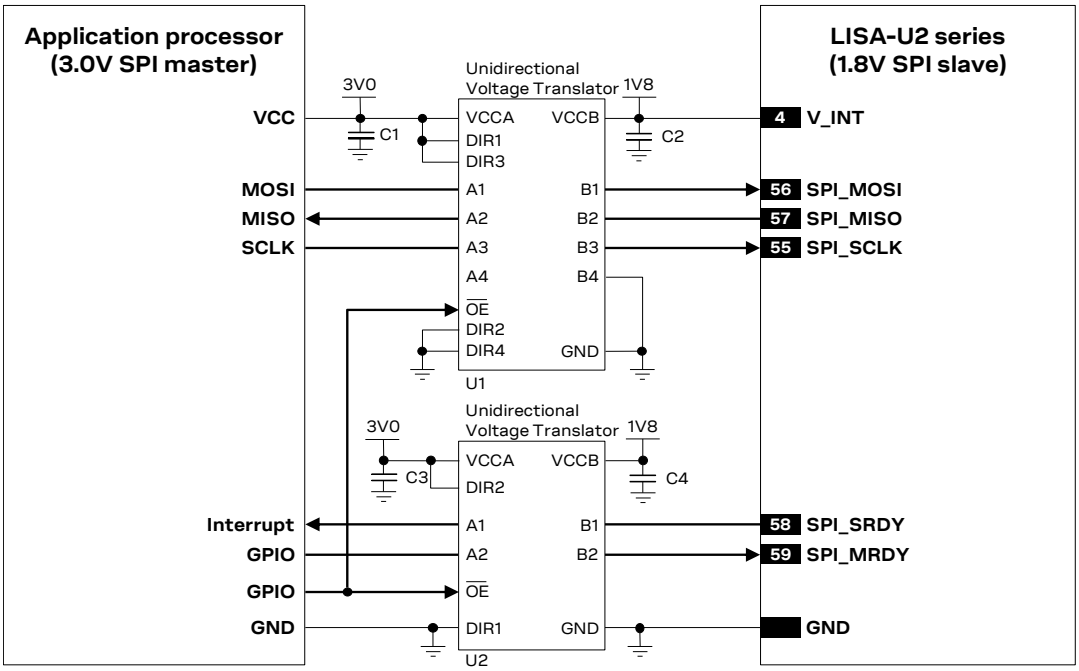


Figure 46: IPC / SPI Interface application circuit connecting LISA-U2 series 1.8V SPI slave to a 3.0 V SPI master

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments
U2	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 36: Parts for IPC / SPI Interface application circuit connecting LISA-U2 series 1.8V SPI slave to a 3.0 V SPI master

If the SPI/IPC interface is not used, the **SPI_MOSI**, **SPI_MISO**, **SPI_SCLK**, **SPI_MRDY**, **SPI_SRDY** pins can be left unconnected.

Any external signal connected to the SPI / IPC interface must be tri-stated when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and allow a clean boot of the module. If the external signals connected to the cellular module cannot be tri-stated, insert a multi-channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two circuit connections and set to high impedance during module power-down mode, when external reset is forced low, and during the power-on sequence.

1.9.5 MUX protocol (3GPP TS 27.010)

LISA-U2 modules have a software layer with MUX functionality, as peer the 3GPP TS 27.010 Multiplexer Protocol [6], available either on the UART or on the SPI physical link. The USB interface does not support the multiplexer protocol.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use the AT command interface on one MUX channel and Packet-Switched / Circuit-Switched data communication on another MUX channel. The multiplexer protocol can be used on one serial interface (UART or SPI) at a time. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GNSS, and AT commands in general. This permits, for example, SMS to be transferred to the DTE when a data connection is in progress.

The following virtual channels are defined:

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection
- Channel 6: GNSS tunneling
- Channel 7: SAP (SIM Access Profile)

For more details, see the Mux implementation Application Note [14].

☞ If the module switch-off AT command +CPWROFF is issued over a multiplexer channel, the completion of the module power-off sequence could require up to 2.5 s, after the module OK reply. Therefore, if the application processor (AP) controls the **VCC** supply of the module, the AP should disable the multiplexer protocol and then issue the AT+CPWROFF command over the used AT interface, or otherwise the AP should issue the AT+CPWROFF command over a multiplexer channel and wait 2.5 s after OK reception before removing the module **VCC** supply.

1.10 DDC (I²C) interface

1.10.1 Overview

An I²C bus compatible Display Data Channel (DDC) interface for communication with u-blox GNSS receivers is available on the LISA-U2 modules. The communication between a u-blox cellular module and a u-blox GNSS receiver is only provided by this DDC (I²C) interface.

Name	Description	Remarks
SCL	I²C bus clock line	Open drain. External pull-up required.
SDA	I²C bus data line	Open drain. External pull-up required.

Table 37: DDC pins

The DDC (I²C) interface pins' ESD sensitivity rating is 1 kV (HBM according to JESD22-A114F). Higher protection levels could be required if the lines are externally accessible on the application board. Higher protection levels can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins, close to the accessible points.

u-blox has implemented special features in LISA-U2 series cellular modules to ease the design effort required for the integration of a u-blox cellular module with a u-blox GNSS receiver.

Combining a u-blox cellular module with a u-blox GNSS receiver allows designers to have full access to the GNSS receiver directly via the cellular module: it relays control messages to the GNSS receiver via a dedicated DDC (I²C) interface. A 2nd interface connected to the GNSS receiver is not necessary: AT commands via the serial interfaces (UART, USB, SPI) of the cellular module allows full control of the GNSS receiver from any host processor.

LISA-U2 modules feature embedded GPS aiding that is a set of specific features developed by u-blox to enhance GNSS performance, decreasing Time-To-First-Fix (TTFF), thus allowing to calculate the position in a shorter time interval with higher accuracy.

The DDC (I²C) interface of all LISA-U2 series modules can be used to communicate with u-blox GNSS receivers and with external I²C devices as an audio codec: the cellular module acts as an I²C master which can communicate to more I²C slaves as allowed by the I²C bus specifications [8]. See section 1.11 for an application circuit with an external audio codec.

For more details regarding the handling of the DDC (I²C) interface and the GPS aiding features, see the u-blox AT Commands Manual [2] (AT+UGPS, AT+UGPRF, AT+UGPIOC, +UI2CO, +UI2CW, +UI2CR, +UI2CREGR, +UI2CC AT commands) and the GNSS Implementation Application Note [15].

1.10.2 DDC application circuits

1.10.2.1 General considerations

The DDC I²C-bus master interface of LISA-U2 series modules can be used to communicate with u-blox GNSS receivers and with other external I²C-bus slaves as an audio codec: besides the general considerations reported below, see section 1.10.2.2 for specific guidelines and application circuit examples for the connection to u-blox GNSS receivers and see section 1.11 for an application circuit example with an external audio codec I²C-bus slave.

To be compliant with the I²C bus specifications, the module bus interface pads are open drain output and pull up resistors must be mounted externally. Resistor values must conform to the I²C bus

specifications [8]: for example, 4.7 kΩ resistors can be commonly used. Pull-ups must be connected to a supply voltage of 1.8 V (typical), since this is the voltage domain of the DDC pins which are not tolerant to higher voltage values (e.g. 3.0 V).

☞ Connect the DDC (I^2C) pull-ups to the **V_INT** 1.8 V supply source, or another 1.8 V supply source enabled after **V_INT** (e.g. as the GNSS 1.8 V supply present in the Figure 47 application circuit), as any external signal connected to the DDC (I^2C) interface must not be set high when the module is in power-down mode, when the external reset is forced low and during the module power-on sequence (at least until the switch-on of the **V_INT** supply of DDC pins), to avoid latch-up of circuits and enable a clean boot of the module. See Figure 18 for the power-on sequence description and timings.

DDC Slave-mode operation is not supported, the module can only act as a master.

Two lines, the serial data (**SDA**) and serial clock (**SCL**), carry information on the bus. **SCL** is used to synchronize data transfers, and **SDA** is the data line. Since both lines are open drain outputs, the DDC devices can only drive them low or leave them open. The pull-up resistor pulls the line up to the supply rail if no DDC device is pulling it down to GND. If the pull-ups are missing, **SCL** and **SDA** lines are undefined and the DDC bus will not work.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus will increase the capacitance. If the bus capacitance is increased, use pull-up resistors with a nominal resistance value less than 4.7 kΩ, to match the I^2C bus specifications [8] regarding rise and fall times of the signals.

☞ Capacitance and series resistance must be limited on the bus to match the I^2C specifications (1.0 µs is the maximum allowed rise time on the **SCL** and **SDA** lines): route the connections as short as is possible.

☞ If the pins are not used as the DDC bus interface, they can be left unconnected.

1.10.2.2Connection with u-blox GNSS receivers

General considerations

LISA-U2 modules support these GPS aiding types:

- Local aiding
- AssistNow Online
- AssistNow Offline
- AssistNow Autonomous

The embedded GPS aiding features can be used only if the DDC (I^2C) interface of the cellular module is connected to the u-blox GNSS receivers.

The GPIO pins of the LISA-U2 series modules can handle:

- GNSS receiver power-on/off ("GNSS supply enable" function provided by **GPIO2**)
- The wake-up from idle mode when the GNSS receiver is ready to send data ("GNSS data ready" function provided by **GPIO3**)
- The RTC synchronization signal to the GNSS receiver ("GNSS RTC sharing" function provided by **GPIO4**)

The **GPIO2** is configured by default to provide the "GNSS supply enable" function (parameter <gpio_mode> of AT+UGPIOC command set to 3 by default), to enable or disable the supply of the u-blox GNSS receiver connected to the cellular module by the AT+UGPS command. The pin is set as

- Output / High, to switch on the u-blox GNSS receiver, if the parameter <mode> of AT+UGPS command is set to 1
- Output / Low, to switch off the u-blox GNSS receiver, if the parameter <mode> of AT+UGPS command is set to 0 (default setting)

The pin must be connected to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GNSS receiver on the application board.

The "GNSS supply enable" function improves the power consumption of the GNSS receiver. When the GNSS functionality is not required, the GNSS receiver can be completely switched off by the cellular module that is controlled by the application processor with AT commands.

The **GPIO3** is by default configured to provide the "GNSS data ready" function (parameter <gpio_mode> of AT+UGPIOC command set to 4 by default), to sense when the u-blox GNSS receiver connected to the cellular module is ready to send data by the DDC (I^2C) interface. The pin will be set as

- Input, to sense the line status, waking up the cellular module from idle mode when the u-blox GNSS receiver is ready to send data by the DDC (I^2C) interface, if the parameter <mode> of +UGPS AT command is set to 1 and the parameter <GPS_IO_configuration> of +UGPRF AT command is set to 16
- Tri-state with an internal active pull-down enabled, otherwise (default setting)

The pin that provides the "GNSS data ready" function must be connected to the data ready output of the u-blox GNSS receiver (i.e. the pin TxD1 of the u-blox GNSS receiver) on the application board.

The "GNSS data ready" function provides an improvement in the power consumption of the cellular module. When power saving is enabled in the cellular module by the AT+UPSV command and the GNSS receiver does not send data by the DDC (I^2C) interface, the module automatically enters idle mode whenever possible. With the "GNSS data ready" function the GNSS receiver can indicate to the cellular module that it is ready to send data by the DDC (I^2C) interface: the GNSS receiver can wake up the cellular module if it is in idle mode, so that data sent by the GNSS receiver will not be lost by the cellular module even if power saving is enabled.

The **GPIO4** is by default configured to provide the "GNSS RTC sharing" function (parameter <gpio_mode> of +UGPIOC AT command set to 5), to provide an RTC (Real Time Clock) synchronization signal at the power-up of the u-blox GNSS receiver connected to the cellular module. The pin will be set as

- Output, to provide an RTC synchronization signal to the u-blox GNSS receiver for RTC sharing if the parameter <mode> of AT+UGPS command is set to 1 and the parameter <GPS_IO_configuration> of +UGPRF AT command is set to 32
- Output / Low, otherwise (default setting)

The pin that provides the "GNSS RTC sharing" function must be connected to the RTC synchronization signal of the u-blox GNSS receiver (i.e. the pin EXTINT0 of the u-blox GNSS receiver) on the application board.

The "GNSS RTC sharing" function provides improved GNSS receiver performance, decreasing the Time-To-First-Fix (TTFF), and thus allowing the calculation of the position in a shorter time with higher accuracy. When GPS local aiding is enabled, the cellular module automatically uploads data such as position, time, ephemeris, almanac, health and ionospheric parameters from the GNSS receiver into its local memory, and restores this to the GNSS receiver at the next power-up of the GNSS receiver.

Connection with u-blox 1.8 V GNSS receivers

Figure 47 shows an application circuit for connecting a LISA-U2 cellular module to a u-blox 1.8 V GNSS receiver.

- The **SDA** and **SCL** pins of the LISA-U2 cellular module are directly connected to the corresponding I²C pins of the u-blox 1.8 V GNSS receiver, with appropriate pull-up resistors connected to the 1.8 V GNSS supply enabled after the **V_INT** supply of the I²C pins of the LISA-U2 cellular module.
- **GPIO3** and **GPIO4** pins are directly connected respectively to the **TxD1** and **EXTINT0** pins of the u-blox 1.8 V GNSS receiver to provide "GNSS data ready" and "GNSS RTC sharing" functions.
- A pull-down resistor is mounted on the **GPIO4** line for correct "GNSS RTC sharing" function implementation.
- A pull-down resistor is mounted on the **GPIO2** line to avoid a switch-on of the u-blox GNSS receiver when the LISA-U2 module is in the internal reset state.
- The **V_BCKP** supply output of the LISA-U2 cellular module is connected to the **V_BCKP** backup supply input pin of the GNSS receiver to provide the supply for the GNSS real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled. This enables the u-blox GNSS receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the GNSS **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

☞ "GNSS data ready" and "GNSS RTC sharing" functions are not supported by all u-blox GNSS receivers HW or ROM/FW versions. See the GNSS Implementation Application Note [15] or the Hardware Integration Manual of the u-blox GNSS receivers for the supported features.

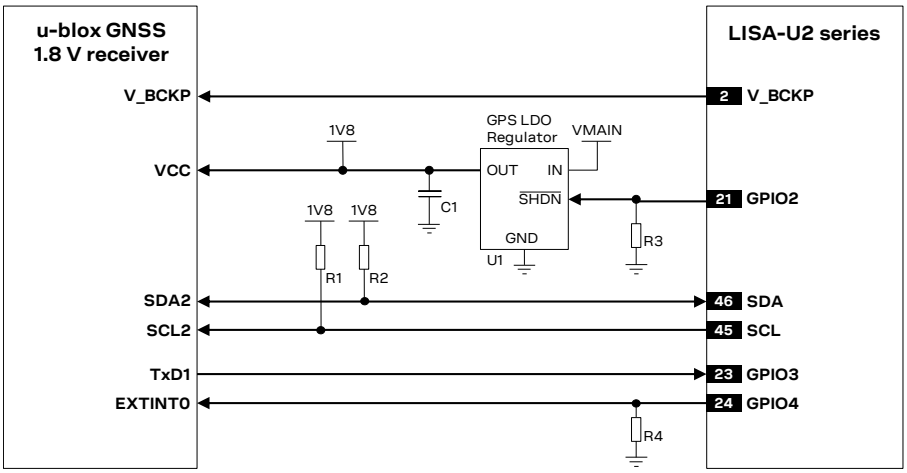


Figure 47: DDC Application circuit for u-blox 1.8 V GNSS receiver

Reference	Description	Part Number - Manufacturer
R1, R2, R4	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1	Voltage Regulator for GNSS receiver	See GNSS receiver Hardware Integration Manual

Table 38: Components for DDC application circuit for u-blox 1.8 V GNSS receiver

As an alternative to using an external voltage regulator, the **V_INT** supply output of LISA-U2 cellular modules can be used to supply a u-blox 1.8 V GNSS receiver of the u-blox 6 generation (or later u-blox generation). The **V_INT** supply is able to withstand the maximum current consumption of these positioning receivers.

The **V_INT** supply output provides low voltage ripple (up to 15 mVpp) when the module is in active mode or in connected mode, but it provides higher voltage ripple (up to 70 mVpp) when the module is in the low-power idle mode with the power saving configuration enabled by AT+UPSV (see the u-blox AT Commands Manual [2]).

According to the voltage ripple characteristic of the **V_INT** supply output:

- The power saving configuration cannot be enabled to use **V_INT** output to properly supply any 1.8 V GNSS receiver of the u-blox 6 generation and any 1.8 V GNSS receiver of the u-blox 7 generation or any newer u-blox GNSS receiver generation with TCXO.
- The power saving configuration can be enabled to use **V_INT** output to properly supply any 1.8 V GNSS receiver of the u-blox 7 generation or any more recent u-blox GNSS receiver generation without TCXO.
- Additional filtering may be needed to properly supply an external LNA, depending on the characteristics of the used LNA, adding a series ferrite bead and a bypass capacitor (e.g. the Murata BLM15HD182SN1 ferrite bead and the Murata GRM1555C1H220J 22 pF capacitor) at the input of the external LNA supply line.

See the GNSS Implementation Application Note [15] for additional guidelines on using the **V_INT** supply output of LISA-U2 cellular modules to supply a u-blox 1.8 V GNSS receiver.

Connection with u-blox 3.0 V GNSS receivers

Figure 48 shows an application circuit for connecting a LISA-U2 cellular module to a u-blox 3.0 V GNSS receiver:

- As the **SDA** and **SCL** pins of the LISA-U2 cellular module are not tolerant up to 3.0 V, the connection to the related I²C pins of the u-blox 3.0 V GNSS receiver must be provided using a proper I²C-bus Bidirectional Voltage Translator (e.g. TI TCA9406, which additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V_INT** 1.8 V cellular supply), with proper pull-up resistors.
- As the **GPIO3** and **GPIO4** pins of the LISA-U2 cellular module are not tolerant up to 3.0 V, the connection to the related pins of the u-blox 3.0 V GNSS receiver must be provided using a proper Unidirectional General Purpose Voltage Translator (e.g. TI SN74AVC2T245, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V_INT** 1.8 V cellular supply).
- The **V_BCKP** supply output of the cellular module can be directly connected to the **V_BCKP** backup supply input pin of the GNSS receiver as in the application circuit for a u-blox 1.8 V GNSS receiver.

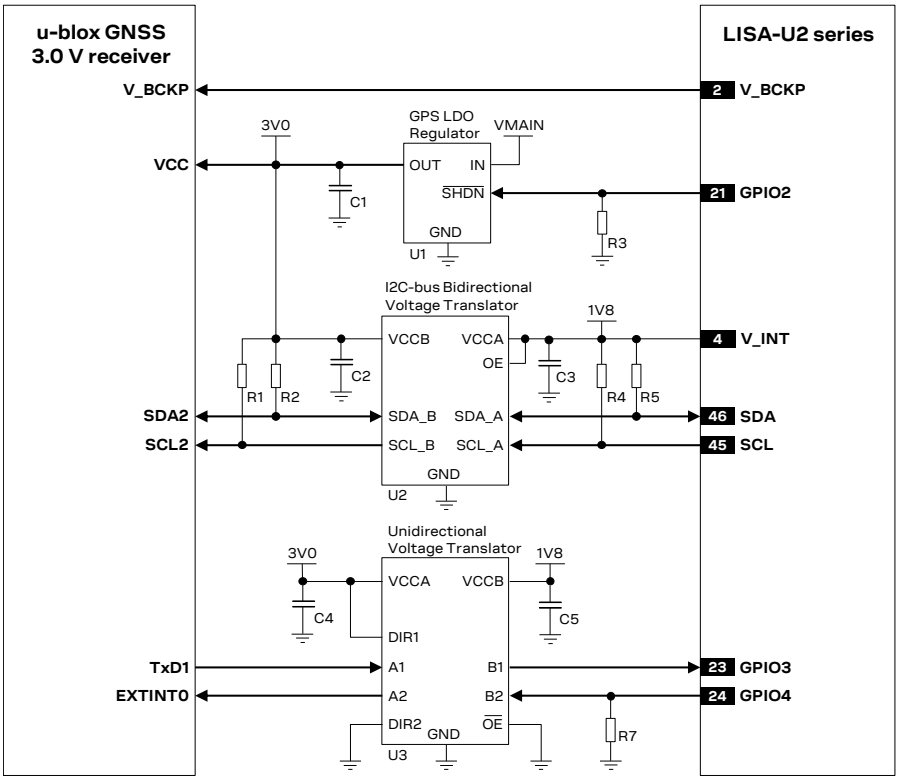


Figure 48: DDC Application circuit for a u-blox 3.0 V GNSS receiver

Reference	Description	Part Number - Manufacturer
R1, R2, R4, R5, R7	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3, C4, C5	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1, C1	Voltage Regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver Hardware Integration Manual
U2	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR - Texas Instruments
U3	Generic Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 39: Components for DDC application circuit for a u-blox 3.0 V GNSS receiver

1.11 Audio Interface

All LISA-U2 series modules provide two bidirectional 4-wire I²S digital audio interfaces for connecting to remote digital audio devices:

- First 4-wire I²S digital audio interface (**I2S_CLK**, **I2S_RXD**, **I2S_TXD** and **I2S_WA**)
- Second 4-wire I²S digital audio interface (**I2S1_CLK**, **I2S1_RXD**, **I2S1_TXD** and **I2S1_WA**)

Audio signal routing can be controlled by the dedicated AT command +USPM (see the u-blox AT Commands Manual [2]). This command allows setting the audio path mode, composed by the uplink audio path and the downlink audio path.

Each uplink and downlink path mode defines the physical input / output, the set of parameters to process the uplink audio signal (uplink gains, uplink digital filters, echo canceller parameters) and the set of parameters to process the downlink audio signal (downlink gains, downlink digital filters and sidetone).

The set of parameters to process the uplink or the downlink audio signal can be changed with dedicated AT commands for each uplink or downlink path and then stored in two profiles in the non-volatile memory (see the u-blox AT Commands Manual [2] for the audio parameters tuning commands).

LISA-U2 series modules can act as I²S master or I²S slave. In master mode, the word alignment and clock signals of the I²S digital audio interface are generated by the module. In slave mode, these signals must be generated by the remote device.

Table 40 lists the signals related to the digital audio function.

Name	Description	Remarks
I2S_TXD	I²S transmit data	Module output
I2S_RXD	I²S receive data	Module input
I2S_CLK	I²S clock	Module output in master mode Module input in slave mode
I2S_WA	I²S word alignment	Module output in master mode Module input in slave mode
I2S1_TXD	Second I²S transmit data	Module output
I2S1_RXD	Second I²S receive data	Module input
I2S1_CLK	Second I²S clock	Module output in master mode Module input in slave mode
I2S1_WA	Second I²S word alignment	Module output in master mode Module input in slave mode
CODEC_CLK	Digital clock output	Digital clock output for external audio codec Configurable to 26 MHz or 13 MHz

Table 40: Digital audio interface pins

☞ The I²S interfaces and **CODEC_CLK** pins' ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the lines are externally accessible on the application board. Higher protection levels can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to the I²S interfaces pins, close to the accessible points, and a low capacitance (i.e. less than 10 pF) ESD protection (e.g. AVX USB0002) on the line connected to **CODEC_CLK** pin, close to the accessible point.

The I²S interface can be set to two modes using the <I2S_mode> parameter of the AT+UI2S command:

- PCM mode
- Normal I²S mode

The I²S interface can be set to two configurations, by the <I2S_Master_Slave> parameter of AT+UI2S:

- Master mode
- Slave mode

The sample rate of transmitted/received words can be set, by the <I2S_sample_rate> parameter of AT+UI2S, to:

- 8 kHz
- 11.025 kHz
- 12 kHz
- 16 kHz
- 22.05 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz

The <main_uplink> and <main_downlink> parameters of the AT+USPM command must be properly configured to select the I²S digital audio interfaces paths (for more details, see the u-blox AT Commands Manual [2]):

- <main_uplink> must be properly set to select:
  - the first I²S interface (using **I2S_RXD** module input)
  - the second I²S interface (using **I2S1_RXD** module input)
- <main_downlink> must be properly set to select:
  - the first I²S interface (using **I2S_TXD** module output)
  - the second I²S interface (using **I2S1_TXD** module output)

Parameters of the digital path can be configured and saved as the normal analog paths, using appropriate path parameters as described in the u-blox AT Commands Manual [2], +USGC, +UMGC, +USTN AT command. Analog gain parameters are not used.

The I²S receive data input and the I²S transmit data output signals can use the following resources:

- Digital filters and digital gains are available in both uplink and downlink directions. They can be correctly configured with the AT commands
- Ringer tone and service tone are mixed on the TX path when active (downlink)
- The HF algorithm acts on the I²S path

☞ See the u-blox AT Commands Manual [2] (AT+UI2S command) for the possible settings of the I²S interface.

1.11.1 I²S interface - PCM mode

Main features of the I²S interface in PCM mode:

- I²S runs in PCM - short alignment mode (configurable by AT commands)
- I²S word alignment signal can be configured to 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz
- I²S word alignment toggles high for 1 or 2 CLK cycles of synchronization (configurable), then toggles low for 16 CLK cycles of sample width. Frame length can be 1 + 16 = 17 bits or 2 + 16 = 18 bits
- I²S clock frequency depends on the frame length and <sample_rate>. Can be 17 x <sample_rate> or 18 x <sample_rate>
- I²S transmit and I²S receive data are 16-bit words long with the same sampling rate as I²S word alignment, mono. Data is in 2's complement notation. MSB is transmitted first
- When I²S word alignment toggles high, the first synchronization bit is always low. The second synchronization bit (present only in case of 2 bit long I²S word alignment configuration) is MSB of the transmitted word (MSB is transmitted twice in this case)
- I²S transmit data changes on the I²S clock rising edge, I²S receive data changes on the I²S clock falling edge

1.11.2 I²S interface - Normal I²S mode

Normal I²S supports:

- 16-bit words
- Mono interface
- Configurable sample rate: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz

Main features of the I²S interface in normal I²S mode:

- I²S word alignment signal always runs at <sample_rate> and synchronizes 2 channels (timeslots on word alignment high, word alignment low)
- I²S transmit data is composed of 16-bit words, dual mono (the words are written on both channels). Data are in 2's complement notation. MSB is transmitted first. The bits are written on I²S clock rising or falling edge (configurable)
- I²S receive data is read as 16-bit words, mono (words are read only on the timeslot with WA high). Data is read in 2's complement notation. MSB is read first. The bits are read on the I²S clock edge opposite to the I²S transmit data writing edge (configurable)
- I²S clock frequency is 16 bits x 2 channels x <sample_rate>

The modes are configurable through a specific AT command (see the u-blox AT Commands Manual [2], +UI2S AT command) and the following parameters can be set:

- MSB can be 1 bit delayed or non-delayed on I²S word alignment edge
- I²S transmit data can change on the rising or falling edge of the I²S clock signal (rising edge in this example)
- I²S receive data are read on the opposite front of the I²S clock signal

1.11.3 I²S interface application circuits

LISA-U2 I²S digital audio interfaces can be connected to an external digital audio device for voice applications.

Any external digital audio device compliant with the configuration of the digital audio interface of the cellular module can be used, given that the external digital audio device must provide:

- The opposite role: slave or master for LISA-U2 modules that may act as master or slave
- The same mode and frame format: PCM / short alignment or Normal I²S mode / long alignment mode with
  - data in 2's complement notation
  - MSB transmitted first
  - word length = 16-bit
  - frame length = 17-bit or 18-bit in PCM / short alignment mode (16 + 1 or 16 + 2 clock cycles, with Word Alignment / Synchronization signal set high for 1 clock cycle or 2 clock cycles), or
  - frame length = 32-bit in Normal I²S mode / long alignment mode (16 x 2 clock cycles)
- The same sample rate and serial clock frequency: as the clock frequency depends on the frame length and the sample rate, the clock frequency can be
  - 17 x <I2S_sample_rate> or 18 x <I2S_sample_rate> in PCM / short alignment mode, or
  - 16 x 2 x <I2S_sample_rate> in Normal I²S mode / long alignment mode
- Compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V digital audio interface of the module to the external 3.0 V (or similar) digital audio device by means of appropriate unidirectional voltage translators (e.g. Texas Instruments SN74AVC4T774 or SN74AVC2T245), using the module **V_INT** output as a 1.8 V supply for the voltage translators on the module side

For the appropriate selection of a compliant external digital audio device, see the +UI2S AT command description in the u-blox AT Commands Manual [2] for further details regarding the capabilities and the possible settings of the I²S digital audio interface of LISA-U2 series modules.

Figure 49 shows an application circuit with a generic digital audio device.

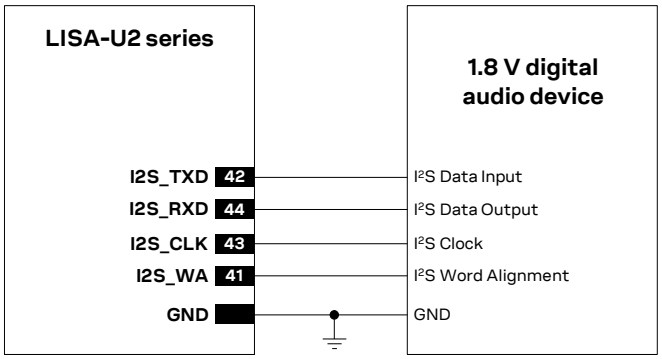


Figure 49: I²S interface application circuit with a generic digital audio device

Because, in general, any external digital audio device compliant to the configuration of the digital audio interface of the cellular module can be used with LISA-U2 series modules, an appropriate specific application circuit must be implemented and configured according to the particular external digital audio device or audio codec used and according to the application requirements.

Examples of manufacturers offering compatible audio codec parts, suitable to provide basic analog audio voice capability on the application device, are the following:

- Maxim Integrated (as the MAX9860, MAX9867, MAX9880A audio codecs)
- Texas Instruments / National Semiconductor
- Cirrus Logic / Wolfson Microelectronics
- Nuvoton Technology
- Asahi Kasei Microdevices
- Realtek Semiconductor

Figure 50 and Table 41 describe an application circuit for I²S digital audio interfaces of LISA-U2 series modules, providing voice capability using an external audio voice codec. DAC and ADC integrated in the external audio codec respectively converts an incoming digital data stream to analog audio output through a mono amplifier and converts the microphone input signal to the digital bit stream over the digital audio interface.

An I²S digital audio interface of the LISA-U2 series modules that acts as an I²S master is connected to the digital audio interface of the external audio codec (that acts as an I²S slave). The first I²S interface can be used as well as the second I²S interface of the cellular module.

The **CODEC_CLK** digital output clock of the cellular module is connected to the clock input of the external audio codec to provide the clock reference.

Signal integrity of the high speed lines may be degraded if the PCB layout is not optimal, especially when the **CODEC_CLK** clock line or also the I²S digital audio interface lines are very long: keep routing short and minimize parasitic capacitance to preserve signal integrity.

The external audio codec is controlled by the cellular module using the DDC (I²C) interface: this interface can be used to communicate with u-blox GNSS receivers and at the same time to control an external audio codec on all LISA-U2 series modules.

The **V_INT** supply output of the cellular module provides the supply to the external audio codec, defining a suitable voltage level for the digital interfaces.

Additional components are provided for EMC and ESD immunity conformity according to European Norms for Radio Equipment Directive (2014/53/EU) and EMC Directive (2014/30/EU) compliance. The recommended parts for EMC and ESD immunity conformity are: a 10 nF bypass capacitor (e.g. Murata GRM155R71C103KA88) and a proper series chip ferrite bead noise/EMI suppression filter (e.g. Murata BLM15HD182SN1) provided on each microphone line input and speaker line output of the external codec as illustrated in Figure 50 and Table 41.

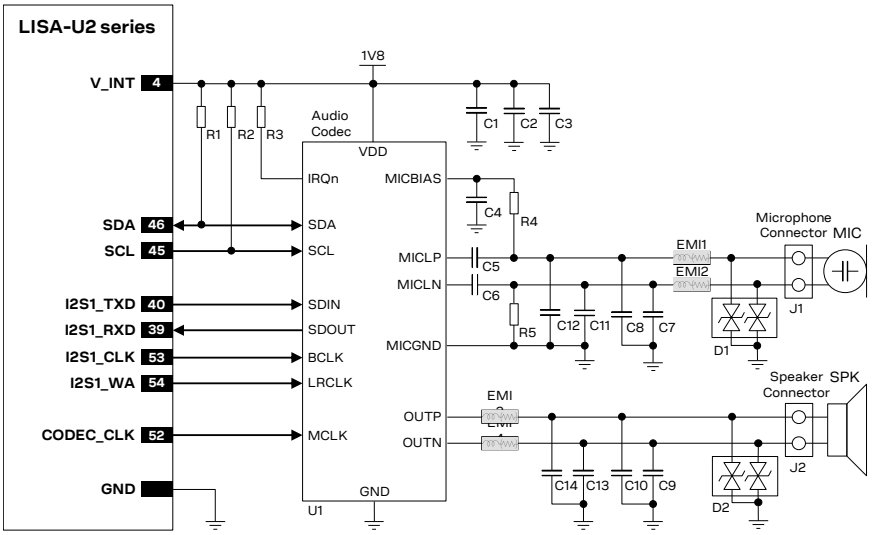


Figure 50: I²S interface application circuit with an external audio codec to provide voice capability

Reference	Description	Part Number – Manufacturer
C1	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
C2, C4, C5, C6	1 µF Capacitor Ceramic X5R 0402 10% 6.3 V	GRM155R60J105KE19 – Murata
C3	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C7, C8, C9, C10	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 – Murata
C11, C12, C13, C14	10 nF Capacitor Ceramic X5R 0402 10% 50V	GRM155R71C103KA88 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
EMI1, EMI2, EMI3, EMI4	Chip Ferrite Bead Noise/EMI Suppression Filter 1800 Ohm at 100 MHz, 2700 Ohm at 1 GHz	BLM15HD182SN1 – Murata
J1	Microphone Connector	Various manufacturers
J2	Speaker Connector	Various manufacturers
MIC	2.2 kΩ Electret Microphone	Various manufacturers
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R4, R5	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
SPK	32 Ω Speaker	Various manufacturers
U1	16-Bit Mono Audio Voice Codec	MAX9860ETG+ - Maxim

Table 41: Example of components for audio voice codec application circuit

☞ Any external signal connected to the digital audio interface must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi-channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set it to high impedance during the module power-down mode and during the module power-on sequence.

☞ If the I²S digital audio pins are not used, they can be left unconnected on the application board.

1.11.4 Voiceband processing system

The voiceband processing on the LISA-U2 modules is implemented in the DSP core inside the baseband chipset.

The external digital audio devices can be interfaced directly to the DSP digital processing part via the I²S digital interface. With exception of the speech encoder/decoder, audio processing can be controlled by AT commands.

The audio processing is implemented within the different blocks of the voiceband processing system:

- Sample-based Voice-band Processing (single sample processed at 16 kHz for Wide Band AMR codec or 8 kHz for all other speech codecs)
- Frame-based Voice-band Processing (frames of 320 samples for Wide Band AMR codec or 160 samples for all other speech codecs are processed every 20 ms)

These blocks are connected by buffers (circular buffer and voiceband sample buffer) and sample rate converters (for 8 / 16 to 47.6 kHz conversion).

The voiceband audio processing implemented in the DSP core of LISA-U2 series modules is summarized in Figure 51.

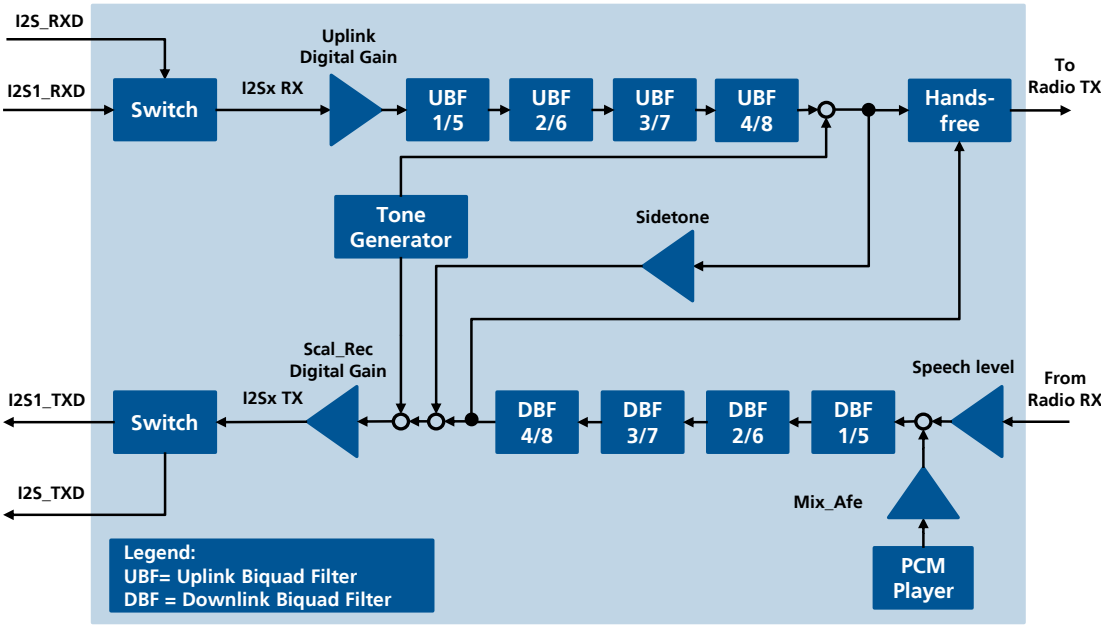


Figure 51: Audio processing system of LISA-U2 series modules

LISA-U2 modules audio signal processing algorithms are:

- Speech encoding (uplink) and decoding (downlink).The following speech codecs are supported in firmware on the DSP for speech encoding and decoding:
  - GERAN GMSK codecs
    - GSM HR (GSM Half Rate)
    - GSM FR (GSM Full Rate)
    - GSM EFR (GSM Enhanced Full Rate)
    - HR AMR (GSM Half Rate Adaptive Multi Rate - Narrow Band)
    - FR AMR (GSM Full Rate Adaptive Multi Rate - Narrow Band)
    - FR AMR-WB (GSM Full Rate Adaptive Multi Rate - Wide Band)
  - UTRAN codecs:
    - UMTS AMR2 (UMTS Adaptive Multi Rate version 2 – Narrow Band)
    - UMTS AMR-WB (UMTS Adaptive Multi Rate – Wide Band)
- Mandatory sub-functions:
  - Discontinuous transmission, DTX (GSM 46.031, 46.041, 46.081 and 46.093 standards)
  - Voice activity detection, VAD (GSM 46.032, 46.042, 46.082 and 46.094 standards)
  - Background noise calculation (GSM 46.012, 46.022, 46.062 and 46.092 standards)
- Function configurable via specific AT commands (see the u-blox AT Commands Manual [2])
  - Signal routing: +USPM command
  - Analog amplification, Digital amplification: +USGC, +CLVL, +CRSL, +CMUT command
  - Digital filtering: +UUBF, +UDBF commands
  - Hands-free algorithms (echo cancellation, Noise suppression, Automatic Gain control) +UHFP command
  - Sidetone generation (feedback of uplink speech signal to downlink path): +USTN command
  - Playing/mixing of alert tones:
    - Service tones: Tone generator with 3 sinus tones +UPAR command
    - User generated tones: Tone generator with a single sinus tone +UTGN command
    - PCM audio files (for prompting): The storage format of PCM audio files is 8 kHz sample rate, signed 16 bits, little endian, mono

1.12 General Purpose Input/Output (GPIO)

LISA-U2 series modules provide up to 14 pins (**GPIO1-14**) which can be configured as general purpose input or output, or can be configured to provide special functions via u-blox AT commands (for further details, see the u-blox AT Commands Manual [2], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF, +USPM).

The following functions are available in the LISA-U2 modules:

GSM Tx burst indication:

GPIO1 pin can be configured by AT+UGPIOC to indicate when a GSM Tx burst/slot occurs, setting the parameter <gpio_mode> of AT+UGPIOC command to 9.

No GPIO pin is configured by default to provide the "GSM Tx burst indication" function.

The pin configured to provide the "GSM Tx burst indication" function is set as

- Output / High, since ~10 µs before the start of first Tx slot, until ~5 µs after the end of last Tx slot
- Output / Low, otherwise

The pin configured to provide the "GSM Tx burst indication" function can be connected on the application board to an input pin of an application processor to indicate when a GSM Tx burst/slot occurs.

GNSS supply enable:

The **GPIO2** is by default configured by AT+UGPIOC command to enable or disable the supply of the u-blox GNSS receiver connected to the cellular module.

The **GPIO1**, **GPIO3**, **GPIO4** or **GPIO5** pins can be configured to provide the "GNSS supply enable" function, alternatively to the default **GPIO2** pin, setting the parameter <gpio_mode> of AT+UGPIOC command to 3. The "GNSS supply enable" mode can be provided only on one pin at a time: it is not possible to simultaneously set the same mode on another pin.

The pin configured to provide the "GNSS supply enable" function is set as

- Output / High, to switch on the u-blox GNSS receiver, if the parameter <mode> of AT+UGPS command is set to 1
- Output / Low, to switch off the u-blox GNSS receiver, if the parameter <mode> of AT+UGPS command is set to 0 (default setting)

The pin configured to provide the "GNSS supply enable" function must be connected to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GNSS receiver on the application board.

GNSS data ready:

Only the **GPIO3** pin provides the "GNSS data ready" function, to sense when a u-blox GNSS receiver connected to the cellular module is ready to send data via the DDC (I^2C) interface, setting the parameter <gpio_mode> of AT+UGPIOC command to 4.

The pin configured to provide the "GNSS data ready" function will be set as

- Input, to sense the line status, waking up the cellular module from idle mode when the u-blox GNSS receiver is ready to send data via the DDC (I^2C) interface; this is possible if the parameter <mode> of AT+UGPS command is set to 1 and the parameter <GPS_IO_configuration> of AT+UGPRF command is set to 16
- Tri-state with an internal active pull-down enabled, otherwise (default setting)

The pin that provides the "GNSS data ready" function must be connected to the data ready output of the u-blox GNSS receiver (i.e. the pin TxD1 of the u-blox GNSS receiver) on the application board.

GNSS RTC sharing:

Only the **GPIO4** pin provides the "GNSS RTC sharing" function to provide an RTC (Real Time Clock) synchronization signal to the u-blox GNSS receiver connected to the cellular module, setting the parameter <gpio_mode> of AT+UGPIOC command to 5.

The pin configured to provide the "GNSS RTC sharing" function will be set as

- Output, to provide an RTC (Real Time Clock) synchronization signal to the u-blox GNSS receiver if the parameter <mode> of AT+UGPS command is set to 1 and parameter <GPS_IO_configuration> of AT+UGPRF command is set to 32
- Output / Low, otherwise (default setting)

The pin that provides the "GNSS RTC sharing" function must be connected to the RTC synchronization input of the u-blox GNSS receiver (i.e. the pin EXTINT0 of the u-blox GNSS receiver) on the application board.

SIM card detection:

The **GPIO5** pin is by default configured by AT+UGPIOC command to detect SIM card presence.

Only the **GPIO5** pin can be configured to provide the "SIM card detection" function, setting the parameter <gpio_mode> of the AT+UGPIOC command to 7 (default setting).

The pin configured to provide the "SIM card detection" function is set as

- Input with an internal active pull-down enabled, to sense SIM card presence

The pin must be connected on the application board to SW2 pin of the SIM card holder, which must provide 2 pins for the mechanical card presence detection, with a 470 kΩ pull-down resistor. SW1 pin of the SIM card holder must be connected to the **V_INT** pin of the module, by a 1 kΩ pull-up resistor. See Figure 52 and section 1.8 for the application circuit. The **GPIO5** signal will be pulled low by the pull-down when a SIM card is not inserted in the holder, and will be pulled high by the pull-up when a SIM card is present.

The **GPIO5** pin is configured as an external interrupt to detect SIM card presence. An Unsolicited Result Code (URC) can be generated each time that there is a change of status (for more details, see the "simind" value of the <descr> parameter of +CIND and +CMER commands in the u-blox AT Commands Manual [2]).

All LISA-U2 series modules provide the additional function "SIM card hot insertion/removal" on the **GPIO5** pin, which can be enabled using the AT+UDCONF=50 command (for more details, see the u-blox AT Commands Manual [2]).

Network status indication:

GPIO1, **GPIO2**, **GPIO3**, **GPIO4** or **GPIO5** can be configured to indicate network status (i.e. no service, registered home 2G network, registered home 3G network, registered visitor 2G network, registered visitor 3G network, voice or data 2G/3G call enabled), setting the parameter <gpio_mode> of AT+UGPIOC command to 2.

No GPIO pin is configured by default to provide the "Network status indication" function.

The "Network status indication" mode can be provided only on one pin at a time: it is not possible to simultaneously set the same mode on another pin.

The pin configured to provide the "Network status indication" function is set as

- Continuous Output / Low, if no service (no network coverage or not registered)
- Cyclic Output / High for 100 ms, Output / Low for 2 s, if registered home 2G network
- Cyclic Output / High for 50 ms, Output / Low for 50 ms, Output / High for 50 ms, Output / Low for 2 s, if registered as a home 3G network

- Cyclic Output / High for 100 ms, Output / Low for 100 ms, Output / High for 100 ms, Output / Low for 2 s, if registered as a visitor 2G network (roaming)
- Cyclic Output / High for 50 ms, Output / Low for 50 ms, Output / High for 50 ms, Output / Low for 100 ms, if registered as a visitor 3G network (roaming)
- Continuous Output / High, if voice or data 2G/3G call enabled

The pin configured to provide the "Network status indication" function can be connected on the application board to an input pin of an application processor or it can drive a LED by a transistor with integrated resistors to indicate network status.

Module status indication:

The **GPIO1** and **GPIO13** pins can be configured to indicate module status (power-off mode, i.e. module switched off, versus idle, active or connected modes, i.e. module switched on), properly setting the parameter <gpio_mode> of the AT+UGPIOC command to 10.

No GPIO pin is configured by default to provide the "Module status indication".

The pin configured to provide the "Module status indication" function is set as

- Output / High, when the module is switched on (any operating mode during module normal operation: idle, active or connected mode)
- Output / Low, when the module is switched off (power-off mode)

The "Module status indication" mode can be provided only on one pin at a time: it is not possible to simultaneously set the same mode on another pin.

Module operating mode indication:

The **GPIO14** and **GPIO5** pins can be configured to indicate module operating mode (idle mode versus active or connected modes), properly setting the parameter <gpio_mode> of AT+UGPIOC command to 11.

No GPIO pin is configured by default to provide the "Module operating mode indication".

The pin configured to provide the "Module operating mode indication" function is set as

- Output / High, when the module is in active or connected mode
- Output / Low, when the module is in idle mode (that can be reached if power saving is enabled by +UPSV AT command: for further details, see the u-blox AT Commands Manual [2])

The "Module operating mode indication" mode can be provided only on one pin at a time: it is not possible to simultaneously set the same mode on another pin.

I²S digital audio interface:

The **GPIO6**, **GPIO7**, **GPIO8**, **GPIO9** pins are by default configured as the second I²S digital audio interface (**I2S1_RXD**, **I2S1_TXD**, **I2S1_CLK**, **I2S1_WA** respectively).

Only these pins can be configured as the second I²S digital audio interface, correctly setting the parameter <gpio_mode> of AT+UGPIOC command to 12 (default setting).

SPI serial interface:

GPIO10, **GPIO11**, **GPIO12**, **GPIO13** and **GPIO14** pins are by default configured as the SPI / IPC serial interface (**SPI_SCLK**, **SPI_MOSI**, **SPI_MISO**, **SPI_SRDY** and **SPI_MRDY** respectively).

Only these pins can be configured as the SPI / IPC serial interface, correctly setting the parameter <gpio_mode> of AT+UGPIOC command to 13 (default setting).

General purpose input:

All the GPIOs can be configured as input to sense a high or low digital level through the AT+UGPIOR command, setting the parameter <gpio_mode> of the AT+UGPIOC command to 1.

The “General purpose input” mode can be provided on more than one pin at a time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

No GPIO pin is configured by default as “General purpose input”.

The pin configured to provide the “General purpose input” function is set as

- Input, to sense high or low digital level by the AT+UGPIOR command.

The pin can be connected on the application board to an output pin of an application processor to sense the digital signal level.

General purpose output:

All the GPIOs can be configured as output to set the high or the low digital level through the AT+UGPIOW command, setting the parameter <gpio_mode> of the +UGPIOC AT command to 0.

The “General purpose output” mode can be provided on more than one pin per time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

No GPIO pin is configured by default as “General purpose output”.

The pin configured to provide the “General purpose output” function is set as

- Output / Low, if the parameter <gpio_out_val> of AT+UGPIOW command is set to 0
- Output / High, if the parameter <gpio_out_val> of AT+UGPIOW command is set to 1

The pin can be connected on the application board to an input pin of an application processor to provide a digital signal.

Pad disabled:

All the GPIOs can be configured in tri-state with an internal active pull-down enabled, as a not used pin, setting the parameter <gpio_mode> of the +UGPIOC AT command to 255.

The “Pad disabled” mode can be provided on more than one pin per time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

The pin configured to provide the “Pad disabled” function is set as

- Tri-state with an internal active pull-down enabled

Table 42 describes the configurations of all the GPIO pins.

Pin	Name	Description	Remarks
20	**GPIO1**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the AT+UGPIOC command as: • Output • Input • Network Status Indication • GNSS Supply Enable • GSM Tx Burst Indication • Module Status Indication
21	**GPIO2**	GPIO	By default, the pin is configured to provide GNSS Supply Enable function. Can be alternatively configured by the +UGPIOC command as: • Output • Input • Network Status Indication • Pad disabled

Pin	Name	Description	Remarks
23	**GPIO3**	GPIO	By default, the pin is configured to provide GNSS Data Ready function. Can be alternatively configured by the +UGPIOC command as: • Output • Input • Network Status Indication • GNSS Supply Enable • Pad disabled
24	**GPIO4**	GPIO	By default, the pin is configured to provide GNSS RTC sharing function. Can be alternatively configured by the +UGPIOC command as: • Output • Input • Network Status Indication • GNSS Supply Enable • Pad disabled
51	**GPIO5**	GPIO	By default, the pin is configured to provide SIM card detection function. Can be alternatively configured by the +UGPIOC command as: • Output • Input • Network Status Indication • GNSS Supply Enable • Module Operating Mode Indication • Pad disabled
39	**I2S1_RXD / GPIO6**	2nd I²S receive data / GPIO	By default, the pin is configured as 2nd I²S receive data input. Can be alternatively configured by the +UGPIOC, +USPM commands as: • Output • Input • Pad disabled
40	**I2S1_TXD / GPIO7**	2nd I²S transmit data / GPIO	By default, the pin is configured as 2nd I²S transmit data output. Can be alternatively configured by the +UGPIOC, +USPM commands as: • Output • Input • Pad disabled
53	**I2S1_CLK / GPIO8**	2nd I²S clock / GPIO	By default, the pin is configured as 2nd I²S clock input/output. Can be alternatively configured by the +UGPIOC, +USPM commands as: • Output • Input • Pad disabled
54	**I2S1_WA / GPIO9**	2nd I²S word alignment / GPIO	By default, the pin is configured as 2nd I²S word alignment input/output. Can be alternatively configured by the +UGPIOC, +USPM commands as: • Output • Input • Pad disabled
55	**SPI_SCLK / GPIO10**	SPI Serial Clock / GPIO	By default, the pin is configured as SPI Serial Clock Input: • Idle low (CPOL=0) • Internal active pull-down to GND enabled Can be alternatively configured by the +UGPIOC command as: • Output • Input • Pad disabled
56	**SPI_MOSI / GPIO11**	SPI Data Line / GPIO	By default, the pin is configured as SPI Data Line Input: • Shift data on rising clock edge (CPHA=1) • Latch data on falling clock edge (CPHA=1) • Idle high • Internal active pull-up to V_INT enabled Can be alternatively configured by the +UGPIOC command as: • Output • Input • Pad disabled

Pin	Name	Description	Remarks
57	**SPI_MISO / GPIO12**	SPI Data Line Output / GPIO	By default, the pin is configured as SPI Data Line Output: • Shift data on rising clock edge (CPHA=1) • Latch data on falling clock edge (CPHA=1) • Idle high Can be alternatively configured by the +UGPIOC command as: • Output • Input • Pad disabled
58	**SPI_SRDY / GPIO13**	SPI Slave Ready / GPIO	By default, the pin is configured as SPI Slave Ready Output: • Idle low Can be alternatively configured by the +UGPIOC command as: • Output • Input • Module Status Indication • Pad disabled
59	**SPI_MRDY / GPIO14**	SPI Master Ready / GPIO	By default, the pin is configured as SPI Master Ready Input: • Idle low • Internal active pull-down to GND enabled Can be alternatively configured by the +UGPIOC command as: • Output • Input • Module Operating Mode Indication • Pad disabled

Table 42: GPIO pin configurations

☞ The GPIO pins' ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the lines are externally accessible on the application board. Higher protection levels can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins, close to accessible points.

An application circuit for a typical GPIOs usage is described in Figure 52:

- Network indication function provided by the **GPIO1** pin
- GNSS supply enable function provided by the **GPIO2** pin
- GNSS data ready function provided by the **GPIO3** pin
- GNSS RTC sharing function provided by the **GPIO4** pin
- SIM card detection function provided by the **GPIO5** pin

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series with the GPIO.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

☞ Any external signal connected to GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low, and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the module cannot be tri-stated, insert a multi-channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power-down mode, when the external reset is forced low, and during the power-on sequence.

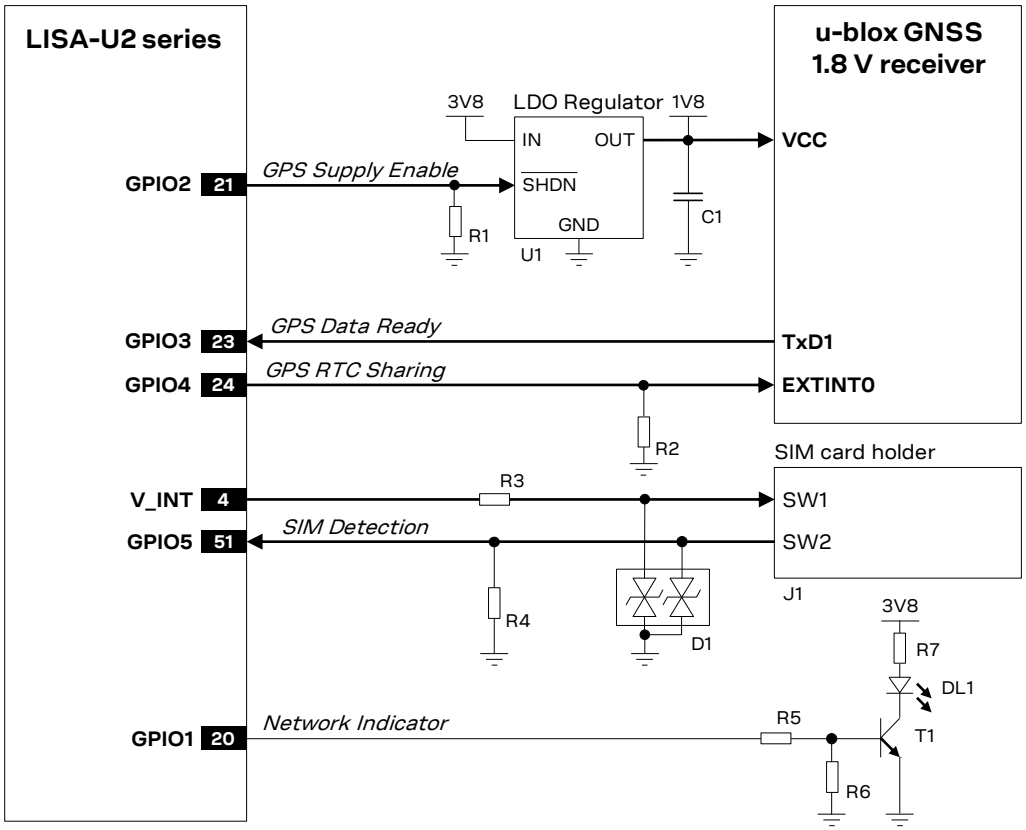


Figure 52: GPIO application circuit

Reference	Description	Part Number - Manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	Voltage Regulator for GNSS receiver	See GNSS Module Hardware Integration Manual
R2	4.7 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	1 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R4	470 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
D1	ESD Transient Voltage Suppressor	USB0002RP or USB0002DP - AVX
J1	SIM Card Holder	CCM03-3013LFT R102 - C&K Components (or equivalent)
R5	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R6	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R7	820 Ω Resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED Red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 43: Components for a GPIO application circuit

The recommended application circuit for the module status indication function, provided by LISA-U2 series module **GPIO1** and **GPIO13** pins to indicate module status (power-off mode, i.e. module switched off, versus idle, active or connected mode, i.e. module switched on), is described in Figure 53.

The logic level of the pin configured to provide the module status indication, that is set high when the module is switched on (with interfaces configured) and low when the module is switched off, is inverted by a transistor biased by the **V_BCKP** supply, which is generated by the module when a valid **VCC** is applied.

A pull-down resistor is provided at the **GPIO1** output (which provides module status indication) to fix a low level at inverting transistor input when **GPIO1** is floating, i.e. when the module is switched off, so that high logic level is present at the application processor input when the module is switched off and low logic level when the module is switched on (i.e. the opposite logic level of the GPIO).

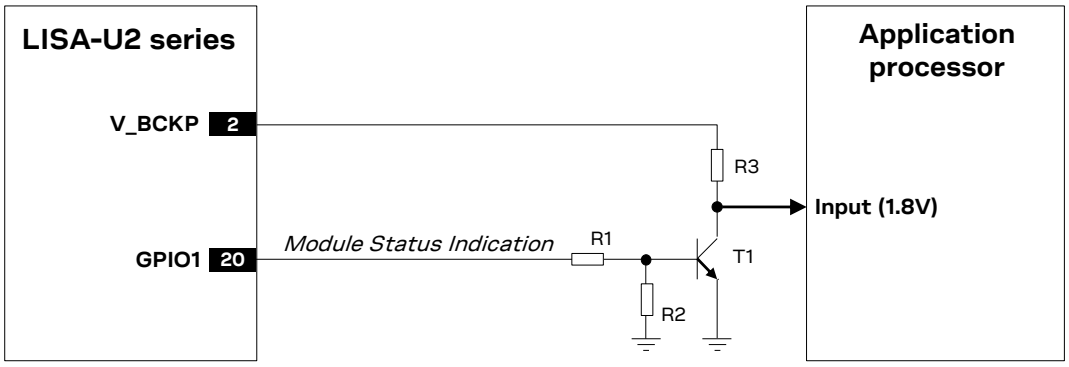


Figure 53: Module status indication application circuit

Reference	Description	Part Number - Manufacturer
R1, R3	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	100 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
T1	NPN BJT Transistor	BC847 - Infineon

Table 44: Components for a module status indication application circuit

1.13 Reserved pins (RSVD)

LISA-U2 modules have pins reserved for future use. All the **RSVD** pins, except pin number **5**, can be left unconnected on the application board.

☞ Pin **5** (**RSVD**) must be connected to GND.

1.14 Schematic for LISA-U2 module integration

Figure 54 is an example of a schematic diagram where the LISA-U2 series module is integrated into an application board, using all the interfaces of the module.

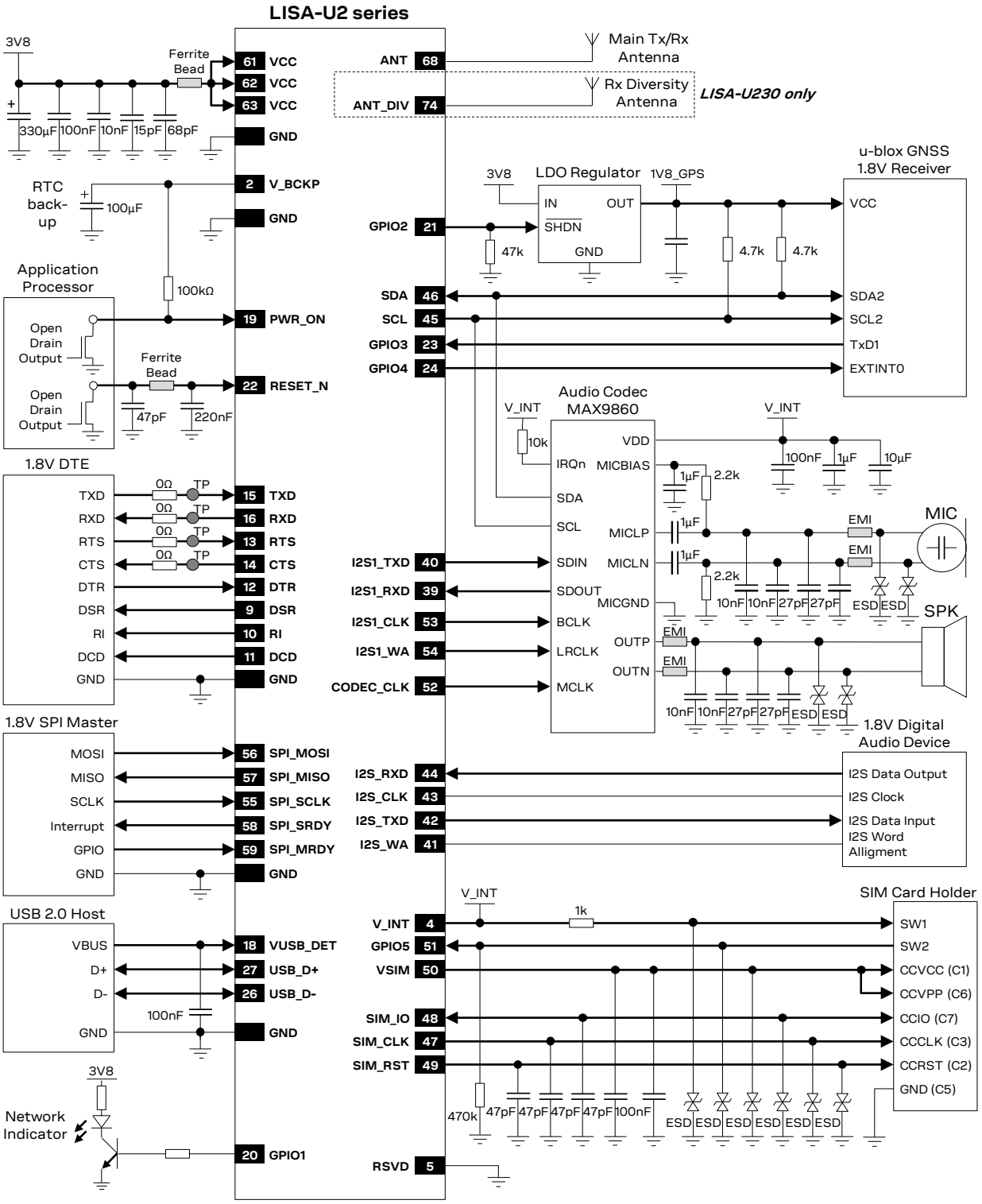


Figure 54: Example of a schematic diagram to integrate LISA-U2 modules in an application board, using all the interfaces

1.15 Approvals

☞ For all the certificates of compliancy and for the complete list of approvals (including countries' and network operators' approvals) of LISA-U2 series modules, see our website (http://www.u-blox.com/) or contact the u-blox office or sales representative nearest you.

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called "certification schemes" that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, as:
    - CE (Conformité Européenne) marking for European Union
    - FCC (Federal Communications Commission) approval for United States
- Industry conformance certification
  - Telecom industry specific approval verifying interoperability between devices and networks:
    - GCF (Global Certification Forum), partnership between device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator specific approval required by some mobile network operator:
    - AT&T network operator in United States

Even if LISA-U2 modules are approved under all major certification schemes, the application device that integrates LISA-U2 modules must be approved under all the certification schemes required by the specific application device to be deployed in the market.

The required certification scheme approvals and the related testing specifications differ depending on the country or the region where the device that integrates LISA-U2 modules will be deployed, on the corresponding vertical market of the device, on the type, features and functionalities of the whole application device, and on the network operators where the device must operate.

☞ The certification of the application device that integrates a LISA-U2 module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

LISA-U2 modules are certified according to all capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to 3GPP TS 51.010-2 [9] and 3GPP TS 34.121-2 [10], is a statement of the implemented and supported capabilities and options of a device.

☞ The PICS document of the application device integrating LISA-U2 series modules must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device. For more details regarding the AT commands settings that affect the PICS, see u-blox AT Commands Manual [2].

☞ Check the specific settings required for mobile network operators approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.

1.15.1 European Conformance CE mark

LISA-U2 series modules have been evaluated against the essential requirements of the Radio Equipment Directive (2014/53/EU).

In order to satisfy the essential requirements of the Radio Equipment Directive (2014/53/EU), the modules are compliant with the following standards:

- Radio Frequency spectrum efficiency (Article 3.2):
  - EN 301 511
  - EN 301 908-1
  - EN 301 908-2
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-52
- Safety (Article 3.1a):
  - EN 60950-1
  - EN 62311

The conformity assessment procedure for the LISA-U2 series modules, referred to in Article 17 and detailed in Annex II of the Radio Equipment Directive (2014/53/EU), has been followed.

Thus, the following marking is included in the product:

CE

⚠ Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for LISA-U200 and LISA-U230 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.37 dBi (900 MHz, i.e. GSM 900 or UMTS FDD-8 band), 10.45 dBi (1800 MHz, i.e. GSM 1800), 14.10 dBi (2100 MHz, i.e. UMTS FDD-1 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U201 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 5.76 dBi (900 MHz, i.e. GSM 900 or UMTS FDD-8 band), 11.44 dBi (1800 MHz, i.e. GSM 1800 band), 13.70 dBi (2100 MHz, i.e. UMTS FDD-1 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U260 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.11 dBi (900 MHz, i.e. GSM 900 band), 9.86 dBi (1800 MHz, i.e. GSM 1800 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U270 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.22 dBi (900 MHz, i.e. GSM 900 or UMTS FDD-8 band), 10.50 dBi (1800 MHz, i.e. GSM 1800 band), 14.75 dBi (2100 MHz, i.e. UMTS FDD-1 band) for mobile and fixed or mobile operating configurations.

1.15.2 US Federal Communications Commission notice

The Federal Communications Commission (FCC) IDs for the LISA-U2 modules are:

- LISA-U200: XPYLISAU200
- LISA-U201: XPYLISAU201
- LISA-U230: XPYLISAU230
- LISA-U260: XPYLISAU200
- LISA-U270: XPYLISAU200

1.15.2.1 Safety warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed

1.15.2.2 Declaration of conformity

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC procedures and as authorized in the module certification filing.

⚠ The gain of the system antenna(s) used for LISA-U200 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.25 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band), 7.30 dBi (in 1700 MHz, i.e. AWS or UMTS FDD-4 band) and 2.74 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U201 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.0 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band) and 3.5 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U230 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.78 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band), 7.55 dBi (in 1700 MHz, i.e. AWS or UMTS FDD-4 band) and 3.95 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U260 and LISA-U270 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.88 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band) and 4.08 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

1.15.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating the LISA-U2 modules are authorized to use the FCC Grants of the LISA-U2 modules for their own final products according to the conditions referenced in the certificates.

⚠ The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

- LISA-U200: "Contains FCC ID: XPYLISAU200" resp.
- LISA-U201: "Contains FCC ID: XPYLISAU201" resp.
- LISA-U230: "Contains FCC ID: XPYLISAU230" resp.
- LISA-U260: "Contains FCC ID: XPYLISAU200" resp.
- LISA-U270: "Contains FCC ID: XPYLISAU200" resp.

⚠ IMPORTANT: Manufacturers of portable applications incorporating the LISA-U2 modules are required to have their final product certified and apply for their own FCC grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

1.15.3 Innovation, Science, Economic Development Canada notice

The ISED Canada (formerly known as IC - Industry Canada) Certification Numbers are:

- LISA-U200: 8595A-LISAU200N
- LISA-U201: 8595A-LISAU201
- LISA-U230: 8595A-LISAU230N
- LISA-U260: 8595A-LISAU200N
- LISA-U270: 8595A-LISAU200N

1.15.3.1 Declaration of conformity

⚠ Radiofrequency radiation exposure Information: this equipment complies with IC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with IC procedures and as authorized in the module certification filing.

⚠ The gain of the system antenna(s) used for LISA-U200 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.25 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band), 7.30 dBi (in 1700 MHz, i.e. AWS or UMTS FDD-4 band) and 2.74 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U201 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 0.7 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band) and 3.5 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U230 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.78 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band), 7.55 dBi (in 1700 MHz, i.e. AWS or UMTS FDD-4 band) and 3.95 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

⚠ The gain of the system antenna(s) used for LISA-U260 and LISA-U270 (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.88 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 band) and 4.08 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 band) for mobile and fixed or mobile operating configurations.

1.15.3.2 Modifications

The IC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating the LISA-U2 modules are authorized to use the Industry Canada Certificates of the LISA-U2 modules for their own final products according to the conditions referenced in the certificates.

⚠ The IC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

- LISA-U200: "Contains IC: 8595A-LISAU200N" resp.
- LISA-U201: "Contains IC: 8595A-LISAU201" resp.
- LISA-U230: "Contains IC: 8595A-LISAU230" resp.
- LISA-U260: "Contains IC: 8595A-LISAU200N" resp.
- LISA-U270: "Contains IC: 8595A-LISAU200N" resp.

⚠ Canada, Industry Canada (IC) Notices

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B) and RSS-210. Operation is subject to the following two conditions:

- this device may not cause interference
- this device must accept any interference, including interference that may cause undesired operation of the device

Radio Frequency (RF) Exposure Information
The radiated output power of the u-blox Cellular Module is below the Industry Canada (IC) radio frequency exposure limits. The u-blox Cellular Module should be used in such a manner such that the potential for human contact during normal operation is minimized.
This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20cm from a person's body).
This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address:
http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng
Additional Canadian information on RF exposure also can be found at the following web address:
http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

⚠ IMPORTANT: Manufacturers of portable applications incorporating the LISA-U2 modules are required to have their final product certified and apply for their own Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

⚠ Canada, avis d'Industrie Canada (IC)

Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3(B) / NMB-3(B) et RSS-210.
Son fonctionnement est soumis aux deux conditions suivantes:

- cet appareil ne doit pas causer d'interférence
- cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Industrie Canada (IC). Utilisez l'appareil de sans fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.
Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).
Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur:
http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra
Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur : http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

⚠ IMPORTANT: les fabricants d'applications portables contenant les modules LISA-U2 series doivent faire certifier leur produit final et déposer directement leur candidature pour un certificat Industrie Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

1.15.4 Australian Regulatory Compliance Mark

LISA-U200-01, LISA-U201-03 and LISA-U230 modules are compliant with the standards made by the Australian Communications and Media Authority (ACMA) under Section 376 of the Telecommunications Act 1997.

The ACMA recommends that telephones be able to support access to emergency numbers (such as 000) for at least 30 minutes during a power failure. For telephones that do not function during a power failure, the technical standard suggests that a warning notice be included in the instructions, advising users that the phone will not operate if there is a power failure.

⚠ It is the customer's responsibility to determine if their product is subject to such recommendations and apply the warning notice requirement as appropriate.

1.15.5 ICASA Certification

LISA-U200 and LISA-U270 modules are certified by the Independent Communications Authority of South Africa (ICASA).

1.15.6 KCC Certification

LISA-U200 and LISA-U270 modules are certified by the Korea Communications Commission (KCC).

KCC ID for LISA-U2 modules:

- LISA-U200: KCC-CRM-ULX-LISA-U200
- LISA-U270: KCC-CRM-ULX-LISA-U270

1.15.7 ANATEL Certification

LISA-U200 and LISA-U201 modules are certified by the Brazilian Agency of Telecommunications (Agência Nacional de Telecomunicações in Portuguese) (ANATEL).

Anatel IDs for LISA-U200 modules:

- EAN barcode: (01)0 789 8941 57508 3
- Homologation number 3309-12-8459

Anatel IDs for LISA-U201 modules:

- EAN barcode: (01)0 789 8941 57526 7
- Homologation number 4466-15-5903

1.15.8 CCC Certification

LISA-U200, LISA-U201, LISA-U230 and LISA-U270 modules are CCC approved (Chinese Compulsory Certification)

1.15.9 Giteki Certification

LISA-U200-62S, LISA-U270-62S, LISA-U270-63S and LISA-U270-68S modules comply with Japanese Telecom [T] and Radio [R] Law and have the Giteki mark placed on the product label.

- LISA-U200-62S:
  - T: AD120274003
  - R: 003-120375
- LISA-U270-62S, LISA-U270-63S and LISA-U270-68S:

- T: AD120274003
- R: 003-120377

2 Design-In

2.1 Design-in checklist

This section provides a design-in checklist.

2.1.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☐ DC supply must provide a nominal voltage at the **VCC** pin above the minimum operating range limit.
- ☐ DC supply must be capable of providing 2.5 A current pulses, providing a voltage at the **VCC** pin above the minimum operating range limit and with a maximum 400 mV voltage drop from the nominal value.
- ☐ **VCC** supply should be clean, with very low ripple/noise: provide the suggested series ferrite bead and bypass capacitors, in particular if the application device integrates an internal antenna.
- ☐ **VCC** voltage must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module.
- ☐ Do not leave **PWR_ON** floating: add a pull-up resistor to **V_BCKP**.
- ☐ Do not apply loads which might exceed the limit for maximum available current from the **V_INT** supply.
- ☐ Check that the voltage level of any connected pin does not exceed the specific operating range.
- ☐ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☐ Insert the suggested low capacitance ESD protection and passive filtering parts on each SIM signal.
- ☐ Check the UART signal directions, since the signal names follow the ITU-T V.24 Recommendation [3].
- ☐ Provide appropriate access to the USB interface and/or to the UART **RxD**, **TxD** lines and access to the **PWR_ON** and/or **RESET_N** lines to flash/upgrade the module firmware using the u-blox EasyFlash tool.
- ☐ Provide appropriate access to the USB interface and/or to the UART **RxD**, **TxD**, **CTS**, **RTS** lines for debugging purposes.
- ☐ Capacitance and series resistance must be limited on each line of the SPI / IPC interface.
- ☐ Add a suitable pull-up resistor to an appropriate supply on each DDC (I^2C) interface line, if the interface is used.
- ☐ Capacitance and series resistance must be limited on each line of the DDC interface.
- ☐ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☐ Connect pin number 5 (**RSVD**) to ground.
- ☐ Check the digital audio interface specifications to connect a relevant device.
- ☐ Capacitance and series resistance must be limited on the **CODEC_CLK** line and each I^2S interface line.
- ☐ Provide suitable precautions for ESD immunity as required on the application board.
- ☐ Any external signal connected to the UART interface, SPI/IPC interface, I^2S interfaces and GPIOs must be tri-stated when the module is in power-down mode, when the external reset is forced low, and during the module power-on sequence (at least for 3 seconds after the start-up event), to avoid latch-up of circuits and enable a clean boot of the module.

- ☐ All unused pins can be left floating on the application board except the **PWR_ON** pin (must be connected to **V_BCKP** by a pull-up resistor) and **RSVD** pin number 5 (must be connected to GND).

2.1.2 Layout checklist

The following are the most important points for a simple layout check:

- ☐ Check the 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** pad (main RF input/output) and to the **ANT_DIV** pad (RF input for Rx diversity).
- ☐ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☐ Ensure no coupling occurs with other noisy or sensitive signals (e.g. SIM signals).
- ☐ The **VCC** line should be as wide and as short as possible.
- ☐ Provide the suggested series ferrite bead and bypass capacitors close to the **VCC** pins implementing the recommended layout and placement, especially if the application device integrates an internal antenna.
- ☐ Route the **VCC** supply line away from sensitive analog signals.
- ☐ The high-power audio outputs lines on the application board must be wide enough to minimize series resistance.
- ☐ Ensure proper grounding.
- ☐ Consider “No-routing” areas for the Data Module footprint.
- ☐ Optimize placement for minimum length of RF line and closer path from the DC source for **VCC**.
- ☐ Design the **USB_D+ / USB_D-** connection as 90 Ω differential pair, with 30 Ω common mode impedance.
- ☐ Keep routing short and minimize parasitic capacitance on the SPI lines to preserve signal integrity.
- ☐ Keep routing short and minimize parasitic capacitance on **CODEC_CLK** line to preserve signal integrity.

2.1.3 Antenna checklist

- ☐ Antenna should have 50 Ω impedance, VSWR less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☐ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☐ Follow the additional guidelines for products marked with the FCC logo (United States only) reported in section 1.15.2.2
- ☐ The antenna connected to the **ANT** pad should have built-in DC resistor to ground to get proper antenna detection functionality.
- ☐ The antenna for the Rx diversity connected to the **ANT_DIV** pin should be carefully separated from the main Tx/Rx antenna connected to the **ANT** pin: the distance between the two antennas should be at least greater than half a wavelength of the lowest used frequency (i.e. distance greater than ~20 cm, for 2G/3G low bands) to distinguish between different multipath channels, for proper spatial diversity implementation.

2.2 Design Guidelines for Layout

The following design guidelines must be met for optimal integration of LISA-U2 modules on the final application board.

2.2.1 Layout guidelines per pin function

This section groups LISA-U2 modules pins by signal function and provides a ranking of importance in layout design.

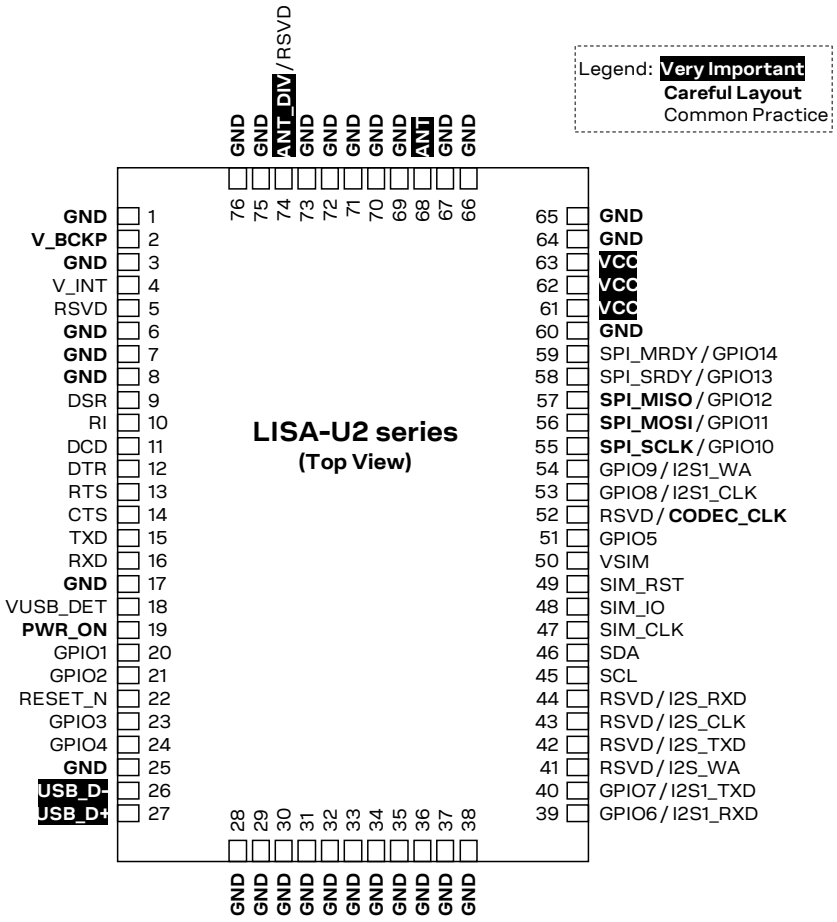


Figure 55: LISA-U2 series modules pin-out (top view) with ranked importance for layout design

Rank	Function	Pin(s)	Layout	Remarks
1st	**RF Antenna**			
	Main RF input/output	**ANT**	**Very Important**	Design for 50 Ω characteristic impedance. See section 2.2.1.1
	RF input for Rx diversity	**ANT_DIV**	**Very Important**	Design for 50 Ω characteristic impedance. See section 2.2.1.1
2nd	**Main DC Supply**	**VCC**	**Very Important**	**VCC** line should be wide and short. Route away from sensitive analog signals. See section 2.2.1.2
3rd	**USB Signals**	**USB_D+** **USB_D-**	**Very Important**	Route USB_D+ and USB_D- as differential lines: design for 90 Ω differential impedance (Z_0) and design for 30 Ω common mode impedance (Z_{CM}). See section 2.2.1.3
4th	**Ground**	**GND**	**Careful Layout**	Provide proper grounding. See section 2.2.1.4
5th	**Sensitive Pin:**		**Careful Layout**	Avoid coupling with noisy signals. See section 2.2.1.5
	Backup Voltage	**V_BCKP**		
	Power-On	**PWR_ON**		
6th	**High-speed digital pins:**		**Careful Layout**	Avoid coupling with sensitive signals. See section 2.2.1.6
	SPI Signals	**SPI_SCLK, SPI_MISO, SPI_MOSI, SPI_SRDY, SPI_MRDY**		
	Clock Output	**CODEC_CLK**		
7th	**Digital pins and supplies:**		Common Practice	Follow common practice rules for digital pin routing. See section 2.2.1.7
	SIM Card Interface	VSIM, SIM_CLK, SIM_IO, SIM_RST		
	Digital Audio	I2S_CLK, I2S_RXD, I2S_TXD, I2S_WA, I2S1_CLK, I2S1_RXD, I2S1_TXD, I2S1_WA		
	DDC	SCL, SDA		
	UART	TXD, RXD, CTS, RTS, DSR, RI, DCD, DTR		
	External Reset	RESET_N		
	General Purpose I/O	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO11, GPIO12, GPIO13, GPIO14		
	USB detection	VUSB_DET		
	Supply for Interfaces	V_INT		

Table 45: Pin list in order of decreasing importance for layout design

2.2.1.1 RF antenna connection

The **ANT** pin (main RF input/output) and the **ANT_DIV** pin (RF input for diversity receiver provided by LISA-U230 modules) are very critical in layout design.

Proper transition between **ANT** and **ANT_DIV** pads and the application board must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** and **ANT_DIV** pads:

- On a multi layer board, the whole layer stack below the RF connection should be free of digital lines
- Increase GND keep-out (i.e. clearance) for **ANT** and **ANT_DIV** pads to at least 250 µm up to adjacent pads metal definition and up to 500 µm on the area below the module, as described in Figure 56
- Add GND keep-out (i.e. clearance) on buried metal layers below **ANT** and **ANT_DIV** pads and below any other pad of component present on the RF line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground (see Figure 56 for the description of the GND keep-out area below **ANT** and **ANT_DIV** pads)

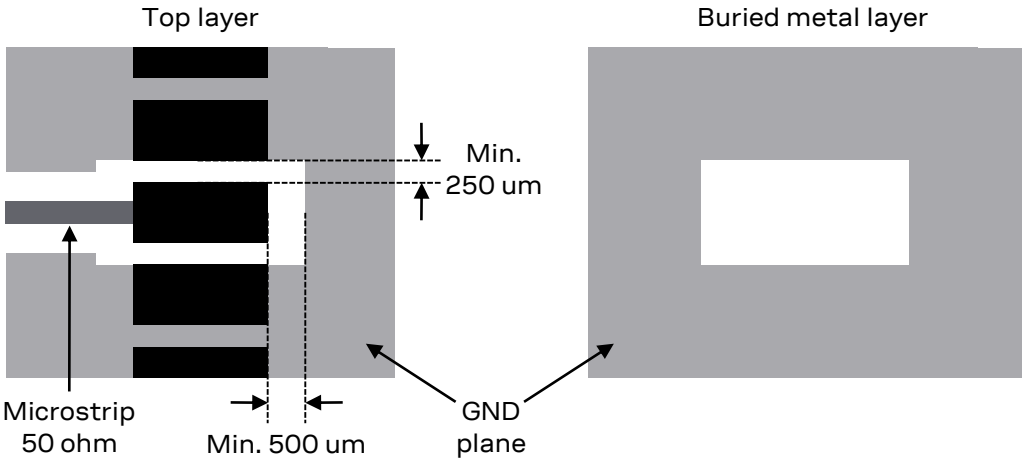


Figure 56: GND keep-out area on top layer around ANT and ANT_DIV pads and on buried layer below ANT and ANT_DIV pads

The transmission line from the **ANT** pad and the **ANT_DIV** pad up to antenna connector(s) or up to the internal antenna(s) pad must be designed so that the characteristic impedance is as close as possible to 50 Ω.

- The transmission line up to antenna connector or pad may be a microstrip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). In any case must be designed to achieve 50 Ω characteristic impedance
- Microstrip lines are usually easier to implement and the reduced number of layer transitions up to antenna connector simplifies the design and diminishes reflection losses. However, the electromagnetic field extends to the free air interface above the stripline and may interact with other circuitry
- Buried striplines exhibit better shielding to external and internally generated interferences. They are therefore preferred for sensitive application. In case a stripline is implemented, carefully check that the via pad-stack does not couple with other signals on the crossed and adjacent layers

Figure 57 and Figure 58 provide two examples of proper 50 Ω coplanar waveguide designs. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

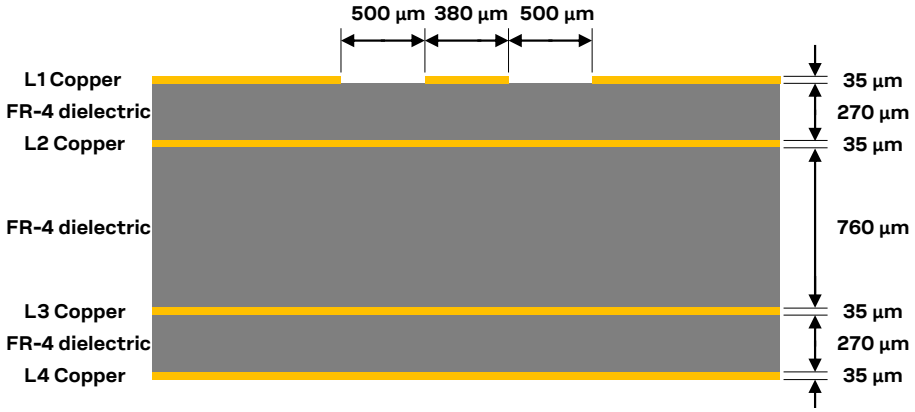


Figure 57: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

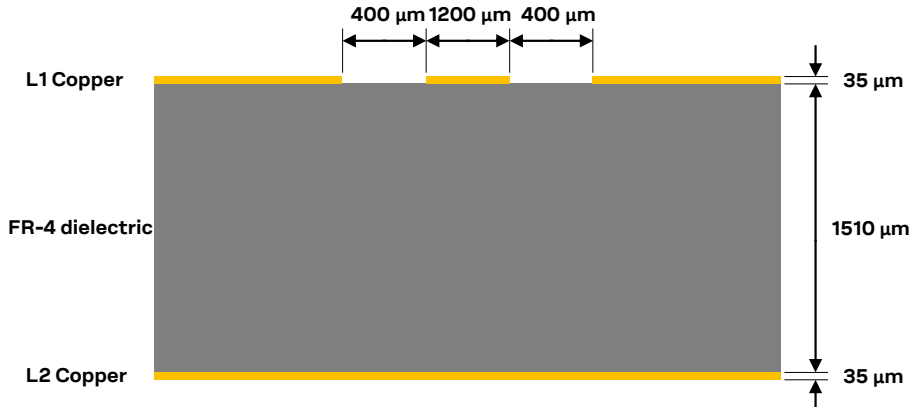


Figure 58: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB layup, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 57 and Figure 58)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 57, 1510 µm in Figure 58)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 57 and Figure 58)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 57, 400 µm in Figure 58)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the microstrip, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for the RF line design:

- Minimize the transmission line length; the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB
- The transmission line should not have abrupt change to thickness and spacing to GND, but must be uniform and routed as smoothly as possible

- The transmission line must be routed in a section of the PCB where minimal interference from noise sources can be expected
- Route RF transmission line far from other sensitive circuits as it is a source of electromagnetic interference
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer
- Add GND vias around transmission line
- Ensure no other signals are routed parallel to transmission line, or that other signals cross on adjacent metal layer
- If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the microstrip, use the “Coplanar Waveguide” model for 50 Ω characteristic impedance calculation
- Do not route microstrip line below discrete component or other mechanics placed on top layer
- When terminating transmission line on antenna connector (or antenna pad) it is very important to strictly follow the connector manufacturer’s recommended layout
- GND layer under RF connectors and close to buried vias should be cut out in order to remove stray capacitance and thus keep the RF line 50 Ω. In most cases the large active pad of the integrated antenna or antenna connector needs to have a GND keep-out (i.e. clearance) at least on first inner layer to reduce parasitic capacitance to ground. Note that the layout recommendation is not always available from connector manufacturer: e.g. the classical SMA Pin-Through-Hole needs to have GND cleared on all the layers around the central pin up to annular pads of the four GND posts. Check 50 Ω impedance of **ANT** and **ANT_DIV** lines
- Ensure no coupling occurs with other noisy or sensitive signals
- The antenna for the Rx diversity should be carefully separated from the main Tx/Rx antenna to ensure that uncorrelated signals are received at each antenna, because signal improvement is dependent on the cross correlation and the signal strength levels between the two received signals. The distance between the two antennas should be greater than half a wavelength of the lowest used frequency (i.e. distance greater than ~20 cm, for 2G/3G low bands) to distinguish between different multipath channels, for proper spatial diversity implementation

☞ Any RF transmission line on PCB should be designed for 50 Ω characteristic impedance.

☞ Ensure no coupling occurs with other noisy or sensitive signals.

2.2.1.2 Main DC supply connection

The DC supply of LISA-U2 modules is very important for the overall performance and functionality of the integrated product. For detailed description, check the design guidelines in section 1.5.2. Some main characteristics are:

- **VCC** pins are internally connected, but it is recommended to use all the available pins in order to minimize the power loss due to series resistance
- **VCC** connection may carry a maximum burst current in the order of 2.5 A. Therefore, it is typically implemented as a wide PCB line with short routing from DC supply (DC-DC regulator, battery pack, etc)
- The module automatically initiates an emergency shutdown if supply voltage drops below hardware threshold. In addition, reduced supply voltage can set a worst case operation point for RF circuitry that may behave incorrectly. It follows that each voltage drop in the DC supply track will restrict the operating margin at the main DC source output. Therefore, the PCB connection must exhibit a minimum or zero voltage drop. Avoid any series component with Equivalent Series Resistance (ESR) greater than a few milliohms

- Given the large burst current, **VCC** line is a source of disturbance for other signals. Therefore route **VCC** through a PCB area separated from sensitive analog signals. Typically it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing
- The **VCC** supply current supply flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source
- A tank bypass capacitor with low ESR is recommended to smooth current spikes. This is most effective when placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and LISA-U2 module tank capacitor. Note that the capacitor voltage rating may be adequate to withstand the charger over-voltage if battery-pack is used. The use of very large capacitors (i.e. greater then 1000 µF) must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module
- **VCC** is directly connected to the RF power amplifiers. It is highly recommended to place a series ferrite bead for GHz band noise, a bypass capacitor with Self-Resonant Frequency in 800/900 MHz range and a bypass capacitor with self-resonant frequency in 1800/1900 MHz range as close as possible to the **VCC** pins, especially if the application device integrates an internal antenna. This is described in Figure 9 and Table 10.
- Since **VCC** is directly connected to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the LISA-U2 modules in the worst case
- The large current generates a magnetic field that is not well isolated by PCB ground layers and which may interact with other analog modules (e.g. VCO) even if placed on opposite side of PCB. In this case route **VCC** away from other sensitive functional units
- The typical GSM burst has a periodic nature of approx. 217 Hz, which lies in the audible audio range. Avoid coupling between **VCC** and audio lines (especially microphone inputs)
- If **VCC** is protected by transient voltage suppressor / reverse polarity protection diode to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the LISA-U2 module, preferably closer to the DC source (otherwise functionality may be compromised)

☞ **VCC** line should be as wide and as short as possible.

☞ Route away from sensitive analog signals.

2.2.1.3 USB signal

The LISA-U2 modules include a high-speed USB 2.0 compliant interface with a maximum throughput of 480 Mbit/s (see Section 1.9.3). Signals **USB_D+** / **USB_D-** carry the USB serial data and signaling. The lines are used in single-ended mode for relatively low speed signaling handshake, as well as in differential mode for fast signaling and data transfer. Characteristic impedance of **USB_D+** / **USB_D-** lines is specified by USB standard. The most important parameter is the differential characteristic impedance applicable for odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential: signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

- Route **USB_D+** / **USB_D-** lines as a differential pair
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω
- Consider design rules for **USB_D+** / **USB_D-** similar to RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area

Figure 59 and Figure 60 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

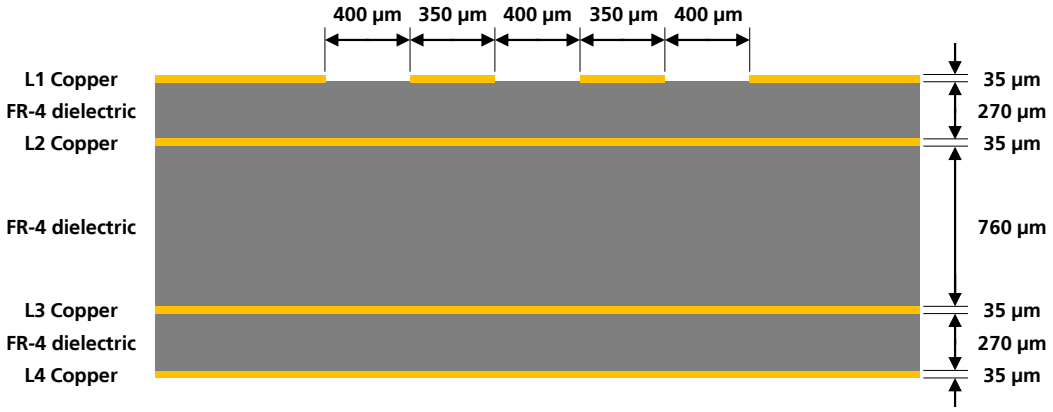


Figure 59: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

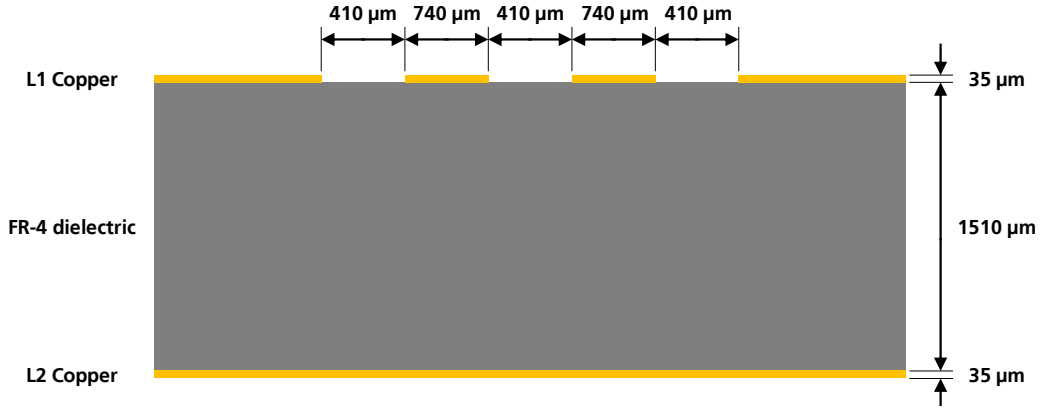


Figure 60: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.2.1.4 Module grounding

Good connection of the module with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer
- If the application board is a multilayer PCB, then it is required to connect together each GND area with complete via stack down to main board ground layer
- It is recommended to implement one layer of the application board as ground plane
- Good grounding of **GND** pads will also ensure thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating

2.2.1.5 Other sensitive pins

A few other pins on the LISA-U2 modules requires careful layout.

- **RTC supply (V_BCKP):** avoid injecting noise on this voltage domain as it may affect RTC oscillator stability
- **Power-On (PWR_ON):** is the digital input to switch-on the LISA-U2 modules. Ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request

2.2.1.6 High-speed digital pins

The following high speed digital pins require careful layout:

- **Serial Peripheral Interface (SPI)**: can be used for high speed data transfer (UMTS/HSPA) between the LISA-U2 modules and the host processor, with a data rate up to 26 Mbit/s (see Section 1.9.3). The high-speed data rate is carried by signals **SPI_SCLK**, **SPI_MISO** and **SPI_MOSI**, while **SPI_SRDY** and **SPI_MRDY** behave as handshake signals with relatively low activity
- **Digital Clock Output (CODEC_CLK)**: can be used to provide a 26 MHz or 13 MHz digital clock to an external audio codec

Follow these hints for high speed digital pins layout:

- High-speed signals become sources of digital noise, route away from RF and other sensitive analog signals
- Keep routing short and minimize parasitic capacitance to preserve digital signal integrity
- It is recommended to match the length of SPI signals

2.2.1.7 Digital pins and supplies

- **External Reset (RESET_N):** input for external reset, a logic low voltage will reset the module
- **SIM Card Interface (VSIM, SIM_CLK, SIM_IO, SIM_RST)**: the SIM layout may be critical if the SIM card is placed far away from the LISA-U2 modules or in close proximity to the RF antenna. In the first case the long connection can cause the radiation of some harmonics of the digital data frequency. In the second case the same harmonics can be picked up and create self-interference that can reduce the sensitivity of GSM Receiver channels whose carrier frequency is coincidental with harmonic frequencies. The latter case, placing the RF bypass capacitors, suggested in the section 1.8, near the SIM connector will mitigate the problem. In addition, since the SIM card is

typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection to protect module SIM pins near the SIM connector

- **Digital Audio (I2S_CLK**, **I2S_RX**, **I2S_TX**, **I2S_WA** and **I2S1_CLK**, **I2S1_RXD**, **I2S1_TXD**, **I2S1_WA)**: the I^2S interface requires the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **DDC (SCL, SDA)**: the DDC interface requires the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **UART (TXD, RXD, CTS, RTS, DSR, RI, DCD, DTR)**: the serial interface requires the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs
- **General Purpose I/O (GPIOx)**: the general purpose input/output pins are generally not critical for layout
- **Reserved pins**: these pins are reserved for future use. Leave them unconnected on the baseboard
- **USB detection (VUSB_DET)**: this input will generate an interrupt to the baseband processor for USB detection. The USB supply (5.0 V typ.) must be provided to **VUSB_DET** by the connected USB host to enable the USB interface of the module
- **Interfaces Supply (V_INT)**: this supply output is generated by an integrated switching step down converter, used internally to supply the digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals

2.2.2 Footprint and paste mask

The following figure describes the footprint and provides recommendations for the paste mask for LISA-U2 modules. These are recommendations only and not specifications. Note that the copper and solder masks have the same size and position.

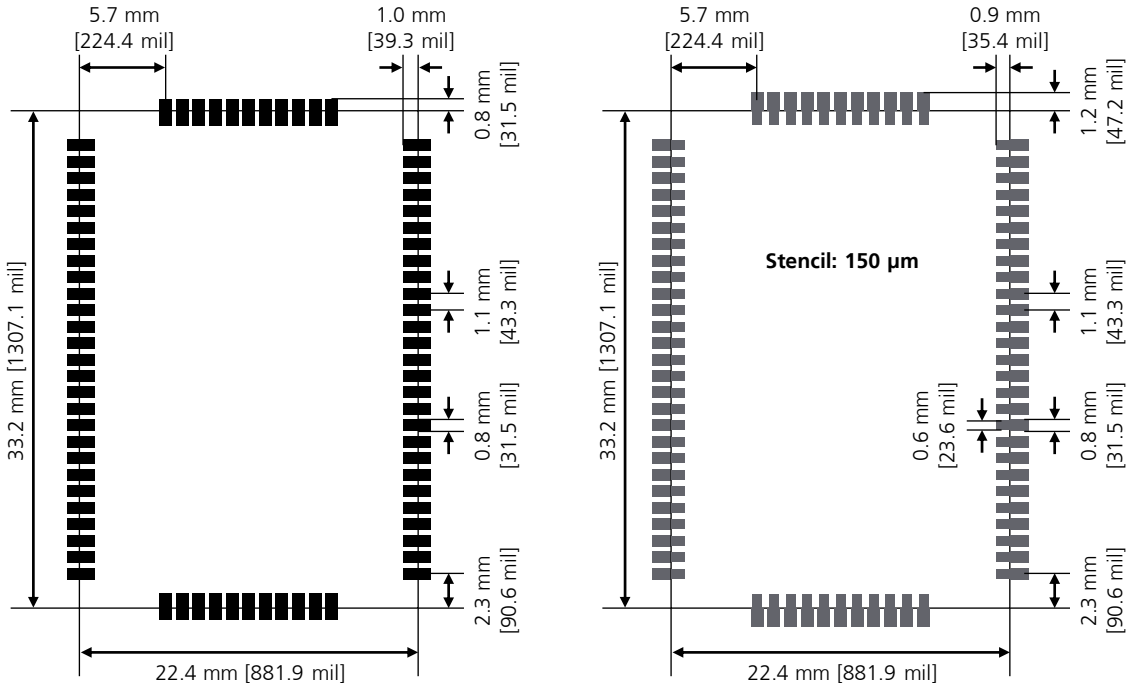


Figure 61: LISA-U2 modules suggested footprint and paste mask

To improve the wetting of the half vias, reduce the amount of solder paste under the module and increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the copper mask. The solder paste should have a total thickness of 150 µm.

☞ The paste mask outline needs to be considered when defining the minimal distance to the next component.

☞ The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

The implemetation of a step stencil (a stencil with different material thicknesses) should be considered if very different sized components must be soldered on the same application PCB: while high density chip housings with small pitch need small solder paste quantities for the avoidance of short-circuits and therefore require thin stencils, large components need more solder paste for a safe connection and thus thicker stencils.

The bottom layer of LISA-U2 series modules has two unprotected copper areas for GND, shown in Figure 62.

☞ Consider “No-routing” areas for the LISA-U2 modules footprint as follows: signal keep-out area on the top layer of the application board, below LISA-U2 modules, due to GND opening on module bottom layer (see Figure 62).

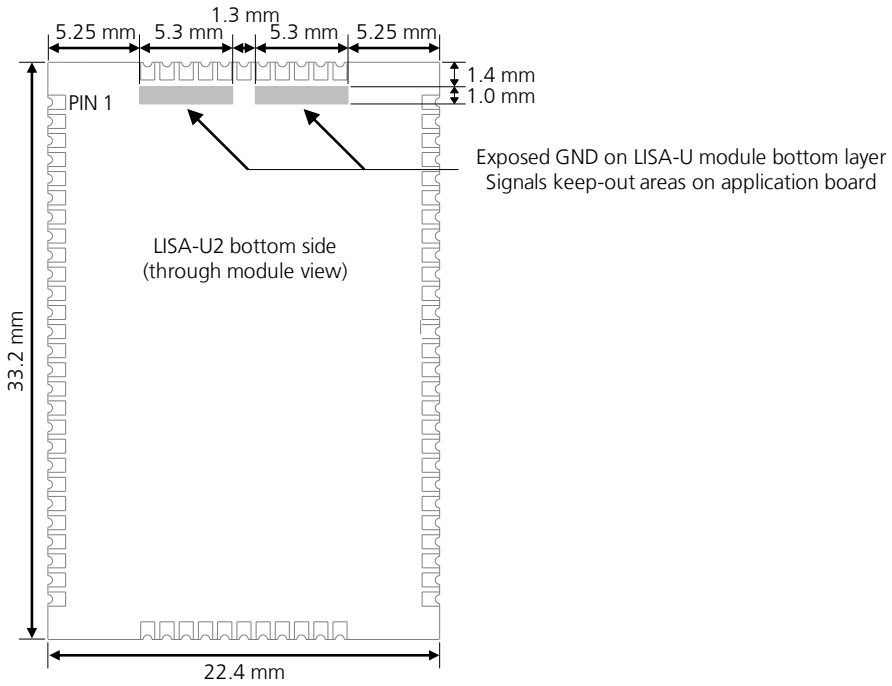


Figure 62: Signals keep-out areas on the top layer of the application board, below LISA-U2 series modules

2.2.3 Placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

Make sure that RF and analog circuits are clearly separated from any other digital circuits on the system board.

Provide enough clearance between the module and any external part due to solder and paste masks design.

Milled edges that are present at module PCB corners, away from module pins metallization, can slightly increase module dimensions from the width and the height described in the mechanical specifications sections of LISA-U2 series Data Sheet [1]: provide enough clearance between module PCB corners and any other external part mounted on the application board.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the LISA-U2 modules: avoid placing temperature sensitive devices (e.g. GNSS receiver) close to the module.

2.3 Thermal guidelines

☞ LISA-U2 module operating temperature range and module thermal resistance are specified in the LISA-U2 series Data Sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload or voice call in connected mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks; however the application should be correctly designed to cope with it.

During transmission at maximum RF power the LISA-U2 modules generate thermal power that can exceed 2 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the number of allocated TX slot and modulation (GMSK or 8PSK) or data rate (WCDMA), transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition (e.g. 2G or 3G mode, transmit band): the overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

Mounting a LISA-U2 module on a 90 mm x 70 mm x 1.46 mm 4-Layers PCB with a high coverage of copper in still air conditions[7], the increase of the module temperature[8] in different modes of operation, referred to idle state initial condition[9], can be summarized as following:

- 7°C during a GSM voice call at max TX power
- 19°C during GPRS data transfer with 4 TX slots at max TX power
- 16°C during EDGE data transfer with 4 TX slots at max TX power
- 25°C in UMTS/HSxPA connection at max TX power

☞ The Module-to-Ambient thermal resistance value and the related increase of module temperature will be different for other mechanical deployments of the module, e.g. PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of thermal dissipation, i.e. the Module-to-Ambient thermal resistance reduction, will decrease the temperature for internal circuitry of LISA-U2 modules for a given operating ambient temperature. This improves the device long-term reliability for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with complete via stack down to main ground layer
- Provide a ground plane as wide as possible on the application board
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power
- Optimize the thermal design of any high-power component included in the application, as linear regulators and amplifiers, to optimize overall temperature distribution in the application device
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure of the application device that integrates the module) so that it provides good thermal dissipation

[7] Refer to LISA-U2 series Data Sheet [1] for the $R_{th,M-A}$ value in this application condition
[8] Temperature is measured by internal sensor of wireless module
[9] Steady state thermal equilibrium is assumed. The module's temperature in idle state can be considered equal to ambient temperature

Further hardware techniques to be used to improve heat dissipation in the application:

- Force ventilation air-flow within mechanical enclosure
- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads and dissipated over the backside of the application board

For example, after the installation of a robust aluminum heat-sink with forced air ventilation on the back of the same application board described above, the Module-to-Ambient thermal resistance ($R_{th,M-A}$) is reduced to 1.5 ÷ 3.5 °C/W. The effect of lower $R_{th,M-A}$ can be seen from the module temperature increase, which now can be summarized as following:

- 1.5°C during a GSM voice call at max TX power
- 3°C during GPRS data transfer with 4 TX slots at max TX power
- 2.5°C during EDGE data transfer with 4 TX slots at max TX power
- 5.5°C in UMTS/HSxPA connection at max TX power

Beside the reduction of the Module-to-Ambient thermal resistance implemented by the hardware design of the application device integrating a LISA-U2 module, the increase of module temperature can be moderated by the software implementation of the application.

Since the most critical condition concerning module thermal power occurs when module connected mode is enabled, the actual module thermal power depends, as module current consumption, on the radio access mode (GERAN / UTRA), the operating band and the average TX power.

A few software techniques may be implemented to reduce the module temperature increase in the application:

- Select the radio access mode which provides lower temperature increase (see the module temperature increase values summarized above) by means of an AT command (see the u-blox AT Commands Manual [2], +COPS command)
- Select the operating band which provides lower current consumption in the selected radio access mode (see current consumption values reported in the LISA-U2 series Data Sheet [1]) by means of an AT command (see the u-blox AT Commands Manual [2], +UBANDSEL command)
- Enable module connected mode for a given time period and then disable it for a time period enough long to properly mitigate temperature increase

2.4 Antenna guidelines

Antenna characteristics are essential for good functionality of the module. Antenna radiating performance has direct impact on the reliability of connections over the Air Interface. A bad termination of the **ANT** pin (main RF input/output) and the **ANT_DIV** pin (RF input for diversity receiver provided by LISA-U230 modules) can result in poor performance of the module.

The following parameters should be checked:

	Item	Recommendations
	Impedance	50 Ω nominal characteristic impedance
	Frequency Range	Depends on the LISA-U2 module HW version and on the Mobile Network used. LISA-U260: 824..960 MHz (GSM 850, GSM 900, UMTS B5) 1710..1990 MHz (GSM 1800, GSM 1900, UMTS B2) LISA-U270: 824..960 MHz (GSM 850, GSM 900, UMTS B8) 1710..2170 MHz (GSM 1800, GSM 1900, UMTS B1) LISA-U200, LISA-U201, LISA-U230: 824..960 MHz (GSM 850, GSM 900, UMTS B5, UMTS B6, UMTS B8) 1710..2170 MHz (GSM 1800, GSM 1900, UMTS B1, UMTS B2, UMTS B4)
	Input Power	>2 W peak
	VSWR	<2:1 recommended, <3:1 acceptable
	Return Loss	S_{11}<-10 dB recommended, S_{11}<-6 dB acceptable

Table 46: General recommendation for GSM antenna

⚠ The antenna gain shall be limited according to regulatory agency RF radiation requirements. For example, see the maximum antenna gain value reported in section 1.15.1 for EU, in section 1.15.2.2 for US FCC, in section 1.15.3.1 for ISED Canada.

Some 2G and 3G bands are overlapping. This depends on worldwide band allocation for telephony services, where different bands are deployed for different geographical regions.

If LISA-U2 series modules are planned for use on the entire supported bands, then an antenna that supports the 824...960 MHz and the 1710...2170 MHz frequency range should be selected. Otherwise, for fixed applications in specific geographical region, antenna requirements can be relaxed for non-deployed frequency bands. See the operating RF frequency bands table in LISA-U2 series Data Sheet [1] for the detailed uplink and downlink frequency ranges of each supported band.

LISA-U230 modules provide 2G and 3G dynamic receive diversity (Rx diversity) capability to improve the quality and reliability of the cellular link. This feature can be optionally used connecting a second antenna to the **ANT_DIV** pin, to receive an RF input signal that is processed by the module to increase the performance.

☞ It is recommended to properly connect the Rx diversity antenna to the **ANT_DIV** pin of LISA-U230 modules unless the 2G and 3G Rx diversity feature is disabled by AT command (see the u-blox AT Commands Manual [2], +URXDIV command).

All the antenna guidelines and recommendations reported for the main Tx/Rx antenna design are applicable also to the Rx diversity antenna design, even if the antenna for the Rx diversity is not used to transmit.

GSM antennas are typically available as:

- Linear monopole: typical for fixed applications. The antenna extends mostly as a linear element with a dimension comparable to lambda/4 of the lowest frequency of the operating band. Magnetic base may be available. Cable or direct RF connectors are common options. The integration normally requires the fulfillment of some minimum guidelines suggested by antenna manufacturer
- Patch-like antenna: better suited for integration in compact designs (e.g. mobile phone). These are mostly custom designs where the exact definition of the PCB and product mechanical design is fundamental for tuning of antenna characteristics

For integration observe these recommendations:

- Ensure 50 Ω antenna termination, minimize the VSWR or return loss, as this will optimize the electrical performance of the module. See sections 2.2.1.1 and 2.4.1
- Select the antenna with the best radiating performance. See section 2.4.2
- If a cable is used to connect the antenna radiating element to application board, select a short cable with minimum insertion loss. The higher the additional insertion loss due to low quality or long cable, the lower the connectivity
- Follow the recommendations of the antenna manufacturer for correct installation and deployment
- Do not include antenna within closed metal case
- Do not place the main antenna in close vicinity to the end user since the emitted radiation in human tissue is limited by S.A.R. regulatory requirements
- Do not use directivity antenna since the electromagnetic field radiation intensity is limited in some countries
- Take care of interactions between co-located RF systems since the GSM transmitted power may interact or disturb the performance of companion systems
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues that may arise
- The antenna for the Rx diversity should be carefully separated from the main Tx/Rx antenna, because signal improvement is dependent on the cross correlation and the signal strength levels between the two received signals. The distance between the two antennas should be at least greater than half a wavelength of the lowest used frequency (i.e. distance greater than ~20 cm, for 2G/3G low bands) to distinguish between different multipath channels

2.4.1 Antenna termination

The LISA-U2 modules are designed to work on a 50 Ω load. However, real antennas have no perfect 50 Ω load on all the supported frequency bands. Therefore the following requirements should be met in order to reduce the performance degradation due to antenna mismatch as much as possible:

Measure the antenna termination with a network analyzer: connect the antenna through a coaxial cable to the measurement device, the $|S_{11}|$ indicates which portion of the power is delivered to the antenna and which portion is reflected by the antenna back to the module output.

A good antenna should have an $|S_{11}|$ below -10 dB over the entire frequency band. Due to miniaturization, mechanical constraints and other design issues, this value will not be achieved. An $|S_{11}|$ value of about -6 dB - (in the worst case) - is acceptable.

Figure 63 shows an example of this measurement:

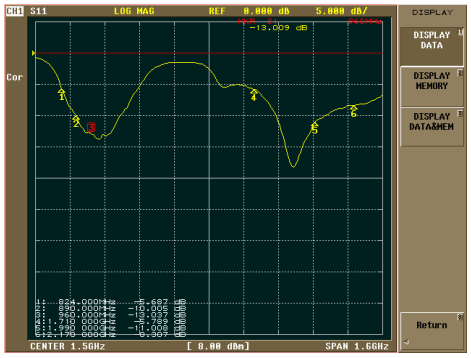


Figure 63: $|S_{11}|$ sample measurement of a penta-band antenna that covers in a small form factor the 4 GSM bands (850 MHz, 900 MHz, 1800 MHz and 1900 MHz) and the UMTS Band I

Figure 64 shows comparable measurements performed on a wideband antenna. The termination is better, but the size of the antenna is considerably larger.

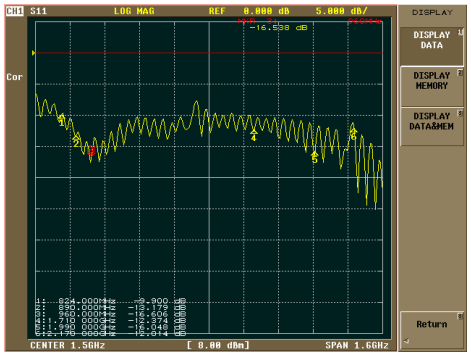


Figure 64: $|S_{11}|$ sample measurement of a wideband antenna

2.4.2 Antenna radiation

An indication of the antenna's radiated power can be approximated by measuring the $|S_{21}|$ from a target antenna to the measurement antenna, using a network analyzer with a wideband antenna. Measurements should be done at a fixed distance and orientation, and results compared to measurements performed on a known good antenna. Figure 65 through Figure 66 show some example measurement results. A wideband log periodic-like antenna was used, and the comparison was done with a half lambda dipole tuned to the 900 MHz frequency. The measurements show both the $|S_{11}|$ and $|S_{21}|$ for the penta-band internal antenna and for the wideband antenna.

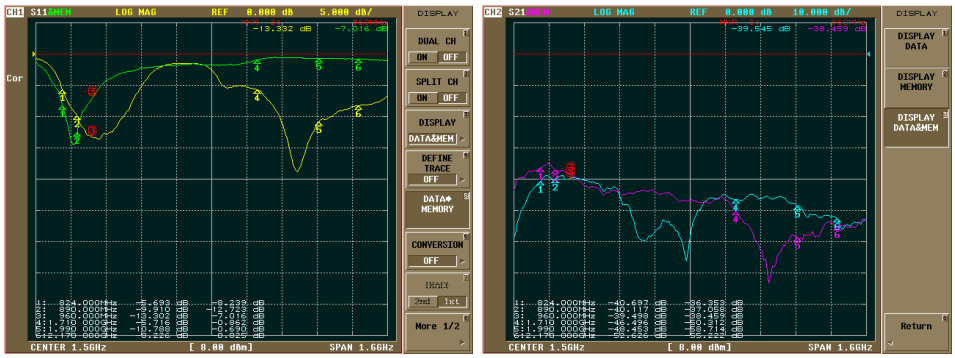


Figure 65: $|S_{11}|$ and $|S_{21}|$ comparison between a 900 MHz tuned half wavelength dipole (green/purple) and a penta-band internal antenna (yellow/cyan)

The half lambda dipole tuned at 900 MHz is known and has good radiation performance (both for gain and directivity). Then, by comparing the $|S_{21}|$ measurement with antenna under investigation for the frequency where the half dipole is tuned (e.g. marker 3 in Figure 65) it is possible to make a judgment on the antenna under test: if the performance is similar, then the target antenna is good.

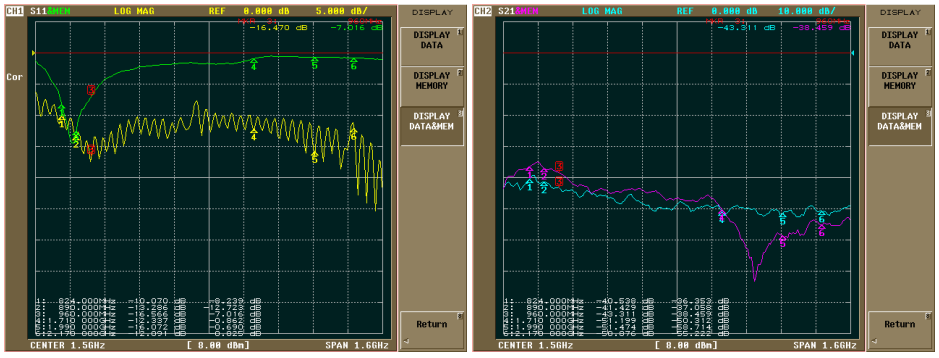


Figure 66: $|S_{11}|$ and $|S_{21}|$ comparison between a 900 MHz tuned half wavelength dipole (green/purple) and a wideband commercial antenna (yellow/cyan)

But if $|S_{21}|$ values for the tuned dipole are instead much better than the antenna under evaluation (like for marker 1/2 area of Figure 66, where dipole is 5 dB better), then it can be argued that the radiation of the target antenna (the wideband dipole in this case) is considerably less.

The same procedure should be repeated on other bands with a half wavelength dipole re-tuned to the band under investigation.

☞ For good antenna radiation performance, antenna dimensions should be comparable to a quarter of the wavelength. Different antenna types can be used for the module, many of them (e.g. patch antennas, monopole) are based on a resonating element that works in combination with a ground plane. The ground plane, ideally infinite, can be reduced down to a minimum size that must be similar to one quarter of the wavelength of the minimum frequency that needs to be radiated (transmitted/received). Numerical sample: frequency = 1 GHz → wavelength = 30 cm → minimum ground plane (or antenna size) = 7.5 cm. Below this size, the antenna efficiency is reduced.

2.4.3 Examples of antennas

Table 47 lists some examples of possible internal on-board surface-mount antennas

Manufacturer	Part Number	Product Name	Description
Taoglas	PA.25.A	Anam	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 36.0 x 6.0 x 5.0 mm
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PA.711.A	Warrior II	GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.06.A	Havok	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm
Antenova	A10340	Calvus	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 28.0 x 8.0 x 3.2 mm
Ethertronics	P522304	Prestta	GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 35.0 x 9.0 x 3.2 mm
2J	2JE04		GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 24.0 x 5.5 x 4.4 mm
Yaego	ANT3505B000TWPENA		GSM / WCDMA SMD Antenna 824..960 MHz, 1710..2170 MHz 35.0 x 5.0 x 6.0 mm

Table 47: Examples of internal surface-mount antennas

Table 48 lists some examples of possible internal off-board antennas with cable and connector.

Manufacturer	Part Number	Product Name	Description
Taoglas	FXP14.A.07.0100A		GSM / WCDMA PCB Antenna with cable and U.FL connector 824..960 MHz, 1710..2170 MHz 70.4 x 20.4 mm
Taoglas	FXP14R.A.07.0100A		GSM / WCDMA PCB Antenna with cable and U.FL connector Integrated 10k shunt diagnostic resistor 824..960 MHz, 1710..2170 MHz 80.0 x 20.8 mm
Taoglas	PC29.09.0100A	TheStripe	GSM / WCDMA PCB Antenna with cable and MMCX(M)RA connector 824..960 MHz, 1710..2170 MHz 80.4 x 29.4 mm
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Ethertronics	P522310	Prestta	GSM / WCDMA PCB Antenna with cable and U.FL connector 824..960 MHz, 1710..2170 MHz 41.0 x 15.0 mm

Manufacturer	Part Number	Product Name	Description
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm
Yaego	ANTX100P001BWPEN3		GSM / WCDMA PCB Antenna with cable and I-PEX connector 824..960 MHz, 1710..2170 MHz 50.0 x 20.0 mm

Table 48: Examples of internal antennas with cable and connector

Table 49 lists some examples of possible external antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE low-profile adhesive-mount Antenna with cable and SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm
Taoglas	GSA.8821.A.301721	I-Bar	GSM / WCDMA low-profile adhesive-mount Antenna with cable and Fakra (code-D) connector 824..960 MHz, 1710..2170 MHz 106.7 x 14.7 x 5.8 mm
Taoglas	TG.30.8112		GSM / WCDMA / LTE swivel dipole Antenna with SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm
Taoglas	OMB.8912.03F21		GSM / WCDMA pole-mount Antenna with N-type (F) connector 824..960 MHz, 1710..2170 MHz 527 x Ø 26 mm
Taoglas	FW.92.RNT.M		GSM / WCDMA whip monopole Antenna with RP-N-type(M) connector 824..960 MHz, 1710..2170 MHz 274 x Ø 20 mm
Nearson	T6150AM		GSM / WCDMA swivel monopole Antenna with SMA(M) connector 824..960 MHz, 1710..2170 MHz 179.3 x 22 x 6.5 mm
Laird Tech.	MAF94300	HEPTA-SM	GSM / WCDMA swivel monopole Antenna with SMA(M) connector 824..960 MHz, 1575.42 MHz,1710..2170 MHz, 2400..2500 MHz 161 x 9.3 mm
Laird Tech.	TRA806/171033P		GSM / WCDMA screw-mount Antenna with N-type(F) connector 824..960 MHz, 1710..2170 MHz 69.8 x Ø 38.1 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount Antenna with N-type(F) connector 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount Antenna with N-type(M) connector 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Abracon	APAMS-102		GSM / WCDMA low-profile adhesive-mount Antenna with cable and SMA(M) connector 824..960 MHz, 1710..2170 MHz 138 x 21 x 6 mm

Table 49: Examples of external antennas

2.4.4 Antenna detection functionality

The internal antenna detect circuit is based on ADC measurement at **ANT**: the RF port is DC coupled to the ADC unit in the baseband chip which injects a DC current (10 µA for 128 µs) on **ANT** and measures the resulting DC voltage to evaluate the resistance from the **ANT** pad to GND.

The antenna detection is forced by the +UANTR AT command: see the u-blox AT Commands Manual [2] for more details on how to access this feature.

To achieve antenna detection functionality, use an RF antenna with a built-in resistor from the **ANT** signal to GND, or implement an equivalent solution with a circuit between the antenna cable connection and the radiating element as shown in Figure 67.

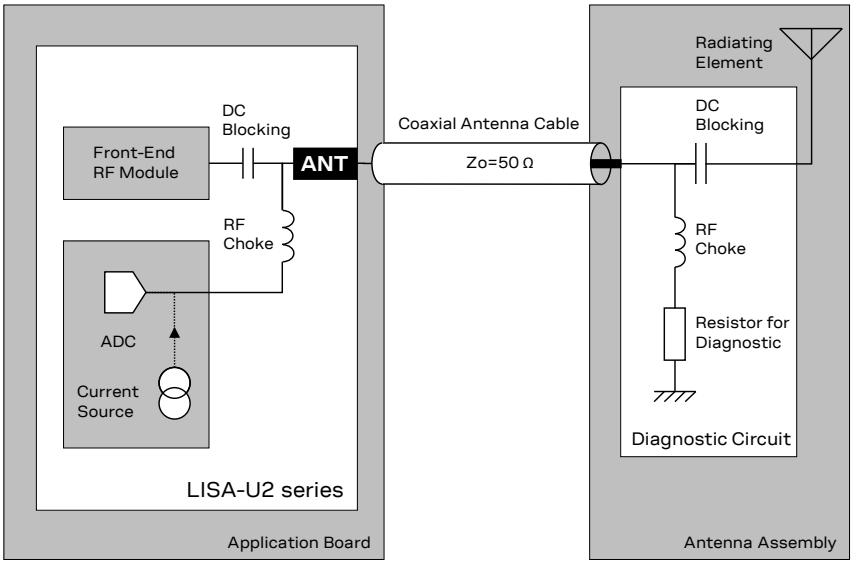


Figure 67: Antenna detection circuit and antenna with diagnostic resistor

Examples of components for the antenna detection diagnostic circuit are listed in the following table:

Description	Part Number - Manufacturer
DC Blocking Capacitor	Murata GRM1555C1H220JA01 or equivalent
RF Choke Inductor	Murata LQG15HS68NJ02, LQG15HH68NJ02 or equivalent (Self Resonance Frequency ~1GHz)
Resistor for Diagnostic	15 kΩ 5%, various Manufacturers

Table 50: Example of components for the antenna detection diagnostic circuit

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 67, the measured DC resistance will always be at the limits of the measurement range (respectively open or short), and there will be no means to distinguish between a defect on the antenna path with similar characteristics (respectively: removal of a linear antenna or RF cable shorted to GND for a PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from the ANT connector to the radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and to avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of the load resistor.

For example, consider a GSM antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the **ANT** connector to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see the u-blox AT Commands Manual [2]) means that that the antenna is not connected or the RF cable is broken
- Reported values below the measurement range minimum limit (1 kΩ) will highlight a short to GND at the antenna or along the RF cable
- Measurement inside the valid measurement range and outside the expected range may indicate an unclean connection, damaged antenna or wrong value of the antenna load resistor for diagnostic purposes
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to the antenna cable length, antenna cable capacity and the used measurement method

2.5 ESD guidelines

2.5.1 ESD immunity test overview

The immunity of devices integrating LISA-U2 modules to Electrostatic Discharge (ESD) is part of the Electromagnetic Compatibility (EMC) conformity which is required for products bearing the CE marking, compliant with the Radio Equipment Directive (2014/53/EU), the EMC Directive (2014/30/EU) and the Low Voltage Directive (2014/35/EU) issued by the Commission of the European Community.

Compliance with these directives implies conformity with the following European Norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 [11] and the radio equipment standards EN 301 489-1 [12], EN 301 489-52 [13], the requirements of which are summarized in Table 51.

The ESD immunity test is performed at the enclosure port, defined by EN 301 489-1 [12] as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is defined as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of the ESD immunity test to the whole device depends on the device classification as defined by ETSI EN 301 489-1 [12]. Applicability of the ESD immunity test to the specific device ports or the specific interconnecting cables to auxiliary devices depends on the devices' accessible interfaces and manufacturer requirements, as defined by ETSI EN 301 489-1 [12].

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in CENELEC EN 61000-4-2 [11].

☞ For the definition of integral antenna, removable antenna, antenna port, device classification see the ETSI EN 301 489-1 [12].

☞ The contact and air discharges are defined in CENELEC EN 61000-4-2 [11].

Application	Category	Immunity Level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Contact Discharge	4 kV
	Air Discharge	8 kV

Table 51: ESD immunity requirements as defined by EN 61000-4-2, EN 301 489-1, EN 301 489-52

2.5.2 ESD immunity test of u-blox LISA-U2 series reference designs

Although Electromagnetic Compatibility (EMC) certification is required for customized devices integrating
LISA-U2 modules for RED and European Conformance CE mark, EMC certification (including ESD immunity) has been successfully performed on the LISA-U2 series modules reference designs according to the CENELEC EN 61000-4-2 [11], ETSI EN 301 489-1 [12], ETSI EN 301 489-52 [13] European Norms.

The EMC / ESD approved u-blox reference designs consist of a LISA-U2 series module soldered onto a motherboard which provides the supply interface, SIM card, headset, and communication port. An external antenna is connected to an SMA connector provided on the motherboard for the main Tx/Rx antenna. An additional external antenna is connected to an additional SMA connector provided on the motherboard for the Rx diversity antenna of the LISA-U230 modules.

Since an external antenna is used, the antenna port can be separated from the enclosure port. The reference design is not enclosed in a box so that the enclosure port is not identified with physical surfaces. Therefore, some test cases cannot be applied. Only the antenna port is identified as accessible for direct ESD exposure.

☞ The u-blox LISA-U2 series reference designs implement all the ESD precautions described in section 2.5.3.

u-blox LISA-U2 series reference designs ESD immunity test results are detailed in Table 52, according to test requirements stated in CENELEC EN 61000-4-2 [11], EN 301 489-1 [12], EN 301 489-52 [13].

Category	Application	Ref. Design	Immunity Level	Remarks
Contact Discharge to coupling planes (indirect contact discharge)	Enclosure	All	+4 kV / -4 kV	
Contact Discharges to conducted surfaces (direct contact discharge)	Enclosure port	All	Not Applicable	Test not applicable to u-blox reference design because it does not provide enclosure surface. The test is applicable only to equipments providing conductive enclosure surface.
	Main Antenna port	All	+4 kV / -4 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with conductive surface.
	Rx Div Antenna port	LISA-U230	+4 kV / -4 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with conductive surface.
Air Discharge at insulating surfaces	Enclosure port	All	Not Applicable	Test not applicable to the u-blox reference design because it does not provide an enclosure surface. The test is applicable only to equipments providing insulating enclosure surface.
	Main Antenna port	All	+8 kV / -8 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with insulating surface.
	Rx Div Antenna port	LISA-U230	+8 kV / -8 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with insulating surface.

Table 52: Enclosure ESD immunity level of u-blox LISA-U2 series modules reference designs

2.5.3 ESD application circuits

The application circuits described in this section are recommended and should be implemented in any device that integrates a LISA-U2 module, according to the application board classification (see ETSI EN 301 489-1 [12]), to satisfy the requirements for the ESD immunity test summarized in Table 51.

2.5.3.1 Antenna interface

The **ANT** pin of LISA-U2 modules provides ESD immunity up to 1000 V (contact and air discharge according to IEC 61000-4-2): a higher protection level is required if the line is externally accessible on the device (i.e. the application board where the LISA-U2 series module is mounted).

The following precautions are suggested for satisfying ESD immunity test requirements:

- If the device implements an embedded antenna, the device insulating enclosure should provide protection to direct contact discharge up to ±4 kV and protection to air discharge up to ±8 kV to the antenna interface
- If the device implements an external antenna, the antenna and its connecting cable should provide a completely insulated enclosure able to provide protection to direct contact discharge up to ±4 kV and protection to air discharge up to ±8 kV to the whole antenna and cable surfaces
- If the device implements an external antenna and the antenna and its connecting cable do not provide a completely insulated enclosure able to provide protection to direct contact discharge up to ±4 kV and protection to air discharge up to ±8 kV to the whole antenna and cable surfaces, an external high pass filter, consisting of a series 15 pF capacitor (Murata GRM1555C1H150JA01) and a shunt 39 nH coil (Murata LQG15HN39NJ02) should be implemented at the antenna port as described in Figure 68, as implemented in the EMC / ESD approved reference design of LISA-U2 series modules

☞ Antenna detection functionality is not provided when implementing the high pass filter described in Figure 68 and Table 53 as the ESD protection for the antenna port of LISA-U2 series modules.

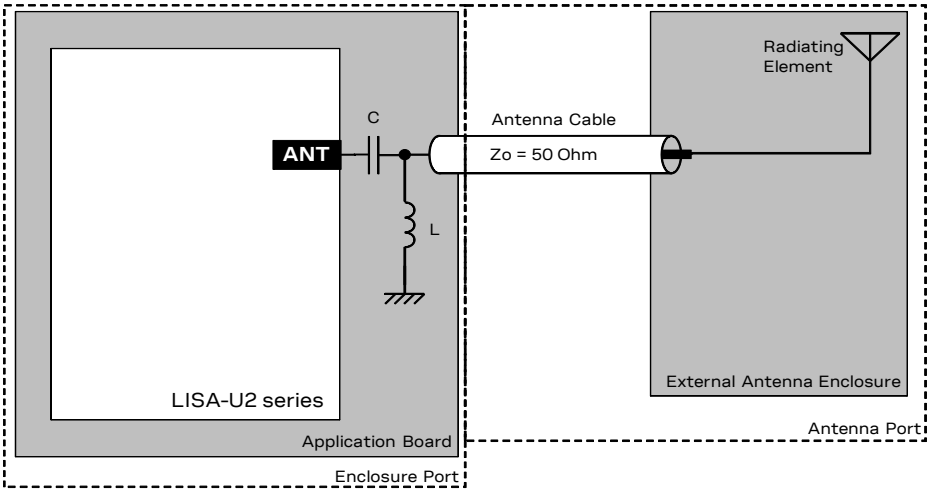


Figure 68: Antenna port ESD immunity protection application circuit for LISA-U2 series modules

Reference	Description	Part Number - Manufacturer
C	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
L	39 nH Multilayer Chip Inductor L0G 0402 5%	LQG15HN39NJ02 - Murata

Table 53: Example of parts for the antenna port ESD immunity protection application circuit for LISA-U2 series modules

With LISA-U230 modules, the **ANT_DIV** pin provides ESD immunity up to ±4 kV for direct Contact Discharge and up to ±8 kV for Air Discharge: no further precaution to ESD immunity test is needed, as implemented in the EMC / ESD approved reference design of LISA-U230 modules.

2.5.3.2 RESET_N pin

The following precautions are suggested for the **RESET_N** line of LISA-U2 modules, depending on the application board handling, to satisfy the ESD immunity test requirements:

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JA01) must be mounted on the line termination connected to the **RESET_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- A proper series chip ferrite bead noise/EMI suppression filter (e.g. Murata BLM15HD182SN1) must be added on the line connected to the **RESET_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- A 220 nF bypass capacitor (e.g. Murata GRM155R60J224KE01) must be mounted as close as possible to the **RESET_N** pin of LISA-U2 series modules to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- It is recommended to keep the connection line to **RESET_N** as short as possible

The maximum ESD sensitivity rating of the **RESET_N** pin is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the **RESET_N** pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection levels:

- A general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the **RESET_N** line, close to the accessible point

The **RESET_N** application circuit implemented in the EMC / ESD approved reference designs of the LISA-U2 series modules is described in Figure 20 and Table 19 (section 1.6.3).

2.5.3.3 SIM interface

The following precautions are suggested for the LISA-U2 module's SIM interface (**VSIM**, **SIM_RST**, **SIM_IO**, **SIM_CLK** pins), depending on the application board handling, to satisfy the ESD immunity test requirements:

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470J) must be mounted on the lines connected to **VSIM**, **SIM_RST**, **SIM_IO** and **SIM_CLK** pins to assure SIM interface functionality when an electrostatic discharge is applied to the application board enclosure
- It is suggested to use as short as possible connection lines at the SIM pins

The maximum ESD sensitivity rating of SIM interface pins is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if SIM interface pins are externally accessible on the application board. The following precautions are suggested to achieve higher protection levels:

- A low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Infineon ESD8V0L2B-03L or AVX USB0002) should be mounted on each SIM interface line, close to the accessible points (i.e. close to the SIM card holder)

The SIM interface application circuit implemented in the EMC / ESD approved reference designs of LISA-U2 series modules versions is described in section 1.8.1.

2.5.3.4 Other pins and interfaces

All the module pins that are externally accessible on the device integrating the LISA-U2 module should be included in the ESD immunity test since they are considered to be a port as defined in ETSI EN 301 489-1 [12]. Depending on applicability, to satisfy the ESD immunity test requirements according to

ESD category level, all the module pins that are externally accessible should be protected up to ±4 kV for direct Contact Discharge and up to ±8 kV for Air Discharge applied to the enclosure surface.

The maximum ESD sensitivity rating of all the other pins of the module is 1 kV (Human Body Model according to JESD22-A114F). Higher protection levels could be required if the relevant pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection levels:

- **USB interface**: a very low capacitance (i.e. less or equal to 1 pF) ESD protection device (e.g. Tyco Electronics PESD0402-140 ESD protection device) should be mounted on the **USB_D+** and **USB_D-** lines, close to the accessible points (i.e. close to the USB connector)
- **SPI interface**: a low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Infineon ESD8V0L2B-03L or AVX USB0002) should be mounted on the **SPI_MISO**, **SPI_MOSI**, **SPI_SCLK**, **SPI_MRDY**, **SPI_SRDY** lines, close to the accessible points
- **CODEC_CLK**: a low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Infineon ESD8V0L2B-03L or AVX USB0001) should be mounted on the **CODEC_CLK** line, close to the accessible point
- **Other pins**: a general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the related line, close to the accessible point

3 Features description

3.1 Network indication

Alternatively from their default settings, the **GPIO1**, **GPIO2**, **GPIO3**, **GPIO4** or **GPIO5** can be configured to indicate the network status (i.e. no service, registered home network, registered visitor network, voice or data call enabled), by means of the AT+UGPIOC command.

For a detailed description, see section 1.12 and to u-blox AT Commands Manual [2], GPIO commands.

3.2 Antenna detection

Antenna presence detection capability is provided, evaluating the resistance from the **ANT** pin to GND by means of an internal antenna detection circuit. The external antenna assembly must be provided with a built-in resistor (diagnostic circuit) to be detected.

The antenna detection feature can be enabled through the +UANTR AT command.

For more details regarding feature description and diagnostic circuit design-in, see section 2.4.4 and the u-blox AT Commands Manual [2].

3.3 Jamming Detection

In real network situations, modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operator choices, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carriers that are entitled to give access to the GSM/UMTS service.

The Jamming Detection Feature detects such "artificial" interference and reports the start and stop of such conditions to the client, which can react appropriately by e.g. switching off the radio transceiver in order to reduce power consumption and monitoring the environment at constant periods.

The feature consists of detecting, at the radio resource level, an anomalous source of interference and signaling it to the client with an unsolicited indication when the detection is entered or released. The jamming condition occurs when:

- The module has lost synchronization with the serving cell and cannot select any other cell
- The band scan reveals at least n carriers with a power level equal or higher than the threshold
- On all such carriers, no synchronization is possible

The number of minimum disturbing carriers and the power level threshold can be configured by the client by using the AT+UCD command [2].

The jamming condition is cleared when any of the above mentioned statements does not hold.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command (for more details, see the u-blox AT Commands Manual [2]).

3.4 TCP/IP and UDP/IP

Via the AT commands, it is possible to access the TCP/IP and UDP/IP functionalities over the Packet Switched data connection. For more details about AT commands, see the u-blox AT Commands Manual [2].

LISA-U2 modules support the Direct Link mode for TCP and UDP sockets. Sockets can be set in Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via the serial interface. In Direct Link mode, data sent to the serial interface from an external application processor is forwarded to the network and vice-versa.

To avoid data loss while using Direct Link, enable HW flow control on the serial interface.

3.4.1 Multiple PDP contexts and sockets

Two PDP context types are defined:

- "external" PDP context: IP packets are built by the DTE, the MT's IP instance only runs the IP relay function
- "internal" PDP context: the PDP context (relying on the MT's TCP/IP stack) is configured, established and handled via the data connection management packet switched data commands described in u-blox AT commands manual [2]

Multiple PDP contexts are supported. The DTE can access these PDP contexts either alternatively through the physical serial port, or simultaneously through the virtual serial ports of the multiplexer (multiplexing mode MUX), with the following constraints:

- Using the MT's embedded TCP/IP stack, only 1 internal PDP context is supported. This IP instance supports up to 7 sockets
- Using only external PDP contexts, it is possible to have at most 3 IP instances (with 3 different IP addresses) simultaneously. If in addition the internal PDP context is used, at most 2 external PDP contexts can be activated

Secondary PDP contexts (PDP contexts sharing the IP address of a primary PDP context) are also supported. Traffic Flow Filters for such secondary contexts shall be specified according to 3GPP TS 23.060 [18].

At most 2 secondary PDP contexts can be activated, since the maximum number of PDP contexts, both normal and secondary, is always 3.

3.5 FTP

LISA-U2 modules support the File Transfer Protocol and Secure File Transfer Protocol functionalities via AT commands. Files are read and stored in the local file system of the module. For more details about AT commands, see the u-blox AT Commands Manual [2].

FTP files can also be transferred using the FTP Direct Link:

- **FTP download**: the data coming from the FTP server is forwarded to the application processor via the serial interface (for FTP without Direct Link mode, the data is always stored in the module's FFS)
- **FTP upload**: the data coming from the application processor via the serial interface is forwarded to the FTP server (for FTP without Direct Link mode, the data is read from the module's FFS)

When Direct Link is used for a FTP file transfer, only the file content pass through the serial interface, whereas all the FTP commands handling is managed internally by the FTP application.

Due to the limited size of the FFS module, FTP direct link is useful to transfer files with a size greater than the FFS.

To avoid data loss while using direct link, enable HW flow control on the serial interface.

3.6 HTTP

LISA-U2 modules support Hypertext Transfer Protocol (HTTP/1.0) functionalities as an HTTP client is implemented: HEAD, GET, POST, DELETE and PUT operations are available. The file size to be uploaded / downloaded depends on the free space available in the local file system (FFS) at the moment of the operation. Up to 4 HTTP client contexts can be used simultaneously.

LISA-U2 modules also support Secure Hypertext Transfer Protocol functionalities providing SSL encryption.

For more details about AT commands, see the u-blox AT Commands Manual [2].

3.7 SSL/TLS

The modules support the Secure Sockets Layer (SSL) / Transport Layer Security (TLS) with certificate key sizes up to 4096 bits to provide security over the FTP and HTTP protocols.

The SSL/TLS support provides various connection security aspects:

- Server authentication[10]: use of the server certificate verification against a specific trusted certificate or a trusted certificates list
- Client authentication[10]: use of the client certificate and the corresponding private key
- Data security and integrity: data encryption and Hash Message Authentication Code (HMAC) generation

The security aspects used during a connection depend on the SSL/TLS configuration and features supported. Table 55 contains the settings of the default SSL/TLS profile and Table 55 to Table 59 detail the main SSL/TLS supported capabilities of the products. For a complete list of supported configurations and settings, see the u-blox AT Commands Manual [2].

Settings	Value	Meaning
Certificates validation level	Level 0	The server certificate will not be checked or verified
Minimum SSL/TLS version	Any	The server can use any of the TLS1.0/TLS1.1/TLS1.2 versions for the connection
Cipher suite	Automatic	The cipher suite will be negotiated in the handshake process
Trusted root certificate internal name	None	No certificate will be used for the server authentication
Expected server host-name	None	No server host-name is expected
Client certificate internal name	None	No client certificate will be used
Client private key internal name	None	No client private key will be used
Client private key password	None	No client private key password will be used
Pre-shared key	None	No pre-shared key password will be used

Table 54: Default SSL/TLS profile

SSL/TLS Version	Supported feature
SSL 2.0	NO
SSL 3.0	YES
TLS 1.0	YES
TLS 1.1	YES[10]
TLS 1.2	YES[10]

Table 55: SSL/TLS version support

[10] Not supported by the "01", "x2" and "68" product versions

Algorithm	Supported feature
RSA	YES[10]
PSK	YES

Table 56: Authentication

Algorithm	Supported feature
RC4	NO[11]
DES	YES
3DES	YES[10]
AES128	YES
AES256	YES[10]

Table 57: Encryption

Algorithm	Supported feature
MD5	NO[11]
SHA/SHA1	YES
SHA256	YES[10]
SHA384	YES[10]

Table 58: Message digest

Description	Registry value	Supported feature
TLS_RSA_WITH_AES_128_CBC_SHA	0x00,0x2F	YES[10]
TLS_RSA_WITH_AES_128_CBC_SHA256	0x00,0x3C	YES[10]
TLS_RSA_WITH_AES_256_CBC_SHA	0x00,0x35	YES[10]
TLS_RSA_WITH_AES_256_CBC_SHA256	0x00,0x3D	YES[10]
TLS_RSA_WITH_3DES_EDE_CBC_SHA	0x00,0x0A	YES[10]
TLS_RSA_WITH_RC4_128_MD5	0x00,0x04	NO[11]
TLS_RSA_WITH_RC4_128_SHA	0x00,0x05	NO[11]
TLS_PSK_WITH_AES_128_CBC_SHA	0x00,0x8C	YES[10]
TLS_PSK_WITH_AES_256_CBC_SHA	0x00,0x8D	YES[10]
TLS_PSK_WITH_3DES_EDE_CBC_SHA	0x00,0x8B	YES[10]
TLS_RSA_PSK_WITH_AES_128_CBC_SHA	0x00,0x94	YES[10]
TLS_RSA_PSK_WITH_AES_256_CBC_SHA	0x00,0x95	YES[10]
TLS_RSA_PSK_WITH_3DES_EDE_CBC_SHA	0x00,0x93	YES[10]
TLS_PSK_WITH_AES_128_CBC_SHA256	0x00,0xAE	YES[10]
TLS_PSK_WITH_AES_256_CBC_SHA384	0x00,0xAF	YES[10]
TLS_RSA_PSK_WITH_AES_128_CBC_SHA256	0x00,0xB6	YES[10]
TLS_RSA_PSK_WITH_AES_256_CBC_SHA384	0x00,0xB7	YES[10]

Table 59: TLS cipher suite registry

[11] Supported only by "01", "x2" and "68" product versions

3.8 Dual stack IPv4/IPv6

☞ Not supported by the "01", "x2", "63" and "68" product versions.

LISA-U2 modules support both Internet Protocol version 4 and Internet Protocol version 6.

For more details about dual stack IPv4/IPv6, see the u-blox AT Commands Manual [2].

3.9 AssistNow clients and GNSS integration

For customers using u-blox GNSS receivers, the LISA-U2 cellular modules feature embedded AssistNow clients. AssistNow A-GPS provides better GNSS performance and a faster Time-To-First-Fix. The clients can be enabled and disabled with an AT command (see the u-blox AT Commands Manual [2]).

LISA-U2 modules act as a stand-alone AssistNow client, making AssistNow available with no additional requirements for resources or software integration on an external host micro controller. Full access to u-blox GNSS receivers is available via the LISA-U2 series, through a dedicated DDC (I^2C) interface, while the available GPIOs can handle the positioning chipset / module power-on/off. This means that GSM/WCDMA and GNSS can be controlled through a single serial port from any host processor.

3.10 Hybrid positioning and CellLocate®

Although GNSS is a widespread technology, its reliance on the visibility of extremely weak GNSS satellite signals means that positioning is not always possible. Especially difficult environments for GNSS are indoors, in enclosed or underground parking garages, as well as in urban canyons where GNSS signals are blocked or jammed by multipath interference. The situation can be improved by augmenting GNSS receiver data with cellular network information to provide positioning information even when GNSS reception is degraded or absent. This additional information can benefit numerous applications.

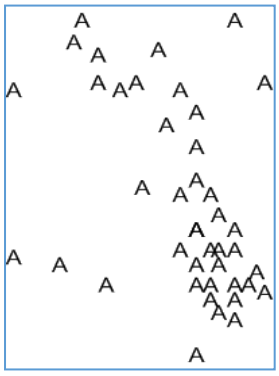
3.10.1 Positioning through cellular information: CellLocate®

u-blox CellLocate® enables the estimation of device position based on the parameters of the mobile network cells visible to the specific device. To estimate its position, the u-blox cellular module sends the CellLocate® server the parameters of network cells visible to it using a UDP connection. In return, the server provides the estimated position based on the CellLocate® database. The u-blox cellular module can either send the parameters of the visible home network cells only (normal scan), or the parameters of all surrounding cells of all mobile operators (deep scan).

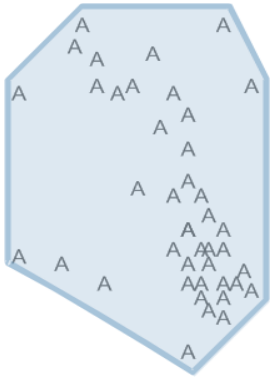
☞ Normal scan is only possible in 2G mode.

The CellLocate® database is compiled from the position of devices which observed, in the past, a specific cell or set of cells (historical observations) as follows:

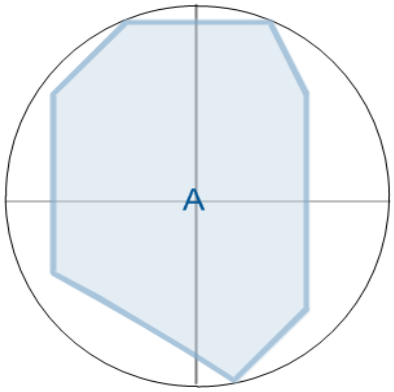
1. Several devices reported their position to the CellLocate® server when observing a specific cell (the As in the picture represent the position of the devices which observed the same cell A)



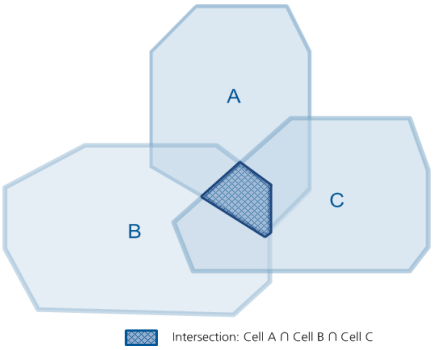
2. The CellLocate® server defines the area of Cell A visibility



3. If a new device reports the observation of Cell A, CellLocate® is able to provide the estimated position from the area of visibility



4. The visibility of multiple cells provides increased accuracy based on the intersection of areas of visibility.



CellLocate® is implemented using a set of two AT commands that allow configuration of the CellLocate® service (AT+ULOCCELL) and requesting position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy.

☞ The accuracy of the position estimated by CellLocate® depends on the availability of historical observations in the specific area.

3.10.2 Hybrid positioning

With u-blox Hybrid positioning technology, u-blox cellular devices can be triggered to provide their current position using either a u-blox GNSS receiver or the position estimated from CellLocate®. The choice depends on which positioning method provides the best and fastest solution according to the user configuration, exploiting the benefit of having multiple and complementary positioning methods.

Hybrid positioning is implemented through a set of three AT commands that allow configuration of the GNSS receiver (AT+ULOCGNSS), configuration of the CellLocate® service (AT+ULOCCELL), and requesting the position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy (if the position has been estimated by CellLocate®), and additional parameters if the position has been computed by the GNSS receiver.

The configuration of mobile network cells does not remain static (e.g. new cells are continuously added or existing cells are reconfigured by the network operators). For this reason, when a Hybrid positioning method has been triggered and the GNSS receiver calculates the position, a database self-learning mechanism has been implemented so that these positions are sent to the server to update the database and maintain its accuracy.

The use of hybrid positioning requires a connection via the DDC (I^2C) bus between the LISA-U2 cellular module and the u-blox GNSS receiver (see section 1.10).

See the GNSS Implementation Application Note [15] for the complete description of the feature.

☞ u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate® server u-blox is unable to track the SIM used or the specific device.

3.11 Control Plane Aiding / Location Services (LCS)

☞ Not supported by the "01", "x2", "63" and "68" product versions

With the Assisted GPS feature, a location server provides the module with the GPS system information that otherwise needs to be downloaded from satellites. The feature allows faster position fixes, increases sensitivity and reduces module power consumption. The feature is invoked by the module through LCS Supplementary Services or by the Network during emergency calls.

The assisted GPS Location Services feature is based on the Radio Resources Location Protocol (RRLP), according to 3GPP TS 44.031 [26], and Radio Resource Control (RRC) according to 3GPP TS 25.331 [27].

For more details, see the u-blox AT Commands Manual [2].

3.12 Firmware update Over AT (FOAT)

3.12.1 Overview

This feature allows upgrading the module firmware over the UART, USB and SPI interfaces, using AT Commands.

- The AT Command AT+UFWUPD triggers a reboot followed by the upgrade procedure at a specified baud rate
- The Xmodem-1k protocol is used for downloading the new FW image via a terminal application
- A special boot loader in the module performs FW installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up and restarts the firmware download from the Xmodem-1k handshake. After completing the upgrade, the module is reset again and wakes up in normal boot mode

3.12.2 FOAT procedure

The application processor must proceed in the following way:

- Send the AT+UFWUPD command through the UART or over the USB interface, specifying the file type and the desired baud rate
- Reconfigure the serial communication at the selected baud rate, without flow control with the Xmodem-1k protocol
- Send the new FW image via Xmodem-1k

For more details about Firmware update Over AT procedure, see the u-blox AT Commands Manual [2] and the Firmware Update Application Note [16].

3.13 Firmware update Over the Air (FOTA)

☞ Firmware update Over the Air (FOTA) is supported only by the “8x” product versions.

This feature allows upgrading the module firmware over the 3G / 2G air interface. The firmware installation procedure triggers the firmware update installation via AT command, starting from an update file stored in the module’s file system. In order to reduce the amount of data to be transmitted over the air, the implemented FOTA feature requires downloading only a “delta file” instead of the full firmware. The delta file contains only the differences between the two firmware versions (old and new). For more details about the Firmware update Over the Air procedure, see the Firmware Update Application Note [16] and the u-blox AT Commands Manual [2], +UFWINSTALL AT command.

3.14 In-Band modem (eCall / ERA-GLONASS)

☞ Not supported by supported by the "01", "x2", "63" and "68" product versions.

LISA-U2 module supports an In-Band modem solution for eCall and ERA-GLONASS emergency call applications over cellular networks, implemented according to the 3GPP TS 26.267 [23], BS EN 16062:2011 [24] and ETSI TS 122 101 [25] specifications.

eCall (European) and ERA-GLONASS (Russian) are two initiatives to combine mobile communications and satellite positioning to provide rapid assistance to motorists in the event of a collision, implementing automated emergency response system, based respectively on the corresponding GPS and GLONASS positioning systems.

When activated, the in-vehicle systems (IVS) automatically initiate an emergency call carrying both voice and data (including location data) directly to the nearest Public Safety Answering Point (PSAP) to determine whether rescue services should be dispatched to the known position.

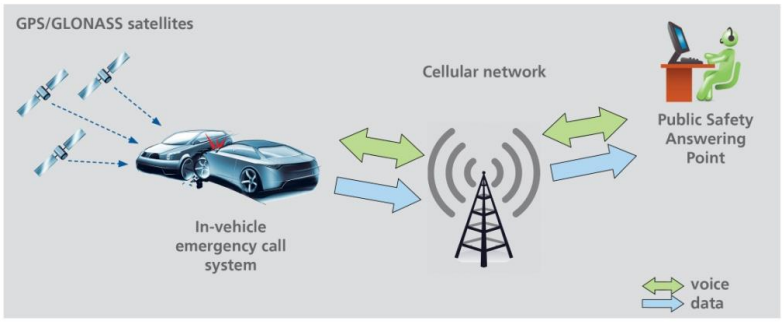


Figure 69: eCall and ERA-GLONASS automated emergency response systems diagram flow

3.15 SIM Access Profile (SAP)

SIM access profile (SAP) feature allows LISA-U2 modules to access and use a remote (U)SIM card instead of the local SIM card directly connected to the module (U)SIM interface.

LISA-U2 modules provide a dedicated USB SAP channel and dedicated multiplexer SAP channel over UART and SPI for communication with the remote (U)SIM card.

The communication between LISA-U2 modules and the remote SIM is conformed to the client-server paradigm: LISA-U2 module is the SAP client establishing a connection and performing data exchange to an SAP server directly connected to the remote SIM that is used by the LISA-U2 module for GSM/UMTS network operations. The SAP communication protocol is based on the SIM Access Profile Interoperability Specification [21].

☞ LISA-U2 modules do not support the SAP server role: the module acts only as an SAP client.

A typical application using the SAP feature is the scenario where a device such as an embedded car-phone with an integrated LISA-U2 module uses a remote SIM included in an external user device (e.g. a simple SIM card reader or a portable phone), which is brought into the car. The car-phone accesses the GSM/UMTS network using the remote SIM in the external device.

LISA-U2 modules, acting as an SAP client, can be connected to an SAP server by a completely wired connection, as shown in Figure 70.

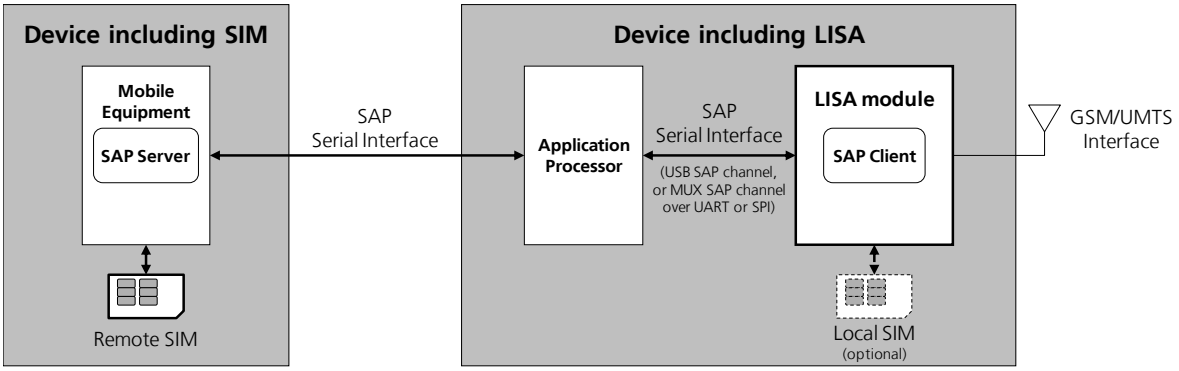


Figure 70: Remote SIM access via completely wired connection

As stated in the SIM Access Profile Interoperability Specification [21], the SAP client can be connected to the SAP server by means of a Bluetooth cellular link, using additional Bluetooth transceivers. In this case, the application processor wired to the LISA-U2 modules establishes and controls the Bluetooth connection using the SAP profile, and routes data received over a serial interface channel to data transferred over a Bluetooth interface and vice versa, as shown in Figure 71.

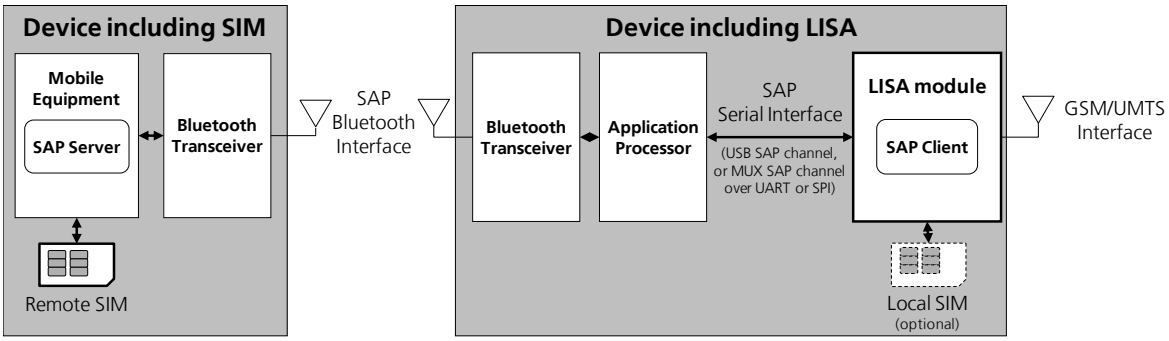


Figure 71: Remote SIM access via Bluetooth and wired connections

The application processor can start an SAP connection negotiation between the LISA-U2 module SAP client and an SAP server using a custom AT command (for more details, see the u-blox AT Commands Manual [2]).

While the connection with the SAP server is not fully established, the LISA-U2 module continues to operate with the attached (local) SIM, if present. Once the connection is established and negotiated, the LISA-U2 module performs a detach operation from the local SIM followed by an attach operation to the remote one. Then the remotely attached SIM is used for any GSM/UMTS network operation.

URC indications are provided to inform the user about the state of both the local and remote SIM. The insertion and the removal of the local SIM card are notified if a proper card presence detection circuit using the **GPIO5** of LISA-U2 modules is implemented as shown in the section 1.8.1, and if the related "SIM card detection" and "SIM hot insertion/removal" functions are enabled by AT commands (for more details, see the u-blox AT Commands Manual [2], +UGPIOC, +UDCONF=50 AT commands).

Upon SAP deactivation, the LISA-U2 modules perform a detach operation from the remote SIM followed by an attach operation to the local one, if present.

3.16 Smart Temperature Management

Cellular modules – independent of the specific model – always have a well-defined operating temperature range. This range should be respected to guarantee full device functionality and long life span.

Nevertheless there are environmental conditions that can affect the operating temperature, e.g. if the device is located near a heating/cooling source, if there is/isn't air circulating, etc.

The module itself can also influence the environmental conditions; such as when it is transmitting at full power. In this case, its temperature increases very quickly and can raise the temperature nearby.

The best solution is always to properly design the system where the module is integrated. Nevertheless, an extra check/security mechanism embedded into the module is a good solution to prevent operation of the device outside of the specified range.

3.16.1 Smart Temperature Supervisor (STS)

The Smart Temperature Supervisor is activated and configured by a dedicated AT+USTS command. See the u-blox AT Commands Manual [2] for more details.

The cellular module measures the internal temperature (Ti) and its value is compared with predefined thresholds to identify the actual working temperature range.

☞ Temperature measurement is done inside the cellular module: the measured value could be different from the environmental temperature (Ta).

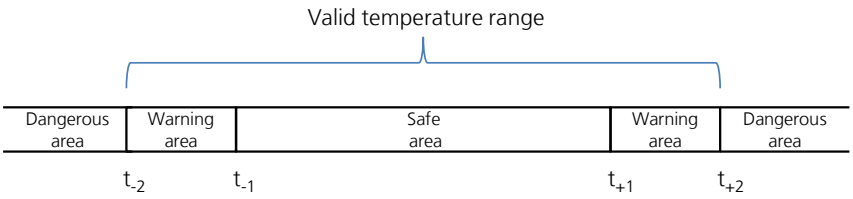


Figure 72: Temperature range and limits

The entire temperature range is divided into sub-regions by limits (see Figure 72) named t_{-2}, t_{-1}, t_{+1} and t_{+2}.

- Within the first limit, (t_{-1} < Ti < t_{+1}), the cellular module is in the normal working range, the Safe Area.
- In the Warning Area, (t_{-2} < Ti < t_{-1}) or (t_{+1} < Ti < t_{+2}), the cellular module is still inside the valid temperature range, but the measured temperature approaches the limit (upper or lower). The module sends a warning to the user (through the active AT communication interface), which can take, if possible, the necessary actions to return to a safer temperature range or simply ignore the indication. The module is still in a valid and good working condition.
- Outside the valid temperature range, (Ti < t_{-2}) or (Ti > t_{+2}), the device is working outside the specified range and represents a dangerous working condition. This condition is indicated and the device shuts down to avoid damage.

☞ For security reasons, the shutdown is suspended in case an emergency call in progress. In this case, the device will switch off at call termination.

☞ The user can decide at any time to enable/disable the Smart Temperature Supervisor feature. If the feature is disabled, there is no embedded protection against disallowed temperature conditions.

Figure 73 shows the flow diagram implemented for the Smart Temperature Supervisor.

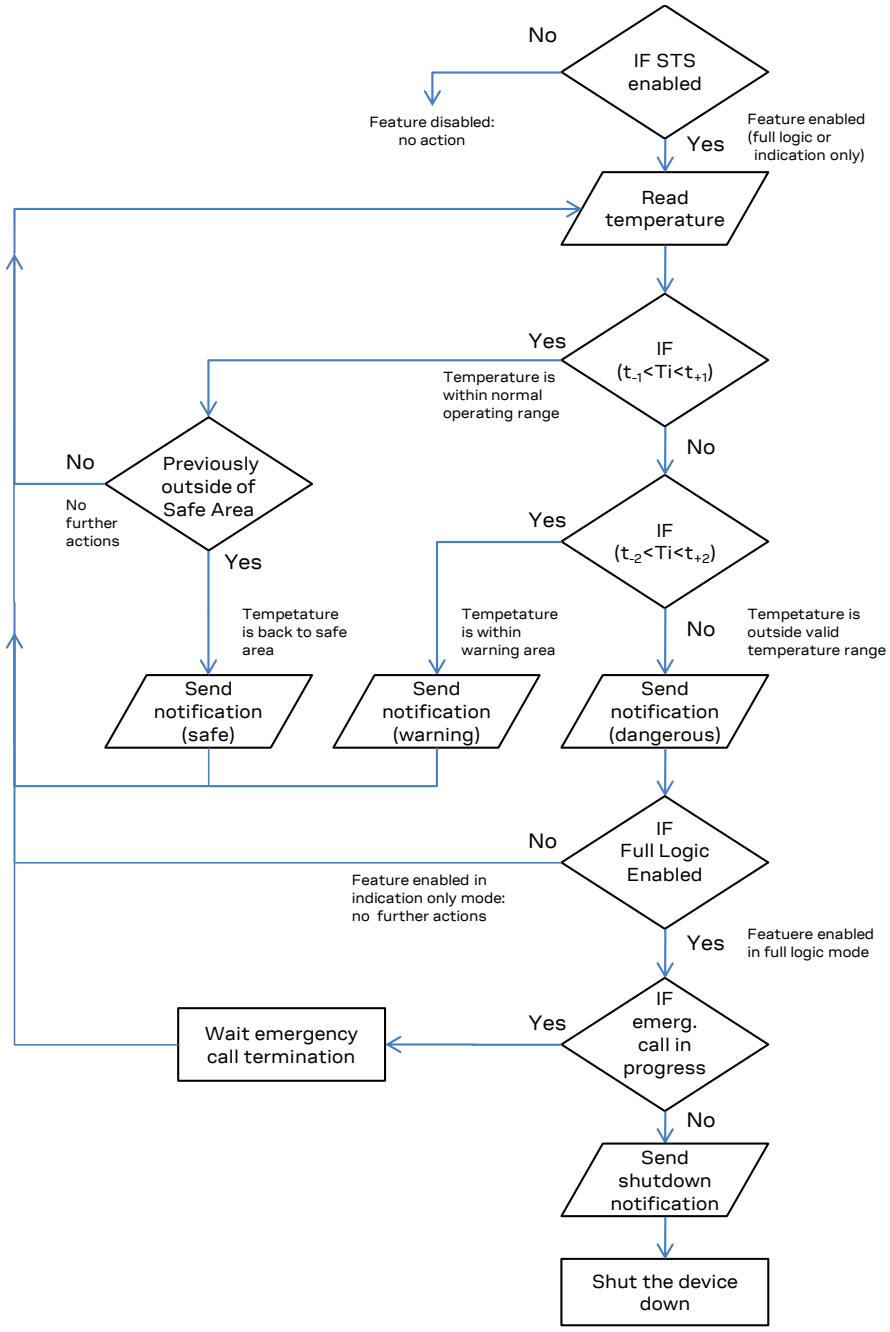


Figure 73: Smart Temperature Supervisor (STS) flow diagram

3.16.2 Threshold definitions

When the application of cellular module operates at extreme temperatures with Smart Temperature Supervisor enabled, the user should note that outside the valid temperature range the device will automatically shut down as described above.

The input for the algorithm is always the temperature measured within the cellular module (Ti, internal). This value can be higher than the working ambient temperature (Ta, ambient), since (for example) during transmission at maximum power a significant fraction of DC input power is dissipated as heat This behavior is partially compensated by the definition of the upper shutdown threshold (t_{+2}) that is slightly higher than the declared environmental temperature limit.

The temperature thresholds are defined in Table 60.

Symbol	Parameter	Temperature	Remarks
t_{-2}	Low temperature shutdown	–40 °C	Equal to the absolute minimum temperature rating for the cellular module (the lower limit of the extended temperature range)
t_{-1}	Low temperature warning	–30 °C	10 °C above t_{-2}
t_{+1}	High temperature warning	+77 °C	20 °C below t_{+2}. The higher warning area for the upper range ensures that any countermeasures used to limit the thermal heating will become effective, even considering some thermal inertia of the complete assembly.
t_{+2}	High temperature shutdown	+97 °C	Equal to the internal temperature Ti measured in the worst case operating condition at typical supply voltage when the ambient temperature Ta in the reference setup (*) equals the absolute maximum temperature rating (upper limit of the extended temperature range)
(*)LISA-U2 module mounted on a 90 x 70 x 1.46 mm 4-Layers PCB with a high coverage of copper within the climatic chamber			

Table 60: Thresholds definition for the Smart Temperature Supervisor on the LISA-U2 modules

☞ The sensor measures the board temperature inside the shields, which can differ from the ambient temperature.

3.17 Bearer Independent Protocol

☞ Not supported by the "01", "x2", "63" and "68" product versions.

The Bearer Independent Protocol is a mechanism by which a cellular module provides a SIM with access to the data bearers supported by the network. With the Bearer Independent Protocol (BIP) for Over-the-Air SIM provisioning, the data transfer from and to the SIM uses either an already active PDP context or a new PDP context established with the APN provided by the SIM card.

For more details, see the u-blox AT Commands Manual [2].

3.18 Multi-Level Precedence and Pre-emption Service

☞ Not supported by the "01", "x2", "63" and "68" product versions.

The Multi-Level Precedence and Pre-emption Service (eMLPP) permits to handle the call priority. The maximum priority associated to a user is set in the SIM: within this threshold, the user can assign different priorities to the calls. This results in a differentiated treatment of the calls by the network in case of abnormal events such as handovers to congested cells.

For more details, see the u-blox AT Commands Manual [2].

3.19 Network Friendly Mode

☞ Not supported by the “01", "x2", "63" and "68" product versions.

The Network Friendly Mode (NFM) feature provides a more efficient access to the network since it regulates the number of network accesses per service type over a configurable amount of time, avoiding scenarios in which the cellular module continuously retries a registration or a PDP context activation procedure until it is successful. In case of appropriate network rejection errors, a back-off timer can be started: when the timer is running or the number of allowed accesses is reached, further attempts are denied and an URC may be enabled to indicate the time remaining before a further attempt can be served. The back-off timer controls the temporal spread of successive attempts to register to CS or PS services, to activate a PDP context and to send SMS messages.

For more details, see the u-blox AT Commands Manual [2].

3.20 Power saving

The power saving configuration is disabled by default, but it can be enabled using the AT+UPSV command. When power saving is enabled, the module automatically enters the low-power idle mode whenever possible, reducing current consumption.

During the low-power idle mode, the module is not ready to communicate with an external device by means of the application interfaces, since it is configured to reduce power consumption. The module wakes up from the low-power idle mode to the active mode in these events:

- Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (see sections 1.5.3.3, 1.9.2.3)
- Automatic periodic enable of the UART interface to receive and send data, if AT+UPSV=1 has been set (see section 1.9.2.3)
- Data received on the UART interface, if HW flow control has been disabled by AT&K0 and AT+UPSV=1 has been set (see section 1.9.2.3)
- **RTS** input set ON by the DTE if HW flow control has been disabled by AT&K0 and AT+UPSV=2 has been set (see section 1.9.2.3)
- **DTR** input set ON by DTE if AT+UPSV=3 has been set (not supported by the "01" product versions, see section 1.9.2.3)
- USB detection, applying 5 V (typ.) to **VUSB_DET** input (see section 1.9.3)
- The connected USB host forces a remote wake-up of the module as a USB device (see section 1.9.3)
- The connected SPI master indicates by means of the **SPI_MRDY** input signal of the module that it is ready for transmission or reception over the SPI interface (see section 1.9.4)
- The connected u-blox GNSS receiver indicates by means of the **GPIO3** pin previously configured for the "GNSS data ready" function that it is ready to send data over the I^2C / DDC interface (see sections 1.10, 1.12)
- RTC alarm previously configured by AT command (see the u-blox AT Commands Manual [2], AT+CALA)

For the complete description of the AT+UPSV command, see the u-blox AT Commands Manual [2].

For the definition and the description of LISA-U2 series modules operating modes, including the events forcing transitions between the different operating modes, see section 1.4.

For the description of current consumption in idle and active operating modes, see sections 1.5.3.3, 1.5.3.4.

For the description of the UART behavior related to module power saving configuration, see section 1.9.2.3.

For the description of the USB behavior related to module power saving configuration, see section 1.9.3.2.

For the description of the SPI behavior related to module power saving configuration, see section 1.9.4.2.

4 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

4.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the LISA-U2 series Data Sheet [1] and the u-blox Package Information Guide [20].

The LISA-U2 modules are Electrostatic Discharge (ESD) sensitive devices.

⚠ Ensure ESD precautions are implemented during handling of the module.

4.2 Soldering

4.2.1 Soldering paste

The use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	+217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.2.2.

☞ The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

4.2.2 Reflow soldering

A convection type soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes".

Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

⚠ Be aware that IPC/JEDEC J-STD-020 applies to integrated circuits, and cannot be properly applied to module devices.

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. This preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s – If the temperature rise is too rapid in the preheat phase, it may cause excessive slumping.
- Time: 60 – 120 s – If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200 °C – If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 - 60 seconds
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C / s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

⚠ Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

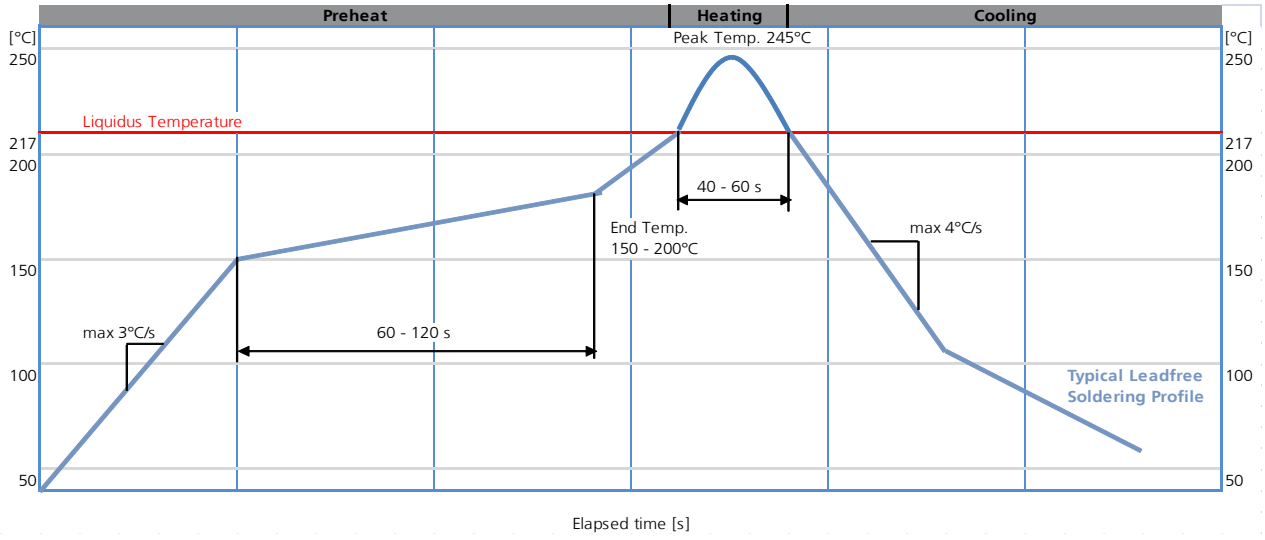


Figure 74: Recommended soldering profile

☞ LISA-U2 modules must not be soldered with a damp heat process.

4.2.3 Optical inspection

After soldering the LISA-U2 modules, inspect the modules optically to verify that the module is accurately aligned and centered.

4.2.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

4.2.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside-down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to LISA-U2 modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the LISA-U2 module, plus one reflow soldering process to mount other parts).

4.2.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for a board with a LISA-U2 module already populated on it.

Wave soldering process is not recommended for LISA-U2 series LCC modules.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty against damages to LISA-U2 modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount the LISA-U2 module, plus one wave soldering process to mount other parts).

4.2.7 Hand soldering

Hand soldering is not recommended.

4.2.8 Rework

The LISA-U2 modules can be unsoldered from the baseboard using a hot air gun.

⚠ Avoid overheating the module.

After the module is removed, clean the pads before placing.

⚠ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

4.2.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the LISA-U2 modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, so care is required in applying the coating.

☞ Conformal coating of the module will void the warranty.

4.2.10 Casting

If casting is required, use viscose or another type of silicone-pottant. The OEM is strongly advised to qualify such processes in combination with the LISA-U2 modules before implementing this in production.

☞ Casting will void the warranty.

4.2.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the LISA-U2 modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

4.2.12 Use of ultrasonic processes

LISA-U2 modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the LISA-U2 modules caused by any ultrasonic processes.

5 Product Testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are made:

- Digital self-test (firmware download, flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, real time clock, battery charger, temperature sensor, antenna detection, SIM card communication)
- Digital tests (GPIOs, digital interfaces)
- Measurement and calibration of RF characteristics in all supported bands (receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels)
- Verification of RF characteristics after calibration (modulation accuracy, power levels and spectrum performance are checked to be within tolerances when the calibration parameters are applied)

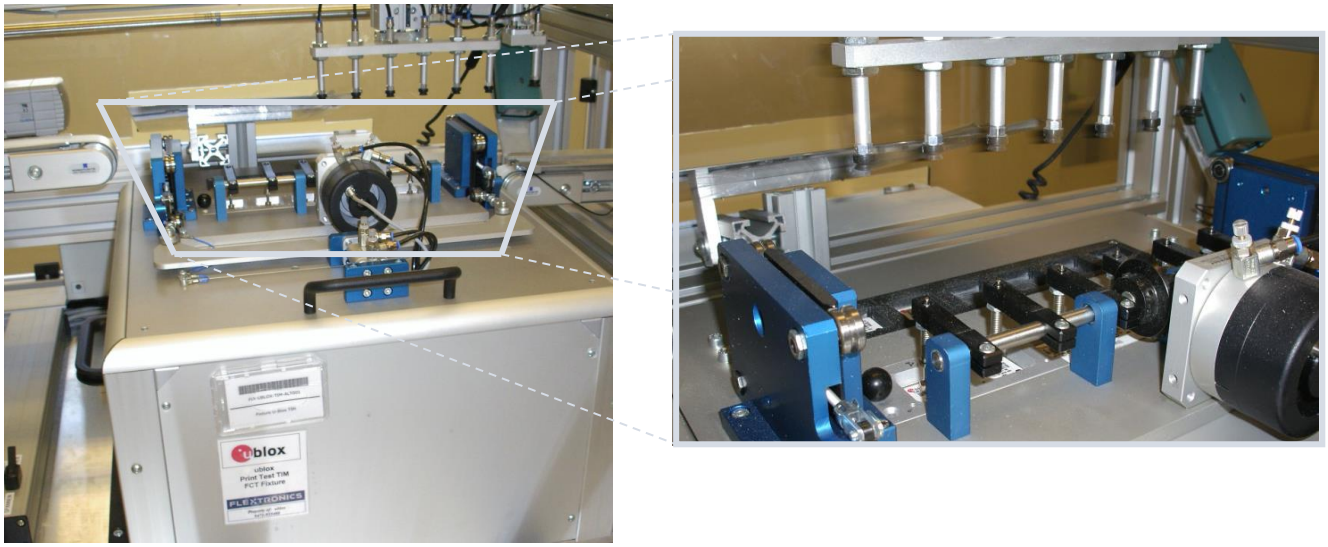


Figure 75: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - The soldering and handling process did not damaged the module components
  - All module pins are well soldered on the device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with the host controller can be established
  - The interfaces between the module and the device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

Module AT commands are used to perform functional tests (communication with host controller, check the SIM card interface, check the communication between module and GNSS, GPIOs, etc.) and to perform RF performance tests.

5.2.1 'Go/No go' tests for integrated devices

A 'Go/No go' test is to compare the signal quality with a "Golden Device" in a position with excellent 2G/3G network coverage and after having dialed a call (see the u-blox AT Commands Manual [2], AT+CSQ command: <rssi>, <ber> parameters).

☞ These kinds of test may be useful as a 'go/no go' test but not for RF performance measurements.

This test is suitable to check the communication with the host controller and SIM card, the audio and power supply functionality, and verify if components at the antenna interface are well soldered.

5.2.2 Functional tests providing RF operation

Overall RF performance test of the device including antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator using the AT+UTEST command over the AT interface.

The AT+UTEST command gives a simple interface to set the module to Rx and Tx test modes ignoring the 2G/3G signaling protocol. The command can set the module:

- Into transmitting mode in a specified channel and power level in all supported modulation schemes (single slot GMSK, single slot 8PSK, WCDMA) and 2G, 3G bands
- Into receiving mode in a specified channel to return the measured power level in all supported bands 2G, 3G

☞ See the u-blox AT Commands Manual [2] for the AT+UTEST command syntax description.

☞ See the End user test Application Note [19] for the AT+UTEST command user guide, limitations and examples of use.

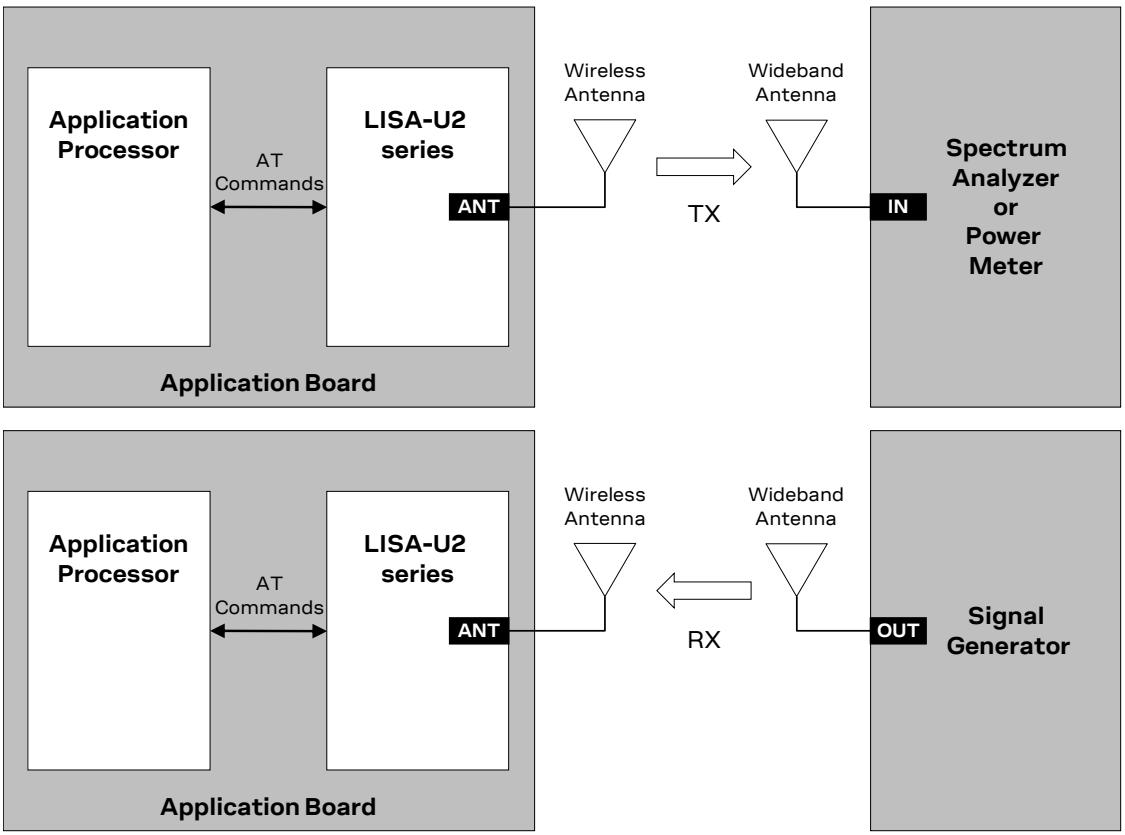


Figure 76: Setup with spectrum analyzer and signal generator for radiated measurements

This feature allows the measurement of the transmitter and receiver power levels to check the component assembly related to the module antenna interface and to check other device interfaces on which the RF performance depends.

⚠ To avoid module damage during the transmitter test, a suitable antenna according to module specifications or a 50 Ω termination must be connected to ANT pin.

⚠ To avoid module damage during receiver test the maximum power level received at ANT pin must meet module specifications.

☞ The AT+UTEST command sets the module to emit RF power ignoring 2G/3G signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purposes in controlled environments by a qualified user and must not be used during the normal module operation. Follow the instructions suggested in the u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Example of production tests for an OEM manufacturer:

1. Trigger TX GMSK burst at low Power Control Level (lower than 15) or a RX measure reporting to check:
   - If the ANT pin is soldered
   - If the ANT pin is in short circuit
   - If the module was damaged during soldering process or handling (ESD, mechanical shock…)
   - If the antenna matching components on the application board are soldered
   - If the integrated antenna is correctly connected

⚠ To avoid module damage during the transmitter test when good antenna termination is not guaranteed, use a low Power Control Level (i.e. PCL lower or equal to 15). u-blox assumes no responsibilities for module damages caused by an inappropriate use of this feature.

2. Trigger TX GMSK burst at maximum PCL:
   - To check if the power supply is correctly assembled and is able to deliver the required current
3. Trigger TX GMSK and 8PSK burst and WCDMA signal:
   - To measure current consumption
   - To check if the module components were damaged during the soldering process or during handling (ESD, mechanical shock…)
4. Trigger RX measurement:
   - To test the receiver signal level. Assuming that there are no losses between the **ANT** pin or **ANT_DIV** pin and the input power source, be aware that the power level estimated by the module can vary approximately within 3GPP tolerances for the average value
   - To check if the module was damaged during the soldering process or during handling (ESD, mechanical shock…)
5. Trigger TX GMSK and 8PSK burst and WCDMA signal and RX measurement to check:
   - Overall RF performance of the device including antenna measuring TX and RX power levels

Appendix

A Migration from LISA-U1 to LISA-U2 series

Migrating LISA-U1 series designs to LISA-U2 series modules is a straight-forward procedure. Nevertheless, there are some points to be considered during the migration.

A.1 Checklist for migration

Have you chosen the optimal module?

- ☐ For HSDPA category 14, 6-band 3G, Digital Audio Interfaces support, select a LISA-U230 module.
- ☐ For HSDPA category 8, 6-band 3G, Digital Audio Interfaces support, select a suitable LISA-U200 module.
- ☐ For HSDPA category 8, 5-band 3G, Digital Audio Interfaces support, select LISA-U201 module.
- ☐ For HSDPA category 8, 2-band 3G 850/1900 (North America), Digital Audio Interfaces support, select a suitable LISA-U260 module.
- ☐ For HSDPA category 8, 2-band 3G 900/2100 (Europe, Asia, Middle-East and Africa), Digital Audio Interfaces support, select a suitable LISA-U270 module.

Check LISA-U2 series Hardware Requirements

- ☐ Check the supported 3G bands for proper antenna circuit development, since LISA-U2 supports various 3G bands in comparison to LISA-U1 series cellular modules.
- ☐ Check audio requirements, since Analog Audio Interfaces are not supported by LISA-U2 series.
- ☐ Check audio requirements, since Digital Audio Interfaces are supported by LISA-U2 series modules.
- ☐ Check the PWR_ON low pulse time specified to switch on the module, since PWR_ON low pulse time requirement is different in comparison to LISA-U1 series modules.
- ☐ Check the PWR_ON behavior, since LISA-U2 series modules can be switched off forcing PWR_ON pin to the low level for at least 1 second.
- ☐ Check the PWR_ON input voltage thresholds, since they are slightly changed in comparison to LISA-U1 series modules. By the way, this is not relevant driving the PWR_ON input by an open drain or open collector driver as recommended.
- ☐ Check the RESET_N input voltage thresholds, since they are slightly changed in comparison to LISA-U1 series modules. By the way, this is not relevant driving the RESET_N input by an open drain or open collector driver as recommended.
- ☐ Check the V_BCKP operating characteristics, since they are slightly changed in comparison to LISA-U1 series modules.
- ☐ Check internal active pull-up / down values at digital interface input pins and the current capability of digital interface output pins, since they are slightly changed in comparison to LISA-U1 series modules.
- ☐ Check board layout, since additional signals keep-out area must be implemented on the top layer of the application board, below the LISA-U2 modules, due to GND opening on the module bottom layer.

A.2 Software migration

A.2.1 Software migration from LISA-U1 series to LISA-U2 series modules

Software migration from LISA-U1 to LISA-U2 series cellular modules is a straight-forward procedure. Nevertheless, there are some differences to be considered with firmware versions. Like its predecessors, the LISA-U2 series cellular module supports AT commands according to 3GPP standards: TS 27.007 [4], TS 27.005 [5], TS 27.010 [6] and the u-blox AT command extension. Backward compatibility has been maintained as far as possible.

☞ For the complete list of supported AT commands and their syntax, see the u-blox AT Commands Manual [2].

A.3 Hardware migration

A.3.1 Hardware migration from LISA-U1 series to LISA-U2 series modules

LISA-U2 series modules have been designed with backward compatibility in mind, but some minor differences were unavoidable. These minor differences will however not be relevant for the majority of the LISA-U1 series designs.

A clean and stable supply is required by LISA-U2 as for the LISA-U1 series: low ripple and low voltage drop must be guaranteed at the **VCC** pins. The voltage provided must be within the normal operating range limits to allow module switch-on and must be above the minimum limit of the extended operating range to avoid module switch-off. Consider that there are large current spikes in connected mode when a GSM call is enabled.

LISA-U2 series provide wider **VCC** input voltage range compared to LISA-U1 series.

The **ANT** pin has 50 Ω nominal characteristic impedance and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the 2G and 3G operating bands. The recommendations of the antenna producer for correct installation and deployment (PCB layout and matching circuitry) must be followed.

The antenna and the whole RF circuit must provide optimal radiating characteristics on the entire supported bands: note that LISA-U2 supports different 3G bands in comparison to LISA-U1 series modules.

An external application circuit can be implemented on the application device integrating LISA-U2 series modules to satisfy ESD immunity test requirements at the antenna interface, as described in Figure 68 and Table 53 in section 2.5.3. The same application circuit is not applicable for LISA-U1 series.

LISA-U230 modules provide the RF antenna input for Rx diversity on the pin 74 (named **ANT_DIV**): it has an impedance of 50 Ω. The same pad is a reserved pin on LISA-U1 series and on the other LISA-U2 series modules.

Analog audio interfaces are not supported by LISA-U2 series modules, but a second 4-wire I^2S digital audio interface is provided instead of the 4 analog audio pins. The same 4 pins can be configured as GPIO on LISA-U2 series modules.

Analog audio can be provided with an external audio codec connected to LISA-U2 series modules, implementing the application circuit described in Figure 50. An external audio codec can be connected to the I^2S digital audio interface of LISA-U1 series modules as shown in the same application circuit described in Figure 50. In this case, the application processor should properly control the audio codec by I^2C interface and should properly provide clock reference to the audio codec. This circuit allows migration from LISA-U1 series to LISA-U2 series, providing analog audio with the same application circuit.

PWR_ON low pulse time required to switch on the module is different in comparison to LISA-U1 series modules.

LISA-U2 series can be switched off forcing **PWR_ON** pin to the low level for at least 1 second.

PWR_ON and **RESET_N** input voltage thresholds are slightly changed in comparison to LISA-U1 series modules, but this is not relevant driving **PWR_ON** and **RESET_N** inputs by open drain / collector drivers as recommended.

V_BCKP operating characteristics are slightly changed in comparison to LISA-U1 series modules.

The voltage level of all the digital interfaces of LISA-U2 series modules is 1.8 V as for LISA-U1 series modules.

The internal active pull-up / pull-down values at the digital interface input pins and the current capability of digital interface output pins LISA-U2 series modules are slightly changed in comparison to LISA-U1 series modules.

UART of LISA-U2 series supports autobauding (default setting) and 921600 bit/s baud rate.

LISA-U2 series provide one additional USB CDC for the remote SIM Access Profile (SAP).

The 5 pins of the SPI / IPC Serial Interface can be configured as GPIOs on LISA-U2 series.

The DDC (I^2C) interface of LISA-U2 series modules can be used to communicate with u-blox GNSS receivers and at the same time to control an external audio codec. The LISA-U2 series module acts as an I^2C master which can communicate to two I^2C slaves as permitted by the I^2C bus specifications [8].

LISA-U2 modules provide additional GPIO functions: Module Status and Operating Mode Indications.

LISA-U2 modules are SMT modules and share the same compact form factor as the LISA-U1 series, featuring Leadless Chip Carrier (LCC) packaging technology.

An additional signal keep-out area must be implemented on the top layer of the application board, below LISA-U2 modules, due to the GND opening on the module bottom layer.

Detailed pinout and layout comparisons between LISA-U1 series and LISA-U2 series modules, with remarks for migration, are provided in subsections A.3.2 and A.3.3.

For more information about the electrical characteristics of the LISA-U1 and LISA-U2 series modules, see the LISA-U1 series Data Sheet [28] and the LISA-U2 series Data Sheet [1].

A.3.2 Pin-out comparison LISA-U1 series vs. LISA-U2 series

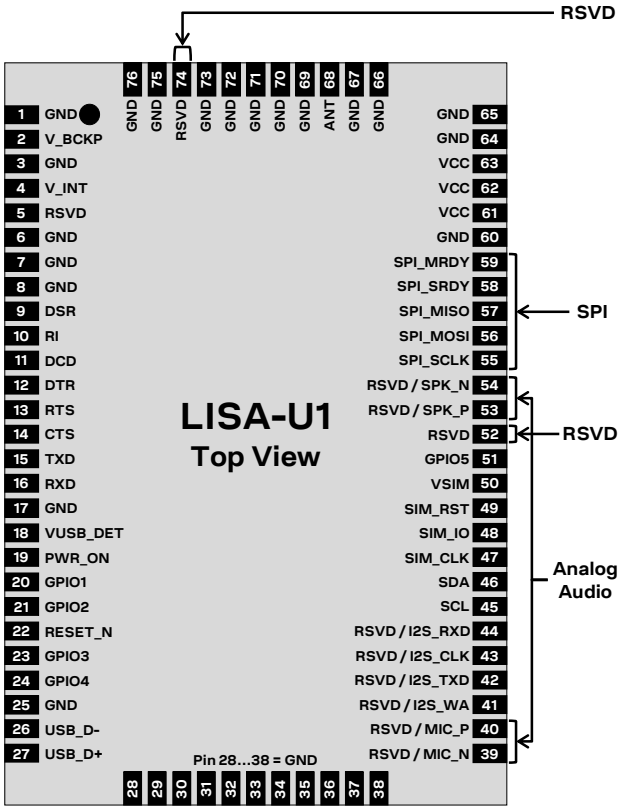


Figure 77: LISA-U1 series pin assignment

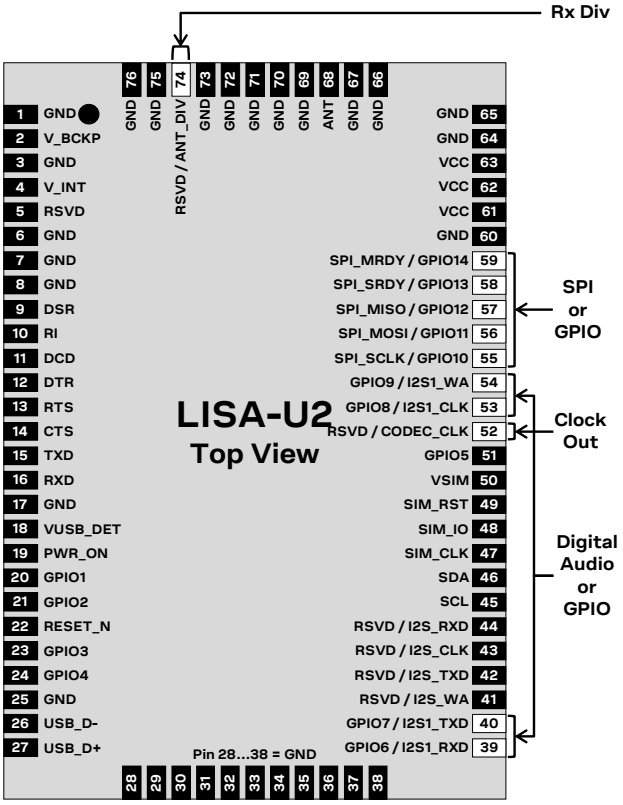


Figure 78: LISA-U2 series pin assignment (highlighted name/function changes)

	LISA-U1 series		LISA-U2 series		
No	**Name**	**Description**	**Name**	**Description**	**Remarks for Migration**
1	GND	Ground	GND	Ground	
2	V_BCKP	RTC supply input/output	V_BCKP	RTC supply input/output	V_BCKP operating characteristics difference: LISA-U1 series: V_BCKP output = 2.3 V typ. V_BCKP input = 1.0 V min / 2.5 V max LISA-U2 series: V_BCKP output = 1.8 V typ. V_BCKP input = 1.0 V min / 1.9 V max
3	GND	Ground	GND	Ground	
4	V_INT	Digital Interfaces supply output	V_INT	Digital Interfaces supply output	No difference: V_INT output = 1.8 V typ., 70 mA max.
5	RSVD	RESERVED pin	RSVD	RESERVED pin	No difference: This pin must be connected to GND
6...8	GND	Ground	GND	Ground	
9	DSR	UART data set ready output	DSR	UART data set ready output	Circuit 107 (DSR) in ITU-T V.24, 1.8 V typ. LISA-U1 series: Output driver strength = 4 mA LISA-U2 series: Output driver strength = 1 mA

	LISA-U1 series		LISA-U2 series		
10	RI	UART ring indicator output	RI	UART ring indicator output	Circuit 125 (RI) in ITU-T V.24, 1.8 V typ. LISA-U1 series: Output driver strength = 4 mA LISA-U2 series: Output driver strength = 2 mA
11	DCD	UART data carrier detect output	DCD	UART data carrier detect output	Circuit 109 (DCD) in ITU-T V.24, 1.8 V typ. LISA-U1 series: Output driver strength = 4 mA LISA-U2 series: Output driver strength = 2 mA
12	DTR	UART data terminal ready input	DTR	UART data terminal ready input	Circuit 108/2 (DTR) in ITU-T V. 24, 1.8 V typ. LISA-U1 series: Internal active pull-up = -110 µA LISA-U2 series: Internal active pull-up = -125 µA
13	RTS	UART ready to send input	RTS	UART ready to send input	Circuit 105 (RTS) in ITU-T V.24, 1.8 V typ. LISA-U1 series: Internal active pull-up = -60 µA LISA-U2 series: Internal active pull-up = -240 µA
14	CTS	UART clear to send output	CTS	UART clear to send output	Circuit 106 (CTS) in ITU-T V.24, 1.8 V typ. LISA-U1 series: Output driver strength = 4 mA LISA-U2 series: Output driver strength = 6 mA
15	TXD	UART transmitted data input	TXD	UART transmitted data input	Circuit 103 (TxD) in ITU-T V.24, 1.8 V typ. LISA-U1 series: Internal active pull-up = -60 µA LISA-U2 series: Internal active pull-up = -240 µA
16	RXD	UART received data output	RXD	UART received data output	Circuit 104 (RxD) in ITU-T V.24, 1.8 V typ. LISA-U1 series: Output driver strength = 4 mA LISA-U2 series: Output driver strength = 6 mA
17	GND	Ground	GND	Ground	
18	VUSB_DET	USB detect input	VUSB_DET	USB detect input	No difference

	LISA-U1 series		LISA-U2 series		
19	PWR_ON	Power-on input	PWR_ON	Power-on input	PWR_ON switch-on low pulse time difference: LISA-U1 series: L-level pulse time = 5 ms min LISA-U2 series: L-level pulse time = 50 µs min / 80 µs max PWR_ON switch-off low pulse time difference: LISA-U1 series: Switch-off by PWR_ON not supported LISA-U2 series: L-level pulse time = 1 s min PWR_ON operating voltage difference: LISA-U1 series: L-level input = -0.30 V min / 0.65 V max H-level input = 2.00 V min / 4.20 V max External pull-up (e.g. to V_BCKP) required LISA-U2 series: L-level input = -0.30 V min / 0.65 V max H-level input = 1.50 V min / 4.40 V max External pull-up (e.g. to V_BCKP) required
20	GPIO1	GPIO	GPIO1	GPIO	Configurable GPIO, 1.8 V typ. LISA-U1 series: Output driver strength = 1 mA LISA-U2 series: Output driver strength = 6 mA Functions on all LISA-U series: Pad disabled (default) Input / Output Network Status Indication GNSS Supply Enable GSM Tx Burst Indication Function on LISA-U2 series: Module Status Indication
21	GPIO2	GPIO	GPIO2	GPIO	Configurable GPIO, 1.8 V typ. LISA-U1 series: Output driver strength = 1 mA LISA-U2 series: Output driver strength = 1 mA Functions on all LISA-U series: Pad disabled Input / Output Network Status Indication GNSS Supply Enable (default)

	LISA-U1 series		LISA-U2 series		
22	RESET_N	External reset input	RESET_N	External reset input	RESET_N hardware reset or switch-on low pulse time: LISA-U1 series: L-level pulse time = 50 ms min LISA-U2 series: L-level pulse time = 50 ms min RESET_N operating voltage difference: LISA-U1 series: L-level input = -0.30 V min / 0.65 V max H-level input = 1.69 V min / 2.48 V max Internal 10kΩ pull-up to V_BCKP (2.3 V typ.) LISA-U2 series: L-level input = -0.30 V min / 0.51 V max H-level input = 1.32 V min / 2.01 V max Internal 10 kΩ pull-up to V_BCKP (1.8 V typ.)
23	GPIO3	GPIO	GPIO3	GPIO	Configurable GPIO, 1.8 V typ. LISA-U1 series: Output driver strength = 4 mA LISA-U2 series: Output driver strength = 6 mA Functions on all LISA-U series: Pad disabled Input / Output Network Status Indication GNSS Supply Enable GNSS Data Ready (default)
24	GPIO4	GPIO	GPIO4	GPIO	Configurable GPIO, 1.8 V typ. LISA-U1 series: Output driver strength = 4 mA LISA-U2 series: Output driver strength = 6 mA Functions on all LISA-U series: Pad disabled Input / Output Network Status Indication GNSS Supply Enable GNSS RTC Sharing (default)
25	GND	Ground	GND	Ground	
26	USB_D-	USB Data Line D- input/output	USB_D-	USB Data Line D- input/output	No difference
27	USB_D+	USB Data Line D+ input/output	USB_D+	USB Data Line D+ input/output	No difference
28...38	GND	Ground	GND	Ground	
39	MIC_N	LISA-U120, LISA-U130: Differential analog audio input (neg.) LISA-U100, LISA-U110: RESERVED pin	I2S1_RXD / GPIO6	LISA-U2 series, 2nd I²S Rx data input / GPIO	LISA-U120, LISA-U130: Differential analog audio input (neg.) LISA-U2 series: I2S1_RXD and configurable GPIO, 1.8 V typ. Output driver strength = 1 mA Internal active pull-down = 150 µA Functions: I2S1_RXD (default) Pad disabled Input / Output

	LISA-U1 series		LISA-U2 series		
40	MIC_P	LISA-U120, LISA-U130: Differential analog audio input (pos.) LISA-U100, LISA-U110: RESERVED pin	I2S1_TXD / GPIO7	LISA-U2 series: 2nd I²S Tx data output / GPIO	LISA-U120, LISA-U130: Differential analog audio input (pos.) LISA-U2 series: I2S1_TXD and configurable GPIO, 1.8 V typ. Output driver strength = 1 mA Functions: I2S1_TXD (default) Pad disabled Input / Output
41	I2S_WA	LISA-U120, LISA-U130: I²S word alignment LISA-U100, LISA-U110: RESERVED pin	I2S_WA	LISA-U2 series: 1st I²S word alignment input/output	I2S_WA, 1.8 V typ. LISA-U120, LISA-U130: Output driver strength = 2.5 mA Internal active pull-down = 100 µA LISA-U2 series: Output driver strength = 2 mA Internal active pull-down = 200 µA
42	I2S_TXD	LISA-U120, LISA-U130: I²S Tx data output LISA-U100, LISA-U110: RESERVED pin	I2S_TXD	LISA-U2 series: 1st I²S Tx data output	I2S_TXD, 1.8 V typ. LISA-U120, LISA-U130: Output driver strength = 2.5 mA LISA-U2 series: Output driver strength = 2 mA
43	I2S_CLK	LISA-U120, LISA-U130: I²S clock LISA-U100, LISA-U110: RESERVED pin	I2S_CLK	LISA-U2 series: 1st I²S clock input/output	I2S_CLK, 1.8 V typ. LISA-U120, LISA-U130: Output driver strength = 2.5 mA Internal active pull-down = 100 µA LISA-U2 series: Output driver strength = 2 mA Internal active pull-down = 200 µA
44	I2S_RXD	LISA-U120, LISA-U130: I²S Rx data input LISA-U100, LISA-U110: RESERVED pin	I2S_RXD	LISA-U2 series: 1st I²S Rx data input	I2S_RXD, 1.8 V typ. LISA-U120, LISA-U130: Output driver strength = 2.5 mA Internal active pull-down = 100 µA LISA-U2 series: Output driver strength = 2 mA Internal active pull-down = 200 µA
45	SCL	I²C bus clock line output	SCL	I²C bus clock line output	LISA-U1 series: I²C SCL for GNSS, 1.8 V typ. Fixed open drain External pull-up (e.g. to V_INT) required LISA-U2 series: I²C SCL for GNSS and other I²C devices, 1.8 V typ. Fixed open drain External pull-up (e.g. to V_INT) required
46	SDA	I²C bus data line input/output	SDA	I²C bus data line input/output	LISA-U1 series: I²C SDA for GNSS, 1.8 V typ. Fixed open drain External pull-up (e.g. to V_INT) required LISA-U2 series: I²C SDA for GNSS and other I²C devices, 1.8 V typ Fixed open drain External pull-up (e.g. to V_INT) required

	LISA-U1 series		LISA-U2 series		
47	SIM_CLK	SIM clock output	SIM_CLK	SIM clock output	No difference: 3.25 MHz clock frequency for SIM card
48	SIM_IO	SIM data input/output	SIM_IO	SIM data input/output	No difference: Internal 4.7 kΩ pull-up resistor to VSIM.
49	SIM_RST	SIM reset output	SIM_RST	SIM reset output	No difference: Reset output for SIM card
50	VSIM	SIM supply output	VSIM	SIM supply output	No difference: VSIM output = 1.80 V typ. or 2.90 V typ.
51	GPIO5	GPIO	GPIO5	GPIO	Configurable GPIO, 1.8 V typ. LISA-U1 series: Output driver strength = 2.5 mA LISA-U2 series: Output driver strength = 6 mA Functions on all LISA-U series: Pad disabled Input / Output SIM card detection (default) Network Status Indication GNSS Supply Enable Functions on LISA-U2 series only: Module Operating Mode Indication SIM card hot insertion/removal (+UDCONF)
52	RSVD	RESERVED pin	CODEC_CLK	LISA-U2 series: Clock output	LISA-U2 series: Digital clock output for external audio codec Output driver strength = 4 mA
53	SPK_P	LISA-U120, LISA-U130: Differential analog audio output (pos.) LISA-U100, LISA-U110: RESERVED pin	I2S1_CLK / GPIO8	LISA-U2 series: 2nd I²S clock input/output / GPIO	LISA-U120, LISA-U130: Differential analog audio output (pos.) LISA-U2 series: I2S1_CLK and configurable GPIO, 1.8 V typ. Output driver strength = 1 mA Internal active pull-down = 150 µA Functions: I2S1_CLK (default) Pad disabled Input / Output
54	SPK_N	LISA-U120, LISA-U130: Differential analog audio output (neg.) LISA-U100, LISA-U110: RESERVED pin	I2S1_WA / GPIO9	LISA-U2 series: 2nd I²S word alignment input/output / GPIO	LISA-U120, LISA-U130: Differential analog audio output (neg.) LISA-U2 series: I2S1_WA and configurable GPIO, 1.8 V typ. Output driver strength = 1 mA Internal active pull-down = 150 µA Functions: I2S1_WA (default) Pad disabled Input / Output

	LISA-U1 series		LISA-U2 series		
55	SPI_SCLK	SPI Serial Clock Input	SPI_SCLK / GPIO10	SPI Serial Clock Input / GPIO	LISA-U1 series: SPI_CLK, 1.8 V typ Internal active pull-down = 100 µA LISA-U2 series: SPI_CLK and configurable GPIO, 1.8 V typ. Internal active pull-down = 200 µA Output driver strength = 6 mA Functions: SPI_CLK (default) Pad disabled Input / Output
56	SPI_MOSI	SPI Data Line Input	SPI_MOSI / GPIO11	SPI Data Line Input / GPIO	LISA-U1 series: SPI_MOSI, 1.8 V typ Internal active pull-up = -110 µA LISA-U2 series: SPI_MOSI and configurable GPIO, 1.8 V typ. Internal active pull-up = -240 µA Output driver strength = 6 mA Functions: SPI_MOSI (default) Pad disabled Input / Output
57	SPI_MISO	SPI Data Line Output	SPI_MISO / GPIO12	SPI Data Line Output / GPIO	LISA-U1 series: SPI_MISO, 1.8 V typ Output driver strength = 2.5 mA LISA-U2 series: SPI_MISO and configurable GPIO, 1.8 V typ. Output driver strength = 6 mA Functions: SPI_MISO (default) Pad disabled Input / Output
58	SPI_SRDY	SPI Slave Ready Output	SPI_SRDY / GPIO13	SPI Slave Ready Output / GPIO	LISA-U1 series: SPI_SRDY, 1.8 V typ Output driver strength = 4 mA LISA-U2 series: SPI_SRDY and configurable GPIO, 1.8 V typ. Output driver strength = 6 mA Functions: SPI_SRDY (default) Pad disabled Input / Output Module Status Indication

	LISA-U1 series		LISA-U2 series		
59	SPI_MRDY	SPI Master Ready Input	SPI_MRDY / GPIO14	SPI Master Ready Input / GPIO	LISA-U1 series: SPI_MRDY, 1.8 V typ Internal active pull-down = 55 µA LISA-U2 series: SPI_MRDY and configurable GPIO, 1.8 V typ. Internal active pull-down = 200 µA Output driver strength = 6 mA Functions: SPI_MRDY (default) Pad disabled Input / Output Module Operating Mode Indication
60	GND	Ground	GND	Ground	
61…63	VCC	Module supply input	VCC	Module supply input	VCC operating voltage difference: LISA-U1 series: VCC normal range = 3.4 V min / 4.2 V max VCC extended range = 3.1 V min / 4.2 V max LISA-U2 series: VCC normal range = 3.3 V min / 4.4 V max VCC extended range = 3.1 V min / 4.5 V max
64…67	GND	Ground	GND	Ground	
68	ANT	RF antenna	ANT	RF input/output for main Tx/Rx antenna	3G band support difference: LISA-U100, LISA-U120, LISA-U260: Band II (1900), Band V (850) LISA-U110, LISA-U130, LISA-U270: Band I (2100), Band VIII (900) LISA-U200-00S: Band I (2100), Band II (1900), Band V (850), Band VI (800) All LISA-U2 series except LISA-U200-00S: Band I (2100), Band II (1900), Band IV (1700), Band V (850), Band VI (800), Band VIII (900)
69…73	GND	Ground	GND	Ground	
74	RSVD	RESERVED pin	RSVD	All except LISA-U230: RESERVED pin	LISA-U1 series and all LISA-U2 series except LISA-U230: RESERVED pin Leave unconnected
			ANT_DIV	LISA-U230: RF input for Rx diversity antenna	LISA-U230: RF antenna input for Rx diversity 50 Ω nominal impedance
75	GND	Ground	GND	Ground	
76	GND	Ground	GND	Ground	

Table 61: Pinout comparison LISA-U1 series vs. LISA-U2 series

A.3.3 Layout comparison LISA-U1 series vs. LISA-U2 series

The additional signals keep-out area must be implemented on the top layer of the application board, below LISA-U2 modules, due to the GND opening on module bottom layer, as described in Figure 79 and Figure 80.

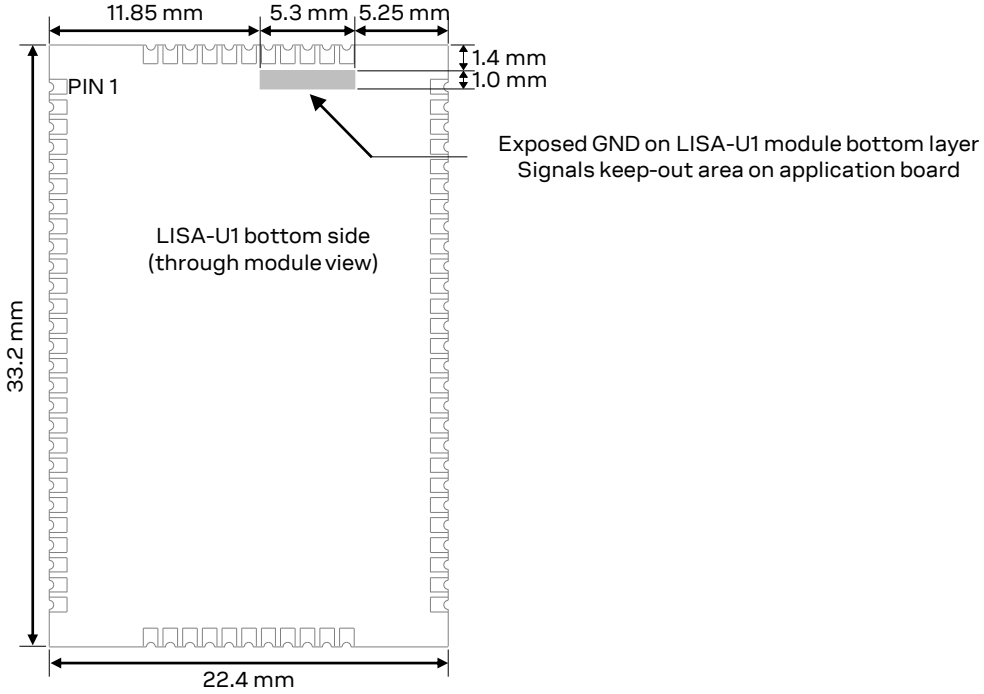


Figure 79: Signals keep-out area on the top layer of the application board, below LISA-U1 series modules

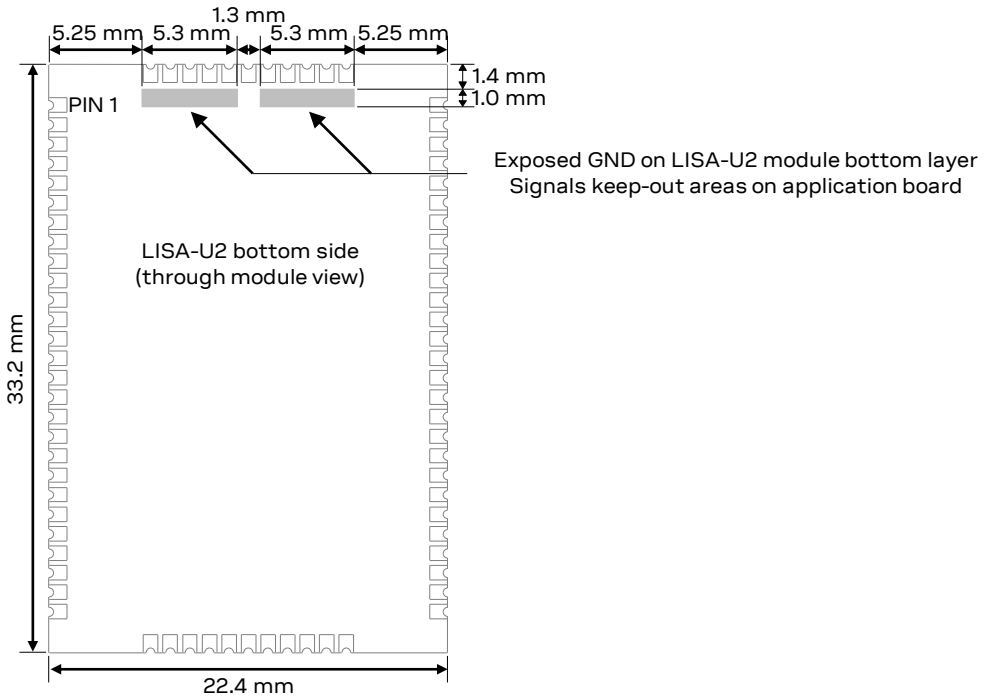


Figure 80: Signals keep-out areas on the top layer of the application board, below LISA-U2 series modules

B Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
AP	Application Processor
AT	AT Command Interpreter Software Subsystem, or attention
CBCH	Cell Broadcast Channel
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DDC	Display Data Channel
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTM	Dual Transfer Mode
DTR	Data Terminal Ready
EBU	External Bus Interface Unit
EDGE	Enhanced Data rates for GSM Evolution
E-GPRS	Enhanced GPRS
FDD	Frequency Division Duplex
FEM	Front End Module
FOAT	Firmware Over AT commands
FTP	File Transfer Protocol
FTPS	FTP Secure
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HF	Hands-free
HSDPA	High Speed Downlink Packet Access
HTTP	HyperText Transfer Protocol
HTTPS	Hypertext Transfer Protocol over Secure Socket Layer
HW	Hardware
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit
I^2S	Inter IC Sound
IP	Internet Protocol
IPC	Inter Processor Communication
LNA	Low Noise Amplifier
MCS	Modulation Coding Scheme
NOM	Network Operating Mode
PA	Power Amplifier

Abbreviation	Definition
PBCCH	Packet Broadcast Control Channel
PCM	Pulse Code Modulation
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
RF	Radio Frequency
RI	Ring Indicator
RTC	Real Time Clock
RTS	Request To Send
RXD	RX Data
SAW	Surface Acoustic Wave
SIM	Subscriber Identification Module
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SPI	Serial Peripheral Interface
SRAM	Static RAM
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TXD	TX Data
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
UTRA	UMTS Terrestrial Radio Access
VC-TCXO	Voltage Controlled - Temperature Compensated Crystal Oscillator
WCDMA	Wideband CODE Division Multiple Access

Table 62: Explanation of the abbreviations and terms used

Related documents

[1] u-blox LISA-U2 series Data Sheet, document UBX-13001734
[2] u-blox AT Commands Manual, document UBX-13002752
[3] ITU-T Recommendation V.24, 02-2000. List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en
[4] 3GPP TS 27.007 - AT command set for User Equipment (UE)
[5] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[6] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
[7] USB Revision 2.0 specification, http://www.usb.org/developers/docs/usb20_docs/
[8] I2C-Bus specification and user manual - NXP Semiconductors, http://www.nxp.com/documents/user_manual/UM10204.pdf
[9] 3GPP TS 51.010-2 - Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS)
[10] 3GPP TS 34.121-2 - Technical Specification Group Radio Access Network; User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 2: Implementation Conformance Statement (ICS)
[11] CENELEC EN 61000-4-2: "Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test".
[12] ETSI EN 301 489-1: “Electromagnetic compatibility and Radio spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements”
[13] ETSI EN 301 489-52: "Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 52: Specific conditions for Cellular Communication Mobile and portable (UE) radio and ancillary equipment"
[14] u-blox Multiplexer Implementation Application Note, document UBX-13001887
[15] u-blox GNSS Implementation Application Note, document UBX-13001849
[16] u-blox Firmware Update Application Note, document UBX-13001845
[17] u-blox SPI Interface Application Note, document UBX-13001919
[18] 3GPP TS 23.060 - Technical Specification Group Services and System Aspects; General Packet Radio Service (GPRS); Service description
[19] u-blox End user test Application Note, document WLS-CS-12002
[20] u-blox Package Information Guide, document GPS-X-11004
[21] SIM Access Profile Interoperability Specification, Revision V11r00, http://www.bluetooth.org
[22] u-blox LISA-U1 / LISA-U2 Audio Application Note, Docu No UBX-13001835
[23] 3GPP TS 26.267 V10.0.0 – eCall Data Transfer; In-band modem solution; General description
[24] BS EN 16062: Intelligent transport systems – eSafety – eCall high level application requirements
[25] ETSI TS 122 101– Service aspects; Service principles (3GPP TS 22.101 v.8.7.0 Rel. 8)
[26] 3GPP TS 44.031 Location Services (LCS); Mobile Station (MS) - Serving Mobile Location Centre (SMLC) Radio Resource LCS Protocol (RRLP)
[27] 3GPP TS 25.331 Radio Resource Control (RRC); Protocol specification
[28] u-blox LISA-U1 series Data Sheet, document UBX-13002048

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
-	21-Oct-2010	sses	Initial Release
1	11-Jan-2011	sses	Thickness information added. GPIO description improved
2	26-Apr-2011	lpah	Update to Advance Information status
3	07-Jul-2011	lpah	Update to Preliminary status
A	26-Oct-2011	sses	Changed status to Objective Specification. Initial release for LISA-U series: From LISA-U1x0-00S system integration manual, added the description and the integration of LISA-U1x0-01S, LISA-U200-00S, LISA-U2x0-01S
A1	22-Nov-2011	sses	Update to Advance Information status. Updated module behavior during power-off sequence. Added LISA-U200-00S ESD application circuit for antenna port. Added application circuit for the module status indication function.
A2	02-Feb-2012	sses	Update to Preliminary status. Updated Federal Communications Commission notice. Updated LISA-U2 features in module power-off and GPIO sections
A3	25-May-2012	gcom	Updated values for antenna gain
A4	20-Jun-2012	sses	Update to Advance Information status. Updated PWR_ON behavior. Updated UART and power saving behavior. Added 3V / 1.8V SPI application circuit. Updated GPS RTC sharing application circuit. Added remote SIM access profile description
A5	24-Aug-2012	sses	Update to Preliminary status. Updated FCC notice. Updated recommended VCC bypass capacitors. Added LISA-U110-60S and LISA-U130-60S
A6	04-Oct-2012	lpah / sses	Update to Advance Information status. Added LISA-U260 and LISA-U270
A7	26-Nov-2012	lpah / sses	Update to Preliminary status. Removed document applicability to LISA-U1x0-00S versions. Added document applicability to LISA-U110-50S versions
A8	29-Mar-2013	sses	Updated additional recommendations for VCC application circuits (Last revision with old doc number, 3G.G2-HW-10002)
B	15-Jul-2013	sses	Update status to Advance Information First release for LISA-U200-02S, LISA-U200-61S, LISA-U200-62S, LISA-U260-02S, LISA-U270-02S, LISA-U270-62S
B1	21-Aug-2013	lpah	Update status to Preliminary
R16	20-Mar-2014	lpah / sses	Extended document applicability to LISA-U200-52S and LISA-U200-82S (LISA-U200 FOTA). Updated recommended I2C voltage translator and clarified I2C application circuits remarks. Clarified and improved power-on, power-off and reset timings and procedures descriptions
R17	26-Jun-2015	sfal	Extended document applicability to LISA-U200-03S and LISA-U201-03S
R18	10-Aug-2015	sfal	Early Production Information status. Removed LISA-U1 series modules and LISA-U200-00S. Extended applicability to LISA-U200-83S and LISA-U270-68S
R19	04-Nov-2015	sses	Updated FCC and IC notices
R20	21-Jan-2016	sfal	Updated European Conformance CE mark notice, added LISA-U201 Anatel certification details, updated the list of supported USB drivers and extended applicability to LISA-U201-83S
R21	12-May-2016	lpah	Extended applicability to LISA-U201-03A and LISA-U270-63S
R22	07-Oct-2016	lpah	Updated status to Production Information Extended applicability to LISA-U200-62S-02 and removed LISA-U200-82S
R23	17-Mar-2017	lpah	"Disclosure restriction" replaces "Document status" on page 2 and document footer Extended applicability to LISA-U201-03A-01
R24	10-Jan-2018	lpah / sses	Updated approvals section Extended document applicability to new LISA-U2 type numbers
R25	10-Apr-2019	lpah / sses	Extended the document applicability to LISA-U200-01S-03, LISA-U200-03S-02, LISA-U200-52S-03, LISA-U200-62S-04, LISA-U230-01S-03, LISA-U270-63S-02. Minor other clarifications, corrections and description improvements.

Contact

For complete contact information, visit us at www.u-blox.com.

u-blox Offices

North, Central and South America

u-blox America, Inc.
Phone:+1 703 483 3180
E-mail:info_us@u-blox.com

Regional Office West Coast:
Phone:+1 408 573 3640
E-mail:info_us@u-blox.com

Technical Support:
Phone:+1 703 483 3185
E-mail:support@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG
Phone:+41 44 722 74 44
E-mail:info@u-blox.com
Support:support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.
Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support:support_ap@u-blox.com

Regional Office Australia:
Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support:support_ap@u-blox.com

Regional Office China (Beijing):
Phone:+86 10 68 133 545
E-mail:info_cn@u-blox.com
Support:support_cn@u-blox.com

Regional Office China (Chongqing):
Phone:+86 23 6815 1588
E-mail:info_cn@u-blox.com
Support:support_cn@u-blox.com

Regional Office China (Shanghai):
Phone:+86 21 6090 4832
E-mail:info_cn@u-blox.com
Support:support_cn@u-blox.com

Regional Office China (Shenzhen):
Phone:+86 755 8627 1083
E-mail:info_cn@u-blox.com
Support:support_cn@u-blox.com

Regional Office India:
Phone:+91 80 405 092 00
E-mail:info_in@u-blox.com
Support:support_in@u-blox.com

Regional Office Japan (Osaka):
Phone:+81 6 6941 3660
E-mail:info_jp@u-blox.com
Support:support_jp@u-blox.com

Regional Office Japan (Tokyo):
Phone:+81 3 5775 3850
E-mail:info_jp@u-blox.com
Support:support_jp@u-blox.com

Regional Office Korea:
Phone:+82 2 542 0861
E-mail:info_kr@u-blox.com
Support:support_kr@u-blox.com

Regional Office Taiwan:
Phone:+886 2 2657 1090
E-mail:info_tw@u-blox.com
Support:support_tw@u-blox.com