WIRELESS

locate, communicate, accelerate

SARA-G3 series

GSM/GPRS modules

System Integration Manual

Abstract

This document describes the features and the system integration of SARA-G3 series GSM/GPRS wireless modules.

These modules are complete and cost efficient solutions offering up to quad-band GSM/GPRS voice and/or data transmission technology in a compact form factor.

26.0 x 16.0 x 3.0 mm

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Document Information	
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Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
SARA-G300	SARA-G300-00S-00	TBD	TBD
SARA-G310	SARA-G310-00S-00	TBD	TBD
SARA-G350	SARA-G350-00S-00	08.45	GSM.G2-TN-13001
SARA-G350 ECALL	SARA-G350-71S-00	08.45	GSM.G2-TN-13001

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

AT Commands Manual: This document provides the description of the supported AT commands by the SARA-G3 series modules to verify all implemented functionalities.

System Integration Manual: This manual provides hardware design instructions and information on how to set up production and final product tests.

Application Note: document provides general design instructions and information that applies to all u-blox Wireless modules. See Related documents section for a list of Application Notes related to your Wireless Module.

How to use this Manual

The SARA-G3 series System Integration Manual provides the necessary information to successfully design in and configure these u-blox wireless modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:


An index finger points out key information pertaining to module integration and performance.


A warning symbol indicates actions that could negatively impact or damage the module.

Questions

If you have any questions about u-blox Wireless Integration:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com
- Read the questions and answers on our FAQ database on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

Contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support, have the following information ready:

- Module type (e.g. SARA-G350) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

SARA-G3 series are versatile 2.5G GSM/GPRS wireless modules in a miniature LGA (Land Grid Array) form factor.

SARA-G350 is a full feature quad-band GSM/GPRS wireless module with a comprehensive feature set including an extensive set of internet protocols. SARA-G350 also provides fully integrated access to u-blox GPS/GNSS positioning chips and modules, with embedded A-GPS (AssistNow Online and AssistNow Offline) functionality.

SARA-G310 and SARA-G300 are respectively quad-band and dual-band GSM/GPRS wireless modules targeted for high volume cost sensitive applications, providing GSM/GPRS functionalities with a reduced set of additional features to minimize the customer's total cost of ownership.

SARA-G3 wireless modules are certified and approved by the main regulatory bodies and operators, and RIL software for Android and Embedded Windows are available free of charge. SARA-G3 modules are manufactured in ISO/TS 16949 certified sites. Each module is tested and inspected during production. The modules are qualified according to ISO 16750 – Environmental conditions and electrical testing for electrical and electronic equipment for road vehicles.

Table 1 describes a summary of interfaces and features provided by SARA-G3 modules.

Module	Data Rate		Bands		Interfaces					Audio		Functions													
	GPRS multi-slot class 10	GPRS multi-slot class 2	GSM/GPRS quad-band	GSM/GPRS dual-band (900/1800 MHz)	UART	SPI	USB	DDC for u-blox GPS/GNSS receivers	GPIO	Analog Audio	Digital Audio	Network indication	Antenna detection	Jamming detection	Embedded TCP/UDP	FTP, HTTP, SMTP	SSL	GPS/GNSS via Modem	AssistNow software	FW update over AT (FOAT)	FW update over the air (FOTA)	In-band modem	CellLocate™	Low power idle-mode
SARA-G300		•		•	2															•				E
SARA-G310		•	•		2															•				E
SARA-G350	•		•		2			•	4	•	•	•	•	•	•	•		•	•	•	A		•	•
SARA-G350 ECALL	•		•		2			•	4	•	•	•	•	•	•	•		•	•	•	A	•	•	•

A = available upon request
E = external 32 kHz signal required for low power idle-mode

Table 1: SARA-G3 series features summary

Table 2 reports a summary of GSM/GPRS characteristics of SARA-G3 series modules.

Item	SARA-G300	SARA-G310	SARA-G350
GSM/GPRS Protocol Stack	3GPP Release 99	3GPP Release 99	3GPP Release 99
Mobile Station Class	Class B[1]	Class B[1]	Class B[1]
GSM/GPRS Bands	E-GSM 900 MHz DCS 1800 MHz	GSM 850 MHz E-GSM 900 MHz DCS 1800 MHz PCS 1900 MHz	GSM 850 MHz E-GSM 900 MHz DCS 1800 MHz PCS 1900 MHz
GSM/GPRS Power Class	Class 4 (33 dBm) for 900 Class 1 (30 dBm) for 1800	Class 4 (33 dBm) for 850/900 Class 1 (30 dBm) for 1800/1900	Class 4 (33 dBm) for 850/900 Class 1 (30 dBm) for 1800/1900
Packet Switched Data Rate	GPRS multi-slot class 2[2] Coding scheme CS1-CS4 Up to 42.8 kb/s DL[3] Up to 21.4 kb/s UL[3]	GPRS multi-slot class 2[2] Coding scheme CS1-CS4 Up to 42.8 kb/s DL[3] Up to 21.4 kb/s UL[3]	GPRS multi-slot class 10[4] Coding scheme CS1-CS4 Up to 85.6 kb/s DL[3] Up to 42.8 kb/s UL[3]
Circuit Switched Data Rate	None	None	Up to 9.6 kb/s DL/UL[3] Transparent mode Non transparent mode
Network Operation Modes	I to III	I to III	I to III

Table 2: SARA-G3 series GSM/GPRS characteristics summary

[1] Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for
[2] GPRS multi-slot class 2 implies a maximum of 2 slots in DL (reception) and 1 slot in UL (transmission) with 3 slots in total.
[3] The maximum bit rate of the module depends on the current network settings.
[4] GPRS multi-slot class 10 implies a maximum of 4 slots in DL (reception) and 2 slots in UL (transmission) with 5 slots in total.

1.2 Architecture

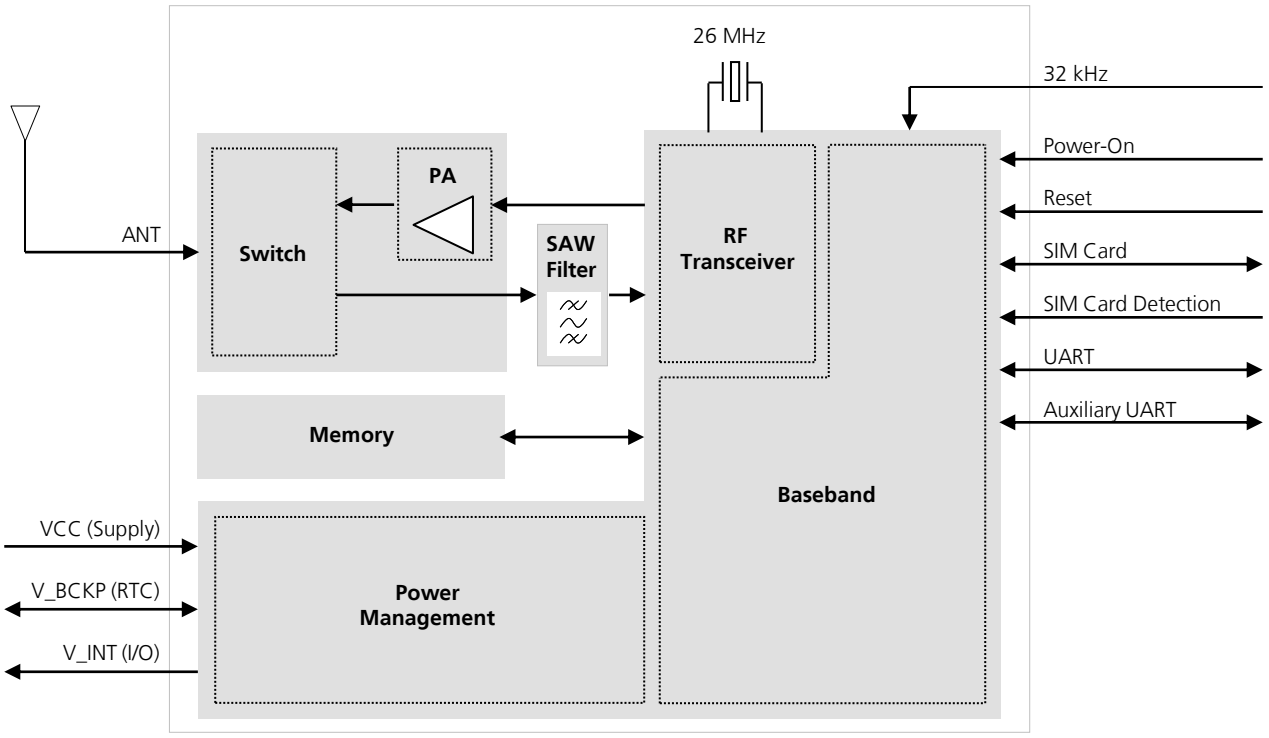


Figure 1: SARA-G300 and SARA-G310 modules block diagram

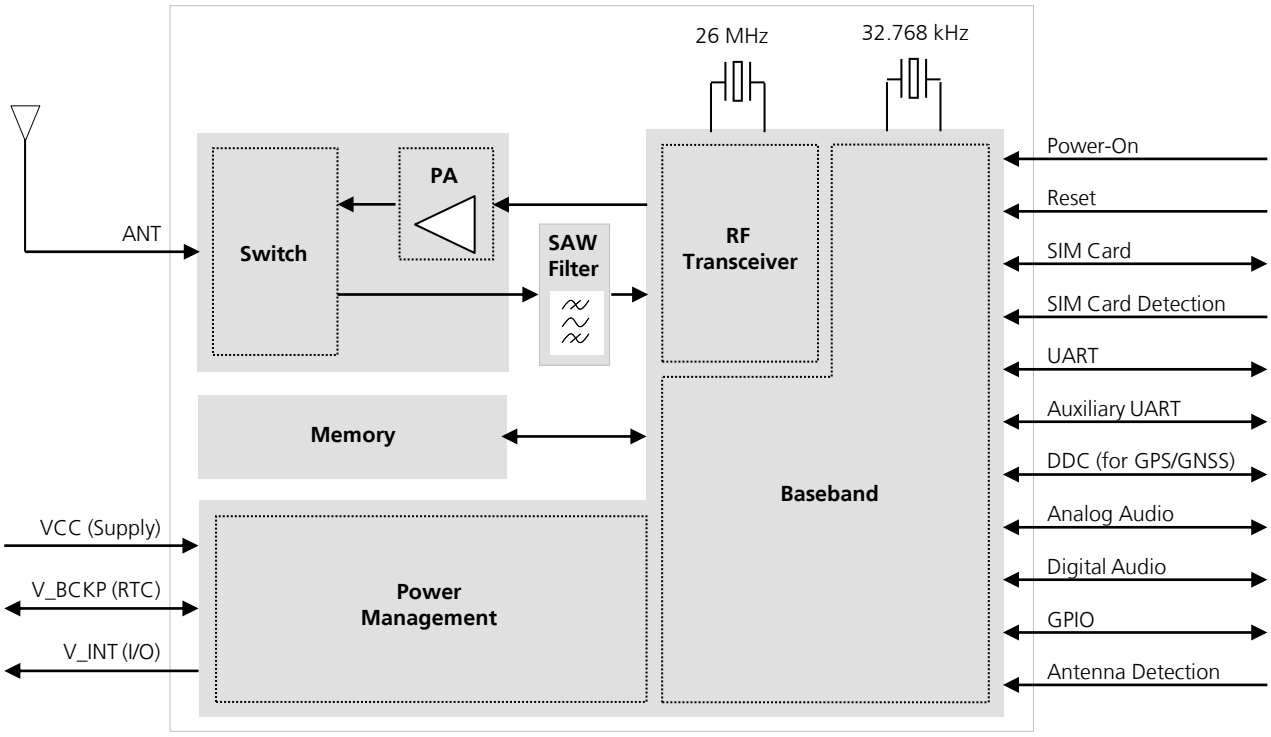


Figure 2: SARA-G350 modules block diagram

1.2.1 Internal blocks

SARA-G3 modules consist of the following internal sections: RF, Baseband and Power Management.

RF section

The RF section is composed of the following main elements:

- RF transceiver performing modulation, up-conversion of the baseband I/Q signals, down-conversion and demodulation of the RF received signals. The RF transceiver includes:
  - Constant gain direct conversion receiver with integrated LNAs
  - Highly linear RF quadrature GMSK demodulator
  - Digital Sigma-Delta transmitter GMSK modulator
  - Fractional-N Sigma-Delta RF synthesizer
  - 3.8 GHz VCO
  - Digital controlled crystal oscillator
- Transmit module, which amplifies the signals modulated by the RF transceiver and connects the single antenna input/output pin (**ANT**) of the module to the suitable RX/TX path, via its integrated parts:
  - Power amplifier
  - Antenna switch
- RX diplexer SAW (band pass) filters
- 26 MHz crystal, connected to the digital controlled crystal oscillator to perform the clock reference in active-mode or connected-mode

Baseband and Power Management section

The Baseband and Power Management section is composed of the following main elements:

- Baseband processor, a mixed signal ASIC which integrates:
  - Microprocessor for controller functions
  - DSP core for GSM/GPRS Layer 1 and audio processing
  - Dedicated peripheral blocks for parallel control of the digital interfaces
  - Audio analog front-end
- Memory system in a multi-chip package integrating two devices:
  - NOR flash non-volatile memory
  - PSRAM volatile memory
- Voltage regulators to derive all the system supply voltages from the module supply **VCC**

SARA-G350 modules are provided with an internal 32.768 kHz crystal connected to the oscillator of the RTC (Real Time Clock) block that gives the RTC clock reference needed to provide the RTC functions as well as to reach the low power idle-mode (with power saving configuration enabled by the AT+UPSV command).

SARA-G300 and SARA-G310 modules are not provided with internal 32.768 kHz crystal: an external 32 kHz signal must be provided at the **EXT32K** input pin of the modules to give the RTC clock reference and to provide the RTC functions as well as to reach the low power idle-mode (with power saving configuration enabled by the AT+UPSV command).

1.3 Pin-out

Table 3 lists the pin-out of the SARA-G3 modules, with pins grouped by function.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
Power	**VCC**	All	51, 52, 53	I	Module supply input	**VCC** pins are internally connected each other. **VCC** supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description and requirements for the **VCC** module supply. See section 2.1.1 for external circuit design-in.
	GND	All	1, 3, 5, 14, 20-22, 30, 32, 43, 50, 54, 55, 57-61, 63-96	N/A	Ground	**GND** pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.1.1 for external circuit design-in.
	V_BCKP	All	2	I/O	Real Time Clock supply input/output	**V_BCKP** = 2.3 V (typical) generated by internal regulator when valid **VCC** supply is present. See section 1.5.2 for functional description. See section 2.1.2 for external circuit design-in.
	V_INT	All	4	O	Digital Interfaces supply output	**V_INT** = 1.8 V (typical) generated by internal regulator when the module is switched on. See section 1.5.3 for functional description. See section 2.1.3 for external circuit design-in.
System	**PWR_ON**	All	15	I	Power-on input	High input impedance: input voltage level has to be properly fixed, e.g. adding external pull-up. See section 1.6.1 for functional description. See section 2.2.1 for external circuit design-in.
	RESET_N	All	18	I	External reset input	A series Schottky diode is integrated in the module as protection, and then an internal 10 kΩ pull-up resistor to **V_INT** is provided. See section 1.6.3 for functional description. See section 2.2.2 for external circuit design-in.
	EXT32K	SARA-G300 SARA-G310	31	I	32 kHz input	Input for RTC reference clock, needed to enter the low power idle-mode and provide RTC functions. See section 1.6.4 for functional description. See section 2.2.3 for external circuit design-in.
Antenna	**ANT**	All	56	I/O	RF input/output for antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for functional description and requirements for the antenna RF interface. See section 2.3 for external circuit design-in.
	ANT_DET	SARA-G350	62	I	Input for antenna detection	ADC input for antenna detection function. See section 1.7.1 for functional description. See section 2.3.2 for external circuit design-in.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
SIM	**VSIM**	All	41	O	SIM supply output	**VSIM** = 1.80 V typ. or 2.85 V typ. automatically generated according to the connected SIM type. See section 1.8 for functional description. See section 2.4 for external circuit design-in.
	SIM_IO	All	39	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM Internal 4.7 kΩ pull-up to **VSIM**. See section 1.8 for functional description. See section 2.4 for external circuit design-in.
	SIM_CLK	All	38	O	SIM clock	3.25 MHz clock output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.4 for external circuit design-in.
	SIM_RST	All	37	O	SIM reset	Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.4 for external circuit design-in.
	SIM_DET	All	42	I	SIM detection	1.8 V input for SIM presence detection function. See section 1.8.2 for functional description. See section 2.4 for external circuit design-in.
UART	**RXD**	All	13	O	UART data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, for AT command, Data communication, FOAT. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.
	TXD	All	12	I	UART data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, for AT command, Data communication, FOAT. Internal active pull-up to **V_INT**. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.
	CTS	All	11	O	UART clear to send output	1.8 V output, Circuit 106 (CTS) in ITU-T V.24, for AT command, Data communication, FOAT. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.
	RTS	All	10	I	UART ready to send input	1.8 V input, Circuit 105 (RTS) in ITU-T V.24, for AT command, Data communication, FOAT. Internal active pull-up to **V_INT**. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.
	DSR	All	6	O	UART data set ready output	1.8 V output, Circuit 107 (DSR) in ITU-T V.24, for AT command, Data communication, FOAT. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.
	RI	All	7	O	UART ring indicator output	1.8 V output, Circuit 125 (RI) in ITU-T V.24, for AT command, Data communication, FOAT. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.
	DTR	All	9	I	UART data terminal ready input	1.8 V input, Circuit 108/2 (DTR) in ITU-T V.24, for AT command, Data communication, FOAT. Internal active pull-up to **V_INT**. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.
	DCD	All	8	O	UART data carrier detect output	1.8 V input, Circuit 109 (DCD) in ITU-T V.24, for AT command, Data communication, FOAT. See section 1.9.1 for functional description. See section 2.5.1 for external circuit design-in.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
Auxiliary UART	**RXD_AUX**	All	28	O	Auxiliary UART data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, for FW upgrade and trace log capture. Access by external test-point is recommended. See section 1.9.2 for functional description. See section 2.5.2 for external circuit design-in.
	TXD_AUX	All	29	I	Auxiliary UART data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, for FW upgrade and trace log capture. Access by external test-point is recommended. Internal active pull-up to **V_INT**. See section 1.9.2 for functional description. See section 2.5.2 for external circuit design-in.
DDC	**SCL**	SARA-G350	27	O	I^2C bus clock line	1.8 V open drain, for the communication with u-blox positioning modules and chips. External pull-up required. See section 1.9.3 for functional description. See section 2.5.3 for external circuit design-in.
	SDA	SARA-G350	26	I/O	I^2C bus data line	1.8 V open drain, for the communication with u-blox positioning modules and chips. External pull-up required. See section 1.9.3 for functional description. See section 2.5.3 for external circuit design-in.
Analog Audio	**MIC_BIAS**	SARA-G350	46	O	Microphone supply output	Supply output (2.2 V typ) for external microphone. See section 1.10.1 for functional description. See section 2.6.1 for external circuit design-in.
	MIC_GND	SARA-G350	47	I	Microphone analog reference	Local ground for the external microphone (reference for the analog audio uplink path). See section 1.10.1 for functional description. See section 2.6.1 for external circuit design-in.
	MIC_N	SARA-G350	48	I	Differential analog audio input (negative)	Differential analog audio signal input (negative) shared for all the analog uplink path modes: handset, headset, hands-free mode. No internal DC blocking capacitor. See section 1.10.1 for functional description. See section 2.6.1 for external circuit design-in.
	MIC_P	SARA-G350	49	I	Differential analog audio input (positive)	Differential analog audio signal input (positive) shared for all the analog uplink path modes: handset, headset, hands-free mode. No internal DC blocking capacitor. See section 1.10.1 for functional description. See section 2.6.1 for external circuit design-in.
	SPK_P	SARA-G350	44	O	Differential analog audio output (positive)	Differential analog audio signal output (positive) shared for all the analog downlink path modes: earpiece, headset and loudspeaker mode. See section 1.10.1 for functional description. See section 2.6.1 for external circuit design-in.
	SPK_N	SARA-G350	45	O	Differential analog audio output (negative)	Differential analog audio signal output (negative) shared for all the analog downlink path modes: earpiece, headset and loudspeaker mode. See section 1.10.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin Name	Module	Pin No	I/O	Description	Remarks
Digital Audio	**I2S_CLK**	SARA-G350	37	O	I^2S clock	1.8 V clock output for PCM / normal I^2S modes. See section 1.10.2 for functional description. See section 2.6.2 for external circuit design-in.
	I2S_RXD	SARA-G350	36	I	I^2S receive data	1.8 V data input for PCM / normal I^2S modes. Internal active pull-down to GND. See section 1.10.2 for functional description. See section 2.6.2 for external circuit design-in.
	I2S_TXD	SARA-G350	35	O	I^2S transmit data	1.8 V data output for PCM / normal I^2S modes. See section 1.10.2 for functional description. See section 2.6.2 for external circuit design-in.
	I2S_WA	SARA-G350	34	O	I^2S word alignment	1.8 V word al. output for PCM / normal I^2S modes See section 1.10.2 for functional description. See section 2.6.2 for external circuit design-in.
GPIO	**GPIO1**	SARA-G350	16	I/O	GPIO	1.8 V GPIO by default configured as pad disabled. See section 1.11 for functional description. See section 2.7 for external circuit design-in.
	GPIO2	SARA-G350	23	I/O	GPIO	1.8 V GPIO by default configured to provide the custom GPS supply enable function. See section 1.11 for functional description. See section 2.7 for external circuit design-in.
	GPIO3	SARA-G350	24	I/O	GPIO	1.8 V GPIO by default configured to provide the custom GPS data ready function. See section 1.11 for functional description. See section 2.7 for external circuit design-in.
	GPIO4	SARA-G350	25	I/O	GPIO	1.8 V GPIO by default configured to provide the custom GPS RTC sharing function. See section 1.11 for functional description. See section 2.7 for external circuit design-in.
Reserved	**RSVD**	All	33	N/A	RESERVED pin	This pin must be connected to ground. See section 2.8
	RSVD	All	17, 19	N/A	RESERVED pin	Leave unconnected. See section 2.8
	RSVD	SARA-G350	31	N/A	RESERVED pin	Internally not connected. Leave unconnected. See section 2.8
	RSVD	SARA-G300 SARA-G310	16, 23-27, 34-37	N/A	RESERVED pin	Pad disabled. Leave unconnected. See section 2.8
	RSVD	SARA-G300 SARA-G310	44-49, 62	N/A	RESERVED pin	Leave unconnected. See section 2.8

Table 3: SARA-G3 series modules pin definition, grouped by function

1.4 Operating modes

SARA-G3 modules have several operating modes. The operating modes are defined in Table 4 and described in details in Table 5, providing general guidelines for operation.

General Status	Operating Mode	Definition
Power-down	**Not-Powered Mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-Off Mode	**VCC** supply within operating range and module is switched off.
Normal Operation	**Idle-Mode**	Module processor core runs with 32 kHz reference, that is generated by: • The internal 32 kHz oscillator (SARA-G350) • The 32 kHz signal provided at the **EXT32K** pin (SARA-G300 and SARA-G310)
	Active-Mode	Module processor core runs with 26 MHz reference generated by the internal oscillator.
	Connected-Mode	Voice or data call enabled and processor core runs with 26 MHz reference.

Table 4: Module operating modes definition

Operating Mode	Description	Transition between operating modes
Not-Powered Mode	Module is switched off. Application interfaces are not accessible. Internal RTC timer only operates if a valid voltage is applied to **V_BCKP** pin (necessary for all SARA-G3 modules), and if a valid 32 kHz signal is provided to **EXT32K** pin (necessary only for SARA-G300 and SARA-G310 modules)	When **VCC** supply is removed, the module enters not-powered mode. When in not-powered mode, the module cannot be switched on by a low level on **PWR_ON** input or by a preset RTC alarm. When in not-powered mode, the module can be switched on applying **VCC** supply (refer to 2.2.1) so that the module switches from not-powered to active-mode.
Power-Off Mode	Module is switched off: normal shutdown by an appropriate power-off event (refer to 1.6.2). Application interfaces are not accessible. Only the internal RTC timer in operation. A valid 32 kHz signal must be provided to **EXT32K** pin of SARA-G300 and SARA-G310 modules to let RTC timer running that otherwise is in operation (this is not needed for the other SARA-G3 series modules).	When the module is switched off by an appropriate power-off event (refer to 1.6.2), the module enters power-off mode from active-mode. When in power-off mode, the module can be switched on by a low level on **PWR_ON** input or by a preset RTC alarm (refer to 2.2.1): module switches from power-off to active-mode. When **VCC** supply is removed, the module switches from power-off mode to not-powered mode.
Idle-Mode	The module is not ready to communicate with an external device by means of the application interfaces since configured to reduce power consumption. The module automatically enters idle-mode whenever possible if power saving is enabled by the AT+UPSV command (refer to u-blox AT Commands Manual [2]), reducing power consumption (refer to 1.5.1.3). The **CTS** output line indicates when the UART interface is disabled/enabled due to the module idle/active-mode according to power saving and hardware flow control settings (refer to 1.9.1.3, 1.9.1.4). Power saving configuration is not enabled by default: it can be enabled by the AT+UPSV command (see u-blox AT Commands Manual [2]). A valid 32 kHz signal must be provided to **EXT32K** pin of SARA-G300 and SARA-G310 modules to let idle-mode that otherwise cannot be reached (this is not needed for the other SARA-G3 series modules).	The module automatically switches from active-mode to idle-mode whenever possible if power saving is enabled (refer to sections 1.5.1.3, 1.9.1.4 and to the u-blox AT Commands Manual [2], AT+UPSV). The module wakes up from idle-mode to active-mode in the following events: • Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (refer to 1.5.1.3, 1.9.1.4) • Automatic periodic enable of the UART interface to receive and send data, if the power saving AT command is set to 1 (refer to 1.9.1.4) • RTC alarm occurs (refer to u-blox AT Commands Manual [2], AT+CALA command) • Data received on UART interface (refer to 1.9.1.4) • **RTS** input line set to the ON state by the DTE if hardware flow control has been disabled by AT&K3 and the power saving AT command is set to 2 (refer to 1.9.1.4) • GPS data ready: when the **GPIO3** pin is informed by the connected u-blox GPS/GNSS receiver that it is ready to send data via the DDC (I^2C) interface (refer to 1.11, 1.9.3)

Operating Mode	Description	Transition between operating modes
Active-Mode	The module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by the AT+UPSV command (refer to sections 1.5.1.3, 1.9.1.4 and to the u-blox AT Commands Manual [2]).	When the module is switched on by an appropriate power-on event (refer to 2.2.1), the module enters active-mode from not-powered or power-off mode. If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from active to idle-mode whenever possible and the module wakes up from idle to active-mode in the events listed above (refer to idle to active transition description). When a voice call or a data call is initiated, the module switches from active-mode to connected-mode.
Connected-Mode	A voice call or a data call is in progress. The module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by the AT+UPSV command (see sections 1.5.1.3, 1.9.1.4 and the u-blox AT Commands Manual [2]).	When a voice call or a data call is initiated, the module enters connected-mode from active-mode. When a voice call or a data call is terminated, the module returns to the active-mode.

Table 5: Module operating modes description

Figure 3 describes the transition between the different operating modes.

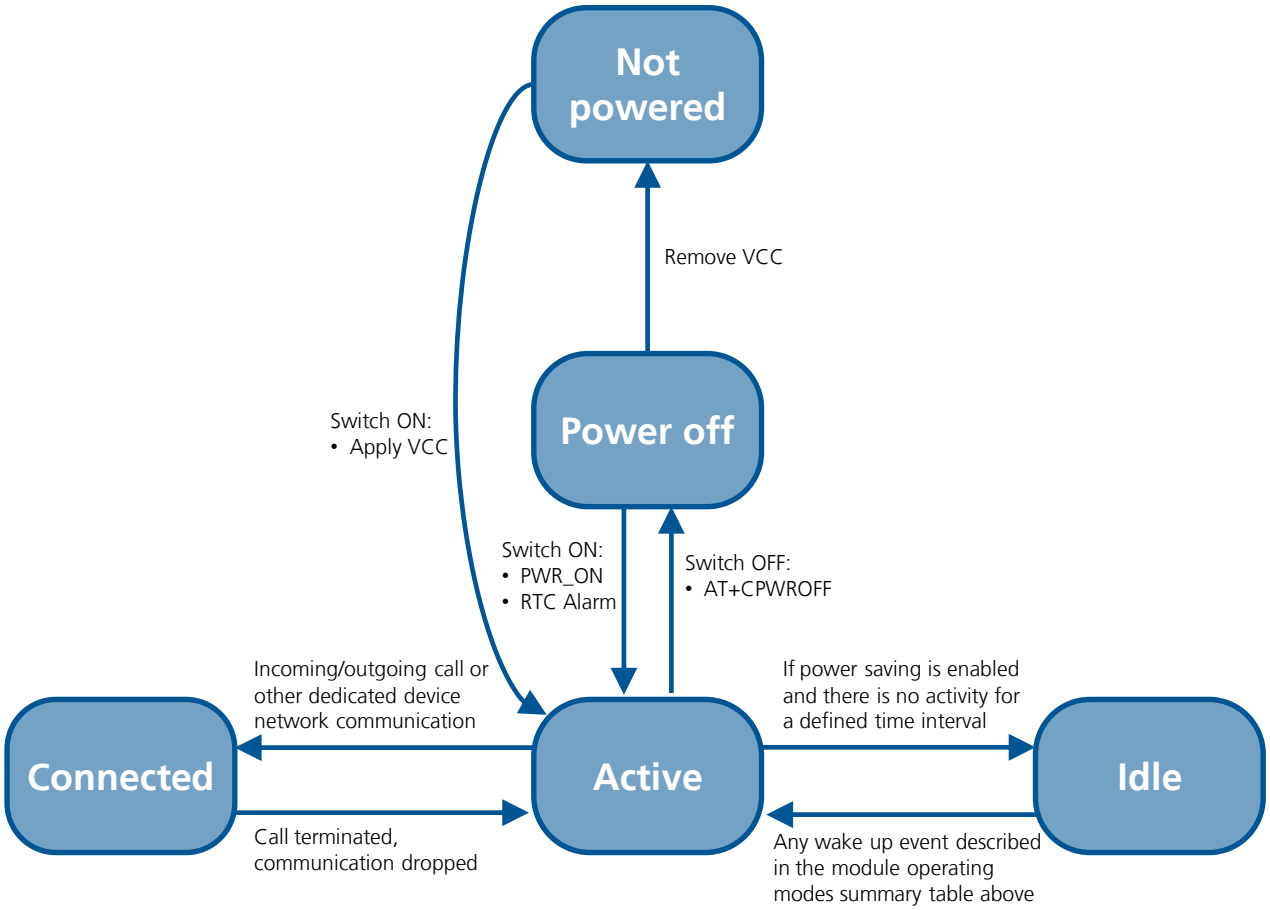


Figure 3: Operating modes transition

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

SARA-G3 modules must be supplied via the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, including **V_BCKP** Real Time Clock supply, **V_INT** digital interfaces supply and **VSIM** SIM card supply.

During operation, the current drawn by the SARA-G3 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the high peak of current consumption during GSM transmitting bursts at maximum power level in connected-mode (as described in the chapter 1.5.1.2), to the low current consumption during low power idle-mode with power saving enabled (as described in the chapter 1.5.1.3).

1.5.1.1 VCC supply requirements

Table 6 summarizes the requirements for the **VCC** module supply. Refer to chapter 2.1.1 for all the suggestions to properly design a **VCC** supply circuit compliant to the requirements listed in Table 6.

The VCC supply circuit affects the RF compliance of the device integrating SARA-G3 series module with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the VCC requirements summarized in the Table 6 are fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.35 V min. / 4.50 V max.	The module cannot be switched on if **VCC** voltage value is below the normal operating range minimum limit. Ensure that the input voltage at **VCC** pins is above the minimum limit of the normal operating range for at least more than 3 s after the module switch-on.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.00 V min. / 4.50 V max.	The module may switch off when **VCC** voltage drops below the extended operating range minimum limit. Operation above extended operating range maximum limit is not recommended and exposure beyond it may affect device reliability.
VCC average current	Considerably withstand maximum average current consumption value in connected-mode conditions specified in SARA-G3 series Data Sheet [1].	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and **VCC** voltage. Chapter 1.5.1.2 describes connected-mode current.
VCC peak current	Withstand the maximum peak current consumption specified in the SARA-G3 series Data Sheet [1].	The specified maximum peak of current consumption occurs during GSM single transmit slot in 850/900 MHz connected-mode, in case of mismatched antenna. Chapter 1.5.1.2 describes connected-mode current.
VCC voltage drop during Tx slots	Lower than 400 mV	**VCC** voltage drop values greater than recommended during 2G TDMA transmission slots directly affect the RF compliance with applicable certification schemes. Figure 5 describes **VCC** voltage drop during Tx slots.
VCC voltage ripple during Tx slots	Lower than 30 mVpp if $f_{ripple} \leq 200$ kHz Lower than 10 mVpp if 200 kHz < $f_{ripple} \leq 400$ kHz Lower than 2 mVpp if $f_{ripple} > 400$ kHz	**VCC** voltage ripple values higher than recommended during 2G/3G transmission directly affect the RF compliance with applicable certification schemes. Figure 5 describes **VCC** voltage ripple during Tx slots.

Item	Requirement	Remark
VCC under/over-shoot at start/end of Tx slots	Absent or at least minimized	**VCC** under/over-shoot higher than recommended at the start/end of 2G TDMA transmission slots directly affect the RF compliance with applicable certification schemes Figure 5 describes **VCC** voltage under/over-shoot at the start/end of Tx slots

Table 6: Summary of VCC supply requirements

1.5.1.2 VCC current consumption in connected-mode

When a GSM call is established, the **VCC** consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. If the module is transmitting in GSM talk mode in the 850 or 900 MHz bands, at the maximum RF power control level (approximately 2 W or 33 dBm in the allocated transmit slot/burst) the current consumption can reach up to 1900 mA (with a highly unmatched antenna) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access). If the module is in GSM connected-mode in the 1800 or 1900 MHz bands, the current consumption figures are lower than the one in the 850 or 900 MHz bands, due to 3GPP transmitter output power specifications (refer to SARA-G3 series Data Sheet [1]).

During a GSM call, current consumption is in the order of 60-130 mA in receiving or in monitor bursts and is about 10-40 mA in the inactive unused bursts (low current period). The more relevant contribution to determine the average current consumption is set by the transmitted power in the transmit slot.

Figure 4 shows an example of the module current consumption profile versus time in GSM talk mode.

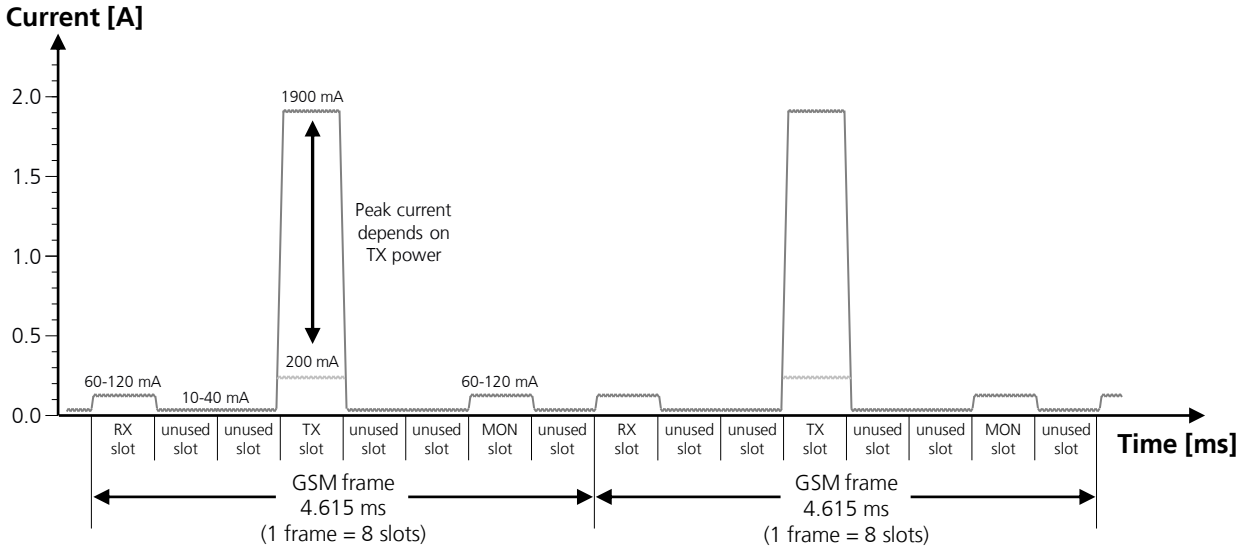


Figure 4: VCC current consumption profile versus time during a GSM call (1 TX slot, 1 RX slot)

Figure 5 illustrates **VCC** voltage profile versus time during a GSM call, according to the relative **VCC** current consumption profile described in the Figure 4.

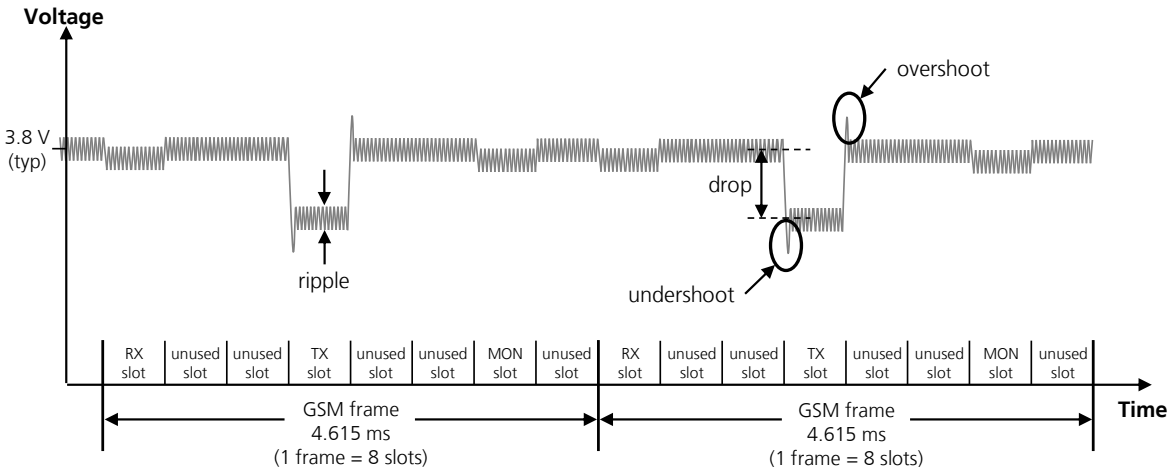


Figure 5: Description of the VCC voltage profile versus time during a GSM call

When a GPRS connection is established, more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions, which set the peak current consumption, but following the GPRS specifications the maximum transmitted RF power is reduced if more than one slot is used to transmit, so the maximum peak of current is not as high as can be in case of a GSM call.

If the module transmits in GPRS multi-slot class 10, in the 850 or 900 MHz bands, at the maximum power control level, the consumption can reach up to 1600 mA (with highly unmatched antenna). This happens for 1.154 ms (width of the 2 Tx slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/4 duty cycle, according to GSM TDMA. If the module is in GPRS connected-mode in 1800 or 1900 MHz bands, consumption figures are lower than in the 850 or 900 MHz band, due to 3GPP Tx power specifications.

Figure 6 reports the current consumption profiles in GPRS connected-mode, in the 850 or 900 MHz bands, with 2 slots used to transmit and 1 slot used to receive.

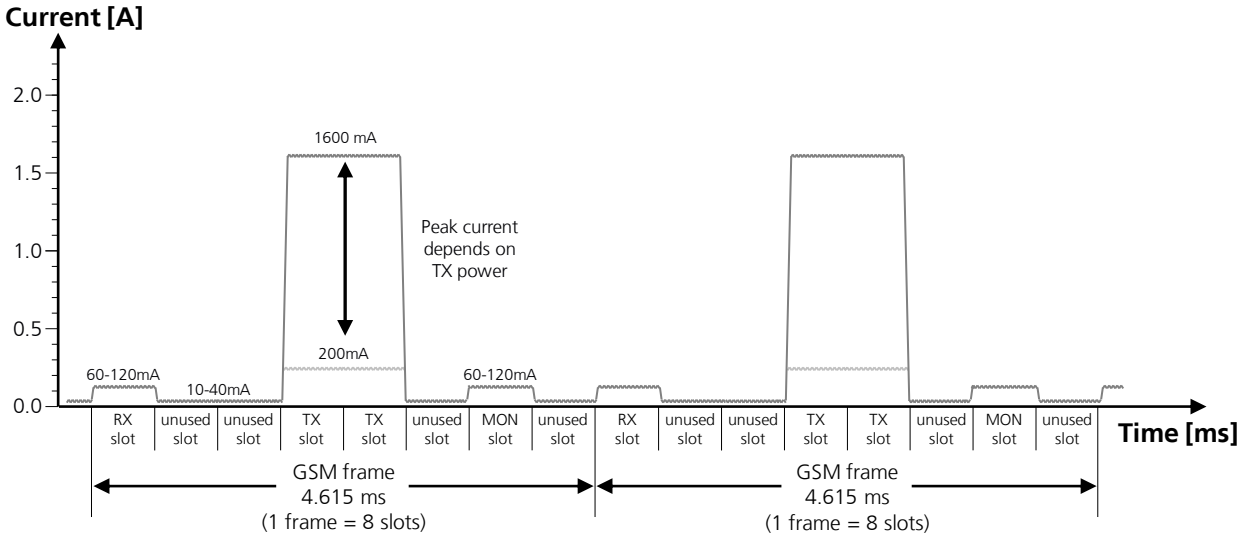


Figure 6: VCC current consumption profile versus time during a GPRS connection (2 TX slots, 1 RX slot)

1.5.1.3 VCC current consumption in cyclic idle/active-mode (power saving enabled)

The power saving configuration is by default disabled, but it can be enabled using the appropriate AT command (refer to u-blox AT Commands Manual [2], AT+UPSV command). When power saving is enabled, the module automatically enters idle-mode whenever possible, reducing current consumption.

During idle-mode, the module processor runs with 32 kHz reference clock frequency. For SARA-G350 modules, the internal oscillator automatically generates the 32 kHz clock. For SARA-G300 and SARA-G310 modules, a valid 32 kHz signal must be provided to the **EXT32K** input pin of the module to let idle-mode, that otherwise cannot be reached (this is not needed for the other SARA-G3 series modules).

When power saving is enabled, the module is registered or attached to a network and a voice or data call is not enabled, the module automatically enters idle-mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to GSM system requirements. When the module monitors the paging channel, it wakes up to active-mode, to enable the reception of paging block. In between, the module switches to idle-mode. This is known as GSM discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 26 MHz used in active-mode.

The time period between two paging block receptions is defined by the network. This is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell.

The time interval between two paging block receptions can be from 470.76 ms (DRX = 2, i.e. width of 2 GSM multiframes = 2 x 51 GSM frames = 2 x 51 x 4.615 ms) up to 2118.42 ms (DRX = 9, i.e. width of 9 GSM multiframes = 9 x 51 frames = 9 x 51 x 4.615 ms).

Figure 7 shows an example of a module current consumption profile: the module is registered with the network, automatically enters idle-mode and periodically wakes up to active-mode to monitor the paging channel for paging block reception.

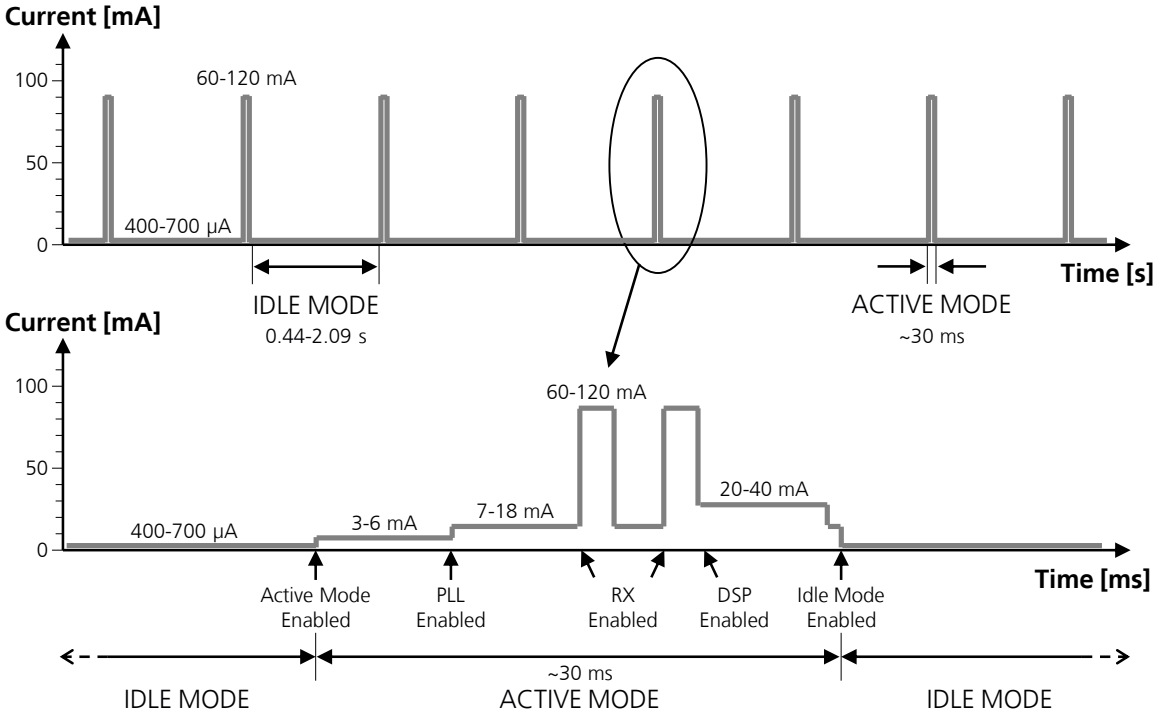


Figure 7: Description of VCC current consumption profile versus time when the module is registered the network: the module is in idle-mode and periodically wakes up to active-mode to monitor the paging channel for paging block reception

1.5.1.4 VCC current consumption in fixed active-mode (power saving disabled)

Power saving configuration is by default disabled, or it can be disabled using the appropriate AT command (refer to u-blox AT Commands Manual [2], AT+UPSV command). When power saving is disabled, the module does not automatically enter idle-mode whenever possible: the module remains in active-mode.

The module processor core is activated during active-mode, and the 26 MHz reference clock frequency is used.

Figure 8 shows an example of the module current consumption profile when power saving is disabled: the module is registered with the network, active-mode is maintained, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception.

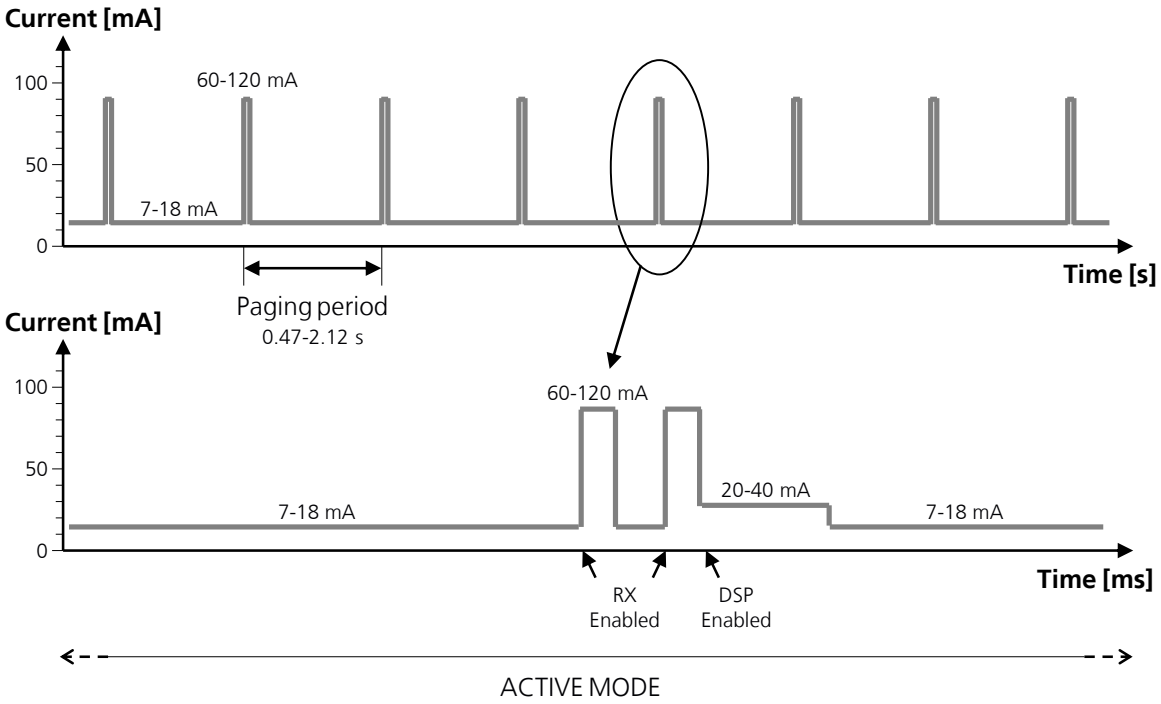


Figure 8: Description of the VCC current consumption profile versus time when power saving is disabled: the active-mode is always held, and the receiver and the DSP are periodically activated to monitor the paging channel for paging block reception

1.5.2 RTC supply input/output (V_BCKP)

The **V_BCKP** pin of SARA-G3 modules connects the supply for the Real Time Clock (RTC) and Power-On internal logic. This supply domain is internally generated by a linear LDO regulator integrated in the Power Management Unit, as described in Figure 9. The output of this linear regulator is always enabled when the main voltage supply provided to the module through the **VCC** pins is within the valid operating range, with the module switched off or switched on.

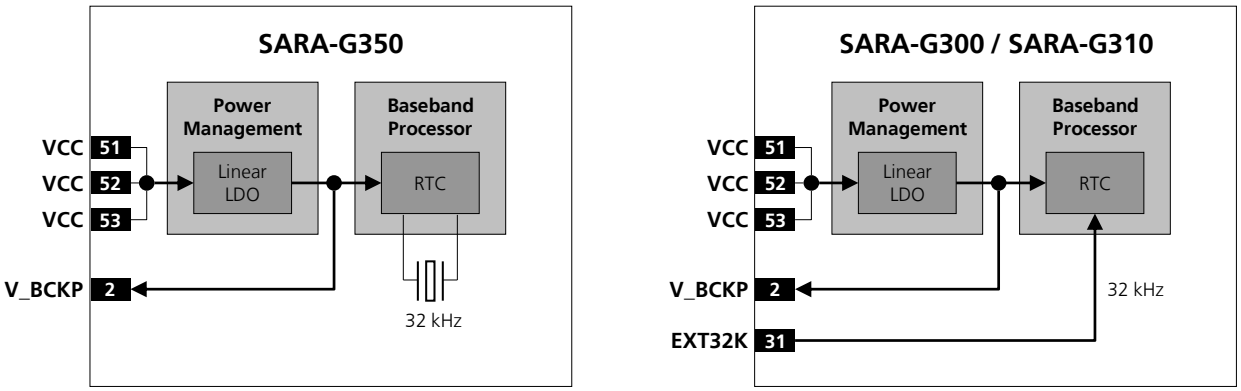


Figure 9: SARA-G3 series RTC supply input/output (V_BCKP) and 32 kHz RTC timing reference clock simplified block diagram

The RTC provides the module time reference (date and time), also in power-off mode, when the **V_BCKP** voltage is within its valid range (specified in the "Input characteristics of Supply/Power pins" table in SARA-G3 series Data Sheet [1]). The RTC timing is normally used to set the wake-up interval during idle-mode periods between network paging, but is able to provide programmable alarm functions by means of the 32.768 kHz clock provided by the internal oscillator on SARA-G350 modules or provided by a valid 32 kHz external signal present at the **EXT32K** input pin of SARA-G300 and SARA-G310 modules.

The RTC can be supplied from an external back-up battery through the **V_BCKP**, when the main voltage supply is not provided to the module through **VCC**. This lets the time reference (date and time) run until the **V_BCKP** voltage is within its valid range, even when the main supply is not provided to the module.

The RTC oscillator does not necessarily stop operation (i.e. the RTC counting does not necessarily stop) when **V_BCKP** voltage value drops below the specified operating range minimum limit (1.00 V): the RTC value read after a system restart could be not reliable as explained in the following Table 7.

V_BCKP voltage value	RTC value reliability	Notes
1.00 V < **V_BCKP** < 2.40 V	RTC oscillator does not stop operation RTC value read after a restart of the system is reliable	**V_BCKP** within operating range
0.05 V < **V_BCKP** < 1.00 V	RTC oscillator does not necessarily stop operation RTC value read after a restart of the system is not reliable	**V_BCKP** below operating range
0.00 V < **V_BCKP** < 0.05 V	RTC oscillator stops operation RTC value read after a restart of the system is reliable	**V_BCKP** below operating range

Table 7: RTC value reliability as function of V_BCKP voltage value

Consider that the module cannot switch on if a valid voltage is not present on **VCC** even when the RTC is supplied through **V_BCKP** (meaning that **VCC** is mandatory to switch on the module).

The RTC has very low power consumption, but is highly temperature dependent. For example at 25 °C, with the **V_BCKP** voltage equal to the typical output value, the power consumption is approximately 2 µA (refer to the

"Input characteristics of Supply/Power pins" table in the SARA-G3 series Data Sheet [1] for the detailed specification), whereas at 70 °C and an equal voltage the power consumption increases to 5-10 µA.

If **V_BCKP** is left unconnected and the module main voltage supply is removed from **VCC**, the RTC is supplied from the bypass capacitor mounted inside the module. However, this capacitor is not able to provide a long buffering time: within few milliseconds the voltage on **V_BCKP** will go below the valid range (1 V min). This has no impact on wireless connectivity, as all the module functionalities do not rely on date and time setting.

1.5.3 Interfaces supply output (V_INT)

The same 1.8 V voltage domain used internally to supply the digital interfaces of SARA-G3 modules is also available on the **V_INT** supply output pin, as described in Figure 10.

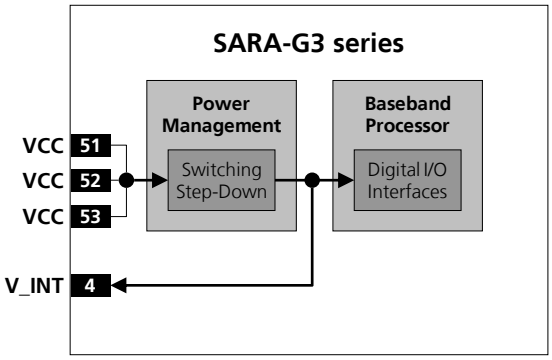


Figure 10: SARA-G3 series interfaces supply output (V_INT) simplified block diagram

The internal regulator that generates the **V_INT** supply is a switching step-down converter that is directly supplied from **VCC**. The voltage regulator output is set to 1.8 V (typical) when the module is switched on and it is disabled when the module is switched off.

The switching regulator operates in Pulse Width Modulation (PWM) for greater efficiency at high output loads when the module is in active-mode or in connected-mode. When the module is in low power idle-mode between paging periods and with power saving configuration enabled by the appropriate AT command, it automatically switches to Pulse Frequency Modulation (PFM) for greater efficiency at low output loads. Refer to the u-blox AT Commands Manual [2], +UPSV command.

1.6 System function interfaces

1.6.1 Module power-on

The power-on sequence of SARA-G3 series modules is initiated in one of these ways:

- Rising edge on the **VCC** pin to a valid voltage as module supply (i.e. applying module supply)
- Low level on the **PWR_ON** pin (normally high with external pull-up) for an appropriate time period
- RTC alarm (i.e. pre-programmed scheduled time by AT+CALA command)

1.6.1.1 Rising edge on VCC

When a SARA-G3 module is in the not-powered mode, it can be switched on by applying the **VCC** supply.

The module is switched on when the voltage rises up to the **VCC** normal operating range minimum limit (3.35 V) starting from a voltage value lower than 2.25 V, and with a proper voltage slope: the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 4 ms to switch on the module. When the **VCC** voltage is stabilized at its nominal value within the normal operating range, the module can be switched on by a low level on **PWR_ON** pin (see section 1.6.1.2) or by RTC alarm (see section 1.6.1.3).

If the **PWR_ON** input pin is held low during the **VCC** apply phase, the SARA-G3 module switches on when voltage rises up to the **VCC** normal operating range minimum limit (3.35 V).

1.6.1.2 Low level on PWR_ON

When a SARA-G3 module is in the power-off mode (i.e. switched off with valid **VCC** supply maintained), the module can be switched on by forcing a low level on the **PWR_ON** input pin at least for 5 ms.

The electrical characteristics of the **PWR_ON** input pin are different from the other digital I/O interfaces. The input voltage thresholds are slightly different since the **PWR_ON** input pin is tolerant of voltages up to the module supply level. The detailed electrical characteristics are described in SARA-G3 series Data Sheet [1].

There is no internal pull-up resistor on the **PWR_ON** pin: the pin has high input impedance and is weakly pulled to the high level by the internal circuit. Therefore the external circuit must be able to hold the high logic level stable, e.g. providing an external pull-up resistor (for further design-in guidelines refer to chapter 2.2.1).

1.6.1.3 RTC alarm

When a SARA-G3 module is in the power-off mode (i.e. switched off with valid **VCC** supply maintained) and the RTC timing (32 kHz reference clock) is available, the module can be switched on by an RTC alarm previously programmed by AT command at a scheduled time (refer to the u-blox AT Commands Manual [2], AT+CALA command). The internal RTC block system will then initiate the module boot sequence by instructing the Power Management Unit to turn on power. Also included in this setup is an interrupt signal from the RTC block to indicate to the baseband processor that an RTC event has occurred.

The RTC timing is generated by the 32 kHz reference clock provided by the internal oscillator on SARA-G350 modules. A valid 32 kHz external signal must be provided at the **EXT32K** input pin of the SARA-G300 and SARA-G310 modules to enable RTC timing, otherwise the switch-on of SARA-G300 and SARA-G310 modules by means of a pre-programmed RTC alarm is not possible (refer to the chapter 1.6.4).

1.6.1.4 Additional considerations

The module is switched on when the **VCC** voltage rises to the normal operating range (i.e. applying module supply): the first time that the module is used, it is switched on in this way. SARA-G3 modules can be switched off by means of the AT+CPWROFF command, entering power-off mode. In this state, the digital input-output pads of the baseband chipset (i.e. all the digital pins of the module) are locked in tri-state (i.e. floating). The power down tri-state function isolates the module pins from the environment, when no proper operation of the outputs can be guaranteed.

The module can be switched on from power-off mode by forcing a proper start-up event (e.g. **PWR_ON** low). After the detection of a start-up event, all the module digital pins are held in tri-state until all the internal LDO voltage regulators are turned on in a defined power-on sequence. Then, as described in Figure 11, the baseband core is still held in reset state for a time interval: the internal reset signal (which is not available on a module pin) is still low and all the digital pins of the module are held in reset state. The reset state of all the digital pins is reported in the pin description table of SARA-G3 Series Data Sheet [1]. When the internal signal is released, the configuration of the module interfaces starts: during this phase any digital pin is set in a proper sequence from the reset state to the default operational configuration. Finally, the module is fully ready to operate when all interfaces are configured.

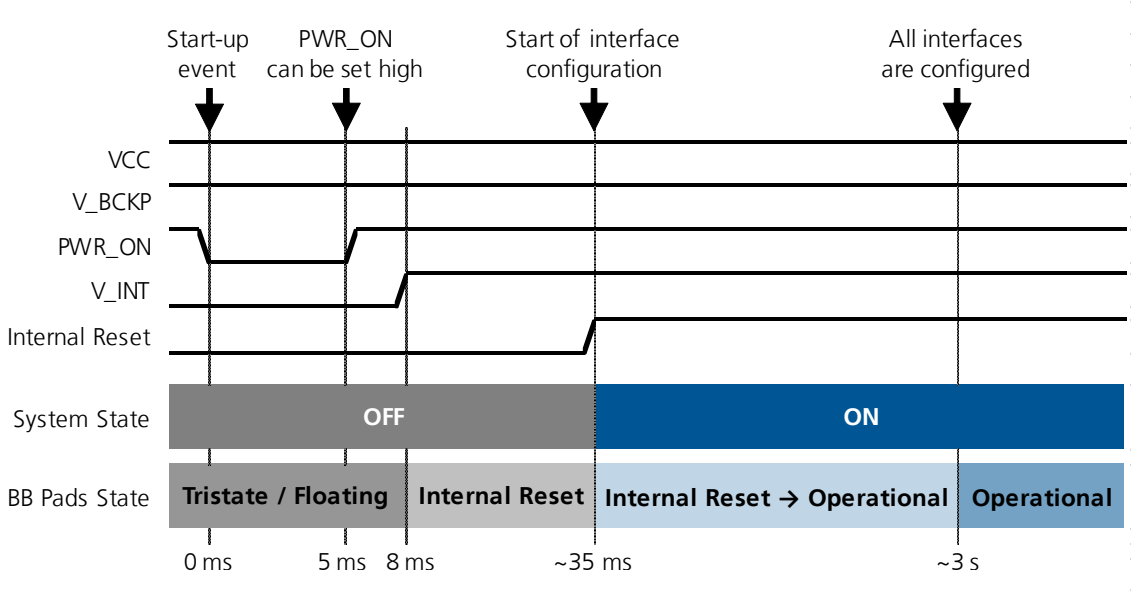


Figure 11: SARA-G3 series power-on sequence description

The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the start of the SARA-G3 series power-on sequence.

1.6.2 Module power-off

The correct way to switch off SARA-G3 modules is by means of +CPWROFF AT command (more details in u-blox AT Commands Manual [2]): in this way the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

An under-voltage shutdown occurs on SARA-G3 modules when the **VCC** supply is removed, but in this case the current parameter settings are not saved in the module's non-volatile memory and a proper network detach cannot be performed.

An over-temperature or an under-temperature shutdown occurs when the temperature measured within the wireless module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is activated and configured by the dedicated AT+USTS command. Refer to chapter 1.13.8 and to the u-blox AT Commands Manual [2] for more details.

Figure 12 describes the power-off sequence by means of +CPWROFF AT command. When the +CPWROFF AT command is sent, the module starts the switch-off routine replying OK on the AT interface. At the end of the switch-off routine, all digital pins are locked in tri-state by the module and all the internal LDO voltage regulators except the RTC supply (**V_BCKP**) are turned off in a defined power-off sequence. The module remains in power-off mode as long as a switch on event does not occur (i.e. applying a low level on the **PWR_ON** pin, or by a pre-programmed RTC alarm), and enters not-powered mode if the supply is removed from the **VCC** pin.

Current parameter settings are stored to the module's non-volatile memory and a network detach is performed before the OK reply from AT+CPWROFF command.

The duration of the switch-off routine phases can largely differ from the values reported in Figure 12, depending on the network settings and the concurrent activities of the module performing a network detach.

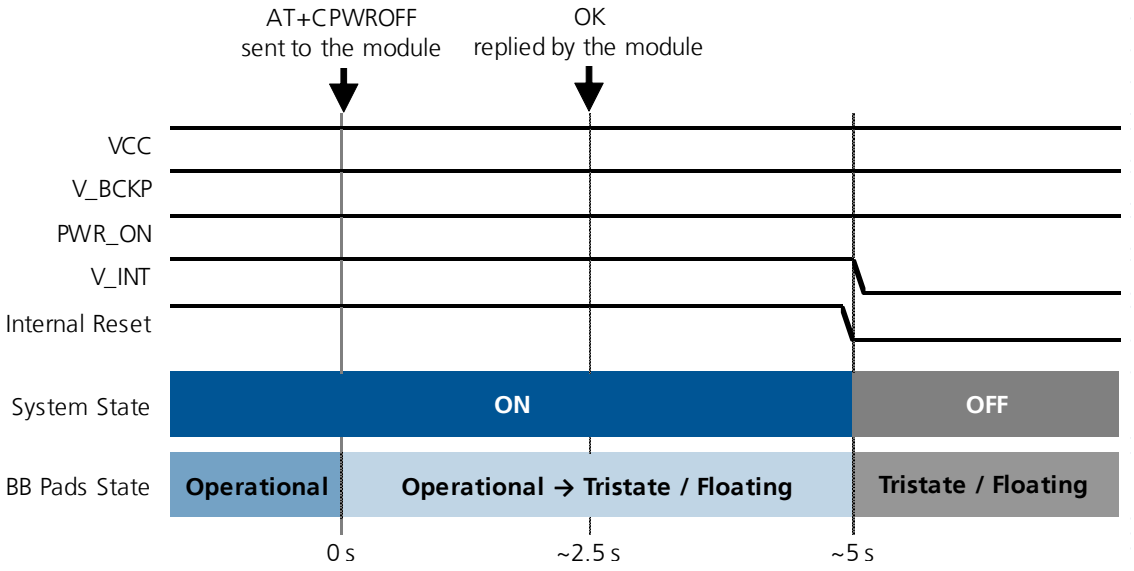


Figure 12: SARA-G3 series power-off sequence description

The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the end of the SARA-G3 series power-off sequence.

1.6.3 Module reset

A SARA-G3 module reset can be performed in one of two ways.

RESET_N input pin: Forces a low level on the **RESET_N** input pin, causing an "external" or "hardware" reset. This must be for at least 50 ms on SARA-G350 modules or 3000 ms on SARA-G300 and SARA-G310 modules. This causes an asynchronous reset of the module baseband processor, excluding the integrated Power Management Unit and the RTC internal block: the **V_INT** interfaces supply is enabled and each digital pin is set in its reset state, the **V_BCKP** supply and the RTC block are enabled. Forcing an "external" or "hardware" reset, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

AT+CFUN command (refer to the u-blox AT Commands Manual [2] for more details): This command causes an "internal" or "software" reset, which is an asynchronous reset of the module baseband processor. The electrical behavior is the same as that of the "external" or "hardware" reset, but in an "internal" or "software" reset the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

After either reset, when **RESET_N** is released from the low level, the module automatically starts its power-on sequence from the reset state.

The reset state of all digital pins is reported in the pin description table in SARA-G3 series Data Sheet [1].

The electrical characteristics of **RESET_N** are different from the other digital I/O interfaces: the **RESET_N** input pin is tolerant of voltages up to the module supply level due to the series Schottky diode mounted inside the module on the **RESET_N** pin. As described in Figure 13, the module has an internal pull-up resistor which pulls the line to the high logic level when the **RESET_N** pin is not forced low from the external. Detailed electrical characteristics are described in SARA-G3 series Data Sheet [1].

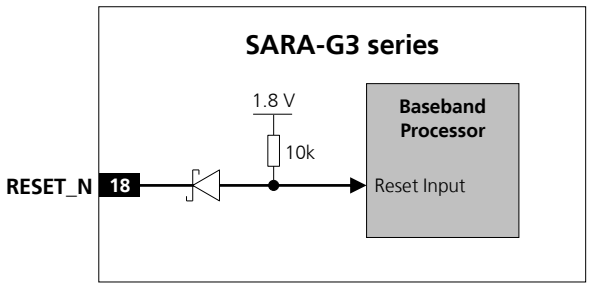


Figure 13: SARA-G3 series reset input (RESET_N) description

1.6.4 External 32 kHz signal input (EXT32K)

The external 32 kHz signal input pin (**EXT32K**) is available on SARA-G300 and SARA-G310 modules to provide the 32 kHz reference clock for the Real Time Clock (RTC) timing, used by the module processor when in the low power idle-mode.

Only if a valid 32 kHz external signal is provided at the **EXT32K** input pin, SARA-G300 and SARA-G310 modules can enter the low power idle-mode (with power saving configuration enabled by the AT+UPSV command) and can provide the RTC functions (as RTC timing by AT+CCLK command and RTC alarm by AT+CALA command).

The detailed electrical characteristics are described in SARA-G3 series Data Sheet [1].

The 32 kHz reference clock for the RTC timing is automatically generated by the internal oscillator provided on the SARA-G350 modules: the same pin (31) is a reserved (**RSVD**) pin internally not connected, since an external 32 kHz signal is not needed to enter the low power idle-mode and to provide the RTC functions.

1.7 Antenna interface

1.7.1 Antenna RF interface (ANT)

The **ANT** pin of SARA-G3 modules represents the RF input/output for transmission and reception of the GSM/GPRS RF signal. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line to allow proper RF transmission and reception in operating bands.

1.7.1.1 Antenna RF interface requirements

Table 8 summarizes the requirements for the antenna RF interface (**ANT**). Refer to section 2.3.1 for suggestions to properly design an antenna circuit compliant to these requirements.

The antenna circuit affects the RF compliance of the device integrating SARA-G3 series module with applicable required certification schemes. Compliance is guaranteed if the antenna RF interface (ANT) requirements summarized in Table 8 are fulfilled.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** pin.
Frequency Range	SARA-G350, SARA-G310: • 824..960 MHz (GSM 850, GSM 900) • 1710..1990 MHz (GSM 1800, GSM 1900) SARA-G300: • 880..960 MHz (GSM 900) • 1710..1880 MHz (GSM 1800)	The required frequency range of the antenna depends on the operating bands of the used SARA-G3 module and the used Mobile Network.
V.S.W.R **Return Loss**	< 2:1 recommended, < 3:1 acceptable S_{11} < -10 dB recommended, S_{11} < -6 dB acceptable	The impedance of the antenna termination must match as much as possible the 50 Ω impedance of the **ANT** pin over the operating frequency range.
Input Power	> 2 W peak	The antenna termination must withstand the maximum peak of power transmitted by SARA-G3 modules during a GSM single-slot call.
Gain	Below the levels reported in the chapter 4.2.2	The antenna gain must not exceed the herein specified value to comply with FCC radiation exposure limits.
Detection	Application board with antenna detection circuit	If antenna detection is required by the custom application, proper antenna detection circuit must be implemented on the application board as described in section 2.3.2.
	Antenna assembly with built-in diagnostic circuit	If antenna detection is required by the custom application, the external antenna assembly must be provided with proper diagnostic circuit as described in section 2.3.2.

Table 8: Summary of antenna RF interface (ANT) requirements

1.7.1 Antenna detection interface (ANT_DET)

☞ SARA-G300 and SARA-G310 modules do not support antenna detection interface (**ANT_DET**).

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. Refer to the u-blox AT Commands Manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (20 µA for 5.4 ms) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

Refer to the section 2.3.2 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM card interface

SARA-G3 modules provide high-speed SIM/ME interface including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported: activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The **VSIM** supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations.

The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM Card.

SIM Application Toolkit (R99) is supported only by SARA-G350 modules.

1.8.2 SIM card detection interface (SIM_DET)

The **SIM_DET** pin is configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin is configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if properly connected to the mechanical switch of a SIM card holder as described in the chapter 2.4:

- Low logic level at **SIM_DET** input pin is recognized as SIM card not present
- High logic level at **SIM_DET** input pin is recognized as SIM card present

The SIM card detection function provided by **SIM_DET** pin is an optional feature that can be implemented / used or not according to the application requirements.

For more details on SIM detection function refer to the u-blox AT Commands Manual [2], “simind” value of the <descr> parameter of the +CIND and +CMER commands.

1.9 Serial interfaces

SARA-G3 series modules provide the following serial communication interfaces:

- UART interface: 9-wire unbalanced 1.8 V asynchronous serial interface available for AT commands interface, Packet-Switched / Circuit-Switched Data communication, FW upgrades by means of the FOAT feature
- Auxiliary UART interface: 3-wire unbalanced 1.8 V asynchronous serial interface available only for the FW upgrade by means of the u-blox EasyFlash tool and for the Trace log capture (debug purpose)
- DDC interface: I^2C compatible 1.8 V interface available only for the communication with u-blox positioning chips and modules

1.9.1 Asynchronous serial interface (UART)

1.9.1.1 UART features

The UART interface is a 9-wire 1.8 V unbalanced asynchronous serial interface, and it is the only serial interface of the SARA-G3 modules available for an AT command interface and for Packet-Switched / Circuit-Switched Data communication.

The module firmware can be upgraded over the UART interface by means of the Firmware upgrade over AT (FOAT) feature only: for more details refer to section 1.13 and Firmware update application note [22].

UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation (more details available in ITU Recommendation [9]), with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state. For detailed electrical characteristics refer to SARA-G3 series Data Sheet [1].

SARA-G3 modules are designed to operate as a GSM/GPRS wireless modem, which represents the data circuit-terminating equipment (DCE) as described by the ITU-T V.24 Recommendation [9]. A customer application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ The signal names of the UART interface of the SARA-G3 modules conform to the ITU-T V.24 Recommendation [9]: e.g. **TXD** line represents the data transmitted by the DTE (application processor data output) and received by the DCE (module input).

The UART interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [10]
- AT commands according to 3GPP TS 27.005 [11]
- AT commands according to 3GPP TS 27.010 [12]
- u-blox AT commands

☞ For the complete list of supported AT commands and their syntax refer to the u-blox AT Commands Manual [2].

All flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see u-blox AT Commands Manual [2], &K, +IFC, \Q AT commands): hardware flow control (RTS/CTS), software flow control (XON/XOFF), or none flow control.

☞ Hardware flow control is enabled by default.

The following baud rates can be configured by AT command:

- 2400 b/s
- 4800 b/s
- 9600 b/s
- 19200 b/s
- 38400 b/s
- 57600 b/s
- 115200 b/s, default value when the autobauding is disabled

The following baud rates are available with autobauding only:

- 1200 b/s
- 230400 b/s

Autobauding is enabled by default.

The following frame formats can be configured by AT command:

- 8N1 (8 data bits, No parity, 1 stop bit), default frame configuration with fixed baud rate
- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 8N2 (8 data bits, No parity, 2 stop bits)
- 7E1 (7 data bits, even parity, 1 stop bit)
- 7O1 (7 data bits, odd parity, 1 stop bit)

Automatic frame recognition is supported and enabled by default in conjunction with the auto-bauding. When auto-bauding is active, the auto-framing is enabled overruling the frame format setting.

Figure 14 describes the 8N1 frame format, which is the default configuration with fixed baud rate.

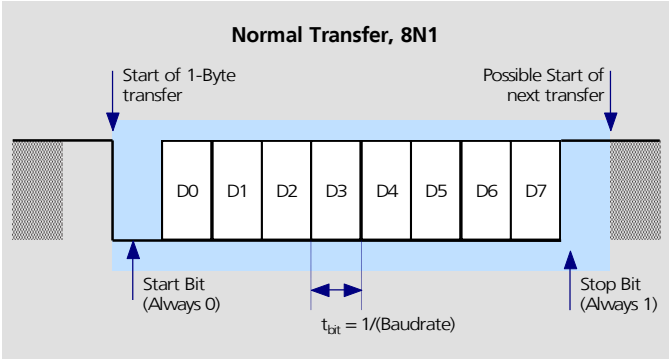


Figure 14: Description of UART default frame format (8N1) with fixed baud rate

1.9.1.2 UART AT interface configuration

The UART interface is the only AT command interface on SARA-G3 series modules. UART is configured as described in Table 9 (for information about further settings, refer to the u-blox AT Commands Manual [2]).

Interface	AT Settings	Comments
UART interface	AT interface: enabled	AT command interface is enabled by default on the UART physical interface
	AT+IPR=0	Automatic baud rate detection enabled by default
	AT+ICF=0	Automatic frame format recognition enabled by default
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode[5] and set OFF in command mode[5]
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command mode[5] and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
	MUX protocol: disabled	Multiplexing mode is disabled by default and it can be enabled by AT+CMUX command. The following virtual channels are defined for SARA-G350 modules: • Channel 0: control channel • Channel 1 – 5: AT commands / data connection • Channel 6: GPS tunneling The following virtual channels are defined for SARA-G300 and SARA-G310 modules: • Channel 0: control channel • Channel 1 – 2: AT commands / data connection

Table 9: Default UART AT interface configuration

1.9.1.3 UART signal behavior (AT commands interface case)

At the module switch-on, before the UART interface initialization (as described in the power-on sequence reported in Figure 11), each pin is first tri-stated and then is set to its relative internal reset state.[6] At the end of the boot sequence, the UART interface is initialized, the module is by default in active-mode, and the UART interface is enabled.

The configuration and the behavior of the UART signals after the boot sequence are described below. See section 1.4 for definition and description of module operating modes referred to in this section.

RXD signal behavior

The module data output line (**RXD**) is set by default to OFF state (high level) at UART initialization. The module holds **RXD** in OFF state until the module does not transmit some data.

TXD signal behavior

The module data input line (**TXD**) is set by default to OFF state (high level) at UART initialization. The **TXD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TXD** input.

[5] Refer to the u-blox AT Commands Manual [2] for the definition of the interface data mode, command mode and online command mode.
[6] See the pin description table in the SARA-G3 series Data Sheet [1].

CTS signal behavior

The module hardware flow control output (**CTS** line) is set to the ON state (low level) at UART initialization.

If the hardware flow control is enabled (for more details, refer to u-blox AT Commands Manual [2], AT&K, AT\Q, AT+IFC AT command) the **CTS** line indicates when the UART interface is enabled (data can be sent and received): the module drives the **CTS** line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE (refer to chapter 1.9.1.4 for the complete description).

If the hardware flow control is not enabled, the **CTS** line is always held in the ON state after UART initialization.

☞ If hardware flow control is enabled, then when the **CTS** line is ON the UART is enabled and the module is in active-mode. If the **CTS** line is OFF it does not necessarily mean that the module is in idle-mode, but only that the UART is not enabled (the module could be forced to stay in active-mode for other activities, e.g. network related).

☞ When the power saving configuration is enabled and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in idle-mode will not be a valid communication character (see chapter 1.9.1.4 for complete description).

☞ When the multiplexer protocol is active, the **CTS** line state is mapped to FCon / FCoff MUX command for flow control issues outside the power saving configuration while the physical **CTS** line is still used as a power state indicator. For more details, refer to Mux Implementation Application Note [20].

RTS signal behavior

The hardware flow control input (**RTS** line) is set by default to the OFF state (high level) at UART initialization. The module then holds the **RTS** line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **RTS** input.

If the HW flow control is enabled (for more details, refer to u-blox AT Commands Manual [2] AT&K, AT\Q, AT+IFC command descriptions) the module monitors the **RTS** line to detect permission from the DTE to send data to the DTE itself. If the **RTS** line is set to OFF state, any on-going data transmission from the module is immediately interrupted or any subsequent transmission forbidden until the **RTS** line changes to ON state.

☞ The DTE must still be able to accept a certain number of characters after the **RTS** line is set to OFF state: the module guarantees the transmission interruption within two characters from **RTS** state change.

If AT+UPSV=2 is set and HW flow control is disabled, the module monitors the **RTS** line to manage the power saving configuration:

- When an OFF-to-ON transition occurs on the **RTS** input line, the UART is enabled and the module is forced to active-mode; after ~20 ms from the transition the switch is completed and data can be received without loss. The module cannot enter idle-mode and the UART is keep enabled as long as the **RTS** input line is held in the ON state
- If the **RTS** input line is set to OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters idle-mode whenever possible

For more details, refer to chapter 1.9.1.4 and u-blox AT Commands Manual [2], AT+UPSV command.

DSR signal behavior

If AT&S0 is set, the **DSR** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&S1 is set, the **DSR** module output line is set by default to OFF state (high level) at UART initialization. The **DSR** line is then set to the OFF state when the module is in command mode or in online command mode and is set to the ON state when the module is in data mode (refer to the u-blox AT Commands Manual [2] for the definition of the interface data mode, command mode and online command mode).

DTR signal behavior

The **DTR** module input line is set by default to OFF state (high level) at UART initialization. The module then holds the **DTR** line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **DTR** input. Module behavior according to **DTR** status depends on the AT command configuration (see u-blox AT Commands Manual [2], &D AT command).

DCD signal behavior

If AT&C0 is set, the **DCD** module output line is set by default to ON state (low level) at UART initialization and is then always held in the ON state.

If AT&C1 is set, the **DCD** module output line is set by default to OFF state (high level) at UART initialization. The module then sets the **DCD** line in accordance with the carrier detect status: ON if the carrier is detected, OFF otherwise. For voice calls, **DCD** is set to the ON state when the call is established. For a data call there are the following scenarios (refer to the u-blox AT Commands Manual [2] for the definition of the interface data mode, command mode and online command mode):

- **Packet Switched Data call**: Before activating the PPP protocol (data mode) a dial-up application must provide the ATD*99***<context_number># to the module: with this command the module switches from command mode to data mode and can accept PPP packets. The module sets the **DCD** line to the ON state, then answers with a CONNECT to confirm the ATD*99 command. The **DCD** ON is not related to the context activation but with the data mode
- **Circuit Switched Data call**: To establish a data call, the DTE can send the ATD<number> command to the module which sets an outgoing data call to a remote modem (or another data module). Data can be transparent (non reliable) or non transparent (with the reliable RLP protocol). When the remote DCE accepts the data call, the module **DCD** line is set to ON and the CONNECT <communication baudrate> string is returned by the module. At this stage the DTE can send characters through the serial line to the data module which sends them through the network to the remote DCE attached to a remote DTE

☞ **DCD** is set to ON during the execution of the +CMGS, +CMGW, +USOWR, +USODL AT commands requiring input data from the DTE: the **DCD** line is set to ON state as soon as the switch to binary/text input mode is completed and the prompt is issued; **DCD** line is set to OFF as soon as the input mode is interrupted or completed (for more details refer to the u-blox AT Commands Manual [2]).

☞ **DCD** line is kept to ON state even during the online command mode to indicate that the data call is still established even if suspended, while if the module enters command mode **DSR** line is set to OFF state. For more details refer to **DSR** signal behavior description.

☞ For scenarios when the **DCD** line setting is requested for different reasons (e.g. SMS texting during online command mode), the **DCD** line changes to guarantee the correct behavior for all the scenarios. For instance, in case of SMS texting in online command mode, if the data call is released, the **DCD** line is kept to ON till the SMS command execution is completed (even if the data call release would request the **DCD** setting to OFF).

RI signal behavior

The **RI** module output line is set by default to the OFF state (high level) at UART initialization. Then, during an incoming call, the **RI** line is switched from OFF state to ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 15), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

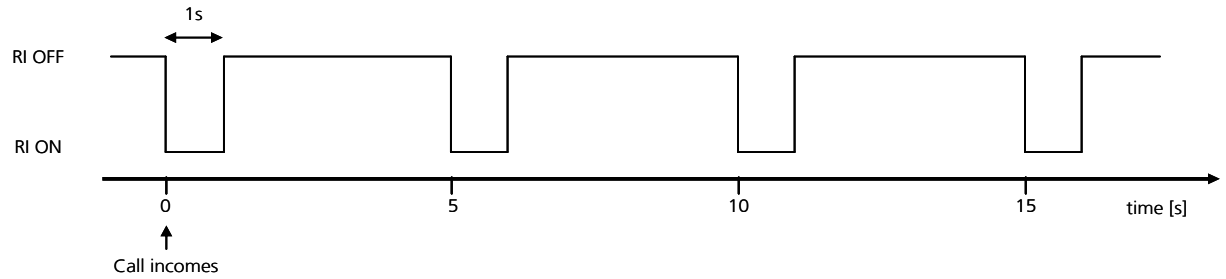


Figure 15: RI behavior during an incoming call

The **RI** line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 16), if the feature is enabled by the proper AT command (refer to the u-blox AT Commands Manual [2], AT+CNMI command).

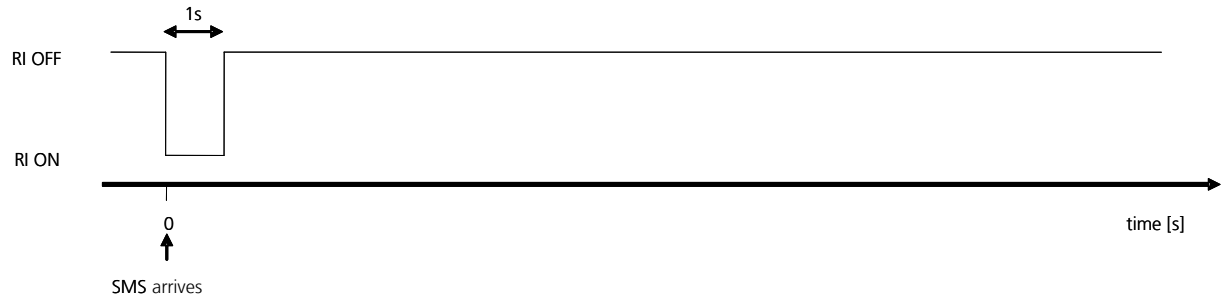


Figure 16: RI behavior at SMS arrival

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.
For SMS arrival, if several events coincidently occur or in quick succession each event independently triggers the **RI** line, although the line will not be deactivated between each event. As a result, the **RI** line may stay to ON for more than 1 s.

If an incoming call is answered within less than 1 s (with ATA or if auto-answering is set to ATS0=1) than the **RI** line is set to OFF earlier.

As a result:

- **RI** line monitoring cannot be used by the DTE to determine the number of received SMSes.
- For multiple events (incoming call plus SMS received), the **RI** line cannot be used to discriminate the two events, but the DTE must rely on the subsequent URCs and interrogate the DCE with the proper commands.

1.9.1.4 UART and power-saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description, refer to u-blox AT Commands Manual [2]). When power saving is enabled, the module automatically enters low power idle-mode whenever possible, and otherwise the active-mode is maintained by the module (see section 1.4 for definition and description of module operating modes referred to in this section).

The AT+UPSV command configures both the module power saving and also the UART behavior in relation to the power saving. The conditions for the module entering idle-mode also depend on the UART power saving configuration.

Three different power saving configurations can be set by the AT+UPSV command:

- AT+UPSV=0, power saving disabled: module forced on active-mode and UART interface enabled (default)
- AT+UPSV=1, power saving enabled: module cyclic active / idle-mode and UART enabled / disabled
- AT+UPSV=2, power saving enabled and controlled by the UART **RTS** input line

The different power saving configurations that can be set by the +UPSV AT command are described in details in the following subchapters. Table 10 summarizes the UART interface communication process in the different power saving configurations, in relation with HW flow control settings and **RTS** input line status. For more details on the +UPSV AT command description, refer to u-blox AT commands Manual [2].

AT+UPSV	HW flow control	RTS line	Communication during idle-mode and wake up
0	Enabled (AT&K3)	ON	Data sent by the DTE is correctly received by the module.
0	Enabled (AT&K3)	OFF	Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line is ON).
0	Disabled (AT&K0)	ON	Data sent by the DTE is correctly received by the module.
0	Disabled (AT&K0)	OFF	Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
1	Enabled (AT&K3)	ON	Data sent by the DTE is buffered by the DTE and will be correctly received by the module when active-mode is entered.
1	Enabled (AT&K3)	OFF	Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
1	Disabled (AT&K0)	ON	The first character sent by the DTE is lost, but it wakes up the UART (if disabled) and the module (if in idle-mode) after ~20 ms. Recognition of subsequent characters is guaranteed only after the complete wake-up of the UART and the module (i.e. after ~20 ms).
1	Disabled (AT&K0)	OFF	Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
2	Enabled (AT&K3)	ON	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Enabled (AT&K3)	OFF	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	Data sent by the DTE is correctly received by the module.
2	Disabled (AT&K0)	OFF	The first character sent by the DTE is lost, but it wakes up the UART (if disabled) and the module (if in idle-mode) after ~20 ms. Recognition of subsequent characters is guaranteed only after the complete wake-up of the UART and the module (i.e. after ~20 ms).

Table 10: UART and power-saving summary

AT+UPSV=0: power saving disabled, fixed active-mode

The module does not enter idle-mode and the UART interface is enabled (data can be sent and received): the **CTS** line is always held in the ON state after UART initialization. This is the default configuration.

AT+UPSV=1: power saving enabled, cyclic idle/active-mode

The module automatically enters idle-mode whenever possible and, if the module is registered with network, it periodically wakes up from idle-mode to active-mode for at least ~11 ms to monitor the paging channel of the current base station (paging block reception), according to the GSM discontinuous reception (DRX) specification.

The idle-mode period depends on the time period between two paging receptions defined by the current base station (i.e. by the network): the paging reception period can vary from ~0.47 s (DRX = 2, i.e. 2 x 51 GSM frames) up to ~2.12 s (DRX = 9, i.e. 9 x 51 GSM frames)

When the module wakes up to active-mode for the paging block receptions, the UART interface is enabled for at least ~11 ms concurrently to each paging reception and then, as data has not been received or sent over the UART, the interface is disabled until the next paging reception.

During a call, the UART interface is kept enabled, regardless of the AT+UPSV setting.

If the module is not registered with a network, the cyclic idle/active-mode configuration is present as well: the module automatically enters idle-mode whenever possible and periodically wakes up to active-mode to enable the UART for at least ~11 ms and then, as data has not been received or sent over the UART, the interface is disabled for a defined period (according to the latest DRX setting) and afterwards the UART is enabled again.

When UART interface is disabled, data transmitted by the DTE is lost if hardware flow control is disabled. If hardware flow control is enabled, data is buffered by the DTE and will be correctly received by the module when UART interface is enabled again.

When UART interface is enabled, data can be received. When a character is received, it forces the UART interface to stay enabled for a longer time and it forces the module to stay in the active-mode for a longer time.

The module active-mode duration depends on:

- The time period for the paging block reception, which is set by the current base station: ~11 ms minimum
- The time period where the UART interface is enabled, when the module is not registered with a network: ~11 ms minimum of in absence of data reception by serial interface
- The time period from the last data received at the serial port during the active-mode: the module does not enter idle-mode until a timeout expires. The second parameter of the +UPSV AT command configures this timeout, from 40 GSM TDMA frames (i.e. 40 x 4.615 ms = ~184 ms) up to 65000 GSM TDMA frames (i.e. 65000 x 4.615 ms = 300 s). Default value is 2000 GSM frames (i.e. 2000 x 4.615 ms = ~9.2 s)

  The active-mode duration can be extended indefinitely since every subsequent character received during the active-mode, resets and restarts the timer.

If HW flow control is enabled, the hardware flow-control output (**CTS** line) indicates when the UART interface is enabled (data can be sent and received) as illustrated in Figure 17.

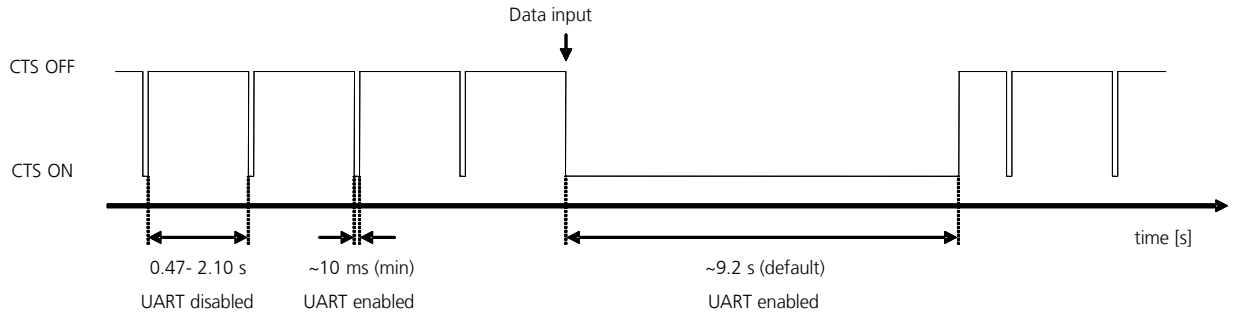


Figure 17: CTS behavior with power saving enabled (AT+UPSV=1) and HW flow control enabled: the CTS output line indicates when the UART interface of the module is enabled (CTS = ON = low level) or disabled (CTS = OFF = high level)

AT+UPSV=2: power saving enabled and controlled by the RTS line

This configuration can only be enabled with the module HW flow control disabled (AT&K0).

The UART interface is immediately disabled after the DTE sets the **RTS** line to OFF. Then, if a voice or data call is not enabled, the module automatically enters idle-mode whenever possible according to any other activity, and periodically wakes up from idle-mode to active-mode to monitor the paging channel of the current base station (paging block reception).

Instead, the UART is disabled as long as the **RTS** line is set to OFF, also when the module is in active-mode, to reduce power consumption. The UART is enabled in the following cases:

- During a call, the UART interface is kept enabled, regardless of the **RTS** line setting
- If the module must transmit some data over the UART (e.g. URC), the interface is temporarily enabled even if the **RTS** line is set to OFF by the DTE
- If the module receives a data over the UART, it causes the system wake-up: this is the "wake up via data reception" feature described in the following subsection

When the DTE sets the **RTS** line to OFF, the timeout to enter idle-mode from the last data received at the serial port during the active-mode is the one previously set with the AT+UPSV=1 configuration or it is the default value.

If the **RTS** line is set to ON by the DTE the module is not allowed to enter idle-mode and the UART is kept enabled until the **RTS** line is set to OFF.

When an OFF-to-ON transition occurs on the **RTS** input line, the UART is re-enabled and the module, if it was in idle-mode, switches from idle to active-mode after ~20 ms: this is the UART and module "wake up time".

☞ Even if HW flow control is disabled, if the DTE sets the **RTS** line to OFF, the module sets the **CTS** line accordingly to its power saving configuration as illustrated in Figure 17, like for the AT+UPSV=1 case with HW flow control enabled.

Wake up via data reception

If the DTE transmits data when the UART is disabled (when power saving is configured), it is lost (not correctly received by the module) in the following cases:

- +UPSV=1 with hardware flow control disabled
- +UPSV=2 with hardware flow control disabled and **RTS** line set to OFF

When the module is in idle-mode, the **TXD** input line of the module is always configured to wake up the UART and the module via data reception: when a low-to-high transition occurs on the **TXD** input line, it causes the system wake-up. The UART is enabled and the module switches from idle-mode to active-mode within ~20 ms from the first data reception: this is the system "wake up time". As a consequence, the first character sent by the DTE when UART is disabled (i.e. the wake up character) is not a valid communication character because it cannot be recognized, and the recognition of the subsequent characters is guaranteed only after the complete system wake-up (i.e. after ~20 ms).

Figure 18 and Figure 19 show an example of common scenarios and timing constraints:

- AT+UPSV=2 power saving configuration is active and the timeout from last data received to idle-mode start is set to 2000 frames due to the timeout previously set by AT+UPSV=1,2000 as the default case
- Hardware flow control disabled on the DCE (as required to enable the AT+UPSV=2 configuration) and **RTS** line set to OFF by the DTE: in this case the **CTS** line is set by the module accordingly to its power saving configuration as illustrated in Figure 17, like for the AT+UPSV=1 case with HW flow control enabled

Figure 18 shows the case where the DCE UART is disabled and only a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE UART is disabled when the timeout from last data received expires (2000 frames without data reception, as the default case).

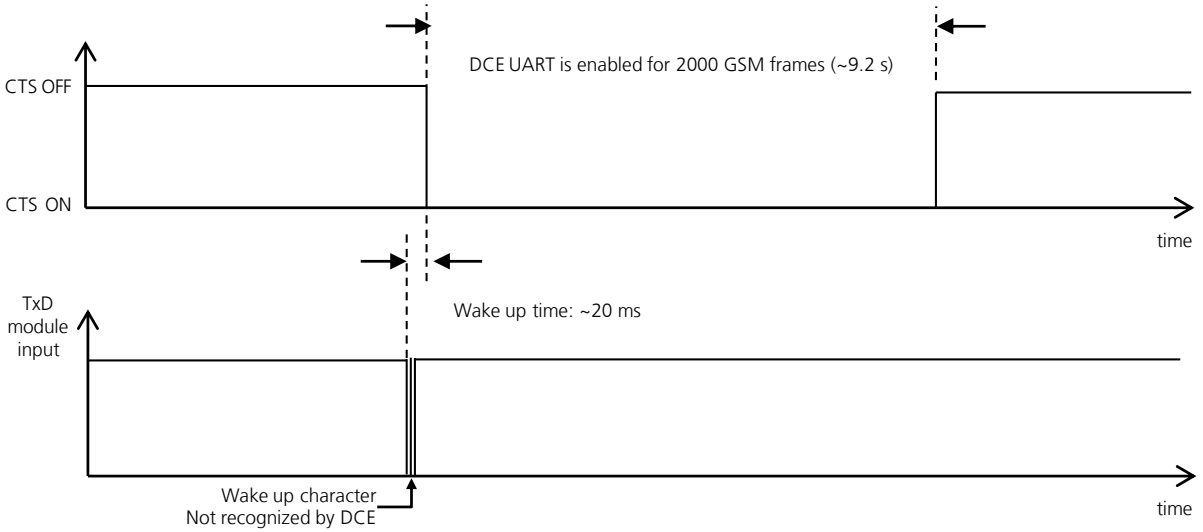


Figure 18: Wake-up via data reception without further communication

Figure 19 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake up character wakes-up the DCE UART. The other characters must be sent after the "wake up time" of ~20 ms. If this condition is satisfied, the DCE recognizes characters. The DCE is allowed to disable the UART and re-enters idle-mode after 2000 GSM frames from the latest data reception.

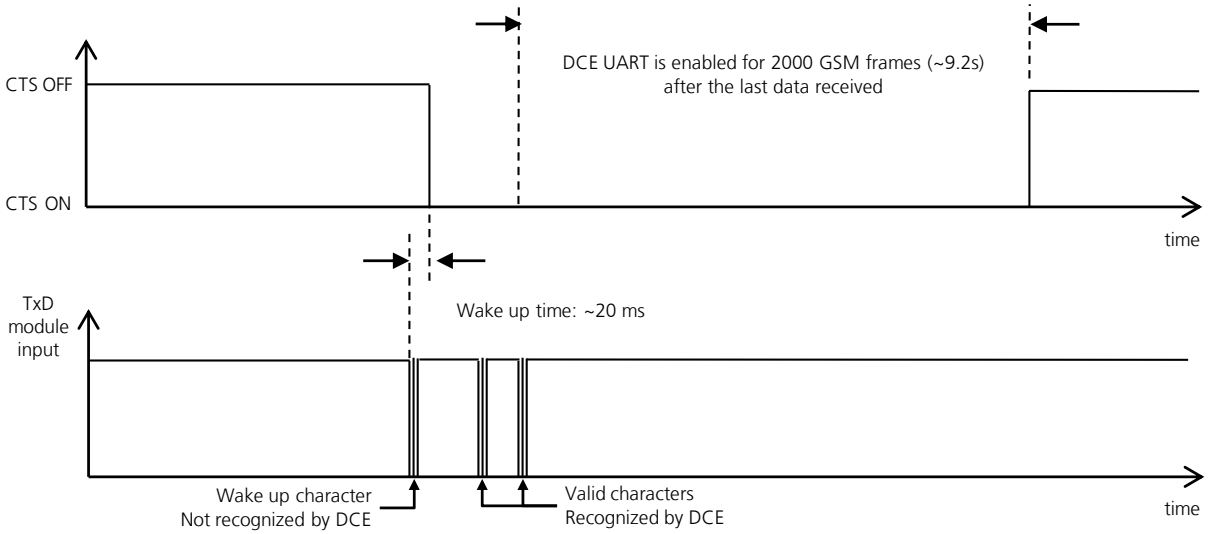


Figure 19: Wake-up via data reception with further communication

☞ The "wake-up via data reception" feature cannot be disabled.

☞ In command mode[7], if autobauding is enabled and the DTE does not implement HW flow control, the DTE must always send a character to the module before the "AT" prefix set at the beginning of each command line: the first character is ignored if the module is in active-mode, or it represents the wake-up character if the module is in idle-mode.

[7] Refer to the u-blox AT Commands Manual [2] for the definition of the interface data mode, command mode and online command mode.

☞ In command mode[7], if autobauding is disabled, the DTE must always send a dummy "AT" before each command line: the first character is not ignored if the module is in active-mode (i.e. the module replies "OK"), or it represents the wake up character if the module is in idle-mode (i.e. the module does not reply).

☞ No wake-up character or dummy "AT" is required from the DTE during a voice or data call since the module UART interface continues to be enabled and does not need to be woken-up. Furthermore in data mode[7] a dummy "AT" would affect the data communication.

1.9.1.5 Multiplexer protocol (3GPP 27.010)

SARA-G3 modules have a software layer with MUX functionality, 3GPP TS 27.010 Multiplexer Protocol [12], available on the UART physical link. The auxiliary UART and the DDC (I^2C) serial interfaces do not support the multiplexer protocol.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use AT command interface on one MUX channel and Packet-Switched / Circuit-Switched Data communication on another multiplexer channel. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GPS, AT commands in general. This permits, for example, SMS to be transferred to the DTE when a data connection is in progress.

The following virtual channels are defined for SARA-G350 modules:

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection
- Channel 6: GPS tunneling

The following virtual channels are defined for SARA-G300 and SARA-G310 modules:

- Channel 0: control channel
- Channel 1 – 2: AT commands / data connection

For more details, refer to Mux implementation Application Note [20].

1.9.2 Auxiliary asynchronous serial interface (UART AUX)

The auxiliary UART interface is a 3-wire unbalanced 1.8 V asynchronous serial interface (only the **RXD_AUX** data output and **TXD_AUX** data input are provided), available for SARA-G3 modules FW upgrade by means of the u-blox EasyFlash tool and for Trace log capture (debug purpose). The AT commands interface is not available on the auxiliary UART interface.

1.9.3 DDC (I^2C) interface

☞ SARA-G300 and SARA-G310 modules do not support DDC (I^2C) interface.

An I^2C bus compatible Display Data Channel (DDC) interface for communication with u-blox GPS/GNSS receivers is available on **SDA** and **SCL** pins of SARA-G350 modules. Only this interface provides the communication between the u-blox wireless module and u-blox positioning chips and modules. The AT commands interface is not available on the DDC (I^2C) interface.

DDC (I^2C) slave-mode operation is not supported: the SARA-G350 wireless module can act as master only, and the connected u-blox GPS/GNSS receiver automatically acts as slave in the DDC (I^2C) communication.

Two lines, serial data (**SDA**) and serial clock (**SCL**), carry information on the bus. **SCL** is used to synchronize data transfers, and **SDA** is the data line. To be compliant to the I²C bus specifications, the module bus interface pads are open drain output and pull up resistors must be used conforming to the I²C bus specifications [13].

u-blox has implemented special features in SARA-G350 wireless modules to ease the design effort required for the integration of a u-blox wireless module with a u blox GPS/GNSS receiver.

Combining a u-blox wireless module with a u-blox GPS/GNSS receiver allows designers to have full access to the positioning receiver directly via the wireless module: it relays control messages to the GPS/GNSS receiver via a dedicated DDC (I²C) interface. A 2nd interface connected to the positioning receiver is not necessary: AT commands via the UART serial interface of the wireless module allows a fully control of the GPS/GNSS receiver from any host processor.

SARA-G350 modules feature embedded GPS aiding that is a set of specific features developed by u-blox to enhance GPS/GNSS performance, decreasing Time To First Fix (TTFF), thus allowing to calculate the position in a shorter time with higher accuracy.

SARA-G350 modules support these GPS aiding types:

- Local aiding
- AssistNow Online
- AssistNow Offline
- AssistNow Autonomous

The embedded GPS aiding features can be used only if the DDC (I²C) interface of the wireless module is connected to the u-blox GPS/GNSS receivers.

SARA-G350 wireless modules provide additional custom functions over GPIO pins to improve the integration with u-blox positioning chips and modules. GPIO pins can handle:

- GPS/GNSS receiver power-on/off: "GPS supply enable" function provided by **GPIO2** improves the positioning receiver power consumption. When the GPS/GNSS functionality is not required, the positioning receiver can be completely switched off by the wireless module that is controlled by the application processor with AT commands
- The wake up from idle-mode when the GPS/GNSS receiver is ready to send data: "GPS data ready" function provided by **GPIO3** improves the wireless module power consumption. When power saving is enabled in the wireless module by the AT+UPSV command and the GPS/GNSS receiver does not send data by the DDC (I²C) interface, the module automatically enters idle-mode whenever possible. With the "GPS data ready" function the GPS/GNSS receiver can indicate to the wireless module that it is ready to send data by the DDC (I²C) interface: the positioning receiver can wake up the wireless module if it is in idle-mode, so the wireless module does not lose the data sent by the GPS/GNSS receiver even if power saving is enabled
- The RTC synchronization signal to the GPS/GNSS receiver: "GPS RTC sharing" function provided by **GPIO4** improves GPS/GNSS receiver performance, decreasing the Time To First Fix (TTFF), and thus allowing to calculate the position in a shorter time with higher accuracy. When GPS local aiding is enabled, the wireless module automatically uploads data such as position, time, ephemeris, almanac, health and ionospheric parameter from the positioning receiver into its local memory, and restores this to the GPS/GNSS receiver at the next power up of the positioning receiver

☞ For more details regarding the handling of the DDC (I²C) interface, the GPS aiding features and the GPS related functions over GPIOs, refer to the chapter 1.11, to the u-blox AT Commands Manual [2] (AT+UGPS, AT+UGPRF, AT+UGPIOC AT commands) and the GPS Implementation Application Note [21].

☞ "GPS data ready" and "GPS RTC sharing" functions are not supported by all u-blox GPS/GNSS receivers HW or ROM/FW versions. Refer to the GPS Implementation Application Note [21] or to the Hardware Integration Manual of the u-blox GPS/GNSS receivers for the supported features.

As additional improvement for the GPS/GNSS receiver performance, the **V_BCKP** supply output of SARA-G350 modules can be connected to the **V_BCKP** backup supply input pin of u-blox positioning chips and modules to provide the supply for the GPS/GNSS real time clock and backup RAM when the **VCC** supply of the wireless module is within its operating range and the **VCC** supply of the GPS/GNSS receiver is disabled.

This enables the u-blox positioning receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the GPS/GNSS receiver **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

1.10 Audio interface

☞ SARA-G300 and SARA-G310 modules do not support audio interface.

SARA-G350 modules provide one analog audio interface and one digital audio interface that can be selected and set by the dedicated AT command +USPM (refer to u-blox AT Commands Manual [2]): this command allows setting the audio path mode, composed by the uplink audio path and the downlink audio path.

Each uplink path mode defines the physical input (i.e. the analog or the digital audio input) and the set of parameters to process the uplink audio signal (uplink gains, uplink digital filters, echo canceller parameters). For example the "Headset microphone" uplink path uses the differential analog audio input with the default parameters for the headset profile.

Each downlink path mode defines the physical output (i.e. the analog or the digital audio output) and the set of parameters to process the downlink audio signal (downlink gains, downlink digital filters and sidetone). For example the "Mono headset" downlink path uses the differential analog audio output with the default parameters for the headset profile.

The set of parameters to process the uplink or the downlink audio signal can be changed with dedicated AT commands for each uplink or downlink path and then stored in two profiles in the non volatile memory (refer to u-blox AT Commands Manual [2] for Audio parameters tuning commands).

1.10.1 Analog audio interface

1.10.1.1 Uplink path

SARA-G350 pins related to the analog audio uplink path are:

- **MIC_P / MIC_N**: Differential analog audio signal inputs (positive/negative). These two pins are internally directly connected to the differential input of an integrated Low Noise Amplifier, without any internal series capacitor for DC blocking. The LNA output is internally connected to the digital processing system by an integrated sigma-delta analog-to-digital converter
- **MIC_BIAS**: Supply output for an external microphone. The pin is internally connected to the output of a low noise LDO linear regulator provided with proper internal bypass capacitor to guarantee stable operation of the linear regulator
- **MIC_GND**: Local ground for the external microphone. The pin is internally connected to ground as a sense line as the reference for the analog audio input

The analog audio input is selected when the parameter <main_uplink> in AT+USPM command is set to "Headset microphone", "Handset microphone" or "Hands-free microphone": the uplink analog path profiles use the same physical input but have different sets of audio parameters (for more details, refer to u-blox AT Commands Manual [2], AT+USPM, AT+UMGC, AT+UUBF, AT+UHFP commands).

SARA-G3 series Data Sheet [1] provides the detailed electrical characteristics of the analog audio uplink path.

1.10.1.2 Downlink path

SARA-G350 pins related to the analog audio downlink path are:

- **SPK_P / SPK_N**: Differential analog audio signal output (positive/negative). These two pins are directly connected internally to the differential output of a low power audio amplifier, for which the input is connected internally to the digital processing system by to an integrated digital-to-analog converter.

The analog audio output is selected when the parameter <main_downlink> in AT+USPM command is set to "Normal earpiece", "Mono headset" or "Loudspeaker": the downlink analog path profiles use the same physical output but have different sets of audio parameters (for more details, refer to the u-blox AT Commands Manual [2], AT+USPM, AT+USGC, AT+UDBF, AT+USTN commands).

The differential analog audio output of SARA-G350 modules (**SPK_P / SPK_N**) is able to directly drive loads with resistance rating greater than 14 Ω: it can be directly connected to a headset earpiece or handset earpiece but cannot directly drive a 8 Ω or 4 Ω loudspeaker for the hands-free mode.

SARA-G3 series Data Sheet [1] provides the detailed electrical characteristics of the analog audio downlink path.

⚠ **Warning: excessive sound pressure from headphones can cause hearing loss.**

1.10.1.3 Headset mode

Headset mode is the default audio operating mode of the modules. The headset profile is configured when the uplink audio path is set to "Headset microphone" and the downlink audio path is set to "Mono headset" (refer to u-blox AT Commands Manual [2]: AT+USPM command: <main_uplink>, <main_downlink> parameters).

1.10.1.4 Handset mode

The handset profile is configured when the uplink audio path is set to "Handset microphone" and the downlink audio path is set to "Normal earpiece" (refer to u-blox AT commands manual [2]: AT+USPM command: <main_uplink>, <main_downlink> parameters).

1.10.1.5 Hands-free mode

The hands-free profile is configured when the uplink audio path is set to "Hands-free microphone" and the downlink audio path is set to "Loudspeaker" (refer to u-blox AT commands manual [2]: AT+USPM command: <main_uplink>, <main_downlink> parameters).

Hands-free functionality is implemented using appropriate digital signal processing algorithms for voice-band handling (echo canceller and automatic gain control), managed via software (refer to u-blox AT commands manual [2], AT+UHFP command).

1.10.2 Digital audio interface

SARA-G350 modules provide one 4-wire I²S digital audio interface (1.8 V) that acts as an I²S master and can be used for digital audio communication with external digital audio devices that acts as I²S slave. Related pins are:

- **I2S_TXD** data output
- **I2S_RXD** data input
- **I2S_CLK** clock output
- **I2S_WA** world alignment output

The I²S interface can be set to two modes, by the <I2S_mode> parameter of the AT+UI2S command:

- PCM mode
- Normal I²S mode

☞ SARA-G350 modules do not support I²S slave mode: module acts as master only.

☞ The sample rate is fixed at 8 kHz only: it is not possible to configure the sample rate of transmitted and received words of SARA-G350 modules.

The <main_uplink> and <main_downlink> parameters of the AT+USPM command must be properly configured to select the I²S digital audio interfaces paths (for more details, refer to u-blox AT Commands Manual [2]):

- <main_uplink> must be properly set to select:
  - the I²S interface (using **I2S_RXD** module input)
- <main_downlink> must be properly set to select:
  - the I²S interface (using **I2S_TXD** module output)

Parameters of digital path can be configured and saved as the normal analog paths, using appropriate path parameter as described in the u-blox AT Commands Manual [2], +USGC, +UMGC, +USTN AT command. Analog gain parameters of microphone and speakers are not used when digital path is selected.

The I²S receive data input and the I²S transmit data output signals are respectively connected in parallel to the analog microphone input and speaker output signals, so resources available for analog path can be shared:

- Digital filters and digital gains are available in both uplink and downlink direction. The AT commands allow to properly configure them
- Ringer tone and service tone are mixed on the TX path when active (downlink)
- The HF algorithm acts on I²S path

☞ Refer to the u-blox AT Commands Manual [2]: AT+UI2S command for possible settings of I²S interface.

1.10.2.1 I²S interface – PCM mode

Main features of the I²S interface in PCM mode:

- I²S runs in PCM – short alignment mode (configurable by AT commands)
- I²S word alignment signal is configured to 8 kHz: this is the <sample_rate> parameter
- I²S word alignment toggles high for 1 or 2 CLK cycles of synchronization (configurable), then toggles low for 16 CLK cycles of sample width. Frame length can be 1 + 16 = 17 bits or 2 + 16 = 18 bits
- I²S clock frequency depends on frame length and the 8 kHz sample rate. Can be 17 x 8 kHz or 18 x 8 kHz
- I²S transmit and I²S receive data are 16 bit words long with the same sampling rate as I²S word alignment, mono. Data is in 2's complement notation. MSB is transmitted first

- When I²S word alignment toggles high, the first synchronization bit is always low. Second synchronization bit (present only in case of 2 bit long I²S word alignment configuration) is MSB of the transmitted word (MSB is transmitted twice in this case)
- I²S transmit data changes on I²S clock rising edge, I²S receive data changes on I²S clock falling edge

1.10.2.2 I²S interface – Normal I²S mode

Normal I²S supports:

- 16 bits word
- Mono interface
- Sample rate: 8 kHz

Main features of I²S interface in normal I²S mode:

- I²S runs in normal I²S – long alignment mode (configurable by AT commands)
- I²S word alignment signal always runs at 8 kHz sample rate and synchronizes 2 channels (timeslots on word alignment high, word alignment low)
- I²S transmit data is composed of 16 bit words, dual mono (the words are written on both channels). Data are in 2's complement notation. MSB is transmitted first. The bits are written on I²S clock rising or falling edge (configurable)
- I²S receive data is read as 16 bit words, mono (words are read only on the timeslot with WA high). Data is read in 2's complement notation. MSB is read first. The bits are read on the I²S clock edge opposite to I²S transmit data writing edge (configurable)
- I²S clock frequency is 16 bits x 2 channels x 8 kHz

The modes are configurable through a specific AT command (refer to the related chapter in the u-blox AT Commands Manual [2], +UI2S AT command) and the following parameters can be set:

- MSB can be 1 bit delayed or non-delayed on I²S word alignment edge
- I²S transmit data can change on rising or falling edge of I²S clock signal
- I²S receive data are read on the opposite front of I²S clock signal

1.10.3 Voice-band processing system

1.10.3.1 Audio processing system overview

The voice-band processing on the SARA-G350 modules is implemented in the DSP core inside the baseband chipset. The analog audio front-end of the chipset is connected to the digital system through 16 bit ADC converters in the uplink path, and through 16 bit DAC converters in the downlink path. External digital audio devices can directly be interfaced to the DSP digital processing part via the I²S digital interface. The analog amplifiers are skipped in this case.

The voice-band processing system can be split up into three different blocks:

- Sample-based Voice-band Processing (single sample processed at 8 kHz, every 125 µs)
- Frame-based Voice-band Processing (frames of 160 samples are processed every 20 ms)
- MIDI synthesizer running at 47.6 kHz

These three blocks are connected by buffers and sample rate converters (for 8 to 47.6 kHz conversion)

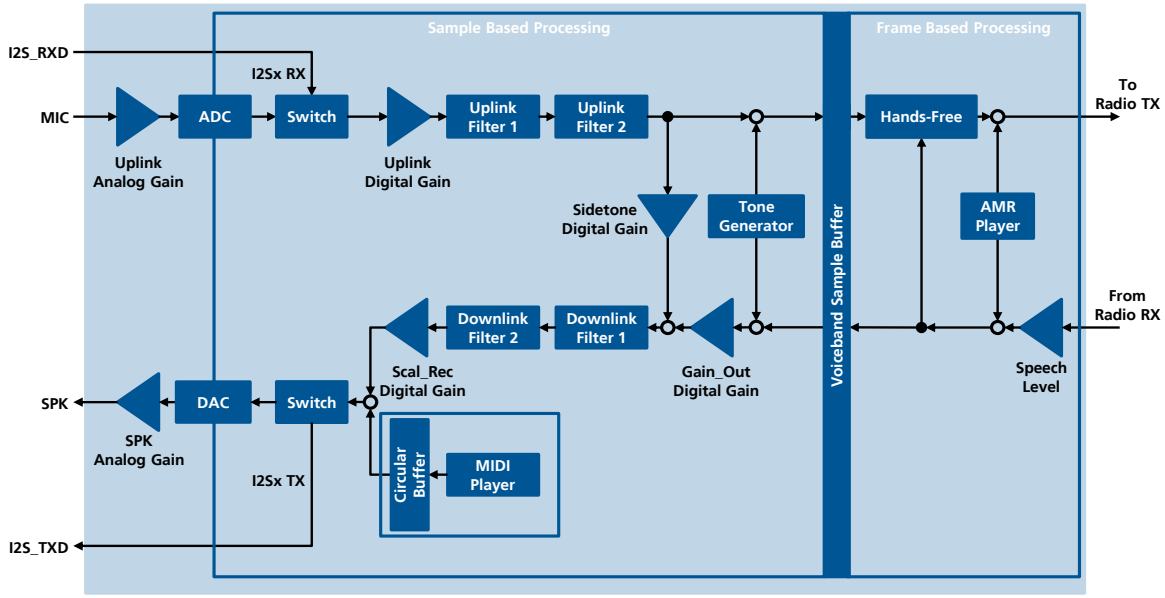


Figure 20: SARA-G350 modules voice-band processing system block diagram

The sample-based voice-band processing main task is to transfer the voice-band samples from either analog audio front-end uplink path or I2Sx RX path to the Voice-band Sample Buffer and from the Voice-band Sample Buffer to the analog audio front-end downlink path and/or I2Sx TX path. While doing this the samples are scaled by digital gains and processed by digital filters both in the uplink and downlink direction and the sidetone is generated mixing scaled uplink samples to the downlink samples (refer to the u-blox AT Commands Manual [2], +UUBF, +UDBF, +UMGC, +USGC, +USTN commands).

The frame-based voice-band processing implements the Hands-Free algorithm. This consists of the Echo Canceller, the Automatic Gain Control and the Noise Suppressor. Hands-Free algorithm acts on the uplink signal only. Algorithms are configurable with AT commands (refer to the u-blox AT Commands Manual [2], +UHFP command). The frame-based voice-band processing also implements an AMR player. The speech uplink path final block before radio transmission is the speech encoder. Symmetrically, on downlink path, the starting block is the speech decoder which extracts speech signal from the radio receiver.

The circular buffer is a 3000 word buffer to store and mix the voice-band samples from Midi synthesizer. The buffer has a circular structure, so that when the write pointer reaches the end of the buffer, it is wrapped to the begin address of the buffer.

Two different sample-based sample rate converters are used: an interpolator, required to convert the sample-based voice-band processing sampling rate of 8 kHz to the analog audio front-end output rate of 47.6 kHz; a decimator, required to convert the circular buffer sampling rate of 47.6 kHz to the I2Sx TX or the uplink path sample rate of 8 kHz.

1.10.3.2 Audio codecs

The following speech codecs are supported by firmware on the DSP :

- GSM Half Rate (TCH/HS)
- GSM Full Rate (TCH/FS)
- GSM Enhanced Full Rate (TCH/EFR)
- 3GPP Adaptive Multi Rate (AMR) (TCH/AFS+TCH/AHS)
    - In AMR Full Rate (AFS) the Active CODEC Set is selected from an overall set of 8 data rates:
      12.2 – 10.2 – 7.95 – 7.40 – 6.70 – 5.90 – 5.15 – 4.75 kb/s
    - In AMR Half Rate (AHS) the overall set comprises 6 different data rates:
      7.95 – 7.40 – 6.70 – 5.90 – 5.15 – 4.75 kb/s

1.11 General Purpose Input/Output (GPIO)

☞ SARA-G300 and SARA-G310 modules do not support GPIOs.

SARA-G350 modules provide 4 pins (**GPIO1**-**GPIO4**) which can be configured as general purpose input or output, or can be configured to provide special functions via u-blox AT commands (for further details refer to the u-blox AT Commands Manual [2], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF).

The following functions are available in the SARA-G350 modules:

- **Network status indication**:

  The **GPIO1**, or the **GPIO2**, **GPIO3** and **GPIO4** alternatively from their default settings, can be configured to indicate network status (i.e. no service, registered home network, registered visitor network, voice or data call enabled), setting the parameter <gpio_mode> of AT+UGPIOC command to 2.

  No GPIO pin is by default configured to provide the "Network status indication" function.

  The "Network status indication" mode can be provided only on one pin per time: it is not possible to simultaneously set the same mode on another pin.

  The pin configured to provide the "Network status indication" function is set as
  - Continuous Output / Low, if no service (no network coverage or not registered)
  - Cyclic Output / High for 100 ms, Output / Low for 2 s, if registered with the home network
  - Cyclic Output / High for 100 ms, Output / Low for 100 ms, Output / High for 100 ms, Output / Low for 2 s, if registered with the visitor network (roaming)
  - Continuous Output / High, if voice or data call enabled

- **GSM Tx burst indication**:

  GPIO1 pin can be configured by AT+UGPIOC to indicate when a GSM Tx burst/slot occurs, setting the parameter <gpio_mode> of AT+UGPIOC command to 9.

  No GPIO pin is by default configured to provide the "GSM Tx burst indication" function.

  The pin configured to provide the "GSM Tx burst indication" function is set as
  - Output / High, since ~10 µs before the start of first Tx slot, until ~5 µs after the end of last Tx slot
  - Output / Low, otherwise

- **GPS supply enable**:

  The **GPIO2** is by default configured by AT+UGPIOC command to enable or disable the supply of the u-blox GPS/GNSS receiver connected to the wireless module.

  The **GPIO1**, **GPIO3** or **GPIO4** pins can be configured to provide the "GPS supply enable" function, alternatively to the default **GPIO2** pin, setting the parameter <gpio_mode> of AT+UGPIOC command to 3. The "GPS supply enable" mode can be provided only on one pin per time: it is not possible to simultaneously set the same mode on another pin.

  The pin configured to provide the "GPS supply enable" function is set as
  - Output / High, to switch on the u-blox GPS/GNSS receiver, if the parameter <mode> of AT+UGPS command is set to 1
  - Output / Low, to switch off the u-blox GPS/GNSS receiver, if the parameter <mode> of AT+UGPS command is set to 0 (default setting)

- **GPS data ready**:

  Only the **GPIO3** pin provides the "GPS data ready" function, to sense when a u-blox GPS/GNSS receiver connected to the wireless module is ready to send data via the DDC (I^2C) interface, setting the parameter <gpio_mode> of AT+UGPIOC command to 4.

  The pin configured to provide the "GPS data ready" function is set as
  - Input, to sense the line status, waking up the wireless module from idle-mode when the u-blox GPS/GNSS receiver is ready to send data via the DDC (I^2C) interface; the parameter <mode> of AT+UGPS command must be set to 1 and the parameter <GPS_IO_configuration> of AT+UGPRF command to 16
  - Tri-state with an internal active pull-down enabled, otherwise (default setting)

- **GPS RTC sharing**:

  Only the **GPIO4** pin provides the "GPS RTC sharing" function, to provide an RTC (Real Time Clock) synchronization signal to the u-blox GPS/GNSS receiver connected to the wireless module, setting the parameter <gpio_mode> of AT+UGPIOC command to 5.

  The pin configured to provide the "GPS RTC sharing" function is set as
  - Output, to provide an RTC (Real Time Clock) synchronization signal to the u-blox GPS/GNSS receiver if the parameter <mode> of AT+UGPS command is set to 1 and parameter <GPS_IO_configuration> of AT+UGPRF command is set to 32
  - Output / Low, otherwise (default setting)

- **General purpose input**:

  All the GPIOs can be configured as input to sense high or low digital level through AT+UGPIOR command, setting the parameter <gpio_mode> of AT+UGPIOC command to 1.

  The "General purpose input" mode can be provided on more than one pin at a time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

  No GPIO pin is by default configured as "General purpose input".

  The pin configured to provide the "General purpose input" function is set as
  - Input, to sense high or low digital level by AT+UGPIOR command.

- **General purpose output**:

  All the GPIOs can be configured as output to set the high or the low digital level through AT+UGPIOW command, setting the parameter <gpio_mode> of +UGPIOC AT command to 0.

  The "General purpose output" mode can be provided on more than one pin per time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

  No GPIO pin is by default configured as "General purpose output".

  The pin configured to provide the "General purpose output" function is set as
  - Output / Low, if the parameter <gpio_out_val> of AT+UGPIOW command is set to 0
  - Output / High, if the parameter <gpio_out_val> of AT+UGPIOW command is set to 1

- **Pad disabled**:

  All the GPIOs can be configured in tri-state with an internal active pull-down enabled, as a not used pin, setting the parameter <gpio_mode> of +UGPIOC AT command to 255.

  The "Pad disabled" mode can be provided on more than one pin per time: it is possible to simultaneously set the same mode on another pin (also on all the GPIOs).

  The pin configured to provide the "Pad disabled" function is set as
  - Tri-state with an internal active pull-down enabled

Table 11 describes the configurations of all SARA-G350 GPIO pins.

Pin	Module	Name	Description	Remarks
16	SARA-G350	**GPIO1**	GPIO	By default, the pin is configured as Pad disabled. Can be alternatively configured by the AT+UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • GSM Tx Burst Indication
23	SARA-G350	**GPIO2**	GPIO	By default, the pin is configured to provide GPS Supply Enable function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • Pad disabled
24	SARA-G350	**GPIO3**	GPIO	By default, the pin is configured to provide GPS Data Ready function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • Pad disabled
25	SARA-G350	**GPIO4**	GPIO	By default, the pin is configured to provide GPS RTC sharing function. Can be alternatively configured by the +UGPIOC command as • Output • Input • Network Status Indication • GPS Supply Enable • Pad disabled

Table 11: GPIO pins configurations

1.12 Reserved pins (RSVD)

SARA-G3 modules have pins reserved for future use: they can all be left unconnected on the application board, except the **RSVD** pin number 33 that must be externally connected to ground.

1.13 System features

1.13.1 Network indication

☞ Not supported by SARA-G300 and SARA-G310 modules.

The **GPIO1**, or the **GPIO2**, **GPIO3** and **GPIO4** alternatively from their default settings, can be configured to indicate network status (i.e. no service, registered home network, registered visitor network, voice or data call enabled), by means of the AT+UGPIOC command.

For the detailed description, refer to chapter 1.11 and to u-blox AT Commands Manual [2], GPIO commands.

1.13.2 Antenna detection

☞ Not supported by SARA-G300 and SARA-G310 modules.

ANT_DET pin of SARA-G350 modules is an Analog to Digital Converter (ADC) provided to sense the presence of an external antenna when optionally set by the +UANTR AT command.

The external antenna assembly must be provided with a built-in resistor (diagnostic circuit) to be detected, and an antenna detection circuit must be implemented on the application board properly connecting the antenna detection input (**ANT_DET**) to the antenna RF interface (**ANT**).

For more details regarding feature description and detection / diagnostic circuit design-in refer to chapters 1.7.1 and 2.3.2, and to the u-blox AT Commands Manual [2].

1.13.3 Jamming detection

☞ Not supported by SARA-G300 and SARA-G310 modules.

In real network situations modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operators' choices, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carriers entitled to give access to the GSM service.

The Jamming Detection Feature detects such "artificial" interference and reports the start and stop of such conditions to the client, which can react appropriately by e.g. switching off the radio transceiver to reduce power consumption and monitoring the environment at constant periods.

The feature detects, at radio resource level, an anomalous source of interference and signals it to the client with an unsolicited indication when the detection is entered or released. The jamming condition occurs when:

- The module has lost synchronization with the serving cell and cannot select any other cell
- The band scan reveals at least n carriers with power level equal or higher than threshold
- On all such carriers, no synchronization is possible

The number of minimum disturbing carriers and the power level threshold can be configured by the client by using the AT+UCD command [2].

The client can configure the number of minimum disturbing carriers and the power level threshold by using the AT+UCD command [2].

The jamming condition is cleared when any of the above mentioned statements does not hold.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command (for more details refer to the u-blox AT Commands Manual [2]).

1.13.4 TCP/IP and UDP/IP

☞ Not supported by SARA-G300 and SARA-G310 modules.

Via the AT commands it is possible to access the TCP/IP and UDP/IP functionalities over the Packet Switched data connection. For more details about AT commands see the u-blox AT Commands Manual [2].

Using the embedded TCP/IP or UDP/IP stack, only 1 IP instance (address) is supported. The IP instance supports up to 7 sockets. Using an external TCP/IP stack (on the application processor), it is possible to have 3 IP instances (addresses).

Direct Link mode for TCP and UDP sockets is supported. Sockets can be set in Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via serial interface. In Direct Link mode, data sent to the serial interface from an external application processor is forwarded to the network and vice-versa.

To avoid data loss while using Direct Link, enable HW flow control on the serial interface.

1.13.5 FTP

☞ Not supported by SARA-G300 and SARA-G310 modules.

SARA-G350 modules support the File Transfer Protocol functionalities via AT commands. Files are read and stored in the local file system of the module. For more details about AT commands see the u-blox AT Commands Manual [2].

1.13.6 HTTP

☞ Not supported by SARA-G300 and SARA-G310 modules.

HTTP client is implemented in SARA-G350 modules: HEAD, GET, POST, DELETE and PUT operations are available. The file size to be uploaded / downloaded depends on the free space available in the local file system (FFS) at the moment of the operation. Up to 4 HTTP client contexts can simultaneously be used.

For more details about AT commands see the u-blox AT Commands Manual [2].

1.13.7 SMTP

☞ Not supported by SARA-G300 and SARA-G310 modules.

SARA-G350 modules support SMTP client functionalities. It is possible to specify the common parameters (e.g. server data, authentication method, etc. can be specified), to send an email to a SMTP server. Emails can be sent with or without attachment. Attachments are store in the local file system of SARA-G350 modules.

For more details about AT commands see the u-blox AT Commands Manual [2].

1.13.8 Smart temperature management

Wireless modules – independent of the specific model – always have a well-defined operating temperature range. This range should be respected to guarantee full device functionality and long life span.

Nevertheless there are environmental conditions that can affect operating temperature, e.g. if the device is located near a heating/cooling source, if there is/is not air circulating, etc.

The module itself can also influence the environmental conditions; such as when it is transmitting at full power. In this case its temperature increases very quickly and can raise the temperature nearby.

The best solution is always to properly design the system where the module is integrated. Nevertheless an extra check/security mechanism embedded into the module is a good solution to prevent operation of the device outside of the specified range.

1.13.8.1 Smart Temperature Supervisor (STS)

The Smart Temperature Supervisor is activated and configured by a dedicated AT+USTS command. Refer to u-blox AT Commands Manual [2] for more details.

The wireless module measures the internal temperature (Ti) and its value is compared with predefined thresholds to identify the actual working temperature range.

☞ Temperature measurement is done inside the module: the measured value could be different from the environmental temperature (Ta).

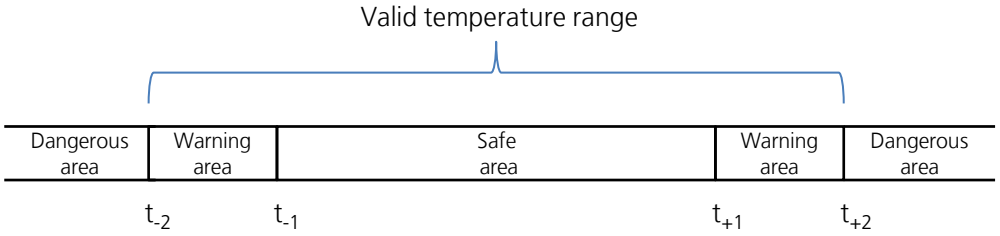


Figure 21: Temperature range and limits

The entire temperature range is divided into sub-regions by limits (see Figure 21) named t_{-2}, t_{-1}, t_{+1} and t_{+2}.

- Within the first limit, ($t_{-1} < Ti < t_{+1}$), the wireless module is in the normal working range, the Safe Area
- In the Warning Area, ($t_{-2} < Ti < t_{-1}$) or ($t_{+1} < Ti < t_{+2}$), the wireless module is still inside the valid temperature range, but the measured temperature approaches the limit (upper or lower). The module sends a warning to the user (through the active AT communication interface), which can take, if possible, the necessary actions to return to a safer temperature range or simply ignore the indication. The module is still in a valid and good working condition
- Outside the valid temperature range, ($Ti < t_{-2}$) or ($Ti > t_{+2}$), the device is working outside the specified range and represents a dangerous working condition. This condition is indicated and the device shuts down to avoid damage

☞ For security reasons the shutdown is suspended in case an emergency call in progress. In this case the device switches off at call termination.

☞ The user can decide at anytime to enable/disable the Smart Temperature Supervisor feature. If the feature is disabled there is no embedded protection against disallowed temperature conditions.

Figure 22 shows the flow diagram implemented in SARA-G3 series modules for the Smart Temperature Supervisor.

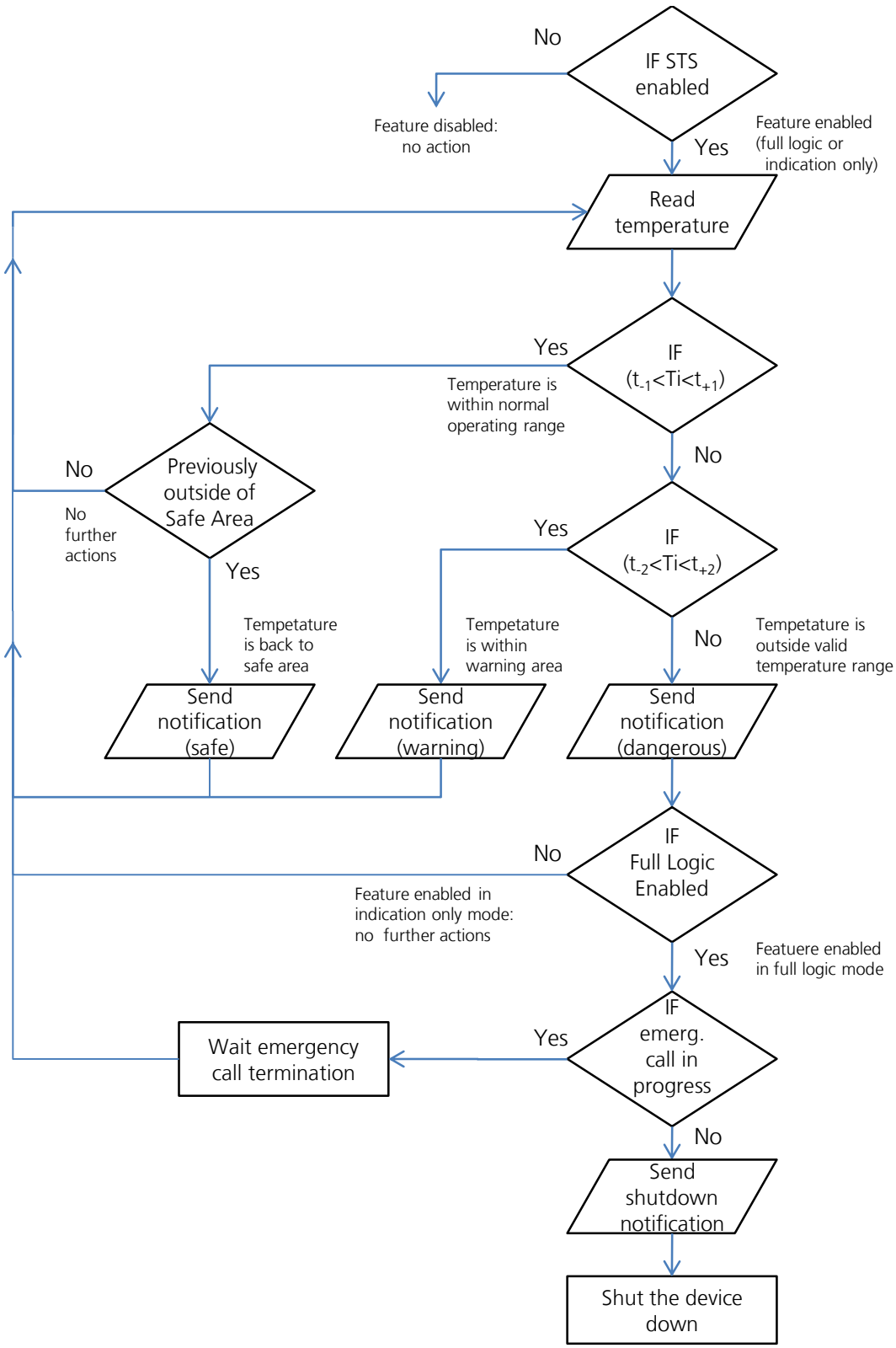


Figure 22: Smart Temperature Supervisor (STS) flow diagram

1.13.8.2 Threshold definitions

When the module application operates at extreme temperatures with Smart Temperature Supervisor enabled, the user should note that outside the valid temperature range the device automatically shuts down as described above.

The input for the algorithm is always the temperature measured within the wireless module (Ti, internal). This value can be higher than the working ambient temperature (Ta, ambient), since (for example) during transmission at maximum power a significant fraction of DC input power is dissipated as heat. This behavior is partially compensated by the definition of the upper shutdown threshold (t_{+2}) that is slightly higher than the declared environmental temperature limit.

Table 12 defines the temperature thresholds.

Symbol	Parameter	Temperature	Remarks
t_{-2}	Low temperature shutdown	–40 °C	Equal to the absolute minimum temperature rating for the wireless module (the lower limit of the extended temperature range)
t_{-1}	Low temperature warning	–30 °C	10 °C above t_{-2}
t_{+1}	High temperature warning	+85 °C	10 °C below t_{+2}. The higher warning area for upper range ensures that any countermeasures used to limit the thermal heating will become effective, even considering some thermal inertia of the complete assembly.
t_{+2}	High temperature shutdown	+95 °C	Equal to the internal temperature Ti measured in the worst case operating condition at typical supply voltage when the ambient temperature Ta in the reference setup (*) equals the absolute maximum temperature rating (upper limit of the extended temperature range)

(*) SARA-G3 series module mounted on a 79 mm x 62 mm x 1.41 mm 4-Layers PCB with a high coverage of copper in still air conditions

Table 12: Thresholds definition for Smart Temperature Supervisor on the SARA-G3 series modules

☞ The sensor measures board temperature inside the shields, which can differ from ambient temperature.

1.13.9 AssistNow clients and GPS/GNSS integration

☞ Not supported by SARA-G300 and SARA-G310 modules.

For customers using u-blox GPS/GNSS receivers, SARA-G350 modules feature embedded AssistNow clients. AssistNow A-GPS provides better GPS/GNSS performance and faster Time-To-First-Fix. The clients can be enabled and disabled with an AT command (see the u-blox AT Commands Manual [2]).

SARA-G350 modules act as a stand-alone AssistNow client, making AssistNow available with no additional requirements for resources or software integration on an external host micro controller. Full access to u-blox positioning receivers is available via the SARA-G350 modules, through a dedicated DDC (I^2C) interface, while the available GPIOs can handle the positioning chipset / module power-on/off. This means that the wireless module and the positioning chips and modules can be controlled through a single serial port from any host processor.

1.13.10 Hybrid positioning and CellLocate™

☞ Not supported by SARA-G300 and SARA-G310 versions.

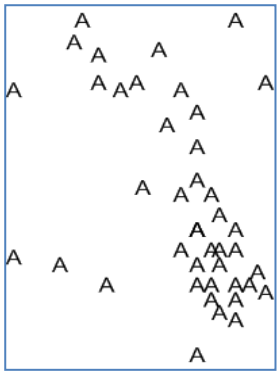
Although GPS/GNSS is a widespread technology, reliance on the visibility of extremely weak GPS/GNSS satellite signals means that positioning is not always possible, particularly in shielded environments such as indoors and enclosed park houses, or when a GPS/GNSS jamming signal is present. The situation can be improved by augmenting GPS/GNSS receiver data with network cell information to provide a level of redundancy that can benefit numerous applications.

1.13.10.1 Positioning through cellular information: CellLocate™

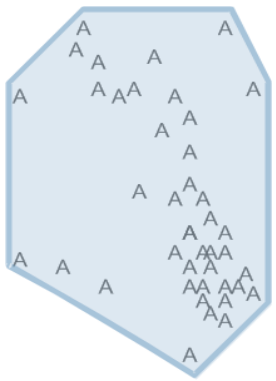
u-blox CellLocate™ enables the device position estimation based on the parameters of the mobile network cells visible to the specific device. To estimate its position the module sends the CellLocate™ server the parameters of network cells visible to it using a UDP connection. In return the server provides the estimated position based on the CellLocate™ database. The SARA-G350 module can either send the parameters of the visible home network cells only (normal scan) or the parameters of all surrounding cells of all mobile operators (deep scan).

The CellLocate™ database is compiled from the position of devices which observed, in the past, a specific cell or set of cells (historical observations) as follows:

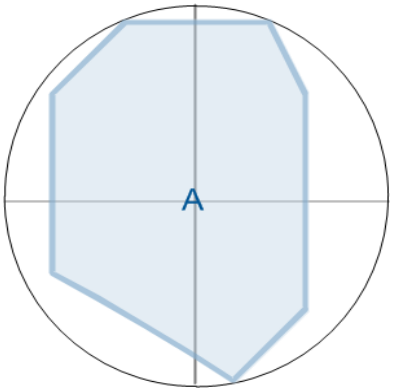
1. Several devices reported their position to the CellLocate server when observing a specific cell (the As in the picture represent the position of the devices which observed the same cell A)



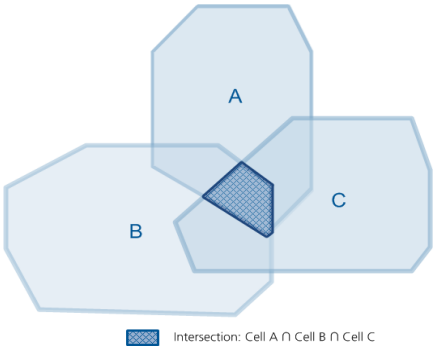
2. CellLocate™ server defines the area of Cell A visibility



3. If a new device reports the observation of Cell A CellLocate™ is able to provide the estimated position from the area of visibility



4. The visibility of multiple cells provides increased accuracy based on the intersection of areas of visibility.



CellLocate™ is implemented using a set of two AT commands that allow configuration of the CellLocate™ service (AT+ULOCCELL) and requesting position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy.

☞ The accuracy of the position estimated by CellLocate™ depends on the availability of historical observations in the specific area.

1.13.10.2 Hybrid positioning

With u-blox hybrid positioning technology, u-blox wireless modules can be triggered to provide their current position using either a u-blox GPS/GNSS receiver or the position estimated from CellLocate. The choice depends on which positioning method provides the best and fastest solution according to the user configuration, exploiting the benefit of having multiple and complementary positioning methods.

Hybrid positioning is implemented through a set of three AT commands that allow GPS/GNSS receiver configuration (AT+ULOCGNSS), CellLocate™ service configuration (AT+ULOCCELL), and requesting the position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy (if the position has been estimated by CellLocate™), and additional parameters if the position has been computed by the GPS/GNSS receiver.

The configuration of mobile network cells does not remain static (e.g. new cells are continuously added or existing cells are reconfigured by the network operators). For this reason, when a hybrid positioning method has been triggered and the GPS/GNSS receiver calculates the position, a database self-learning mechanism has been implemented so that these positions are sent to the server to update the database and maintain its accuracy.

The use of hybrid positioning requires a connection via the DDC (I^2C) bus between the SARA-G350 wireless module and the u-blox GPS/GNSS receiver (Refer to chapter 2.5.3).

Refer to GPS Implementation Application Note [21] for the complete description of the feature.

☞ u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate server u-blox is unable to track the SIM used or the specific device.

1.13.11 Firmware upgrade Over AT (FOAT)

1.13.11.1 Overview

This feature allows upgrading the module Firmware over the UART interface, using AT Commands.

- AT Command AT+UFWUPD triggers a reboot followed by the upgrade procedure at specified a baud rate (refer to u-blox AT Commands Manual [2] for more details)
- Both Xmodem-1k protocol (1024 bytes packets) and Xmodem protocol (128 bytes packets) can be used for downloading the new firmware image via a terminal application
- A special boot loader on the module performs firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the firmware download from the Xmodem-1k handshake. After completing the upgrade, the module is reset again and wakes-up in normal boot

1.13.11.2 FOAT procedure

The application processor must proceed in the following way:

- Send the AT+UFWUPD command through UART interface, specifying the file type and the desired baud rate
- Reconfigure serial communication at selected baud rate, without flow control with the used protocol
- Send the new FW image via the used protocol

For more details, refer to the Firmware Update Application Note [22].

1.13.12 Firmware upgrade Over The Air (FOTA)

☞ Not supported by SARA-G300 and SARA-G310 modules.

☞ Supported upon request on SARA-G350 modules.

This feature allows upgrading the module Firmware over the air, i.e. over the GSM network. The main idea with updating Firmware over the air is to reduce the amount of data required for transmission to the module. This is achieved by downloading only a “delta file” instead of the full firmware. The delta contains only the differences between the two firmware versions (old and new), and is compressed.

For more details, refer to the Firmware Update Application Note [22].

1.13.13 In-Band modem (eCall / ERA-GLONASS)

☞ Supported only by SARA-G350 ECALL module version.

SARA-G350 ECALL module version supports an In-Band modem solution for eCall and ERA-GLONASS emergency call applications over cellular networks, implemented according to 3GPP TS 26.267 [19], BS EN 16062:2011 [26] and ETSI TS 122 101 [27] specifications.

eCall and ERA-GLONASS are respectively a European and Russian initiatives to combine mobile communications and satellite positioning to provide rapid assistance to motorists in the event of a collision, implementing automated emergency response system based the first on GPS the latter on GLONASS positioning system.

When activated, the in-vehicle systems (IVS) automatically initiate an emergency call carrying both voice and data (including location data) directly to the nearest Public Safety Answering Point (PSAP) to determine whether rescue services should be dispatched to the known position.

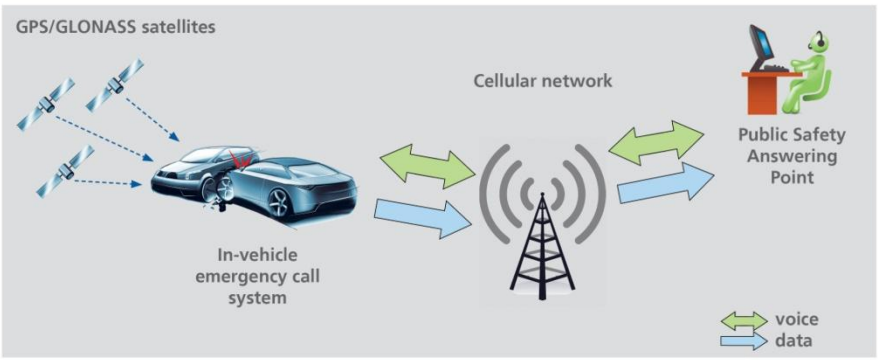


Figure 23: eCall and ERA-GLONASS automated emergency response systems diagram flow

1.13.14 Power saving

The power saving configuration is by default disabled, but it can be enabled using the AT+UPSV command. When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption.

During low power idle-mode, the module is not ready to communicate with an external device by means of the application interfaces, since it is configured to reduce power consumption. It can be woken up from idle-mode to active-mode by the connected application processor, by the connected u-blox positioning receiver or by network activities, as described in the Table 5.

During idle-mode, the module processor core runs with the RTC 32 kHz reference clock, which is generated by:

- The internal 32 kHz oscillator, in case of SARA-G350 modules
- The 32 kHz signal provided at the **EXT32K** input pin, in case of SARA-G300 and SARA-G310 modules

☞ SARA-G300 and SARA-G310 need a 32 kHz signal at **EXT32K** input to reach the low power idle-mode.

For the complete description of the AT+UPSV command, refer to the u-blox AT Commands Manual [2].

For the definition and the description of SARA-G3 series modules operating modes, including the events forcing transitions between the different operating modes, refer to the chapter 1.4.

For the description of current consumption in idle and active operating modes, refer to chapters 1.5.1.2, 1.5.1.4.

For the description of the UART settings related to module power saving configuration, refer to chapter 1.9.1.4.

For the description of the **EXT32K** input and relative application circuit design-in, refer to chapters 1.6.4, 2.2.3.

2 Design-in

For an optimal integration of SARA-G3 modules in the final application board follow the design guidelines stated in this chapter.

Every application circuit must be properly designed to guarantee the correct functionality of the relative interface, however a number of points require high attention during the design of the application device.

The following list provides a ranking of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT** and **ANT_DET** pins. Antenna circuit directly affects the RF compliance of the device integrating SARA-G3 module with applicable certification schemes. Very carefully follow the suggestions provided in the relative chapter 2.3 for schematic and layout design.
2. Module supply: **VCC** and **GND** pins. The supply circuit affects the RF compliance of the device integrating SARA-G3 module with applicable required certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in the relative chapter 2.1.1 for schematic and layout design.

3. SIM card interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**, **SIM_DET** pins. Accurate design is required to guarantee SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in the relative chapter 2.4 for schematic and layout design.
4. System functions: **RESET_N**, **PWR_ON** pins. Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in the relative chapter 2.2 for schematic and layout design.
5. Analog audio interface: **MIC_BIAS**, **MIC_GND**, **MIC_P**, **MIC_N** uplink and **SPK_P**, **SPK_N** downlink pins. Accurate design is required to obtain clear and high quality audio reducing the risk of noise from audio lines due to both supply burst noise coupling and RF detection. Carefully follow the suggestions provided in the relative chapter 2.6.1 for schematic and layout design.
6. External 32 kHz input: the **EXT32K** input pin of SARA-G300 and SARA-G310 modules requires accurate layout design as it may affect the stability of the RTC timing reference. Carefully follow the suggestions provided in the relative chapter 2.2.3 for schematic and layout design.

7. Other digital interfaces: UART and auxiliary UART interfaces, DDC I^2C-compatible interface, digital audio interface and GPIOs. Accurate design is required to guarantee proper functionality. Follow the suggestions provided in the relative chapters 2.5.1, 2.5.2, 2.5.3, 2.6.2 and 2.7 for schematic and layout design.
8. Other supplies: the **V_BCKP** RTC supply input/output and the **V_INT** digital interfaces supply output. Accurate design is required to guarantee proper functionality. Follow the suggestions provided in the relative chapters 2.1.2 and 2.1.3 for schematic and layout design.

2.1 Supply interfaces

2.1.1 Module supply (VCC)

2.1.1.1 General guidelines for VCC supply circuit selection and design

VCC pins are internally connected, but connect all the available pads to the external supply to minimize the power loss due to series resistance.

GND pins are internally connected but connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-G3 modules must be supplied through the **VCC** pins by a proper DC power supply that should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6.

The proper DC power supply can be selected according to the application requirements (see Figure 24) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

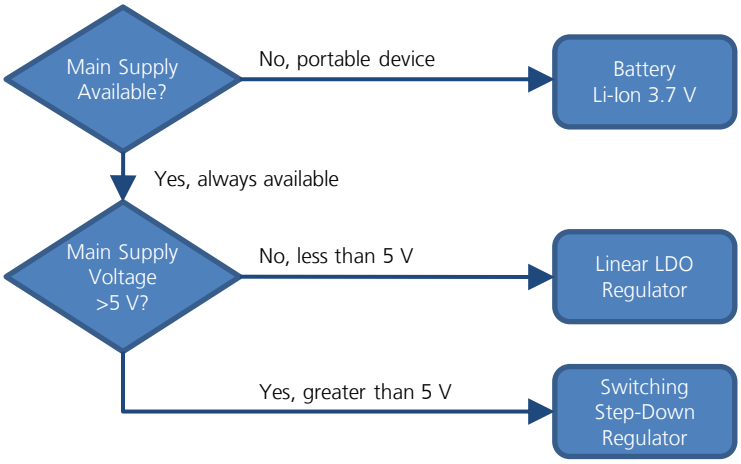


Figure 24: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the SARA-G3 modules operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power.

If SARA-G3 modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided.

The use of primary (not rechargeable) battery is uncommon, since the most cells available are seldom capable of delivering the burst peak current for a GSM call due to high internal resistance.

Keep in mind that the use of batteries requires the implementation of a suitable charger circuit (not included in SARA-G3 modules). The charger circuit should be designed in order to prevent over-voltage on **VCC** beyond the upper limit of the absolute maximum rating.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The usage of a regulator or a battery not able to withstand the maximum peak current consumption specified in the SARA-G3 series Data Sheet [1] is generally not recommended. However, if the selected regulator or battery is not able to withstand the maximum peak current of the module, it must be able to considerably withstand at least the maximum average current consumption value specified in the SARA-G3 series Data Sheet [1], and the additional energy required by the module during a GSM/GPRS Tx slot (when the current consumption can rise up to 1.9 A in the worst case, as described in section 1.5.1.2) could be provided by a proper bypass tank capacitor with very large capacitance and very low ESR (depending on the actual capability of the selected regulator or battery, the required capacitance can be considerably larger than 1 mF) placed close to the module **VCC** pins. Carefully evaluate the implementation of this solution since the aging and temperature conditions highly affects the actual capacitors characteristics.

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 6.

2.1.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering 1.9 A current pulses with 1/8 duty cycle to the **VCC** pins
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile
- **High switching frequency:** for best performance and for smaller applications select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile and therefore negatively impact GSM modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple on **VCC**, but adds extra voltage drop due to resistive losses on series inductors
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected-mode Pulse Frequency Modulation (PFM) mode and PFM/PWM mode, transitions must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators that are able to switch between low ripple PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition occurs when the module changes status from idle/active-mode to connected-mode (where current consumption increases to a value greater than 100 mA): it is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 60 mA)
- **Output voltage slope**: the use of the soft start function provided by some voltage regulators should be carefully evaluated, since the **VCC** pins voltage must ramp from 2.5 V to 3.2 V within 4 ms to switch on the module that otherwise can be switched on by a low level on **PWR_ON** pin

Figure 25 and the components listed in Table 13 show an example of a high reliability power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering 1.9 A current pulses with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

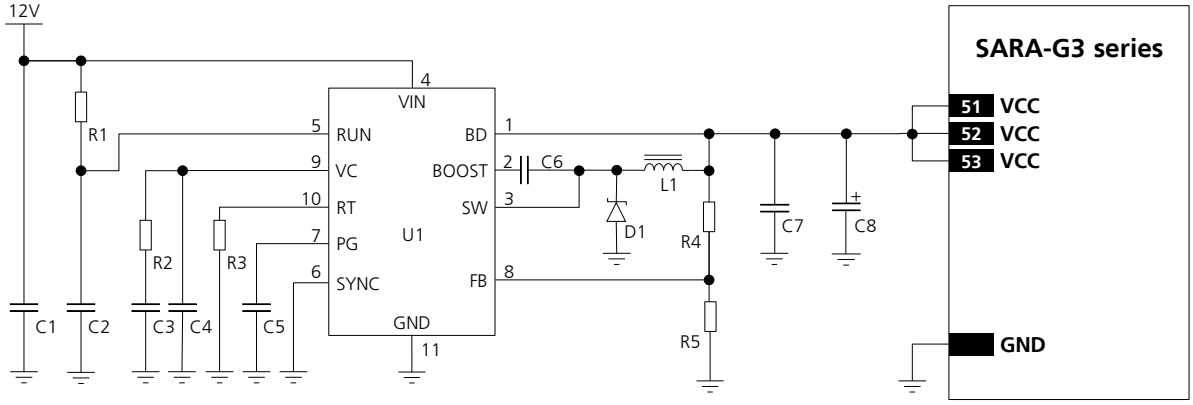


Figure 25: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 kΩ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	22 kΩ Resistor 0402 5% 0.1 W	2322-705-87223-L - Yageo
R4	390 kΩ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 kΩ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step-Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 13: Suggested components for the VCC voltage supply application circuit using a step-down regulator

Figure 26 and the components listed in Table 14 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable of delivering 1.9 A current pulses, transforming a 12 V supply input.

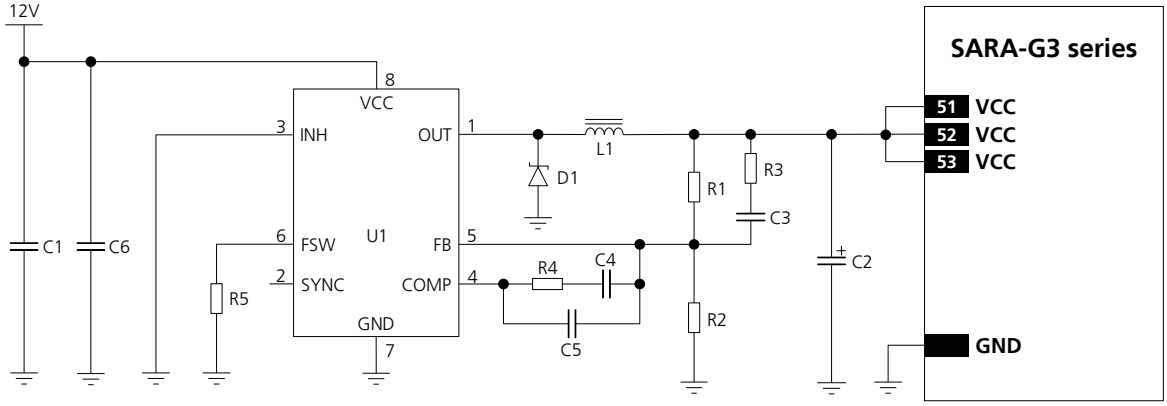


Figure 26: Suggested low cost solution for the VCC voltage supply application circuit using step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 – Murata
C2	100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 – Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 – Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H560JA01 – Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 – Murata
D1	Schottky Diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ Resistor 0402 1% 0.063 W	RC0402FR-074K7L – Yageo
R2	910 Ω Resistor 0402 1% 0.063 W	RC0402FR-07910RL – Yageo
R3	82 Ω Resistor 0402 5% 0.063 W	RC0402JR-0782RL – Yageo
R4	8.2 kΩ Resistor 0402 5% 0.063 W	RC0402JR-078K2L – Yageo
R5	39 kΩ Resistor 0402 5% 0.063 W	RC0402JR-0739KL – Yageo
U1	Step-Down Regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 14: Suggested components for low cost solution VCC voltage supply application circuit using a step-down regulator

2.1.1.3 Guidelines for VCC supply circuit design using a Low Drop-Out (LDO) linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pins and of delivering 1.9 A current pulses with 1/8 duty cycle
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator)
- **Output voltage slope**: the use of the soft start function provided by some voltage regulator should be carefully evaluated, since the **VCC** pins voltage must ramp from 2.5 V to 3.2 V within 4 ms to switch-on the module that otherwise can be switched on by a low level on **PWR_ON** pin

Figure 27 and the components listed in Table 15 show an example of a power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering 1.9 A current pulses, with proper power handling capability.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module VCC normal operating range (e.g. ~4.1 V as in the circuit described in Figure 27 and Table 15). This reduces the power on the linear regulator and improves the thermal design of the supply circuit.

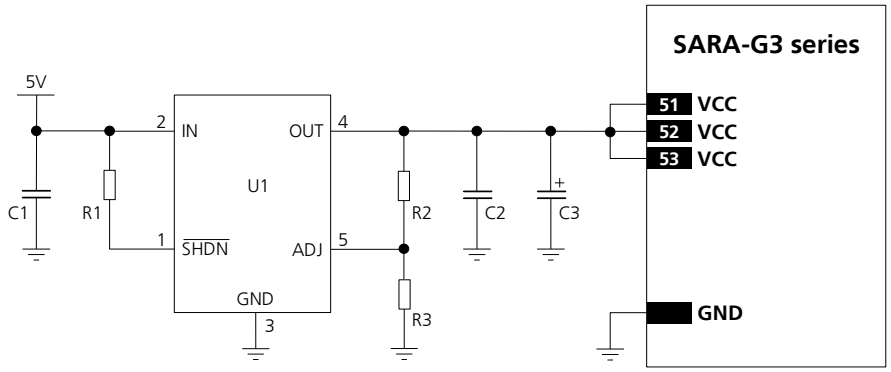


Figure 27: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C3	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	9.1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-079K1L - Yageo Phycomp
R3	3.9 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K9L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 15: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

2.1.1.4 Guidelines for VCC supply circuit design using a rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its output circuit must be capable of delivering 1.9 A current pulses with 1/8 duty-cycle to the **VCC** pins and must be capable of delivering a DC current greater than the module maximum average current consumption to **VCC** pins. The maximum pulse discharge current and the maximum DC discharge current are not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts

2.1.1.5 Guidelines for VCC supply circuit design using a primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its output circuit must be capable of delivering 1.9 A current pulses with 1/8 duty-cycle to the **VCC** pins and must be capable of delivering a DC current greater than the module maximum average current consumption at the **VCC** pins. The maximum pulse and the maximum DC discharge current is not always reported in battery data sheets,

but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour

- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 400 mV during transmit bursts

2.1.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated for **VCC** supply. Another twenty pins are designated for **GND** connection. Even if all the **VCC** pins and all the **GND** pins are internally connected within the module, it is recommended to properly connect all of them to supply the module to minimize series resistance losses.

To avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a GSM call (when current consumption on the **VCC** supply can rise up to as much as 1.9 A in the worst case), place a bypass capacitor with large capacitance (more than 100 µF) and low ESR near the **VCC** pins, for example:

- 330 µF capacitance, 45 mΩ ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

The use of very large capacitors (i.e. greater then 1000 µF) on the **VCC** line should be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 4 ms to switch on the module that otherwise can be switched on by a low level on **PWR_ON** pin.

To reduce voltage ripple and noise, especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 100 nF capacitor (e.g Murata GRM155R61C104K) to filter digital logic noise from clocks and data sources
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 56 pF capacitor with Self-Resonant Frequency in 800/900 MHz range (e.g. Murata GRM1555C1E560J) to filter transmission EMI in the GSM/EGSM bands
- 15 pF capacitor with Self-Resonant Frequency in 1800/1900 MHz range (e.g. Murata GRM1555C1E150J) to filter transmission EMI in the DCS/PCS bands

Figure 28 shows the complete configuration but the mounting of each single component depends on the application design: it is recommended to provide all the **VCC** bypass capacitors as described in Figure 28 and Table 16 if the application device integrates an internal antenna.

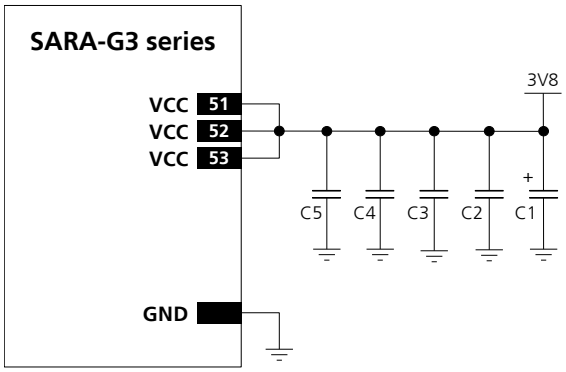


Figure 28: Suggested schematic and layout design for the VCC bypass capacitors to reduce ripple / noise on VCC voltage profile and to avoid undershoot / overshoot on VCC voltage drops

Reference	Description	Part Number - Manufacturer
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C3	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata

Table 16: Suggested components to reduce ripple / noise on VCC and to avoid undershoot/ overshoot on VCC voltage drops

ESD sensitivity rating of the **VCC** supply pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to **VCC** pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

2.1.1.7 Guidelines for external battery charging circuit

SARA-G3 modules do not have an on-board charging circuit. Figure 29 provides an example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the **VCC** supply input of SARA-G3 module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA)
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Alternatively the L6924U, providing input voltage range up to 12 V, can charge from an AC wall adapter. When a current-limited adapter is used, it can operate in quasi-pulse mode, reducing power dissipation.

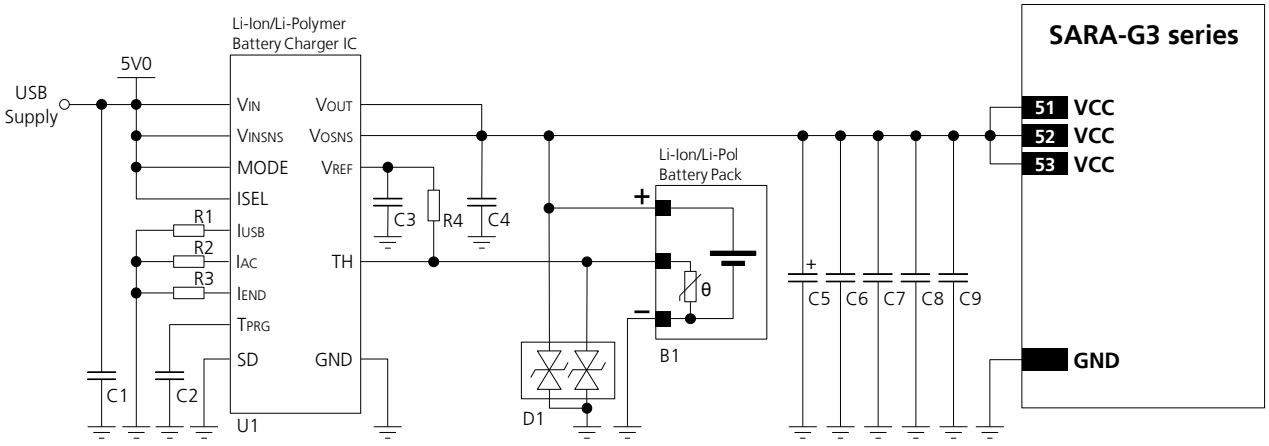


Figure 29: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Various manufacturer
C1, C4	1 µF Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C9	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
D1	Low Capacitance ESD Protection	USB0002RP or USB0002DP - AVX
R1, R2	24 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0724KL - Yageo Phycomp
R3	3.3 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K3L - Yageo Phycomp
R4	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC for USB port and AC Adapter	L6924U - STMicroelectronics

Table 17: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit

2.1.1.8 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source
- **VCC** connection must be as wide as possible and as short as possible
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided
- **VCC** connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing
- Coupling between **VCC** and audio lines (especially microphone inputs) must be avoided, because the typical GSM burst has a periodic nature of approx. 217 Hz, which lies in the audible audio range
- The tank bypass capacitor with low ESR for current spikes smoothing described in Figure 28 and Table 16 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and SARA-G3 module tank capacitor
- The bypass capacitors in the pF range described in Figure 28 and Table 16 should be placed as close as possible to the **VCC** pins. This is highly recommended if the application device integrates an internal antenna
- Since **VCC** is directly connected to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-G3 series modules in the worst case
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the SARA-G3 module, preferably closer to the DC source (otherwise protection functionality may be compromised)

2.1.1.9 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer

- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source
- If the application board is a multilayer PCB, then it is required to connect together each GND area with complete via stack down to main board ground layer
- It is recommended to implement one layer of the application board as ground plane as wide as possible
- Good grounding of **GND** pads also ensures thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating

2.1.2 RTC supply (V_BCKP)

2.1.2.1 Guidelines for V_BCKP circuit design

If RTC timing is required to run for a time interval of T [s] at 25 °C when **VCC** supply is removed, place a capacitor with a nominal capacitance of C [µF] at the **V_BCKP** pin. Choose the capacitor using the following formula:

C [µF] = (Current_Consumption [µA] x T [s]) / Voltage_Drop [V]

= 1.5 x T [s]

For example, a 100 µF capacitor (such as the Murata GRM43SR60J107M) can be placed at **V_BCKP** to provide a long buffering time. This capacitor holds **V_BCKP** voltage within its valid range for around 50 s at 25 °C, after the **VCC** supply is removed. If a very long buffering time is required, a 70 mF super-capacitor (e.g. Seiko Instruments XH414H-IV01E) can be placed at **V_BCKP**, with a 4.7 kΩ series resistor to hold the **V_BCKP** voltage within its valid range for approximately 10 hours at 25 °C, after the **VCC** supply is removed. The purpose of the series resistor is to limit the capacitor charging current due to the large capacitor specifications, and also to let a fast rise time of the voltage value at the **V_BCKP** pin after **VCC** supply has been provided. These capacitors allow the time reference to run during battery disconnection.

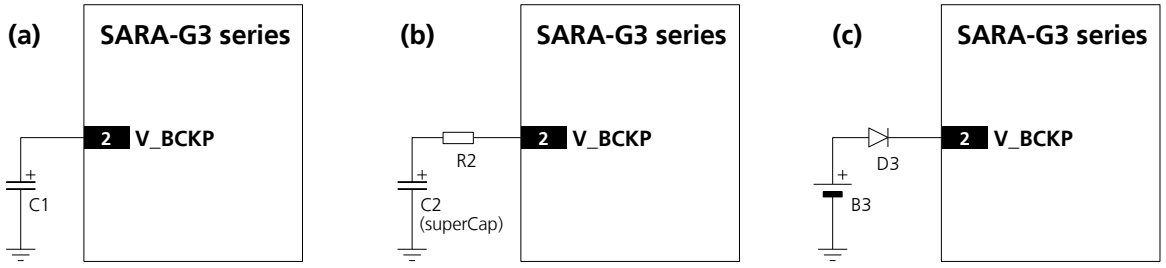


Figure 30: Real time clock supply (V_BCKP) application circuits: (a) using a 100 µF capacitor to let the RTC run for ~50 s after VCC removal; (b) using a 70 mF capacitor to let RTC run for ~10 hours after VCC removal; (c) using a non-rechargeable battery

Reference	Description	Part Number - Manufacturer
C1	100 µF Tantalum Capacitor	GRM43SR60J107M - Murata
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C2	70 mF Capacitor	XH414H-IV01E - Seiko Instruments

Table 18: Example of components for V_BCKP buffering

If longer buffering time is required to allow the RTC time reference to run during a disconnection of the **VCC** supply, then an external battery can be connected to **V_BCKP** pin. The battery should be able to provide a proper nominal voltage and must never exceed the maximum operating voltage for **V_BCKP** (specified in the Input characteristics of Supply/Power pins table in SARA-G3 series Data Sheet [1]). The connection of the battery

to **V_BCKP** should be done with a suitable series resistor for a rechargeable battery, or with an appropriate series diode for a non-rechargeable battery. The purpose of the series resistor is to limit the battery charging current due to the battery specifications, and also to allow a fast rise time of the voltage value at the **V_BCKP** pin after the **VCC** supply has been provided. The purpose of the series diode is to avoid a current flow from the module **V_BCKP** pin to the non-rechargeable battery.

☞ If the RTC timing is not required when the **VCC** supply is removed, it is not needed to connect the **V_BCKP** pin to an external capacitor or battery. In this case the date and time are not updated when **VCC** is disconnected. If **VCC** is always supplied, then the internal regulator is supplied from the main supply and there is no need for an external component on **V_BCKP**.

Combining a SARA-G3 wireless module with a u-blox GPS/GNSS positioning receiver, the positioning receiver **VCC** supply is controlled by the wireless module by means of the "GPS supply enable" function provided by the **GPIO2** of the wireless module. In this case the **V_BCKP** supply output of the SARA-G3 wireless module can be connected to the **V_BCKP** backup supply input pin of the GPS/GNSS receiver to provide the supply for the positioning real time clock and backup RAM when the **VCC** supply of the wireless module is within its operating range and the **VCC** supply of the GPS/GNSS receiver is disabled. This enables the u-blox GPS/GNSS receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the positioning **VCC** outage) and to maintain the configuration settings saved in the backup RAM. Refer to section 2.5.3 for more details regarding the application circuit with a u-blox GPS/GNSS receiver.

On SARA-G300 and SARA-G310 modules, the **V_BCKP** supply output can be used to supply an external 32 kHz oscillator which provides a 32 kHz signal to the **EXT32K** input pin as reference clock for the RTC timing, so that the modules can enter the low power idle-mode and can make available the RTC functions.

☞ The internal regulator for **V_BCKP** is optimized for low leakage current and very light loads. Do not apply loads which might exceed the limit for maximum available current from **V_BCKP** supply, as this can cause malfunctions in the module. SARA-G3 series Data Sheet [1] describes the detailed electrical characteristics.

V_BCKP supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ ESD sensitivity rating of the **V_BCKP** supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible back-up battery connector is directly connected to **V_BCKP** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

2.1.2.2 Guidelines for V_BCKP layout design

RTC supply (**V_BCKP**) requires careful layout: avoid injecting noise on this voltage domain as it may affect the stability of the 32 kHz oscillator.

2.1.3 Interface supply (V_INT)

2.1.3.1 Guidelines for V_INT circuit design

The **V_INT** digital interfaces 1.8 V supply output can be mainly used to:

- Pull-up DDC (I^2C) interface signals (see section 2.5.3 for more details)
- Pull-up SIM detection signal (see section 2.4 for more details)
- Supply voltage translators to connect digital interfaces of the module to a 3.0 V device (see section 2.5.1)
- Supply a 1.8 V u-blox 6 or subsequent GPS/GNSS receiver (see section 2.5.3 for more details)
- Indicate when the module is switched on

☞ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply, as this can cause malfunctions in internal circuitry supplies to the same domain. SARA-G3 series Data Sheet [1] describes the detailed electrical characteristics.

☞ **V_INT** can only be used as an output; do not connect any external regulator on **V_INT**.

Since the **V_INT** supply is generated by an internal switching step-down regulator, the **V_INT** voltage ripple can range from 15 mVpp during active-mode or connected-mode (when the switching regulator operates in PWM mode), to 90 mVpp in idle-mode (when the switching regulator operates in PFM mode).

☞ It is not recommended to supply sensitive analog circuitry without adequate filtering for digital noise.

V_INT supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

☞ If the **V_INT** supply output is not required by the customer application, since DDC (I^2C) interface and SIM detection functions are not used and voltage translation of digital interfaces are not needed, the **V_INT** pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint directly connected to the **V_INT** pin.

2.1.3.2 Guidelines for V_INT layout design

V_INT digital interfaces supply output is generated by an integrated switching step-down converter, used internally to supply the digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

2.2 System functions interfaces

2.2.1 Module power-on (PWR_ON)

2.2.1.1 Guidelines for PWR_ON circuit design

Connecting the **PWR_ON** input to a push button that shorts the **PWR_ON** pin to ground, provide an external pull-up resistor (e.g. 100 kΩ) biased by the **V_BCKP** supply pin of the module, as described in Figure 31 and Table 19. Connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device: according to EMC/ESD requirements of the application, provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point.

The **PWR_ON** pin has high input impedance and is weakly pulled to the high level on the module. Avoid keeping it floating in a noisy environment. To hold the high logic level stable, the **PWR_ON** pin must be connected to a pull-up resistor (e.g. 100 kΩ) biased by the **V_BCKP** supply pin of the module.

ESD sensitivity rating of the **PWR_ON** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **PWR_ON** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

Connecting the **PWR_ON** input to an external device (e.g. application processor), use an open drain output on the external device with an external pull-up resistor (e.g. 100 kΩ) biased by the **V_BCKP** supply pin of the module, as described in Figure 31 and Table 19.

A compatible push-pull output of an application processor can also be used: in this case the pull-up can be provided to pull the **PWR_ON** level high when the application processor is switched off. If the high-level voltage of the push-pull output pin of the application processor is greater than the maximum input voltage operating range of the **V_BCKP** pin (refer to SARA-G3 series Data Sheet [1]), the **V_BCKP** supply cannot be used to bias the pull-up resistor: the supply rail of the application processor or the module **VCC** supply could be used, but this increases the **V_BCKP** (RTC supply) current consumption when the module is in not-powered mode (**VCC** supply not present). Using a push-pull output of the external device, take care to fix the proper level in all the possible scenarios to avoid an inappropriate module switch-on.

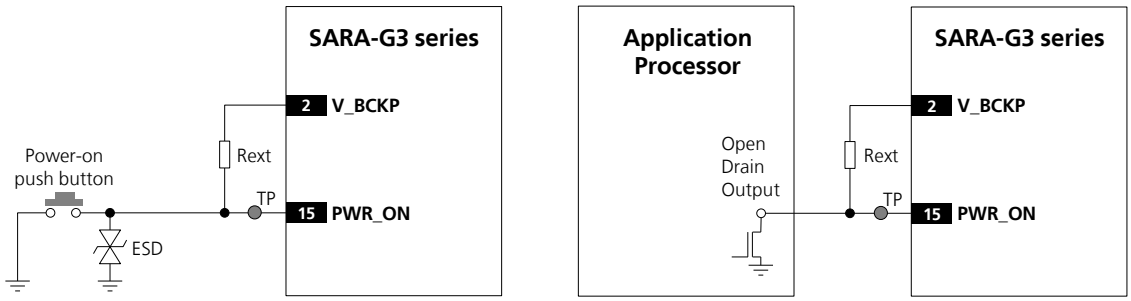


Figure 31: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
Rext	100 kΩ Resistor 0402 5% 0.1 W	External pull-up resistor
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 19: Example of pull-up resistor and ESD protection for the PWR_ON application circuit

It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of accessible testpoint directly connected to the **PWR_ON** pin.

2.2.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout since it is the sensitive input available to switch on the SARA-G3 modules until a valid **VCC** supply is provided after that the module has been switched off by means of the AT+CPWROFF command: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.2.2 Module reset (RESET_N)

2.2.2.1 Guidelines for RESET_N circuit design

As described in Figure 13, the module has an internal pull-up resistor on the reset input line: an external pull-up is not required on the application board.

Connecting the **RESET_N** input to a push button that shorts the **RESET_N** pin to ground, the pin will be externally accessible on the application device: according to EMC/ESD requirements of the application, provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point, as described in Figure 32 and Table 20.

ESD sensitivity rating of the **RESET_N** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **RESET_N** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

Connecting the **RESET_N** input to an external device (e.g. application processor), an open drain output can be directly connected without any external pull-up, as described in Figure 32 and Table 20: the internal pull-up resistor provided by the module pulls the line to the high logic level when the **RESET_N** pin is not forced low by the application processor. A compatible push-pull output of an application processor can be used too.

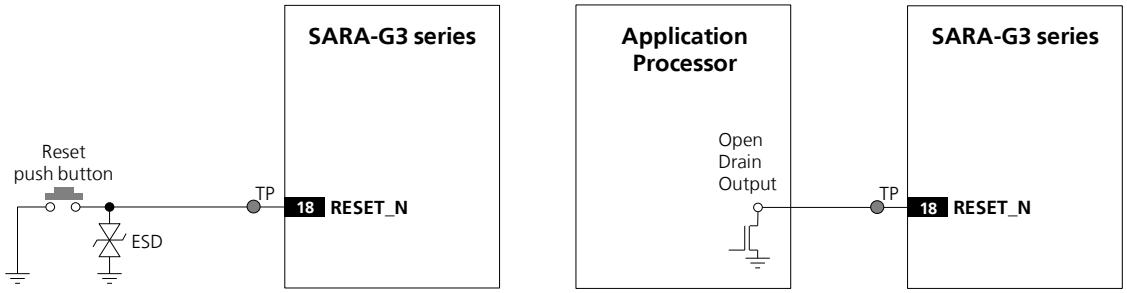


Figure 32: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 20: Example of ESD protection component for the RESET_N application circuit

If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint directly connected to the **RESET_N** pin.

2.2.2.2 Guidelines for RESET_N layout design

The reset circuit (**RESET_N**) requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** as short as possible.

2.2.3 External 32 kHz signal input (EXT32K)

2.2.3.1 Guidelines for EXT32K circuit design

The application circuit of Figure 33 and Table 21 describe how to provide a 32.768 kHz square wave from an external oscillator to the **EXT32K** input pin of SARA-G300 and SARA-G310 modules, as reference clock for the Real Time Clock timing, so that the modules can enter the low power idle-mode and can provide RTC functions. As alternative solution, a reference signal with proper frequency and voltage levels can be provided by the used application processor, if capable, instead of using a dedicated stand-alone oscillator.

SARA-G350 modules do not provide **EXT32K** input pin since the 32 kHz reference clock for the Real Time Clock (RTC) timing is generated by the available internal oscillator.

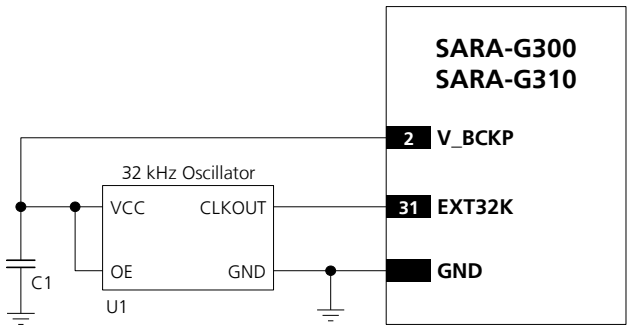


Figure 33: EXT32K application circuit using an external 32 kHz oscillator

Reference	Description	Remarks
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Low Power Clock Oscillator 32.768 kHz	OV-7604-C7 - Micro Crystal or SG-3040LC - EPSON TOYOCOM

Table 21: Example of components for the EXT32K application circuit

ESD sensitivity rating of the **EXT32K** input pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

If the low power idle-mode and the RTC functions are not required by the customer application, the **EXT32K** input pin can be left not connected.

2.2.3.2 Guidelines for EXT32K layout design

The external 32 kHz (**EXT32K**) input pin requires accurate layout design: avoid injecting noise on this pin as it may affect the stability of the RTC timing reference.

2.3 Antenna interface

The **ANT** pin, provided by all SARA-G3 modules, represents the main RF input/output used to transmit and receive the GSM/GPRS RF signal: the main antenna must be connected to this pad. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the 2G and 3G operating bands.

2.3.1 Antenna RF interface (ANT)

2.3.1.1 General guidelines for antenna selection and design

The GSM antenna is the most critical component to be evaluated: care must be taken about it at the start of the design development, when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating SARA-G3 module with all the applicable required certification schemes depends from antenna radiating performance.

GSM antennas are typically available as:

- Linear monopole / External antenna:
  - External antenna usage basically does not imply physical restriction to the design of the PCB where the SARA-G3 series module is mounted
  - The radiation performance mainly depends on the antenna: select the antenna with optimal radiating performance in the operating bands
  - If antenna detection functionality is required, select an antenna assembly provided with a proper built-in diagnostic circuit with a resistor connected to ground: refer to guidelines in section 2.3.2
  - Select an RF cable with minimum insertion loss: additional insertion loss due to low quality or long cable reduces radiation performance
  - Select a suitable 50 Ω connector providing proper PCB-to-RF-cable transition: it is recommended to strictly follow the layout guidelines provided by the connector manufacturer
- Patch-like antenna / Integrated antenna:
  - Internal integrated antenna implies physical restriction to the design of the PCB: the ground plane can be reduced down to a minimum size that must be similar to the quarter of the wavelength of the minimum frequency that has to be radiated. As numerical example:

    Frequency = 1 GHz → Wavelength = 30 cm → Minimum GND plane size = 7.5 cm
  - The radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage: select the antenna with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product
  - Select a complete custom antenna designed by an antenna manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide): the antenna design process should begin at the start of the whole product design process
  - Select an integrated antenna solution provided by an antenna manufacturer if the required ground plane dimensions are enough large according to the relative integrated antenna solution specifications: the antenna selection and the definition of its placement in the product layout should begin at the start of the product design process
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry
  - Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes: it is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application

In both cases, selecting an external or an internal antenna, observe these recommendations:

- Select an antenna providing optimal return loss (or V.S.W.R.) figure over all the operating frequencies
- Select an antenna providing optimal efficiency figure over all the operating frequencies
- Select an antenna providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States, as reported in the chapter 4.2.2)

2.3.1.2 Guidelines for antenna RF interface design

Guidelines for ANT pin RF connection design

Proper transition between the **ANT** pad and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** pad:

- On a multi layer board, the whole layer stack below the RF connection should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** pad, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 34
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 34

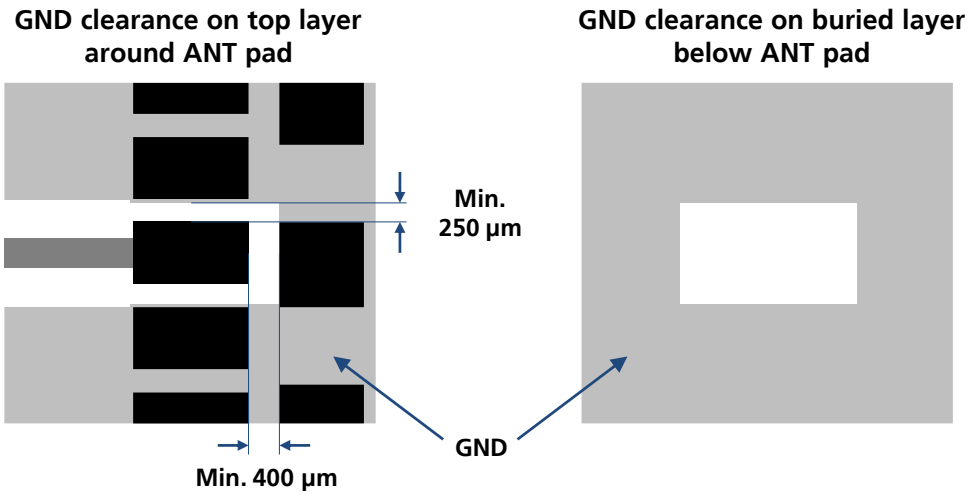


Figure 34: GND keep-out area on the top layer around ANT pad and on the very close buried layer below ANT pad

Guidelines for RF transmission line design

The transmission line from the **ANT** pad up to antenna connector or up to the internal antenna pad must be designed so that the characteristic impedance is as close as possible to 50 Ω.

The transmission line can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 35 and Figure 36 provide two examples of proper 50 Ω coplanar waveguide designs: the first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

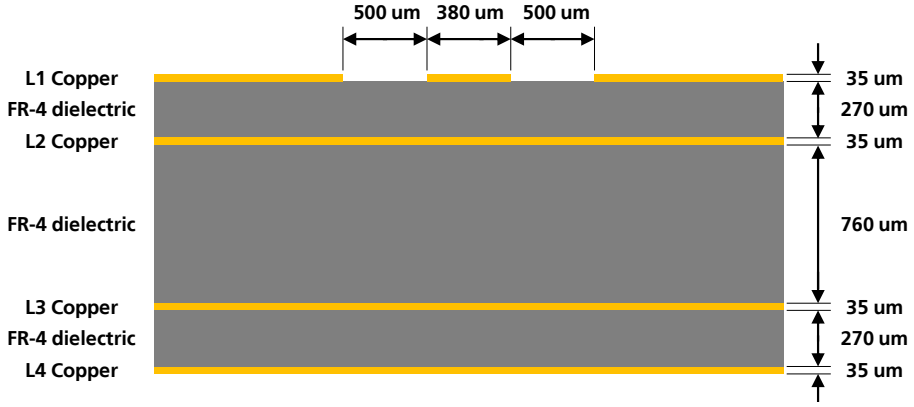


Figure 35: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

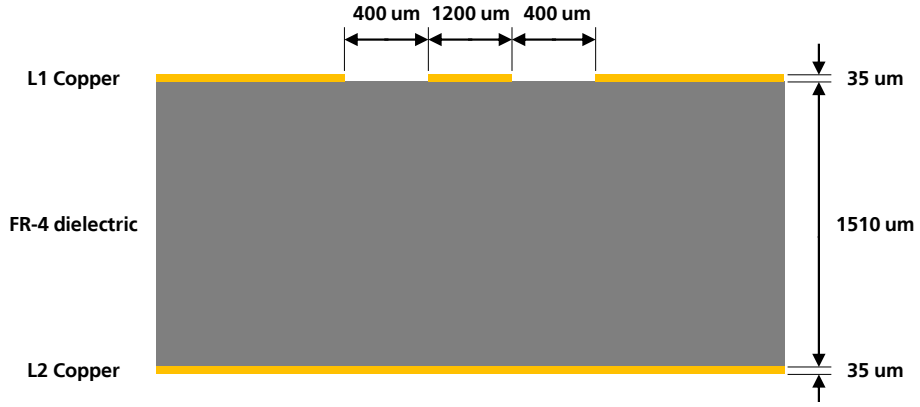


Figure 36: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB layup, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent or TXLine from Applied Wave Research, taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 35 and Figure 36)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 35, 1510 µm in Figure 36)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 35 and Figure 36)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 35, 400 µm in Figure 36)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for the transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground
- The transmission line width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND
- Add GND vias around transmission line, as described in Figure 37
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough on the adjacent metal layer, as described in Figure 37
- Route RF transmission line far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as analog audio lines)
- Avoid stubs on the transmission line
- Avoid signal routing in parallel to transmission line or crossing the transmission line on buried metal layer
- Do not route microstrip line below discrete component or other mechanics placed on top layer

An example of proper RF circuit design is reported in the Figure 37. In this case, the antenna detection circuit is not implemented: the **ANT** pin is directly connected to an SMA connector by means of a proper 50 Ω transmission line, designed with proper layout.

If the antenna detection function is required by the application, follow the guidelines for circuit and layout implementation reported in section 2.3.2.

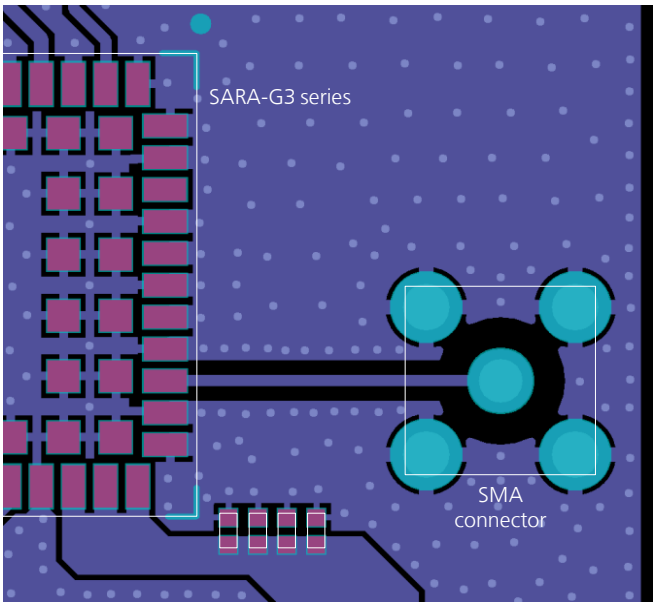


Figure 37: Suggested circuit and layout for antenna RF circuit on application board, if antenna detection is not required

Guidelines for RF termination design

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination itself, to match the characteristic impedance of the **ANT** pin of SARA-G3 modules.

However, real antennas have no perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antenna mismatch, the RF termination must provide optimal return loss (or V.S.W.R.) figure over all the operating frequency bands, as summarized in Table 8.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing proper PCB-to-RF-cable transition
- Strictly follow the connector manufacturer's recommended layout, for example:
    - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts, as shown in Figure 37
    - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads
- Cut out the GND layer under RF connectors and close to buried vias, to remove stray capacitance and thus keep the RF line 50 Ω: e.g. the active pad of U.FL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on first inner layer to reduce parasitic capacitance to ground

If an integrated antenna is used, the RF termination is represented by the integrated antenna itself:

- Use an antenna designed by an antenna manufacturer, providing the best possible return loss (or V.S.W.R.)
- Provide a ground plane enough large according to the relative integrated antenna requirements: the ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. As numerical example

  Frequency = 1 GHz → Wavelength = 30 cm → Minimum GND plane size = 7.5 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes: it is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna matching relative to the custom application

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not include antenna within closed metal case
- Do not place the antenna in close vicinity to end user since the emitted radiation in human tissue is limited by regulatory requirements
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues
- Take care of interaction between co-located RF systems since the GSM transmitted power may interact or disturb the performance of companion systems

2.3.2 Antenna detection interface (ANT_DET)

2.3.2.1 Guidelines for ANT_DET circuit design

Figure 38 and Table 22 describe the recommended schematic and components for the antenna detection circuit to be provided on the application board for the diagnostic circuit that must be provided on the antenna assembly to achieve antenna detection functionality.

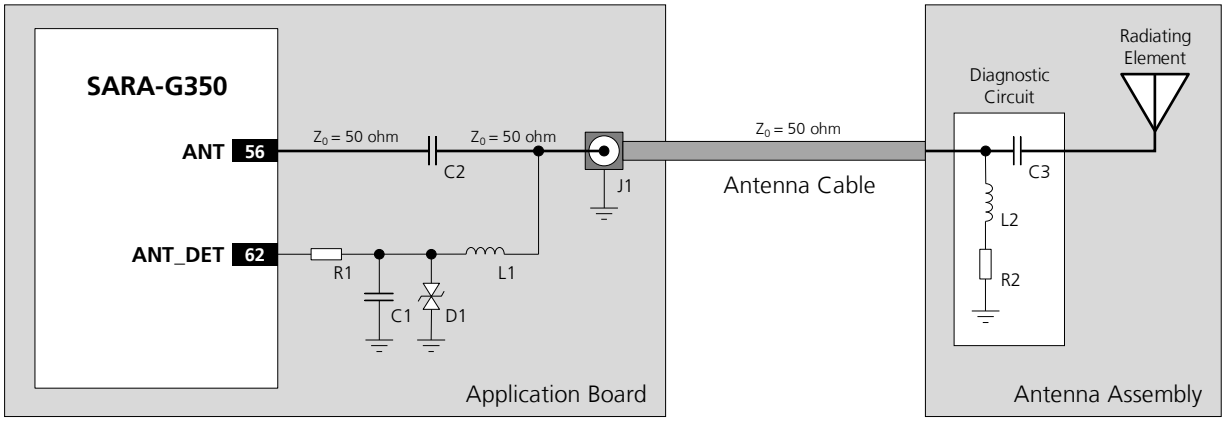


Figure 38: Suggested schematic for antenna detection circuit on application board and diagnostic circuit on antenna assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C3	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L2	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 22: Suggested components for antenna detection circuit on application board and diagnostic circuit on antenna assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 38 and Table 22 are here explained:

- When antenna detection is forced by the +UANTR AT command, the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C3) to decouple the DC current generated by the **ANT_DET** pin
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L2), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 38) are needed at the **ANT_DET** pin as ESD protection
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 38, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider a GSM antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see u-blox AT Commands Manual [2]) means that that the antenna is not connected or the RF cable is broken
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 37.

2.3.2.1 Guidelines for ANT_DET layout design

Figure 39 describes the recommended layout for the antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in Figure 38 and Table 22.

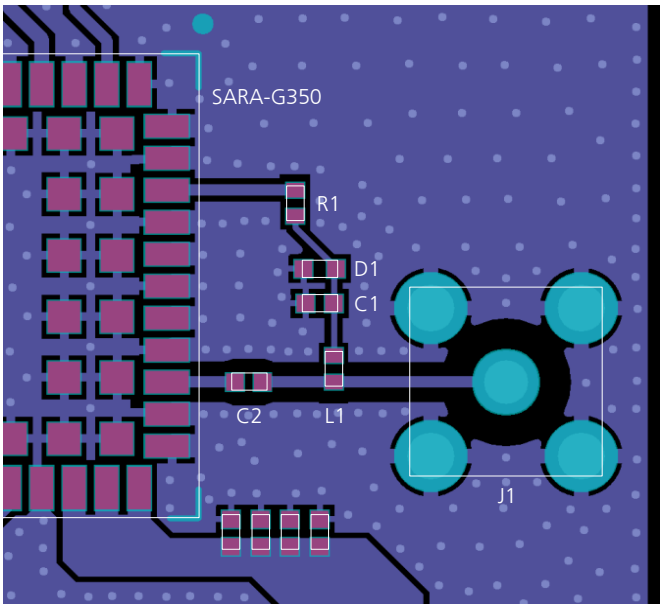


Figure 39: Suggested layout for antenna detection circuit on application board

The antenna detection circuit layout suggested in Figure 39 is here explained:

- The **ANT** pin is connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.3.1 and the recommendations of the SMA connector manufacturer
- DC blocking capacitor at the **ANT** pin (C2) is placed in series to the 50 Ω transmission line
- The **ANT_DET** pin is connected to the 50 Ω transmission line by means of a sense line
- Choke inductor in series at the **ANT_DET** pin (L1) is placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin
- The additional components (R1, C1 and D1) on the **ANT_DET** line are placed as ESD protection

2.4 SIM interface

2.4.1.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC) which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the GSM network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It must be connected to **VSIM**
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1 = VCC, C2 = RST, C3 = CLK, C5 = GND, C6 = VPP, C7 = I/O) or 8 contacts, providing also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses. Only 6 contacts are required and must be connected to the module SIM card interface as described above, since SARA-G3 modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Removable SIM card are suitable for applications where the SIM changing is required during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided: select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contacts mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as follows:

- Package Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Package Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Package Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Package Pin 5 = UICC Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Package Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to **GND**
- Package Pin 2 = UICC Contact C6 = VPP (Programming supply) → It must be connected to **VSIM**
- Package Pin 3 = UICC Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Package Pin 4 = UICC Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can provide also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above, since SARA-G3 modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected the SIM card interface of SARA-G3 modules as described in Figure 40, where the optional SIM detection feature is not implemented (refer to the circuit described in Figure 42 if the SIM detection feature is not required).

Follow these guidelines connecting the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) and C6 (VPP) to the **VSIM** pin of the module
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module
- Connect the UICC / SIM contact C5 (GND) to ground
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the relative pad of the SIM connector, to prevent digital noise
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each relative pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (Human Body Model according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines)

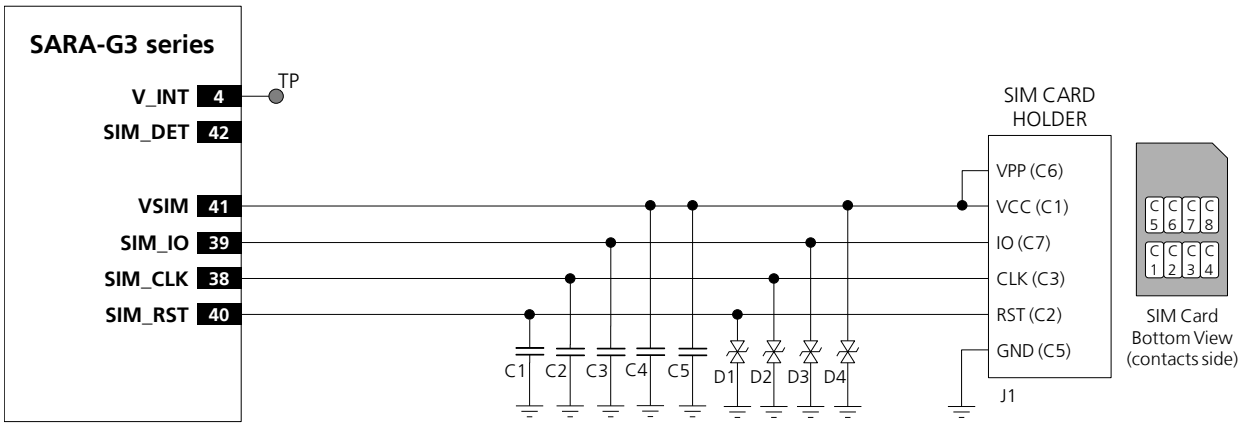


Figure 40: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol

Table 23: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

Guidelines for single SIM chip connection

A solderable SIM chip (M2M UICC Form Factor) must be connected the SIM card interface of SARA-G3 modules as described in Figure 41, where the optional SIM detection feature is not implemented (refer to the circuit described in Figure 42 if the SIM detection feature is not required).

Follow these guidelines connecting the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) and C6 (VPP) to the **VSIM** pin of the module
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module
- Connect the UICC / SIM contact C5 (GND) to ground
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**) close to the relative pad of the SIM chip, to prevent digital noise
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines)

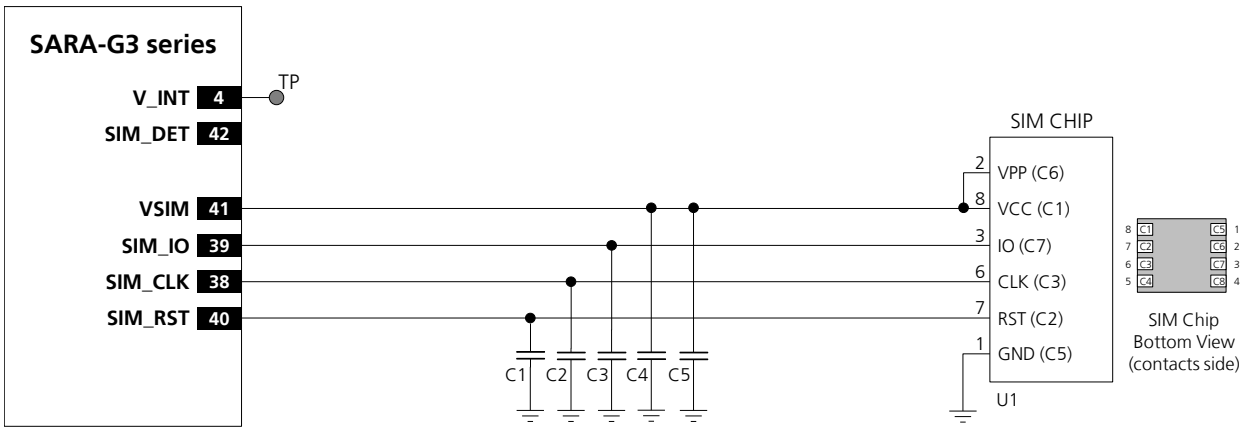


Figure 41: Application circuit for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 24: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

Guidelines for single SIM card connection with detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of SARA-G3 modules as described in Figure 42, where the optional SIM card detection feature is implemented.

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) and C6 (VPP) to the **VSIM** pin of the module
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module

- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module
- Connect the UICC / SIM contact C5 (GND) to ground
- Connect one pin of the mechanical switch integrated in the SIM connector (e.g. the SW2 pin as described in Figure 42) to the **SIM_DET** input pin of the module
- Connect the other pin of the mechanical switch integrated in the SIM connector (e.g. the SW1 pin as described in Figure 42) to the **V_INT** 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 resistor in Figure 42
- Provide a weak (e.g. 470 kΩ) pull-down resistor at the SIM detection line, as the R2 resistor in Figure 42
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the relative pad of the SIM connector, to prevent digital noise
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each relative pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (Human Body Model according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines)

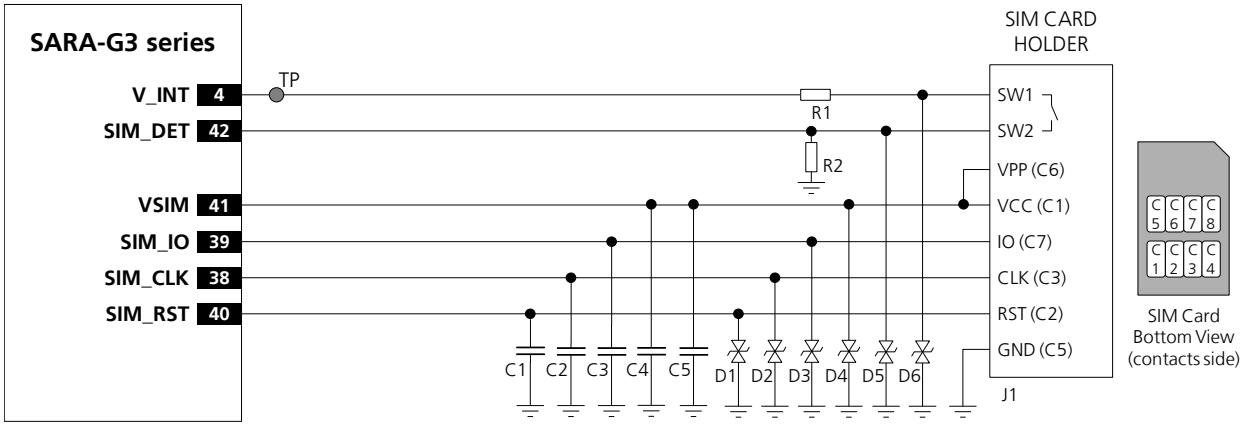


Figure 42: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4, D5, D6	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM Card Holder 6 + 2 positions, with card presence switch	Various Manufacturers, CCM03-3013LFT R102 - C&K Components

Table 25: Example of components for the connection to a single removable SIM card, with SIM detection implemented

Guidelines for dual SIM card connection with detection

Two removable SIM card placed in two different SIM card holders must be connected to the SIM card interface of SARA-G3 modules as described in Figure 43, providing also the SIM card detection feature.

SARA-G3 modules do not support the usage of two SIM at the same time, but two SIM can be populated on the application board providing a proper switch to connect only the first or only the second SIM per time to the SIM card interface of the SARA-G3 modules as described in Figure 43.

SARA-G3 modules do not support SIM hot insertion / removal: the module is able to properly use a SIM only if the SIM / module physical connection is provided before the module boot and then held for normal operation. Switching from one SIM to another one can only be properly done within one of these two time periods:

- after module switch-off by the AT+CPWROFF and before module switch-on by **PWR_ON**
- after network deregistration by AT+COPS=2 and before module reset by AT+CFUN=16 or **RESET_N**

In the application circuit represented in Figure 43, the application processor must drive the SIM switch using its own GPIO before the module boot, to properly select the SIM that is used after the module boot.

If the SIM detection feature is not required by the custom application, the relative detection circuit described in Figure 43 can be not implemented in the dual SIM connection circuit, leaving **SIM_DET** pin not connected.

The dual SIM connection circuit described in Figure 43 can be implemented for SIM chips as well, providing proper connection between SIM switch and SIM chip as described in Figure 41.

If it is required to switch between more than two SIM, a circuit similar to the one described in Figure 43 can be implemented: for example, in case of four SIM circuit, using proper four-throw switches instead of the suggested double-throw switches.

Follow these guidelines connecting the module to two SIM connectors implementing SIM presence detection:

- Connect the contacts C1 (VCC) and C6 (VPP) of the two UICC / SIM to the **VSIM** pin of the module by means of a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) double-throw analog switch (e.g. Fairchild FSA2567) to ensure high-speed data transfer according to SIM requirements
- Connect the contact C7 (I/O) of the two UICC / SIM to the **SIM_IO** pin of the module by means of a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) double-throw analog switch (e.g. Fairchild FSA2567) to ensure high-speed data transfer according to SIM requirements
- Connect the contact C3 (CLK) of the two UICC / SIM to the **SIM_CLK** pin of the module by means of a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) double-throw analog switch (e.g. Fairchild FSA2567) to ensure high-speed data transfer according to SIM requirements
- Connect the contact C2 (RST) of the two UICC / SIM to the **SIM_RST** pin of the module by means of a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) double-throw analog switch (e.g. Fairchild FSA2567) to ensure high-speed data transfer according to SIM requirements
- Connect the contact C5 (GND) of the two UICC / SIM to ground
- Connect one pin of the mechanical switch integrated in the two SIM connectors (e.g. the SW2 pins as described in Figure 43) to the **SIM_DET** input pin of the module by means of a proper double-throw digital switch (e.g. NXP 74LVC1G157)
- Connect the other pin of the mechanical switch integrated in the two SIM connectors (e.g. the SW1 pins as described in Figure 43) to the **V_INT** 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 and R3 resistors in Figure 43
- Provide a weak (e.g. 470 kΩ) pull-down resistor at the SIM detection line, between the double-throw digital switch and the relative SIM connector as the R2 and R4 resistors in Figure 43
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the relative pad of the two SIM connectors, to prevent digital noise
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each relative pad of the two SIM connectors, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holders

- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each relative pad of the two SIM connectors, according to the EMC/ESD requirements of the custom application
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines)

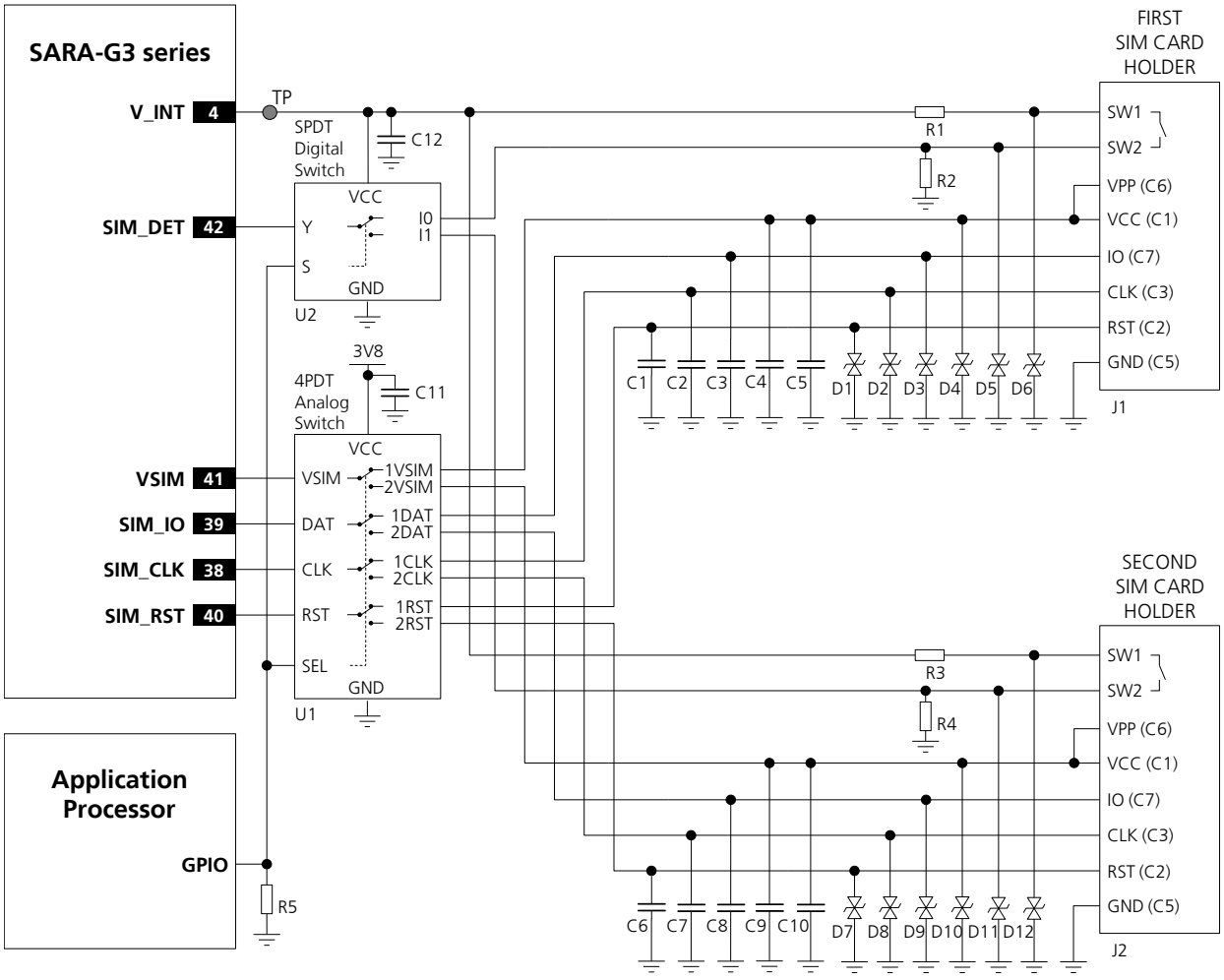


Figure 43: Application circuit for the connection to two removable SIM cards, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1 – C4, C6 – C9	33 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5, C10 – C12	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D12	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1, R3	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2, R4	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
R5	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL- Yageo Phycomp
J1, J2	SIM Card Holder, 6 + 2 p., with card presence switch	CCM03-3013LFT R102 - C&K Components
U1	4PDT Analog Switch, with Low On-Capacitance and Low On-Resistance	FSA2567 - Fairchild Semiconductor
U2	Single 2-Input Digital Multiplexer	74LVC1G157 - NXP Semiconductors

Table 26: Example of components for the connection to two removable SIM cards, with SIM detection implemented

2.4.1.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the SARA-G3 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface: keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of GSM receiver channels whose carrier frequency is coincidental with harmonic frequencies: placing the RF bypass capacitors suggested in Figure 42 near the SIM connector will mitigate the problem.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection as suggested in Figure 42 to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications: the connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency

2.5 Serial interfaces

2.5.1 Asynchronous serial interface (UART)

2.5.1.1 Guidelines for UART circuit design

Providing the full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC8T245PW) can be used to provide full RS-232 (9 lines) functionality. The Texas Instruments chip provides the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8V application processor is used, for complete RS-232 functionality conforming to ITU Recommendation [9] in DTE/DCE serial communication, the complete UART interface of the module (DCE) must be connected to a 1.8 V application processor (DTE) as described in Figure 44.

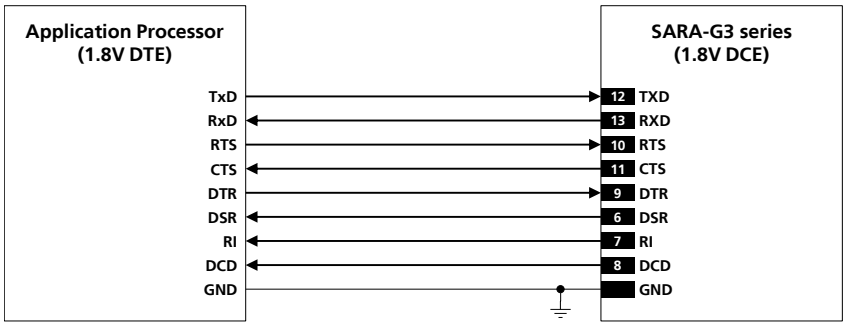


Figure 44: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output as 1.8 V supply, as described in Figure 45.

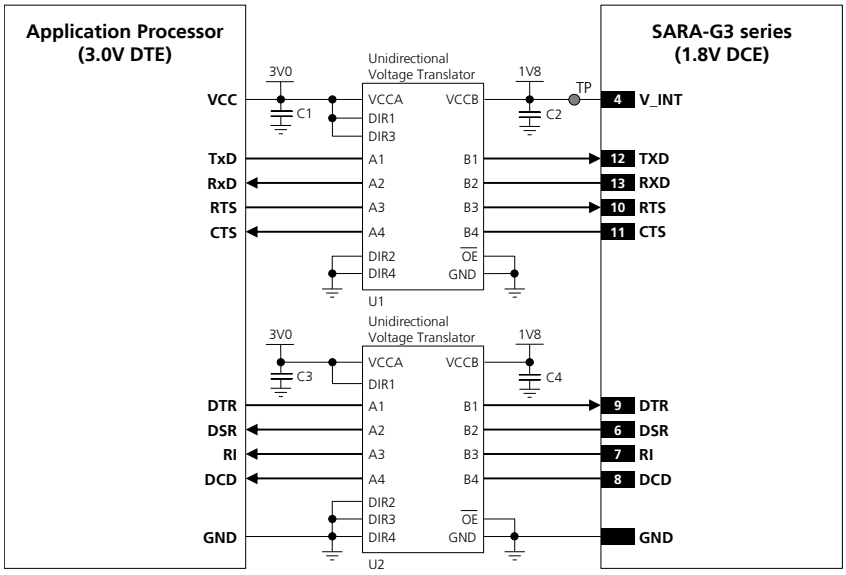


Figure 45: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments

Table 27: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Providing the TXD, RXD, RTS and CTS lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required in, or the lines are not available:

- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level)
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, the Maxim 13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor is used, the circuit should be implemented as described in Figure 46.

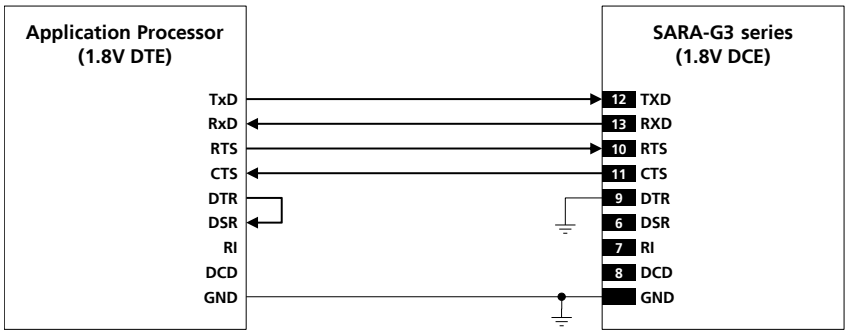


Figure 46: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output as 1.8 V supply, as described in Figure 47.

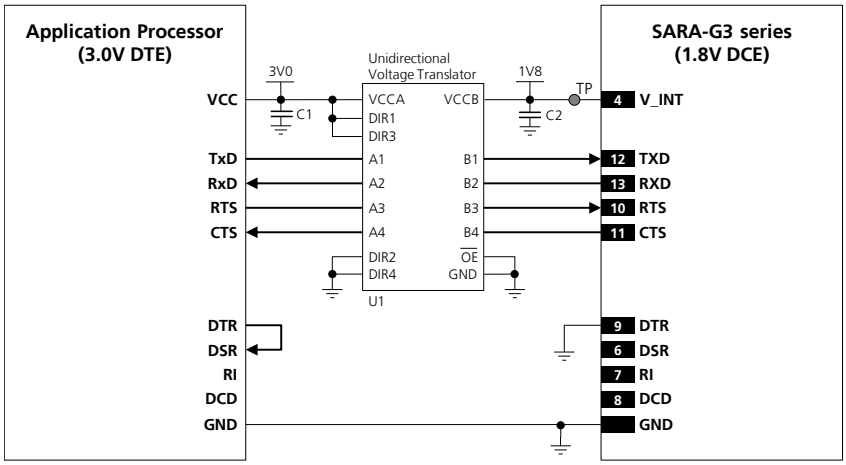


Figure 47: UART interface application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774 - Texas Instruments

Table 28: Component for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

If only **TXD**, **RXD**, **RTS** and **CTS** lines are provided, as implemented in Figure 46 and in Figure 47, the procedure to enable power saving depends on the HW flow-control status. If HW flow-control is enabled (AT&K3, that is the default setting) power saving will be activated by AT+UPSV=1. Through this configuration, when the module is in idle-mode, data transmitted by the DTE is buffered by the DTE and is correctly received by the module when active-mode is entered.

If the HW flow-control is disabled (AT&K0), AT+UPSV=2 can enable the power saving. The module is in idle-mode until a high-to-low (i.e. OFF-to-ON) transition on the **RTS** input line switches the module from idle-mode to active-mode in 20 ms. The module is forced into active-mode if the **RTS** input line is held in the ON state.

Providing the TXD and RXD lines only (not using the complete V24 link)

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available, the circuit with a 1.8 V Application Processor should be implemented as described in Figure 48:

- Connect the module **RTS** input line to GND or to the **CTS** output line of the module: since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, that is the default setting), the pin can be connected using a 0 Ω series resistor to GND or to the active-module **CTS** (low electrical level) when the module is in active-mode, the UART interface is enabled and the HW flow-control is enabled
- Connect the module **DTR** input line to GND, since the module requires **DTR** active (low electrical level)
- Leave **DSR**, **DCD** and **RI** lines of the module unconnected and floating

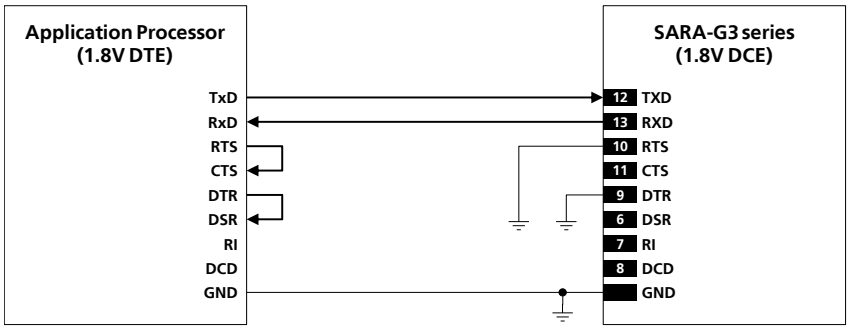


Figure 48: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output as 1.8 V supply, as described in Figure 49.

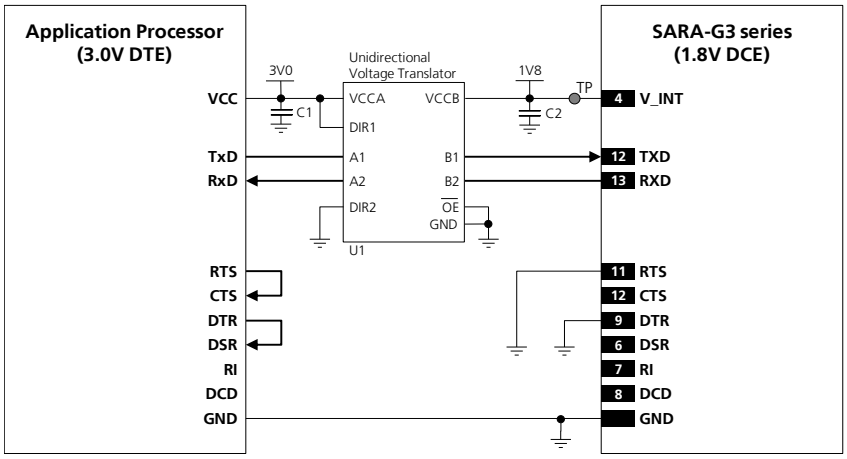


Figure 49: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 29: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

If only **TXD** and **RXD** lines are provided, as described in Figure 48 or in Figure 49, and HW flow-control is disabled (AT&K0), the power saving must be enabled by AT+UPSV=1. In this way, the UART of the module is re-enabled 20 ms after a low-to-high transition on the **TXD** input line, and the recognition of the subsequent characters is guaranteed until the module is in active-mode.

☞ Data delivered by the DTE can be lost using this configuration and the following settings:

- HW flow-control enabled in the module (AT&K3, that is the default setting)
- Module power saving enabled by AT+UPSV=1
- HW flow-control disabled in the DTE

☞ In this case the first character sent when the module is in idle-mode will be a wake-up character and will not be a valid communication character (refer to chapter 1.9.1.4 for the complete description).

☞ If power saving is enabled the application circuit with the **TXD** and **RXD** lines only is not recommended. During command mode the DTE must send to the module a wake-up character or a dummy "AT" before each command line (refer to chapter 1.9.1.4 for the complete description), but during data mode the wake-up character or the dummy "AT" would affect the data communication.

Additional considerations

☞ Any external signal connected to the UART interface must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.

☞ ESD sensitivity rating of UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.5.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.5.2 Auxiliary asynchronous serial interface (UART AUX)

2.5.2.1 Guidelines for UART AUX circuit design

The auxiliary UART interface can be connected to an application processor if it can be set in pass-through mode so that the auxiliary UART interface can be accessed for SARA-G3 modules' firmware upgrade by means of the u-blox EasyFlash tool and for Trace log capture (debug purpose).

☞ To directly enable PC (or similar) connection to the module for firmware upgrade using the u-blox EasyFlash tool and for debugging purposes, it is highly recommended to provide direct access on the application board to the **TXD_AUX** and **RXD_AUX** pins, by means of accessible testpoints directly connected to the pins of the module. Also provide access to the **V_INT** pin to make possible the voltage translation to the auxiliary UART interface voltage level, and to the **PWR_ON** or **RESET_N** pins, or enable the DC supply connected to the **VCC** pin to start the firmware upgrade using the u-blox EasyFlash tool.

The circuit with a 1.8 V Application Processor should be implemented as described in Figure 48.

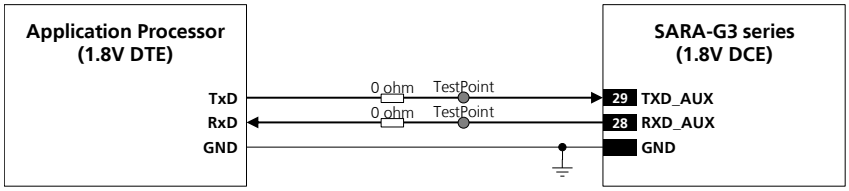


Figure 50: UART AUX interface application circuit connecting a 1.8 V application processor

If a 3.0 V Application Processor is used, appropriate unidirectional voltage translators must be provided using the module **V_INT** output as 1.8 V supply, as described in Figure 49.

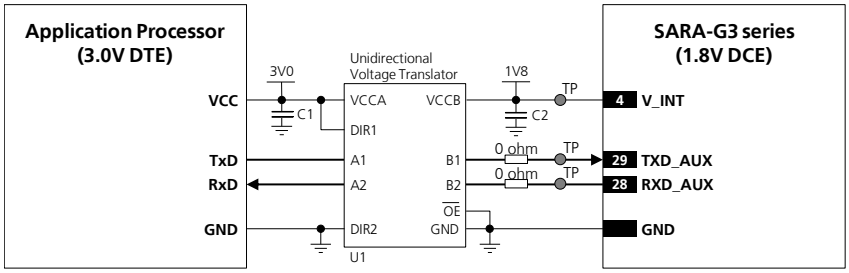


Figure 51: UART AUX interface application circuit connecting a 3.0 V application processor

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 30: Component for UART AUX interface application circuit connecting a 3.0 V application processor

Refer to Firmware Update Application Note [22] for additional guidelines regarding the procedure for SARA-G3 modules' firmware upgrade over the auxiliary UART interface using the u-blox EasyFlash tool.

☞ Any external signal connected to the auxiliary UART interface must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.

☞ ESD sensitivity rating of auxiliary UART pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.5.2.2 Guidelines for UART AUX layout design

The auxiliary UART serial interface is not critical for the layout design since it is not used during normal operation of SARA-G3 modules. Ensure accessibility to the **TXD_AUX** and **RXD_AUX** pins providing test points on the application board.

2.5.3 DDC (I²C) interface

2.5.3.1 Guidelines for DDC (I²C) circuit design

The **SDA** and **SCL** lines must be connected to the DDC (I²C) interface pins of the u-blox GPS/GNSS receiver (i.e. the SDA2 and SCL2 pins of the u-blox positioning receiver) on the application board to allow the communication between the wireless module and the u-blox GPS/GNSS receiver, enabled by the AT+UGPS command (for more details refer to u-blox AT Commands Manual [2]).

To be compliant to the I²C bus specifications, the module bus interface pads are open drain output and pull up resistors must be used conforming to the I²C bus specifications [13]. Since the pull-up resistors are not mounted on the module, they must be mounted externally.

☞ Provide external pull-ups resistors (e.g. 4.7 kΩ) on **SDA** and **SCL** lines and connect them to the **V_INT** 1.8 V supply source, or another 1.8 V supply source enabled after **V_INT** (e.g., as the 1.8 V supply present in the application circuit of Figure 52, controlled by the wireless module).

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus increase the capacitance. If the bus capacitance is increased, use pull-up resistors with nominal resistance value lower than 4.7 kΩ, to match the I²C bus specifications [13] regarding rise and fall times of the signals.

☞ Capacitance and series resistance must be limited on the bus to match the I²C specifications (1.0 µs is the maximum allowed rise time on the **SCL** and **SDA** lines): route connections as short as possible.

☞ If the pins are not used as DDC bus interface, they can be left unconnected.

The following special features over GPIOs can be optionally implemented on the application board to improve the integration of SARA-G350 wireless modules with a u blox GPS/GNSS receiver:

- The **GPIO2**, by default configured to provide the "GPS supply enable" function, must be connected to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox positioning receiver on the application board to enable or disable the supply of the u-blox GPS/GNSS receiver connected to the wireless module by the AT+UGPS command
- The **GPIO3**, by default configured to provide the "GPS data ready" function, must be connected to the data ready output of the u-blox positioning receiver (i.e. the pin TXD1 of the u-blox GPS/GNSS receiver) on the application board, to sense when the u-blox positioning receiver connected to the wireless module is ready to send data by the DDC (I²C) interface
- The **GPIO4**, by default configured to provide the "GPS RTC sharing" function, must be connected to the RTC synchronization signal of the u-blox positioning receiver (i.e. the pin EXTINT0 of the u-blox GPS/GNSS receiver) on the application board, to provide an RTC (Real Time Clock) synchronization signal at the power up of the u-blox positioning receiver connected to the wireless module

☞ "GPS data ready" and "GPS RTC sharing" functions are not supported by all u-blox GPS/GNSS receivers HW or ROM/FW versions. Refer to the GPS Implementation Application Note [21] or to the Hardware Integration Manual of the u-blox GPS/GNSS receivers for the supported features.

Figure 52 illustrates an application circuit for SARA-G350 connection to a u-blox 1.8 V GPS/GNSS receiver:

- The **SDA** and **SCL** pins of the SARA-G350 module are directly connected to the relative pins of the u-blox 1.8 V GPS/GNSS receiver, with appropriate pull-up resistors.
- The **GPIO3** and **GPIO4** pins are directly connected respectively to **TXD1** and **EXTINT0** pins of the u-blox 1.8 V GPS/GNSS receiver providing "GPS data ready" and "GPS RTC sharing" functions.

- The **GPIO2** pin is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 1.8 V GPS/GNSS receiver providing the "GPS supply enable" function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the SARA-G350 module is switched off or in the reset state.
- The **V_BCKP** supply output of the SARA-G350 wireless module is connected to the **V_BCKP** backup supply input pin of the GPS/GNSS receiver to provide the supply for the GPS/GNSS real time clock and backup RAM when the **VCC** supply of the wireless module is within its operating range and the **VCC** supply of the GPS/GNSS receiver is disabled. This enables the u-blox GPS/GNSS receiver to recover from a power breakdown with either a Hot-start or a Warm-start (depending on the actual duration of the GPS/GNSS **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

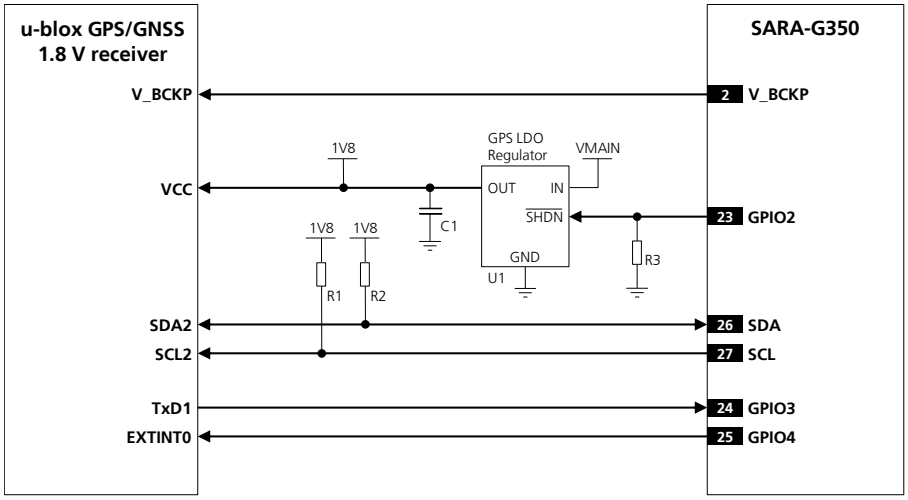


Figure 52: DDC (I^2C) application circuit for u-blox 1.8 V GPS/GNSS receiver

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1	Voltage Regulator for GPS/GNSS Receiver	See GPS/GNSS Receiver Hardware Integration Manual

Table 31: Components for DDC (I^2C) application circuit for u-blox 1.8 V GPS/GNSS receiver

As an alternative to using an external voltage regulator, the **V_INT** supply output of SARA-G350 wireless modules can be used to supply a u-blox 1.8 V GPS/GNSS receiver of the u-blox 6 family (or later u-blox family). The **V_INT** supply is able to withstand the maximum current consumption of these positioning receivers.

The **V_INT** supply output provides low voltage ripple (up to 15 mVpp) when the module is in active-mode or in connected-mode, but it provides higher voltage ripple (up to 90 mVpp) when the module is in the low power idle-mode with power saving configuration enabled by AT+UPSV (refer to u-blox AT Commands Manual [2]).

According to the voltage ripple characteristic of the **V_INT** supply output:

- The power saving configuration cannot be enabled to properly supply by **V_INT** output any 1.8 V GPS/GNSS receiver of the u-blox 6 family and any 1.8 V GPS/GNSS receiver of the u-blox 7 family with TCXO
- The power saving configuration can be enabled to properly supply by **V_INT** output any 1.8 V GPS/GNSS receiver of the u-blox 7 family without TCXO
- Additional filtering may be needed to properly supply an external LNA, depending on the characteristics of the used LNA, adding a series ferrite bead and a bypass capacitor (e.g. the Murata BLM15HD182SN1 ferrite bead and the Murata GRM1555C1H220J 22 pF capacitor) at the input of the external LNA supply line.

Refer to the GPS Implementation Application Note [21] for additional guidelines using the **V_INT** supply output of SARA-G350 wireless modules to supply a u-blox 1.8 V GPS/GNSS receiver.

Figure 53 illustrates the application circuit for SARA-G350 connection to a u-blox 3.0 V GPS/GNSS receiver:

- **SDA** and **SCL** pins of SARA-G350 are directly connected to the relative pins of the u-blox 3.0 V GPS/GNSS receiver, with appropriate pull-up resistors: an I2C-bus Voltage Translator is not needed because SARA-G350 DDC (I^2C) pins are capable up to 3.3 V.
- **GPIO3** and **GPIO4** pins of SARA-G350 are connected to the u-blox 3.0 V GPS/GNSS receiver by means of a general purpose Voltage Translator, needed for SARA-G350 generic digital pins because only 1.8 V capable.
- **GPIO2** is connected to the active-high enable pin of the external voltage regulator that supplies the u-blox 3.0 V GPS/GNSS receiver to enable or disable the 3.0 V GPS/GNSS supply.
- The **V_BCKP** supply output of SARA-G350 is directly connected to the **V_BCKP** backup supply input pin of the u-blox 3.0 V GPS/GNSS receiver as in the application circuit for a u-blox 1.8 V GPS/GNSS receiver.

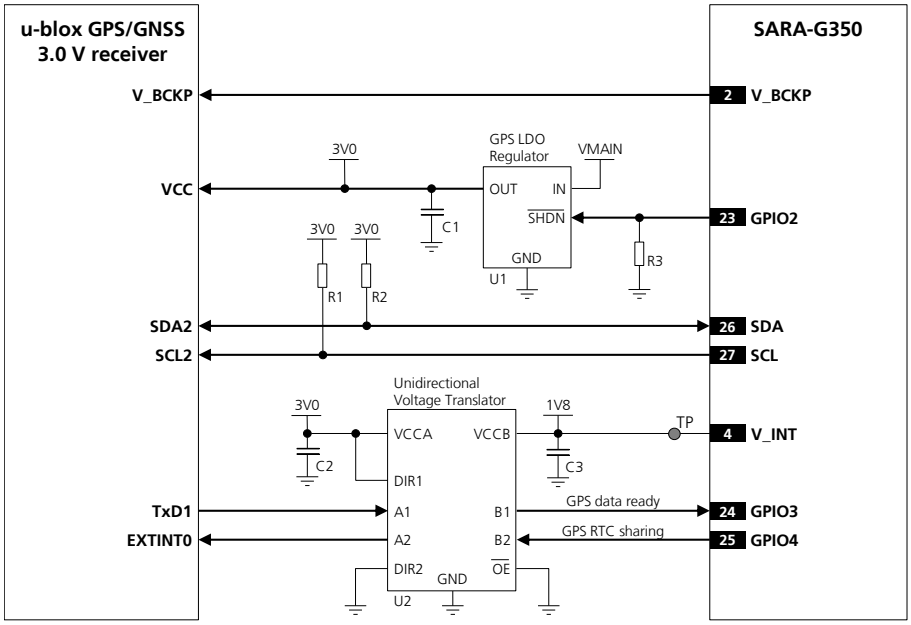


Figure 53: DDC (I^2C) application circuit for u-blox 3.0 V GPS/GNSS receiver

Reference	Description	Part Number – Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1	Voltage Regulator for GPS/GNSS Receiver	See GPS/GNSS Receiver Hardware Integration Manual
U2	Generic Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 32: Components for DDC (I^2C) application circuit for u-blox 3.0 V GPS/GNSS receiver

ESD sensitivity rating of the DDC (I^2C) pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.5.3.2 Guidelines for DDC (I^2C) layout design

The DDC (I^2C) serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Audio Interface

2.6.1 Analog Audio interface

2.6.1.1 Guidelines for microphone and speaker connection circuit design (headset / handset modes)

SARA-G350 modules provide one analog audio input path and one analog audio output path: the same paths are used for both headset and handset modes, so that basically the same application circuit can be implemented for both headset and handset modes.

Figure 54 shows an application circuit for the analog audio interface in headset and handset modes, connecting a 2.2 kΩ electret microphone and a 16 Ω receiver / speaker:

- External microphone can be connected to the uplink path of the module as described in Figure 54, since the module provides supply and reference as well as differential signal input for the external microphone
- 16 Ω receiver / speaker can be directly connected to the balanced output of the module as described in Figure 54, since the differential analog audio output of the module is able to directly drive loads with resistance rating greater than 14 Ω

The general guidelines for the design of the analog audio circuit for both headset and handset modes, fulfilled implementing the circuit of Figure 54, are the following:

- Provide proper supply to the used electret microphone, providing a proper connection from the MIC_BIAS supply output to the microphone. It's suggested to implement a bridge structure as described in Figure 54:
  - the electret microphone, with its nominal intrinsic resistance value, represents one resistor of the bridge
  - to achieve good supply noise rejection, the ratio of the two resistance in one leg (R2/R3) should be equal to the ratio of the two resistance in the other leg (R4/MIC), i.e. R2 has to be equal to R4 (e.g. 2.2 kΩ) and R3 has to be equal to the microphone nominal intrinsic resistance value (e.g. 2.2 kΩ)
- Provide a proper series resistor at the MIC_BIAS supply output and then mount a proper large bypass capacitor to provide additional supply noise filtering, as the R1 series resistor (2.2 kΩ) and the C1 bypass capacitor (10 µF) in the circuit implemented in Figure 54
- Do not place a bypass capacitor directly at the MIC_BIAS supply output, since proper internal bypass capacitor is already provided to guarantee stable operation of the internal regulator
- Connect the reference of the microphone circuit to the MIC_GND pin of the module as a sense line: implement the connection described in Figure 54
- Provide a proper series capacitor at both MIC_P and MIC_N analog uplink inputs for DC blocking (as the C2 an C3 100 nF Murata GRM155R71C104K capacitors in Figure 54) to provide an high-pass filter for the microphone DC bias with proper cut-off frequency according to the value of the resistors of the microphone supply circuit, and then connect the signal lines to the microphone as described in Figure 54
- Provide proper parts on each line connected to the external microphone as noise and EMI improvements, to minimize RF coupling and TDMA noise, according to the custom application requirements. Following the circuit described in Figure 54:
  - mount an 82 nH series inductor with self resonance frequency ~1 GHz (e.g. Murata LQG15HS82NJ02) on each microphone line, as L1 and L2 inductors in Figure 54
  - mount and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each microphone line to solid ground plane, as C4 and C5 capacitors in Figure 54
- Use a micropone designed for GSM applications which typically have internal built-in bypass capacitor
- Connect the **SPK_P** and **SPK_N** analog downlink outputs directly to the receiver / speaker (which resistance rating has to be greater than 14 Ω) as in the circuit described in Figure 54

- Provide proper parts on each line connected to the receiver / speaker as noise and EMI improvments, to minimize RF coupling, according to EMC requirements of the custom application. Following the circuit described in Figure 54:
  - mount and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each speaker line to solid ground plane, as C6 and C7 capacitors in Figure 54
- Provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) if the analog audio lines will be externally accessible on the application device, according to EMC/ESD requirements of the custom application. The protection should be mounted close to accessible point of the line, as the D1 and D2 parts in the circuit described in Figure 54

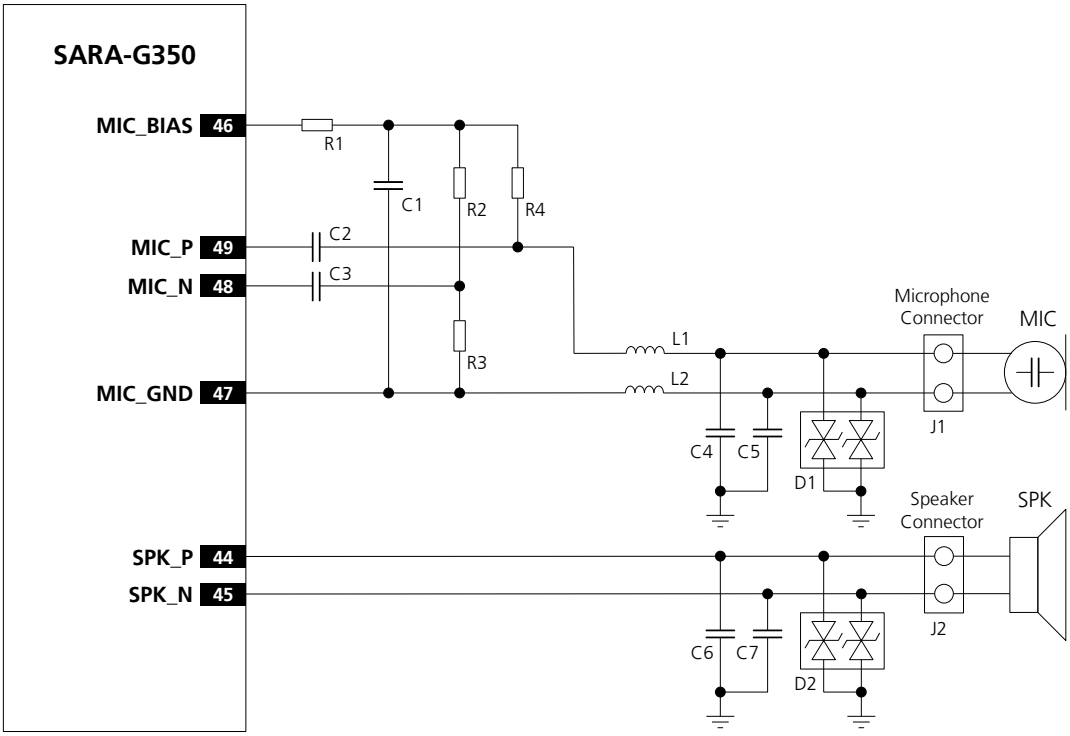


Figure 54: Analog audio interface headset and handset mode application circuit

Reference	Description	Part Number – Manufacturer
C1	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C2, C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA88 – Murata
C4, C5, C6, C7	27 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H270JA01 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
J1	Microphone Connector	Various Manufacturers
J2	Speaker Connector	Various Manufacturers
L1, L2	82 nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
MIC	2.2 kΩ Electret Microphone	Various Manufacturers
R1, R2, R3, R4	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
SPK	16 Ω Speaker	Various Manufacturers

Table 33: Example of components for analog audio interface headset and handset mode application circuit

☞ If the analog audio interface is not used, the analog audio pins (**MIC_BIAS**, **MIC_GND**, **MIC_P**, **MIC_N**, **SPK_P**, **SPK_N**) can be left unconnected on the application board.

2.6.1.2 Guidelines for microphone and loudspeaker connection circuit design (hands-free mode)

Figure 55 shows an application circuit for the analog audio interface in hands-free mode, connecting a 2.2 kΩ electret microphone and an 8 Ω or 4 Ω loudspeaker:

- External microphone can be connected to the uplink path of the module as described in Figure 55, since the module provides supply and reference as well as differential signal input for the external microphone
- Using a 8 Ω or 4 Ω loudspeaker for the hands-free mode, an external audio amplifier must be provided on the application board to amplify the low power audio signal provided by the downlink path of the module, so that the external audio amplifier will drive the 8 Ω or 4 Ω loudspeaker, since differential analog audio output of the module is able to directly drive loads with resistance rating greater than 14 Ω

The general guidelines for the design of the analog audio circuit for hands-free mode, fulfilled implementing the circuit of Figure 55, are the following:

- Provide proper supply to the used electret microphone, providing a proper connection from the MIC_BIAS supply output to the microphone. It's suggested to implement a bridge structure as described in Figure 55:
  - the electret microphone, with its nominal intrinsic resistance value, represents one resistor of the bridge
  - to achieve good supply noise rejection, the ratio of the two resistance in one leg (R2/R3) should be equal to the ratio of the two resistance in the other leg (R4/MIC), i.e. R2 has to be equal to R4 (e.g. 2.2 kΩ) and R3 must be equal to the microphone nominal intrinsic resistance value (e.g. 2.2 kΩ)
- Provide a series resistor at the MIC_BIAS supply output and then mount a good bypass capacitor to provide additional supply noise filtering, as the R1 series resistor (2.2 kΩ) and the C1 bypass capacitor (10 µF) in the circuit implemented in Figure 55
- Do not place a bypass capacitor directly at the MIC_BIAS supply output, since proper internal bypass capacitor is already provided to guarantee stable operation of the internal regulator
- Connect the reference of the microphone circuit to the MIC_GND pin of the module as a sense line: implement the connection described in Figure 55
- Provide a proper series capacitor at both MIC_P and MIC_N analog uplink inputs for DC blocking (as the C2 an C3 100 nF Murata GRM155R71C104K capacitors in Figure 55) to provide an high-pass filter for the microphone DC bias with proper cut-off frequency according to the value of the resistors of the microphone supply circuit, and then connect the signal lines to the microphone as described in Figure 55
- Provide proper parts on each line connected to the external microphone as noise and EMI improvements, to minimize RF coupling and TDMA noise, according to the custom application requirements. Following the circuit described in Figure 55:
  - mount an 82 nH series inductor with self resonance frequency ~1 GHz (e.g. Murata LQG15HS82NJ02) on each microphone line, as L1 and L2 inductors in Figure 55
  - mount and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each microphone line to solid ground plane, as C4 and C5 capacitors in Figure 55
- Use a microphone designed for GSM applications which typically have internal built-in bypass capacitor
- Provide a 47 nF series capacitor at both **SPK_P** and **SPK_N** analog downlink outputs for DC blocking (as the C8 an C9 Murata GRM155R71C473K capacitors in Figure 55) and then connect the lines to the differential input of a proper external audio amplifier which differential output has to be connected the 8 Ω or 4 Ω loudspeaker as for the Analog Devices SSM2305CPZ filter-less mono 2.8 W class-D Audio Amplifier in the circuit described in Figure 55
- Provide proper parts on each line connected to the external loudspeaker as noise and EMI improvments, to minimize RF coupling, according to EMC requirements of the custom application. Following the circuit described in Figure 55:
  - mount and a 27 pF bypass capacitor (e.g. Murata GRM1555C1H270J) from each loudspeaker line to solid ground plane, as C6 and C7 capacitors in Figure 55

- Provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) if the analog audio lines will be externally accessible on the application device, according to EMC/ESD requirements of the custom application. The protection should be mounted close to accessible point of the line, as the D1 and D2 parts in the circuit described in Figure 55

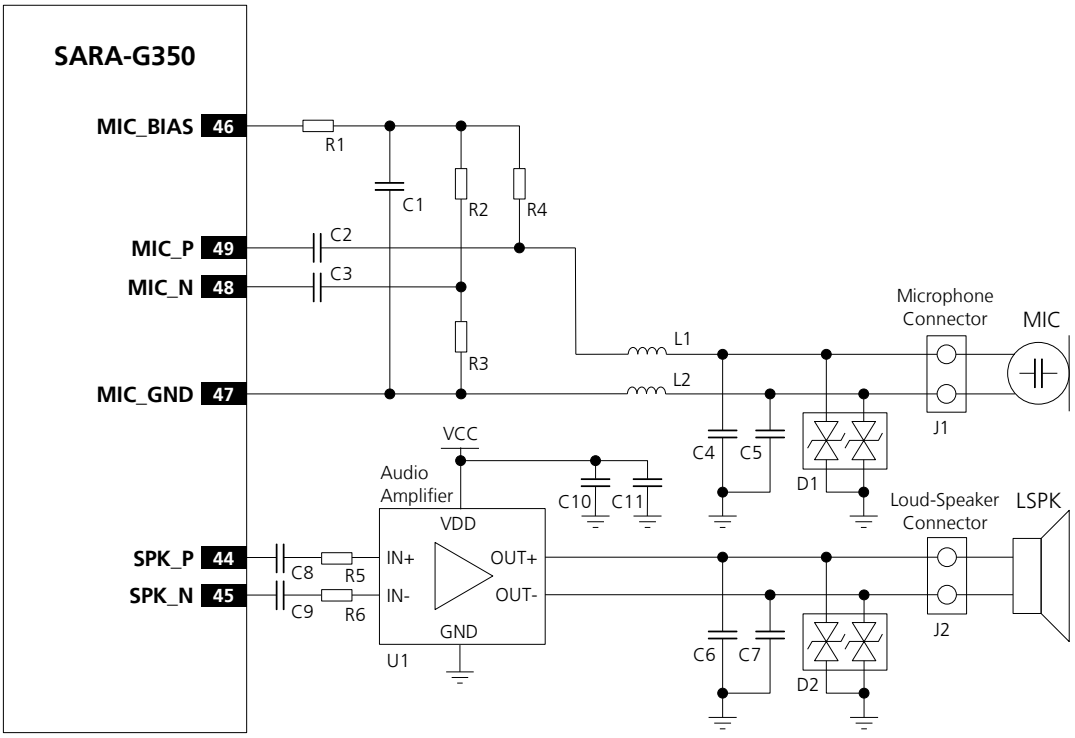


Figure 55: Analog audio interface hands-free mode application circuit

Reference	Description	Part Number – Manufacturer
C1, C10	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C2, C3, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA88 – Murata
C4, C5, C6, C7	27 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H270JA01 – Murata
C8, C9	47 nF Capacitor Ceramic X7R 0402 10% 16V	GRM155R71C473KA01 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
J1	Microphone Connector	Various Manufacturers
J2	Speaker Connector	Various Manufacturers
L1, L2	82 nH Multilayer inductor 0402 (self resonance frequency ~1 GHz)	LQG15HS82NJ02 – Murata
LSPK	8 Ω Loud-Speaker	Various Manufacturers
MIC	2.2 kΩ Electret Microphone	Various Manufacturers
R1, R2, R3, R4	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
R5, R6	0 Ω Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
U1	Filter-less Mono 2.8 W Class-D Audio Amplifier	SSM2305CPZ – Analog Devices

Table 34: Example of components for analog audio interface hands-free mode application circuit

☞ If the analog audio interface is not used, the analog audio pins (**MIC_BIAS**, **MIC_GND**, **MIC_P**, **MIC_N**, **SPK_P**, **SPK_N**) can be left unconnected on the application board.

2.6.1.3 Guidelines for external analog audio device connection circuit design

The differential analog audio input / output can be used to connect the module to an external analog audio device. Audio devices with a differential analog input / output are preferable, as they are more immune to external disturbances.

Figure 56 and Table 35 describe the application circuits, following the suggested circuit design-in.

Guidelines for the connection to a differential analog audio input:

- The **SPK_P** / **SPK_N** balanced output of the module must be connected to the differential input of the external audio device by means of series capacitors for DC blocking (e.g. 10 µF Murata GRM188R60J106M) to decouple the bias present at the module output, as described in the left side of Figure 56

Guidelines for the connection to a single ended analog audio input:

- A proper differential to single ended circuit must be inserted from the **SPK_P** / **SPK_N** balanced output of the module to the single ended input of the external audio device, as described in the right side of Figure 56: 10 µF series capacitors (e.g. Murata GRM188R60J106M) are provided to decouple the bias present at the module output, and a voltage divider is provided to properly adapt the signal level from the module output to the external audio device input

Guidelines for the connection to a differential analog audio output:

- The **MIC_P** / **MIC_N** balanced input of the module must be connected to the differential output of the external audio device by means of series capacitors for DC blocking (e.g. 10 µF Murata GRM188R60J106M) to decouple the bias present at the module input, as described in the left side of Figure 56

Guidelines for the connection to a single ended analog audio output:

- A proper single ended to differential circuit has to be inserted from the single ended output of the external audio device to the **MIC_P** / **MIC_N** balanced input of the module, as described in the right side of Figure 56: 10 µF series capacitors (e.g. Murata GRM188R60J106M) are provided to decouple the bias present at the module input, and a voltage divider is provided to properly adapt the signal level from the external audio device output to the module input

Additional guidelines for any connection:

- The DC-block series capacitor acts as high-pass filter for audio signals, with cut-off frequency depending on both the values of capacitor and on the input impedance of the device. For example: in case of differential input impedance of 600 Ω , the two 10 µF capacitors will set the -3 dB cut-off frequency to 53 Hz, while for single ended connection to 600 Ω external device, the cut-off frequency with just the single 10 µF capacitor will be 103 Hz. In both cases the high-pass filter has a low enough cut-off to not impact the audio signal frequency response
- Use a suitable power-on sequence to avoid audio bump due to charging of the capacitor: the final audio stage should be always enabled as last one
- The signal levels can be adapted by setting gain using AT commands (refer to the u-blox AT Commands Manual [2], +USGC, +UMGC), but additional circuitry must be inserted if the **SPK_P** / **SPK_N** output level of the module is too high for the input of the audio device or if the output level of the audio device is too high for **MIC_P** / **MIC_N**, as the voltage dividers present in the circuits described in the right side of Figure 56 to properly adapt the signal level

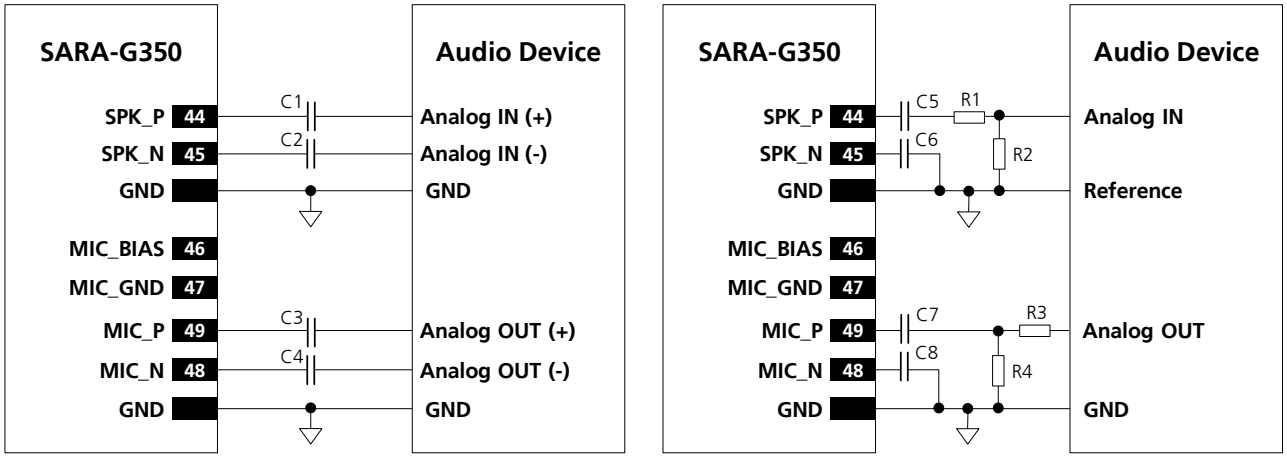


Figure 56: Application circuits to connect the module to audio devices with proper differential or single-ended input/output

Reference	Description	Part Number – Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8	10 µF Capacitor X5R 0603 5% 6.3 V	GRM188R60J106M – Murata
R1, R3	0 Ω Resistor 0402 5% 0.1 W	RC0402JR-070RL – Yageo Phycomp
R2, R4	Not populated	

Table 35: Connection to an analog audio device

2.6.1.4 Guidelines for analog audio layout design

Accurate analog audio design is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 217 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise from audio lines due to both **VCC** burst noise coupling and RF detection.

Guidelines for the uplink path, which is the most sensitive since the analog input signals are in the microVolts range, are the following:

- Avoid coupling of any noisy signal to microphone lines: it's strongly recommended to route microphone lines away from module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source
- Keep ground separation from microphone lines to other noisy signals. Use an intermediate ground layer or vias wall for coplanar signals
- Route microphone signal lines as a differential pair embedded in ground to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise
- Route microphone reference as a signal line since the **MIC_GND** pin is internally connected to ground as a sense line as the reference for the analog audio input
- Cross other signals lines on adjacent layers with 90° crossing
- Place bypass capacitor for RF very close to active microphone. The preferred microphone should be designed for GSM applications which typically have internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device

Guidelines for the downlink path are the following:

- The physical width of the audio output lines on the application board must be wide enough to minimize series resistance since the lines are connected to low impedance speaker transducer
- Avoid coupling of any noisy signal to speaker lines: it's recommended to route speaker lines away from module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source

- Route speaker signal lines as a differential pair embedded in ground up to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise
- Cross other signals lines on adjacent layers with 90° crossing
- Place bypass capacitor for RF close to the speaker

2.6.2 Digital Audio interface

2.6.2.1 Guidelines for digital audio circuit design

SARA-G3 series I²S digital audio interface can be connected to an external digital audio device for voice applications. The external digital audio device must act as an I²S slave (since the SARA-G3 modules act as an I²S master only), with compatible I²S mode (i.e. PCM mode or Normal I²S mode), I²S sample rate and I²S clock frequency. The external device must provide compatible voltage levels (1.80 V typ.), otherwise the lines must be connected by means of a proper unidirectional voltage translator (e.g. Texas Instruments SN74AVC4T774 or SN74AVC2T245).

Figure 57 shows an application circuit with a generic digital audio device.

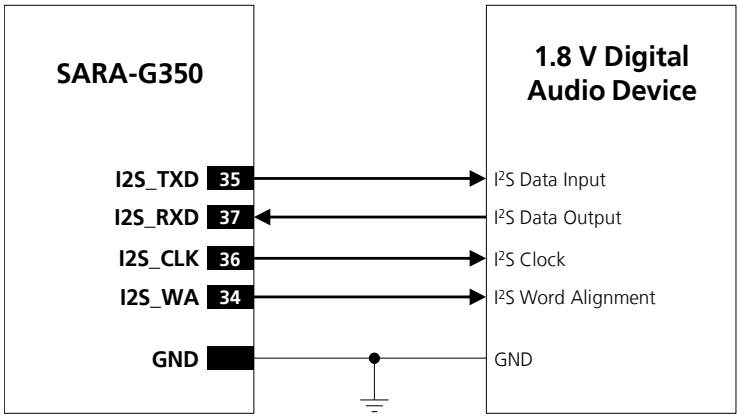


Figure 57: I²S interface application circuit with a generic digital audio device

Any external signal connected to the digital audio interface must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.

ESD sensitivity rating of I²S interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

If the I²S digital audio pins are not used, they can be left unconnected on the application board.

2.6.2.2 Guidelines for digital audio layout design

The I²S interfaces lines (**I2S_CLK**, **I2S_RX**, **I2S_TX**, **I2S_WA**) require the same consideration regarding electro-magnetic interference as the SIM card. Keep the traces short and avoid coupling with RF line or sensitive analog inputs.

2.7 General Purpose Input/Output (GPIO)

2.7.1.1 Guidelines for GPIO circuit design

The following application circuits are suggested as general guideline for the usage of the GPIO pins available with the SARA-G350 modules, according to the relative custom function.

- **Network status indication**:
  The pin configured to provide the "Network status indication" function, e.g. the **GPIO1**, can be connected on the application board to an input pin of an application processor or can drive a LED by a transistor with integrated resistors to indicate network status.
- **GSM Tx burst indication**:
  The **GPIO1** pin, as configured to provide the "GSM Tx burst indication" function, can be connected on the application board to an input pin of an application processor to indicate when a GSM Tx burst/slot occurs.
- **GPS supply enable**:
  The pin configured to provide the "GPS supply enable" function (**GPIO2** by default) has to be connected to the active-high enable pin (or the active-low shutdown pin) of the voltage regulator that supplies the u-blox GPS/GNSS receiver.
- **GPS data ready**:
  The **GPIO3** pin, by default configured to provide the "GPS data ready" function, has to be connected to the data ready output of the u-blox GPS/GNSS receiver (i.e. the pin TXD1).
- **GPS RTC sharing**:
  The **GPIO4** pin, by default configured to provide the "GPS RTC sharing" function, has to be connected to the RTC synchronization input of the u-blox GPS/GNSS receiver (i.e. the pin EXTINT0).

Figure 58 describes an application circuit for a typical usage of the GPIOs of SARA-G350 modules:

- Network indication function provided by the **GPIO1** pin
- GPS supply enable function provided by the **GPIO2** pin
- GPS data ready function provided by the **GPIO3** pin
- GPS RTC sharing function provided by the **GPIO4** pin

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO.

☞ ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

☞ Any external signal connected to the GPIOs must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the wireless module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. Texas Instruments SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance during module power down mode and during the module power-on sequence.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

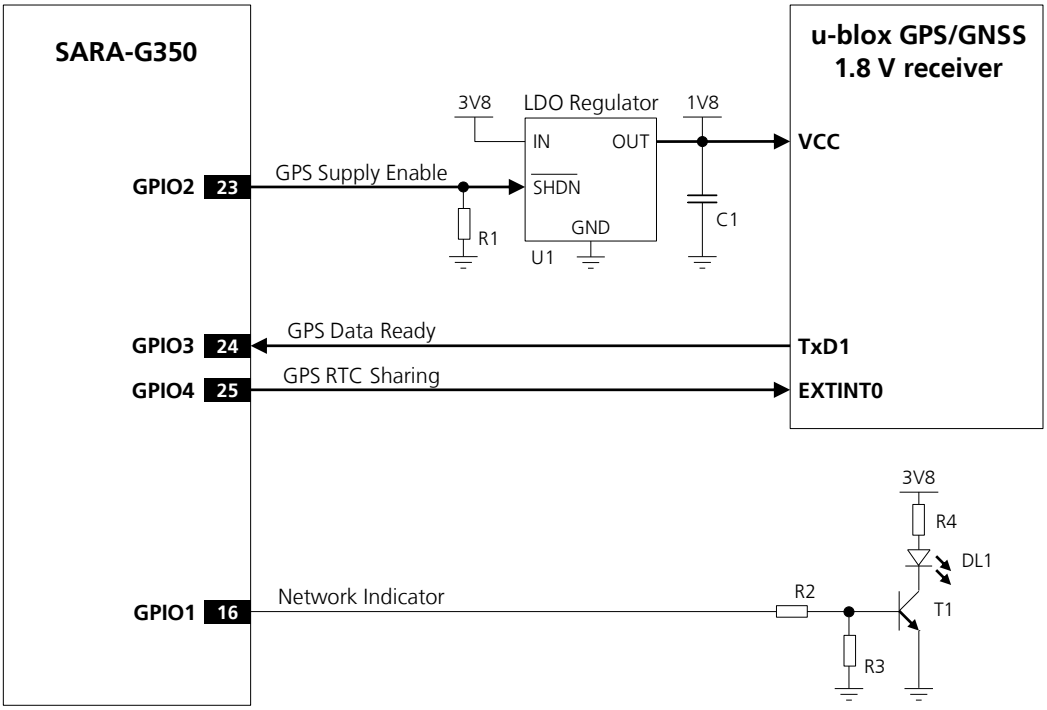


Figure 58: GPIO application circuit

Reference	Description	Part Number - Manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	Voltage Regulator for GPS/GNSS Receiver	See GPS/GNSS Module Hardware Integration Manual
R2	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R4	820 Ω Resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED Red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 36: Components for GPIO application circuit

2.7.1.1 Guidelines for GPIO layout design

The general purpose input/output pins are generally not critical for layout.

2.8 Reserved pins (RSVD)

SARA-G3 series modules have pins reserved for future use. All the **RSVD** pins, except pin number 33, can be left unconnected on the application board. Figure 59 illustrates the application circuit.

Pin 33 (**RSVD**) must be connected to GND.

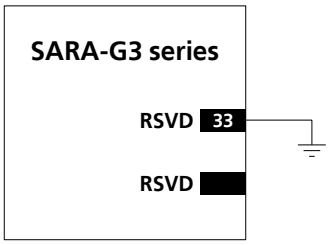


Figure 59: Application circuit for the reserved pins (RSVD)

2.9 Module placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

Make sure that RF and analog circuits are clearly separated from any other digital circuits on the system board.

Provide enough clearance between the module and any external part.

The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the SARA-G3 modules: avoid placing temperature sensitive devices close to the module.

2.10 Module footprint and paste mask

Figure 60 and Table 37 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA-G3 modules: the proposed land pattern layout reflects the modules' pads layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, implementing the solder mask opening 50 µm larger per side than the corresponding copper pad.

The recommended solder paste thickness is 150 µm, according to application production process requirements.

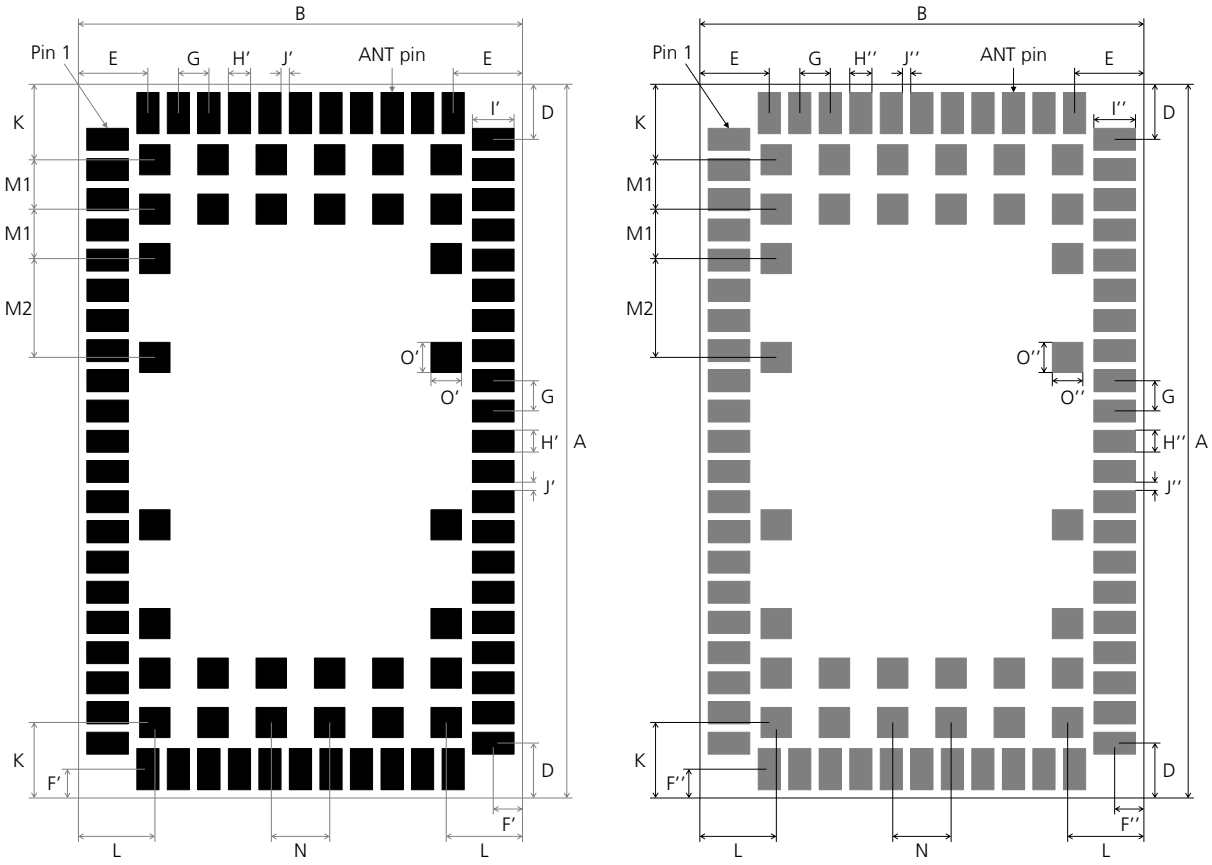


Figure 60: SARA-G3 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	G	1.10 mm	K	2.75 mm
B	16.0 mm	H'	0.80 mm	L	2.75 mm
C	3.00 mm	H''	0.75 mm	M1	1.80 mm
D	2.00 mm	I'	1.50 mm	M2	3.60 mm
E	2.50 mm	I''	1.55 mm	N	2.10 mm
F'	1.05 mm	J'	0.30 mm	O'	1.10 mm
F''	1.00 mm	J''	0.35 mm	O''	1.05 mm

Table 37: SARA-G3 series modules suggested footprint and paste mask dimensions

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.11 Thermal guidelines

SARA-G3 series module operating temperature range and module thermal resistance are specified in the SARA-G3 series Data Sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload or voice call in connected-mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks; however the application should be correctly designed to cope with it.

During transmission at maximum RF power the SARA-G3 series modules generate thermal power that can exceed 1 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the number of allocated TX slot, transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition (e.g. GSM or GPRS mode, transmit band): the overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

Mounting a SARA-G3 series module on a 79 mm x 62 mm x 1.41 mm 4-Layers PCB with a high coverage of copper in still air conditions[8], the increase of the module temperature[9] in different modes of operation, referred to idle state initial condition[10], can be summarized as following:

- ~8 °C during a GSM voice call (1 TX slot, 1 RX slot) at max TX power
- ~12 °C during a GPRS data transfer (2 TX slots, 3 RX slots) at max TX power

The Module-to-Ambient thermal resistance value and the relative increase of module temperature will be different for other mechanical deployments of the module, e.g. PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of thermal dissipation, i.e. the Module-to-Ambient thermal resistance reduction, will decrease the temperature for internal circuitry of SARA-G3 series modules for a given operating ambient temperature. This improves the device long-term reliability for applications operating at high ambient temperature.

A few hardware techniques may be used to reduce the Module-to-Ambient thermal resistance in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with complete via stack down to main ground layer
- Provide a ground plane as wide as possible on the application board
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power
- Optimize the thermal design of any high-power component included in the application, as linear regulators and amplifiers, to optimize overall temperature distribution in the application device
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure of the application device that integrates the module) so that it provides good thermal dissipation
- Force ventilation air-flow within mechanical enclosure

[8] Refer to SARA-G3 series Data Sheet [1] for the $R_{th,M-A}$ value in this application condition
[9] Temperature is measured by internal sensor of wireless module
[10] Steady state thermal equilibrium is assumed. The module's temperature in idle state can be considered equal to ambient temperature

- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the wireless module

For example, after the installation of a robust aluminum heat-sink with forced air ventilation on the back of the same application board described above, the Module-to-Ambient thermal resistance ($R_{th,M-A}$) is reduced up to the Module-to-Case thermal resistance ($R_{th,M-C}$) defined in the SARA-G3 series Data Sheet [1]. The effect of lower $R_{th,M-A}$ can be seen from the module temperature increase, which now can be summarized as following:

- ~1 °C during a GSM voice call (1 TX slot, 1 RX slot) at the maximum TX power
- ~2 °C during a GPRS data transfer (2 TX slots, 3 RX slots) at the maximum TX power

Beside the reduction of the Module-to-Ambient thermal resistance implemented by the hardware design of the application device integrating a SARA-G3 series module, the increase of module temperature can be moderated by the software implementation of the application.

Since the most critical condition concerning module thermal power occurs when module connected-mode is enabled, the actual module thermal power depends, as module current consumption, on the radio access mode (GSM / GPRS), the operating band and the average TX power.

A few software techniques may be implemented to reduce the module temperature increase in the application:

- Select by means of AT command (refer to the u-blox AT Commands Manual [2], +UCLASS command) the module's GPRS multi-slot class which provides lower current consumption (refer to current consumption values reported in the SARA-G3 series Data Sheet [1])
- Select by means of AT command (refer to the u-blox AT Commands Manual [2], +UBANDSEL command) the operating band which provides lower current consumption (refer to current consumption values reported in the SARA-G3 series Data Sheet [1])
- Enable module connected-mode for a given time period and then disable it for a time period enough long to properly mitigate temperature increase

2.12 ESD guidelines

2.12.1 ESD immunity test overview

The immunity of devices integrating SARA-G3 series modules to Electro-Static Discharge (ESD) is part of the Electro-Magnetic Compatibility (EMC) conformity which is required for products bearing the CE marking, compliant with the R&TTE Directive (99/5/EC), the EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with these directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 [15] and the radio equipment standards ETSI EN 301 489-1 [16], ETSI EN 301 489-7 [17], ETSI EN 301 489-24 [18], which requirements are summarized in Table 38.

The ESD immunity test is performed at the enclosure port, defined by ETSI EN 301 489-1 [16] as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of ESD immunity test to the whole device depends on the device classification as defined by ETSI EN 301 489-1 [16]. Applicability of ESD immunity test to the relative device ports or the relative interconnecting cables to auxiliary equipments, depends on device accessible interfaces and manufacturer requirements, as defined by ETSI EN 301 489-1 [16].

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in CENELEC EN 61000-4-2 [15].

☞ For the definition of integral antenna, removable antenna, antenna port, device classification refer to ETSI EN 301 489-1 [16].

☞ CENELEC EN 61000-4-2 [15] defines the contact and air discharges.

Application	Category	Immunity Level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Contact Discharge	4 kV
	Air Discharge	8 kV

Table 38: Electro-Magnetic Compatibility ESD immunity requirements as defined by CENELEC EN 61000-4-2, ETSI EN 301 489-1, ETSI EN 301 489-7, ETSI EN 301 489-24

2.12.2 ESD immunity test of u-blox SARA-G3 series reference designs

Although Electro-Magnetic Compatibility (EMC) certification is required for customized devices integrating SARA-G3 series modules for R&TTED and European Conformance CE mark, EMC certification (including ESD immunity) has been successfully performed on SARA-G3 series modules reference design according to CENELEC EN 61000-4-2 [15], ETSI EN 301 489-1 [16], ETSI EN 301 489-7 [17], ETSI EN 301 489-24 [18] European Norms.

The EMC / ESD approved u-blox reference designs consist of a SARA-G3 series module soldered onto a motherboard which provides supply interface, SIM card, headset and communication port. An external antenna is connected to an SMA connector provided on the motherboard for the GSM antenna.

Since an external antenna is used, the antenna port can be separated from the enclosure port. The reference design is not enclosed in a box so that the enclosure port is not indentified with physical surfaces. Therefore, some test cases cannot be applied. Only the antenna port is identified as accessible for direct ESD exposure.

☞ u-blox SARA-G3 series reference design implement all the ESD precautions described in section 2.12.3.

Table 39 reports the u-blox SARA-G3 series reference designs ESD immunity test results, according to test requirements stated in the CENELEC EN 61000-4-2 [15], ETSI EN 301 489-1 [16], ETSI EN 301 489-7 [17] and ETSI EN 301 489-24 [18].

Category	Application	Immunity Level	Remarks
Contact Discharge to coupling planes (indirect contact discharge)	Enclosure	+4 kV / -4 kV	
Contact Discharges to conducted surfaces (direct contact discharge)	Enclosure port	Not Applicable	Test not applicable to u-blox reference design because it does not provide enclosure surface. The test is applicable only to equipments providing conductive enclosure surface.
	Antenna port	+4 kV / -4 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with conductive surface.
Air Discharge at insulating surfaces	Enclosure port	Not Applicable	Test not applicable to the u-blox reference design because it does not provide an enclosure surface. The test is applicable only to equipments providing insulating enclosure surface.
	Antenna port	+8 kV / -8 kV	Test applicable to u-blox reference design because it provides antenna with conductive & insulating surfaces. The test is applicable only to equipments providing antenna with insulating surface.

Table 39: Enclosure ESD immunity level of u-blox SARA-G3 series modules reference designs

2.12.3 ESD application circuits

The application circuits described in this section are recommended and should be implemented in the device integrating SARA-G3 series modules, according to the application board classification (see ETSI EN 301 489-1 [16]), to satisfy the requirements for ESD immunity test summarized in Table 38.

Antenna interface

The **ANT** pin of SARA-G3 series modules provides ESD immunity up to ±4 kV for direct Contact Discharge and up to ±8 kV for Air Discharge: no further precaution to ESD immunity test is needed, as implemented in the EMC / ESD approved reference design of SARA-G3 series modules.

The antenna interface application circuit implemented in the EMC / ESD approved reference designs of SARA-G3 series modules is described in Figure 37 in case of antenna detection circuit not implemented, and is described in Figure 38 and Table 22 in case of antenna detection circuit implemented (section 2.3).

RESET_N pin

The following precautions are suggested for the **RESET_N** line of SARA-G3 series modules, depending on the application board handling, to satisfy ESD immunity test requirements:

- It is recommended to keep the connection line to **RESET_N** as short as possible

Maximum ESD sensitivity rating of the **RESET_N** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the **RESET_N** pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the **RESET_N** line, close to accessible point

The **RESET_N** application circuit implemented in the EMC / ESD approved reference designs of SARA-G3 series modules is described in Figure 32 and Table 20 (section 2.2.2).

SIM interface

The following precautions are suggested for SARA-G3 series modules SIM interface (**VSIM**, **SIM_RST**, **SIM_IO**, **SIM_CLK** pins), depending on the application board handling, to satisfy ESD immunity test requirements:

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470J) must be mounted on the lines connected to **VSIM**, **SIM_RST**, **SIM_IO** and **SIM_CLK** pins to assure SIM interface functionality when an electrostatic discharge is applied to the application board enclosure
- It is suggested to use as short as possible connection lines at SIM pins

Maximum ESD sensitivity rating of SIM interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if SIM interface pins are externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Tyco Electronics PESD0402-140) should be mounted on each SIM interface line, close to accessible points (i.e. close to the SIM card holder)

The SIM interface application circuit implemented in the EMC / ESD approved reference designs of SARA-G3 series modules is described in Figure 42 and Table 25 (section 2.4).

Other pins and interfaces

All the module pins that are externally accessible on the device integrating SARA-G3 series module should be included in the ESD immunity test since they are considered to be a port as defined in ETSI EN 301 489-1 [16]. Depending on applicability, to satisfy ESD immunity test requirements according to ESD category level, all the module pins that are externally accessible should be protected up to ±4 kV for direct Contact Discharge and up to ±8 kV for Air Discharge applied to the enclosure surface.

The maximum ESD sensitivity rating of all the other pins of the module is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the relative pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG or EPCOS CT0402S14AHSG varistor) should be mounted on the relative line, close to accessible point

2.13 Schematic for SARA-G3 series module integration

Figure 61 is an example of a schematic diagram where a SARA-G350 module is integrated into an application board, using all the available interfaces and functions of the module.

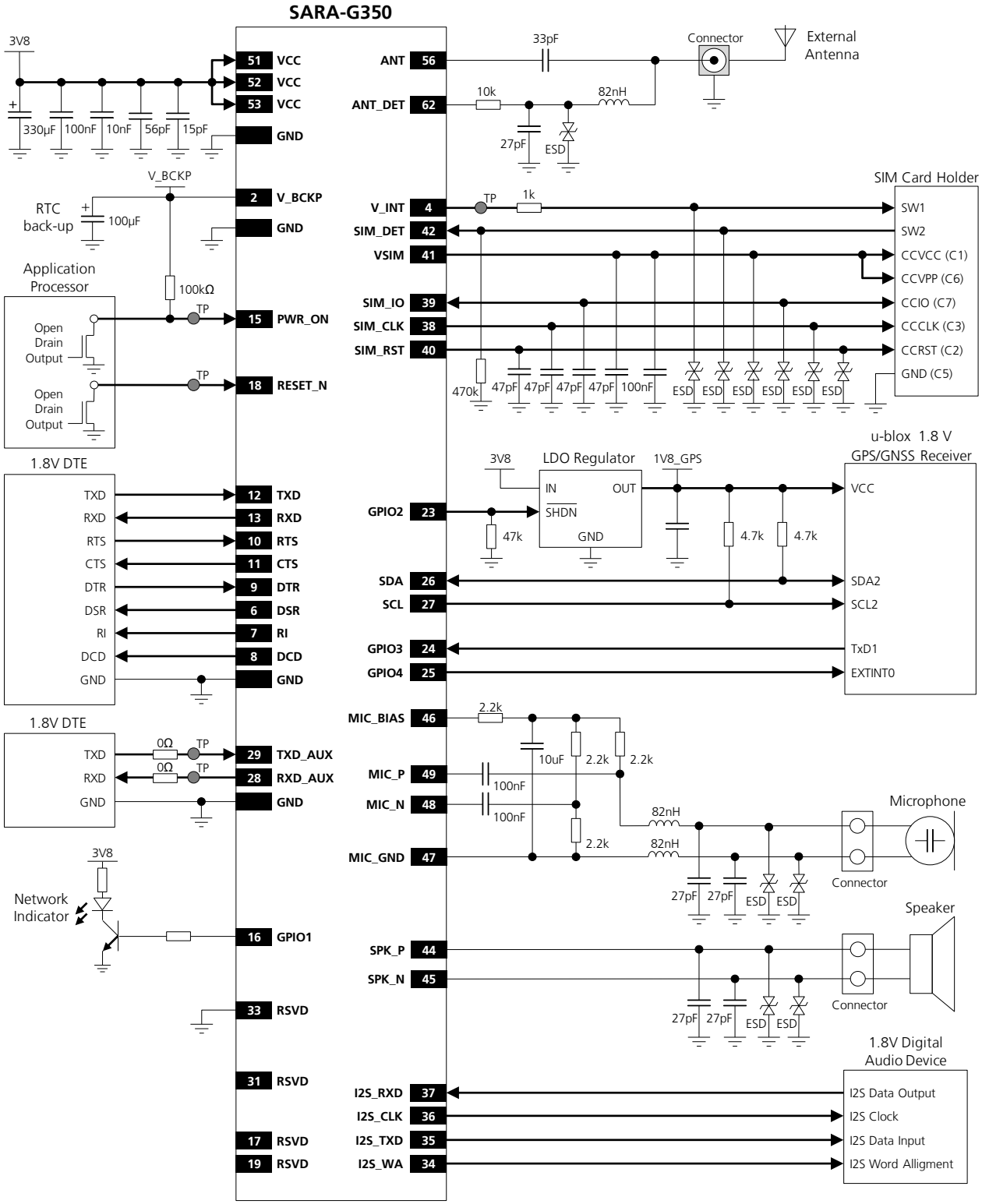


Figure 61: Example of schematic diagram to integrate SARA-G350 module in an application board, using all the interfaces

Figure 62 is an example of a schematic diagram where a SARA-G300 / SARA-G310 module is integrated into an application board, using all the available interfaces and functions of the module.

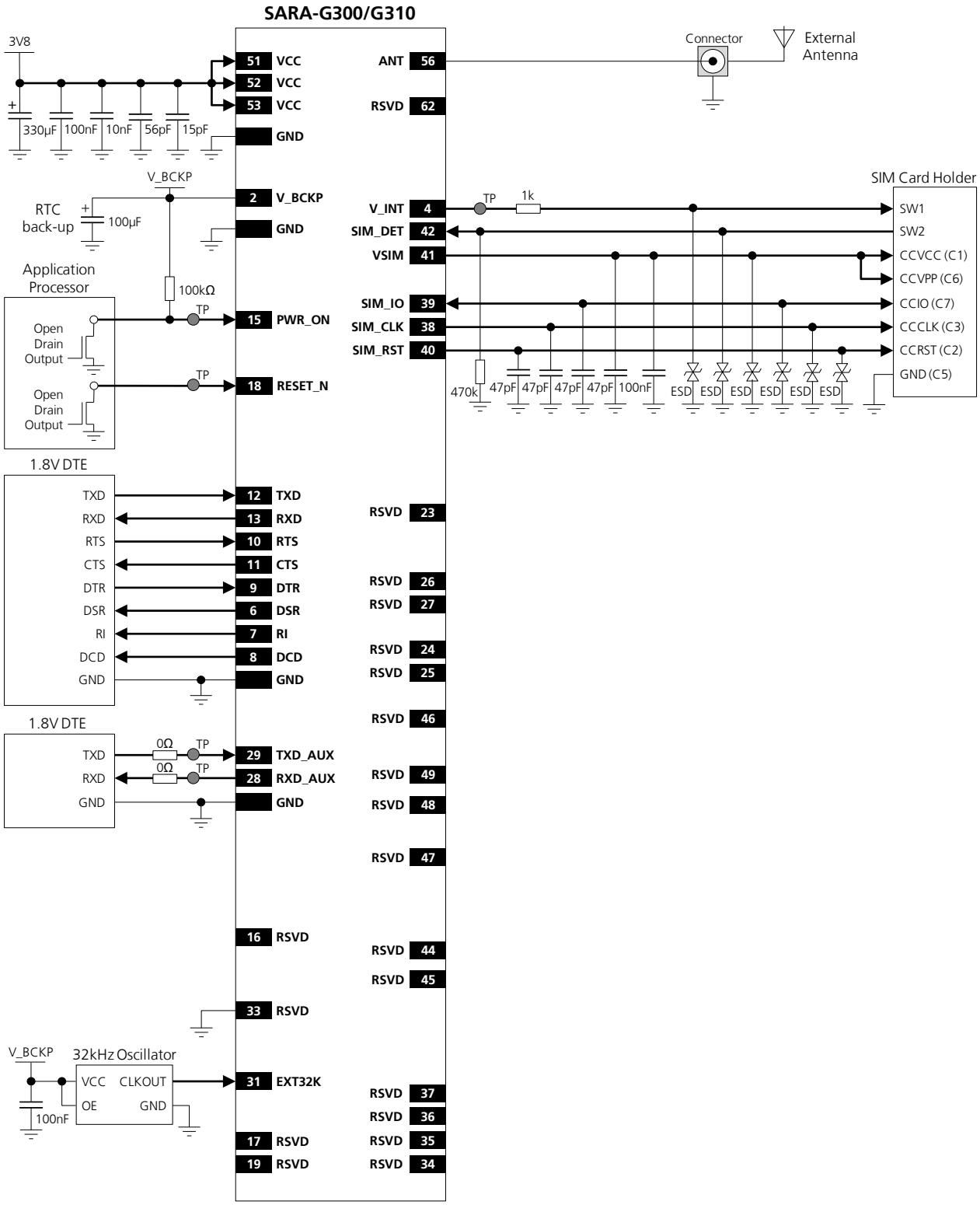


Figure 62: Example of schematic diagram to integrate SARA-G300/G310 modules in an application board, using all the interfaces

2.14 Design-in checklist

This section provides a design-in checklist.

2.14.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin above the minimum operating range limit.
- ☑ DC supply must be capable of providing 1.9 A current pulses, providing a voltage at **VCC** pin above the minimum operating range limit and with a maximum 400 mV voltage drop from the nominal value.
- ☑ **VCC** supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ **VCC** voltage must ramp from 2.5 V to 3.2 V within 4 ms to allow a proper switch-on of the module.
- ☑ Do not leave **PWR_ON** floating: fix properly the level, e.g. adding a proper pull-up resistor to **V_BCKP**.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, since the signal names follow the ITU-T V.24 Recommendation [9].
- ☑ Provide accessible testpoints directly connected to the following pins: **TXD_AUX** and **RXD_AUX** pins, **V_INT** pin, **PWR_ON** and/or **RESET_N** pins, to allow the module firmware upgrade using the u-blox EasyFlash tool and to allow the trace log capture (debug purpose).
- ☑ Add a proper pull-up resistor (e.g. 4.7 kΩ) to **V_INT** or another proper 1.8 V supply on each DDC (I^2C) interface line, if the interface is used.
- ☑ Capacitance and series resistance must be limited on each line of the DDC (I^2C) interface.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Connect the pin number 33 (**RSVD**) to ground.
- ☑ Insert the suggested passive filtering parts on each used analog audio line.
- ☑ Check the digital audio interface specifications to connect a proper device.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ Any external signal connected to the UART interface, auxiliary UART interface, I^2S interfaces and GPIOs must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and let a proper boot of the module.
- ☑ All unused pins can be left unconnected except the **PWR_ON** pin (its level must be properly fixed, e.g. adding a 100 kΩ pull-up to **V_BCKP**) and the **RSVD** pin number 33 (it must be connected to GND).

2.14.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** pad (antenna RF input/output interface).
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (primarily analog audio input/output signals, SIM signals, high-speed digital lines).
- ☑ **VCC** line should be wide and short.
- ☑ Route **VCC** supply line away from sensitive analog signals.
- ☑ Ensure proper grounding.
- ☑ Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.
- ☑ Route analog audio signals away from noisy sources (primarily RF interface, **VCC**, switching supplies).
- ☑ The audio outputs lines on the application board must be wide enough to minimize series resistance.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.

2.14.3 Antenna checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Follow the additional guidelines for products marked with the FCC logo (United States only) reported in chapter 2.3.1.2 and 4.2.2
- ☑ Follow the guidelines in chapter 2.3.2 to get proper antenna detection functionality, if required.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the SARA-G3 series Data Sheet [1] and the u-blox Package Information Guide [25].

The SARA-G3 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ **Ensure ESD precautions are implemented during handling of the module.**

3.2 Soldering

3.2.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.10

☞ The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

3.2.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Reflow profiles are to be selected according to the following recommendations.

⚠ **Failure to observe these recommendations can result in severe damage to the device!**

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200 °C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of 217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217 °C liquidus temperature: 40 - 60 s
- Peak reflow temperature: 245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

⚠ **Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.**

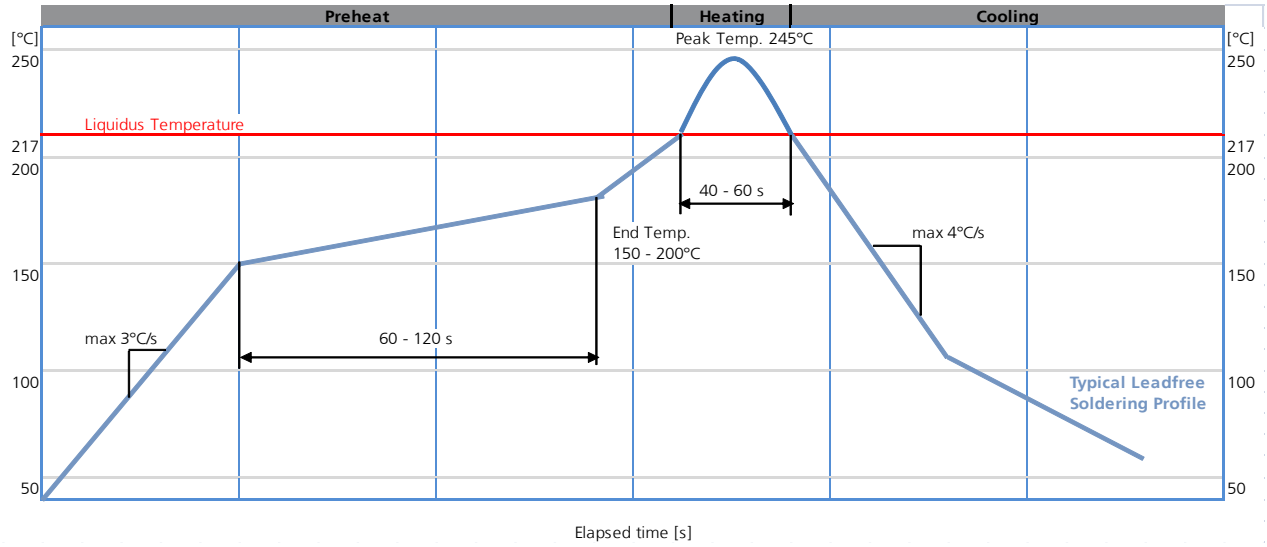


Figure 63: Recommended soldering profile

☞ SARA-G3 series modules must not be soldered with a damp heat process.

3.2.3 Optical inspection

After soldering the SARA-G3 series modules, inspect the modules optically to verify that the module is properly aligned and centered.

3.2.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.2.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a SARA-G3 series module populated on it. The reason for this is the risk of the module falling off due to high weight in relation to the adhesive properties of the solder.

3.2.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with SARA-G3 series modules.

3.2.7 Hand soldering

Hand soldering is not recommended.

3.2.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.2.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the SARA-G3 series modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.2.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the SARA-G3 series modules before implementing this in the production.

☞ Casting will void the warranty.

3.2.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the SARA-G3 series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.2.12 Use of ultrasonic processes

SARA-G3 series modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the SARA-G3 series modules caused by any Ultrasonic Processes.

4 Approvals

For the complete list of all the certification schemes approvals of SARA-G3 series modules and the corresponding declarations of conformity, refer to the u-blox web-site (http://www.u-blox.com).

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called "certification schemes" that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, as:
    - CE (Conformité Européenne) marking for European Union
    - FCC (Federal Communications Commission) approval for United States
- Industry certification
  - Telecom industry specific approval verifying the interoperability between devices and networks:
    - GCF (Global Certification Forum), partnership between European device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator specific approval required by some mobile network operator, as:
    - AT&T network operator in United States

Even if SARA-G3 modules are approved under all major certification schemes, the application device that integrates SARA-G3 modules must be approved under all the certification schemes required by the specific application device to be deployed in the market.

The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device that integrates SARA-G3 series modules must be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device must operate.

The certification of the application device that integrates a SARA-G3 module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

SARA-G3 modules are certified according to all capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to 3GPP TS 51.010-2 [14], is a statement of the implemented and supported capabilities and options of a device.

The PICS document of the application device integrating a SARA-G3 module must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device, as for the following cases:

- if any RF band is disabled by AT+UBANDSEL command
- if the automatic network attach is disabled by AT+COPS command
- if the module's GPRS multi-slot class is changed by AT+UCLASS command

4.2 Federal Communications Commission and Industry Canada notice

Federal Communications Commission (FCC) ID:

- XPYSARAG350

Industry Canada (IC) Certification Number:

- 8595A-SARAG350

4.2.1 Safety Warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed

4.2.2 Declaration of Conformity – United States only

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for the SARA-G3 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 8.39 dBi (850 MHz) and 3.11 dBi (1900 MHz) for mobile and fixed or mobile operating configurations.

4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the SARA-G3 series modules are authorized to use the FCC Grants and Industry Canada Certificates of the SARA-G3 series modules for their own final products according to the conditions referenced in the certificates.

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPYSARAG350" resp.

The IC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains IC: 8595A-SARAG350" resp.

Canada, Industry Canada (IC) Notices

This Class B digital apparatus complies with Canadian ICES-003 and RSS-210.

Operation is subject to the following two conditions:

- **this device may not cause interference**

- **this device must accept any interference, including interference that may cause undesired operation of the device**

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Wireless Module is below the Industry Canada (IC) radio frequency exposure limits. The u-blox Wireless Module should be used in such a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address: http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng

Additional Canadian information on RF exposure also can be found at the following web address: http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: Manufacturers of portable applications incorporating the SARA-G3 series modules are required to have their final product certified and apply for their own FCC Grant and Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canada, avis d'Industrie Canada (IC)

Cet appareil numérique de classe B est conforme aux normes canadiennes ICES-003 et RSS-210.

Son fonctionnement est soumis aux deux conditions suivantes:

- **cet appareil ne doit pas causer d'interférence**
- **cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement**

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans fil u-blox Wireless Module est inférieure à la limite d'exposition aux fréquences radio d'Industrie Canada (IC). Utilisez l'appareil de sans fil u-blox Wireless Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur:

http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: les fabricants d'applications portables contenant les modules SARA-G3 series doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat Industrie Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.3 R&TTED and European Conformance CE mark

This device has been evaluated against the essential requirements of the 1999/5/EC Directive.

In order to satisfy the essential requirements of 1999/5/EC Directive, the module is compliant with the following standards:

- Radio Frequency spectrum use (R&TTE art. 3.2):
  - EN 301 511 V9.0.2
- Electromagnetic Compatibility (R&TTE art. 3.1b):
  - EN 301 489-1 V1.9.2
  - EN 301 489-7 V1.4.1
- Health and Safety (R&TTE art. 3.1a)
  - EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + AC:2011
  - EN 62311:2008

The conformity assessment procedure referred to in Article 10 and detailed in Annex IV of Directive 1999/5/EC has been followed with the involvement of the following Notified Body No: 1909

Thus, the following marking is included in the product:

CE 1909

There is no restriction for the commercialisation of this device in all the countries of the European Union.

5 Product Testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (Serial interface communication, analog audio interface, real time clock, temperature sensor, antenna detection, SIM card communication)
- Digital tests (GPIOs, digital interfaces)
- Measurement and calibration of RF characteristics in all supported bands (Receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels)
- Verification of RF characteristics after calibration (modulation accuracy, power levels and spectrum performance are checked to be within tolerances when calibration parameters are applied)

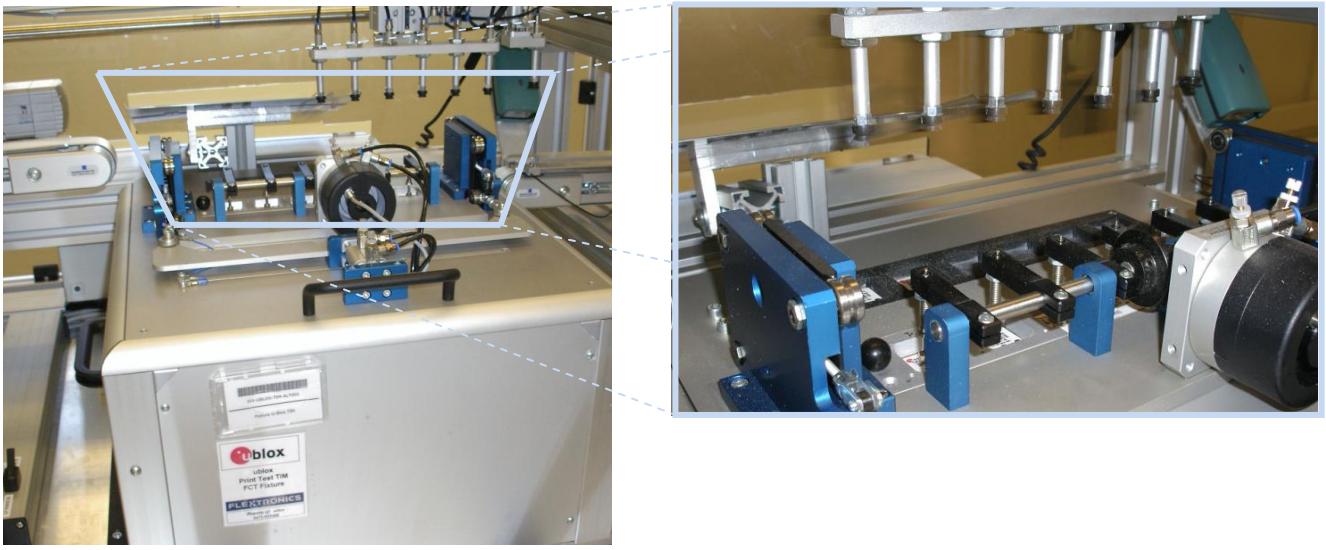


Figure 64: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damaged the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins

- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

Module AT commands are used to perform functional tests (communication with host controller, check SIM card interface, check communication between module and GPS/GNSS, GPIOs, etc.) and to perform RF performance tests.

5.2.1 "Go/No go" tests for integrated devices

A 'Go/No go' test is to compare the signal quality with a "Golden Device" in a position with excellent network coverage and after having dialed a call (refer to u-blox AT Commands Manual [2], AT+CSQ command: <rssi>, <ber> parameters).

☞ These kinds of test may be useful as a 'go/no go' test but not for RF performance measurements.

This test is suitable to check the communication with host controller and SIM card, the audio and power supply functionality and verify if components at antenna interface are well soldered.

5.2.2 Functional tests providing RF operation

Overall RF performance test of the device including antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator using AT+UTEST command over AT interface.

The AT+UTEST command gives a simple interface to set the module to Rx and Tx test modes ignoring GSM/GPRS signaling protocol. The command can set the module:

- In transmitting mode in a specified channel and power level in all supported modulation schemes (single slot GMSK) and bands
- In receiving mode in a specified channel to returns the measured power level in all supported bands

☞ Refer to the u-blox AT Commands Manual [2], for AT+UTEST command syntax description.

☞ Refer to the End user test Application Note [24], for AT+UTEST command user guide, limitations and examples of use.

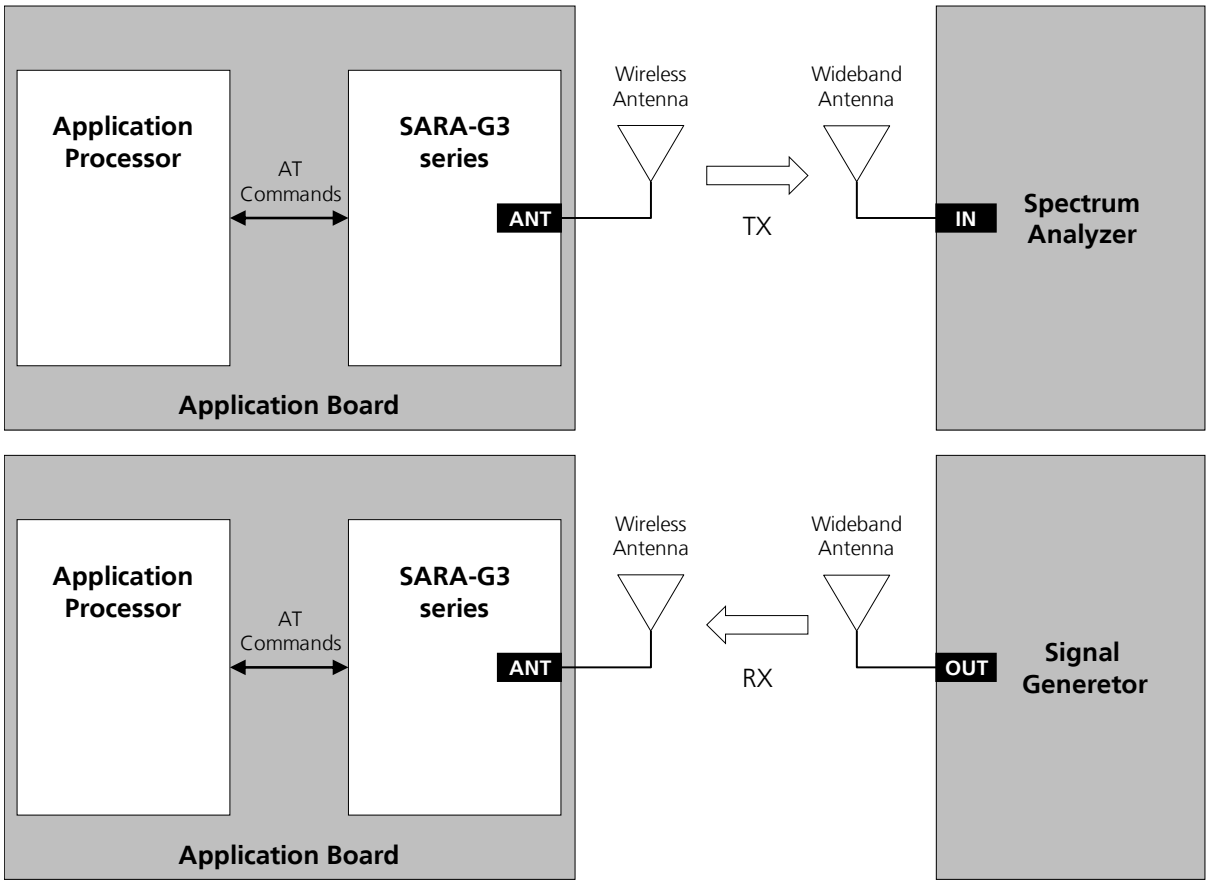


Figure 65: Setup with spectrum analyzer and signal generator for radiated measurement

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces from which depends the RF performance.

To avoid module damage during transmitter test, a proper antenna according to module specifications or a 50 Ω termination must be connected to ANT pin.

To avoid module damage during receiver test the maximum power level received at ANT pin must meet module specifications.

The AT+UTEST command sets the module to emit RF power ignoring GSM/GPRS signalling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purpose in controlled environments by qualified user and must not be used during the normal module operation. Follow instructions suggested in u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Example of production tests for OEM manufacturer:

1. Trigger TX GMSK burst at low Power Control Level (lower than 15) or a RX measure reporting to check:
   - If **ANT** pin is soldered
   - If **ANT** pin is in short circuit
   - If the module was damaged during soldering process or during handling (ESD, mechanical shock…)
   - If antenna matching components on application board are soldered
   - If integrated antenna is correctly connected

To avoid module damage during transmitter test when good antenna termination is not guaranteed, use a low Power Control Level (i.e. PCL lower or equal to 15). u-blox assumes no responsibilities for module damaging caused by an inappropriate use of this feature.

2. Trigger TX GMSK burst at maximum PCL:
   - To check if the power supply is correctly assembled and is able to deliver the required current

3. Trigger TX GMSK burst:
   - To measure current consumption
   - To check if module components were damaged during soldering process or during handling (ESD, mechanical shock…)

4. Trigger RX measurement:
   - To test receiver signal level. Assuming that there are no losses between **ANT** pin and input power source, be aware that the power level estimated by the module can vary approximately within 3GPP tolerances for the average value
   - To check if module was damaged during soldering process or during handling (ESD, mechanical shock…)

5. Trigger TX GMSK burst and RX measurement to check:
   - Overall RF performance of the device including antenna measuring TX and RX power levels

Appendix

A Migration between LISA and SARA modules

A.1 Overview

Migrating between LISA-U1, LISA-U2, LISA-C2 series and SARA-G3 series wireless modules designs is a fairly procedure that allows customers to take maximum advantage of their hardware and software investments.

SARA-G3 wireless modules (26.0 x 16.0 mm LGA) have a different form factor than LISA wireless modules (33.2 x 22.4 mm LCC), but the footprint for each SARA and LISA module has been developed so that all the pads on the same lateral edge of the antenna pin can be shared on the application board, due to the same pitch and nearly the same functions provided, as described in Figure 66.

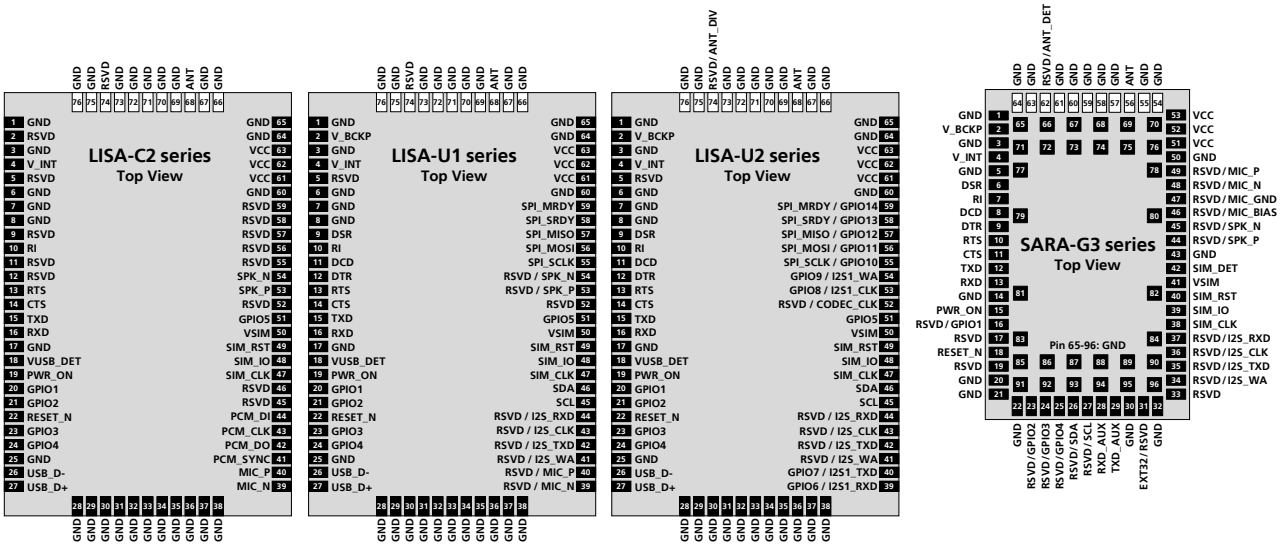


Figure 66: LISA series vs. SARA-G3 series modules pin assignment: highlighted pads that can be shared on the application board

This is the basis of the Nested Design concept: any SARA-G3, any LISA-U1, any LISA-U2, any LISA-C2 module can be alternatively mounted on the same nested board as shown in Figure 67, enabling straightforward development of products supporting either GSM/GPRS, W-CDMA or CDMA wireless technology with the same application board.

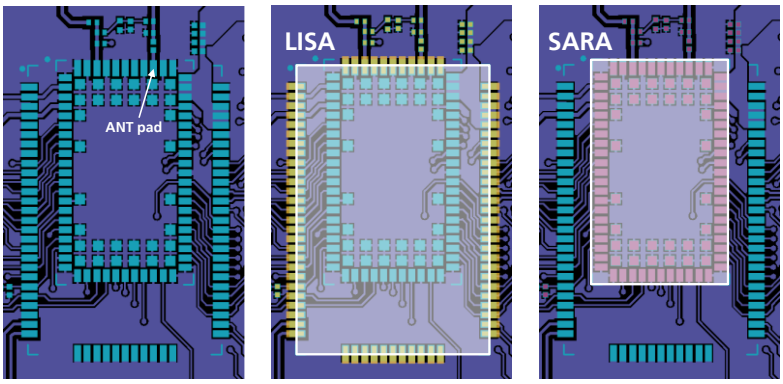


Figure 67: Nested Design concept description: LISA and SARA modules alternatively mounted on the same application board

The voltage level of all the digital interfaces of SARA-G3 and LISA modules is 1.8 V: this allows the direct connection from a 1.8 V external device (e.g. application processor) to all the modules.

The following chapters explains in details all the points to consider during the migration between LISA and SARA designs, implementing or not a nested design

For further details regarding SARA-G3 and LISA modules characteristics, usage, settings refer to the relative module datasheet [1], [3], [4], [5], System Integration Manual [6], [7], and AT commands manual [2], [8].

A.2 Checklist for migration

Have you chosen the optimal SARA-G3 series module?

- ☑ For quad-band GSM/GPRS class 12, full feature set, select the SARA-G350 module.
- ☑ For quad-band GSM/GPRS class 2, reduced feature set, select the SARA-G310 module.
- ☑ For dual-band GSM/GPRS class 2, reduced feature set, select the SARA-G300 module.

Check SARA-G3 series modules hardware requirements

- ☑ Check power capabilities of the external supply circuit: SARA-G3 modules require large current pulses in connected-mode as well as LISA-U series modules when a 2G call is enabled. LISA-C2 series modules do not require large current pulses due to the CDMA channel access technology.
- ☑ Check supported bands for proper antenna circuit development: SARA-G3 modules frequency ranges are within LISA-U modules ranges, but LISA-C2 modules range is quite different.
- ☑ Check antenna detection requirements: SARA-G350 modules provide the antenna detection function implementing an external application circuit between **ANT_DET** and **ANT** pins.
- ☑ Check the module power-on requirements: Table 40 and relative section summarize differences between SARA-G3 series and LISA modules.
- ☑ Check the module requirements to enter low power idle-mode: SARA-G300 and SARA-G310 modules require an external 32 kHz signal at **EXT32K** input pin.
- ☑ Check serial interfaces requirements: SARA-G3 modules provide UART interface for AT command, data communication, multiplexer functionality, FW upgrade over AT and provide auxiliary UART interface for FW upgrade using the u-blox EasyFlash tool and for Trace log capture (debug purpose).
- ☑ Check analog audio requirements: SARA-G350 modules do not provide DC blocking capacitors at the **MIC_P** / **MIC_N** input pins and provide supply output and local ground for an external microphone at the **MIC_BIAS** / **MIC_GND** pins.
- ☑ Check digital audio requirements: SARA-G350 modules provide a 4-wire 1.8 V interface supporting PCM and Normal I2S modes, master role and fixed sample rate.
- ☑ Check internal active pull-up / down values at digital interface input pins and the current capability of digital interface output pins, since they are slightly different between SARA-G3 and LISA modules.

Check SARA-G3 series modules software requirements

- ☑ Not all of the functionalities available with LISA modules are supported by all the SARA-G3 modules versions. SARA-G300 and SARA-G310 modules do not support:
  - Audio interfaces, DDC (I^2C) interface, Antenna detection interface, GPIOs
  - Low power idle-mode, if an external 32 kHz signal at **EXT32K** input pin is not provided
  - TCP/IP, UDP/IP, FTP, HTTP
  - GPS/GNSS via Modem, AssistNow clients, Hybrid positioning and CellLocate™ functionalities
  - Jamming detection

A.3 Software migration

Software migration between SARA-G3 and LISA wireless modules is a straightforward procedure. Nevertheless there are some differences to be considered with firmware version. Each wireless module supports AT commands according to 3GPP standards: TS 27.007 [10], TS 27.005 [11], TS 27.010 [12] and the u-blox AT command extension. Backward compatibility has been maintained as far as possible.

☞ For the complete list of supported AT commands and their syntax refer to the relative AT commands manual of the module [2], [8].

A.4 Hardware migration

SARA-G3 series modules have been designed with backward compatibility to LISA series modules in mind but some minor differences were unavoidable. These minor differences are however not relevant for the majority of the designs.

The following subchapters describe the hardware differences between the interfaces of SARA-G3 series modules and LISA series modules while Table 41 summarizes the detailed differences between the pins.

A.4.1 Supply interfaces

Module supply input (VCC)

The same compatible external circuit can be implemented for SARA-G3 and LISA even if there are minor differences in the **VCC** input voltage ranges and some differences in the current consumption figures.

The voltage provided must be within the normal operating range limits to allow module switch-on and must be above the minimum limit of the extended operating range to avoid module switch-off. For the detailed **VCC** input voltage ranges values refer to Table 41 or to the relative datasheet of the module [1], [3], [4], [5].

The SARA-G3 maximum average current consumption is lower than the LISA one due to the lower data rate or the different channel access technology. SARA-G3 modules require large current pulses in connected-mode as well as LISA-U series when a 2G call is enabled. LISA-C2 series do not require large current pulses due to the CDMA channel access technology. For the detailed current consumption values refer to the relative datasheet of the module [1], [3], [4], [5].

Detailed supply circuit design-in guidelines are reported in section 2.1.1 and in the relative System Integration Manual of the module [6], [7].

RTC supply input/output (V_BCKP)

The same compatible external circuit can be implemented for SARA-G3 series and LISA-U series even if there are minor differences in the **V_BCKP** typical output voltage and input voltage range as reported in Table 41 or in the relative datasheet of the module [1], [3], [4], [5]. LISA-C2 series do not provide **V_BCKP** RTC supply input/output as well as the whole RTC functionality.

Interfaces supply output (V_INT)

The same compatible external circuit can be implemented for SARA-G3 series and LISA series: there are no differences in the **V_INT** output characteristics.

A.4.2 System functions interfaces

Module power-on

SARA-G3 and LISA series power-on sequence is initiated in one of the ways summarized in Table 40. For more details refer to section 1.6.1 or to the relative System Integration Manual of the module [6], [7].

SARA-G3 series	LISA-C2 series	LISA-U1 series	LISA-U2 series
Rising edge on the **VCC** pins to a valid voltage as module supply	Rising edge on the **VCC** pins to a valid voltage as module supply with **PWR_ON** pin permanently low when **VCC** is applied	Rising edge on the **VCC** pins to a valid voltage as module supply	Rising edge on the **VCC** pins to a valid voltage as module supply
Low level on the **PWR_ON** pin for appropriate time period	Low pulse on the **PWR_ON** pin for appropriate time period	Low pulse on the **PWR_ON** pin for appropriate time period	Low pulse on the **PWR_ON** pin for appropriate time period
Pre-programmed RTC alarm (32 kHz signal at EXT32K input needed for SARA-G300/G310)		Pre-programmed RTC alarm	Pre-programmed RTC alarm
		RESET_N input pin released from the low level	**RESET_N** input pin released from the low level

Table 40: Summary of power on events among modules

The same compatible external power-on circuit can be implemented for SARA-G3 series and LISA series even if there are minor differences in the **PWR_ON** input voltage levels ranges and in the low level time or low pulse time to switch-on the module, as reported in Table 41 or in the relative datasheet of the module [1], [3], [4], [5]. **PWR_ON** falling edge (i.e. low pulse) is required for LISA series, but it is not required for SARA-G3 series. External pull-up is not needed for LISA-C2 series since internal pull-up is provided.

Module power-off

SARA-G3 and LISA modules can be all properly switched off by means of the AT+CPWROFF command.

All LISA-U2 modules except LISA-U200-00S modules can be additionally properly switched off by low pulse on **PWR_ON** pin, as reported in Table 41 or in the relative datasheet of the module [5].

Module reset

SARA-G3 series and LISA series modules reset can be performed in one of the following ways:

- Forcing a low level on the RESET_N pin, causing an "external" or "hardware" reset
- By means of the AT+CFUN command, causing an "internal" or "software" reset

The same compatible external reset circuit can be implemented for SARA-G3 series and LISA series even if there are minor differences in the **RESET_N** input voltage levels ranges and in the low level time, as reported in Table 41 or in the relative datasheet of the module [1], [3], [4], [5].

Additional precautions are suggested for the **RESET_N** line of LISA-U series modules, depending on the application board handling, to satisfy ESD immunity test requirements as described in the LISA-U Series System Integration Manual [7].

External 32 kHz input

The external 32 kHz signal input pin (**EXT32K**) is available only on the SARA-G300 and SARA-G310 modules to provide the 32 kHz reference clock for the Real Time Clock (RTC) timing, used by the module processor to reach the low power idle-mode and provide the RTC functions.

SARA-G350 and LISA-U modules are equipped with internal 32 kHz oscillator to provide the same functions.

LISA-C2 series do not provide RTC and the relative functions.

A.4.3 Antenna interface

RF interface for Tx/Rx antenna

The same compatible external circuit can be implemented for SARA-G3 series and LISA series **ANT** pin even if there are some differences in the operating bands frequency ranges as summarized in Figure 68.

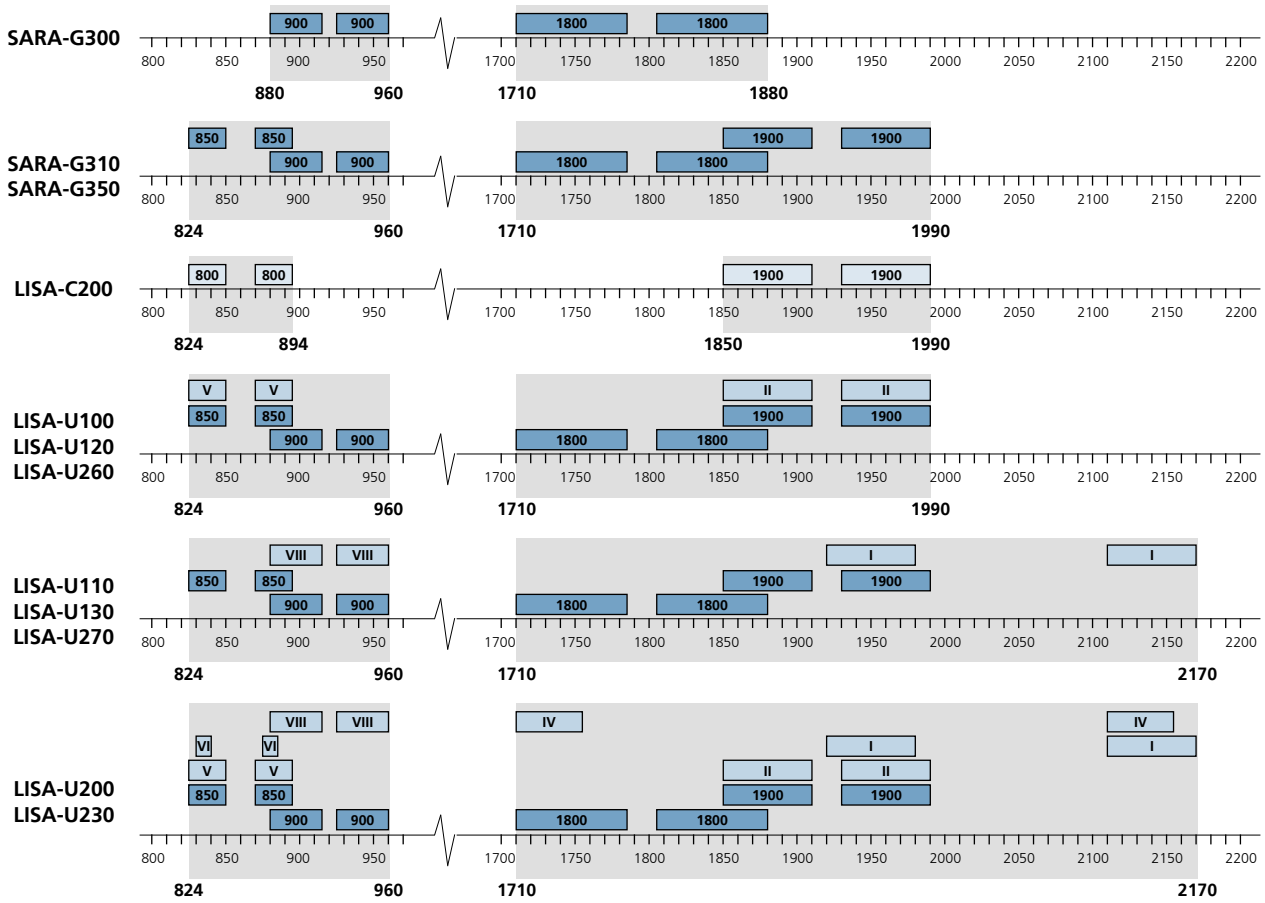


Figure 68: Summary of operating bands frequency ranges among modules

An external application circuit can be implemented on the application device integrating LISA-U2 series modules to satisfy ESD immunity test requirements at the antenna port, as described in the LISA-U Series System Integration Manual [7]. The same application circuit is not applicable for SARA-G3 series, LISA-U1 series and LISA-C2 series.

RF interface for Rx diversity antenna

Only the LISA-U230 modules provide the RF input for Rx diversity antenna (**ANT_DIV**).

SARA-G3, LISA-C2, LISA-U1 and the other LISA-U2 series modules do not support Rx diversity.

Antenna detection interface

An external application circuit can be implemented on the application device integrating SARA-G350 modules to provide antenna detection functionality, with a proper connection between the **ANT_DET** pin and the **ANT** pin, as described in section 2.3.2.

LISA-U modules are equipped with internal circuit for antenna detection support.

SARA-G300, SARA-G310 and LISA-C2 series modules do not support antenna detection.

A.4.4 SIM interface

SIM interface

The same compatible external circuit can be implemented for SARA-G3 and LISA modules: 1.8 V and 3.0 V SIM card / IC are supported. LISA-C2 modules do not need an external SIM for Sprint and Verizon mobile operators. LISA-C2 series SIM interface is hardware ready but the support of external SIM card / IC will be provided by the upcoming firmware releases.

SIM detection interface

The same compatible external circuit can be implemented for SARA-G3 and LISA modules: SIM detection function is provided by the **SIM_DET** pin on SARA-G3 modules and by the **GPIO5** pin on LISA-U modules. SIM card hot insertion/removal is additionally supported by all LISA-U2 series except LISA-U200-00S.

LISA-C2 modules do not support SIM detection.

A.4.5 Serial interfaces

UART interface

The same compatible external circuit can be implemented for SARA-G3 and LISA modules: 1.8 V unbalanced asynchronous serial port with RS-232 functionality is provided on SARA-G3 modules (for AT command, data communication, MUX functionality, FW upgrade over AT), LISA-C2 modules (for AT command, data communication, MUX functionality), LISA-U modules (for AT command, data communication, MUX functionality, FW upgrade over AT or using the u-blox EasyFlash tool).

LISA-C2 modules do not support **DSR**, **DCD** and **DTR** functions.

Table 41 and in relative datasheet of the module [1], [3], [4], [5] report minor differences in the internal pull-ups and drivers strengths.

These are the default settings of the UART interfaces:

- SARA-G3 modules: automatic baud rate and frame format detection
- LISA-U2 except LISA-U200-00S modules: one-shot automatic baud rate and frame format detection
- LISA-C2, LISA-U1 and LISA-U200-00S modules: 115200 b/s baud rate and 8N1 frame format

For further details regarding UART interface settings refer to the relative datasheet of the module [1], [3], [4], [5] and to the relative AT commands manual of the module [2], [8].

UART AUX interface

Only the SARA-G3 modules provide auxiliary UART interface for FW upgrade using the u-blox EasyFlash tool and for Trace log capture (debug purpose).

LISA modules do not provide auxiliary UART interface.

USB interface

SARA-G3 modules do not provide USB interface that is available on LISA-U modules (High-Speed USB 2.0 for AT command, data communication, FW upgrade over AT or using the u-blox EasyFlash tool, and for Trace log capture) and on LISA-C2 modules (Full-Speed USB 2.0 for AT command, Data communication, FW upgrade).

SPI interface

SARA-G3 and LISA-C2 modules do not provide SPI interface that is available on LISA-U modules (5-wire IPC interface for AT command, data communication, MUX functionality, FW upgrade over AT).

DDC (I^2C) interface

The same compatible external circuit can be implemented for SARA-G350 and LISA series: 1.8 V DDC (I^2C bus compatible) interface is provided to communicate with u-blox GPS/GNSS receivers.

SARA-G300, SARA-G310 and LISA-U200-00S modules do not support DDC (I^2C) interface.

LISA-C2 modules will support DDC (I^2C) interface by the upcoming firmware releases.

All LISA-U2 except LISA-U200-00S modules additionally support the communication with I^2C slaves other then u-blox positioning receivers over the same DDC (I^2C) interface, by means of dedicated AT commands.

A.4.6 Audio interfaces

Analog audio interfaces

Differential analog audio input is provided on the **MIC_P** / **MIC_N** pins of SARA-G350 modules (without internal DC blocking capacitor) and LISA-C2 series, LISA-U120, LISA-U130 modules (with internal DC blocking capacitor).

Supply output and local ground for an external microphone is provided on the **MIC_BIAS** / **MIC_GND** pins of SARA-G350 modules only: the supply for an external microphone has to be provided by an external LDO linear regulator with the other modules.

Differential analog audio output is provided on the **SPK_P** / **SPK_N** pins of SARA-G350, LISA-U120, LISA-U130 modules (16 ohm load capable) and LISA-C2 series modules (32 ohm load capable).

SARA-G300/G310, LISA-U100/U110, LISA-U200-00S modules do not provide analog audio interfaces.

LISA-U2 series modules do not provide analog audio interfaces but analog audio can be provided with external audio codec connected to a digital audio interface of all LISA-U2 series except LISA-U200-00S modules (e.g. the 4-wire I^2S digital audio interface provided instead of the 4 analog audio pins). The modules provide control of the external codec by means of the I^2C interface and clock reference by means of the **CODEC_CLK** pin.

For further details regarding analog audio interfaces characteristics, usage, settings refer to the relative module datasheet [1], [3], [4], [5], System Integration Manual 1.10.1, 2.6.1, [6], [7], and AT commands manual [2], [8].

Digital audio interfaces

Digital audio interface is provided on the **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA** pins of SARA-G350 modules (1.8 V, PCM & Normal I2S modes, master, fixed sample rate) and LISA-U120/U130 and all LISA-U2 series except LISA-U200-00S modules (1.8 V, PCM & Normal I2S modes, master & slave, configurable sample rate), and it is provided on the **PCM_DO**, **PCM_DI**, **PCM_CLK**, **PCM_SYNC** pins of LISA-C2 series modules (1.8 V, PCM): the same compatible external circuit can be implemented according to external digital audio device capabilities.

Additional digital audio interface is provided on **I2S1_TXD**, **I2S1_RXD**, **I2S1_CLK**, **I2S1_WA** pins of all LISA-U2 series except LISA-U200-00S (1.8 V, PCM & Normal I2S modes, master & slave, configurable sample rate).

SARA-G300/G310, LISA-U100/U110, LISA-U200-00S modules do not provide digital audio interfaces.

For further details regarding digital audio interfaces characteristics, usage, settings refer to the relative module datasheet [1], [3], [4], [5], System Integration Manual 1.10.2, 2.6.2, [6], [7], and AT commands manual [2], [8].

A.4.7 GPIO pins

The same compatible external circuit can be implemented for SARA-G350 and LISA series: four 1.8 V GPIOs are provided by SARA-G350 modules, providing the same functionalities as LISA series modules except Module Status and Operating Mode Indications. SIM detection function is provided by the **SIM_DET** pin on SARA-G3 series modules instead of the **GPIO5** pin on LISA-U series modules.

SARA-G300 and SARA-G310 modules do not provide GPIOs.

A.4.8 Reserved pins

SARA-G3 series modules **RSVD** pin 33 must be connected to ground as LISA series modules **RSVD** pin 5.

A.4.9 Pin-out comparison between LISA and SARA

Table 41 summarizes the pin electrical differences between LISA and SARA wireless modules.

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
Power						
VCC	51-53	Normal op. range: 3.35 V – 4.5 V Extended op. range: 3.00 V – 4.5 V High pulse current due to GSM TDMA	61-63	Normal op. range: 3.3 V – 4.4 V Extended op. range: Not applicable No high pulse current due to CDMA	Normal op. range: 3.4 V – 4.2 V Extended op. range: 3.1 V – 4.2 V High pulse current due to GSM TDMA	Normal op. range: 3.3 V – 4.4 V Extended op. range: 3.1 V – 4.5 V High pulse current due to GSM TDMA
V_BCKP	2	Output characteristics: 2.3 V typ, 2 mA max Input op. range: 1.0 V – 2.4 V	2	Not Available	Output characteristics: 2.3 V typ, 3 mA max Input op. range: 1.0 V – 2.5 V	Output characteristics: 1.8 V typ, 3 mA max Input op. range: 1.0 V – 1.9 V
V_INT	4	Output characteristics: 1.8 V typ, 50 mA max	4	Output characteristics: 1.8 V typ, 50 mA max	Output characteristics: 1.8 V typ, 50 mA max	Output characteristics: 1.8 V typ, 50 mA max
Antenna						
ANT	56	RF input/output for Tx/Rx antenna	68	RF input/output for Tx/Rx antenna	RF input/output for Tx/Rx antenna	RF input/output for main Tx/Rx antenna
ANT_DIV		Not Available	74	Not Available	Not Available	LISA-U230 only: RF input for Rx diversity antenna
ANT_DET	62	SARA-G350 only: Input for antenna detection circuit		Not Available	Internal antenna detection circuit	Internal antenna detection circuit
System						
PWR_ON	15	No internal pull-up L-level: -0.10 V – 0.65 V H-level: 2.00 V – 4.50 V ON L-level time: 5 ms min OFF L-level pulse time: Not Available	19	180 kΩ internal pull-up L-level: -0.30 V – 0.30 V H-level: 2.00 V – 4.70 V ON L-level pulse time: 150 ms min OFF L-level pulse time: Not Available	No internal pull-up L-level: -0.30 V –0.65 V H-level: 2.00 V – 4.50 V ON L-level pulse time: 5 ms min OFF L-level pulse time: Not Available	No internal pull-up L-level: -0.30 V – 0.65 V H-level: 1.50 V – 4.40 V ON L-level pulse time: 50 µs min / 80 µs max OFF L-level pulse time: Not Available
RESET_N	18	Internal diode & pull-up L-level: -0.30 V – 0.30 V H-level: 2.00 V – 4.70 V Reset L-level pulse time: 50 ms min (SARA-G350) 3 s min (SARA-G300/G310)	22	550 Ω internal pull-up L-level: -0.30 V – 0.63 V H-level: 1.32 V – 2.10 V Reset L-level pulse time: 300 ms min	10 kΩ internal pull-up L-level: -0.30 V – 0.65 V H-level: 1.69 V – 2.48 V Reset L-level pulse time: 50 ms min	10 kΩ internal pull-up L-level: -0.30 V – 0.51 V H-level: 1.32 V – 2.01 V Reset L-level pulse time: 50 ms min
EXT32K	31	SARA-G300/G310: 32 kHz input for RTC & low power idle mode SARA-G350: Internal 32 kHz for RTC & low power idle mode		Not Available	Internal 32 kHz for RTC & low power idle mode	Internal 32 kHz for RTC & low power idle mode
SIM						
SIM_CLK	38	1.8V / 3V SIM clock	47	1.8V / 3V SIM clock (upcoming FW releases)	1.8V / 3V SIM clock	1.8V / 3V SIM clock
SIM_IO	39	1.8V / 3V SIM data Internal 4.7k pull-up	48	1.8V / 3V SIM data (upcoming FW releases) Internal 10k pull-up	1.8V / 3V SIM data Internal 4.7k pull-up	1.8V / 3V SIM data Internal 4.7k pull-up
SIM_RST	40	1.8V / 3V SIM reset	49	1.8V / 3V SIM reset (upcoming FW releases)	1.8V / 3V SIM reset	1.8V / 3V SIM reset
VSIM	41	1.8V / 3V SIM supply	50	1.8V / 3V SIM supply (upcoming FW releases)	1.8V / 3V SIM supply	1.8V / 3V SIM supply
SIM_DET	42	1.8 V, SIM detect input Inner pull-down: 103 µA		Not Available	Provided by GPIO5: 1.8 V, SIM detect input Inner pull-down: 55 µA	Provided by GPIO5: 1.8 V, SIM detect input Inner pull-down: 200 µA

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
UART						
DSR	6	1.8 V, DSR output Driver strength: 6 mA	9	Not Available	1.8 V, DSR output Driver strength: 4 mA	1.8 V, DSR output Driver strength: 1 mA
RI	7	1.8 V, RI output Driver strength: 6 mA	10	1.8 V, RI output Driver strength: 6 mA	1.8 V, RI output Driver strength: 4 mA	1.8 V, RI output Driver strength: 2 mA
DCD	8	1.8 V, DCD output Driver strength: 6 mA	11	Not Available	1.8 V, DCD output Driver strength: 4 mA	1.8 V, DCD output Driver strength: 2 mA
DTR	9	1.8 V, DTR input Internal pull-up: -55 µA	12	Not Available	1.8 V, DTR input Internal pull-up: -110 µA	1.8 V, DTR input Internal pull-up: -125 µA
RTS	10	1.8 V, Flow ctrl input Internal pull-up: -31 µA	13	1.8 V, Flow ctrl input Internal pull-up: -30 µA	1.8 V, Flow ctrl input Internal pull-up: -60 µA	1.8 V, Flow ctrl input Internal pull-up: -240 µA
CTS	11	1.8 V, Flow ctrl output Driver strength: 6 mA	14	1.8 V, Flow ctrl output Driver strength: 4 mA	1.8 V, Flow ctrl output Driver strength: 4 mA	1.8 V, Flow ctrl output Driver strength: 6 mA
TXD	12	1.8 V, Data input Internal pull-up: -102 µA	15	1.8 V, Data input Internal pull-up: -30 µA	1.8 V, Data input Internal pull-up: -60 µA	1.8 V, Data input Internal pull-up: -240 µA
RXD	13	1.8 V, Data output Driver strength: 5 mA	16	1.8 V, Data output Driver strength: 4 mA	1.8 V, Data output Driver strength: 4 mA	1.8 V, Data output Driver strength: 6 mA
UART AUX						
TXD_AUX	29	1.8 V, Data input Internal pull-up: -102 µA		Not Available	Not Available	Not Available
RXD_AUX	28	1.8 V, Data output Driver strength: 5 mA		Not Available	Not Available	Not Available
USB						
VUSB_DET		Not Available	18	5 V, Supply detection	5 V, Supply detection	5 V, Supply detection
USB_D-		Not Available	26	Full-Speed USB 2.0	High-Speed USB 2.0	High-Speed USB 2.0
USB_D+		Not Available	27	Full-Speed USB 2.0	High-Speed USB 2.0	High-Speed USB 2.0
SPI						
SPI_SCLK		Not Available	55	Not Available	1.8 V, Clock input Inner pull-down: 100 µA	1.8 V, Clock input Inner pull-down: 200 µA
SPI_MOSI		Not Available	56	Not Available	1.8 V, Data input Internal pull-up: -220 µA	1.8 V, Data input Internal pull-up: -240 µA
SPI_MISO		Not Available	57	Not Available	1.8 V, Data output Driver strength: 2.5 mA	1.8 V, Data output Driver strength: 6 mA
SPI_SRDY		Not Available	58	Not Available	1.8 V, Flow ctrl output Driver strength: 4 mA	1.8 V, Flow ctrl output Driver strength: 6 mA
SPI_MRDY		Not Available	59	Not Available	1.8 V, Flow ctrl input Inner pull-down: 55 µA	1.8 V, Flow ctrl input Inner pull-down: 200 µA
DDC (I^2C)						
SCL	27	SARA-G350 only: 1.8 V, open drain Driver strength: 3 mA	45	1.8 V, open drain (upcoming FW releases)	1.8 V, open drain Driver strength: 1 mA	1.8 V, open drain Driver strength: 1 mA LISA-U200-00S: N.A.
SDA	26	SARA-G350 only: 1.8 V, open drain Driver strength: 3 mA	46	1.8 V, open drain (upcoming FW releases)	1.8 V, open drain Driver strength: 1 mA	1.8 V, open drain Driver strength: 1 mA LISA-U200-00S: N.A.
Audio						
Analog						
MIC_BIAS	46	SARA-G350 only: 2.2 V supply output for external microphone		Not Available	Not Available	Not Available
MIC_GND	47	SARA-G350 only: Local ground sense for external microphone		Not Available	Not Available	Not Available
MIC_P	49	SARA-G350 only: Differential input (+) No internal capacitor for DC blocking	40	Differential input (+) 100 nF internal capacitor for DC blocking	LISA-U120/U130 only: Differential input (+) 100 nF internal capacitor for DC blocking	Not Available

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
MIC_N	48	SARA-G350 only: Differential input (-) No internal capacitor for DC blocking	39	Differential input (-) 100 nF internal capacitor for DC blocking	LISA-U120/U130 only: Differential input (-) 100 nF internal capacitor for DC blocking	Not Available
SPK_P	44	SARA-G350 only: Differential output (+) 16 ohm load capable	53	Differential output (+) 32 ohm load capable	LISA-U120/U130 only: Differential output (+) 16 ohm load capable	Not Available
SPK_N	45	SARA-G350 only: Differential output (-) 16 ohm load capable	54	Differential output (-) 32 ohm load capable	LISA-U120/U130 only: Differential output (-) 16 ohm load capable	Not Available
Digital						
I2S_TXD	35	SARA-G350 only: 1.8 V, Data Out PCM / Normal I2S mode Driver strength: 5 mA	42	PCM_DO: 1.8 V, PCM Data Out	LISA-U120/U130 only: 1.8 V, Data Out PCM / Normal I2S mode Driver strength: 2.5 mA	1.8 V, Data Out PCM / Normal I2S mode Driver strength: 2 mA LISA-U200-00S: N.A.
I2S_RXD	37	SARA-G350 only: 1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 103 µA	44	PCM_DI: 1.8 V, PCM Data In	LISA-U120/U130 only: 1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 100 µA	1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 200 µA LISA-U200-00S: N.A.
I2S_WA	34	SARA-G350 only: 1.8 V, Word align. Out Fixed frequency Driver strength: 6 mA	41	PCM_SYNC: 1.8 V, PCM Sync Out	LISA-U120/U130 only: 1.8 V, Word align. In/Out Configurable frequency Inner pull-down: 100 µA Driver strength: 2.5 mA	1.8 V, Word align. In/Out Configurable frequency Inner pull-down: 200 µA Driver strength: 2 mA LISA-U200-00S: N.A.
I2S_CLK	36	SARA-G350 only: 1.8 V, Clock Out Fixed frequency Driver strength: 5 mA	43	PCM_CLK: 1.8 V, PCM Clock Out	LISA-U120/U130 only: 1.8 V, Clock In/Out Configurable frequency Inner pull-down: 100 µA Driver strength: 2.5 mA	1.8 V, Clock In/Out Configurable frequency Inner pull-down: 200 µA Driver strength: 2 mA LISA-U200-00S: N.A.
I2S1_WA		Not Available	54	Not Available	Not Available	1.8 V, Data Out PCM / Normal I2S mode Driver strength: 1 mA LISA-U200-00S: N.A.
I2S1_TXD		Not Available	40	Not Available	Not Available	1.8 V, Data In PCM / Normal I2S mode Inner pull-down: 150 µA LISA-U200-00S: N.A.
I2S1_CLK		Not Available	53	Not Available	Not Available	1.8 V, Word align. In/Out Configurable frequency Inner pull-down: 150 µA Driver strength: 1 mA LISA-U200-00S: N.A.
I2S1_RXD		Not Available	39	Not Available	Not Available	1.8 V, Clock In/Out Configurable frequency Inner pull-down: 150 µA Driver strength: 1 mA LISA-U200-00S: N.A.
Other						
CODEC_CLK		Not Available	52	Not Available	Not Available	1.8 V, 13/26 MHz Out Driver strength: 4 mA LISA-U200-00S: N.A.
GPIO						
GPIO1	16	SARA-G350 only: 1.8 V, configurable GPIO Default: Pad disabled Driver strength: 6 mA Inner pull-down: 51 µA	20	1.8 V, configurable GPIO Default: Pad disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: Pad disabled Driver strength: 1 mA Inner pull-down: 100 µA	1.8 V, configurable GPIO Default: Pad disabled Driver strength: 6 mA Inner pull-down: 200 µA

Pin Name	N°	SARA-G3 series	N°	LISA-C2 series	LISA-U1 series	LISA-U2 series
GPIO2	23	SARA-G350 only: 1.8 V, configurable GPIO Default: GPS supply ena. Driver strength: 6 mA Inner pull-down: 51 µA	21	1.8 V, configurable GPIO Default: Pad disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: GPS supply en. Driver strength: 1 mA Inner pull-down: 85 µA	1.8 V, configurable GPIO Default: GPS supply en. Driver strength: 1 mA Inner pull-down: 150 µA
GPIO3	24	SARA-G350 only: 1.8 V, configurable GPIO Default: GPS data ready Driver strength: 5 mA Inner pull-down: 27 µA	23	1.8 V, configurable GPIO Default: Pad disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: GPS data ready Driver strength: 4 mA Inner pull-down: 55 µA	1.8 V, configurable GPIO Default: GPS data ready Driver strength: 6 mA Inner pull-down: 200 µA
GPIO4	25	SARA-G350 only: 1.8 V, configurable GPIO Default: GPS RTC shar. Driver strength: 6 mA Inner pull-down: 51 µA	24	1.8 V, configurable GPIO Default: Pad disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: GPS RTC sharing (4.7 k external pull-down required for RTC sharing) Driver strength: 4 mA Inner pull-down: 55 µA	1.8 V, configurable GPIO Default: GPS RTC sharing Driver strength: 6 mA Inner pull-down: 200 µA
GPIO5		Not Available	51	1.8 V, configurable GPIO Default: Pad disabled Driver strength: 4 mA Inner pull-down: 30 µA	1.8 V, configurable GPIO Default: SIM detection Driver strength: 2.5 mA Inner pull-down: 55 µA	1.8 V, configurable GPIO Default: SIM detection Driver strength: 6 mA Inner pull-down: 200 µA
GPIO6		Not Available	39	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_RXD Driver strength: 1 mA Inner pull-down: 150 µA
GPIO7		Not Available	40	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_TXD Driver strength: 1 mA Inner pull-down: 150 µA
GPIO8		Not Available	53	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_CLK Driver strength: 1 mA Inner pull-down: 150 µA
GPIO9		Not Available	54	Not Available	Not Available	1.8 V, configurable GPIO Default: I2S1_WA Driver strength: 1 mA Inner pull-down: 150 µA
GPIO10		Not Available	55	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_SCLK Driver strength: 6 mA Inner pull-down: 200 µA
GPIO11		Not Available	56	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_MOSI Driver strength: 6 mA Inner pull-down: 200 µA
GPIO12		Not Available	57	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_MISO Driver strength: 6 mA Inner pull-down: 200 µA
GPIO13		Not Available	58	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_SRDY Driver strength: 6 mA Inner pull-down: 200 µA
GPIO14		Not Available	59	Not Available	Not Available	1.8 V, configurable GPIO Default: SPI_MRDY Driver strength: 6 mA Inner pull-down: 200 µA

Table 41: Summary of pin differences and compatibility level among modules

B Glossary

3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
AP	Application Processor
AT	AT Command Interpreter Software Subsystem, or attention
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DDC	Display Data Channel interface
DL	Down-link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTM	Dual Transfer Mode
DTR	Data Terminal Ready
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
ESR	Equivalent Series Resistance
FEM	Front End Module
FOAT	Firmware Over AT commands
FTP	File Transfer Protocol
FTPS	FTP Secure
FW	Firmware
GMSK	Gaussian Minimum Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HF	Hands-free
HTTP	HyperText Transfer Protocol
HTTPS	Hypertext Transfer Protocol over Secure Socket Layer
HW	Hardware
I/Q	In phase and Quadrature

I^2C	Inter-Integrated Circuit interface
I^2S	Inter IC Sound interface
IP	Internet Protocol
LCC	Leadless Chip Carrier
LDO	Low-Dropout
LGA	Land Grid Array
LNA	Low Noise Amplifier
M2M	Machine-to-Machine
MCS	Modulation Coding Scheme
N/A	Not Applicable
N.A.	Not Available
PA	Power Amplifier
PCM	Pulse Code Modulation
PCN / IN	Product Change Notification / Information Note
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PSRAM	Pseudo-Static RAM
PWM	Pulse Width Modulation
RF	Radio Frequency
RI	Ring Indicator
RTC	Real Time Clock
RTS	Request To Send
SAW	Surface Acoustic Wave
SIM	Subscriber Identification Module
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SPI	Serial Peripheral Interface
SRF	Self Resonant Frequency
TBD	To Be Defined
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TP	Test-Point
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
UTRA	UMTS Terrestrial Radio Access
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio

Related documents

[1] u-blox SARA-G3 series Data Sheet, Docu No GSM.G2-HW-12001

[2] u-blox AT Commands Manual, Docu No WLS-SW-11000

[3] u-blox LISA-C200 series Data Sheet, Docu No CDMA-2X-11001

[4] u-blox LISA-U1 series Data Sheet, Docu No 3G.G2-HW-10001

[5] u-blox LISA-U2 series Data Sheet, Docu No 3G.G3-HW-11004

[6] u-blox LISA-C200 & FW75-C200 System Integration Manual, Docu No CDMA-2X-11004

[7] u-blox LISA-U series System Integration Manual, Docu No 3G.G2-HW-10002

[8] u-blox C200 AT Commands Manual, Docu No CDMA-2X-11002

[9] ITU-T Recommendation V.24, 02-2000. List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en

[10] 3GPP TS 27.007 – AT command set for User Equipment (UE) (Release 1999)

[11] 3GPP TS 27.005 – Use of Data Terminal Equipment – Data Circuit terminating; Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)

[12] 3GPP TS 27.010 – Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)

[13] I2C-Bus Specification Version 2.1 Philips Semiconductors (January 2000), http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf

[14] 3GPP TS 51.010-2 – Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS)

[15] CENELEC EN 61000-4-2 (2001): "Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test".

[16] ETSI EN 301 489-1 V1.8.1: "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements"

[17] ETSI EN 301 489-7 V1.3.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 7: Specific conditions for mobile and portable radio and ancillary equipment of digital cellular radio telecommunications systems (GSM and DCS)"

[18] ETSI EN 301 489-24 V1.4.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment"

[19] 3GPP TS 26.267 V10.0.0 – eCall Data Transfer; In-band modem solution; General description (Rel. 10)

[20] Multiplexer Implementation Application Note, Docu No WLS-CS-11002

[21] GPS Implementation Application Note, Docu No GSM.G1-CS-09007

[22] Firmware Update Application Note, Docu No WLS-CS-11001

[23] 3GPP TS 23.060 – Technical Specification Group Services and System Aspects; General Packet Radio Service (GPRS); Service description

[24] End user test Application Note, Docu No WLS-CS-12002

[25] u-blox Package Information Guide, Docu No GPS-X-11004

[26] BS EN 16062:2011 – Intelligent transport systems – eSafety – eCall high level application requirements

[27] ETSI TS 122 101 V8.7.0 – Service aspects; Service principles (3GPP TS 22.101 v.8.7.0 Rel. 8)

Some of the above documents can be downloaded from u-blox web-site (http://www.u-blox.com).

Revision history

Revision	Date	Name	Status / Comments
-	Oct. 30, 2012	sses	Initial Release
1	Mar. 28, 2013	sses	Updated suggested paste mask Updated current consumption description Updated voice-band processing system block diagram Updated DDC (I^2C) application circuit for 3V u-blox GPS/GNSS receivers

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