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VERA-P1 series

Host-based V2X transceiver module

Data Sheet

Abstract

This technical data sheet describes the VERA-P1 series transceiver module that enables development of electronics for Vehicle-to-Everything (V2X) communication systems. The VERA-P1 series includes an integrated MAC/LLC/Baseband processor and the required RF front-end components. It is connected to a host processor through a USB or SPI interface.

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Engineering Sample	Advance Information	Data based on early testing. Revised and supplementary data will be published later.
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Mass Production / End of Life	Production Information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Firmware version	PCN reference	Product status
VERA-P173	VERA-P173-00A-00	N/A	N/A	Engineering Samples
VERA-P174	VERA-P174-00A-00	N/A	N/A	Engineering Samples

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1 Functional description

1.1 Overview

The VERA-P1 series are compact, embedded transceiver modules that enables development of electronics for Vehicle-to-Everything (V2X) communication systems. These automotive grade modules are designed for applications such as traffic safety, intelligent traffic management and entertainment. The modules can be used for both in-vehicle units (OBU - On Board Unit) and infrastructure (RSU - Road Side Unit). They provide superior performance compared to V2X systems based on consumer-grade Wi-Fi chipsets, especially at high vehicle speeds and in non-line-of-sight (NLOS) conditions.

The VERA-P1 series includes an integrated MAC/LLC/Baseband processor and the required RF front-end components. The module is connected to a host processor through USB or SPI interface. Both interfaces can be used for data communication and firmware download.

1.2 Product features

Model	Radio			Interfaces				Power	Features			Grade		
	802.11p	Max output power at antenna pin	Antenna type	USB 2.0	GPIO	1PPS	SPI	Power supply: 3.3 V and 5.0 V	Antenna diversity	Single channel operation	Concurrent dual-channel operation	Standard	Professional	Automotive
VERA-P173	•	23 dBm	2p	•	•	•	•	•	•	•				•
VERA-P174	•	23 dBm	2p	•	•	•	•	•	D	•	D			•

2p = Two antenna pins / D = Can be configured by the user as dual-channel or diversity

Table 1: VERA-P1 series main features summary

1.3 Block diagram

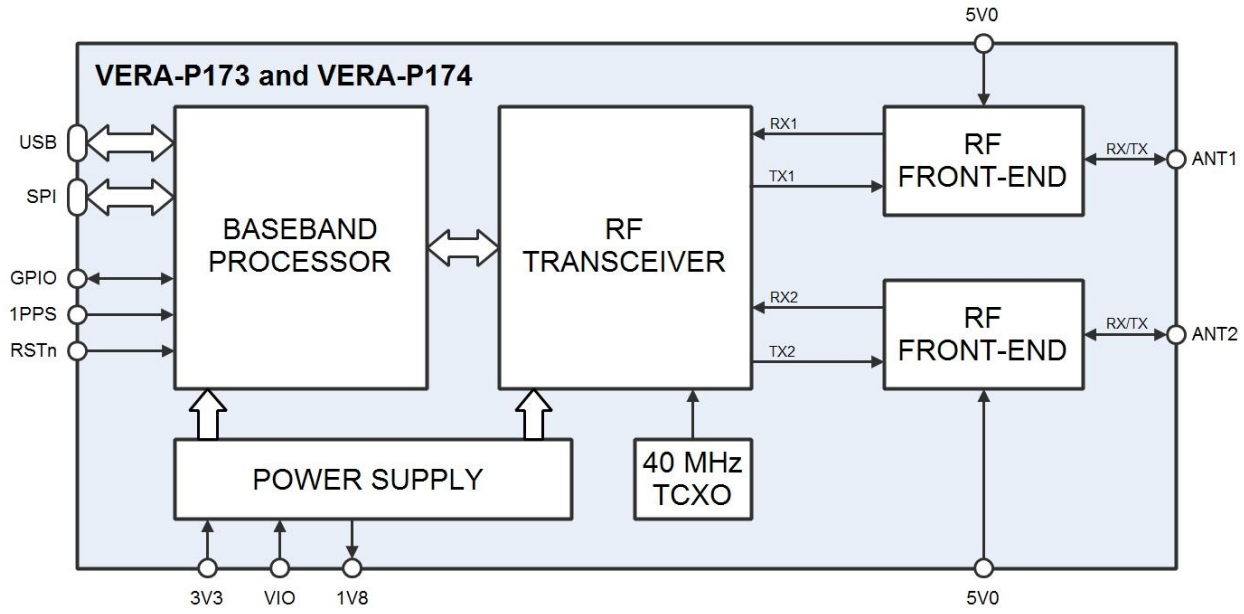


Figure 1: Block diagram of VERA-P173 and VERA-P174

1.4 Product description

Model	Description
VERA-P173	Single channel, antenna diversity, two antennas
VERA-P174	Dual channel or single channel with antenna diversity, two antennas

Table 2: Product description

1.5 Supported features

- Compliance with WAVE and ETSI ITS G5 for US and Europe operations
- USB and SPI[1] host interfaces
- Frequency band 5.850 – 5.925 MHz (channels 172, 174, 176, 178, 180, 182, 184)
- Channel bandwidth 10 MHz[2]
- Data rates 3, 4.5, 6, 9, 12, 18, 24, 27 Mbps
- Antenna diversity (VERA-P173, VERA-P174) – CDD for TX and MRC for RX mode
- TX output power from 0 to +23 dBm (Class C), RX sensitivity -98 dBm at 3 Mbps
- Power supply 3.3 V and 5.0 V, 5 W
- Operation temperature -40 °C to +95 °C
- Dimensions 29.6 x 24.8 x 3.5 mm

1 SPI is not recommended as the main host interface for communication due to performance limitations.
2 Support for 20 MHz mode is planned for future firmware releases subject to certain limitations, as the requirements for 20 MHz operation have not been fully specified.

2 Host interfaces

2.1 USB interface

The VERA-P1 series module supports a USB 2.0 high-speed interface for firmware loading (booting) and high speed data transfer (> 200 Mbps). The USB interface of the module is powered with 3.3 V supply voltage. The module acts as a device on the USB bus.

2.2 SPI interface

The VERA-P1 series module supports an SPI interface for firmware loading (booting) and data communication. Firmware can be loaded by the host processor while the module operates as a slave or from the FLASH memory while the module is in the master mode. The interface is capable of full-duplex operation in master or slave mode. The maximum clock rate is 50 MHz in master mode, and 25 MHz in slave mode[3].

⚠ Due to performance limitations, it is recommended not to use the SPI interface as the main host interface for communication and operation of the module.

3 SPI host interface for data communication in slave mode is tested only with 15 MHz clock rate.

3 Pin Definition

3.1 Pin description

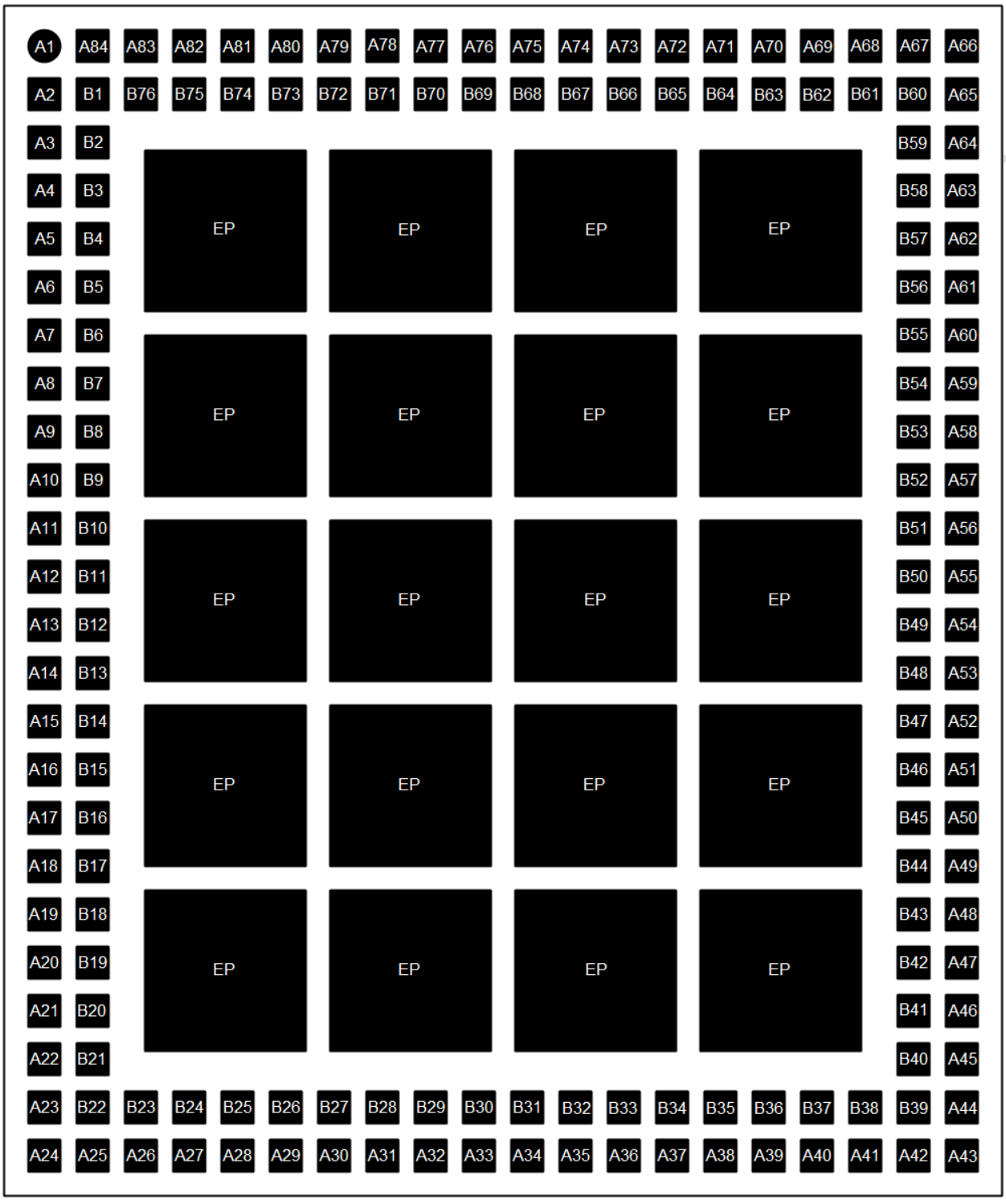


Figure 2: Pin allocation (top view)

No.	Name	Pin type	Power Domain	Description
A1	GND	Ground	-	Ground
A2	GND	Ground	-	Ground
A3	RSTn	I	VIO	Module Reset, has internal pull-up 100k to VIO
A4	GND	Ground	-	Ground
A5	3V3	Power	-	Baseband/Radio supply
A6	GND	Ground	-	Ground
A7	NC	-	-	Leave unconnected
A8	VIO	Power	-	I/O voltage (1.8/2.5/3.3V), in case of 1.8V pin 8 can get supply from pin B7
A9	GND	Ground	-	Ground
A10	NC	-	-	Leave unconnected
A11	GND	Ground	-	Ground
A12	NC	-	-	Leave unconnected
A13	NC	-	-	Leave unconnected
A14	NC	-	-	Leave unconnected
A15	NC	-	-	Leave unconnected
A16	NC	-	-	Leave unconnected
A17	NC	-	-	Leave unconnected
A18	GND	Ground	-	Ground
A19	5V0_A1	Power	-	Antenna 1 radio front-end supply
A20	GND	Ground	-	Ground
A21	GPIO2_11	I/O	1V8	GPIO2_11
A22	GPIO2_12	I/O	1V8	GPIO2_12
A23	GND	Ground	-	Ground
A24	GND	Ground	-	Ground
A25	GND	Ground	-	Ground
A26	ANT1	RF I/O	-	Antenna 1
A27	GND	Ground	-	Ground
A28	GND	Ground	-	Ground
A29	NC	-	-	Leave unconnected
A30	GND	Ground	-	Ground
A31	GND	Ground	-	Ground
A32	NC	-	-	Leave unconnected
A33	GND	Ground	-	Ground
A34	GND	Ground	-	Ground
A35	NC	-	-	Leave unconnected
A36	GND	Ground	-	Ground
A37	GND	Ground	-	Ground
A38	NC	-	-	Leave unconnected
A39	GND	Ground	-	Ground
A40	GND	Ground	-	Ground
A41	ANT2	RF I/O	-	Antenna 2

No.	Name	Pin type	Power Domain	Description
A42	GND	Ground	-	Ground
A43	GND	Ground	-	Ground
A44	GND	Ground	-	Ground
A45	5V0_A2	Power	-	Antenna 2 radio front-end supply
A46	GND	Ground	-	Ground
A47	SPI_MOSI	I/O	VIO	SPI Bus
A48	SPI_MISO	I/O	VIO	SPI Bus
A49	MOD_IO_SPARE	I/O	VIO	Optional SPI CS, GPIO1_10
A50	GND	Ground	-	Ground
A51	NC	-	-	Leave unconnected
A52	NC	-	-	Leave unconnected
A53	NC	-	-	Leave unconnected
A54	NC	-	-	Leave unconnected
A55	NC	-	-	Leave unconnected
A56	NC	-	-	Leave unconnected
A57	GND	Ground	-	Ground
A58	NC	-	-	Leave unconnected
A59	NC	-	-	Leave unconnected
A60	NC	-	-	Leave unconnected
A61	GND	Ground	-	Ground
A62	USB_DN	I/O	-	USB Bus
A63	USB_DP	I/O	-	USB Bus
A64	USB_VBUS	I	-	USB VBUS detect input
A65	GND	Ground	-	Ground
A66	GND	Ground	-	Ground
A67	GND	Ground	-	Ground
A68	GPIO1_12	I/O	VIO	UART1_RX
A69	GND	Ground	-	Ground
A70	1PPS	I	1V8	One pulse per second input
A71	GND	Ground	-	Ground
A72	NC	-	-	Leave unconnected
A73	NC	-	-	Leave unconnected
A74	NC	-	-	Leave unconnected
A75	NC	-	-	Leave unconnected
A76	NC	-	-	Leave unconnected
A77	GND	Ground	-	Ground
A78	GPIO1_14	I/O	VIO	UART2_RX
A79	BOOT_0	I	VIO	Boot mode configuration
A80	NC	-	-	Leave unconnected
A81	GND	Ground	-	Ground

No.	Name	Pin type	Power Domain	Description
A82	NC	-	-	Leave unconnected
A83	NC	-	-	Leave unconnected
A84	GND	Ground	-	Ground
B1	NC	-	-	Leave unconnected
B2	NC	-	-	Leave unconnected
B3	GND	Ground	-	Ground
B4	3V3	Power	-	Baseband/Radio supply
B5	GND	Ground	-	Ground
B6	NC	-	-	Leave unconnected
B7	1V8	O	-	1.8 V supply output, can be connected to pin 8 only as a VIO voltage source
B8	GND	Ground	-	Ground
B9	NC	-	-	Leave unconnected
B10	GND	Ground	-	Ground
B11	NC	-	-	Leave unconnected
B12	NC	-	-	Leave unconnected
B13	NC	-	-	Leave unconnected
B14	NC	-	-	Leave unconnected
B15	NC	-	-	Leave unconnected
B16	NC	-	-	Leave unconnected
B17	GND	Ground	-	Ground
B18	5V0_A1	Power	-	Antenna 1 radio front-end supply
B19	GND	Ground	-	Ground
B20	GPIO2_13	I/O	1V8	GPIO2_13
B21	GPIO2_14	I/O	1V8	GPIO2_14
B22	GND	Ground	-	Ground
B23	GND	Ground	-	Ground
B24	GND	Ground	-	Ground
B25	PA1_EN	I/O	VIO	PA enable for ANT1
B26	NC	-	-	Leave unconnected
B27	LAN1_EN	I/O	VIO	LNA enable for ANT1
B28	GND	Ground	-	Ground
B29	GND	Ground	-	Ground
B30	GND	Ground	-	Ground
B31	GND	Ground	-	Ground
B32	GND	Ground	-	Ground
B33	GND	Ground	-	Ground
B34	LNA2_EN	I/O	VIO	LNA enable for ANT2
B35	NC	-	-	Leave unconnected
B36	PA2_EN	I/O	VIO	PA enable for ANT2
B37	GND	Ground	-	Ground

No.	Name	Pin type	Power Domain	Description
B38	GND	Ground	-	Ground
B39	GND	Ground	-	Ground
B40	5V0_A2	Power	-	Antenna 2 radio front-end supply
B41	GND	Ground	-	Ground
B42	SPI_SCK	I/O	VIO	SPI Bus
B43	SPI_CSn	I/O	VIO	SPI Bus
B44	NC	-	-	Leave unconnected
B45	GND	Ground	-	Ground
B46	NC	-	-	Leave unconnected
B47	NC	-	-	Leave unconnected
B48	NC	-	-	Leave unconnected
B49	NC	-	-	Leave unconnected
B50	NC	-	-	Leave unconnected
B51	NC	-	-	Leave unconnected
B52	GND	Ground	-	Ground
B53	NC	-	-	Leave unconnected
B54	NC	-	-	Leave unconnected
B55	NC	-	-	Leave unconnected
B56	GND	Ground	-	Ground
B57	NC	-	-	Leave unconnected
B58	NC	-	-	Leave unconnected
B59	NC	-	-	Leave unconnected
B60	NC	-	-	Leave unconnected
B61	GPIO1_11	I/O	VIO	UART1_TX
B62	NC	-	-	Leave unconnected
B63	GND	Ground	-	Ground
B64	NC	-	-	Leave unconnected
B65	NC	-	-	Leave unconnected
B66	NC	-	-	Leave unconnected
B67	NC	-	-	Leave unconnected
B68	NC	-	-	Leave unconnected
B69	NC	-	-	Leave unconnected
B70	GND	Ground	-	Ground
B71	BOOT_2	I	VIO	Boot mode configuration, UART2_TX
B72	BOOT_1	I	VIO	Boot mode configuration
B73	NC	-	-	Leave unconnected
B74	GND	Ground	-	Ground
B75	NC	-	-	Leave unconnected
B76	NC	-	-	Leave unconnected
EP	GND	Ground	-	20 Ground/Thermal exposed pads, connect to the ground

Table 3: VERA-P1 series pin description

4 Electrical specification

⚠ Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions section of this document should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ Operating condition ranges define those limits within which the functionality of the device is guaranteed. Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Units
5V0_A1, 5V0_A2	Power supply voltage 5.0 V	-0.3	6.0	V
3V3	Power supply voltage 3.3 V	-0.3	3.9	V
VIO	I/O supply voltage 1.8 V/2.5 V/3.3 V	-0.3	3.9	V
$T_{STORAGE}$	Storage temperature	-40	+95	°C

Table 4: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.

4.2 Operating conditions

Symbol	Parameter	Min.	Typ	Max.	Units
5V0_A1, 5V0_A2	Power supply voltage 5.0 V	4.5	5.0	5.5	V
3V3	Power supply voltage 3.3 V	3.0	3.3	3.6	V
VIO	I/O supply voltage 1.8 V/2.5 V/3.3 V	1.65	1.8	1.95	V
		2.3	2.5	2.8	
		3.0	3.3	3.6	V
T_A	Ambient operating temperature	-40	-	+95	°C
Ripple Noise	Peak-to-peak voltage ripple on 5V0 and 3V3 supply lines.	-	-	10	mV

Table 5: Operating conditions[4]

[4] Min and Max limits apply for T_A = +25 °C.

4.3 Digital pad ratings

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IH}	Input high voltage		0.7*VIO[5]	VIO[1]	V
V_{IL}	Input low voltage		-0.3	0.6[6]	V
V_{HYS}	Input hysteresis		0.18	-	V
V_{OH}	Output high voltage	$I_O$max = 5 mA	VIO-0.4	-	V
V_{OH}	Output low voltage	$I_O$max = -5 mA	-	0.4	V

Table 6: Digital pad ratings

4.4 Peak current consumption

Operation Mode		Peak current typ. (mA)		
		3V3	VIO	5V0_A1, 5V0_A2
Idle		372	0.55	1.7
RX single antenna		382	0.45	30
RX dual antenna (5V0 peak current applies to each RX chain)		461	0.55	30
TX single antenna	+0 dBm	432	0.45	186
	+10 dBm	434	0.45	197
	+20 dBm	437	0.45	273
TX dual antenna (output power and 5V0 peak current apply to each TX chain)	+0 dBm	563	0.55	186
	+10 dBm	565	0.55	197
	+20 dBm	570	0.55	273

Table 7: Peak current consumption (typical values are referenced to T_A = +25 °C, 3V3 = 3.3 V, VIO = 1.8 V, 5V0_A1 = 5V0_A2 = 5.0 V)

☞ The **average** current consumption for full operation mode strongly depends on the RX/TX time ratio and remains within the range between the peak values of RX and TX.

[5] 1PPS pad always use 1.8 V internally generated IO supply regardless of the VIO pad voltage.
[6] RSTn pad internally pulled high to VIO voltage by 100k. During reset it should be below 0.2 V.

4.5 Radio specifications

Parameter	Operation Mode			Specification
RF Frequency Range	802.11p			5.85 – 5.925 GHz
Modulation	802.11p			OFDM
Supported Data Rates	802.11p			3, 4.5, 6, 9, 12, 18, 24, 27 Mbps
Supported Bandwidth	802.11p			10 MHz
Maximum Transmit Power (combined on 2 antennas)	802.11p			23 dBm[7]
Minimum Transmit Power	802.11p			0 dBm
Receiver sensitivity	802.11p	10 MHz, no multipath	3 Mbps	-98 dBm typ.
			4.5 Mbps	-96 dBm typ.
			6 Mbps	-95 dBm typ.
			9 Mbps	-93 dBm typ.
			12 Mbps	-90 dBm typ.
			18 Mbps	-86 dBm typ.
			24 Mbps	-82 dBm typ.
			27 Mbps	-80 dBm typ.
		10 MHz, NLoS (Non-line-of-sight)	3 Mbps	-95 dBm typ.
			4.5 Mbps	-92 dBm typ.
			6 Mbps	-88 dBm typ.
			9 Mbps	-86 dBm typ.
			12 Mbps	-85 dBm typ.
			18 Mbps	-82 dBm typ.
			24 Mbps	Na
			27 Mbps	Na
Receiver maximum operating input level	802.11p			-20 dBm
RSSI accuracy	802.11p	Over temperature range		+/-3 dB
Center frequency and symbol clock tolerance	802.11p			+/-10 ppm
Transmitter spectral flatness	802.11p	All modulation modes		< +/-2 dB
Transmitter center frequency leakage	802.11p			< -15 dB
Transmit power control step size	802.11p			0.5 dB
Transmit power control accuracy	802.11p	Over temperature range		+/-2 dB

Table 8: Radio specifications (values are referenced to T_A = -40 to +95 °C, 3V3 = VIO = 3.3 V, 5V0_A1 = 5V0_A2 = 5.0 V)

Table 9 shows the Highway NLoS (Non-line-of-sight) channel parameters that are used to obtain the receiver sensitivity values in Table 8. This channel was used in RF testing at the third ETSI Plug test (CMS3).

Each tap is faded using Pure Doppler, but the second antenna has a Doppler increased by 11 Hz, which prevents phase synchronization of channels. The RX Power listed in Table 8 refers to the power of Tap 0.

[7] To protect the module against permanent damage caused by overheating, the transmit power is derated at high temperature. The derating depends on the RX/TX time ratio.

The values presented are typical values, measured at +25 °C.

Tap#	Relative Power (dB)	Delay (ns)	Doppler Frequency (Hz)
0	0	0	0
1	-2	200	689
2	-5	433	-492
3	-7	700	886

Table 9: Highway NLoS channel parameters

The adjacent and non-adjacent channel rejection measurements are provided in Table 10 and Table 11 respectively.

Bit rate	Target ACR (dB)	Target opt. enc. ACR (dB)	VERA-P1 typical ACR (dB)
3 Mbps (1/2BPSK)	16	28	37
4.5 Mbps (3/4BPSK)	15	27	33
6 Mbps (1/2QPSK)	13	25	35
9 Mbps (3/4QPSK)	11	23	29
12 Mbps (1/2QAM16)	8	20	29
18 Mbps (3/4QAM16)	4	16	25
24 Mbps (2/3QAM64)	0	12	22
27 Mbps (3/4QAM64)	-1	11	20

Table 10: Adjacent channel rejection

Bit rate	Target ACR (dB)	Target opt. enc. ACR (dB)	VERA-P1 typical ACR (dB)
3 Mbps (1/2BPSK)	32	42	51
4.5 Mbps (3/4BPSK)	31	41	48
6 Mbps (1/2QPSK)	29	39	48
9 Mbps (3/4QPSK)	27	37	45
12 Mbps (1/2QAM16)	24	34	42
18 Mbps (3/4QAM16)	20	30	38
24 Mbps (2/3QAM64)	16	26	34
27 Mbps (3/4QAM64)	15	25	32

Table 11: Non-adjacent channel rejection

Channel	Frequency, GHz
172	5.860
174	5.870
176	5.880
178	5.890
180	5.900
182	5.910
184	5.920

Table 12: Supported channels

5 Mechanical specifications

5.1 Physical dimensions

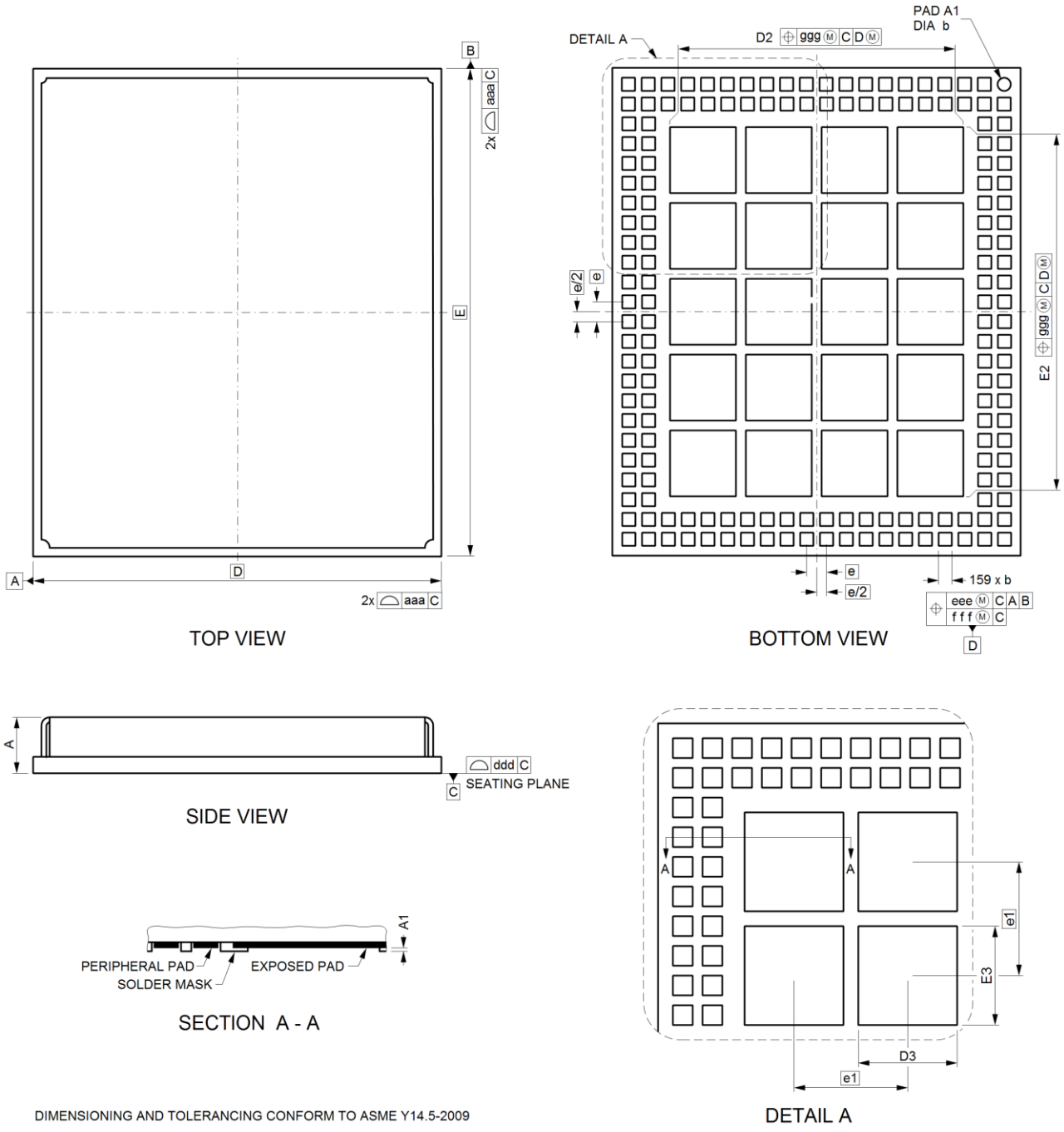


Figure 3: Physical dimensions

Symbol	Description	Millimeters		
		Min.	Nom.	Max.
A	Module Thickness	3.3	3.5	3.7
A1	Vertical distance from the solder mask to the pad surface	0.010	0.020	0.035
b	Width of the peripheral pads	0.70	0.75	0.80
D	Module horizontal dimension	24.8 BSC		
D2	Horizontal dimension of the exposed thermal pads pattern	17.7	17.8	17.9
D3	Horizontal dimension of the individual exposed thermal pad	3.9	4.0	4.1
E	Module vertical dimension	29.6 BSC		
E2	Vertical dimension of the exposed thermal pads pattern	22.3	22.4	22.5
E3	Vertical dimension of the individual exposed thermal pad	3.9	4.0	4.1
e	Pitch of the peripheral pads	1.2 BSC		
E1	Pitch of the individual exposed thermal pads	4.6 BSC		
aaa	Bilateral profile tolerance of the module body		0.2	
ddd	Co-planarity of the module bottom surface (unilateral tolerance)		0.1	
eee	Tolerance of the peripheral pads pattern position		0.2	
fff	Tolerance of the peripheral pads position with respect to each other		0.04	
ggg	Tolerance of the exposed thermal pads pattern position		0.08	

Table 13: VERA-P1 series dimensional references

☞ The “aaa” tolerances +/- 0.2 mm may be exceeded in the corners of the PCB due to the cutting process. In worst case, the outer dimension “D” could reach 25.3 mm.

6 Qualification and approvals

6.1 Approvals[8]

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).
VERA-P1 series V2X modules are RoHS compliant.

6.1.1 European Union regulatory compliance

TBD

6.1.2 FCC compliance

The VERA-P1 series modules comply with Part 95, Subpart L and Part 90, Subpart M of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

⚠ Non authorized modification could void authority to use this equipment. The internal / external antenna(s) used for this module must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the manufacturer's instructions, may cause harmful interference to radio communications.

☞ The outside of final product that contains the VERA-P173 or VERA-P174 module must display in a user accessible area a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: XPYVERAP174" or "Contains FCC ID: XPYVERAP174".

6.1.3 FCC IDs

Model	FCC ID
VERA-P173	XPYVERAP174
VERA-P174	XPYVERAP174

Table 14: FCC IDs for different models of VERA-P1 series

6.1.4 Certification in other countries

TBD

6.2 Approved antennas

Please refer to the *VERA-P1 series antenna reference design [2]* for the essential specifications to be fulfilled in the end-product design to make use of the module's radio type approval. It provides PCB layout details and electrical specifications as well as information about approved antennas.

[8] These approvals are pending.

7 Product handling & soldering

7.1 Packaging

The VERA-P1 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the *u-blox Package Information Guide [1]*.

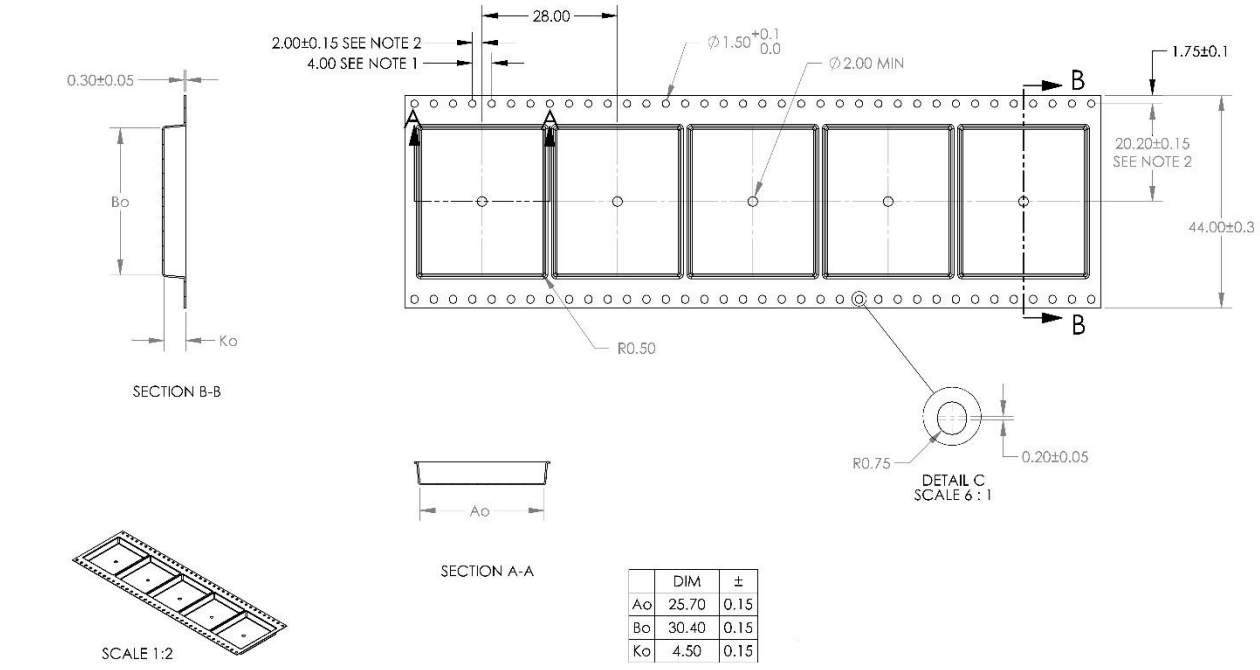
7.1.1 Reels

The VERA-P1 series modules are deliverable in quantities of 250 pieces on a reel. The VERA-P1 series modules are shipped on reel Type A as specified in the *u-blox Package Information Guide [1]*.

7.1.2 Tapes

Figure 4 shows the position and orientation of the VERA-P1 modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 5.

Figure 4: Orientation of VERA-P1 module on tape



	DIM	±
Ao	25.70	0.15
Bo	30.40	0.15
Ko	4.50	0.15

Figure 5: VERA-P1 tape dimensions

7.2 Shipment, storage and handling

For more information regarding shipment, storage and handling see the u-blox Package Information Guide *[1]*.

7.2.1 Moisture sensitivity levels

The VERA-P1 series modules are rated at moisture sensitivity level 3. See moisture sensitive warning label on each shipping bag for detailed information. After opening the dry pack, modules must be mounted within 168 hours in factory conditions of maximum 30 °C/60%RH or must be stored at less than 10%RH. Modules require baking if the humidity indicator card shows more than 10% when read at 23±5°C or if the conditions mentioned above are not met. Please refer to J-STD-033B standard for bake procedure.

7.2.2 Mounting process and soldering recommendations

The VERA-P1 series module is a surface mount module supplied on an 8-layer FR4-type PCB with gold plated connection pins and produced in a lead-free process with a lead-free soldering paste. The wrap page of the PCB is max. 0.75% according to IPC-A-610E. The thickness of solder resist on the host PCB top side and the JODY-W1 bottom side must be considered for the soldering process.

This module is compatible with industrial reflow profile for RoHS/Pb-free solders, Sn96.5/Ag3.0/Cu0.5 solder is a right choice. Use of "No Clean" soldering paste is strongly recommended, cleaning the populated modules is strongly discouraged - residuals under the module cannot be easily removed with any cleaning process. Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pins.

Only a single reflow soldering process is permitted for host boards with the VERA-P1 series modules.
The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Recommendations below should be taken as a starting point guide. In case of basic information necessity, refer to J-STD-020C standard.

Profile feature	Sn-Pb eutectic (Sn63/Pb37)	RoHS/Pb-free (Sn96.5/Ag3.0/Cu0.5)
Ramp up rate (T_{SMAX} to T_P)	3 °C/sec max	3 °C/sec max
Minimum soak temperature (T_{SMIN})	100 °C	150 °C
Maximum soak temperature (T_{SMAX})	150 °C	200 °C
Soak time (ts)	60 - 120 sec	60 - 180 sec
Liquidus temperature (T_L)	183 °C	217 °C
Time above T_L (t_L)	60 - 150 sec	60 - 150 sec
Peak temperature (T_P)	215 – 225 °C	235 – 245 °C
Time within +0 / -5°C of actual TP (tp)	10 - 30 sec	20 - 40 sec
Ramp down rate	6 °C/sec max	6 °C/sec max
Time from 25°C to T_P	6 min max	8 min max

Table 15: Recommended reflow profile

☞ The lowest value of T_P and slower ramp down rate (2 – 3 °C/sec) is preferred.

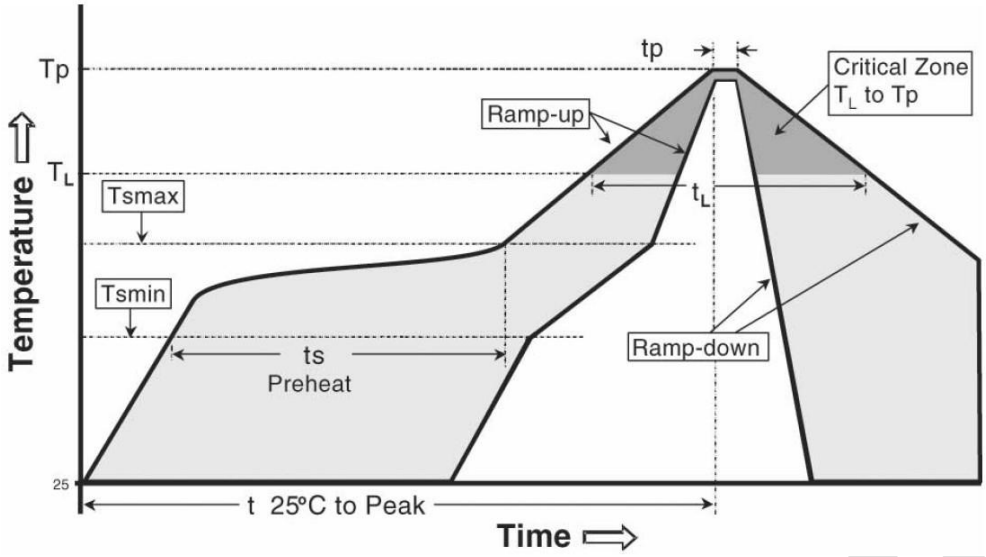


Figure 6: Reflow profile

7.2.3 ESD handling precautions

⚠ VERA-P1 series modules are Electrostatic Sensitive Devices (ESD). Observe precautions for handling! Failure to observe these precautions can result in severe damage to the Wi-Fi receiver!

Wi-Fi transceivers are Electrostatic Sensitive Devices (ESD) and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device

- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10 pF, coax cable ~50-80 pF/m, soldering iron, ...)

- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.

- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).

8 Labeling and ordering information

8.1 Product labeling

The labels of VERA-P1 series include important product information as described in this section.

Figure 7 illustrates the sample label of the VERA-P1 series. A detailed description of the label components are listed in Table 16.

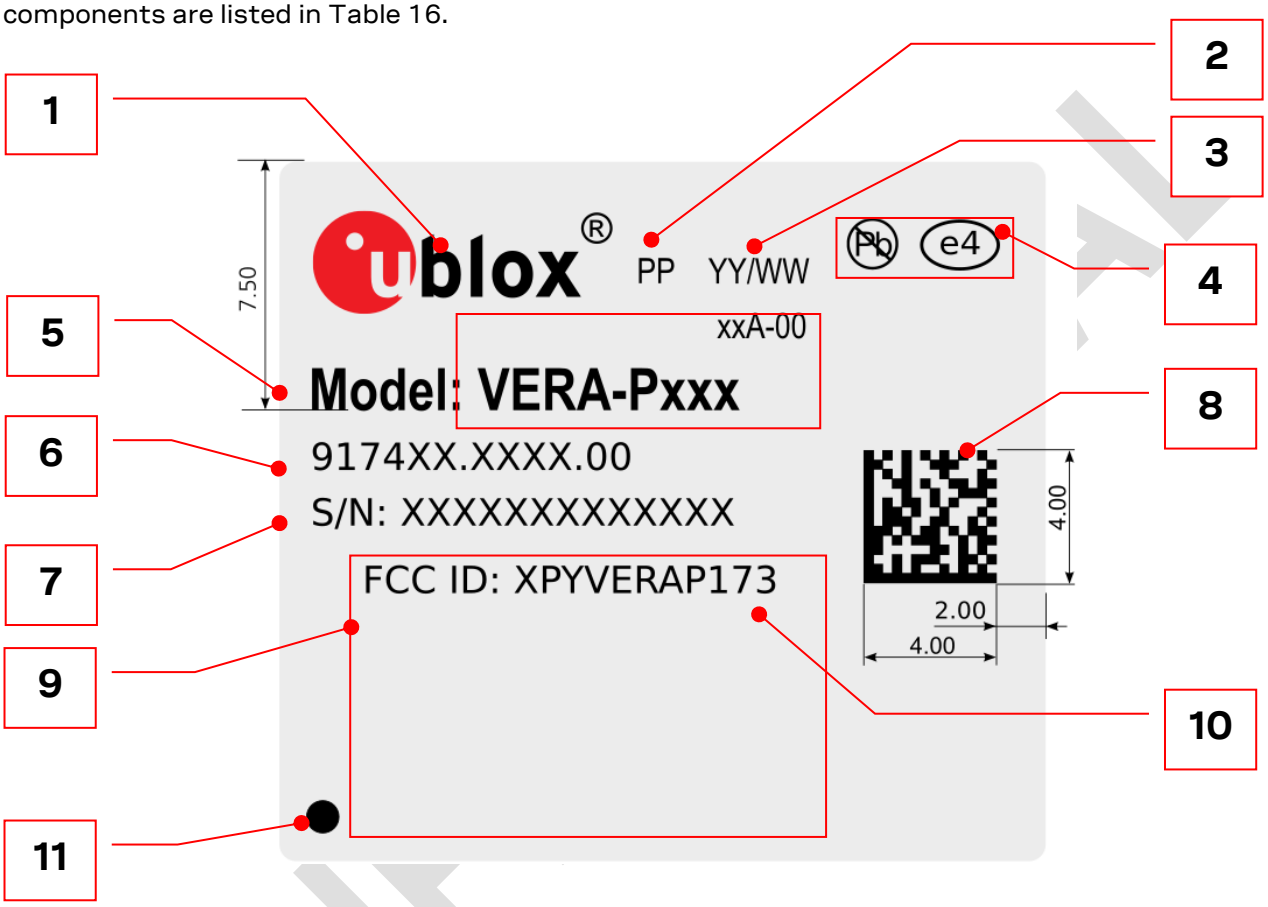


Figure 7: VERA-P1 series - Sample label

Reference	Description
1	Company logo and trademark
2	Panel position number
3	Production date YY/WW (year/week)
4	Pb-Free, Platin Spec IPC-1066/JESD97
5	Type number (format PPPP-TGVV-TTQ-XX), e.g. VERA-P173-00A-00
	"Model:" PPPP-TGVV
	TTQ-XX
6	Datacode
7	Serial number "S/N:" MAC address (Format of MAC address: D4-CA-6E-01-02-03)
8	DataMatrix (product identifier, serial number, datacode) Product identifier: 3 digits Serial number: MAC address Datacode: 4 digits
9	Text box containing approval IDs
10	FCC ID: XPYVERA173 (example)
11	Pin 1 marker

Table 16: VERA-P1 series label description

8.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 17 below details these three different formats:

Format	Structure
Product Name	PPPP-TGVV
Ordering Code	PPPP-TGVV-TTQ
Type Number	PPPP-TGVV-TTQ-XX

Table 17: Product Code Formats

Code	Meaning	Example
PPPP	Form factor	VERA
TG	Platform T – Dominant technology, For example, W: Wi-Fi, B: Bluetooth G – Generation	P1
VV	Variant based on the same platform; range [00…99]	73
TT	Major Product Version	00
Q	Quality grade A: Automotive B: Professional C: Standard	A
XX	Minor product version (not relevant for certification)	00

Table 18: Part identification code

8.3 Ordering codes

Ordering Code	Product name	Product
VERA-P173-00A-00	VERA-P173	VERA-P173 automotive grade module
VERA-P174-00A-00	VERA-P174	VERA-P174 automotive grade module
EVK-VERA-P174-00A	EVK-VERA-P174	Evaluation kit for VERA-P173 and VERA-P174

Table 19: Product ordering codes

☞ Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website.

Appendix

A Glossary

Abbreviation	Definition
COTS	Commercial off-the-shelf
CS	Chip select
ESD	Electrostatic Sensitive Devices
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
GND	Ground
GPIO	General-purpose input/output
IC	Industry Canada
LLC	Logical Link Control
MAC	Media Access Control
nACR	Non-adjacent channel rejection
NLoS	Non-Line-of-Sight
OBU	On Board Unit
OFDM	Orthogonal frequency-division multiplexing
PCB	Printed Circuit Board
RF	Radio Frequency
RSU	Road Side Unit
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
V2X	Vehicle-to-Everything

Table 20: Explanation of the abbreviations and terms used

Related documents

[1] u-blox Package Information Guide, document number UBX-14001652
[2] VERA-P1 series antenna reference design, document number UBX-18022092

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	23-Feb-2017	ishe, kgom	Initial release.
R02	5-May-2017	ddie, kgom	Added VERA-P174 product variant and included block diagram, FCC/IC ID, and ordering code for this variant.
R03	11-Sep-2017	mzes, kgom, ddie	Updated Table 1. Included footnotes in section 1.5. Updated the ordering codes (section 8.3). Added reel size (section 7.1) and tape dimensions (Figure 5).
R04	17-Oct-2017	ddie, kgom	Removed references to VERA-P175 variant. Updated Table 1.
R05	4-June-2018	smay, kgom	Updated total power consumption in section 1.5. Added SPI limitation in section 2.2. Added peak current consumption in Table 7. Extended worst case dimension D in section 5.1. Added position and orientation in section 7.1.2. Added product labeling in section 8.1. Update lowest TX power level. Removed all references to VERA-P171 variant.
R06	22-June-2018	ddie	Added clarification that 23 dBm max output power is the combined output power of two antennas. Added FCC approvals section (6.1.2).

Contact

For complete contact information, visit us at www.u-blox.com.

u-blox Offices

North, Central and South America

u-blox America, Inc.

Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:

Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

Technical Support:

Phone: +1 703 483 3185
E-mail: support@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG

Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.

Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office Australia:

Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support: support_ap@u-blox.com

Regional Office China (Beijing):

Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Chongqing):

Phone: +86 23 6815 1588
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shanghai):

Phone: +86 21 6090 4832
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shenzhen):

Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office India:

Phone: +91 80 405 092 00
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

Regional Office Japan (Osaka):

Phone: +81 6 6941 3660
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Japan (Tokyo):

Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:

Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:

Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com